Practical Virtual Cell Designing Environment

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Abstract— We have developed a novel and practical virtual cell designing environment. For the practical use, the system provides simulators highly calibrated and adaptive to new structure devices and processes; tools for analyzing the effect of process variations on device characteristics or parasite capacitance; and easy-to-use GUI. This environment is used in practical work and has reduced TAT of cell designing to less than one eighth. Furthermore, it has enabled evaluation of even new structured devices.

I. Introduction

The realization of virtual cell designing environment, in which a series of operations from transistor designing to cell verification are done only by computer simulations, is an essential factor for concurrent designing of ULSI. However, the virtual cell environment for practical use requires well-calibrated simulators and an easy-to-use interface for reliable result and efficient operation. This requirement caused the realization of virtual cell environment for practical use very difficult. We have developed a virtual cell environment tolerable for daily work by device engineers. For the use of practical work, the system has following novel points: simulators are highly calibrated with referring measured data stored in a database[1][2] and also very adaptive to new structure devices and new processes since the system is well established for tuning procedures; practical tools for analyzing the effect of process variations on device characteristics or parasite capacitance are provided; to deal with the needs of increasing and spreading simulator users, user-friendly GUI (Graphical User Interface) is implemented on low-cost platforms.

In this paper, after explaining the modules which consist the virtual cell environment, we will present an application example of utilizing this system for predicting the performance of 0.13μm generation MOSFET.

II. Characteristics of the Virtual Cell Designing Environment

Module structure of the virtual cell environment is shown on Fig.1. Electrical characteristics, such as threshold voltage (Vth) and saturation current, and transistor C-V characteristics are simulated with 2D process/device simulators. Interconnect capacitance is calculated with 3D capacitance simulator. SPICE parameters including I-V characteristics, C-V characteristics and interconnect capacitance are extracted from these calculation results and then the circuit characteristics are analyzed.

A. Process/Device Simulation Module

In this module, 2D process and device simulations are performed to extract the electrical and C-V characteristics[3]. The novel points of this module are as follows: (1)Both of process and device simulators are highly calibrated by referring measured data stored in a database, which enables accurate prediction of the effect on device characteristics for variations of process conditions; (2)The effect of process variations on device characteristics can be specified and automatically simulated. Any process parameters, including mask dimension, such as gate mask length and sidewall mask length, can be specified with an easy-to-use GUI. Also, when more than two process vary according to Gauss distribution, the effect can be predicted with less than 1/100 times calculations compared with Monte Carlo method; (3)According to the transistor type of P-ch or N-ch, and characteristics to be calculated, such as Id-Vg, Id-Vd, Cgs-Vg etc., well-calibrated parameters are automatically specified. Furthermore, parameters or mesh structures for new type devices can be efficiently specified with GUI, which assists not only designing work by device engineers but also tuning of simulators by TCAD engineers.

B. Interconnect Capacitance Simulation Module

To extract SPICE parameters including interconnect capacitance and net-list, 3D simulation of interconnect capacitance is performed with this module[4,5,6], with the input of GDS-II formatted mask data. The novel point of this module is that the variation of mask dimension such as magnification and reduction, deviation of its position, and other process parameters such as thickness of the films and permittivity ratio, can be easily specified with GUI and simulated. Fig.2 shows this module being operated. Masks of a buffer cell are shown and an input panel for specifying interconnect thickness is exposed at the upper half of the figure. Input data files for the simu-

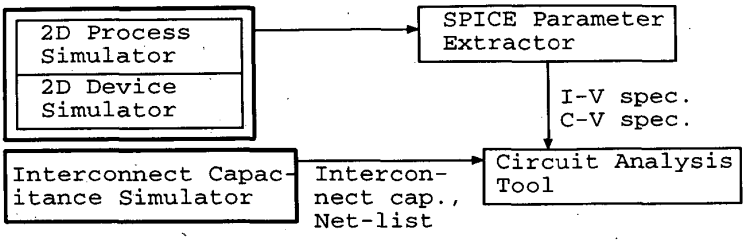

Fig.1 Module structure of the virtual cell design environment

lator, which correspond to the specification are automatically synthesized and then calculated. The lower halves of fig.2 are the result of mask shapes when interconnect width is reduced or magnified by 0.05μm to both X and Y directions. Table 1 shows the comparison of capacitance for each interconnect conditions to the original.

III. Implementation and Use of the System

To deal with the needs of increasing and spreading simulator users, this virtual cell designing environment is used under server-client environment, which enables "remote simulation" on low-cost platforms[7]. Client program, which is GUI program for users' data operation, is written with JAVA. Simulator users access this virtual cell environment from WWW browser via WWW server. This mechanism enables engineers to use the newest program version and reduces the amount of data transfer a lot compared with remote login use.

IV. Application Example

In the development of 0.13μm generation MOSFET device, device characteristics are calculated utilizing the virtual cell designing environment to predict the performance before manufacturing and then compared with the measured characteristics of test chips manufactured with the predicted process conditions. Fig.3 is the cell layout of the tested inverter forming a ring-oscillator for delay and power estimation. An equivalent circuit of it is shown in fig.4. The goal of this simulation is to predict threshold voltage (Vth) roll-off curve and delay vs power characteristics.

Utilizing the virtual cell environment, a series of simulations are performed and SPICE parameters are extracted from the results. Firstly, two dimensional process simulation is performed. Fig.5 shows BF2 distribution, implanted to S/D, to depth direction and fig.6 parallel to surface. Three kinds of implantation energy is simulated to evaluate the effect of it. By using GUI provided in this system, process variations are easily specified, simulated and visualized.

Device simulations are then performed with the result of process simulation. Fig.7 is a graph of junction capac-

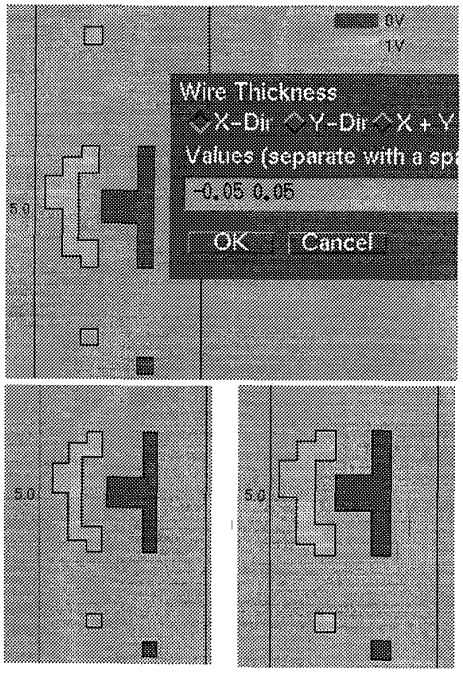

Fig. 2 Original mask for interconnect (upper) and the result of deviating width (lower left: thinner, right: thicker)

Table 1 Effect of interconnect width deviation on interconnect capacitance (unit: F)

Original	1.5433e-15
0.05um Thicker	1.6113e-15
0.05um Thinner	1.4623e-15

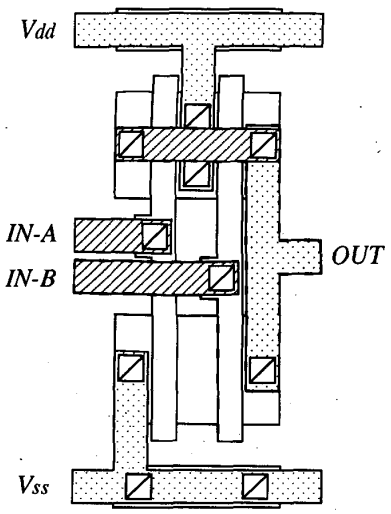

Fig. 3 Cell layout of the tested inverter

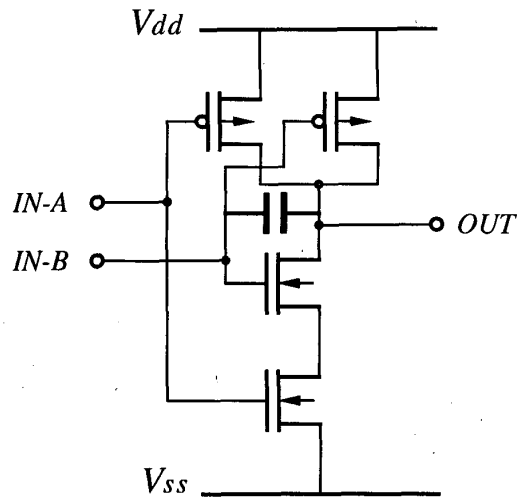

Fig. 4 Equevalent circuit of the cell layout shown in fig.3

itance vs drain voltage. Once specified in process simulation, three conditions of implantation energy in this case are simulated automatically. Fig.8 is a drain current vs gate voltage (Id-Vg). Three kinds of dosage for Boron, the ion for threshold voltage adjustment ion implantation process, are simulated here. Fig.9 is the graph of Vth roll-off curve for calculated and measured MOS device. X-axis stands for gate length and Y-axis for threshold voltage. This result shows fairly good match between simulated and measured data.

Utilizing the electrical characteristics simulated above and interconnect capacitance which is also simulated with this system, the performance of the devices are analyzed with the circuit analysis engine SPECTRE[8]. Fig.10 is the comparison of delay (X-axis) vs power (Y-axis) dependence. In this case, to evaluate it on measured data, SPICE parameters are extracted from manufactured test chips and simulated utilizing the virtual cell designing environment. The simulation results also showed quite good agreement with measurement.

Even for the user who is not an expert of simulation, it took only one week for this analysis. By utilizing this system, the time for evaluation of new process is reduced to one eighth or less compared with test manufacturing which usually requires two to three months or more.

V. Summary and Conclusions

We have developed a novel and practical virtual cell designing environment which provides well-calibrated simulator and easy-to-use GUI. This environment is used in practical work and has reduced TAT of cell designing to less than one eighth and enabled evaluation of even new structured devices.

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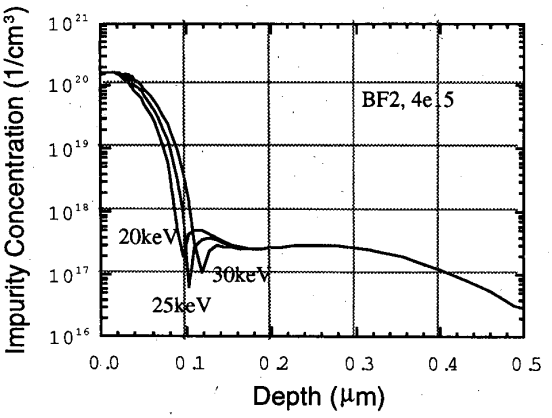

Fig.5 BF2 distribution (depth) with three variation of implantation energy

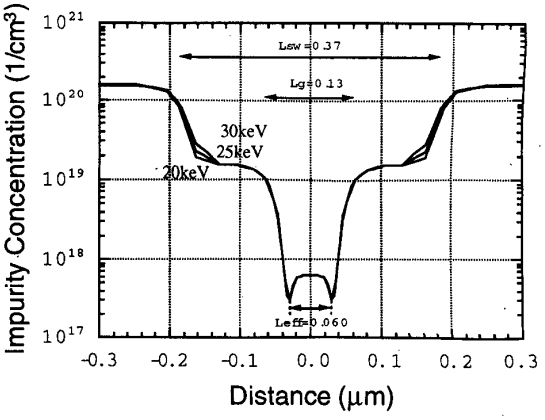

Fig.6 BF2 distribution (surface) with three variations of implantation energy

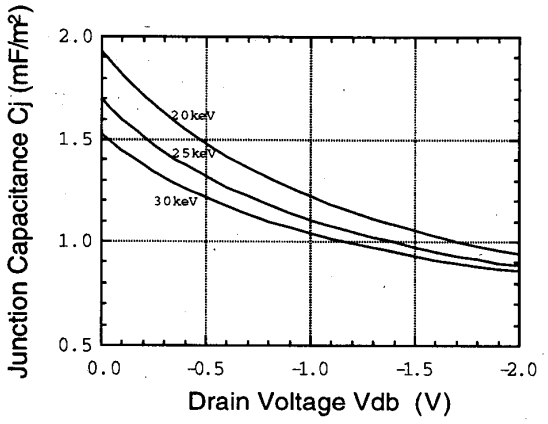

Fig.7 Junction capacitance vs drain voltage with three variations of BF2 implantation energy

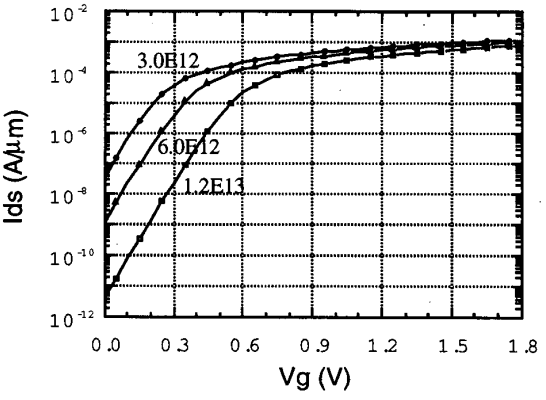

Fig.8 Drain current vs gate voltage with three variations of BF2 implantation energy

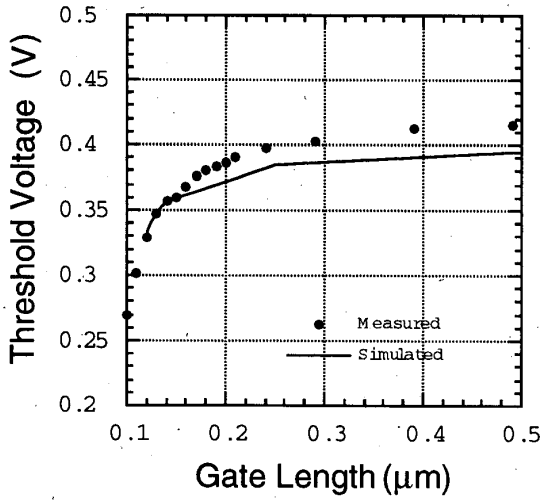

Fig.9 Threshold voltage (Vth) roll-off curve

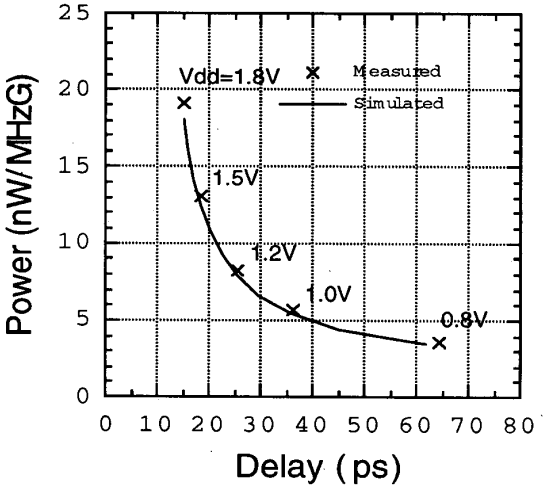

Fig.10 Delay vs power calculated from simulated and measured data