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Surface morphology and I-V characteristics of single crystal, polycrystalline and amorphous silicon FEAs

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ABSTRACT

This paper reports surface morphology and I-V characteristics of single crystal silicon(c-Si), polycrystalline silicon(poly-Si) and amorphous silicon(a-Si) field emitter arrays(FEAs). As-deposited a-Si film has smoother surface than poly-Si film. The surface morphology of the a-Si remains smooth after phosphorus doping and 950°C oxidation. a-Si FEAs have improved emission characteristics i. e. smaller anode current deviation among arrays, smaller gate current, and higher failure voltage than poly-Si FEAs. Such improved characteristics can be explained by the smooth surface morphology which is kept during doping and oxidation. The surface roughness and emission characteristics of a-Si FEAs are comparable to those of c-Si FEAs.

I. INTRODUCTION

There is an unavoidable restriction to make a large area display panel on a crystalline silicon wafer due to its size limitation. The fabrication of poly-Si FEAs has been reported to overcome this problem[1]. However, poly-Si FEAs have shown rough gate electrode surface, asymmetric gate holes and asymmetric tip shapes. Thus poly-Si FEAs have many problems in uniformity, reliability and electrical stability. To overcome these problems, a-Si FEAs have been fabricated using the deposition of a-Si film by low pressure chemical vapor deposition(LPCVD) at 550°C.

This paper describes surface morphology observed by atomic force microscope(AFM) and scanning electron microscope(SEM), and the electrical characteristics of c-Si FEAs, poly-Si FEAs and a-Si FEAs.

II. EXPERIMENTS

Major fabrication steps are described in Fig 1. The common starting material was a boron doped, p-type (100)-oriented single crystal silicon wafer with a resistivity of 10 Ωcm. The silicon wafers were oxidized and then poly-Si and a-Si were deposited as thick as 1.6 μm by LPCVD hot wall reactor at 625°C and 550°C, respectively. Phosphorus doping at 950°C and masking oxide(TEOS) deposition are performed. And oxide was patterned into discs with a diameter of 1.4 μm by reactive ion etching (RIE) (Fig. 1(a)). Then, silicon was isotropically etched using SF_6 to isolate cathode lines and form silicon tips (Fig. 1(b)). The 1st oxidation was performed to make the tips sharp at 950°C and then deposition and RIE of Si_3N_4 were performed to prevent tip-blunting due to excessive oxidation in the following step(Fig. 1(c)). The 2nd oxidation was performed to form the complete gate insulator at 950°C(Fig.1 (d)). Si_3N_4 strip and contact oxide etch were carried out, and molybdenum was deposited for a gate electrode and contact pad formation using E-gun evaporator(Fig. 1(e)). By lift-off process of the overlying structure on the tip and photolithography process of the gate electrode, the fabrication of silicon-tip field emitters was completed (Fig. 1(f)).

III. RESULTS AND DISCUSSION

AFM and SEM analyses

AFM measurement was done for these key process. Firstly, the initial film surface was evaluated after deposition process. Secondly, the silicon films were investigated after phosphorus doping step. Thirdly, the surface of the thermally grown oxide after oxidation step for tip sharpening was evaluated. The RMS roughness values are summarized in Table 1. Figure 2 shows AFM 3D images. The amorphous films were initially smooth and remained same following process steps, although surface roughness slightly increased. In contrast, the poly-Si films were initially very rough, but its surface roughness was slightly reduced after phosphorus doping and then increased after oxidation. Dopant concentration in the grain boundaries can be unusually large because of dopant segregation and this might lead to an enhanced oxidation rate caused by an increase in the surface reaction rate and diffusivity through

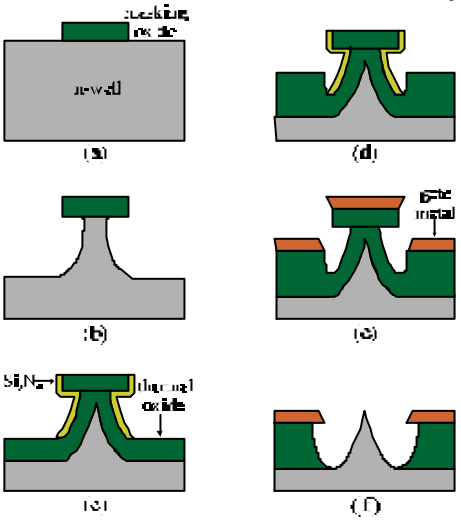
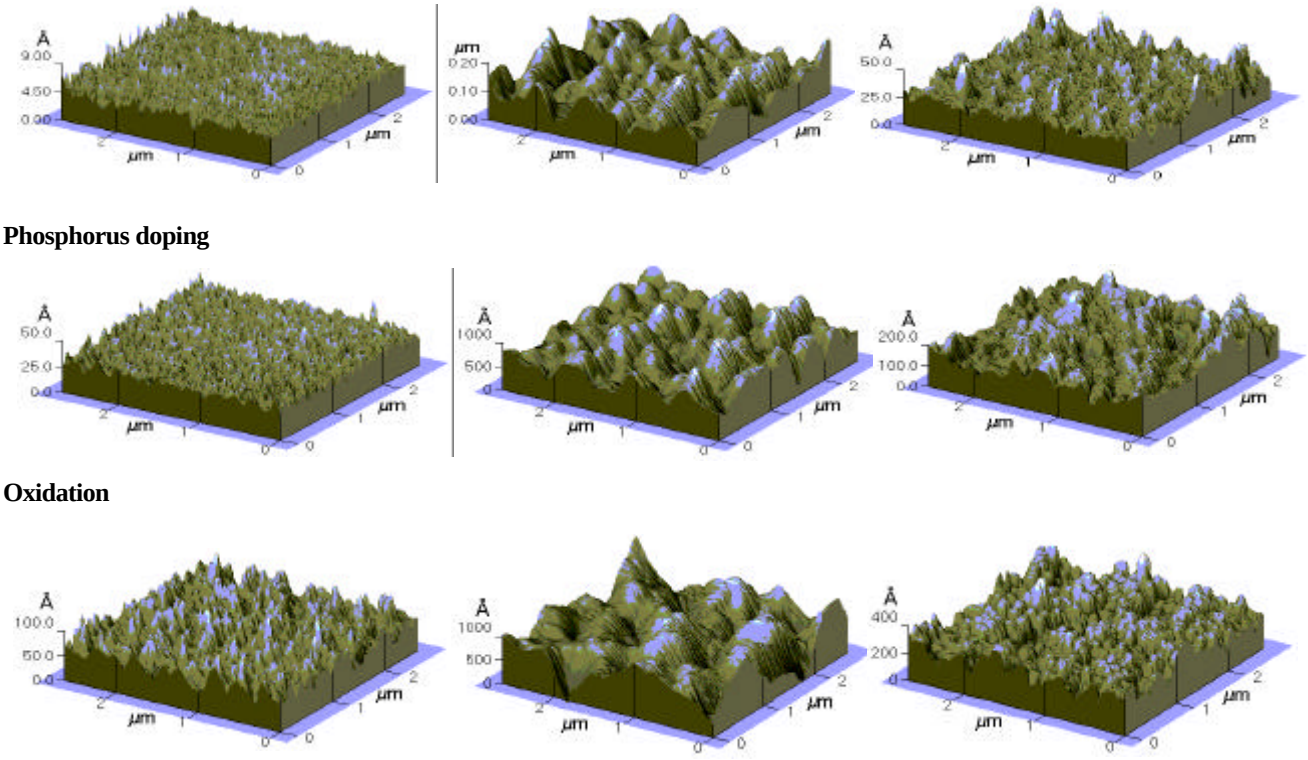


Fig. 1. Process sequence of a silicon field emitter array using Si_3N_4 sidewall formation and subsequent thermal oxidation for a gate insulator.

As-deposition

Phosphorus doping

Oxidation



(a) c-Si **(b) poly-Si** **(c) a-Si**

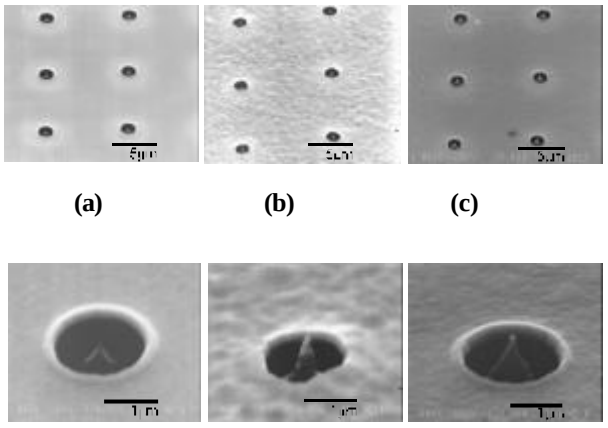
Fig. 2. AFM 3D images of Si films for three process steps. 1st row, initial films; 2nd row, after phosphorus doping; 3rd low after sharpening oxidation. 1st column, c-Si; 2nd column, poly-Si; 3rd column, a-Si.

the grown oxide, resulting in rough surface[2]. Amorphous film surface is preserved for probably these two reasons. The first reason is that its surface is stabilized by a native oxide when it is exposed to air after deposition or it is heated into the furnace before it is crystallized by phosphorus doping at 950°C. The second is that enhanced oxidation effect in grain boundary is reduced due to random grain structure and small grain boundary area. Whereas, polysilicon has columnar structure and lager grain boundary area[2, 3].

Figure 3 shows the SEM photographs of a c-Si, a poly-Si and an a-Si emitter. The a-Si emitter have much smoother gate surface and better defined gate aperture than poly-Si emitter. The gate morphology of an a-Si emitter approaches that of a c-Si emitter. However, the shape of tips was not as good as that of the c-Si tips.

Table 1. Summary of the AFM data of initial surface(a), after phosphorus doping(b), and after sharpening oxidation(c).

films	c-Si			poly-Si			a-Si		
sequence / statistics	(a)	(b)	(c)	(a)	(b)	(c)	(a)	(b)	(c)
RMS roughness (Å)	0.68	4.32	14.3	289	186	206	5.29	38.1	59.1
average roughness (Å)	0.47	3.39	11.1	231	147	166	3.76	29.6	47.7
mean height (Å)	3.95	30.6	54.3	854	737	753	19.8	143	244
surface area (μm^2)	7.456	7.331	6.964	7.530	7.327	7.364	7.329	6.561	7.365



(a) (b) (c)

(d) (e) (f)

Fig. 3. SEM micrographs of fabricated FEAs for (a) c-Si (b) poly-Si (c) a-Si, and emitter tip for (d) c-Si (e) poly-Si (f) a-Si

Electrical characteristics

Testing was performed in an ultra-high vacuum system at a pressure 2.4×10^{-9} torr. Fig 4 shows the result of the electrical measurements. The highest data points in Figure 4 indicate the device failure points. Because the surface of a-Si FEAs is smooth and gate aperture is well defined, the local electric field in gate oxide, between gate electrode and anode plate, and between gate electrode and cathode is lower than that of poly-Si FEAs. Thus, the measured emission characteristics of a-Si FEAs shows small anode current deviation among arrays and less gate current, and higher failure voltage in comparison with poly-Si FEAs[2, 4].

IV. CONCLUSIONS

In order to improve the shape of the gate apertures and reduce surface roughness, amorphous silicon deposited at 550°C was used for tip and gate insulator formation. The a-Si FEAs were successfully fabricated and showed improved electrical characteristics which come from smaller surface roughness and better defined gate apertures in comparison with poly-Si FEAs. It is expected that a-Si FEAs can give good reliability, uniformity and electrical stability in a large area display application.

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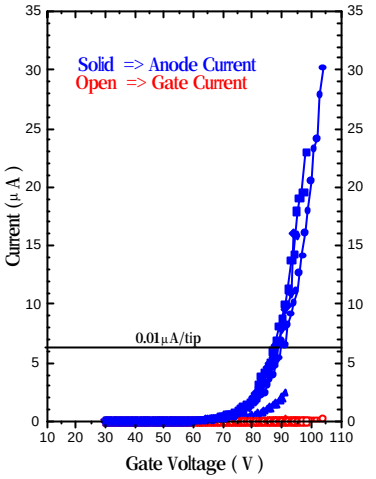
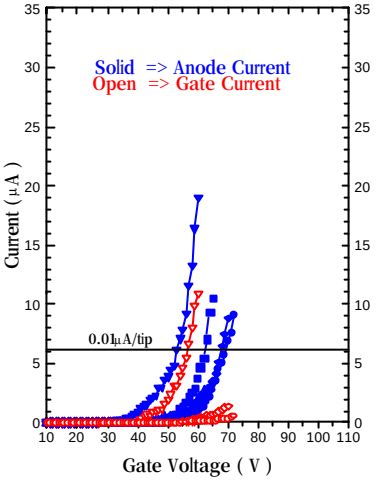


(a)



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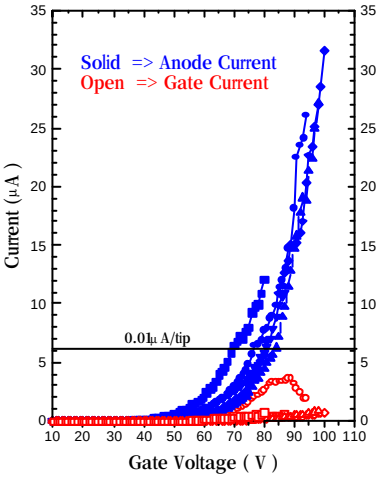

(c)

Fig. 4. I-V curves of different 625-tip FEAs on a wafer for