# Vertical Nanowire TFET Diameter Influence on Intrinsic Voltage Gain for Different Inversion Conditions

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In this work, the impact of the nanowire TFET diameter on analog parameters in "weak" and "strong inversion" conditions is analyzed. Its relation with the current conduction mechanism is also studied. A comparison of the analog performance among TFETs doped with different source doping profile (abrupt and non-abrupt) and MOSFETs was experimentally realized for larger diameter nanowires. Additionally the TFET evaluation was extrapolated for smaller diameters by numerical simulation. The transistor efficiency and the Early voltage were considered in order to calculate the intrinsic voltage gain ($A_V$). Both effects influence $A_V$ degradation for TFETs with smaller diameters biased in "weak inversion". While larger TFET nanowires show better $A_V$ than MOSFETs under "strong inversion" bias, narrower nanowires present potentialities for low power and low voltage applications, since their $A_V$ is better than the corresponding values for larger diameters TFET nanowires under "weak inversion" bias.

## Introduction

TFETs arise as promising devices for low power and low voltage applications, since they don't present a subthreshold swing limit of 60 mV/dec like in MOSFETs (1-3) and they also show a higher intrinsic voltage gain ($A_V$) than the conventional MOS transistors (4). Furthermore, in order to improve the performance and the scaling, the nanowire structure for this technology has been studied (5). The better electrostatic control of the tunneling carriers provided by the nanowire structure leads to an improvement of the transconductance (gm) value (6).

From simulations, it was observed that the predominant conduction mechanism and the interactions between the diagonally opposite surfaces of the nanowire TFETs are changed when the transistor diameter is reduced. When the transistor is biased in "strong inversion", the predominant conduction mechanism near the silicon/oxide interface is the band-to-band tunneling (BTBT). However, it is known that there is a gradual transition of mechanisms along the source/channel junction. As a consequence, coming closer to the center of the nanowire, the trap-assisted tunneling (TAT) influence becomes higher. In the center and nearby regions, the energy bands of source and channel are far from being overlapped and therefore there is no tunneling occurrence and the conduction occurs through the Shockley-Read-Hall (SRH) mechanism. This work focuses on the impact of

the nanowire diameter reduction on the main analog performance parameters. This analysis will be performed both experimentally and by simulations.

## Experimental and simulation details

The studied devices were fabricated at IMEC, Belgium and are silicon nanowire nTFETs, which use a top down vertical process flow. The gate stack consists of 3nm $HfO_2$ on 1nm $SiO_2$. The gate material is composed by TiN and α-silicon. Regarding their dimensions, the devices have a physical gate length ($L_G$) of 150 nm, a gate/source overlap ($L_{GS}$) of 30 nm, a gate/drain underlap ($L_{GD}$) of 50 nm and a channel length of 170 nm. The source and the drain region are doped with $1.10^{20}$ at.cm$^{-3}$ boron and $2.10^{19}$ at.cm$^{-3}$ As, respectively. The channel is doped with $1.10^{16}$ at.cm$^{-3}$ As. The measured devices contain 400 nanowires in parallel. The difference between the abrupt and the non-abrupt TFETs process resides in the source doping process. In the first and in the latter, a boron in-situ doping and a boron ion implantation were performed, respectively (5). Figure 1 shows a schematic representation of the studied device structure.

The simulations were performed using the Atlas simulator from Silvaco, considering the different current conduction mechanisms: Shockley-Read-Hall (SRH) recombination, trap assisted tunneling (TAT) and nonlocal band-to-band tunneling (BTBT).

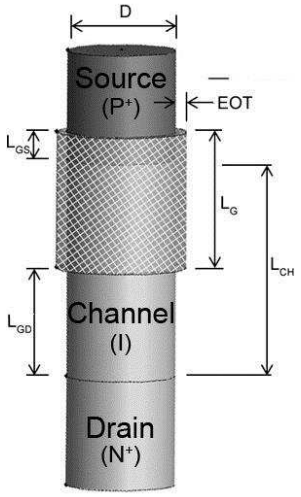


Figure 1. Structure of the studied devices.

## Results and analysis

The main difference between MOSFETs and TFETs is the conduction mechanism, since TFETs operate through tunneling mechanisms while MOSFETs are based on drift/diffusion. Figure 2 shows the drain current behavior as function of gate voltage ($V_{GS}$) for abrupt and non-abrupt junction nTFETs and nMOSFETs. This figure shows that the on-current ($I_{ON}$) generated by the TFET devices is at least 3 or 4 orders of magnitude lower than for MOSFETs due to the BTBT conduction of TFETs.

However, considering that the devices with a large diameter are biased in "strong inversion" condition, the TFETs present a higher intrinsic voltage gain ($A_V$) than the MOSFETs, as shown in figure 3. Although the transconductance (gm) of the MOSFETs is higher, TFETs are less affected by the electric field from the drain and thus have a good output characteristic (lower gd values).

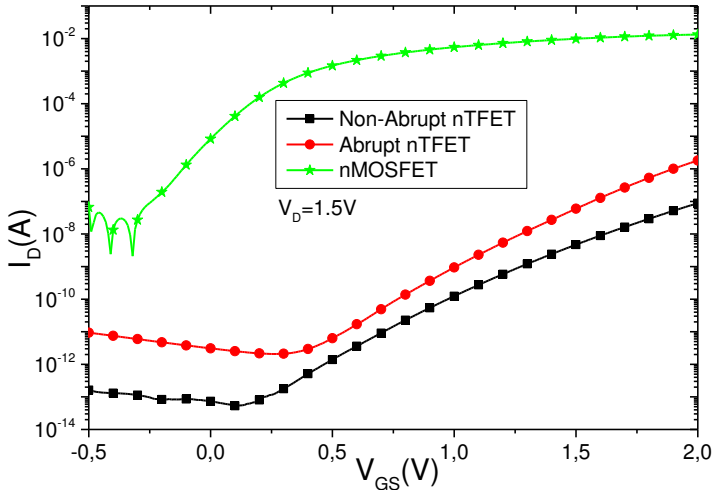


Figure 2. Experimental drain current as a function of gate bias for TFET and MOSFET.

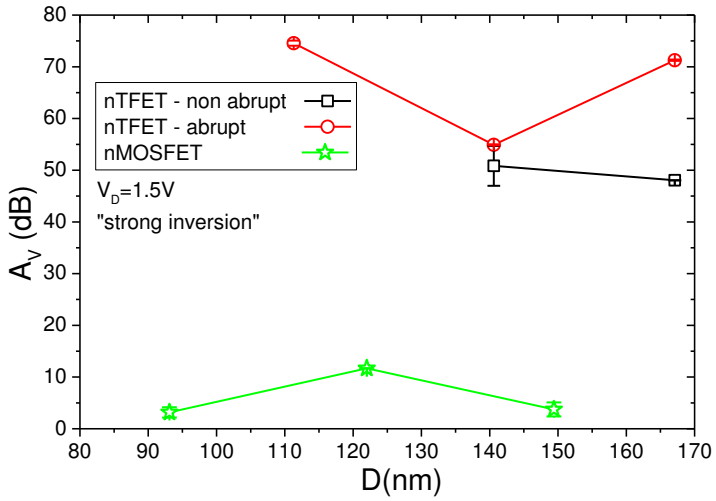


Figure 3. Experimental intrinsic voltage gain as a function of the nanowire diameter for TFET and MOSFET.

Figure 4 shows experimental and simulated $A_V$ of an abrupt nTFET as a function of the diameter. From this figure it is possible to observe that for devices with smaller diameters in the "strong inversion" condition, in which an interaction between the potential of the opposite surfaces appears and the symmetrical BTBT regions becomes closer to each other, $A_V$ is degraded due to the stronger dependence of BTBT on the drain voltage, causing a higher gd.

Due to this interaction, the BTBT predominance begins to occur at a lower gate voltage for nanowires with smaller diameters as can be observed in figure 5, which shows the simulated $I_D$x$V_G$ curves for an abrupt nTFET with different diameters. These curves are normalized in relation to the cross sectional area of the device.

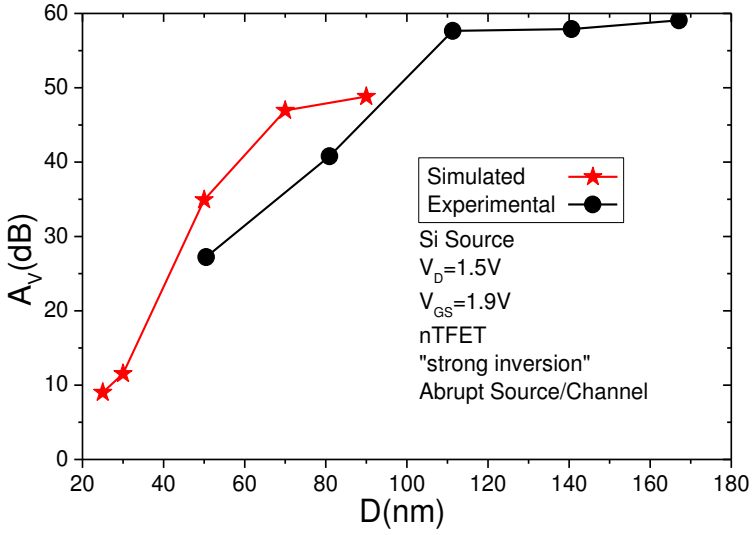


Figure 4. Experimental and simulated intrinsic voltage gain of an abrupt nTFET as a function of the nanowire diameter.

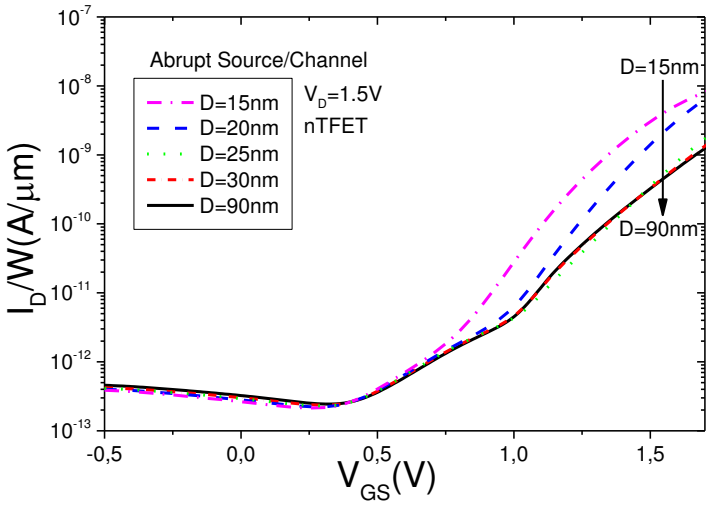


Figure 5. Simulated normalized drain current as a function of gate voltage for abrupt nTFETs with different diameters.

Since TFETs have been studied for low voltage applications, the analog analysis is also performed in "weak inversion". When a TFET is biased in this condition, the efficiency ($g_m/I_D$) is higher for smaller diameter devices, as shown in figure 6. This happens owing to the higher percentage of the junction, in which the predominant transport mechanism is BTBT, if compared with larger devices. Consequently, the value

of gm is higher for nanowire nTFETs with smaller diameter. $A_V$ was calculated using equation [1] and the results are presented in table 1.

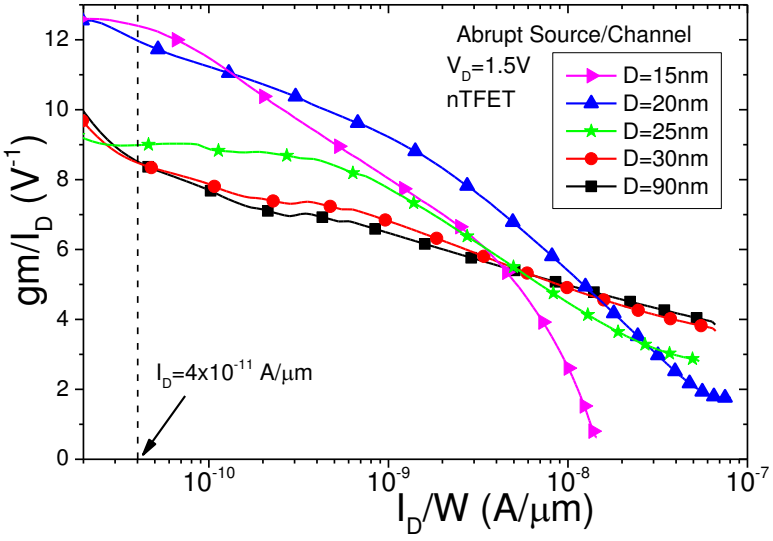


Figure 6. Simulated $gm/I_D$ x $I_D$ of abrupt nTFETs for different diameters.

$$A_V \approx gm/g_D \approx V_{EA.*}\ gm / I_D \qquad [1]$$

**TABLE I.** Simulated $A_v$ of an abrupt nTFET in "weak" and "strong inversion" for different diameters.

| **Diameter** | **$A_V$ (dB) @ $I_D$ = 2x10$^{-11}$A/μm "weak inversion"** | **$A_V$ (dB) @ $V_{GS}$ = 1.9V "strong inversion"** |
|---|---|---|
| 15 nm | 68.6 | --- |
| 20 nm | 73.3 | --- |
| 25 nm | 75.7 | 9.0 |
| 30 nm | 72.9 | 11.5 |
| 90 nm | 72.3 | 47.0 |

Considering the "weak inversion condition", there is a point of maximum $A_V$ for a specific diameter and a degradation for smaller and larger nanowire diameters because of a competition between both effects, the increase of $gm/I_D$ and the decrease of the Early voltage ($V_{EA}$) with the reduction of the diameter. The $V_{EA}$ decrease is caused by the higher dependence of the current conduction on the drain voltage, since for the smaller devices, BTBT predominates along the entire source/channel junction. Going from a large to a narrow nanowire, the BTBT regions from opposite surfaces become ever closer. The diameter for which these regions start to overlap, is the one associated with maximum $A_V$. Therefore, it is possible to conclude that the decrease of the intrinsic voltage gain for higher diameters is more dependent on the transistor efficiency, and for smaller diameters it is more dependent on the Early voltage.

Considering the "strong inversion condition", $A_V$ is higher for larger nanowire diameters. Observing the curves presented in figure 6, it is possible to notice that the transistor efficiency ($gm/I_D$) is higher for the nanowires with larger diameters. The junction area for narrower devices is smaller and when the BTBT regions of the

diagonally opposed surfaces of the nanowires overlap, the value of gm decreases. Therefore, $A_V$ is also degraded for devices with smaller diameters in this condition.

## Conclusion

Vertical nanowire nTFETs arise as an alternative for substituting conventional MOS technology, especially regarding energy efficiency and scaling. This work presents the analysis of the nanowire diameter reduction influence on the intrinsic voltage gain for "weak" and "strong inversion" conditions. It is possible to notice a reverse trend of the gain efficiency ($gm/I_D$) for both conditions, since in "weak inversion" the smaller the diameter, the higher the percentage of the junction that is tunneling BTBT dominated. This happens because BTBT is "triggered" by lower gate voltages for narrower TFETs.

Besides the larger diameter nanowire nTFETs, which show better analog behavior than MOSFETs in "strong inversion" (this result was also found for FinFET structures (4)), the smaller diameter devices show potentialities for low power and low voltage applications, since their $A_V$ is better for low gate voltages than for the larger diameter nanowire nTFETs.

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