Flexible Evaluation of RFID System Parameters using Rapid Prototyping

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Abstract—Today's RFID systems are dependent on a wide range of different parameters, that influence the overall performance. Such system parameters can for example be the selected data rate, encoding scheme, modulation setting, transmit power or different hardware configurations, like one or two antenna scenarios. Furthermore, it is often desired to optimise several performance goals, like read-out range, read-out quality, throughput, etc., which are often contradicting each other. In order to achieve a desired performance of an RFID system, it is essential to understand the influences of the individual parameters of interest and their interconnection. Due to the multitude, wide range and interdependencies of influencing factors, this however is a complex task. Simulations offer insights in these relations but rely on the correct modeling of the dependencies of- and between the parameters. With our established prototyping system for RFID, we are able to flexibly and accurately explore the influence and interconnection of such parameters in a wide range on a basis of real-time measurements. Results on the evaluation of read-out quality depending on the transmit power and the data rate are presented.

I. INTRODUCTION

Radio Frequency Identification (RFID) is a wireless identification technology that offers great potential for many applications domains like automated tracking of goods in library systems, on airports, in pharmaceutics or logistics in general. Some of these applications have so far been carried into effect, however there is still some gap between existing and desired RFID technology that fullfills all the imagined goals for potential applications. Such desired performance goals are for example high read-out quality and a small number of packet errors in the communication with tags, a high throughput, a large communication range or an almost infinitesimal number of not accessed tags in the read range. However, some of these goals are often contradicting and just offer tradeoffs, such as throughput and read-out distance. In order to further increase potentials in RFID technology, it is essential to understand the interconnection between these performance goals and their dependency on other system parameters, such as modulation and encoding parameters, selected data rates, used output power or maximum read range, and hardware configurations such as single or two antenna systems.

Such dependencies and interconnections can be explored by simulation, however it is crucial to model the various influences of a single parameter accurately and derive realistic models. Due to the multitude of parameters in RFID systems this is a difficult task. Using off-the-shelf components allows to measure the performance of the system in a certain scenario and explore the influence of different configurations. However, such components often do not provide the required flexibility to access all parameters of interest separately. Additionally, one has to accept the provided performance of the available RFID equipment, not having any influence to improve it. If for instance commercially available UHF RFID readers are used (e.g. from Feig electronic), one has to accept the provided data rates (up to 320 kHz), even if higher data rates are standardised (up to 640 kHz).

Floerkemeier et al. [1] recently presented their RFIDSim simulation engine and compared its capabilities to measurements using commercially available RFID equipment. Their results comparing medium access behaviour in a multi tag scenario show very good accordance between their measurement and simulation results. Derbek et al. [2] present a simulation platform for UHF RFID, that aims at a consistent design methodology for building a system architecture and to run UHF RFID tag simulations of high complexity. They present an extendable and flexible simulation framework. However, they do not focus on implementations and measurements, and do not give any performance results. Mayer et al. [3] show measurement results on the input impedance of RFID transponders, depending on the operating power. Furthermore, they present results about the minimum required power at the transponder in order to get an answer from the transponder chip. Nikitin et al. [4] present various factors influencing the read-out range. They give a good overview, however they do not show any details, or their own simulation or measurement results.

In this work we present a rapid prototyping framework that allows to explore various RFID scenarios with real-time measurements. In contrast to commercially available RFID equipment, it provides full control to *all* parameters of interest. Hence it allows for a multitude of different experiments with various system configurations. The prototyping framework supports both, the high frequency (HF, 13.56 MHz) as well as the ultra high frequency (UHF, 868 MHz) domain and systems using passive transponders. Previous work has presented results in the HF domain. Due to the higher complexity of UHF RFID systems, we only focus on results achieved in this frequency domain in this paper.

The rest of the paper is organised as follows: Section II introduces the rapid prototyping concept, Section III presents the digital and analogue configuration, while Section IV shows the measurement setup and results. The last section concludes the paper.

II. RAPID PROTOTYPING SYSTEM

Our established rapid prototyping framework for RFID allows for evaluation of RFID systems on different layers of abstraction. It exhibits two simulation layers for verification of protocol- and signal processing tasks. A third layer is comprised of a rapid prototyping board and an analogue frontend for conducting real-time measurements. The rapid prototyping board accomplishes RFID reader baseband processing using programmable, digital components. DSP and FPGA code for this RFID reader is semiautomatically generated out of the simulation layers [5]. This hardware platform provides access to all system parameters of interest and permits evaluation with real-time measurements in different scenarios. Due to the automatic generation of configuration files for the digital hardware, various implementation alternatives can be derived rapidly, allowing for a multitude of experiments.

Such a rapid prototyping approach provides full access to all system parameters of interest: on the rapid prototyping board, the FPGA firmware is set up very flexibly to allow to change several parameters in their defined range. This is achieved using registers, that are accessed from the DSP during run time, like e.g. encoding and modulation settings, backscatter link frequency selection, timing intervals, etc. Moreover, the analogue frontend allows for different hardware configurations, like single or two antenna setups. The following section provides some deeper insight into the actual setup.

III. TARGET HARDWARE SETUP

The target hardware consists of a rapid prototyping board and a radio frequency (RF) frontend. The rapid prototyping board comprises the digital, reconfigurable part, consisting of an FPGA and a DSP, digital-to-analogue (DAC) and analogue-to-digital (ADC) converters as well as a network connection to a remote interfacing software (see Figure 1). All of the protocol and signal processing tasks are realised in the digital domain in order to have sufficient flexibility to reconfigure the system rapidly and evaluate various different transmitter and receiver architectures. The DSP is used for handling the protocol processing while the FPGA accomplishes the required signal processing tasks. The analogue frontend serves as a high performance, linear heterodyne up- and down-converter [6]. Further, the frontend is exchangeable to either support the high frequency (HF, 13.56 MHz) or ultra high frequency domain (UHF, 868 MHz) and is designed to be extended to the 2.4 GHz domain. Different ISO and EPCglobal standards [7], [8], [9] in both, the HF and UHF frequency domain are supported. The results of this work only focus on the UHF domain, following the EPCglobal standard (almost equivalent to the ISO 18006-C standard). Future research will aim to extend the setup to a multi antenna system, to evaluate the applicability of MIMO and beamforming algorithms for RFID.
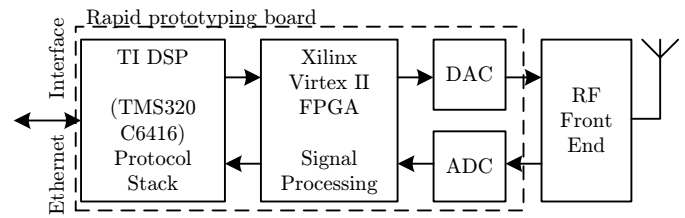

Fig. 1. Block diagram of rapid prototyping board.

A. Digital Baseband Hardware

On the digital baseband hardware, the transmit signals are generated at an intermediate frequency (IF) of 13.33 MHz, and the received signals are processed (see Figure 2). Thereby, the DSP controls the protocol processing and forwards the bits-to-transmit to the FPGA. Registers provide an interface for control information, such as for example pulse interval encoding configurations and amplitude shift keying modulation settings. The FPGA transmitter generates the desired logical stream, modulates and upconverts it, applies a transmit filter and interfaces the generated samples to the DAC. At the receiver the signal is sampled at a center frequency of 13.33 MHz by the ADC. In the FPGA part it is firstly bandpass filtered in order to limit the overall noise bandwith and then downconverted using an I/Q demodulator with low pass filters. After that the signal is integrated over the half link frequency period, which is a matched filtering if the tag answers using a rectangular signal shape. Subsequently a slicer sets a threshold to discriminate between the two tag states *"absorb"* and *"reflect"* power. This is achieved using the time interval between reader command and tags response to estimate the strength of the carrier leakage and the noise power. At the first response symbol of the tag, the slicer estimates the position of the *"reflect"* state of the tag in the I/Q plane to set its threshold accordingly to the receive signal strength [10]. The thereby detected tag response signal, is subsequently synchronised and
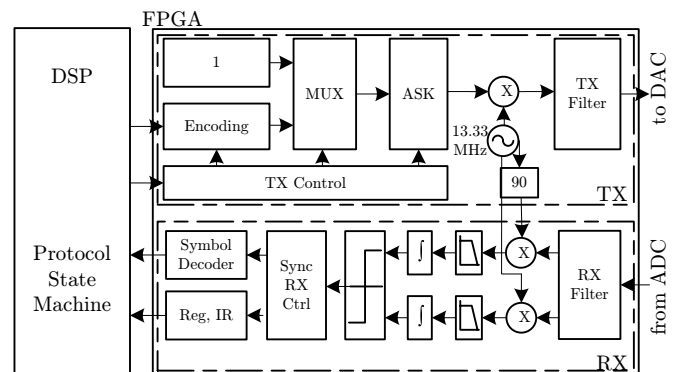

Fig. 2. Block diagram of digital baseband hardware modules.

decoded using a correlator structure [11]. Finally, the received bits are forwarded to the DSP, that generates the next command according to the communication protocol.

Additionally, the signal to noise ratio (SNR) in front of the slicer is estimated in the FPGA receiver: The noise power is estimated during the idle state before a tag responses, by calculating the variance of the receive samples. The receive signal power P_S is calculated using the I and Q coordinates of the two estimated receive states *"absorbe"* (S_a) and *"reflect"* (S_r):

$$P_S = (S_{r,I} - S_{a,I})^2 + (S_{r,Q} - S_{a,Q})^2.$$

It should be noted, that the SNR is estimated after the matched filtering. Depending on the link frequency, the integration interval in the matched filter lasts between $0.78\mu s$ and $12.5\mu s$ (corresponding to a link frequency range from 40 - 640 kHz) according to the EPCglobal standard for UHF RFID. This results in much higher SNR values at lower link frequencies. In depth details on this SNR estimation and the functionality of the slicer are presented in [10].

B. Radio Frequency Frontend

The analogue frontend was especially designed to extend the existing HF rapid prototyping system to the European UHF band centered at 866.5 MHz. Both, the transmitter and the receiver, are based on a low IF to RF concept [12]. The frequency conversion is done from HF to UHF at the transmitter and analogous from UHF to HF at the receiver in two steps. The intermediate frequency for both modules is at 140 MHz. Flexibility for rapid prototyping systems means to shift as much functionality as possible into the digital domain where a redefinition of system specifications like modulation schemes or pulse shaping can be implemented much faster than a frontend can be adopted. Therefore, the main tasks for a frontend of such a system are filtering, amplification and frequency conversion. Figure 3 shows a simplified block diagram of the transmitter. The input TX_{IN} is directly connected
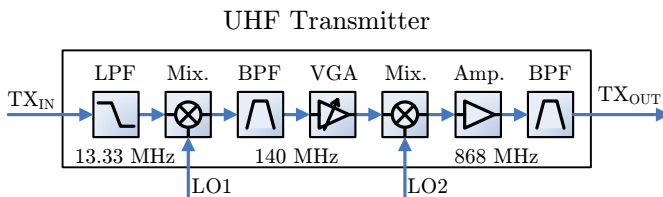

Fig. 3. Simplified block diagram of the analogue UHF transmitter.

to the DAC of the rapid prototyping board. A low pass filter at the analogue transmitter is used to suppress undesired signal components due to the digital-to-analogue conversion. Then follows the frequency conversion to the 140 MHz intermediate frequency. At this section a high quality SAW band pass filter defines a 5 MHz system bandwidth. The following variable gain amplifier enables an adjustment range of 50 dB for the transmit power. In the UHF band after the second frequency up-conversion stage an amplifier and a second SAW filter

are implemented. The maximum output power at TX_{OUT} of 24 dBm is sufficient to drive an external power amplifier.

Figure 4 illustrates a simplified block diagram of the receiver. The receive signal at the input RX_{IN} is firstly filtered by a SAW band pass filter and then amplified. After the frequency down-conversion to 140 MHz a SAW band pass filter defines the receiver bandwidth equal to that of the transmitter. The variable gain amplifier at the receiver allows to adjust the output power for best ADC operation. After the second frequency down-conversion a low pass filter suppresses undesired signal components. The output RX_{OUT} of the receiver can be connected directly to the ADC input of the rapid prototyping board. Additionally, the receiver supports a second output ED_{OUT} for an integrated envelope detector path. This output can be used for monitoring backscattered transponder signals.
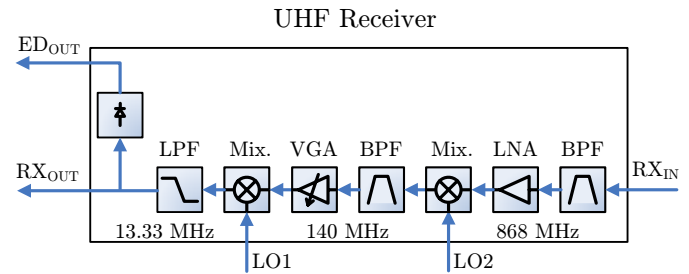

Fig. 4. Simplified block diagram of the analogue UHF receiver.

The modular and scalable design of the analogue frontend allows for different configurations. Evaluation measurements concerning the read range of the frontend in combination with the rapid prototyping hardware were investigated in an anechoic chamber. Successful reader-tag communication was possible up to a distance of 4.5 m, where the limitation was only caused by the dimensions of the chamber. A more detailed description of all modules of the rapid prototyping UHF frontend can be found in [6].

IV. MEASUREMENTS

One of the major design goals in RFID systems, namely the read-out quality and its dependency on data rate and transmit power has been evaluated. The read-out quality is reflected by the estimated SNR at the receiver and the measured packet error ratio (PER).

A. Measurement Setup

In order to mitigate environmental influences and soley measuring the dependency between data rate, transmit power, SNR at the receiver and packet error ratio, we conducted our measurement in an anechoic room. Figure 5 illustrates the hardware measurement setup. For this measurement we have used a single antenna scenario in which transmitter and receiver share a single antenna. A circulator separates transmit and receive signals and connects the external power amplifier of the transmitter and the UHF receiver to the antenna. Reflections of the transmit signal back into the measurement
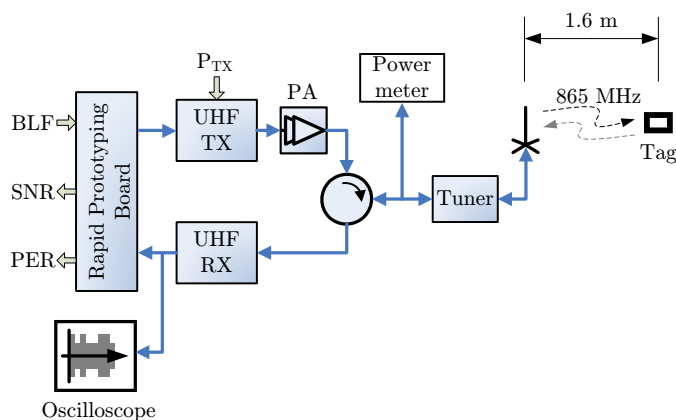
Fig. 5.   Measurement setup

parameter	range according to EPCglobal UHF standard	value
reset	-	10ms
lead in	-	3ms
lead out	-	2ms
encoding	-	FM0
DR	8, 64/3	8, 64/3
BLF	40 - 640 kHz	variable
TRCal	17.2 - 225 μs	variable
RTCal	TRCal/1.1 - TRCal/3	maximum
tari	6.25 - 25μs	RTCal/3
PW	max(0.265 tari,2) - 0.525 tari	0.5 tari

TABLE I
PARAMETER SETTINGS FOR MEASUREMENT.

system, caused due to impedance mismatch of the antenna, were reduced by an impedance tuner placed between antenna and circulator. The transmit power was observed continuously during the measurements with a power meter after the circulator. To measure the correct unmodulated carrier power of our transmitter the power measurement was gated to the so called lead in phase of the used test signal (see Figure 6). In this time period only the unmodulated carrier at 865 MHz was transmitted. The output of the UHF receiver was connected directly to the ADC input of the rapid prototyping board. Additionally, the output was monitored by an oscilloscope. The reader antenna, a circular polarised patch antenna, and the tag were placed in a distance of $1.6m$ inside the anechoic chamber whereas all other equipment was placed outside the chamber. Throughout the entire measurement one single, commercially available tag was used.

For this campaign the varied system input parameters were the Backscatter Link Frequency (BLF) and the transmit power (P_{TX}), and the monitored system output parameters were the estimated signal-to-noise ratio and the observed packet error ratio. During the measurement, the backscatter link frequency was varied from 107 kHz to 640 kHz, for different adjusted transmit power values. The reader reads out the electronic product code (EPC code) of the tag periodically using the same parameter settings, before updating its input parameters. Each parameter set has been applied for 10^4 EPC code read-outs, where each of these read-outs consisted of the following intervals: reset, lead in, Query, T1, RN16, T2, Acknowledge, T1, EPC code, lead out (Figure 6). During the reset phase, the
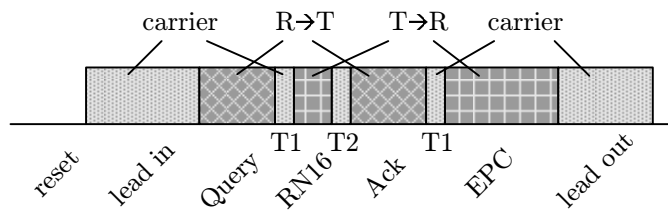

Fig. 6.   Test sequence for measurements.

tag was not supplied with energy, the lead in phase is used to power the tag before reading its EPC code. After the EPC code read-out the tag was still supplied with energy during the lead out phase, before the next interrogation started with a reset phase. The time interval T1 is used to estimate the SNR as well as the noise and "absorb" state in the digital receiver (compare with Section III).

Furthermore, the settings shown in Table I have been applied (according to the EPCglobal standard [9]). The divide ratio (DR) and tag to reader calibration symbol (TRCal) control the backscatter link frequency of the tag, and hence are variable. The reader to tag calibration symbol (RTCal) is used to calibrate the tag to distinguish between '0' and '1' in reader to tag communications. As also the link timing T1 is dependent on this RTCal value, and the period T1 is used for estimating the noise and "absorb" state as well as the SNR in the digital receiver, we try to maximise this value. Finally, the reader to tag communications encoding parameters tari (type A reference interval) and pulse width (PW) are set to RTCal/3 and tari/2 respectively. Throughout this measurement, FM0 encoding for the tag to reader communication has been selected. This maximises the data rate among all possible uplink encoding schemes, with the data rate being equal to the backscatter link frequency.

B. Results

For evaluation of the read-out quality the SNR and packet error ratio (PER) have been considered. The SNR has been calculated by dividing the average of both, the estimated receive signal power ($\bar{P}_S$) and the estimated noise power ($\bar{P}_N$) during the 10^4 read-out attempts ($SNR = \bar{P}_S/\bar{P}_N$). The PER has been calculated by dividing the successful EPC code read-outs by the total amount of read-out trials (10^4). A correct read-out implies the correct reception of both, the 16 bit random number as a response to the query command as well as the 128 bit EPC code. Note that the sequence as shown in Figure 6 has been used to read-out the EPC code, not demanding any retransmissions using the NAK (not acknowledged) command if the CRC check of the EPC code did not succeed. Hence, only the successful read-outs at the first attempt are considered.

Figure 7 and Figure 8 show the SNR and PER depending on the backscatter link frequency. It can clearly be observed
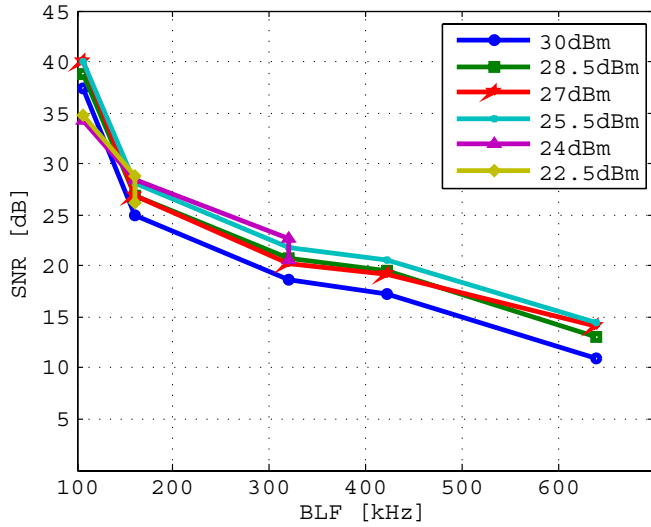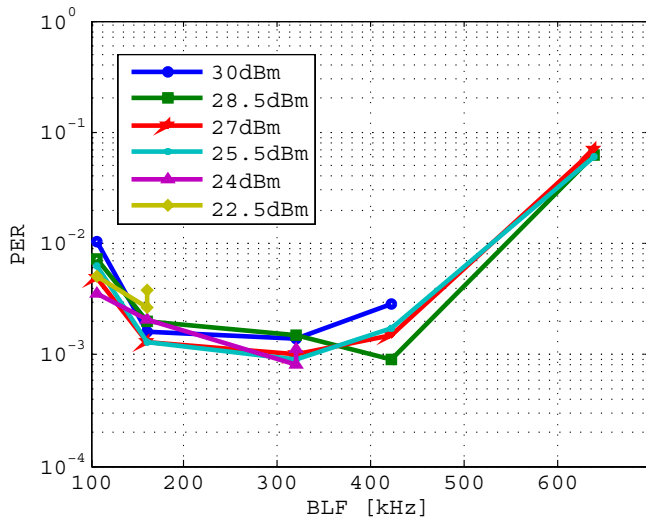
Fig. 7.   Estimated SNR as a function of BLF.

Fig. 8.   Packet errors as a function on BLF.

changes over time, leading to unequal duty cycles at the output of the slicer in the receiver and therefore an increased packet error probability. The PER reaches its minimum at a BLF of 320 kHz, with a value below 0.001.

For selecting a certain BLF, there are overlapping configurations for a different setting of the divide ratio (DR) bit. Two BLF points, namely 107 kHz and 160 kHz have been evaluated using both configurations, however not showing any performance difference for the distinct settings.

The different curves in Figures 7 and 8 belong to distinct transmit power levels. It is worth noting, that at higher BLF and lower output power, the tag has not sufficient energy left to respond. These points are not plotted in the graphs, the edge at the end of the corresponding curve indicates, that this was the last BLF value the tag could still respond with the applied transmit power. This could also be observed on the oscilloscope, showing that at higher BLF and low transmit power, the tag is not capable to transmit its total EPC code, but stops after some fractions of it.
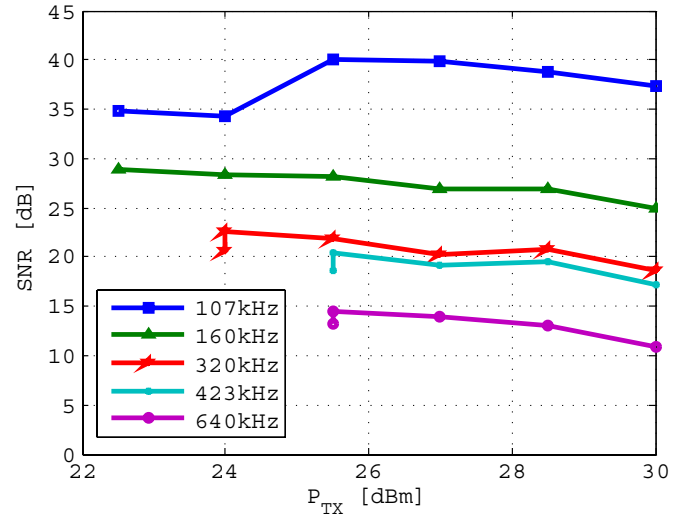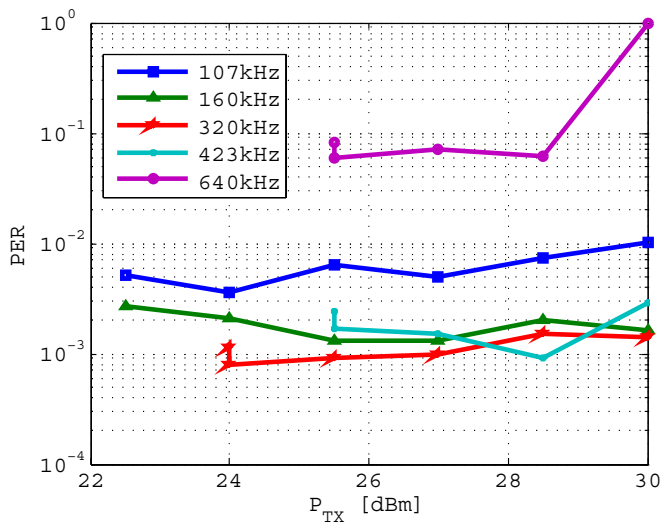

Fig. 9.   Estimated SNR as a function of P_{TX}.

Figure 9 and Figure 10 show the results of the measurement depending on the transmit power. Here, the parameter for the distinct curves is the BLF. In both figures it can be observed, that the tag starts to communicate at a certain transmit power level. The SNR is slightly decreasing with rising transmit power. The reason for this effect is that the energy storing capacitors at the tags are full at a certain output power, and thereafter the excessive energy is drained off in the shunt transistor, also during absorbing phases. This slightly decreases the $|\Delta\Gamma|$ value of the tag, which describes the efficiency of the backscatter modulation as the difference between the tag's reflection coefficients in the *"reflect"* and *"absorb"* state. This effect has also been observed by Mayer et al. [3]. It leads to a saturation of the receive signal power, even at increasing transmit power. However, at higher transmit power, more transmitter oscillator phase noise is produced, decreasing the overall SNR. A second reason for this slight

that for increasing BLF the SNR decreases. On the one hand the matched filter in the digital receiver integrates over a shorter period, thus accumulating less energy per bit and hence provides a smaller SNR output. On the other hand the tag requires more power for processing its data at a higher clock frequency. Finally, a third reason for this behaviour is the wider tolerance for the backscatter link frequency accuracy at increasing BLF values, as defined in the EPCglobal standard.

Similarly, the PER increases with increasing BLF. Additionally, there is a slight increase at small backscatter link frequencies. This has been investigated to be caused from the long total response time at small BLFs: As the digital receiver adapts its threshold just at the very beginning of the packet, it does not track any additional changes during the reception [10]. It has been observed, that however during long tag response times, the backscatter behaviour of the tag slightly

Fig. 10. Packet Errors as a function of P_{TX}.

SNR decrease is the external power amplifier, that saturates at higher transmit power.

Similarly, the PER (Figure 10) shows a weak increase at the higher transmit power. Again it is observed, that at low transmit power values, the communication at higher data rates ceases firstly.

V. CONCLUSION

To further improve the performance of the complex RFID systems that are currently developed, accurate knowledge about RFID system parameters and their interconnection is essential. With the presented RFID prototyping system full access to all the settings and configurations of interest is provided, and various impacting system parameters and their dependencies can be evaluated in realistic scenarios with real-time measurements. Neither this possibility to access all configurations is given using off-the-shelf RFID equipment, nor the realness of assumptions, accuracy of results and realisability of the system can be ensured using simulations. In this work we investigate the relation of data rate and transmit power on reliability, by means of SNR and packet error ratio measurements.

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