Low-voltage operation of a CMOS image sensor based on pulse frequency modulation

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ABSTRACT

Inspired by biological information scheme, pulse frequency modulation (PFM) technique is robust for noise sources due to its digital encode of analog signals. In a viewpoint of image sensors, PFM is also useful for a wide dynamic range and has already been demonstrated over 60 dB. We have designed a pixel circuit of a CMOS image sensor using PFM for the next generation architecture of vision chips. The chip is fabricated using a standard 0.35 µm double poly, triple metal CMOS technology. The photodiode is a parasitic pn diode between p-well and n-diffusion with the size of 2 µm squares. The top of the photodiode is covered with third metal and 1 µm square hole is open for aperture. Feedback circuits consist of a Schmitt trigger and two inverters. We have demonstrated by introducing PFM the chip works well under the power supply voltage of 0.55V with 50 dB. Such a low voltage operation suggests deep sub-micron technologies, for example, 0.18 µm technologies could be applied to the sensor. The other important point in our chip is that the photodiode is very small in size of 2 µm x 2 µm with the aperture size of 1 µm x 1 µm. This enables us to realize an image sensor with a small fill factor, which is very useful for vision chips where functional circuits are integrated in each pixel.

Keywords: CMOS image sensors, pulse frequency modulation, low voltage operation, vision chips

1. INTRODUCTION

A vision chip is an image sensor that integrates a photo-sensor with signal processing circuits in each pixel [1]. Their advantages over conventional image processing systems based on CCDs (charge coupled devices) are in fast and versatile image pre-processing due to incorporating signal processing functions in each pixel. Many works on vision chips have been reported so far [2] and classified into an analog type and a digital type in a viewpoint of signal processing. The analog type is more natural because the input signal or light intensity is analog, although it is far from robust against noise and thus has less precision. On the contrary, the digital type is robust and more suitable to communication, while it requires analog-to-digital converter (ADC). In addition, digital multiplication is area consuming. In each type the integration density is critical to incorporating much function in a pixel and/or increasing resolution. The trend toward deep sub-micron fabrication process in LSI is suitable to vision chips, because such fine process enables to integrate more functions in a pixel. However, the operation voltage decreases accompanied with such a deep sub-micron process, and it may directly affect the signal quality and thus deteriorate a signal-to-noise-ratio (SNR) [3]. In addition, the area of a photodiode decreases as the process rule becomes fine, and consequently the signal capacity in the photodiode decreases, which also causes to degrade the SNR. Thus, the great issue is to develop architecture that can deal with lowering of the operation voltage and shrinking of the area of a photodiode.

A pulse frequency modulation (PFM) technique uses pulse trains to represent analog signals in time domain [3]. Thus, in nature a PFM is robust in the signal transmission and well compatible with digital logic circuits. These features are very effective in vision chips where an image pre-processing function is integrated in each pixel. Neurobiological systems also use PFM in not only communication but also information processing as pulsed neural networks. This architecture is very suitable to deep sub-micron technologies in the following reasons. First, PFM is essentially digital circuits except for a photodiode, thus deep sub-micron technology is applicable to it with little modification. Second, the output is pulse trains or digital signals, which means the operation voltage hardly affects the performance of the signal quality. Third, the shrinkage

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of the photodiode size may increase the frequency of the output pulses as described later and thus it generally degrades SNR little.

In this paper, we have developed an image sensor based on PFM technique using 0.35 µm CMOS technology, where a small size of a photodiode with 1µm square is employed. We have demonstrated a low voltage operation below 1V with a dynamic range of 50dB. First, we will describe the basic circuit design and then demonstrate the experimental results as well as the simulation. Finally, we will make a discussion.

2. BASIC CIRCUIT DESIGN AND SIMULATION

A PFM is an output representation that an analog output is converted into pulse frequency, and is used in the output from the nerve cells as spikes described before. To employ a PFM in a vision chip, relaxation oscillation circuits [4, 5] are constructed as shown in Fig.1. The photodiode PD acts as a variable current source controlled by the input light intensity and is charged through the reset transistor M1. The gate of M1 is switched by the feedback from the Schmitt trigger ST and the two inverters INV1 and INV2. In such configuration the stronger the light intensity is, the higher the pulse frequency is. The analog value of the light intensity is consequently converted into a pulse train as digital signal naturally.

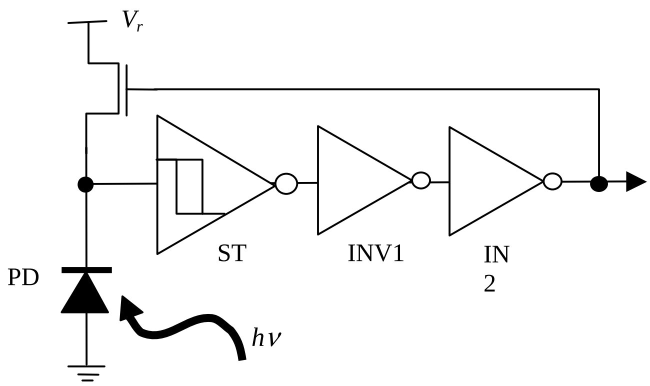

Figure 1: Fundamental PFM circuits. ST; Schmitt trigger, INV; inverter, PD; photodiode.

The operation sequence of the PFM circuits is as follows. In the first time interval, T1 the voltage of the PD V_{PD} is larger than the threshold of ST V_{th}. The outputs of ST, INV1 and INV2 are then in the logic level “L”, “H” and “L”, respectively, and thus M1 is in OFF-state. As light illuminates PD, V_{PD} gradually drops from the reset voltage near V_r by the photocurrent and finally reaches V_{th}. After time delay t_d, which corresponds the second time interval T2, the outputs of ST, INV1 and INV2 are completely inverted. M1 is then switched to ON-state, which leads to reset PD. Due to the time delay t_d PD is kept charged until the output of INV2 is reverted. This period is the third time interval T3. Repeating these three stages, pulse trains are produced. If the time delay t_d is small, the oscillation frequency f is given as

$$f = \frac{I_{ph}}{C_{PD}\left(V_r - V_{th}\right)} , \quad (1)$$

where V_r is the bias voltage of the reset transistor M1, V_{th} is the threshold voltage of ST. As can be seen from Eq. (1), the frequency f or the firing rate increases if the input light intensity becomes large and the size of PD becomes small.

To confirm fundamental characteristics of the PFM circuits, a test chip was designed using triple-metal double-poly 0.35 µm CMOS process. Figure 2 shows the circuits of the chip. To confirm the frequency dependence on the operation voltage, the bias voltage of the reset transistor M1 is different from the voltage of the inverters. The output of the inverter in the final stage is in open-drain and to output current pulse trains. The layout pattern of one pixel is shown in Fig. 3, where the number of transistors are 10. The photodiode consists of a parasitic pn junction diode between N-diffusion and P-substrate. To demonstrate the size effect of the photodiode only 1µm square hole is opened on the top of the shield metal of the photodiode with the size of 2µm square. The capacitance is estimated around 1fF. The distance from the bottom of the photodiode to the top of the metal is over 2μm, thus the input viewing solid angle of the detector is smaller than one in a photodiode of a conventional image sensor. All of the transistors except for the output transistor have the minimum L/W in the process technology used here.

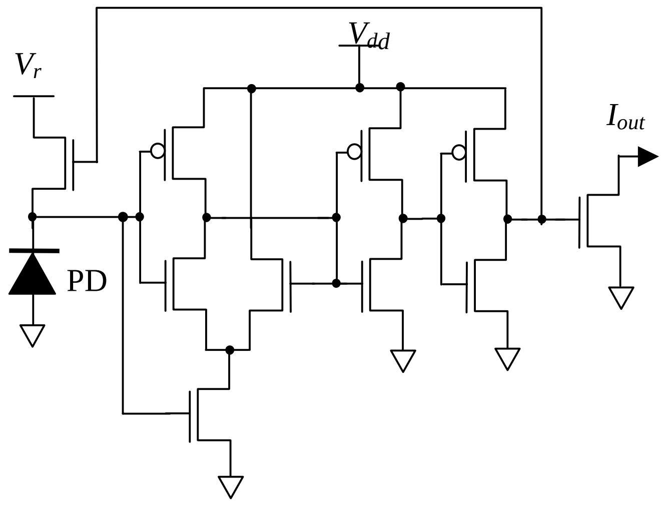

Figure 2: Pixel circuits

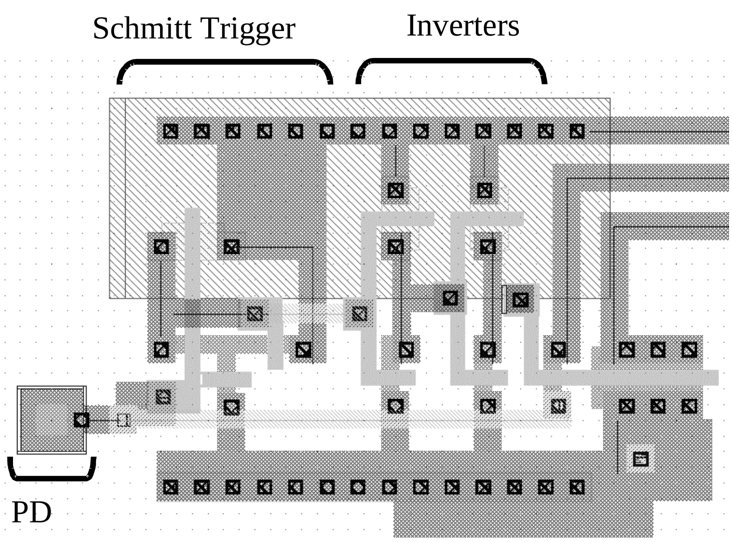

Figure 3: Pixel Layout

Figure 4 shows HSPICE simulation results based on the netlists extracted from the layout in Fig. 3. The input photocurrent changes from 0 to 50 pA in a lump manner. In this case, the maximum input light level corresponds to 100 Klux with the assumption of the quantum efficiency of 10%. The extracted capacitance of the photodiode is around 1 fF. In Fig.4, the simulation was done under three conditions of V_r and V_{dd}. Here V_{dd} is the power supply voltage of the Schmitt trigger and the inverters. This results of the simulation demonstrate that the chip works well under the low voltage of less than 1 V, although it does not work stable in the low input light intensity if V_{dd} is large.

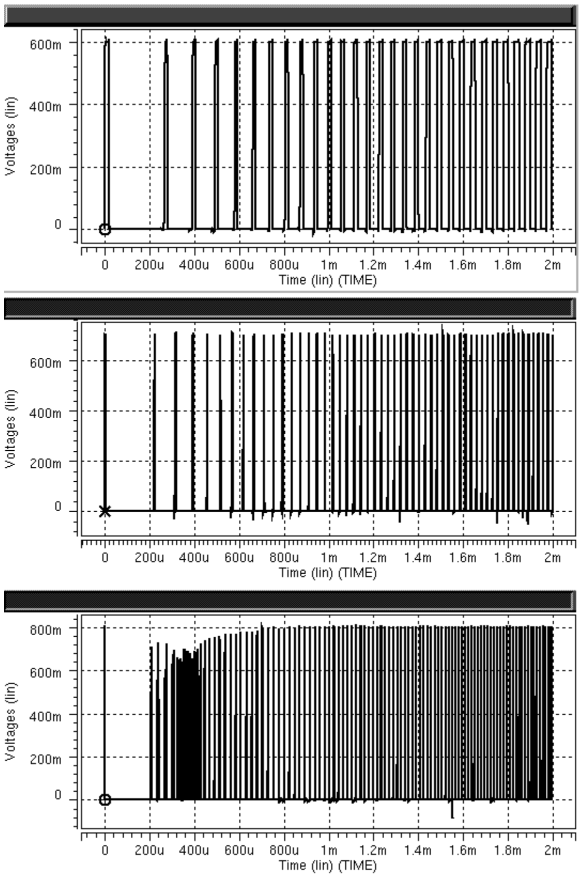

Figure 4: Circuit simulation results. (a) V_{dd}=V_r=0.6V, (b) V_{dd}=V_r=0.7V, (c) V_{dd}=V_r=0.8V.

3. EXPERIMANTAL RESULTS

A halogen lamp was used for the input light source onto the chip. The light intensity varied from around 0.1 lux to 100 Klux by using ND filter with adjusting the input current into the lamp. The output current was converted into the voltage with a off-chip current-to-voltage converter and was monitored the waveforms by an oscilloscope. Figure 5 shows the typical experimental result in the input light intensity of 1 lux.

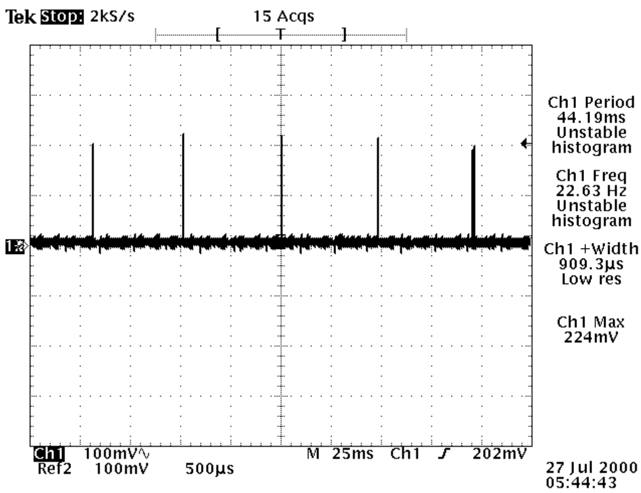

Figure 5: Typical experimental result of output pulse trains. Input light power is 1 lux.

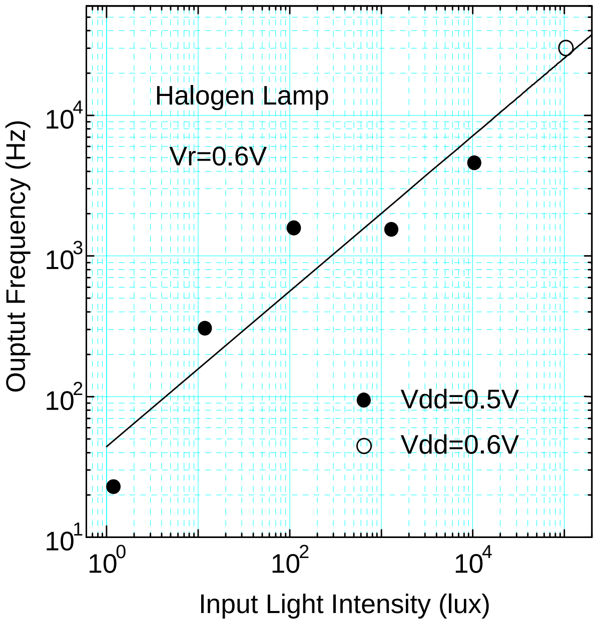

Figure 6: Dependence of output pulse frequency on input light intensity.

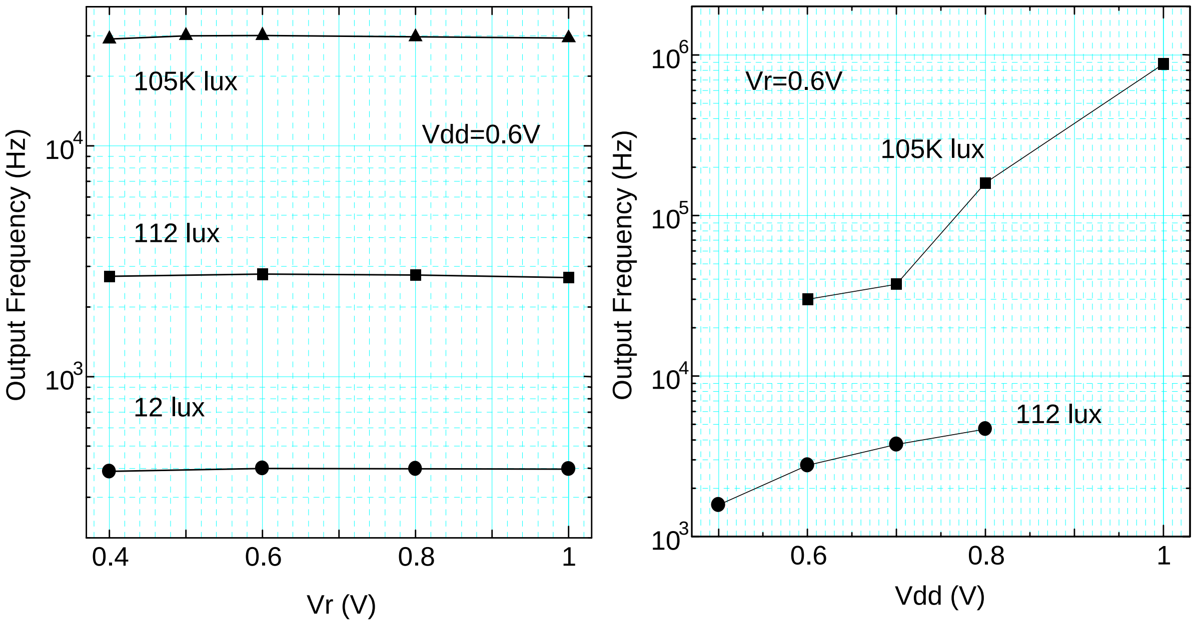

Figure 7: Dependence of output pulse frequency on V_r and V_{dd}..

Figure 6 shows the dependence of the output frequency on the input light intensity. When the operation voltage of the inverters V_{dd} is 0.5V or 0.6V and the reset transistor bias voltage V_r is 0.6V, the dynamic range of over 50 dB is obtained. The maximum input light intensity is limited by the measurement system and thus the value of the dynamic range may be larger.

In Fig. 7 the dependence of the output frequency on V_{dd} and V_r is shown. These results show that the output frequency is little dependent on V_r but is strongly affected by V_{dd}. This is because the delay time and/or the driving capability of the inverter are dependent on the operation voltage.

4. DISCUSSION

To study how the area size affects the output pulse frequency, we have made simulation of the circuits where the capacitance of the photodiode is assumed to be 100 fF. Figure 8 shows the simulation result when the input light intensity varied as the same in Fig. 4 and V_{dd}=V_r=0.6V. This result small size of the photodiode is effective to detection of low light intensity.

The dynamic range of our chip was over 50dB. The minimum detection limit may be determined by a dark current of the photodiode as well as a leak current of the reset transistor. The maximum may be limited by a delay time of the inverters, although it has not been evaluated due to the limit in our measurement system. The minimum and maximum frequency are given by

$$f_{\min} = \frac{I_{leak}}{C_{PD}\left(V_r - V_{th}\right)} , \tag{2}$$

$$f_{\max} = \frac{1}{2t_d} . \tag{3}$$

Here I_{leak} is a leak current of the photodiode, t_d is the total delay time in the feedback loop of the inverters. If the leakage current is assumed a few fA, then the minimum frequency is estimated a few 10 Hz. The delay time is dependent on the operation voltage, thus it is possible to expand the dynamic range by adaptively changing the voltage.

Figure 9 shows the simulation results how V_r influences the output pulse characteristics. The top, middle and bottom traces are output pulse trains with V_r=0.5, 1.0 and 1.5V, respectively, while V_{dd} is kept constant of 0.9V. The pulse width is changed by the bias voltage of the reset transistor. The pulse width becomes large when the reset current is close to the photocurrent, which means resetting the photodiode requires longer time in this case.

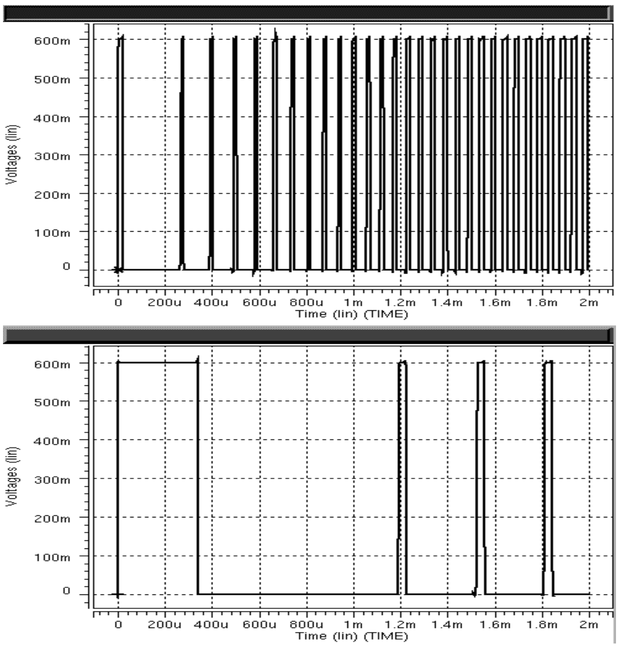

Figure 8: Output pulse characteristics in two types of photodiode size, C_{PD}~1fF (upper) and C_{PD}~100fF (lower)

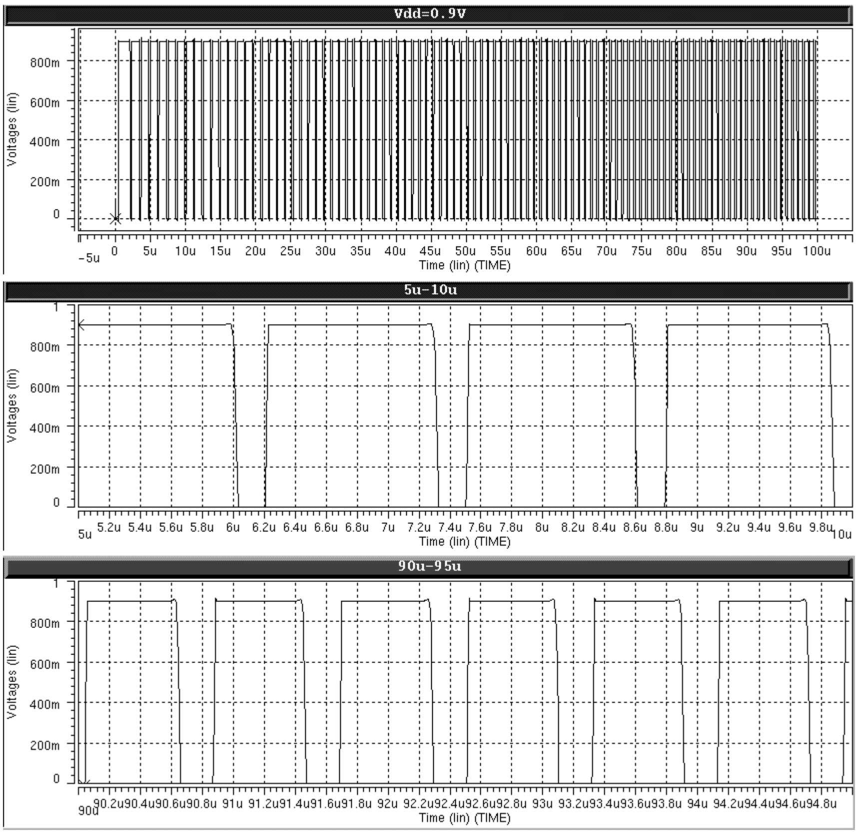

Figure 9: Dependence of output pulse characteristics on V_r.

5. CONCLUSION

We have designed a pixel circuit based on a pulse frequency modulation using 0.35µm 2-poly 3-metal CMOS technology and showed the fundamental characteristics. The chip demonstrates the dynamic range over 50dB under very low operation voltage of less than 1V. A small photodiode with the junction area of 2µm square and the aperture size of 1µm square is effective for such a low voltage operation. We will continue to study the characteristics and focus on expanding the minimum detection limit to enable a photon counting. Another issue is to explore applications to be effective for such a low voltage operation.

ACKNOWLEDGEMENT

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