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Stable tungsten disilicide contacts for surface and thin film resistivity measurements

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High-temperature stable electric contacts of tungsten disilicide (WSi_2) on Si(001) are fabricated by a simple two-step process: vacuum deposition of W on the native Si dioxide and subsequent annealing under ultrahigh-vacuum conditions. Silicidation starts at 1000 K, as, it is believed to occur, the Si diffuses to the surface through the defects in the oxide. Flash annealing to 1500 K removes the oxide, resulting in stable WSi_2 contacts on the surface. Contamination due to migrating W is confined to within a micrometer of the edge of the WSi_2 contacts. Beyond this micrometer-sized zone, the surface is free of contamination as confirmed by low-energy electron microscopy and high-resolution low-energy electron diffraction. Reproducible resistance curves during annealing and cooling of the Si(001) sample confirm the reliability of the contacts, which can withstand many flash-annealing cycles without degradation. © *2009 American Vacuum Society.*
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I. INTRODUCTION

Metal silicides on silicon have been widely studied because of low resistivity and process compatibility for fabricating semiconductor devices.[1,2] Among them, the refractory metal (e.g., vanadium, molybdenum, and tungsten) silicides have drawn special attraction to engineers and researchers because of their high-temperature stability and low resistivity in comparison with doped polycrystalline silicon.[3] In particular, tungsten silicides (WSi_2) have become increasingly useful for contacts and gate electrodes, because they also solve the problem of the gate-depletion phenomena in metal-oxide-semiconductor field-effect transistors (MOSFETs).[4]

Besides these technological aspects, high-quality contacts are equally useful for basic research purposes such as the *in situ* measurement of surface or ultrathin-film resistivity. However, such measurements demand stable contact areas that are compatible with the specific requirements of surface science. In general, the contacts must be ultrahigh-vacuum (UHV) compatible, form an Ohmic contact with the surface layer, exhibit a low resistance, and withstand various preparation procedures. In the case of Si as a substrate, the contact must be thermally and mechanically stable up to flash-annealing temperatures, i.e., 1500 K, without contaminating the remaining Si surface. There has been a concern in the surface-science community that silicide contacts are not stable after repeated flash-annealing cycles of the silicon samples. Most of the metals diffuse across the surface due to their high diffusivity (such as Co, Mn, Fe, and Cr) and most of them generate defects on the surface (e.g., Ni causes ordered missing dimer defects on the Si surface).[5] Titanium silicide exhibits very good electrical conductivity, but still has disadvantages of high-temperature processing limitations.[6,7] To overcome these problems, tungsten offers an alternative.

There have been several techniques proposed so far to fabricate WSi_2 films on Si. These include sputter deposition of WSi_2 on silicon,[3] reacting tungsten with silicon at high temperatures,[8,9] ion-beam synthesis,[10] low-pressure chemical vapor deposition (LPCVD),[11] and co-deposition from separate sources for metal and Si.[12] However, all these processes have some complexity to achieve low-resistivity contacts that are stable up to 1500 K. Therefore, a simple technique of fabricating contacts, which are stable up to such high temperatures, would be extremely helpful to basic research and the technological aspects, as well.

In this article, we report a simple recipe for fabricating thermally stable WSi_2 contacts on Si(001) substrates, which are compatible with classic surface-science sample preparation, i.e., high temperature flash annealing under UHV-conditions without W diffusion or contamination of the area surrounding the contacts. These contacts do not affect the surface structure and surface physics. The surface morphology of the WSi_2 contacts and the Si(001) surface are analyzed by *in situ* spot-profile-analyzing low-energy electron diffraction (SPA-LEED) and *ex situ* scanning electron microscopy (SEM), respectively. Additionally, the change of surface morphology of the silicide structure and the surrounding regions of Si are studied by *in situ* low-energy electron microscopy and photoemission electron microscopy (LEEM/PEEM). The reliability and the quality of the contacts are tested by the resistance measurements of a clean Si(001) substrate under UHV conditions by using a four-point probe (4PP) setup.

II. EXPERIMENT

The WSi_2 contacts were fabricated in a two-step process: deposition of W on a native oxide of a Si(001) substrate (boron-doped, resistivity $= 8-12\ \Omega\,\mathrm{cm}$, miscut $< 0.2°$, and

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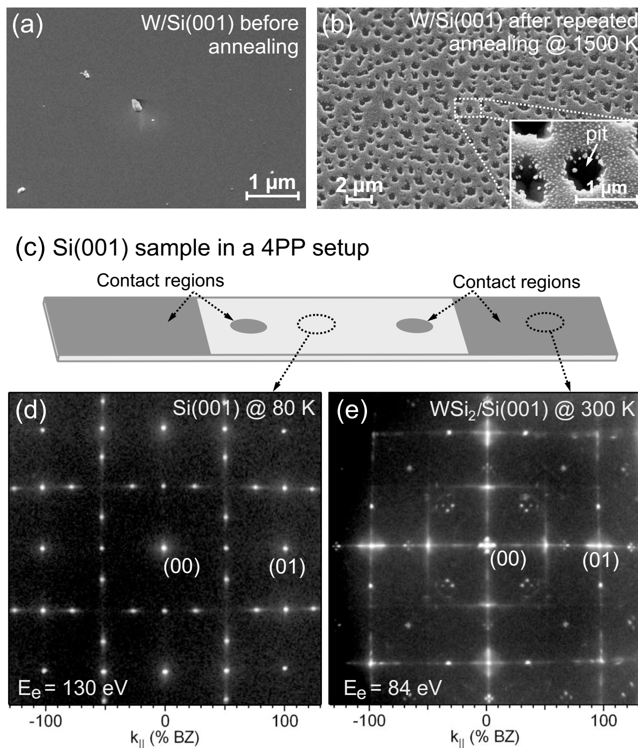

FIG. 1. Surface structure and the morphology at the respective regions on the sample: (a) SEM images of a vacuum-deposited continuous tungsten film before the annealing processes and (b) the surface topography after the annealing processes, with an inset of the magnified image at particular region showing a pit. (c) A sketch of the Si(001) sample with contact regions in a 4PP setup. (d) LEED pattern taken in the center area of the sample, which shows a clear $c(4\times 2)$ reconstruction of Si(001) surface at 80 K. (e) LEED pattern taken in the contact regions at both sides of the sample, where W is deposited, shows additional spots on (2×1) reconstructed Si(001) surface, which appear due to the facets surrounding the pit formed by silicidation process.

dimensions of $l=3.5$ cm, $w=0.4$ cm, and $t=500$ μm) under high-vacuum conditions (base pressure below 1×10^{-7} mbar), followed by subsequent annealing up to 1500 K under UHV conditions (base pressure below 2×10^{-10} mbar). A shadow mask was used to define contact regions on the sample for the resistance measurements. For the deposition, a tungsten wire (material purity of 99.98% and dimensions of length of 6 cm and diameter of 0.015 cm was placed at a distance of 6 cm from the sample and a current of 4 A was supplied until the wire burned out due to the sublimation of W. A homogeneous film of W as shown in Fig. 1(a) resulted from the deposition. *Ex situ* atomic force microscopy (AFM) measurements show that under these deposition conditions the film is 30 nm thick. The actual overall shape of the sample with contact regions is shown in Fig. 1(c).

After the deposition process, the sample was transferred into the UHV chamber and annealed at 1000 K for 5 h, as a first but very important step. The native oxide of the Si surface was then removed by flash annealing to 1500 K for only 3 s. This preparation results in a clear (2×1) LEED pattern at room temperature (only at the area where no tungsten was deposited). After cooling to 80 K, the (2×1) reconstruction undergoes the structural phase transition into a $c(4\times 2)$ reconstruction.[13–15]

It is well known that the $c(4\times 2)$ reconstruction is extremely sensitive to surface defects or contamination since the correlated buckling of Si dimers is destroyed by defects.[16–19] Small traces of metal, especially in the case of W, with a density as low as 6×10^{12} atoms/cm^2, transform the surface from (2×1) reconstruction to a $(2\times n)$ phase, where n is the periodicity length of the missing Si dimers.[19] This fact clearly suggests that the bare part of Si(001) surface is free of contamination, at least beyond the upper limit given by Ref. 19.

To verify that the contacts are stable at high temperatures, the sample was repeatedly flash annealed to 1500 K. *In situ* SPA-LEED (Refs. 20 and 21) measurements were performed to study the surface morphology after the annealing processes. *Ex situ* SEM measurements were performed to study the morphology after several flash-annealing cycles.

Furthermore, the long-term reliability of the contacts was verified by measuring the resistance of the Si substrate, using the WSi_2 contacts in a 4PP technique.

The change of morphology during the silicide formation was studied under UHV conditions by IBM's first-generation LEEM/PEEM prototype.[22] A sample (dimension of 6×6 mm^2) with an array of W structures was prepared by following same procedure as before and inserted into the microscope. To fabricate an array of microscopic W patches on the sample, a silicon nitride (SiN) shadow mask with dimensions below 100 μm was used during W deposition. The sample was annealed by following the same recipe as described earlier, and the alloying of the W with the Si was monitored by real-time PEEM.

III. RESULTS

LEED measurements were performed in two different regions: the contact regions of the sample, where W was deposited, and in the center of the sample. A sketch of the sample with these different regions and the respective LEED patterns are shown in Fig. 1(c). The LEED pattern of the large area of the sample, where no W was deposited, exhibits the sharp spots of a clean Si(001) surface at 80 K [cf. Fig. 1(d)]. The surface shows a $c(4\times 2)$ reconstruction in two rotational domains. The LEED pattern of the WSi_2 contact regions exhibits additional spots near the spots of Si-(2×1), as shown in Fig. 1(e). These spots move in reciprocal space upon changes of the electron energy and reflect the presence of (111) facets. These facets are attributed to the Si substrate. The polycrystalline WSi_2 does not form sharp diffraction spots with sufficient intensity to show up in the LEED
pattern.

For the topographic information, the sample was investigated by *ex situ* SEM. The continuous W film as shown in Fig. 1(a) was transformed into a WSi_2 film with a high number of micropits [Fig. 1(b)]. These pits start at the top of the silicide and go deep into the Si bulk. The micropits are also

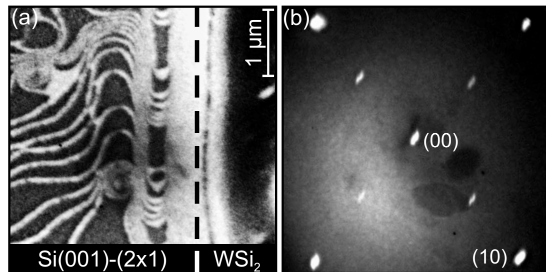

FIG. 2. (a) LEEM-dark-field (DF) image taken around the edge of the WSi_2 patch. Si terraces of both (2×1) and (1×2) reconstructed surfaces appear as bright and dark. The dotted line roughly indicates the boundary between the WSi_2 patch and the Si(001) surface. (b) Microdiffraction pattern of clean Si(001) surface taken in between the patches at room temperature.

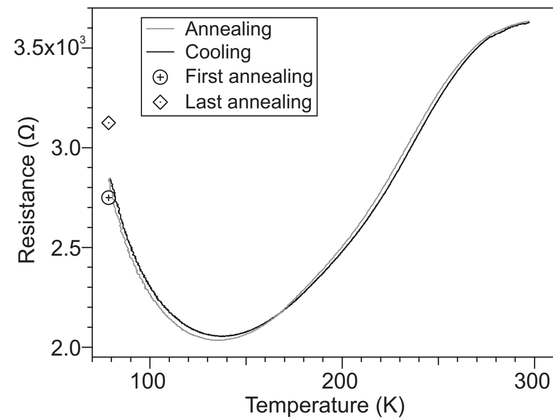

FIG. 3. Annealing behavior of the resistance of the Si(001) sample measured by using the WSi_2 contacts in a 4PP setup as shown in Fig. 1(c). The dark-gray line represents the annealing curve and the light-gray line shows the cooling curve. The measurement was carried out one after the another without breaking. Two different symbols indicate the resistance of the bare Si sample measured at 80 K after the very first flash-annealing and after 30 flash-annealing cycles (the last annealing process) in the course of measurements.

responsible for the additional LEED spots that we observe in the contact area of the sample. The facet spots originate from the side walls of the pits, which consist of Si. The pits are not connected to each other, however, which suggests that there is a continuous path for the electric current on the WSi_2 contact area.

The silicidation process of W pads was also studied with *in situ* LEEM and PEEM. During flash annealing, the size and shape of the patches remained constant, even after many heating cycles. We never observed a spreading out of the patch over the surface. The brightness of the patches and their surrounding, however, changed to reflect the structural change of the W patches and the desorption of SiO_2 in the vicinity of the patches during the initial flash. Figure 2 summarizes the LEEM/PEEM results. Panel (a) shows a dark-field LEEM image of a part of a WSi_2 patch with the surrounding Si. Under dark-field imaging conditions in LEEM, one domain of the (2×1) reconstructed Si(001) terraces is imaged in bright, whereas the other domain appears dark. Thus, in the left side of the panel (a), the alternating sequence of bright and dark stripes indicates an undisturbed sequence of clean and reconstructed Si(001) terraces, separated by single steps. It is not surprising that microdiffraction patterns from this area on the surface [one example reproduced in panel (b)] show a Si(001)-(2×1) diffraction pattern without any indication of W contamination. Closer to the WSi_2 patch, which appears as a dark stripe on the right side of Fig. 2(a), the featureless gray area indicates that the step density is higher in the vicinity of the WSi_2 patch. AFM measurements show deep grooves with (111) side facets that surround the WSi_2 patches, indicating that the Si has been taken from these areas for the formation of WSi_2. Not surprisingly, microdiffraction patterns of the WSi_2 patch reveal a polycrystalline composition.

We believe that the grooves around the microscopic patches that we observed in the LEEM/PEEM system fulfill the same purpose as the micropits in the larger patches that we used in the SPA-LEED system, i.e., they provide the material for the silicidation. If the contacts are small enough, as in the LEEM/PEEM case, the material is transported from the sides of the contact patches, leaving the patch surrounded by grooves. Larger contact areas do not have that option, because their dimensions are bigger than the Si diffusion length for diffusion of Si on WSi_2. As a result, Si is transported through cracks in the oxide and leaves micropits. This interpretation is supported by the fact that we do not observe micropits in the small contact areas in the LEEM.

Although the contacts between the WSi_2 and the Si exhibit Schottky-diode behaviors, the characteristics of the individual contact can be bypassed by using a 4PP setup for surface resistivity measurements. In these experiments, where temperatures are changed and films are grown, it is more crucial that the contacts do not peel off and exhibit long-term stability and reproducibility. The reliability of the contacts was checked via resistance measurements of the Si(001) sample using a 4PP setup during the annealing and cooling of the sample from 80 to 300 K and vice versa. The curve in Fig. 3 shows the expected resistance behavior of low-doped silicon.[23] Initially, the resistivity decreases due to the ionization of dopants. Around 150 K, the ionization process saturates completely, whereas the carrier density remains unaltered. Above 150 K, the carrier mobility changes with temperature by the carrier-carrier and the carrier-lattice scattering processes, causing an increase of resistance. A small deviation of the cooling curve with respect to the annealing curve was observed due to a small hysteresis during the cooling and annealing cycle. This resistance curve of the silicon substrate was reproduced even after many flash-annealing cycles of the sample. However, the resistance increases slightly after 30 flash-annealing cycles in several days of experiments (see Fig. 3).

IV. DISCUSSION

The solid-phase reaction between W and Si starts during the first annealing step at 1000 K.[24] The oxide layer that separates the Si surface from the W pads, however, prevents a direct reaction between the two. Because there are no ther-

modynamically favorable reaction products found between W and SiO_2 at any temperature,[25] another mechanism is necessary to enable silicide formation. Oxide films often exhibit defects such as microchannels or pinholes[25–27] that are initially present in the native SiO_2 layer, and these are the most likely candidates for the beginning of necessary atomic transport through the oxide. At such intrinsic oxide defects, W atoms or Si atoms might be able to migrate through the oxide to the Si/SiO_2 interface or to the W/SiO_2 interface, respectively. The bulk diffusion of W through SiO_2, however, is too low for effective W mass transport. In contrast, the migration of Si atoms through defects in the oxide to the surface already occurs at 850 K.[28] During flash annealing at 1500 K, the Si reacts with SiO_2 and forms a volatile silicon monoxide (SiO) that already desorbs at 1250 K.

Once the SiO_2 is desorbed, the silicidation of Si from the bulk with the W patches leaves the surface covered with WSi_2 structures, as shown in the SEM image of Fig. 1(b). The Si necessary for the alloying process is removed either from the surroundings of the W patches, or, if the contacts are too large to effectively transport Si from the sides to the center of the patch, from the Si below the W patch. In the first case, the patch will be surrounded by grooves with (111) side facets; in the second case, the patches will exhibit micropits with (111) side facets. Nevertheless, once formed, the contacts remain stable and unchanged, even after at least 50 flash-annealing cycles to 1500 K. Identical LEED patterns were obtained after each cycle of flash annealing [Figs. 1(d) and 1(e)], and PEEM did not show any evidence of morphological changes of the contacts during the repeated annealing cycles. The dark-field image in Fig. 2(a) confirms that the Si surface only a few micrometers away from the contact is clean and free of contamination, and the surface remains clean even after many flash-annealing cycles.

One important point that should be emphasized is the annealing at 1000 K for 5 h before the first flash annealing to 1500 K, which seems essential to achieve stable WSi_2 in the contact regions and a clean Si(001) surface in the regions where no W was deposited. We believe that the silicide formation during the first annealing step at 1000 K may have prevented diffusion of W across the oxide or Si surface at higher temperatures. In contrast, we observed a W-contaminated Si(001) surface when we performed a direct flash-annealing of the sample to 1500 K, without performing the first annealing step. This is in agreement with a previous study of formation of epitaxial WSi_2 films on Si(111).[29]

The reproducible resistance curves (Fig. 3) during annealing and cooling confirm that the high-temperature annealing step provides stable and metallic silicide contacts. Previous studies have reported that WSi_2 undergoes a phase transition from a low-temperature hexagonal crystal to a high-temperature tetragonal crystal.[12,29–32] Moreover, they have concluded that the low-temperature phase is semiconducting and the high-temperature phase is metallic and stable.[12,29] Obviously, we observe the stable high-temperature phase of WSi_2.

V. CONCLUSION

We presented a simple and easy-to-use recipe to fabricate metallic WSi_2 contacts for surface conductivity studies on Si surfaces. The contacts are mechanically stable and reliably withstand many flash-annealing cycles up to 1500 K. No contamination of the bare Si surface at distances larger than 2 μm from the contacts via diffusion of W atoms was detected during the course of these experiments. Here, we have used both macroscopic and microscopic contacts, which illustrate that the contact areas can be scaled down to allow a wide application of the technique.

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