UNIVERSITI PUTRA MALAYSIA

MULTIPLE AND SOLID DATA BACKGROUND SCHEME FOR TESTING STATIC SINGLE CELL FAULTS ON SRAM MEMORIES

NOR AZURA ZAKRIA

MULTIPLE AND SOLID DATA BACKGROUND SCHEME FOR TESTING STATIC SINGLE CELL FAULTS ON SRAM MEMORIES

By

NOR AZURA BINTI ZAKARIA

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfillment of the Requirements for the Degree of Master of Science

August 2013

DEDICATION

This thesis is dedicated to my beloved family;

Syed Al Firdaus Jamallulail B Syed Ahmad,

Sharifah Shahida Husna, Syed Mohd Nazim

and Sharifah Nurhana.

Appreciate your sacrifices.

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the degree of Master of Science

MULTIPLE AND SOLID DATA BACKGROUND SCHEME FOR TESTING STATIC SINGLE CELL FAULTS ON SRAM MEMORIES

By

NOR AZURA BINTI ZAKARIA

August 2013

Chairman : Associate Professor Wan Zuha Wan Hasan, PhD
Faculty : Engineering

Memory testing is a method that requires an algorithm capable of detecting faulty memory as comprehensively as possible to facilitate the efficient manufacture of fault free memory products. Therefore, the purpose of this thesis is to introduce a Data Background (DB) scheme to generate an optimal March Test Algorithm (MTA) for detecting faults of memory that are undetectable using existing algorithms. The present research focuses on two types of Static Single Cell Faults (SSCFs): Write Disturb Faults (WDFs) and Deceptive Read Destructive Faults (DRDFs). These faults are undetectable by existing algorithms with insufficient operation. To date, the main effort in this field of research is to improve fault detection by modifying or adding an operation sequence in the MTA. A relatively small number of test approaches have worked on the DB scheme instead of the MTA to improve fault coverage. However, these approaches were designed to improve the fault coverage for detectable faults only. Thus, the present research develops a new DB scheme to be applied to existing MTA to detect two WDFs and two DRDFs.

Two methods are proposed in this project. In Method 1, a multiple DBs generator with a bit-adjacent DB management scheme is applied for the selected MTA. This method is evaluated in terms of function and performance differences between the proposed MTA and existing MTA using the User Defined Algorithm (UDA) available in the MBISTArchitect tool. Findings show that both MTAs have the same testing time. However, the existing MTA of the Memory Built-In-Self Test (MBIST) required a bigger area overhead and consumed more power. Hence, Method 1 is not suitable to be used with the MBIST for System on Chip (SoC).

For Method 2, suitable solid DBs are used to provide higher fault coverage instead of using the existing MTA. The new MTA is defined by designing an automation program called DB generator. The DB generator computes all the possible DBs and filters the list of preferable DBs using efficient combination logic. The proposed MTA is obtained after the eliminating procedure of the preferable DB list using the SQ generation rule. Finally, the fault coverage will be calculated manually by doing fault evaluation analysis using Fault Primitives (FP) rules. Results show that WDFs and DRDFs are successfully detected with each proposed MTA. The proposed MTAs are also able to detect other SSCFs, such as Transition Fault, Stuck-At Fault, Incorrect Read Fault, Read Destructive Fault, and State Fault. Finally, based on the SQ generation rule, and the development of the DB generator, MTAs are generated. The present research demonstrates that the DB generator and proposed MTAs, such as March CL-1, March Cl-2, March SR-1, and March SR-2, are successfully applied and designed, with up to 100% fault coverage.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

SKIM LATAR BELAKANG DATA PELBAGAI DAN PADU UNTUK MENGESAN KESALAHAN SEL TUNGGAL STATIK DALAM MEMORI SRAM

Oleh

NOR AZURA BINTI ZAKARIA

Ogos 2013

Pengerusi : Profesor Madya Wan Zuha Wan Hasan, PhD
Fakulti : Kejuruteraan

Ujikaji memori merupakan teknik penting yang memerlukan algoritma yang baik bagi mengesan kesalahan memori dengan kadar liputan yang tinggi untuk menghasilkan produk memori tanpa kesalahan. Oleh itu, objektif tesis ini adalah memperkenalkan skim data yang bersesuaian untuk diguna pakai dalam Algoritma March (MTA) untuk mengesan dua jenis kesalahan sel tunggal statik memori iaitu kesalahan "Write Disturb Faults" (WDFs) dan "Deceptive Read Destructive Faults" (DRDFs). Hasil kerja penyelidikan sebelum ini, didapati MTA yang diperkenalkan gagal untuk mengesan kesalahan-kesalahan tersebut dalam masa ujian yang sesuai. Pelbagai usaha telah dibuat untuk meningkatkan kadar pengesanan kesalahan dengan kaedah mengubah atau menambah turutan operasi di dalam MTA. Tetapi kaedah ini tidak sesuai kerana ia akan meningkatkan masa ujian. Sebaliknya, terdapat beberapa penyelidikan terdahulu telah membuktikan dengan menggunakan skim latar belakang data (DB) di dalam MTA, kadar pengesanan kesalahan adalah tinggi dan penggunaan masa ujian yang pendek. Walau bagaimanapun, penyelidikan terdahulu hanya mengesan kesalahan konvensional sahaja. Oleh yang demikian, satu kajian susulan haruslah dibuat untuk menghasilkan kaedah baru dengan menghasilkan DB yang baru untuk mengatasi kelemahan algoritma.

Terdapat dua kaedah yang telah digunakan dalam projek ini. Dalam Kaedah 1, penjanaan pelbagai DB dilakukan dengan skim pengurusan DB pada MTA yang terpilih. Hasilnya, MTA yang dijana dengan DB baru berjaya mengesan kesalahan tersebut. Kaedah ini telah dinilai dari segi prestasi dan fungsi pada setiap MTA baru dan konvensional. Setiap MTA diperterjemahkan kepada perkakasan rekabentuk ujian dalaman memori (MBIST) dengan menggunakan perisian MBISTArchitect. Dari hasil penilaian, didapati kedua-dua simulasi mempunyai masa ujian yang sama.

Walau bagaimanapun, rekabentuk MBIST yang dihasilkan mempunyai saiz yang lebih besar dan penggunaan kuasa elektrik yang tinggi. Oleh itu, Kaedah 1 tidak sesuai untuk digunakan untuk system cip memori (SoC).

Bagi Kaedah 2, penghasilan DB padu (solid DB) yang sesuai di dalam MTA hendaklah digunakan untuk mencapai liputan pengesanan kesalahan yang lebih tinggi berbanding menggunakan MTA sedia ada. MTA baru dijana dengan bentuk program automasi dipanggil penjana DB. Penjana DB mengambil kira semua DB dan menapis senarai DB menggunakan gabungan logik yang cekap. Cadangan MTA diperoleh dengan mengikuti prosedur ujian yang dicadangkan menggunakan peraturan generasi SQ. Akhirnya, liputan kesalahan akan dikira secara manual dengan melakukan analisis penilaian kesalahan berpandukan peraturan Primitif Kerosakan Primitif (FP). Keputusan menunjukkan bahawa WDFs dan DRDFs berjaya dikesan dengan setiap penghasilan MTA. MTA yang dihasilkan juga dapat mengesan SSCFs lain, seperti "Transition Fault" , "Stuck-At Fault", "Incorrect Read Fault", "Read Destructive Fault", and "State Fault". Hasil penyelidikan menunjukkan bahawa penjana DB dan MTA yang dicadangkan, seperti March CL-1, March Cl-2, March SR-1, dan March SR-2, berjaya dijana dengan liputan kesalahan sehingga 100%.

ACKNOWLEDGEMENT

Alhamdulillah.

Great thanks and appreciation goes to my supervisory committee, Dr Wan Zuha Wan Hasan, Dr Izhal Abd. Halin and Dr Roslina Mohd Sidek. Special thank goes to my family and friends (Masnita, Julie, Ammad Udin, Solmaz, Aiman, Zarina, Firdaus et al.) for all the support.

I certify that a Thesis Examination Committee has met on 2 August 2013 to conduct the final examination of Nor Azura binti Zakaria on her thesis entitled "Multiple and Solid Data Background Scheme for Testing Static Single Cell Faults on SRAM Memories" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Master of Science.

Members of the Thesis Examination Committee were as follows:

Suhaidi bin Shafie, PhD
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

Nurul Amziah binti Md Yunus, PhD
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Internal Examiner)

M. Iqbal bin Saripan, PhD
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Internal Examiner)

Abu Khari A'ain, PhD
Professor
Universiti Teknologi Malaysia
Malaysia
(External Examiner)

NORITAH OMAR, PhD
Associate Professor and Deputy Dean
School of Graduate Studies
Universiti Putra Malaysia

Date: 20 November 2013

This thesis was submitted to the Senate of the Universiti Putra Malaysia and has been accepted as fulfillment of the requirement for the degree of Master of Science. The members of the Supervisory Committee were as follows:

Wan Zuha Wan Hasan, PhD
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

Izhal Abd Halin, PhD
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Member)

Roslina Mohd. Sidek, PhD
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Member)

BUJANG KIM HUAT, PhD
Professor and Dean
School of Graduate Studies
Universiti Putra Malaysia

Date:

Declaration by graduate student

I hereby confirm that:

- this thesis is my original work;
- quotations, illustrations and citations have been duly referenced;
- this thesis has not been submitted previously or concurrently for any other degree at any institutions;
- intellectual property from the thesis and copyright of thesis are fully-owned by Universiti Putra Malaysia, as according to the Universiti Putra Malaysia (Research) Rules 2012;
- written permission must be obtained from supervisor and the office of Deputy Vice-Chancellor (Research and innovation) before thesis is published (in the form of written, printed or in electronic form) including books, journals, modules, proceedings, popular writings, seminar papers, manuscripts, posters, reports, lecture notes, learning modules or any other materials as stated in the Universiti Putra Malaysia (Research) Rules 2012;
- there is no plagiarism or data falsification/fabrication in the thesis, and scholarly integrity is upheld as according to the Universiti Putra Malaysia (Graduate Studies) Rules 2003 (Revision 2012-2013) and the Universiti Putra Malaysia (Research) Rules 2012. The thesis has undergone plagiarism detection software

Signature: _____ Date: _____

Name and Matric No: Nor Azura Binti Zakaria, GS22143

Declaration by Members of Supervisory Committee

This is to confirm that:

- the research conducted and the writing of this thesis was under our supervision;
- supervision responsibilities as stated in the Universiti Putra Malaysia (Graduate Studies) Rules 2003 (Revision 2012-2013) were adhered to.

Signature: _____
Name of Chairman of Supervisory Committee: Associate Professor Dr. Wan Zuha Wan Hasan

Signature: _____
Name of Member of Supervisory Committee: Dr. Izhal Abd Halin

Signature: _____
Name of Member of Supervisory Committee: Associate Professor Dr. Roslina Mohd. Sidek

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

<U̶/0>	Stuck At Zero notation
<U̶/1>	Stuck At One notation
⇑	increasing address order
⇓	decreasing address order
⇳	arbitrary address order
BIST	Built In Self Test
BL	Bit Line
BLB	Complementary Bit Line
BOM	Bit Oriented Test Memories
CFdrds	Coupling Deceptive Destructive Faults
CFid	Coupling Idempotent Fault
CFin	Coupling Inversion Fault
CFst	Coupling State Faults
CFtrs	Coupling Transition Faults
CFwds	Coupling Write Disturb Faults
CMOS	Complementary Metal Oxide Semiconductor
DB	Data Background
DFT	Design for Testability
DPM	Defective Parts Per Million
DRAM	Dynamic Random Access Memories
DRDF< 0r0/1/0>	Deceptive Read Destructive Fault Zero
DRDF<1r1/0/1>	Deceptive Read Destructive Fault One
DRDFs	Deceptive Read Disturb Faults
DRT	Data Retention Test

FFMs	Functional Fault Models
FFPs	Functional Fault Primitives
FSMs	Finite State Machines
ICs	Integrated Circuits
IFA	Inductive Fault Analysis
IFA	Inductive Fault Analysis
IRF <r0/0/1>	Incorrect Read Fault Zero
IRF <r1/1/0>	Incorrect Read Fault One
IRFs	Incorrect Read Faults
ITRS	International Technology Roadmap for Semiconductor
LSI	Large Scale Integration
MBIST	Memory Built In Self Test
ME	March element
ME	March Element
MTA	March Test Algorithm
MUT	Memories Under Test
r0	read 0 operation
R0	reading operation
r1	read 1 operation
RAM	Random Access Memories
RAMSES	Random Access Memory Simulator for Error Screening
RDF <0r0/1/1>	Read Destructive Fault Zero
RDF <1r1/0/0>	Read Destructive Fault One
RDFs	Read Disturb Faults
ROM	Read Only Memory
RTL	Register Transfer Level

S0	State 0
SAF0	Stuck At Fault Zero
SAF1	Stuck At Fault One
SAFs	Stuck At Faults
SDCFs	Static Double Cell Faults
SF <0/1/->	State Fault One
SF <1/0/->	State Fault Zero
SFs	State Faults
SoC	System On Chip
SOF	Stuck Open Fault
SQ	New Sequence of Writing Operations
SRAM	Static Random Access Memories
SSCFs	Static Single Cell Faults
TAGS	Test Algorithm Generation by Simulation
TF <↑/0>	Transition Up notation
TF <↓/1>)	Transition Down notation
TFs	Transition Faults
TPG	Test Pattern Graph
TSMC	Taiwan Semiconductor Manufacturing Company
UDA	User Defined Algrithm
ULSI	Ultra Large Scale Integration
VDSM	Very Deep Submicron
VLSI	Very Large Scale Integration
w0	write 0 operation
w1	write 1 operation
WDF<0w0/1/->	Write Destructive Fault Zero

WDF<1w1/0/->	Write Destructive Fault One
WDFs	Write Disturb Faults
WL	Word Line
WOM	Word Oriented Test Memories

CHAPTER 1

INTRODUCTION

1.1 Research Background

Static Random Access Memory (SRAM) has become an indispensable component of digital systems. It is used for specified capabilities for standalone products or embedded memories in System on Chip (SoC) products. The number of SRAM cores used in SoC products is increasing dramatically because of the need to facilitate multiple applications simultaneously. Moreover, technology scaling will lead to smaller feature sizes while enabling a huge number of CMOS (Complementary Metal Oxide Semiconductor) transistors to be fabricated into a single chip (Wang et al., 2006). However, the smaller feature sizes of the transistor will increase the density of the cell array (Akashe et al., 2011), leading to the risk of unknown defects occurring in the memory cells (Fonseca et al., 2010).

Figure 1.1 : Memory Dominance on Silicon (Schrader, 2005)

It was reported by Schrader et al., (2005) that the memory component dominates the SoC by silicon area, as shown in Figure 1.1. Figure 1.2 (Executive Summary, 2011) shows that the function size, including memory size, is becoming smaller, thus increasing the likelihood of defect occurrence. Achieving a high memory yield requires understanding memory designs, modeling their faulty behaviors in the presence of defects, and designing adequate tests with minimum area overhead as well as efficient repair schemes (Hamdioui et al., 2004).

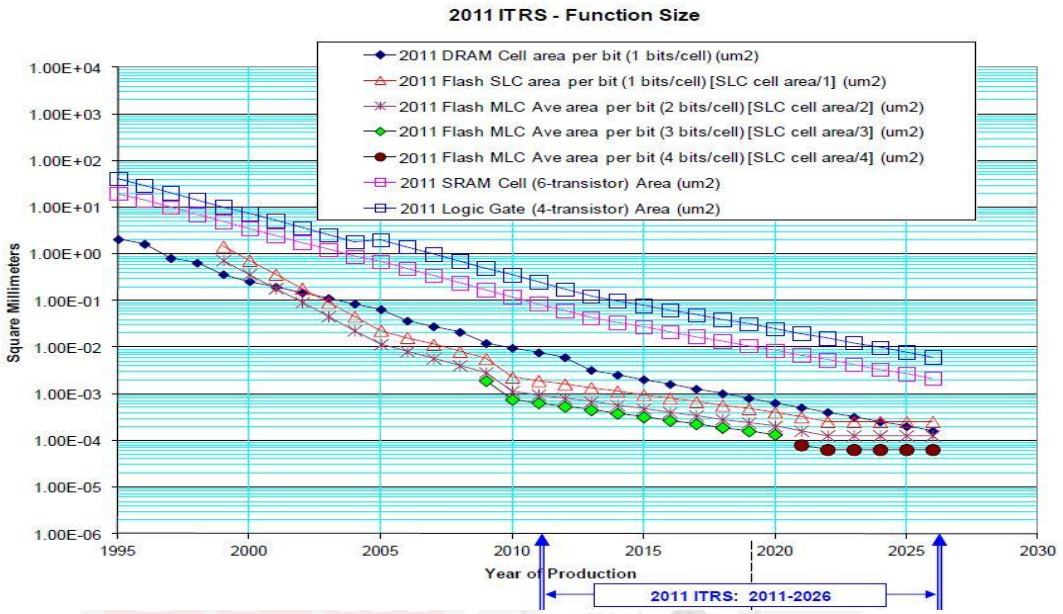

Figure 1.2 : 2011 ITRS Product Function Size Trends: MPU Logic Gate Size (4-transistor); Memory Cell Size [SRAM (6-transistor); Flash (SLC and MLC), and DRAM (transistor + capacitor)] (Executive Summary, 2011)

In CMOS testing, defects occur due to the failure mode being prompted by the manifestation of a defect at the electrical level. Typically, failure modes are modeled as faults at the logic level abstraction of a physical defect. Fault abstractions or fault modeling provide the number of conditions that must be considered in deriving tests. To trace the substance of physical defect in memory testing, the test procedure is created based on the definition of the fault model (FM) described in fault primitives (FP).

```
(March element ⇑ (r0, w1))
for cell := 0 to n - 1 do
begin
read Memory[cell]; {expected value = 0);
write 1 to Memory[cell];
end;
{March element ⇓ (r1, w0)]
for cell := n - 1 downto 0 do
begin
read Memory[cell]; {expected value = 1);
write 0 to Memory[cell];
end;
```

Figure 1.3 : Example of a March Test (Van de Goor et al., p19, 1990)

Normally, embedded memory testing is tested by the developed a test algorithm known as a March Test Algorithm (MTA), as in Figure 1.3. Nair et al. (1978) first proposed an Algorithm Test Sequence to test stuck at fault physical defects with an optimum 4N test operation; later, Suk et al. (1981) proposed the MTA, with a 16N test procedure to test coupling faults. A detailed discussion of the MTA's operation in fault detection can be found in Chapter 3. Basically, an MTA is developed based on the test procedure; the MTA consists of a sequence set of March elements containing writing and reading operations. An example of the March element is described in Figure 1.3. An example of a March element is (w0,r1), where 'w0' is writing a 0 into each cell and 'r1' is reading each cell with an expected 1 value. A memory cell is deemed faulty if the reading results show a 0 value. In Figure 1.3, the operation of "⇑ (r0, w1)" means reading a 0 and writing a 1 into the memory cell with an ascending address order from the lowest address to highest address. The operation of "⇓ (r1, w0)" means reading a 1 and writing a 0 into the memory cell with descending address order, '⇓' from the highest to the lowest address.

The test area can range in size from that appropriate for an LSI (Large Scale Integration) chip to that appropriate for an Ultra Large Scale Integration (ULSI) chip due to the rapid scaling of semiconductor devices. Therefore, the traditional test algorithms are no longer sufficient for testing various faults in standalone memories and embedded memories in SoC contexts. Thus, the development of efficient and effective testing procedures is essential to detect the defects that are expected to occur in SRAM.

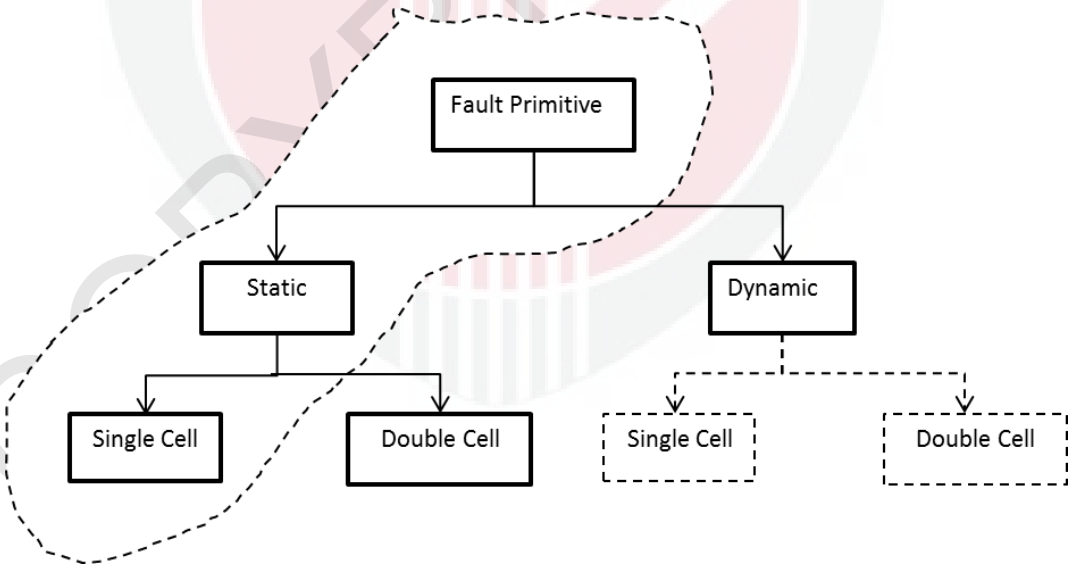

Figure 1.4 : Fault Classification

The CMOS process technology necessary for the dominant memories to be equipped into the ULSI silicon chip is under 180nm and below. SRAM testing under this process technology can be classified into two categories: dynamic and static faults (Figure 1.4). Static faults are FPs that sensitizes a fault by performing one operation; dynamic faults are FPs that performs more than one operation sequentially in order to sensitize a fault (Hamdioui et al., 2004). Until now, static faults have been a predominant fault class model of the memory cell, and numerous researches on the characteristics of static faults in CMOS memory and development of effective MTAs are still being conducted. Therefore, the focus of the present research, as highlighted in Figure 1.4, is to test Static Single Cell Faults (SSCFs). There are six types of SSCFs: Transition Faults (TFs), State Faults (SFs), Write Disturb Faults (WDFs), Read Disturb Faults (RDFs), Incorrect Read Faults (IRFs), and Deceptive Read Disturb Faults (DRDFs) (Van de Goor et al., 2000). The research conducted will also observe the detection of Static Double Cell Faults (SDCFs), such as Coupling Transition Faults (CFtr), Coupling Deceptive Destructive Faults (CFdrds), and Coupling Write Disturb Faults (CFwds) (Van de Goor et al., 2000).

1.2 Problem Statement

Over the years, the fault characterizations of ULSI chip fabrication in Very Deep Submicron (VDSM) CMOS process technology has become more challenging because of new faults arising that are not fully covered by the existing MTAs. Thus, the investigation of the SRAM testing approach involves functional fault models and MTA definition (Hamdioui et al., 2004). Therefore, in order to define the efficient MTAs required for VDSM technology, some problems need to be identified and addressed, such as undetectable static single cell faults (e.g., WDF and DRDF). Previously, these faults could not be detected by Van de Goor et al., (2000), Zordan et al., (2011), or Vardanian et al., (2002), as shown in Table 1.1. The undetected faults of WDF and DRDF have been tabulated in gray colored columns in the table.

Table 1.1 : Fault Detection on Single Static Cell Faults by March Test

March Algorithm (Authors)	Fault Detection Results						
	SAF	SF	TF	WDF	RDF	DRDF	IRF
MATS+ (Van de Goor et al. (2002) and Zordan et al. (2011))	2/2	2/2	2/2	0/2	2/2	0/2	2/2
March C- (Van de Goor et al. (2002) and Zordan et al. (2011))	2/2	2/2	2/2	0/2	2/2	0/2	2/2
March SR (Van de Goor et al. (2002) and Zordan et al. (2011))	2/2	2/2	2/2	0/2	2/2	2/2	2/2
March CL (Vardanian & Zorian, 2002)	2/2	2/2	2/2	0/2	2/2	1/2	2/2

Table Notation:
0/2 – None of the faults are detected.
1/2 - One of the faults is detected.
2/2- Both faults are detected.
Each fault is divided into two types of faults; e.g., SAF is divided to SAF0 and SAF1.

From Table 1.1, it is shown that the MATS+(4N) and March C- (10N) algorithms failed to detect DRDFs and WDFs, March CL (12N) and March SR (14N) failed to detect WDFs, and March CL (12N) was only able to detect fault DRDFs faults. Based on the analysis, there are two assumptions can be made concerning how these shortcomings occur. One is that the faults cannot be detected due to the test sequence of the test algorithm's inability to fulfill its Functional Fault Primitives (FFPs) for both (Van de Goor and Al-Ars, 2002). The second is that the Data Background (DB) used in the MTA is inappropriate to detect the SRAM faults (Wu et al., 1999).

Weaknesses of an algorithm depend on the effectiveness of the operational test and operational data background set. An algorithm can be carried out in accordance with testing bit by bit, classified under Bit Oriented Test Memories (BOM), and testing word by word, classified under Word Oriented Test Memories (WOM) (Van de Goor et al., 1998). Effectiveness is achieved if an algorithm is said to have complete coverage for detecting faults in a short time rate (Wang et al., 2006; Wan Hassan et al., 2006). Shorter test times will reduce the cost of testing, resulting in low-cost production of the mass-manufactured chips (Hamdioui et al., 2000).

Previously, researchers have produced a number of improvements to MTAs by adding N operations to enable the testing of previously undetected faults (Hamdioui et al., 2002; Hamdioui et al., 2003; Vardanian et al., 2002; Harutunyan et al., 2007; Harutyunyan et al., 2012; Hamdioui et al., 2002; Hamdioui et al., 2003; Vardanian et al., 2002; Harutunyan et al., 2007; Zordan et al., 2011; Harutyunyan et al., 2012). By adding N operations, the test time will be increased, thus increasing test cost.

Table 1.2 : Test Approaches Using Various Types of DBs

March Test Algorithm (Author)	Solid DBs	Multiple DBs	Conventional Fault (SF)	Improvement Coverage	Static Single Cell Fault	Coverage
RAMSES (Wu et al., 1999)	Yes	Yes (Varies up to 8 DB)	Yes (STAF, TF)	100%	No	NIL
Data Background Generator (Wang et al., 2002)	Yes	No	Yes (STAF, TF)	100%	No	NIL
Detecting Fault Under Bit Line Coupling (Irobi et al., 2010)	No	Yes	Yes	100%	Yes (SF, DRDF, WDF, IRF, RDF)	100% at March m-MSS but not March SR, March C-, or MATS++
Proposed Method	Yes	Yes	Yes (STAF, TF)	100%	Yes (SF, DRDF, WDF, IRF, RDF)	100%

The undetectable fault can also be solved by changing the DB operation in the test algorithm. Comparison between test approaches using various type of DBs in term of their fault detection improvement on conventional fault and SSCFs is tabulated in Table 1.2. Wu et al. (1999) developed the Random Access Memory Simulator for Error Screening (RAMSES) program to provide multi DB, consisting of eight DBs: P1 (0000), P2 (0101), P3 (0011), P4 (0110), P5 (0001), P6 (0010), P7 (0100), and P8 (1000). Wu et al. (1999) proved that by extending March C- and MATS++ with those DBs, the fault coverage is improved. Their designing of a data background generator to generate sequences of solid DBs (0s and 1s) proved to achieve up to 100% detection. However, the fault model covered in their works only conventional fault.

Irobi et al. (2010) proposed a new test algorithm, March m-MSS, which provided a solid-0 data background (00000000) , solid-1 data background (11111111), double-column stripes data background (00110011), double-column stripes data background (11001100), shifted double-column stripes data background (01100110) and shifted double-column stripes data background (10011001), which was able test all SSCF and SDCF faults under bit line coupling conditions. It was reported that using multiple DBs on March C-, March SR, and MATS+, the SSCFs are undetected with the condition of bit line coupling. Given these developments, it is necessary to develop

experiments to provide multiple DBs and to modify solid DBs to solve the undetectable issues.

1.3 Aim and Objective

The aim of the thesis is to improve the detection of SSCFs in existing MTAs to increase fault coverage. The main objectives of the proposed research can be summarized as follows:

To develop a test procedure consisting of sequence rules of DBs to detect the presently undetectable faults of SSCFs and SDCFs in the existing MTAs.

To provide a new method to modify DBs of the existing MTAs for obtaining better fault coverage and better hardware performance.

1.4 Scope of Research

The following items comprise the scope of this research:

The research involves generating multiple DBs and solid DBs after considering all possible DBs to test the conventional MTAs below 14N test length, such as MATS++ (9N), March C- (10N), March SR (14N), and Mod March CL (12N). Both methods are proposed to improve fault coverage of SSCFs. Figure 1.5 illustrates the flow of generating the new MTA based on the write operations numbers. DBs are filtered from all possible DBs following the test procedure rule. Those filtered DBs will be replaced by old DBs in the conventional MTA. Manual analysis to check the fault detection on each generated MTA will take place. The approach of this research is different compared to the approach based on the Address Fault Primitive and Test Pattern Graph used by Benso et al. (2005) and "Test Algorithm Generation by Simulation" used by Wu et al. (1999).

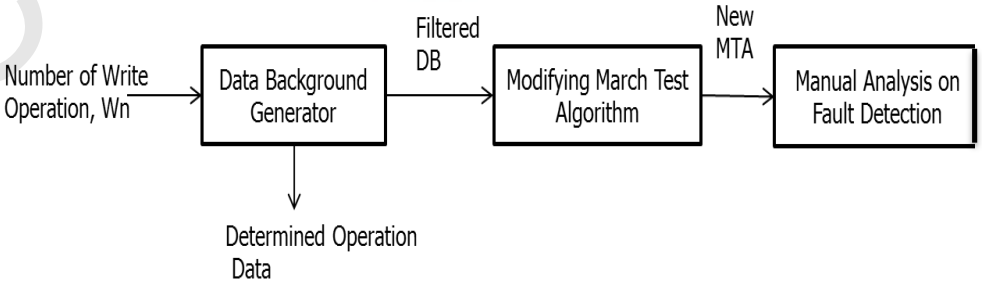

Figure 1.5 : The Overview of the Flow for Generating the New MTA

Method 1 manages the transition and non-transition at its bit-adjacent to memory word to generate managed DBs. There are two schemes included: a static scheme, whereby the data will write the same value twice, and a dynamic scheme whereby the new data will be written with the opposite values of the previous data.

The test evaluation of the specified MTA by Method 1 with static and dynamic scheme and MTA with solid DBs (0s and 1s) is conducted. The result of the generated MTAs will be compared in terms of its fault detection and Built-In-Self-Test (BIST) hardware performance with those with the conventional MTAs. The evaluation only picks one set of DBs per each Mod March SR (multiple DBs), March SR (solid DBs), and March SS (solid DBs) in the context of memory BIST. The testing scheme will be applied to single port and double port memories to evaluate the hardware performance in terms of hardware complexity, test cycle time, and test power.

Method 2 involves designing an automation program using Verilog HDL; it follows a proposition solution under the SQ generation rule to generate solid DBs. The flow in generating the possible DB follows the steps shown in Figure 1.5. Method 2 differs compared to the Method 1only in terms of the rule used. Referring to the generated test patterns, the SQ rule will determine the final sequence bit pattern. The final bit test pattern will be used to generate the new MTA but will retain the sequence of the operation in the original MTA.

Since the rule on the proposed test procedure involves transition and a non-transition data, the solution will also observe the detection of SDCFs, especially CFtrs, CFwds, CFrds, and CFdrds.

Finally, based on the fault coverage and the hardware test evaluation results, the best method to be practiced in industry and research will be proposed.

1.5 Project Contribution

The test proposal consists of two methods to improve fault coverage in SSCFs detection as well as achieving low area overhead, test power, and test time by limiting the test length to 14N test operations. The following list briefly summarizes the main contributions of this dissertation:

A new method of bit adjacent management in BOM tests by practicing dynamic and static DBs to improve fault coverage of SSCFs.

A new method to generate a new MTA by generating a new sequence of DBs that follows the SQ generation rule to improve the fault coverage of SSCFs.

Designing data background generator follows the SQ generation rule. The design architecture is able to generate the optimum data background automatically with transition and non-transition operations to generate new MTAs.

1.6 Thesis Layout

The thesis is organized as follows:

In Chapter 1, the motivations of SRAM testing research are described, introducing the fundamental work of the importance of March Test Algorithm and its issues concerning test performance, including the problem statement, objectives, project contribution, research methodology and scope of the project.

Chapter 2 presents a detailed literature review of the relevant research work. Some of the analysis will take place in the context of highlighting the motivation of this research project. This chapter also explains the test fundamentals of the SRAM testing involved in the research work. The fault taxonomy of SSCFs and SDCFs are explained in detail. A summarized overview of SRAM testing that involves generating the FFM, FPs, and MTAs will be presented. The overview of the basic test algorithm elements and fault detection of each fault is discussed in detail.

Chapter 3 shows the research and methodology used in this research. The implementation of Method 1 and the overview of the development of the test algorithm, the proposed test procedure, the produced new MTA, and the result of fault detection is also discussed in detail. The MBIST implementation and the result in terms of area, test time, and test power are discussed in this chapter. A comparison of utilization of multiple DB and solid DB approach also takes place.

Chapter 4 discusses in detail the implementation of Method 2 based on the proposed SQ generation rule. The flow chart of designing the Data Background Generator and the generated DB results are presented. The produced MTAs and their fault detections are tabulated. Discussion of the results for the fault coverage and test power based on the produced MTA is also included in this chapter.

Chapter 5 summarizes research work and findings, also discussing research limitation and highlighting potential future work.

REFERENCES

Adams, R. D. (2002). *High Performance Memory Testing: Design Principles, Fault Modeling, and Self test.* Boston, MA: Kluwer Academic Publishers.

Adams, R. D. (2006). Chapter 8: Embedded Memory Testing. In *Advances in Electronic Testing: Chalenges and Methodologies,* Dimitris Gizopoulos, 263–300.Netherland:Springer.

Adams, R. D., & Cooley, E. S. (1996). Analysis of a Deceptive Read Destructive Memory Fault Model and Recommended Testing. Proceedings from *IEEE North Atlantic Test Workshop*.

Agrawal, V. D., Kime, C. R., & Saluja, K. K. (1993). A tutorial on Built-in Self-test. I. Principles. *Design & Test of Computers, IEEE, 10*(1), 73–82.

Agrawal, V. D., Kime, C. R., & Saluja, K. K. (1993). A Tutorial on Built-in Self-test. 2. Applications. *Design & Test of Computers, IEEE, 10*(2), 69–77.

Akashe, S., Shastri, M., & Sharma, S. (2011). Multi Vt 7T SRAM Cell for High Speed Application at 45 nm Technology. Proceedings from *Nanoscience, Engineering and Technology (ICONSET), 2011 International Conference*, 351–354, 28–30 Nov.

Al-Ars, Z., & van de Goor, A. J. (2001). Static and Dynamic Behavior of Memory Cell Array Opens and Shorts in Embedded DRAMs. Proceedings from *Design Automation and Test in Europe*, 496–503.

Al-Harbi, S. M., Noor, F., & Al Turjman, F. M. (2007). March DSS: A New Diagnostic March Test for All Memory Simple Static Faults. *IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, 26*(9).

Bai Hong, F., & Nicolici, N. (2003). Power-Constrained Embedded Memory BIST Architecture. Proceedings from *Defect and Fault Tolerance in VLSI Systems, 18th IEEE International Symposium on*, 451–458, 3–5 Nov.Bardell, P. H., Jr., & McAnney, W. H. (1988). Built-in test for RAMs. *Design & Test of Computers, IEEE, 5*(4), 29–36.

Berthelot, D., Flottes, M. L., & Rouzeyre, B. (2000). A Method for Trading Off Test Time, Area and Fault coverage in Datapath BIST Synthesis. Proceedings from *Test Workshop, 2000. IEEE European*, 133–139.

Bosio, A., Di Carlo, S., Di Natale, G., & Prinetto, P. (2007). March AB, a State-of-the-art March Test for Realistic Static Linked Fault and Dynamic Faults in SRAMs. *Computers & Digital Techniques, IET, 1*(3), 237–245.

Bosio, A., & Di Natale, G. (2008). March Test BDN: A New March Test for Dynamic Faults. Proceedings from *IEEE International Conference on Automation, Quality and Testing, Robotics, 1*, 85–89.

Cha, S., & Yoon, H. (2013). Single Error Correction Code for Simultaneous Testing of Data Bit and Check Bit Arrays for Word-oriented Memories. *Device and Materials Reliability, IEEE Transactions*, 99, 1.

Chaudhry, S., Chattopadhyay, S., & Krishna, T. S. (2007). Synthesis of Finite State Machines for Low Static and Dynamic Power. *International Symposium on Integrated Circuits, 26–28 Sept. 2007*, 437, 440.

Chi-Feng, W., Chih-Tsun, H., & Cheng-Wen, W. (1999). RAMSES: A Fast Memory Fault Simulator. Proceedings from *Defect and Fault Tolerance in VLSI Systems, 1999*,165–173.

Dekker, R., Beenker, F., & Loek, T. (1988). Fault Modeling and Test Algorithm Development for Static Random Access Memories. Proceedings from *International Test Conference 1988*, 343–352.

Dekker, R., Beenker, F., & Thijssen, L. (1988). Fault Modeling and Test Algorithm Development for Static Random Access Memories. Proceedings from *New Frontiers in Testing, International Test Conference*, 343–352, 12–14 Sep.

Di Carlo, S., Prinetto, P., Scionti, A., Figueras, J., Manich, S., & Rodriguez-Montanes, R. (2009). A Low-cost FPGA-based Test and Diagnosis Architecture for SRAMs," *Advances in System Testing and Validation Lifecycle, 2009*, 141,146.

Executive Summary, *International Technology Roadmap for Semiconductors 2011 Edition*, Semiconductor Industry Association, 2011. Retrieved from http://www.itrs.net/Links/2011ITRS/2011Chapters/2011ExecSum.pdf

Fonseca, R. A., Dilillo, L., Bosio, A., Girard, P., Pravossoudovitch, S., Virazel, A., & Badereddine, N. (2010). Impact of Resistive-bridging Defects in SRAM Core-cell.

Fritzemeier, R. R., Hawkins, C. F., & Soden, J. M. (1991). CMOS IC Fault Models, Physical Defect Coverage, and I_{DDQ} Testing. Proceedings from *Custom Integrated Circuits Conference, IEEE 1991*, 13.1/1–13.1/8, 12–15 May.

Gorsche, S. S. (1992). An Efficient Memory Fault-test Technique for ASIC-based Memories. Proceedings from *Communications, 1992. ICC '92, Conference Record, SUPERCOMM/ICC '92, Discovering a New World of Communications, IEEE International Conference on, 1*, 136–141, 14–18 Jun.

Hamdioui, S. (2004). *Testing Static Random Access memories: Defects, Fault Models, and Test Patterns.* Boston, MA: Kluwer Academic Publishers.

Hamdioui, S., Gaydadjiev, G., & Van de Goor, A. J. (2004). The State-of-art and Future Trends in Testing Embedded Memories. Proceedings from *Memory Technology, Design and Testing, Records of the 2004 International Workshop*, 54–59, 9–10 Aug.

Hamdioui, S., & Reyes, J. E. Q. D. (2005). New Data-Background Sequences and Their Industrial Evaluation for Word-Oriented Random-Access Memories. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, 24*(6), 892–904.

Hamdioui, S., & Van de Goor, A. J. (2000). An Experimental Analysis of Spot Defects in SRAMs: Realistic Fault Models and Tests. Proceedings from *the Ninth Asian Test Symposium, (ATS 2000)*, 131–138.

Hamdioui, S., Van de Goor, A. J., & Rodgers, M. (2002). March SS: A Test for All Static Simple RAM Faults. Proceedings from *IEEE International Workshop on Memory Technology, Design, and Testing*, 95–100.

Hamzaoglu, I., & Patel, J. H. (2000). Reducing Test Application Time for Built-In-Self-Test Test Pattern Generators. Proceedings from *VLSI Test Symposium, 2000. 18th IEEE,* 369–375.

Harutyunyan, G., Shoukourian, S., Vardanian, V., & Zorian, Y. (2012). A New Method for March Test Algorithm Generation and Its Application for Fault Detection in RAMs. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, 31*(6), 941–949, June.

Harutyunyan, G., Vardanian, V. A., & Zorian, Y. (2005). Minimal March Tests for Unlinked Static Faults in Random Access Memories. Proceedings from *23rd IEEE VLSI Test Symposium*, 53–59.

Harutyunyan, G., Vardanian, V., & Zorian, Y. (2007). Minimal March Tests for Detection of Dynamic Faults in Random Access Memories. *Journal of Electronic Testing: Theory and Applications, 23*(2), 55–74.

Hasan, W. Z. W., Halin, I., Shafie, S., & Othman, M. (2011). An Efficient Diagnosis March-Based Algorithm for Coupling Faults in SRAM. Proceedings from *Micro and Nanoelectronics (RSM), 2011 IEEE Regional Symposium on*, 198–201, 28–30 Sept.

Huang, Y-J., & Li, J-F. (2012). Low-cost Self-test Techniques for Small RAMs in SOCs Using Enhanced IEEE 1500 Test Wrappers. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, 20*(11), 2123–2127.

Huzum, C., & Cascaval, P. (2001). A Multibackground March Test for All Static Simple Neighborhood Pattern-sensitive Faults in RAMs,"*15th International Conference on System Theory, Control, and Computing (ICSTCC), 2011*, pp.1,6, 14–16.

Irobi, S., Al-Ars, Z., & Hamdioui, S. (2010). Detecting Memory Faults in the Presence of Bit Line Coupling in SRAM Devices. Proceedings from *Test Conference (ITC), 2010 IEEE International*, 1–10, 2–4 Nov.

Jain, S. K., & Stroud, C. E. (1986). Built-in Self Testing of Embedded Memories. *Design & Test of Computers, IEEE, 3*(5), 27–37.

Kaushik, S. & Zorian, Y. Embedded Memory Test and Repair Optimizes SoC Yields, Electonic Design News, July 17 2012. Retrieved from http://www.tmworld.com/design/manufacturing/4390489/Embedded-memory-test-and-repair-optimizes-SoC-yields

Kavousianos, Xrysovalantis; Chakrabarty, Krishnendu, "Testing for SoCs with Advanced Static and Dynamic Power-management Capabilities," *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2013* , pp.737,742, 18-22.

Li, C. (2008). *Testing of Deep-submicron Embedded Memories in FPGAs*. (Master's thesis). Delft University of Technology, Delft.

Li, J.-F., & Wu, C.-W. (2001). Memory Fault Diagnosis by Syndrome Compression. Proceedings from *Design, Automation, and Test in Europe (DATE),* 97–101, 13–16 March.

Lobetti Bodoni, M., Benso, A., Chiusano, S., Di Carlo, S., Di Natale, G., & Prinetto, P. (2000). An Effective Distributed BIST Architecture for RAMs. Proceedings from *the Test Workshop, 2000. IEEE European*, 119–124.

Manikandan, P., Larsen, B. B., Aas, E. J., & Areef, M. (2011). A Programmable BIST with Macro and Micro Codes for Embedded SRAMs. Proceedings from *Design & Test Symposium (EWDTS), 2011 9th East-West*, 144–150, 9–12 Sept.

Marinescu, M. (1982). Simple and Efficient Algorithms for Functional RAM Testing. Proceedings from *International Test Conference, ITC 1982,* 236–239.

Masnita, M. I., Zuha, W. H. W., Sidek, R. M., & Izhal, A. H. (2009). March-based SRAM Diagnostic Algorithm for Distinguishing Stuck-at and Transition faults. *Journal of IEICE Electronic Express (ELEX), 6*(15), 1091–1097.

Matas, B., & de Subercasaux, C. (1997). *Complete Coverage of DRAM, SRAM, EPROM, and Flash Memory ICs.* Scottsdale, AZ: Integrated Circuit Engineering Corp.

Mentor Graphics. (2012). *MBISTArchitect Process Guide* (Ver. 201.3). Wilsonville, OR: Mentor Graphics Corporation.

Mentor Graphics. (2010). *Tessent™ MemoryBIST Usage Guide and Reference.* Wilsonville, OR : Mentor Graphics Corporation.

Miyazaki, M., Yoneda, T., & Fujiwara, H. (2006). A Memory Grouping Method for Sharing Memory BIST Logic. Proceedings from *Design Automation, Asia and South Pacific Conference*, 6, 24–27 Jan.

Mo, C. T., Lee, C. L., & Wu, W. C. (1994). A Self-diagnostic BIST Memory Design Scheme. Proceedings from *IEEE International Workshop on Memory Technology, Design and Testing*, 7 – 9.

Moore, G. E. (1998). Cramming More Components onto Integrated Circuits. *Proceedings of the IEEE*, 86(1), 82–85.

Nag, P. K., Gattiker, A., Sichao, W., Blanton, R. D., & Maly, W. (2002). Modeling the Economics of Testing: A DFT Perspective. *Design & Test of Computers, IEEE*, *19*(1), 29–41, Jan/Feb.

Nair, R., Thatte, S. M., & Abraham, J. A. (1978). Efficient Algorithms for Testing Semiconductor Random Access Memories. *Computers, IEEE Transactions on*, *C-27*(6), 572–576.

Nicolici, N., & Al-Hashimi, B. M. (2001). Tackling Test Trade-offs for BIST RTL Data Paths: BIST Area Overhead, Test Application Time and Power Dissipation. Proceedings from *Test Conference, 2001. International*, 72–81.

Niggemeyer, D., & Rudnick, E. M. (2004). Automatic Generation of Diagnostic Memory Tests Based on Fault Decomposition and Output Tracing. *Computers, IEEE Transactions*, *53*(9), 1134–1146.

Park, K., Lee, J., & Kang, S. (2010). An Area Efficient Programmable Built-in Self-test for Embedded Memories using an Extended Address Counter. Proceedings from *SoC Design Conference (ISOCC), 2010 International*, 59–62, 22–23 Nov.

Proceedings from the *Fifth IEEE International Symposium on Electronic Design, Test & Applications (DELTA '10),* 265–269.

Process Integration, Devices and Structure Chapter, International Technology Roadmap for Semiconductors 2011 Edition, Semiconductor Industry Association, 2011. Retrieved from http://www.itrs.net/Links/2011ITRS/2011Chapters/2011Test.pdf

Sanguhn Cha; Hongil Yoon, "Single-Error-Correction Code for Simultaneous Testing of Data Bit and Check Bit Arrays for Word-Oriented Memories," IEEE Transactions on *Device and Materials Reliability*, vol.13, no.1, pp.266,271, March 2013.

Shiyanovskii, Y., Wolff, F., & Papachristou, C. (2009). SRAM Cell Design using Tri-state Devices for SEU Protection. Proceedings from *On-Line Testing Symposium, 2009. IOLTS 2009. 15th IEEE International*, 114–119, 24–26 June.

Schrader, M., & McConnell, R. (2005). *DFT, DFM Tests Assure Quality SoC Design, Online EE Times Asia.* Retrieved from http://www.eetasia.com/ARTICLES/2005AUG/B/2005AUG16_DT_TA.pdf

Suk, D. S., & Reddy, S. M. (1981). A March Test for Functional Faults in Semiconductor Random Access Memories. *Computers, IEEE Transactions on, C-30*(12), 982–985.

Swapnil, B., & Vishal, S. (2008). Self-programmable Shared BIST for Testing Multiple Memories. Proceedings from *13th European Test Symposium (ETS)*, 91–96.

Tehranipour, M. H., Navabi, Z., & Fakhraie, S. M. (2000). An Efficient BIST Method for Testing of Embedded SRAMs. *Circuits and Systems, ISCAS 2001, the 2001 IEEE International Symposium, 5*, 73–76.

Treurer, P. R., & Agarwal, V. K. (1993). Fault Location Algorithms for Repairable Embedded RAMs. Proceedings from *IEEE Int. Test Conference 1993*, 825–834.

Van de Goor, A. J. (1991). *Testing Semiconductor Memories: Theory and Practice.* Chichester, England: John Wiley & Sons.

Van de Goor, A. J., & Al-Ars, Z. (2000). Functional Memory Faults: A Formal Notation and A Taxonomy. Proceedings from *18th IEEE VLSI Test Symposium*, 281–289, 6 August.

Van de Goor, A. J., Hamdioui, S., & Wadsworth, R. (2004). Detecting Faults in The Peripheral Circuits and An Evaluation of SRAM Tests. Proceedings from *International Test Conference 2004*, 114–123, 26–28 Oct.

Van de Goor, A. J., Offerman, A., & Schanstra, I. (1996). Towards a Uniform Notation for Memory Tests. Proceedings from *European Design and Test Conference*, 420–427, 11–14 Mar.

Van de Goor, A. J., & Smit, B. (1994). Generating March Tests Automatically. Proceedings from *Test Conference*, 870–878, 2–6 Oct.

Van de Goor, A. J., & Tlili, I. B. S. (1998). March Tests for Word-Oriented Memories. Proceedings from *Design, Automation, and Test in Europe,* 501–508, 23–26 Feb.

Van de Goor, A. J., & Tlili, I. B. S. (2003). A Systematic Method for Modifying March Tests for Bit-Oriented Memories into Tests for Word-Oriented Memories. *Computers, IEEE Transactions on, 52*(10), 1320–1331.

Van de Goor, A. J., Tlili, I. B. S., & Hamdioui, S. (1998). Converting March Tests for Bit-Oriented Memories into Tests for Word-Oriented Memories. Proceedings from *Memory Technology, Design, and Testing, International Workshop on*, 46–52, 24–25 Aug.

Van de Goor, A. J., & Verruijt C. A. (1990). An Overview of Deterministic Functional RAM Chip Testing. *ACM Computing Surveys (CSUR)*, *22*(1), 5–33.

Vardanian, J. V. A., & Zorian, Y. (2002). A March-Based Fault Location Algorithm for Static Random Access Memories. Proceedings from the *Eighth IEEE International On-Line Testing Workshop,* 256–261, 7 Nov.

Voyiatzis, I., Efstathiou, C., Tsiatouhas, Y., & Sgouropoulou, C. (2012). A Novel Architecture to Reduce Test Time in March-Based SRAM Tests. Proceedings from *Design & Technology of Integrated Systems in Nanoscale Era (DTIS), 2012 7th International Conference on*, 1–6, 16–18 May.

Wang, W.-L., & Lee, K.-J. (2002). A Programmable Data Background Generator for March Based Memory Testing. Proceedings from *IEEE Asia-Pacific Conference on Digital 2002, APASIC 2002*, 347–350.

Wang, L.-T., Wu, C.-W., & Wen, X. (Eds.) (2006). *VLSI Test Principles and Architectures: Design for Testability.* San Francisco: Elsevier.

Wan Hasan, W. Z., Othman, M., & Suparjo, B. S. (2006). A Realistic March-12N Test and Diagnosis Algorithm for SRAM Memories. Proceedings from *Semiconductor Electronics, 2006. ICSE '06. IEEE International Conference,* 919–923, Oct. 29–Dec. 1.

Wu, C.-F. et al. (2002). Fault Simulation and Test Algorithm Generation for Random Access Memories. *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, 21*(4), 480–490.

Wu, C-W. (2005). SOC Testing Methodology and Practice. Proceedings from *Design, Automation and Test in Europe, 2*, 1120–1121, 7–11.

Wu, R., Gerner, J., Weelus, R., & Lew, K. (1997). Testing Logic-Intensive Memory ICs on Memory Testers. *Design & Test of Computers, IEEE, 14*(1), 50–54.

Wu, Y., & Ivanov, A. (2006). Low Power SoC memory BIST. Proceedings from *Defect and Fault Tolerance in VLSI Systems, DFT '06. 21st IEEE International Symposium on*, 197–205, Oct.

Yong-Jyun Hu, Yu-Jen Huang, & Jin-Fu Li, Modeling and Testing Comparison Faults of TCAMs with Asymmetric Cells, *Proceeding of 27th VLSI Test Symposium, 2009*, pp.15,20, 3–7.

Yu-Jen Huang, & Jin-Fu Li; , "Low-Cost Self-Test Techniques for Small RAMs in SOCs Using Enhanced IEEE 1500 Test Wrappers," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, 20*,(11), 2123–2127.

Zarrineh, K., Upadhyaya, S. J., & Chakravarty, S. (2001). Automatic Generation and Compaction of March Tests for Memory Arrays. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, *9*(6), 845–857.

Zaourar, L., Kieffer, Y., & Wenzel, A. (2011). A Complete Methodology for Determining Memory BIST Optimization Under Wrappers Sharing Constraints. Proceedings from *Quality Electronic Design (ASQED), 3rd Asia Symposium*, 46–53.

Zordan, L. B., Bosio, A., Dilillo, L., Girard, P., Pravossoudovitch, S., Virazel, A., & Badereddine, N. (2011). Optimized March Test Flow for Detecting Memory Faults in SRAM Devices Under Bit Line Coupling. Proceedings from *Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2011 IEEE 14th International Symposium*, 353–358, 13–15 April.

BIODATA OF STUDENT

The student was born in northern Malaysian city of Perak, on March 20,1978. She received her degree in Electrical & Electronics Engineering from Universiti Kebangsaan Malaysia in 2001.

She then attended the Master of Science with Thesis Program in the Department of Electrical and Electronic Engineering at Universiti Putra Malaysia.

At the same time, she works as a senior engineer in the Microelectronic Department actively doing Design for Testability projects and Front End design projects at MIMOS Berhad.

Here her research focused on VLSI and memory testing and automation design development.

She has been published seven paper publications including 1 journal and 6 conference publications. She also been awarded of one patent with others pending.

LIST OF PUBLICATIONS

This research work presented in this thesis has yielded the following publications:

Zakaria, Nor Azura, W. Z. W. Hasan, I. A. Halin, R. M. Sidek, and Xiaoqing Wen. "*Testing Static Single Cell Faults using Static and Dynamic Data Background*." In Research and Development (SCOReD), 2011 IEEE Student Conferencen, pp. 1-6. IEEE, 2011

Zakaria, Nor Azura, W. Z. W. Hasan, I. A. Halin, R. M. Sidek, and Xiaoqing Wen. "*Fault Detection with Optimum March Test Algorithm*" Intelligent Systems, Modelling and Simulation (ISMS), 2012 Third International Conference, pp. 700-704. IEEE, 2012.

Zakaria, Nor Azura, W. Z. W. Hasan, I. A. Halin, R. M. Sidek, and Xiaoqing Wen. "Fault Detection with Optimum March Test Algorithm." Journal of Theoretical and Applied Information Technology, pp 018 – 027, Vol. 47. No. 1 2013

UNIVERSITI PUTRA MALAYSIA

STATUS CONFIRMATION FOR THESIS / PROJECT REPORT AND COPYRIGHT

ACADEMIC SESSION : First Semester 2013/2014

TITLE OF THESIS / PROJECT REPORT :

MULTIPLE AND SOLID DATA BACKGROUND SCHEME FOR TESTING STATIC SINGLE CELL FAULTS ON SRAM MEMORIES

NAME OF STUDENT: NOR AZURA BINTI ZAKARIA

I acknowledge that the copyright and other intellectual property in the thesis/project report belonged to Universiti Putra Malaysia and I agree to allow this thesis/project report to be placed at the library under the following terms:

1. This thesis/project report is the property of Universiti Putra Malaysia.
2. The library of Universiti Putra Malaysia has the right to make copies for educational purposes only.
3. The library of Universiti Putra Malaysia is allowed to make copies of this thesis for academic exchange.

I declare that this thesis is classified as :

*Please tick (√)

☐	**CONFIDENTIAL**	(Contain confidential information under Official Secret Act 1972).
☐	**RESTRICTED**	(Contains restricted information as specified by the organization/institution where research was done).
☐	**OPEN ACCESS**	I agree that my thesis/project report to be published as hard copy or online open access.

This thesis is submitted for :

☐ **PATENT** Embargo from _____ (date) until _____ (date)

Approved by:

_____ (Signature of Student)
New IC No/ Passport No.:

Date :

_____ (Signature of Chairman of Supervisory Committee)
Name:

Date :

[Note : If the thesis is CONFIDENTIAL or RESTRICTED, please attach with the letter from the organization/institution with period and reasons for confidentially or restricted.]