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3D Simulation Investigating ZnO NWFET Characteristics

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Abstract: 3D Simulation was carried out and compared with fabricated ZnO NWFET. The device had the following electrical output characteristics: mobility value of 10.0 cm^2/Vs at a drain voltage of 1.0 V, threshold voltage of 24 V, and subthreshold slope (SS) of 1500 mV/decade. The simulation showed that the device output results are influenced by two main issues: (i) contact resistance ($R_{con} \approx 11.3$ MΩ) and (ii) interface state trapped charge number density ($Q_{IT} = 3.79 \times 10^{15}$ cm^{-2}). The Q_{IT} was derived from the Gaussian distribution that depends on two parameters added together. These parameters are: an acceptor-like exponential band tail function $g_{GA}(E)$ and an acceptor-like Gaussian deep state function $g_{TA}(E)$. By de-embedding the contact resistance, the simulation is able to improve the device by producing excellent field effect mobility of 126.9 cm^2/Vs.

Introduction

Modelling and simulation of semiconductor devices provides an important method of analysis; easily verified, communicated and understood [1-5]. Before any fabrication can be carried out, there is a need to simulate so as to improve understanding, save costs and time. More importantly, it can also predict unknown future behaviours of devices and determine ways of reaching such lofty ideals. Over the years, researchers have developed the software into 2D and 3D. 2D is faster and works best for micro-meter devices, whereas, 3D is slower but it is a requirement for nano-meter devices.

3D simulation is used to characterise earlier work at the University of Southampton by S. M. Sultan, et al., [1] on ZnO NWFET and finds ways of improving it. The device had a p-typed boron doped silicon substrate, an oxide thickness of 100 nm and nanowire dimensions of length 10 μm, width 40 nm, and thickness 36 nm. The electrical characteristics included a field effect mobility of 10.0 cm^2/Vs at a drain voltage of 1V, a threshold voltage of 24 V, a subthreshold slope (SS) of 1500 mV/decade and an on/off ratio current ratio of 10^6. By analysing the characteristics of the device, it is clear the device has room for improvement. The field effect mobility is low compared with ZnO TFTs that have mobility around 110 cm^2/Vs [2] , while state of the art top-down ZnO nanowire transistors have reported mobility of 80 cm^2/Vs [3]. The threshold voltage is high and needs to be reduced to a value close to 0.5 V. A value close to 0.5 V is desired so as to reduce power consumption. The subthreshold slope is also poor and need to be improved.

Little work on 2D simulation has been reported on ZnO TFTs [4–8] and even less has been reported on 3D simulation of ZnO NWFETs. The work reported is therefore expected to provide new insights into the performance of ZnO NWFETs.

Simulation Procedure

Two Silvaco products were used: Devedit [9] and Atlas [10]. Fig. 1 shows the 3D device structure that was developed using Devedit, whereas electrical characteristics and bias conditions were simulated through Atlas. The structure is assumed to have a single crystal ZnO channel with parameters as stated in Table 1. The research investigation uses Devedit over Athena software because Devedit has a more advanced mesh definition which allows for greater accurate and precise output results. Devedit also allows for direct 3D interfacing with Atlas whereas it is impossible with the Athena software. Atlas numerical methods used for calculating device output results are: newton and direct. Block cannot be used in 3D simulation and gummel is very slow to utilize. Therefore the numerical methods used throughout the simulation are newton and direct.

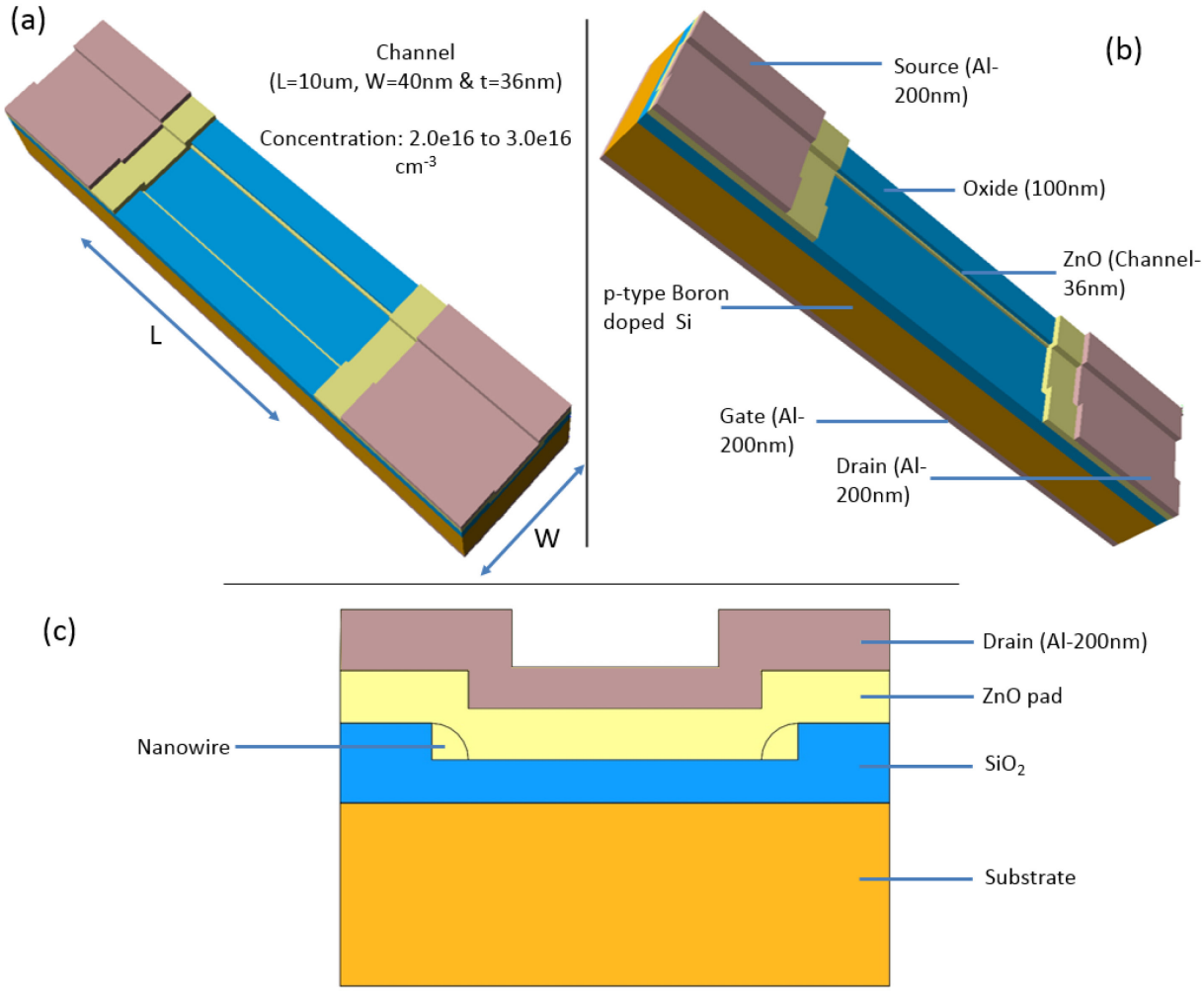

Fig. 1: 3D simulated device structure modelled through Devedit software and then derived from deckbuild using tonyplot. (a) Schematic diagram clearly showing two parallel nanowires. (b) Schematic diagram showing another point-of-view. (c) Cross-sectional diagram of the device. The simulated has an oxide thickness 100 nm and p-typed boron doped silicon substrate. It has source, drain and gate aluminium electrode. The device has a nanowire length of 10 µm, width 40 nm and thickness 36 nm.

Under ATLAS, the physical model used is the Boltzmann model which is sufficient in this case because the other models are for specific situations such as heavily doped regions, low temperatures that tend to freeze the carriers, and for bipolar transistors. No mobility model was used therefore, Atlas used the default values which are entirely isotropic in nature and there is no directional component. ZnO is a new material and ATLAS software does not cater for ZnO mobility models. For recombination models, the Shockley-Read-hall (SRH) model was utilized as it is the most general model for simulating new materials [10]. Impact ionization models include: Silberrherr's

model, Grant's model, Crowell-Sze model, Toyabe model, and Concannon model. All these models are used for breakdown voltage. The breakdown voltage will not be simulated hence these models are not required [10].

Table 1: Parameters used for ZnO NW Simulation; All simulation parameters were defined to be the same as the experimental device.

No.	Physical Parameter	S. M. Sultan, et al., [1] Experiment	Simulation Work Done	Units
1	N_d = carrier concentration	$2.0x10^{16}$ to $3.0x10^{16}$	$2.17x10^{16}$	cm^{-3}
2	Si Substrate Doping	$1.32x10^{15}$	$1.32x10^{15}$	cm^{-3}
3	L = Length of channel	$1.0x10^{-3}$	$1.0x10^{-3}$	cm
4	T_{ZnO} = Thickness of channel	$3.6x10^{-6}$	$3.6x10^{-6}$	cm
5	W = Z = Width of channel	$4.0x10^{-6}$	$4.0x10^{-6}$	cm
6	SiO_2 Insulator thickness (d)	$1.0x10^{-5}$	$1.0x10^{-5}$	cm
7	Si Substrate thickness	$7.0x10^{-5}$	$7.0x10^{-5}$	cm

3D simulation is slower and more complex than 2D simulation [11–18]. Its main advantage over 2D simulation is that it allows for a more precise and accurate estimation of the experimental device. The curved shapes that are inherent within device fabrication were not simulated but rectangular shapes were assumed instead for simplicity. This infers that the edges are not accurately characterized. Also surface roughness was not simulated. Surface roughness can be simulated by introducing zig-zag shapes on the surface of the channel. The problem is that experimentally measured roughness is between 1.5 nm to 6.0 nm which is too small for efficient convergence.

Table 2: Parameters used for interface state charge Q_{IT} definition in the 3D-simulation; the values were collected from a number of sources [1-16].

No.	Physical Parameter	Atlas Simulation (Default Values for poly-Si)	Literature [3–18]	Simulation Work Done	Units
1	Band gap, Eg(300K) (Ec-Ev)	1.12	3.4	3.4	eV
2	Effective mass of an electron in the conduction band, me*	0.318	0.318	0.318	m_0
3	Electron affinity, ζ(Evac-Ec)	-	4.29	4.29	eV
4	Work Function, Φs(Evac-Ef)	4.17	4.45	4.45	eV
5	Donor level, Ec-Ed	44	30	30	meV
6	Energy level of peak trap state density in Grain Boundary, E_{GA}=E1	0.62	1.7	1.7	eV
7	Characteristic decay energy of Gaussian distribution, W_{GA}=E2	0.033	0.25	0.20	eV
8	The density of acceptor-like states in the tail distribution at the conduction band edge, N_{TA}	$1.0x10^{21}$	$4.0x10^{17}$ to $1.2x10^{21}$	$3.79x10^{20}$	cm^{-3}
9	The density of donor-like states in the tail distribution at the valence band edge, N_{TD}	$1.0x10^{21}$	$4.0x10^{17}$ to $1.2x10^{21}$	$3.79x10^{20}$	cm^{-3}
10	The total density of acceptor-like states in a Gaussian distribution, N_{GA}	1.5×10^{15}	$3.0x10^{16}$ to $7.3x10^{19}$	4.81×10^{18}	cm^{-3}
11	The total density of donor-like states in a Gaussian distribution, N_{GD}	$1.5 x10^{15}$	$3.0x10^{16}$ to $7.3x10^{19}$	4.81×10^{18}	cm^{-3}
12	The conduction band density of states, Nc300	$2.8x10^{19}$	$2.24x10^{18}$	$5.31x10^{18}$	cm^{-3}

Defects are very important in modelling the performance of ZnO nanowire FETs. Two types of charge defects were investigated which are surface charge and interface state trapped charge (Q_{IT}). Surface charge was simulated by including it in the oxide fixed charge parameter (Q_f). Interface state trapped charge was modelled using Equation 1 and shows that the density of defect states (DoS = g(E) which defines the trapped charge) depends on two functions: an acceptor-like exponential band tail function $g_{GA}(E)$ and an acceptor-like Gaussian deep state function $g_{TA}(E)$ [11, 13, 14] N-type ZnO semiconductor contains defect states mainly due to acceptor-like trapped charge. Equations 2 & 3 describe the $g_{GA}(E)$ and $g_{TA}(E)$ functions, where:

a. N_{GA} is the density at peak energy,
b. E_{GA} is the peak energy,
c. W_{GA} is the Gaussian decay energy for the Gaussian distribution $g_{GA}(E)$
d. N_{TA} is the conduction band edge intercept density,
e. W_{TA} is the Gaussian decay energy for the Gaussian distribution $g_{TA}(E)$

$$g(E) = g_{GA}(E) + g_{TA}(E) \quad (1)$$

$$g_{GA}(E) = N_{GA} \exp[-\left(\frac{E_{GA} - E}{W_{GA}}\right)^2] \quad (2)$$

$$G_{TA}(E) = N_{TA} \exp(\frac{E - E_c}{W_{TA}}) \quad (3)$$

Interface state trapped charge (Q_{IT}) was therefore modelled by fitting the parameters within the above set of equations to the measured ZnO nanowire FET characteristics. Starting with parameters from literature on ZnO FETs [3–18], all parameters were varied as shown in Table 2 but still kept within the literature values.

After modelling a basic n-type ZnO nanowire field effect transistor, the simulation was then compared with experimental results [1]. The values are presented on Table 3. The top-down fabrication process utilized remote-plasma atomic layer deposition (RP-ALD) at 190 °C and anisotropic inductively coupled plasma (ICP) etching at an RF power of 100 W and pressure of 15 mtorr.

Table 3: Electrical performance achieved by S. M. Sultan, et al., [1]

No.	Physical Parameter	S. M. Sultan, **et al., [1]** Experiment	Units
1	Field effect mobility	10.0	cm^2/Vs
2	Fixed drain voltage	1.0	V
3	Threshold voltage	24.0	V
4	Subthreshold slope	1500	mV/decade
5	On/Off current ratio	10^6	

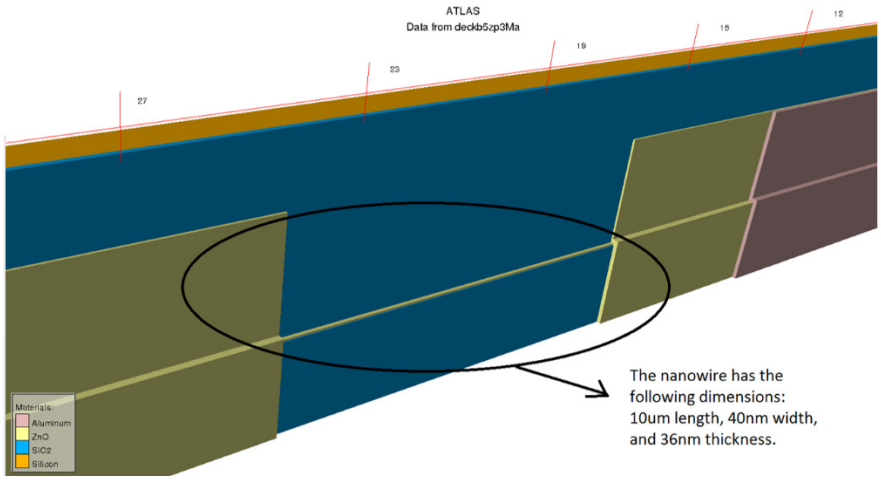

Fig. 2: 3D simulated device structure. Only one nanowire was simulated and then the current was multiplied by two (2) to get the true experimental representation.

Table 1 shows the physical parameters that were used to define the ZnO NWFET whereas Table 2 shows the parameters used to characterize the defects. All simulation parameters were obtained wherever possible from measurements on an experimental device reported in the literature [3–18]. The donor concentration for the nanowire was measured experimentally to be between 2.0 x 10^{16} and 3.0 x 10^{16} cm^{-3}. The silicon substrate doping is derived from a p-type resistivity between 1 and 30 Ω.cm. Fig. 1 shows a Devedit 3D structure with two ZnO nanowires that act as the active channel modelled through parameters stated in Table 2. It is composed of bottom and side oxide layers which are 10 µm and 100 nm respectively. It possesses source-drain pads that help reduce the contact resistance by providing a large surface area for the metal electrodes to connect with the nanowires. These metal electrodes are deposited on top of the pads. Two nanowires are very slow to simulate due to mesh constraints, therefore one nanowire is simulated as depicted in Fig. 2.

Results and Discussion

Fig. 3 shows the initial 3D simulated subthreshold $I_{DS}V_{GS}$ characteristic for a ZnO nanowire transistor using default parameters derived from literature [10–13]. These parameters are summarised in Table 2 where they are compared with the final ones used. At this point, no defects were introduced at the oxide/channel interface. Default parameters give a high current and a steep sub-threshold slope of 100 mV/decade whereas the experimental curve shows a low current and a poor slope of 1500 mV/decade.

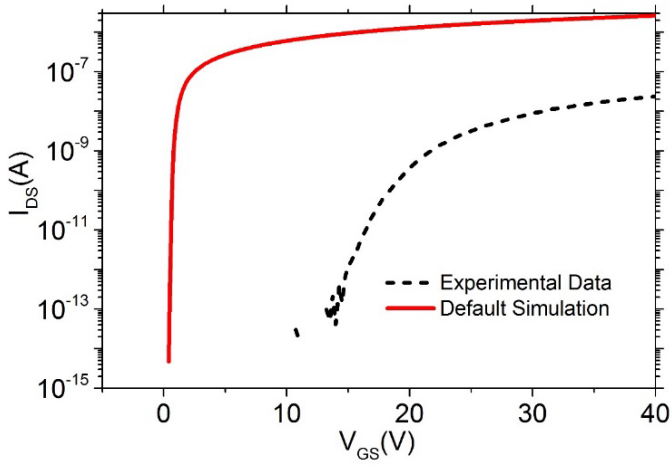

Fig. 3: 3D Simulation of the ZnO NWFET reported in [1]. This simulation used default parameters derived from literature (Table 2).

The difference in currents and the subthreshold slopes indicates that the experimental device is greatly affected by defects. Therefore, defects were introduced into the modelled device. As stated, two types of defect were introduced which are fixed charge (Q_f) and interface state charge (Q_{IT}). Fig. 4 shows simulated and experimental results after introducing defects with the parameters listed in Table 2. The fixed charge is kept at a low number value of 3.0 x 10^{10} cm^{-2} which means it has little effect on the simulation. When this value is increased or decreased, it shifts the threshold voltage, but does not change the shape of the sub-threshold plot. Fig. 4 shows the main Q_{IT} parameters that were altered to fit. Nc300 was altered from 2.24 x 10^{18} cm^{-3} to 5.31 x 10^{18} cm^{-3}. N_D is the donor concentration and is un-altered so as to keep it the same as the experimental value. N_{GA} was altered from 9.0 x 10^{16} cm^{-3} to 1.0 x 10^{19} cm^{-3} and N_{TA} was altered from 4.0 x 10^{19} cm^{-3} to 9.0 x 10^{20} cm^{-3}. The simulated device matches the measured device reasonably well at low currents.

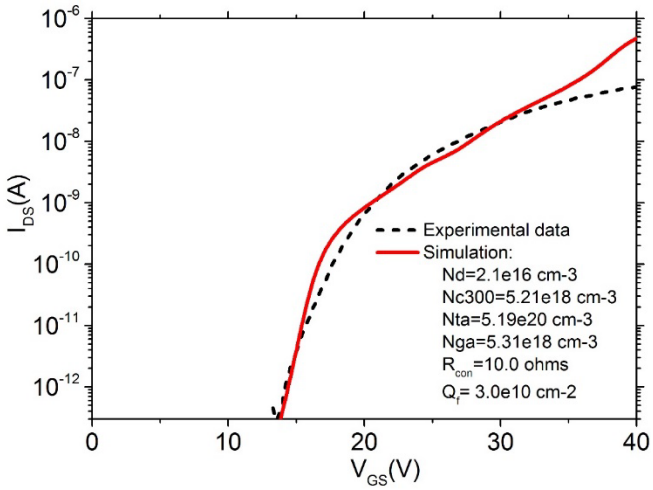

Fig. 4: 3D Simulation of the ZnO NWFET reported in [1]. Fixed charge and interface state charge were introduced into the simulation so as to fit the experimental results

After introducing defects, the 'fit' between simulation and measurements is still poor at high currents, with the simulation predicting much higher currents than the experimental device. The most likely explanation for this discrepancy is contact resistance. There is therefore a need to simulate the effect of contact resistance. The device is simulated with different values contact resistance, varying from 10 Ω to 1.13 x 10^7 Ω. The simulation used a low fixed oxide charge of 3.0 x 10^{10} cm^{-2} and high interface state trapped charge of 3.79 x 10^{20} cm^{-3} which is derived from the above equations. To use the equations, *'E'* is assumed to be 3.4 eV. Inserting parameters from Table 2, the value of Q_{IT} can then be derived. Fig. 5 shows a variation of contact resistance from R_{con1} = 10 Ω to R_{con5} = 8.0 x 10^{10} Ω. The current remains constant from a contact resistance value of 0 Ω to 1.0 x 10^6 Ω, after that it sharply decreases. As can be seen from Fig. 5, contact resistance has negative impact on the electrical characteristics of NWFET. It reduces the voltage across the channel and thereby limits the maximum on-current. This result indicates that the experimental devices should have values of contact resistance less than about 1.0 x 10^6 Ω.

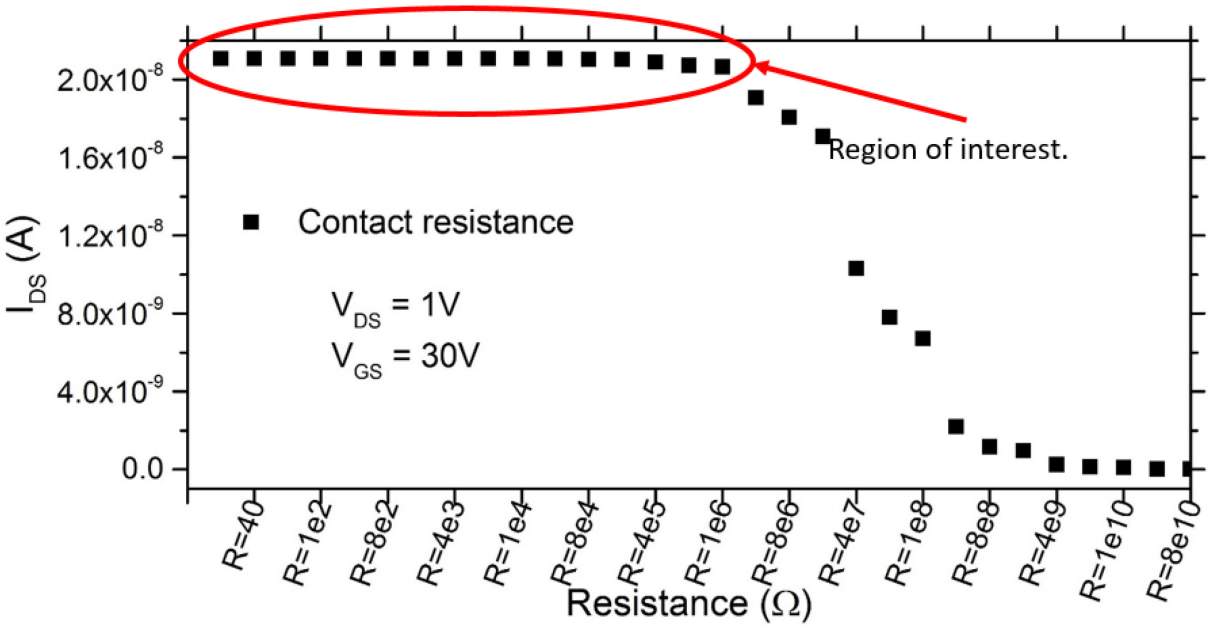

Fig. 5: 3D Simulation of the ZnO NWFET reported in [1], showing the effect of contact resistance (R_{con}) by varying it from 40 Ω to 8.0 x 10^{10} Ω. The value of I_{DS} was simulated at V_{GS} = 30 V and V_{DS} = 1.0 V

It must be noted that the simulation assumed that the fabricated device process produced single crystal ZnO, but that is not the case as the etching process of the nanowire damages the nanowire and also the deposition process of ZnO on top of an insulating material, that is not lattice matched to the ZnO. This effect was not investigated here. Devedit can model polycrystalline materials, but this requires information on grain size and recombination parameters at grain boundaries.

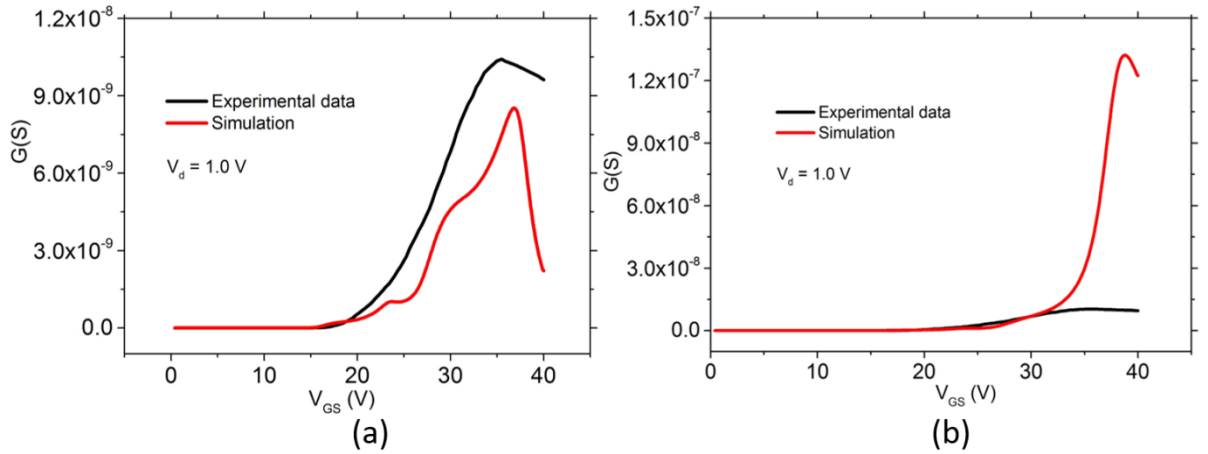

Fig. 7: 3D Simulation of the ZnO NWFET reported in [16]; (a) simulated and measured transconductance verses gate voltage (b) Simulated and measured transconductance Vs gate voltage for a device in which the series resistance has been de-embeded.

To complete the simulation work, transconductance graphs were derived and plotted. Fig. 6 (a) shows simulated and measured transconductance as a function of gate voltage. The simulation curve has peak transconductance of 8.52 x 10^{-9} S at 36.8 V whereas the experimental curve has peak transconductance of 2.27 x 10^{-8} S at 35.5 V. Using these peak values of transconductance, a field effect mobility (μ_{FE}) can be derived for both the simulated and experimental devices. The simulated device gives a μ_{FE} of 8.2 cm^2/Vs which is comparable to the experimental value of 10.0 cm^2/Vs.

The above values of mobility μ_{FE} include the effect of contact resistance and hence may underestimate the true mobility. However, the effect of contact resistance can be de-embedded by performing an identical simulation without any contact resistance. De-embedding in simulation is

whereby the contact resistance is lowered to an insignificant value such 10 Ω. To reduce contact resistance under fabrication process, the channel doping can be increased while keeping the fabrication process the same. This implies that the surface charge and roughness will remain relatively the same as before as it depends on the etching techniques. The ZnO channel doping can be increased from $2.17x10^{16}$ cm-3 to $1.0x10^{18}$ cm^{-3}. Fig. 6 (b) shows that by de-embedding the device, the peak transconductance value is increased from 8.52 x 10^{-9} S to 1.32 x 10^{-7} S. The field effect mobility derived from this new value of transconductance is found to be 126.9 cm^2/Vs, as summarized in Table 4. This is an excellent value that future work will aim for. This analysis indicates that the true mobility of the ZnO layer is much higher than that extracted from the measured transistor characteristics and is much closer to state-of-the-art values in ZnO devices. The de-embedded value is comparable to the state-of-the-art TFT by B. Bayraktaroglu, et al., [2]. Table 4 summarises the important characterisitics obtained through simulation.

Table 4: Simulation results derived from matched experimental curve.

Parameter	Experiment	Simulation	Units
Oxide fixed trapped Charge (default)	-	$3.0x10^{10}$	cm^{-2}
Aluminum Work Function	-	4.27	eV
Contact Resistance (R)	-	$1.13x10^{7}$	Ohm
Field Effect Mobility	10.0	8.2	cm^2/Vs
Field Effect Mobility (De-embedded device)	-	126.9	cm^2/Vs

Conclusion

3D Simulation was carried out and compared with a fabricated device. The experimental results had an oxide thickness of 100 nm and nanowire dimensions of length 10 µm, width 40 nm, and thickness of 36 nm. The device had the following electrical output characteristics: mobility value of 10.0 cm^2/Vs at a drain voltage of 1.0 V, threshold voltage of 24 V and subthreshold slope (SS) of 1500 mV/decade. Using simulation, it was discovered that the experimental output results are degraded due to two main defects: contact resistance ($R_{con} \approx 11.3$ MΩ) and interface state trapped charge number of Q_{IT} = 3.79 x 10^{15} cm^{-2}. De-embedding the contact resistance shows the device gives excellent field effect mobility of 126.9 cm^2/Vs. Surface charge and roughness were not simulated due to limitations of the simulation software, but are hypothesized to contribute toward poor output characteristics.

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References

[1] S. M. Sultan, N. J. Ditshego, R. Gunn, P. Ashburn, and H. M. Chong, "Effect of atomic layer deposition temperature on the performance of top-down ZnO nanowire transistors.," *Nanoscale Res. Lett.*, vol. 9, no. 1, p. 517, Jan. 2014.

[2] B. Bayraktaroglu, S. Member, K. Leedy, and R. Neidhard, "High-Frequency ZnO Thin-Film Transistors on Si Substrates," vol. 30, no. 9, pp. 946–948, 2009.

[3] C. Hsu and T. Tsai, "Fabrication of fully transparent indium-doped ZnO nanowire field-effect transistors on ITO/glass substrates," *J. Electrochem. Soc.*, vol. 158, no. 2, pp. K20–K23, Feb. 2011.

[4] Z. Yu-Ming, H. Yi-Gang, L. Ai-Xia, and W. Qing, "Simulation of grain boundary effect on characteristics of ZnO thin film transistor by considering the location and orientation of grain boundary," *Chinese Phys. B*, vol. 18, no. 9, pp. 3966–3969, Sep. 2009.

[5] F. Hossain, J. Nishii, and S. Takagi, "Modeling and simulation of polycrystalline ZnO thin-film transistors," *J. Appl.*, vol. 94, no. 12, pp. 7768–7777, Dec. 2003.

[6] F. Hossain, J. Nishii, and S. Takagi, "Modeling of grain boundary barrier modulation in ZnO invisible thin film transistors," *Phys. E Low*, vol. 21, no. 2–4, pp. 911–915, Mar. 2004.

[7] W.-K. Hong, G. Jo, S.-S. Kwon, S. Song, and T. Lee, "Electrical Properties of Surface-Tailored ZnO Nanowire Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3020–3029, Nov. 2008.

[8] J. Maeng, W. Park, M. Choe, G. Jo, Y. H. Kahng, and T. Lee, "Transient drain current characteristics of ZnO nanowire field effect transistors," *Appl. Phys. Lett.*, vol. 95, no. 12, p. 123101, 2009.

[9] SILVACO International, "devedit.manual - devedit_users.pdf," (Silvaco International) [Online] May 2010. Available: http://www.silvaco.co.uk/content/kbase/devedit.pdf. [Accessed: 28-May-2015].

[10] SILVACO International, "atlas_umv1.book - atlas_users.pdf," (Silvaco International) [Online] December 2006. Available: http://ridl.cfd.rit.edu/products/manuals/Silvaco/atlas_users.pdf. [Accessed: 28-May-2015].

[11] F. Torricelli and J. Meijboom, "Transport Physics and Device Modeling of Zinc Oxide Thin-Film Transistors Part I: Long-Channel Devices," *Electron Devices,* vol. 58, no. 8, pp. 2610–26192619, Aug. 2011.

[12] D. Redinger, "Lifetime modeling of ZnO thin-film transistors," *Electron Devices, IEEE Trans.*, vol. 57, no. 12, pp. 3460–3465, Dec. 2010.

[13] A. Ahnood, K. Ghaffarzadeh, A. Nathan, P. Servati, F. Li, M. R. Esmaeili-Rad, and A. Sazonov, "Non-ohmic contact resistance and field-effect mobility in nanocrystalline silicon thin film transistors," *Appl. Phys. Lett.*, vol. 93, no. 16, p. 163503, 2008.

[14] A. Zhang, X.-R. Zhao, L.-B. Duan, J.-M. Liu, and J.-L. Zhao, "Numerical study on the dependence of ZnO thin-film transistor characteristics on grain boundary position," *Chinese Phys. B*, vol. 20, no. 5, p. 057201, May 2011.

[15] Y. Zhou and Y. He, "Effect of grain boundary on electric performance of ZnO nanowire transistor with wrap-around gate," *J. Cent. South Univ. Technol.*, vol. 18, no. 4, pp. 1009–1012, Aug. 2011.

[16] S. M. Sultan, K. Sun, O. D. Clark, T. B. Masaud, Q. Fang, R. Gunn, J. Partridge, M. W. Allen, P. Ashburn, and H. M. H. Chong, " Electrical Characteristics of Top-Down ZnO Nanowire Transistors Using Remote Plasma ALD," IEEE Electron Device Letters, vol. 33, no. 2, pp. 203-205, Feb. 2012.

[17] N.A.B. Ghazali, M. Ebert, N.M.J. Ditshego, M.R.R. de Planque, H.M.H. Chong, "Top-down fabrication optimisation of ZnO nanowire-FET by sidewall smoothing," Microelectronic Engineering (MNE), vol. 159, pp. 121–126, Feb. 2016.

[18] N.M.J. Ditshego ⇑, K. Sun, I. Zeimpekis, P. Ashburn, M.R.R. de Planque, H.M.H. Chong, "Effects of surface passivation on top-down ZnO nanowire transistors," Microelectronic Engineering (MNE), vol. 145, pp. 91–95, March 2015