A FLEXIBLE REAL TIME NETWORK MODEL FOR EVALUATING HVDC SYSTEMS' IMPACT ON AC PROTECTION PERFORMANCE

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Abstract

This paper presents a reduced but reprehensive real time network model constructed in RSCAD for RTDS to evaluate the impact of HVDC systems and Non-Synchronous Generation (NSG) on the protection performance in the AC grid. The proposed network model could be flexibly configured to evaluate key factors that could affect the protection performance, including the level of system strength, different control strategies adopted in the HVDC system, different levels of synchronous compensation installed at the HVDC site, etc. The developed network model contains a Modular Multilevel Converter (MMC)-based HVDC system, a NSG unit representing the converter-interfaced generation and a Synchronous Condenser (SC) representing the level of synchronous compensation. A flexible controller is designed for the HVDC system to realise various typically used control strategies, including balanced current control, constant active power control and constant reactive power control, and inject a desired level of the negative sequence current as required. The NSG employs the widely-adopted PQ control strategy. Three typical controllers, comprising the Automatic Voltage Regulator (AVR), constant reactive power and droop controller, are implemented for the SC to realistically emulate the SC behaviour under different control modes. Case studies on the application of the model for testing distance protection performance are presented. The developed model is suitable for both pure simulation-based studies and also hardware-in-the-loop test when connected to an external physical relay, thus providing an ideal testing platform for identifying the potential critical protection issues and the potential solutions in future power networks with high penetration of renewables.

1 Introduction

HVDC systems play a critical role in facilitating the objective of the GB power system achieving the net-zero carbon operation by 2025 [1]. The ambitious plans for HVDC system development and growth, along with the rapidly increasing penetration of converter-interfaced NSG, have introduced significant challenges to the operation of transmission systems. One of the key challenges is the potential impact of the increasing capacity of the converters on the reliable operation of existing AC protection systems. Comparing with the conventional synchronous generators, converters contribute limited short-circuit current and this contribution may also vary depending on the nature of the controllers and the specific manufacturer's practices [1][2]. These uncertainties and variations relating to converters' behaviours during faults introduce significant concerns and risks of compromised AC protection performance. Therefore, there is a compelling need for a flexible network model that could be used for comprehensive evaluation of the protection performance in the AC grid with the integration of HVDC systems in a network with increasing penetration of NSGs.

In existing technical literature, there are a number of network models reported for testing the distance relay performance. In [3][4], the impact of the converter-interfaced units, including the HVDC system and NSG, on the distance relay performance is reviewed, but the models included in these papers do not allow the investigation of the influence of different HVDC control strategies and synchronous compensation. A relatively flexible network is implemented in [5], where the controller in [6] is used for the design of the HVDC system. It allows to simulate three typically used control strategies, including constant active power control [7], balanced current control [8] and constant reactive power control [9], and inject the varied levels of the negative sequence current during faults. Additionally, the impact of the synchronous compensation provided by SC can also be simulated by this network. However, in this work, a full transmission network was used. As a result, it is difficult to adopt the model for investigating HVDC systems in other transmission systems. Furthermore, the SC in that network only has one type of controller, it cannot operate in other control modes (e.g. the constant reactive power control mode and droop mode).

To address the aforementioned challenges associated with the lack of a suitable and flexible network model for testing impact of system strength and HVDC control strategies on protection performance, this paper presents a reduced but representative real time network model constructed in RSCAD for RTDS. The developed network model can be configured to represent the equivalent network condition for selected circuit to be investigated, so it is not constrained to a specific transmission

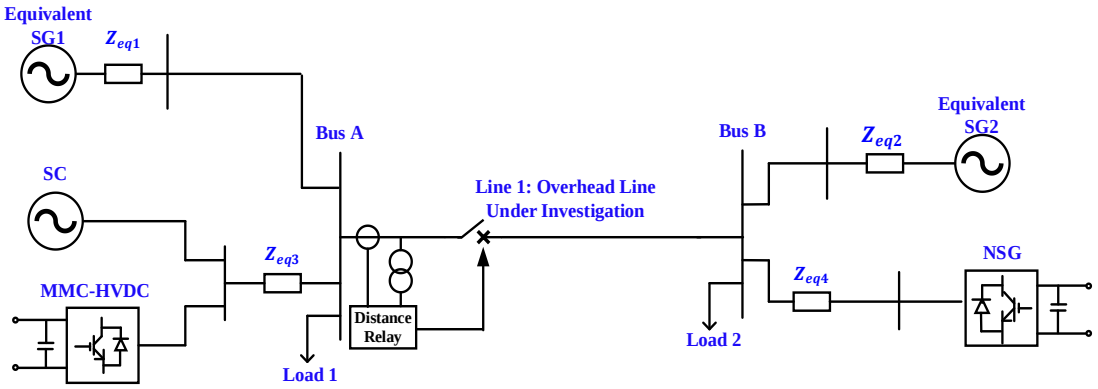

Fig. 1 Schematic of the developed RTDS network model.

system. The developed network model can also be flexibly configured to evaluate key factors that could affect protection performance, including the level of system strength, different control strategies adopted in the HVDC system, different levels of synchronous compensation installed at the HVDC site, and other influencing factors. The network model is constructed in RTDS and can be coupled with analogue amplifiers to form a Hardware-In-the-Loop (HIL) setup, offering an ideal tool for testing physical relays' performance.

The rest of the paper is organised as follows. Section 2 presents an overview of the developed network model and highlights its capabilities. Section 3 discusses the modelling of the individual key elements and the configuration of the network model. Section 4 presents case studies to illustrate the use of the model in evaluating the potential impact of the HVDC control modes and SC on distance protection. Finally, the conclusions are drawn in Section 5.

2 Overview of the network model

An overview of the network model structure is shown in Fig. 1. In this model, SG1 and SG2 represent the equivalent "lumped" synchronous generation sources at the bus A and B, connected to the protected line (i.e. Line 1) where the protection relay being investigated is installed; Load 1 and Load 2 represent the equivalent loads connected at the two busbars; the MMC-HVDC element represents the MMC-HVDC station where a flexible controller is implemented to emulate different control strategies; SC represents the synchronous condenser installed at the HVDC site, which could be switched on or off and its capacity can be adjusted to represent different level of synchronous compensation at the HVDC site; NSG represents the converter-interfaced non-synchronous generation at the remote end of the protected line, which represents general converter-interfaced generation connected at both distribution and transmission levels, e.g. wind, PV and other converter-based technologies; Z_{eq1} and Z_{eq2} represent the equivalent impedance of SG1 and SG2. By adjusting the values of Z_{eq1} and Z_{eq2} , along with the capacity of HVDC system and the NSG unit, the network model can represent different penetration levels of converter-based generation, and thus different levels of system strength at bus A and B. Z_{eq3} represents the impedance between the HVDC system and Bus A, which could be adopted from the actual system data. As NSG represents an aggregated converter-based generation in the system, Z_{eq4} does not directly link to a specific system parameter in the network, and it is typically manually adjustable to ensure the NSG control system is stable; and Line 1 is the protected line under investigation. In this model, the SG1 and SG2 are represented by ideal voltage sources. SC is the machine model provided by RSCAD [10]. The type of the HVDC unit is MMC-HVDC and the NSG is represented using a two-level power electronic converter.

3 Development and Configuration of the Network Model

3.1 Modelling of the HVDC system and its controller.

The structure of the HVDC unit with a dual-sequence current control loop is shown in Fig. 2 [11]. As shown in the figure, the converter is synchronised with the grid by the Phase Locked Loop (PLL) [12]. Considering the opposite rotational direction between the positive and negative sequence components in the synchronous reference frame (*dq* frame), the phase angle of the latter is the additive inverse of the phase angle of the former. The derived angels are used in the Park Transformation. Assisted by the notch filter, with a cut-off frequency of 2 times of the fundamental frequency (aiming to suppress the oscillations with 2 times of the fundamental frequency), the positive and negative sequence voltage and current are separated. The behaviour of the HVDC system during the faults is mainly determined by the current references generated by the outer power controller, which is calculated based on the current calculation function in the outer power controller. The fault current limiter is provided to restrict the fault current to the defined safety level. The generated references are tracked by the inner current controller with positive and negative sequence control loop.

3.1.1 Outer loop controller design of the HVDC system.

When asymmetrical faults occur in the grid, the negative sequence components are introduced to the three phase voltage and current. Based on the instantaneous power theory [13], the active and reactive power generated from the converter in *abc* frame can be expressed as (1) and (2).

$$p = v \cdot i \tag{1}$$

$$q = v_{\perp} \cdot i \tag{2}$$

Where v and i are the three-phase voltage and current and $v_{\perp}$ is the orthogonal version of the original grid voltage vector v. Considering the positive and negative sequence components, the (1) and (2) can be extended as (3) and (4).

$$p = v^{+}i^{+} + v^{-}i^{-} + v^{+}i^{-} + v^{-}i^{+} \tag{3}$$

$$q = v_{\perp}^{+}i^{+} + v_{\perp}^{-}i^{-} + v_{\perp}^{+}i^{-} + v_{\perp}^{-}i^{+} \tag{4}$$

To further simplify the analysis, (3) and (4) are transformed

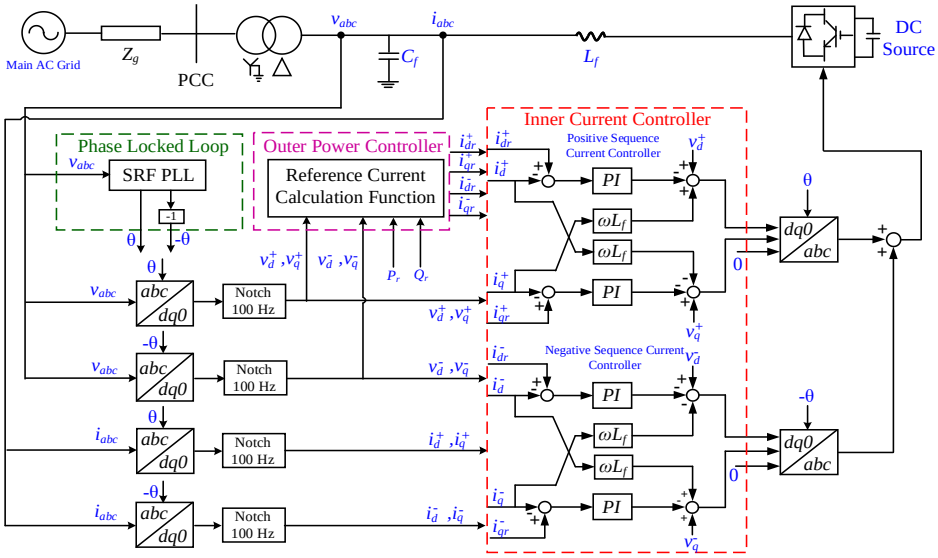

Fig. 2 Control structure of the HVDC system with dual- sequence current control loop [11].

into the synchronous reference frame by applying the Park Transformation, which yields (5) [7]:

$$\begin{bmatrix} \bar{P} \\ P_C \\ P_S \\ \bar{Q} \\ Q_C \\ Q_S \end{bmatrix} = \frac{3}{2}\begin{bmatrix} +v_d^+ & +v_q^+ & +v_d^- & +v_q^- \\ +v_d^- & +v_q^- & +v_d^+ & +v_q^+ \\ +v_q^- & -v_d^- & -v_q^+ & +v_d^+ \\ +v_q^+ & -v_d^+ & +v_q^- & -v_d^- \\ +v_q^- & -v_d^+ & +v_q^+ & -v_d^+ \\ -v_d^- & -v_q^- & +v_d^+ & +v_q^+ \end{bmatrix} \times \begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \end{bmatrix} \quad (5)$$

where v_d^+, v_q^+, i_d^+ and i_q^+ are the positive sequence voltage and current and v_d^-, v_q^-, i_d^- and i_q^- are the negative sequence voltage and current in d and q axes. $\bar{P}$ and $\bar{Q}$ are the average real and reactive power, which are the power references given by the user. P_C, Q_C and P_s, Q_s are the cosine and sine terms of active power and reactive power respectively. The solution of (5) is shown as (6)[14].

$$\begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \end{bmatrix}_r = \frac{2}{3}\begin{bmatrix} +v_d^+ & +v_q^+ & +v_d^- & +v_q^- \\ +v_q^+ & -v_d^+ & +v_q^- & -v_d^- \\ +v_d^- & +v_q^- & +v_d^+ & +v_q^+ \\ +v_q^- & -v_d^- & -v_q^+ & +v_d^+ \\ +v_q^- & -v_d^- & +v_q^+ & -v_d^+ \\ -v_d^- & -v_q^- & +v_d^+ & +v_q^+ \end{bmatrix}^{-1} \times \begin{bmatrix} \bar{P} \\ \bar{Q} \\ P_C \\ P_S \\ Q_C \\ Q_S \end{bmatrix}_r \quad (6)$$

In (6), the values of i_{dr}^+, i_{qr}^+, i_{dr}^- and i_{qr}^- on the left hand side can be manually set, therefore, these variables are called as 'controllable variables'. Based on the control objectives, different control strategies can be realised to achieve different response during the faults, i.e. balanced current control ($i_{dr}^- = i_{qr}^-$=0) to generate three-phase balanced currents, constant active power control ($P_C = P_S = 0$) to suppress the active power oscillation, and constant reactive power control ($Q_C = Q_S = 0$) to suppress the reactive power oscillation during the faults. The outer power controller of the developed HVDC unit is designed based on (7) [14], which can achieve the same performance as the controller in [6]:

$$\begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \end{bmatrix}_r = \begin{bmatrix} \frac{+v_d^+}{D'} & \frac{+v_q^+}{E'} \\ \frac{+v_q^+}{D'} & \frac{-v_d^+}{E'} \\ \frac{-K_{mode}v_d^-}{D'} & \frac{+K_{mode}v_q^-}{E'} \\ \frac{-K_{mode}v_q^-}{D'} & \frac{-K_{mode}v_d^-}{E'} \end{bmatrix} \times \begin{bmatrix} \bar{P} \\ \bar{Q} \end{bmatrix} \quad (7)$$

where the D' and E' are defined as:

$$D' = \left((v_d^+)^2 + \left(v_q^+\right)^2\right) - K_{mode}\left((v_d^-)^2 + \left(v_q^-\right)^2\right)$$

$$E' = \left((v_d^+)^2 + \left(v_q^+\right)^2\right) + K_{mode}\left((v_d^-)^2 + \left(v_q^-\right)^2\right)$$

The constant active power, balanced current and constant reactive power controllers are achieved when the values of K_{mode} equal 1, 0 and -1, respectively. Furthermore, the values of K_{mode} can be continually varied between -1 and 1, hence, different levels of negative sequence current can be injected in order to achieve a specific objective or desirable response.

3.1.2 Fault current limiter design of the HVDC system.

To ensure the fault current is always within the maximum tolerable limit when different control strategies are used by the HVDC system, a dedicated fault current magnitude limiter (used by all control modes) has been developed. The flowchart of the limiter is shown in Fig. 3, where there are two stages involved: i.e. stage I for fault detection and stage II for current suppression. In stage I, the positive sequence voltage in d axis, i.e. V_{dqF_d}, is transformed to per unit value and compared with the user-defined voltage threshold, V_{de}. If the value of V_{dqF_d} (pu) is lower than this threshold, the converter will consider there is a fault in the grid and it will move to stage II to suppress the fault current from the converter. Otherwise, the converter will take the initial input P_r^0 and Q_r^0 as the power references. The variable SF is a scaling factor, which is defined in (8), where I_d^+, I_q^+, I_d^-, I_q^- are the positive and negative sequence current on the dq frame and I_{FCL} is the allowed maximum current. In stage II, the power references in each step are calculated by (9) and (10), where n equals 1,2,…N. According to (9) and (10), the power references in the current step equals the power reference in the last step dividing the value of SF in the last step. These decreased power references will decrease the fault current from the converter and further reduce the value of the SF. The iterative process in stage II will continue until the value of the SF is lower than 1, which means the current has been supressed below the maximum tolerable current of the converter.

$$SF = \frac{\sqrt{I_d^{+2} + I_q^{+2}} + \sqrt{I_d^{-2} + I_q^{-2}}}{I_{FCL}} \quad (8)$$

$$P_r^n = \frac{P_r^{n-1}}{SF^{n-1}} \quad (9)$$

$$Q_r^n = \frac{Q_r^{n-1}}{SF^{n-1}} \quad (10)$$

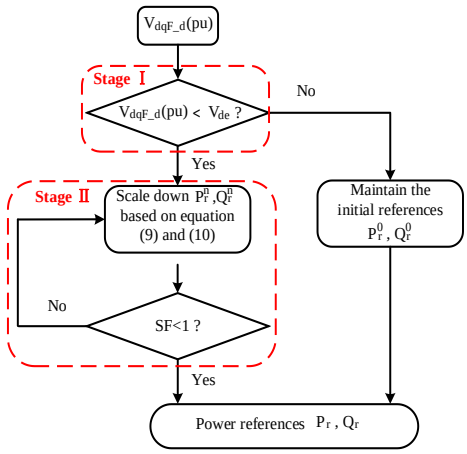

Fig. 3 Flowchart of the designed fault current limiter.

3.2 Modelling of the NSG and its controller.

Since the NSG element in the model represents, in a general manner, the overall equivalent non-synchronous generation connected at the remote bus, the most widely used PQ control strategy is adopted for the NSG element. The basic structure of the controller of the NSG converter is available in [15]. Similarly, to avoid the overcurrent issue during fault periods, the fault current limiter is designed based on (11), where i_{dref} and i_{qref} are the current references at dq frame and i_{max} is the maximum acceptable current of the converter.

$$i_{dref} = \sqrt{(i_{max})^2 - (i_{qref})^2} \quad (11)$$

3.3 Modelling of the SC.

3.3.1 SC based on the AVR control.

The AVR controller is the one of the most commonly used controllers for the SC. An AVR controller is implemented based on the IEEE type 1 excitation system [16] and its structure can be found in the manual of RSCAD [17].

3.3.2 SC based on the constant reactive power control.

Different from the AVR controller, the constant reactive power controller can ensure the reactive power from the SC to track the pre-set reactive power reference. The diagram of the controller is shown as Fig. 4, where it can be seen that, a PI controller is employed to ensure the output reactive power, Q_{pu}, to follow the reactive power reference, Q_{pu}^*.

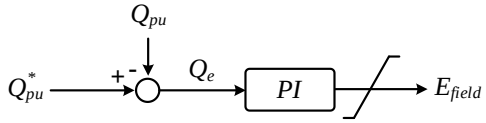

Fig. 4 Structure of the constant reactive power controller.

3.3.3 SC based on the droop control.

Compared with the previous two controllers, the reactive power governed by the droop controller is not only determined by the power reference, but also dependent on the machine's terminal voltage. Its characteristic is described as (12), where K_q is the droop gain. Based on which, the droop controller is developed as shown in Fig. 5.

$$Q_{pu} = Q_{pu}^* - \frac{(V_{pu} - V_{pu}^*)}{K_q} \quad (12)$$

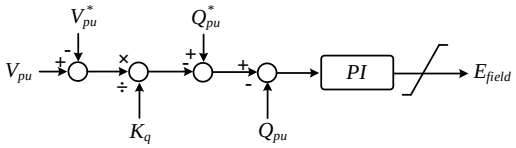

Fig. 5 Structure of the reactive power droop controller.

3.3 Configuration of the developed network.

As shown in Fig. 1, there are four equivalent impedances, Z_{eq1} to Z_{eq4}. In transmission systems, fault level data is typically available, which includes both single-phase-to-earth and three-phase-earth fault level at each bus and the fault contribution from each connected element. With the fault level data either from fault level studies or users' input, positive and zero sequence impedance of Z_{eq1} and Z_{eq2} could be calculated. Based on IEC 60909, the fault level is calculated with assumptions [18]:

- The resistance is neglected in the calculation.
- The line capacitance is neglected.
- The pre-fault voltage in the network is assumed to be the rated system voltage.
- The fault impedance for fault level calculation is zero.

Table 1 Fault level data for the configuration

Name	Definition
$I_{A\_3PH\_T}$	Total 3Ph-E fault level at Bus A
$I_{A\_1PH\_T}$	Total Ph-E fault level at Bus A
$I_{A\_3PH\_L}$	3Ph-E fault contribution from Line 1 at Bus A
$I_{A\_1PH\_L}$	Ph-E fault contribution from Line 1 at Bus A
$I_{B\_3PH\_T}$	Total 3Ph-E fault level at Bus B
$I_{B\_1PH\_T}$	Total Ph-E fault level at Bus B
$I_{B\_3PH\_L}$	3Ph-E fault contribution from Line 1 at Bus B
$I_{B\_1PH\_L}$	Ph-E fault contribution from Line 1 at Bus B

Provided the fault level data in Table 1 is known, Z_{eq1} and Z_{eq2} can be calculated. Firstly, the fault infeed of Bus A under three-phase and single-phase to ground fault are calculated by (13) and (14) respectively.

$$I_{F\_3PH} = I_{A\_3PH\_T} - I_{A\_3PH\_L} \quad (13)$$

$$I_{F\_1PH} = I_{A\_1PH\_T} - I_{A\_1PH\_L} \quad (14)$$

The positive sequence impedance of Z_{eq1} is calculated based on (15), where V_s is the rated value of the line voltage.

$$Z_{eq1\_1} = j\frac{V_s}{\sqrt{3}\times I_{F\_3PH}}\ (\Omega) \quad (15)$$

When the single phase to ground fault occurs in the grid, the values of the positive, negative and zero sequence fault current, $I_{F\_1PH\_1}$, $I_{F\_1PH\_2}$, $I_{F\_1PH\_0}$, are the same and equal to $\frac{1}{3}I_{F\_1PH}$ [19]. Additionally, the positive and negative sequence impedance, Z_{eq1_1} and Z_{eq1_2}, are regarded having the same magnitude. The sequence network is shown in Fig. 6, where V_p is the rated phase voltage. The zero-sequence impedance is calculated by (16).

$$Z_{eq1\_0} = j\left(\frac{V_p}{\left(\frac{1}{3}\times I_{F\_1PH}\right)} - 2\times Z_{eq1\_1}\right)\ (\Omega) \quad (16)$$

Similar procedure can be followed for calculating the value for Z_{eq2}, which determines the system strength at Bus B. It should be noted that instead of using fault level data from system studies, the users can also intentionally select a certain fault

level of interest to adopt a set of values for Z_{eq1} and Z_{eq2}, which would allow the representation of a correspond level of system strength at the two buses for testing purpose.

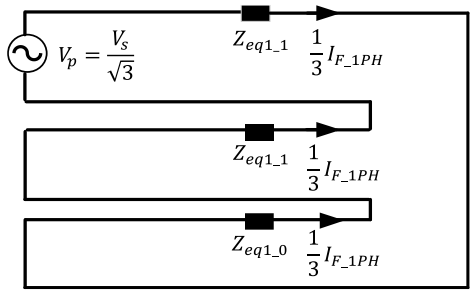

Fig. 6 Sequence network for single phase to ground fault.

4 Case Studies

4.1 Studied network and cases.

In these studies, the impact of integrating a 1 GVA HVDC system on distance protection is investigated using the developed network model. It is intended to investigate a scenario with three phase to earth and single phase to earth fault level contributing from SG1 at bus A of $I_{F\_3PH} = 4.33\ kA$ and I_{F_1PH} =2.78 kA. Using (15) and (16), the positive and zero sequence impedance of Z_{eq1} can be calculated, i.e. $Z_{eq1\_1} = j53.33$ and $Z_{eq1\_0} = j142.56\ \Omega$. For simplicity, in this study the impedance of Z_{eq2} is assumed to be the same as Z_{eq1}. It should be noted that in reality, the users can adjust the fault level data at Bus A and B, which would effectively adjust the system strength at these two buses to suit specific testing purposes. The parameters of the studied network are shown in Table 2. Four cases outlined in Table 3 are designed to test the distance relay performance.

4.2 Distance relay model.

In these studies, the simulated three phase voltage and current measured at the distance relay point (Bus A) in the RTDS network (Fig. 1) are saved and used as the inputs for a distance relay model constructed in SIMULINK. The distance relay model with the basic structure is designed based on the Mho characteristic [19]. Two protective zones, 'zone1' and 'zone 2', are investigated in these studies. The settings of zone 1 and zone 2 are set as 80% and 120 % of the total positive sequence impedance of the line.

4.3 Simulation results.

In the studies, Phase A to B faults at 75% of the line with 1 Ω resistance are simulated for all four cases. The distance relay performance under different cases are presented in Fig. 7 to Fig. 10. In these figures, the impedance locus of the distance relay is displayed in (a) with normal view, and (b) with a zoomed-in impedance locus version. The voltage and current seen by the relay during the fault are displayed in (c) and (d) respectively in these figures. Through comparing the results in Fig. 7 to Fig. 9, it is obvious that with the decrease of the values of K_{mode}, the values of the measured reactance gain a small increase and the impedance locus moves gradually to zone 2. The worst scenario can be found in Fig. 9, where the measured impedance of distance relay is almost out of the protective zone 1. Based on the results in Fig. 9 and Fig. 10, the measured impedance is pulled back to zone 1 with the assistance from the SC. Therefore, it can be concluded that the control strategies of the HVDC unit along with the connection of SC have clear impacts on the distance relay performance, and the presented representative model offers an ideal tool for detailed investigation and evaluation of such impact under different network operating conditions.

Table 2 Parameters of the studied network

Parameters	Values
V_S	400 kV
Z_{Line}	1.15+ j12.65 Ω
Z_{eq1_1}, Z_{eq2_1}	j53.33 Ω
Z_{eq1_0}, Z_{eq2_0}	j142.56 Ω
Z_{eq3}	0.29+ j3.12 Ω
Z_{eq4}	0.29+ j3.12 Ω
P_{HVDC}, Q_{HVDC}	1000 MW; 0 MVar
P_{NSG}, Q_{NSG}	2000 MW; 1000 MVar
P_{L1}, Q_{L1}	100 MW; 50 MVar
P_{L2}, Q_{L2}	2000 MW; 900 MVar

Table 3 The information of the designed cases

Cases Number	K_{mode} Value	SC (MVar)
1	1	N/A
2	0	N/A
3	-1	N/A
4	-1	300

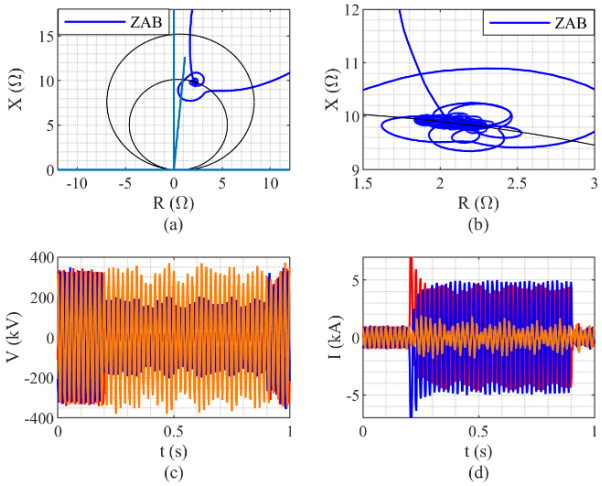

Fig. 7. Simulation results of Case 1: (a) impedance locus, (b) zoomed impedance locus, (c) input voltage, (d) input current.

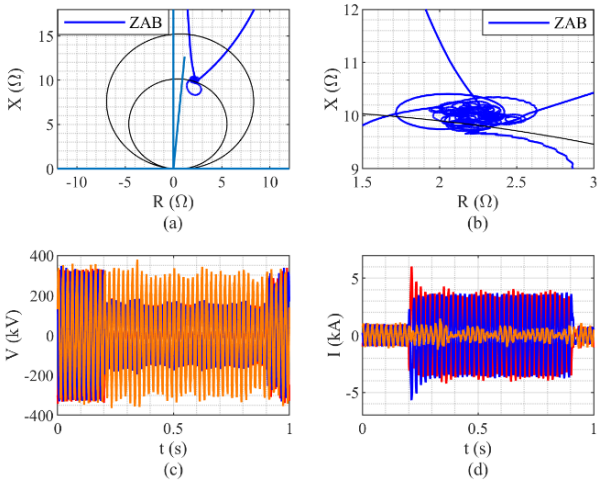

Fig. 8 Simulation results of case 2: (a) impedance locus, (b) zoomed impedance locus, (c) input voltage, (d) input current.

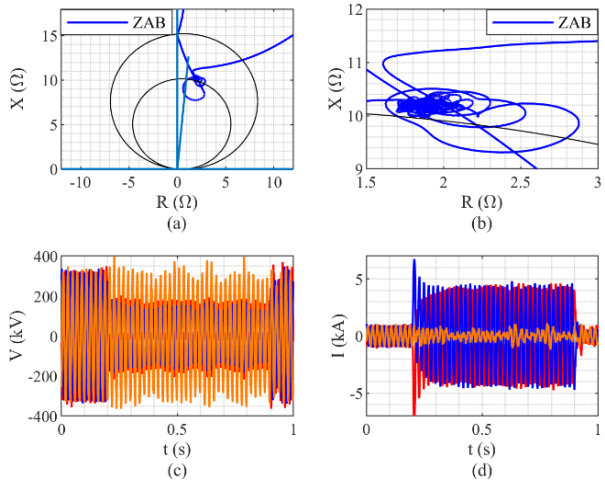

Fig. 9 Simulation results of case 3: (a) impedance locus, (b) zoomed impedance locus, (c) input voltage, (d) input current.

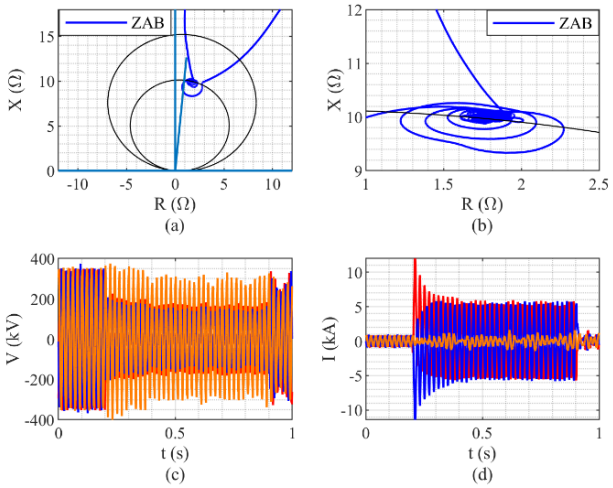

Fig. 10 Simulation results of case 4: (a) impedance locus, (b) zoomed impedance locus, (c) input voltage, (d) input current.

5 Conclusions

In this paper, a reduced but reprehensive RTDS network is developed to assist the evaluation and testing of potential impact of HVDC systems' control and the system strength on the AC protection performance. The developed network model can be configured to represent the equivalent network condition for a selected circuit and it can also be flexibly configured to evaluate key factors that could affect the protection performance, including the level of system strength, different control strategies adopted in the HVDC system, different levels of synchronous compensation installed at the HVDC site, etc. Case studies have been presented to show the use of the model for evaluating the distance protection performance with different HVDC controllers and installed SC capacities. The developed model is not only suitable for pure simulation-based studies but can also be used for hardware-in-the-loop tests of an external physical relay, thus providing an ideal platform for testing potential critical protection issues and investigating potential solutions in future power networks with high penetration of renewables.

5 Acknowledgements

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