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A Scheme to Improve the Stability and Accuracy of Power Hardware-in-the-Loop Simulation

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***Abstract*—Power hardware-in-the-loop (PHIL) is a state-of-the-art simulation technique that combines real-time digital simulation and hardware experiments into a closed-loop testing environment. The transportation delay or communication latency impacts the stability and accuracy of PHIL simulations. In this paper, for the purpose of synchronizing the PHIL output signal and promoting both the stability and accuracy of PHIL simulation, a hybrid compensation scheme is proposed to compensate for the time delay in the PHIL configuration. A model-based compensator is implemented to shift the time delay out of the PHIL closed-loop to enhance PHIL stability. A time delay compensation model and its equivalent inverse model are employed in the PHIL closed-loop to compensate for the time delay. A phase lead compensator and digital linear-phase frequency sampling filter (FSF) are candidate compensation models to compensate for the time delay and reshape the phase curve on a harmonic-by-harmonic basis. Simulations are made to validate the effectiveness of the compensation scheme.**

***Index Terms*—Power hardware-in-the-loop (PHIL), time delay compensation, model-based compensator, stability and accuracy.**

I. INTRODUCTION

Power hardware-in-the-loop (PHIL) simulation is an effective way to narrow the gap between computation-based digital simulation and analogue hardware laboratory testing [1], [2]. Advanced real-time digital simulators facilitate the simulation capability of PHIL, which enables large scale power system to be replicated accurately in the real-time simulation environment and provides an effective way to carry out non-destructive and repeated investigation of the complex power system, candidate apparatus, and control algorithms under broad-spectrum operating conditions, in particular for extreme scenarios [3], [4]. In PHIL simulation, a four-quadrant power amplifier-based power interface (PI) is widely utilized to realize the transparent power exchange between the digital real-time simulation (DRTS) platform and the hardware under test (HUT) [4]. Due to the splitting of the original power system into digital simulation and real power hardware, the digital processing of DRTS platform, the analog-to-digital converter (ADC), digital-to-analog converter (DAC), and the digital control of the power amplifier all inevitably introduce a time delay to the PHIL closed-loop configuration [5]. The time delay that exists in the closed-loop significantly deteriorates the system stability margin and introduces a phase lag to the power signal, which plays a dominant role in unstable and inaccurate PHIL simulation [6]–[8]. Mitigating the time delay effects is a priority in PHIL simulation to avoid significant simulation errors and potential damage to the apparatus in the closed-loop simulation configuration, especially for high power level application [6].

As the time delay contributes to unstable and inaccurate PHIL simulation on a considerable scale, many research efforts have been devoted to either increase the PHIL closed-loop stability margin or compensate for the time delay. The hardware inductance addition method was introduced in [9] to increase the impedance of the HUT side. However, in doing so, the PHIL system stability margin is improved at the expense of distorting the original PHIL topology, which leads to inaccurate simulation. A first-order low-pass filter can be deployed in the feedback path of the PHIL closed-loop to improve the system stability, thus enhancing system tolerance to the time delay [10]. However, setting the cut-off frequency of the low-pass filter is a trade-off between realising improved stability margin whist minimizing the deterioration of accuracy. The introduction of a low-pass filter also significantly limits the system bandwidth. In [7], [11], an FFT-based frequency domain phase lag compensation algorithm was proposed. The frame-by-frame processing scheme of FFT presents a significant computation burden, which limits not only the upper harmonics this method can compensate for but also its application to the consideration of electromagnetic transient (EMT). Based on modern real-time computation platforms, a multi-rate partitioning interface [12] was proposed to divide the original PHIL system into some dedicated fast subsystems with small time-steps. The introduction of multiple fast subsystems can improve the system stability significantly, guarantee certain accuracy, and improve system bandwidth. This method requires multi-core real-time simulation platforms and the fidelity depends on the dynamic coupling and clock synchronization between all subsystems.

In this paper, we propose a hybrid time delay compensation scheme for PHIL real-time simulation. This paper is organized in the following way: Section II provides an overview of the PHIL system, interface algorithms, and time delay effects on PHIL stability. In section III, the derivation and implementa-

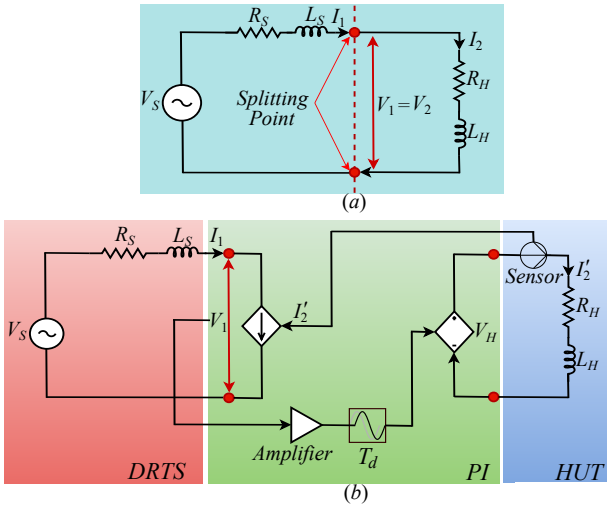

Fig. 1: (a) Natural lumped voltage divider system and (b) PHIL system with ITM algorithm.

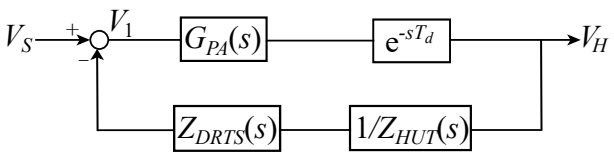

Fig. 2: Equivalent diagram of voltage-type ITM PHIL system.

tion details of the proposed hybrid compensation scheme are elaborated. Section IV presents an extension of the time delay compensation scheme, including a phase-lead compensator and frequency sampling filter. In section V, case studies with digital simulations are carried out to validate the effectiveness of the proposed compensation scheme. Section VI makes a conclusion and summarizes the scope of the proposed method.

II. An Overview of PHIL Simulation

This section explains the interface algorithms, the most commonly used PHIL configuration, its system transfer functions, the time delays, and their effects on PHIL stability.

A. Interface algorithm and PHIL configuration

The interface algorithm (IA) defines the processing manner of the exchanged signal within the PHIL simulation configuration. In terms of the accuracy and stability, the ideal transformer model (ITM) and damping impedance method (DIM) are the most widely utilized algorithms as summarised in [13]. ITM is the most straightforward approach as a result of its ease of implementation and relatively high stability and accuracy. The voltage-type or current-type ITM is determined by the impedance ratio of the Z_{DRTS}/Z_{HUT} to maintain stability criterion [3], [13].

Fig. 1 illustrates the PHIL configuration with ideal naturally coupled power system and voltage-type ITM interface algorithm. The original power system is expressed by a lumped voltage divider topology and is divided into DRTS platform and HUT from the splitting point. The power interface consists of the power amplifier and power signal channels that set the links between DRTS and HUT. This PHIL configuration will be used throughout the paper.

B. Time delay and PHIL system stability

As summarised in [5], the Laplace transform of the total time delay in the PHIL closed-loop can be expressed as e^{-sT_d}. Being proportional to the frequency of input power signal, the phase shift caused by the time delay distorts the V-I phase relationship and changes the power transfer between the DRTS platform and the hardware components.

The equivalent diagram of voltage-type ITM-based PHIL configuration is shown in Fig. 2 and its closed-loop system transfer function is expressed as:

$$G_{cl}(s) = \frac{G_{PA}(s)\, e^{-sT_d}}{1 + G_{PA}(s)\, \frac{Z_{DRTS}(s)}{Z_{HUT}(s)} e^{-sT_d}} \tag{1a}$$

$$Z_{DRTS}(s) = R_S + sL_S, Z_{HUT}(s) = R_H + sL_H \tag{1b}$$

where $G_{PA}(s)$, $Z_{DRTS}(s)$, and $Z_{HUT}(s)$ are the transfer functions of the power amplifier, DRTS platform, and HUT.

It is evident from (1a) that the time delay is present in the system characteristic equation and the open-loop transfer function. Phase margin (PM) measures the system stability tolerance to the time delay. Stability can only be guaranteed provided that PM is larger than zero and that the corresponding phase response satisfies the following criterion:

$$\angle \left[G_{PA}(jw_{cg})\, \frac{Z_{DRTS}(jw_{cg})}{Z_{HUT}(jw_{cg})} \right] - \angle(w_{cg}T_d) > -180^\circ \tag{2}$$

where w_{cg} is the gain crossover frequency at which the magnitude of open-loop transfer function is equal to 1 (0 dB).

The time delay has no effect on the magnitude of the frequency response of the open-loop transfer function and the gain crossover frequency w_{cg} [14]. However, as shown in (2), the phase lag (i.e., $\angle(w_{cg}T_d)$) caused by the time delay significantly degrades system stability as a result of the reduced phase margin (PM).

III. A Hybrid PHIL Interface Compensation Scheme

This section presents the derivation and design procedures of the proposed hybrid time delay compensation scheme. The details of its digital implementation are also presented.

A. Model-based compensator

The Smith predictor is known as an effective time delay compensation approach and has been applied in various engineering categories, such as in power electronics systems [15], [16]. Based on the Smith predictor compensation design criterion, a model-based compensator $C_{eq}(s)$ is designed to make the system behave like the original system in series with a pure time delay in the open-loop.

As shown in Fig. 3a, the compensator model $C_{eq}(s)$ is implemented in the forward path of the PHIL setup, whose closed-loop transfer function is:

$$TF_1 = \frac{C_{eq}(s) G_{PA}(s)\, e^{-sT_d}}{1 + C_{eq}(s) G_{PA}(s)\, \frac{Z_{DRTS}(s)}{Z_{HUT}(s)} e^{-sT_d}} \tag{3}$$

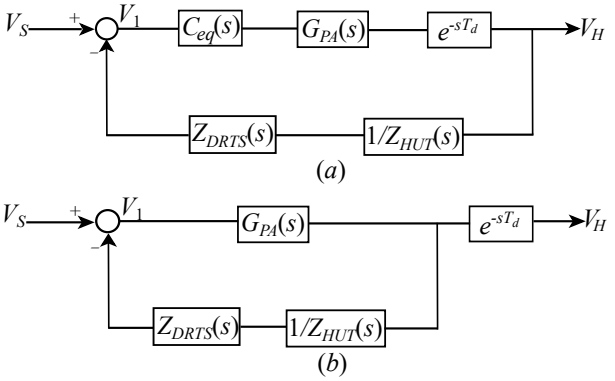

Fig. 3: (a) PHIL system diagram with compensator $C_{eq}(s)$ and (b) Equivalent PHIL system with shifted time delay in the open-loop.

Fig. 3b shows the equivalent PHIL diagram with time delay present in open-loop, whose closed-loop transfer function is:

$$TF_2 = \frac{G_{PA}(s)}{1 + G_{PA}(s)\frac{Z_{DRTS}(s)}{Z_{HUT}(s)}} e^{-sT_d} \tag{4}$$

For simplicity, let $G_p(s) = G_{PA}(s)\frac{Z_{DRTS}(s)}{Z_{HUT}(s)}$. $C_{eq}(s)$ is derived by setting the equivalence between the systems in Fig. 3 (i.e., $TF_1 = TF_2$), which yields:

$$C_{eq}(s) = \frac{1}{1 + \widetilde{G_p}(s)(1 - e^{-s\widetilde{T_d}})} \tag{5}$$

where $\widetilde{G_p}(s)$ and $\widetilde{T_d}$ are the estimations of $G_p(s)$ and T_d.

The structure of $C_{eq}(s)$ is illustrated in Fig. 4. The compensator is implemented under the assumption that the time delay T_d and the system models $G_p(s)$ are known accurately in advance, namely $\widetilde{G_p}(s) = G_p(s)$ and $\widetilde{T_d} = T_d$, which is reasonable in the controlled environment for PHIL.

For digital implementation, the continuous-time delay is expressed by delaying the uniformly sampled signal z^{-1} in the order of D [17] and the z-domain transfer function is in the form of:

$$H(z) = z^{-D}, D = T_d/Ts = Int(D) + F \tag{6}$$

where D is the division of time delay T_d and sampling time T_s and can be expressed by the sum of integer part $Int(D)$ and fractional part F.

Based on the recursive duplication of linear Lagrange interpolation techniques, an all-pass fractional delay Thiran filter [18] is utilized for the approximation of fractional delay F. Depending on the value of F, the transfer function of the Thiran all-pass filter can be further expressed by:

$$H(z) = \begin{cases} z^{-1} & \text{if } Int(D) = 0, \quad F > 0 \\ z^{-D} & \text{if } Int(D) \in R^+, F = 0 \\ \frac{\sum_{k=0}^{N} h_k z^{-(N-k)}}{\sum_{k=0}^{N} h_k z^{-k}} & \text{if } Int(D) \in R^+, F > 0 \end{cases} \tag{7a}$$

$$h_{k(k=0,1,2,\ldots N)} = (-1)^k \binom{N}{k} \prod_{n=0}^{N} \frac{D - N + n}{D - N + k + n} \tag{7b}$$

where $N(N = ceil(D))$ is the order of Thiran all-pass filter.

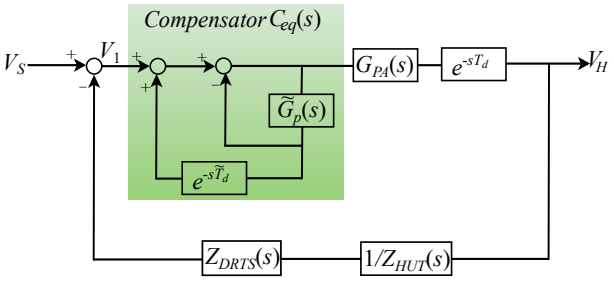

Fig. 4: PHIL block diagram with compensator $C_{eq}(s)$.

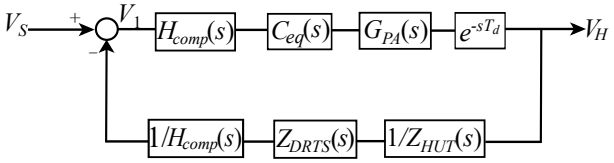

Fig. 5: Proposed PHIL system diagram with compensator $H_{comp}(s)$ and its inverse model.

B. Open-loop time delay compensation scheme

By implementing $C_{eq}(s)$, the overall system stability is guaranteed but there is still a presence of the delay e^{-sT_d} in the open-loop, which leads to inaccurate power transfer between the DRTS and HUT. The most straightforward way is to implement a compensation scheme $H_{comp}(s)$ in the open-loop. However, it is not practically feasible to introduce the compensator transfer function, $H_{comp}(s)$, within the simulated electrical system without creating a new interface to provide the equivalent open-loop compensation. Accordingly, this is implemented in the already available power interface which processes the output voltage signal from the DRTS and the current signal from the HUT. A scheme that implements $H_{comp}(s)$ in the forward path and its inverse block in the feedback path of the PHIL closed-loop is employed to provide equivalent open-loop compensation.

As shown in Fig. 5, $H_{comp}(s)$ and its inverse model are deployed in the PHIL closed-loop system, whose closed-loop transfer function is:

$$TF_{cl} = \frac{H_{comp}(s)C_{eq}(s)G_{PA}(s)\, e^{-sT_d}}{1 + H_{comp}(s)C_{eq}(s)G_{PA}(s)\frac{1}{H_{comp}(s)}\frac{Z_{DRTS}(s)}{Z_{HUT}(s)} e^{-sT_d}} \tag{8}$$

Assuming that $\widetilde{G_p}(s)$ and $\widetilde{T_d}$ are accurate estimations, substituting (5) into (8), the closed-loop transfer function becomes:

$$TF'_{cl} = H_{comp}(s)\frac{G_{PA}(s)}{1 + G_{PA}(s)\frac{Z_{DRTS}(s)}{Z_{HUT}(s)}} e^{-sT_d} \tag{9}$$

The overall closed-loop system behaviour, particularly the stability and accuracy, will not be directly influenced by the time delay and its compensation block errors as both of these are equivalent in the open-loop. Compared with the compensation scheme being directly deployed in the closed-loop, this hybrid compensation scheme can effectively avoid the distortion of the original PHIL system.

IV. Time Delay Compensation Schemes

It often happens in PHIL that the grid frequency/speed remains constant or varies slightly during the simulations, when the grid frequency/speed is governed by a slow time constant. Moreover, the real-time simulation is concerned only with a limited amount of harmonics. According to the frequency components to be processed, the following schemes could be employed as $H_{comp}(s)$ to provide phase lag compensation.

A. Single-frequency phase lead compensator

For the phase lead compensator in the form of:

$$PL = K\frac{\lambda s+1}{\alpha\lambda s+1}, (\alpha<1) \tag{10}$$

The maximum phase compensation ϕ_{max} contributed by a single phase lead compensator for the frequency of interest f_i is equivalent to the phase lag $2\pi f_i T_d$. The details of the tuning process of α and λ could be found in [14]. In order to provide the maximum phase compensation without distorting the input signal, the parameter K is tuned to maintain unity gain (0 dB) of the PL compensator at the frequency f_i.

The phase lead compensator provides positive phase over a wide range of frequencies, among which the unity gain can only be maintained for f_i while the magnitudes for other frequency components are non-unity and the phase for other harmonics are not in linear relationship as $\phi = 2\pi f T_d$. This method is only efficient to compensate the time delay for a single-frequency input signal. However, for an input signal with harmonics, the phase lead compensator amplifies or attenuates the input signal and leads to remarkable errors.

B. Linear-phase frequency sampling filter

Being equivalent to the non-recursive finite impulse response (FIR) filter, the frequency sampling filter (FSF) presents linear phase and steep cut-off amplitude characteristics [19], which enable the selective update of the signal phase or amplitude characteristics against any desired frequencies. Deduced from the frequency sampling theorem, FSF can be represented as the comb filter in series with complex resonator banks [17] and be written as:

$$H_{FSF}(z) = (1-r^N z^{-N})\sum_{k=1}^{N}\frac{e^{j\frac{2\pi k}{N}}}{1-rz^{-1}e^{j\frac{2\pi k}{N}}} \tag{11}$$

where $N\,(N=\frac{f_s}{f_0})$ is the window size, f_s is the sampling frequency, f_0 is the fundamental frequency, and $k\,(k=1,2,3,\cdots N)$ corresponds to the resonator for kf_0. r is the damping factor to force the zeros or poles of comb filter and resonator to be located at the circle with radius of $r\,(r=1-\varepsilon)$ to guarantee the stability of FSF and its inverse model.

The frequency response characteristics of the comb filter are shown in Fig. 6a. Being widely employed for the power system harmonic injection and harmonic extraction, it is evident from Fig. 6a that the comb filter can be envisioned as the notch filter with notches periodically spaced at the fundamental and harmonic frequencies. Being equivalent to the narrow band-pass

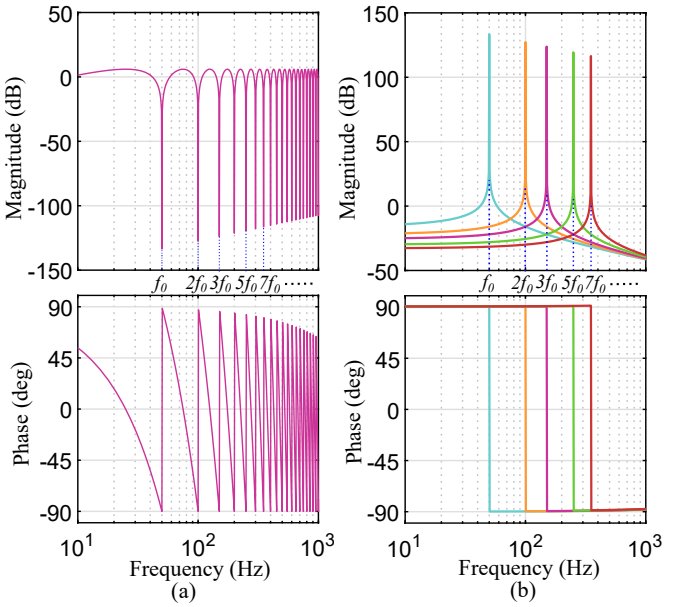

Fig. 6: (a) The frequency response of the $N-th$ order comb filter (b) The frequency response of the complex resonator for 1^{st},2^{nd},3^{rd},5^{th}, and 7^{th} harmonics.

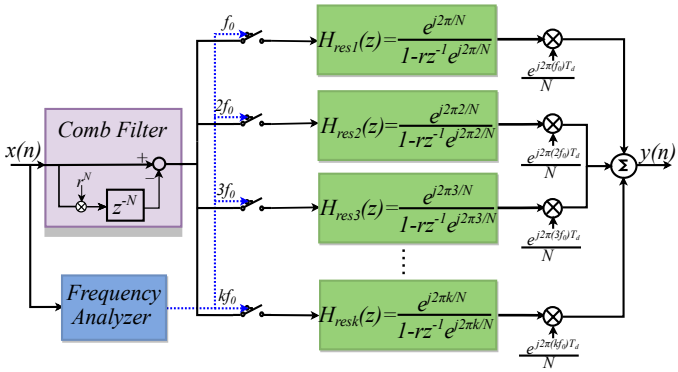

Fig. 7: The block diagram of the FSF with complex resonator banks and harmonic-by-harmonic time delay compensations.

filter, the comb filter attenuates the amplitude of the specific notch frequency component to an extremely low level. Fig. 6b shows the frequency response of single complex resonators. The single complex resonator presents the characteristics of a narrow bandwidth bandpass filter centred at the frequency kf_0 with a sharp cut-off amplitude.

An FSF filter with k-th order complex resonator in cascade with a comb filter can be envisioned as a band-pass filter centred at the resonant frequency kf_0. A scaling factor $\frac{1}{N}$ is implemented to each single resonator to reduce the overflow errors and to maintain the unity gain of the FSF, of which the phase updates over every sampling period. To compensate for the time delay on a harmonic-by-harmonic basis, an additional phase shift $e^{j2\pi k f_0 T_d}$ is implemented at the output of the resonator with resonator frequency kf_0. The FSF with time delay compensation can be expressed as:

$$H_{FSF}^{comp}(z) = (1-r^N z^{-N})\frac{1}{N}\sum_{k=1}^{N}\frac{e^{j\frac{2\pi k}{N}}e^{j2\pi k f_0 T_d}}{1-rz^{-1}e^{j\frac{2\pi k}{N}}} \tag{12}$$

TABLE I: PHIL system parameters for analysis and simulations.

Description	*Symbol*	*Value*
Nominal HUT resistance	R_H	$2\,\Omega$
Nominal HUT inductance	L_H	$1\,\text{mH}$
Naturally coupled DRTS resistance	R_S	$5\,\Omega$
Naturally coupled DRTS inductance	L_S	$2\,\text{mH}$
System fundamental frequency	f_0	$50\,\text{Hz}$
PHIL system time delay	T_d	$600\,\mu\text{s}$
DRTS voltage signal	V_S	$100sin(100\pi t)$

Fig. 7 presents the block diagram of the FSF-based time delay compensation filters. A real-time frequency component identification model is employed to obtain the frequency information and to determine the connection of corresponding complex resonators. This can reduce the computation burden, especially if only limited harmonics are to be processed.

For the practical implementation of the open-loop compensation scheme, it is feasible to implement the inverse phase lead filter in the feedback path. For a single-frequency input signal, an FSF with a single resonator and its inverse model can be deployed directly in the open-loop compensation scheme as the stability of both models have been guaranteed by the damping factor. For an input signal with harmonics, the FSF is implemented with different resonators connected in parallel, which means the inverse FSF under multiple frequencies scenarios is non-feasible. As the FSF with time delay compensation is equivalent to the approximation of e^{sT_d}, the Thiran approximation of time delay T_d is employed to represent the inverse FSF in the feedback path.

V. Case Study and Simulation Results

Matlab/Simulink simulation models are utilized to verify the effectiveness of the proposed compensation scheme. Table I shows the parameters of the PHIL set-up with equivalent voltage-divider topology as shown in Fig.1. In order to evaluate the effectiveness of the hybrid compensation scheme on a harmonic-by-harmonic basis, a voltage signal with 3^{rd} (20 V) and 5^{th} (3 V) harmonic injection is emulated as the equivalent voltage source at the DRTS platform. The voltage signal at the HUT side (i.e., V_H) is exploited to assess the performance of the proposed scheme.

A. Stability improvement by compensator $C_{eq}(s)$

By following (5) and the block diagram in Fig. 4, a digitized compensator $C_{eq}(s)$ is implemented in the forward path of the PHIL closed-loop with the assumption that the nominal estimation of the plant is equivalent to the emulated plant model, namely $\widetilde{G_p}(s) = G_p(s)$.

As shown in Fig. 8, for the ITM-based PHIL system without implementing compensation scheme, the output signal at the HUT side shows significant oscillations and reaches an unstable state. The existence of time delay contributes to unstable PHIL simulation as it exceeds the closed-loop critical value (PM/w_{cg}) and does not comply with the criterion in (2). After implementing the compensator $C_{eq}(s)$, comparing the output voltage curve of the compensator-based simulation with that of the uncompensated scenario, the closed-loop PHIL simulation becomes stable with the oscillations eliminated.

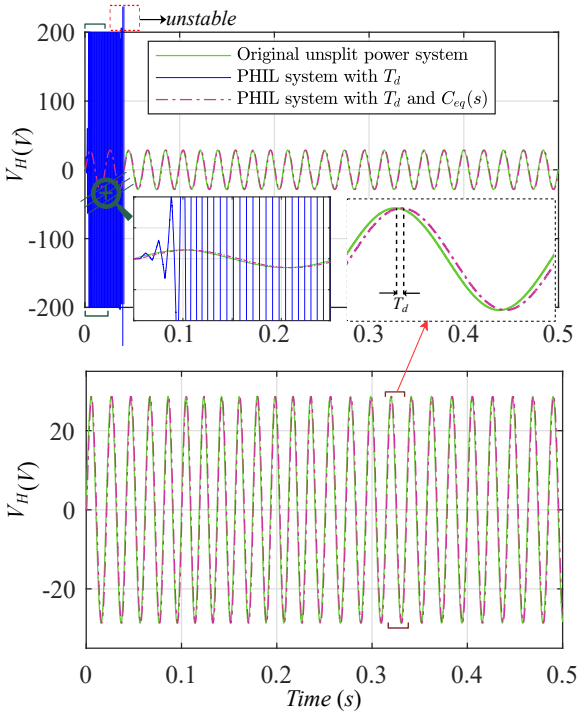

Fig. 8: HUT voltage of the original unsplit power system, PHIL system without $C_{eq}(s)$, and PHIL system with $C_{eq}(s)$.

Even though the compensator-based PHIL simulation presents enhanced stability, if its output signal is compared with that of the original unsplit case, it is evident that the phase lag caused by the time delay still exists.

B. Time delay compensation by phase lead filter and FSF

The phase lead compensator, FSF with single resonator for f_0 (exact inverse model), and FSF with resonator banks for multiple frequencies (approximate inverse model) are considered. The 3^{rd} and 5^{th}harmonics are injected at $t = 0.25$s.

Fig. 9 presents the output voltage behaviour of the compensated PHIL system. Before the harmonic injection, the voltage curve of the PHIL system with the phase lead compensator scheme is consistent with that of the original unsplit scenario. As a result of the introduction of damping factor r, there are slight differences between the output voltages of the FSF-based compensation scheme and the original unsplit scenario. All the compensation schemes provide the desired time delay compensation for the single-frequency input signal.

After harmonic injection, the output signal of phase lead compensator-based PHIL system presents significant discrepancies to that of the original PHIL system. For the phase lead compensator, the unity gain can only be maintained for f_0 while the gain for 3^{rd} and 5^{th} harmonics are larger than 0 dB and the phase compensation for these harmonics are not in linear relationship as $\phi_{comp} = 2\pi f$, which result in the amplified signal and the phase offset. The output voltage of the FSF (with single resonator for f_0) scheme only contains the fundamental frequency component due to the fact that the 3^{rd} and 5^{th} harmonics have been filtered out by the comb filter. For the input signal with harmonics, the phase lead filter or

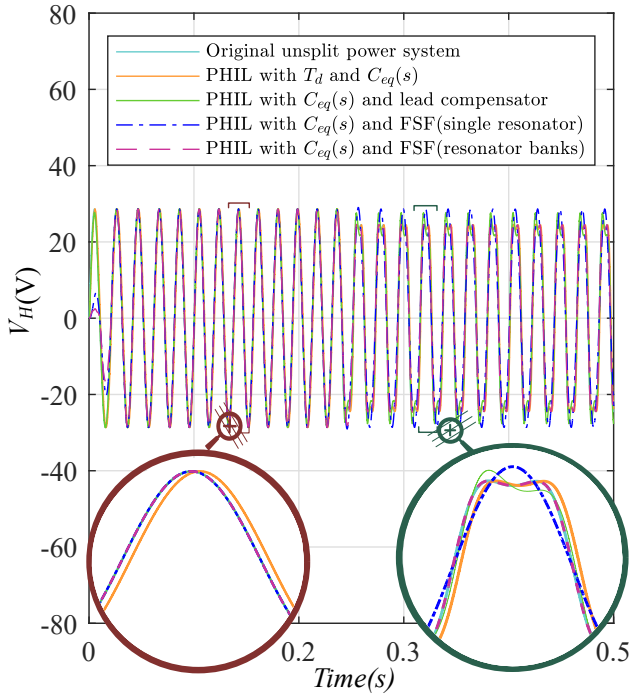

Fig. 9: HUT voltage of the PHIL system with phase lead filter, FSF (with single resonator for f_0), and FSF (with resonator banks for all harmonics) time delay compensation schemes.

the FSF (with single resonator) can only compensate phase lag to some extent and distorts the output signal waveform.

After two cycles, the output voltage of the PHIL system with FSF (with resonator banks for all harmonics) is consistent with that of the original PHIL system at the steady-state. Provided that stability is guaranteed, the FSF (with resonator banks for all harmonics) provides phase compensation on a harmonic-by-harmonic basis and the compensated phases are in linear relationship with the frequency components. Hence, this compensation scheme is more effective than phase lead filter or FSF (with single resonator for f_0) compensation under the harmonic injection scenarios.

VI. Conclusion

This paper presents a hybrid time delay compensation scheme for PHIL simulations. This scheme significantly mitigates the time delay effects on PHIL stability, enhance system stability margin, and simultaneously provides phase lag compensation to realize power signal synchronization. The derivations of the model-based compensation, FSF, and phase lead compensator are shown in this paper. The effectiveness and performance of the hybrid scheme on the stability improvement and phase curve reshaping have been validated and demonstrated via time-domain simulation results. Among all of these phase lag compensation cases, the hybrid compensation scheme with the FSF (with resonator banks for all harmonics) provides high-accuracy time delay compensation provided that the closed-loop stability is assured. The proposed method is useful for both of the single-frequency or harmonics cases, which is desirable for real-time PHIL simulations.

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