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Series Connection of Power Semiconductors for Medium Voltage Applications

PROGRAMA DE DOCTORADO:

AUTOMÁTICA Y ELECTRÓNICA

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Abstract

The series connection of power semiconductor devices allows the operation at voltage levels higher than the levels allowed by one single semiconductor. However, due to individual parameter differences of the series connected devices it is difficult to ensure a proper voltage balance between the series connected power devices and if any semiconductor exceeds its maximum blocking voltage it will fail.

Because of its gate controllability and its low gate energy requirements, the IGBT is the preferred choice when high number of switching devices must be connected in series. In this research work an IGBT gate driver has been developed which will control the behaviour of the IGBT during the switching process. In consequence, this gate driver should ensure a proper voltage balance between the series connected IGBT devices.

Basically, this PhD research work deals with the analysis and the modelling of the behaviour of the IGBT / Diode, proposes an active gate control and shows its validity for the series connection of IGBT / Diode devices.

Finally, voltage source converter topologies are briefly compared for reactive power compensation applications at Medium Voltage utility grids. The required blocking voltage capacity is achieved by means of the series connection of power semiconductor devices.

Resumen

La conexión en serie de semiconductores de potencia permite trabajar a tensiones de trabajo superiores a las que podría soportar un único semiconductor. Sin embargo, debido a diferencias en las características de los propios semiconductores es difícil garantizar el equilibrado adecuado de las tensiones de trabajo entre los distintos semiconductores conectados en serie. Si algún semiconductor supera su máxima tensión de trabajo este fallará.

Debido a su controlabilidad y bajo requerimiento energético por puerta el IGBT es la opción preferida cuando se requiere la conexión en serie de gran cantidad de semiconductores. En este trabajo de investigación se ha desarrollado un driver para IGBT que permita el control del proceso de conmutación del IGBT y garantice el equilibrado de las tensiones entre los IGBTs conectados en serie.

Básicamente, en este trabajo de investigación se presenta el análisis y modelado del comportamiento del IGBT/Diodo, el control activo empleado para controlar el proceso de conmutación del IGBT y su validez para la conexión en serie.

Finalmente, se presenta una pequeña comparación de convertidores de fuente de tensión para aplicaciones de compensación de energía reactiva conectados directamente a redes de Media Tensión. La capacidad de bloqueo requerida se obtiene mediante la conexión en serie de semiconductores de potencia.

Laburpena

Potentzi erdi eroaleen serie elkarketak, erdi eroale batek jasan dezakeena baino tentsio maila altuagoan lan egitea ahalbideratzen du. Hala ere, erdi eroaleen arteko ezaugarri ezberditasunak direla eta, zaila egiten da tentsio banaketa egokia zihurtatzea. Erdi eroaleetariko batek bere gehienezko tentsio maila gainditzen badu honek huts egingo du.

Erdi eroale asko seriean elkartu behar direnean IGBT-a izaten da aukerarik hobetsiena bere kontrolagarritasuna eta behar duen ateko energia maila baxua dela eta. Ikerketa lan honetan IGBT baten ateko “driver”-a garatu da. Honek IGBT-aren konmutazio prozesua kontrolatu behar du eta aldi berean, seriean elkarturiko IGBT-en artean, tentsio banaketa egokia lortu.

Funtsean, ikerketa lan honetan IGBT eta Diodo-aren analisia eta modelatua erakusten dira. Modu berean “driver”-ean erabilitako kontrola eta bere baliozkotasuna IGBT/Diodo-en serie elkarketarako erakusten dira.

Azkenik, Tentsio Ertaineko sarera zuzenean konektaturiko Tentsio Iturri Bihurgailuen arteko konparaketa bat egin da. Sareko tentsio maila altua dela eta erdi eroaleen serie elkarketa derrigorrezkoa da.

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“Azkenik, nire familiari eskertu nahi diot ni hemen egotearen aukera beraiek eman didatelako. Nire Ama Belen eta nire Aita Agustin-i bereziki eskertzen diet egunero daukaten guztia ematen dutelako beraien seme alabak behar duten guztiarekin hasi eta hezi daitezen. Nire arreba Idurre-ri, norbait arreba ona bada hori zu zarelako. Nire koñatu Arkaitz eta nire loba Xabier eta Eñaut-i, zuen irribarrea hor daukadala jakiteak egunero pozten nauelako. Eta batez ere nire izeba Nieves-i, bizitzak gogor astindu arren irribarrea galdu gabe egiten diezulako aurre arazoei. Eskerrikasko zuen maitasunarengaitik.”

Nomenclature

AC or ac Alternating current

A Curve fitting parameter

ASD Adjustable Speed Drives

ANPC Active NPC

BJT Bipolar Junction Transistor

$\mathbf{C_{GE}}$ Gate emitter capacitance

$\mathbf{C_{GC}}$ Gate collector capacitance

$\mathbf{C_{CE}}$ Collector emitter capacitance

$\mathbf{C_{iss}}$ Input capacitance

$\mathbf{C_{oss}}$ Output capacitance

$\mathbf{C_{rss}}$ Reverse transfer capacitance

$\mathbf{C_{eq}}$ Equivalent output capacitance

CSC Current Source Converter

CMC Cascaded Multilevel converter

DC or dc Direct Current

DCC Diode Clamped Converter

DVR Dynamic Voltage Restorer

$\mathbf{dI_C/dt}$ Collector current slope

$\mathbf{dV_{CE}/dt}$ Collector-emitter voltage slope

$\mathbf{dV_{GE}/dt}$ Gate voltage slope

$\mathbf{dI_G/dt}$ Gate current slope

$\mathbf{d_{dpl}}$ Deplexion region length

$\mathbf{dd_{dpl}/dt}$ Deplexion region change speed

EST Emitter-Switched Thyristor

ETO Emitter Switch-Off Thyristor

$\mathbf{Q_{rr}}$ Reverse recovery charge

Q Reactive power

RCD snubber Resistor Capacitor Diode snubber

$\mathbf{R_{DS(ON)}}$ Drain source on current

$\mathbf{R_g}$ Gate resistor

$\mathbf{R_{CE}}$ Collector emitter resistor

$\mathbf{R_{GINT}}$ Internal gate resistor

$\mathbf{R_{lim}}$ Current limiting resistor

r Redundancy on series connected devices

$\mathbf{r_d}$ Dynamic resistance

$\mathbf{R_{thJC}}$ Junction Capsule thermal resistance

$\mathbf{S_{AC}}$ Cable area of the Alternating system

$\mathbf{S_{DC}}$ Cable area of the Direct system

SVC Static Var Compensator

Si Silicon

SiC Silicon Carbide

SITh Static Induction Thyristor

SIT Static Induction Transistor

S1 … S4 Comparators output voltage (chapter 8)

SSSC Static Series Synchronous Compensator

SVM Space Vector Modulation

SHE Selective Harmonic Elimination

$\mathbf{S_1 \ldots S_n}$ Switching states of switches in a VSC (chapter 12)

E Electric field

E_{on} Switch on energy

E_{off} Switch off energy

f_{sw} switching frequency

FCTh Field-Controlled Thyristor

FCT Field Controlled Transistor

FACTS Flexible AC Transmission System

FC Flying Capacitor

GTO Gate Switch-Off Thyristor

g_{fs} transconductance

G1, G2 Electric Generators

HVDC High Voltage Direct Current Transmission

HVIGBT High Voltage IGBT

HCMC Hybrid Cascade Multilevel Converter

IGBT Insulated Gate Bipolar Transistor

IGTT Insulated Gate Switch-Off Thyristor

IGT Insulated Gate Thyristor

IGCT Integrated Gate-Commutated Thyristor

IEGT Injection Enhanced Gate Transistor

I_g or I_G Gate current

I_{DS} Drain source current

I_C Collector current

I_{CES} Collector-emitter leakage current

I_m Gate collector capacitance current

I_{GE} Gate emitter capacitance current

I_{CE} Collector emitter capacitance current

S_S Installed switching power

S_{SR} Relative installed switching power

STATCOM Static Var Compensator

THD Total Harmonic Distortion

T_J Junction temperature

T_C Capsule temperature

T1 and T1' Power switches in a VSC (chapter 12)

T1 … T6 Time intervals during the switching process (chapter 8)

t_{T1} ... t_{T6} Duration of each time interval (chapter 8)

TCR Thyristor controlled reactance

t_{delay} Delay time

t_{rr} reverse recovery time

U_R Load voltage

Ud1, Ud2 DC voltages

UPFC Unified Power Flow Controller

U_{conv} Converter's Output voltage

Uac Utility voltage

V_{ceth} Curve fitting parameter

Vak Anode-cathode voltage

V_{ce} or V_{CE} Collector-emitter voltage

V_{ge} or V_{GE} Gate-collector voltage

$V_{(BR)DS}$ Maximum blocking voltage of the device

$V_{GE(th)}$ Gate emitter threshold voltage

V_{CESAT} Collector-emitter saturation voltage

V_{CES} Maximum collector-emitter blocking voltage

I_{RRM} Reverse recovery current

$I_{leakage}$ Leakage current

$I_{Gprevious}$ Gate current during the previous time interval

$I_{G\_T2\_n}$ Gate current applied to T2 time interval

i_s Supply current

i_{sh} Harmonic content of the supply current

I_F Diode forward current

K Curve fitting parameter

LVIGBT Low Voltage IGBT

L_e Common emitter stray inductance

LVRT Low Voltage Ride Through

LCC Line Commutated Converter

MOS Metal Oxide Semiconductor

MCT MOS-Controlled Thyristor

MTO MOS Switch-Off Thyristor

N Number of voltage levels

NPC Neutral Point Clamped

n_s Number of switches in the switching valve

P_{GATE} Gate terminal power

P_{AC} Alternating line power

P_{DC} Direct line power

P Active power

PWM Pulse Width Modulation

PLC Programmable Logic Controllers

P_n Maximum output power

Q_G Gate charge

$V_{(BR)CES}$ Breakdown voltage

V_{CC} Output voltage

V_{GG-} Negative driver output voltage

V_{GG+} Positive driver output voltage

V_{CGE} Gate voltage on the IGBT chip

$V_{GE(th)}$ Gate threshold voltage

V_{th} Threshold voltage

V_p Curve fitting parameter

V_s Curve fitting parameter

V_{CE0} Curve fitting parameter

V_s DC bus voltage

V_{clamp} Clamp voltage

VG_L, E-, E+, VCE_L1, VCE_L2, VCE_SAT Voltage comparison levels in the gate driver

VSC Voltage Source Converter

V_{AB} Voltage between A terminal and B terminal

V_{an} Voltage between a terminal and n terminal

V_{DC}, V_{dc} DC bus Voltage

V_r voltage ripple

WTHD Weighted THD

α_{vp} Curve fitting parameter

α Switching angle in line commutated converters (chapter 16.1)

α Duty cycle in self commutated converters (chapter 13)

ΔI Curve fitting parameter (chapter 0)

ΔI Current ripple (chapter 13)

δ Phase difference between voltage vectors

Q_{GTOT} Total gate charge (chapter 16.2)

η Efficiency

Part 1: INTRODUCTION AND STATE OF THE ART OF SILICON BASED POWER SEMICONDUCTOR DEVICES

1 Introduction

Power Electronic Systems provide the ability to transform and transport electrical energy achieving reasonable levels of efficiency and reliability. In general, power electronic systems use power semiconductors operating in switching mode. Therefore, power electronic systems transform the energy flow from one form to another satisfying specific needs of the application. The hardware used to control the electrical energy is known as power converter. Depending on the performed transformation type the converter is known as rectifier (ac to dc), inverter (dc to ac), chopper (dc to dc) or frequency converter (ac to ac). These power electronic converters usually are composed by Control Systems, Switching Semiconductors, Passive Components (resistors, capacitors, inductors and transformers), Cooling Systems, Protection Systems, etc (Figure 1-1).

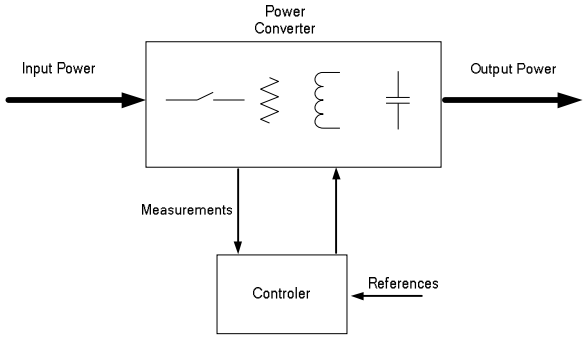


Figure 1-1: Block diagram of a power converter

Most of the current Power Electronic converters are used as motor drives, pumps and compressors. However, the development of power semiconductors has increased the number and type of applications where power converters have been used. Among these applications there are High Voltage Direct Current converter stations (HVDC) [JA-06] [AN-07], which allow higher efficiency and stability with respect to Alternating High Voltage transmission networks with long distance lines. Similarly, STATCOM converters replace SVCs (Static Var Compensator) in applications as voltage regulation, power factor correction and power flow stabilization [BA-05], [BE]. STATCOMs show better efficiency, lower size and higher flexibility than SVCs [NO-03]. On the other hand, about the 30% of the generated electrical energy employs power converters somewhere between the generation and the consumption [TO-05]. In the field of distributed generation, such converters act as interface between storage and distributed generation sources.

In general, the use of such converters improves the controllability of the voltage and the power flow. In addition, it helps mitigating the effects of possible faults in the network. Furthermore, the use of power converters increases the damping and stability of the electrical

grid and increases the capacity of the network to carry electrical energy close to the thermal limit of the line.

These power electronic systems offer excellent prospects for systems integration and therefore they are a very important research and development field worldwide [TO-05]. In fact, power electronics is considered one of the key technologies for energy transmission and distribution programs for the U.S. DOE, as well as for the European policy, which aims to achieve sustainable energy systems.

Power electronics are based mainly on power semiconductors, being the silicon (Si) the most widely used semiconductor material for their construction. The development of power converters has been accelerated as the result of the progress in the area of semiconductor physics and improvements in manufacturing technology [TO-05].

Power semiconductors are basically controllable switches which can be classified into two families: thyristors and transistors [AL-05]. These semiconductors can switch voltage and current levels that involve powers beginning from few watts to several megawatts in a fast and efficient way. This allows the development of High Power converters operating at high switching frequencies which cover applications before unattainable. There are four commercially available semiconductors suitable for Medium Voltage applications: GTO, IGCT, IGBT and IEGT. Among them, due to their operation characteristics, the IGBT and the IGCT are mainly used for Medium Voltage applications. While the IGBT provides a wide SOA, control simplicity and relatively low power losses, the IGCT, with its thyristor structure, is probably the best alternative for High Power applications. Next generations in power semiconductor technology will depend on the research of solutions in the areas of materials, circuits, system integration, etc...

Silicon (Si) based power Semiconductors can be processed practically without any defect. However, Silicon technology presents intrinsic problems to the properties of the material [TO-05]. One of these limitations resides in the (relatively) low thermal conductivity of the Silicon. This causes substantial junction temperature increases when power losses are generated inside the power semiconductor. In general, for silicon based semiconductors, the maximum working temperature of the semiconductor is close to 150 ºC. This fact makes compulsory the use of cooling systems to ensure that the operating junction temperature of the semiconductor does not exceed its maximum junction temperature. There are three standard options for removing the generated heat from power semiconductors: Air cooling, forced air cooling and water-cooled radiator. If the semiconductor withstand greater junction temperature, it is possible to reduce the cooling requirements making the cooling system cheaper and smaller.

However, the most important limit is related to the voltage blocking capability of Silicon based semiconductors. Due to the relatively narrow band gap of the Silicon (1.1eV), most semiconductor devices have a maximum voltage blocking capability lower than 10kV. This

implies that for Medium / High voltage applications the voltage blocking capability of these semiconductors is not sufficient. Therefore, there is a need of High Voltage semiconductors useful for energy distribution applications (tens of kV), energy transmission applications (hundreds of kV) and traction applications (Figure 1-2).

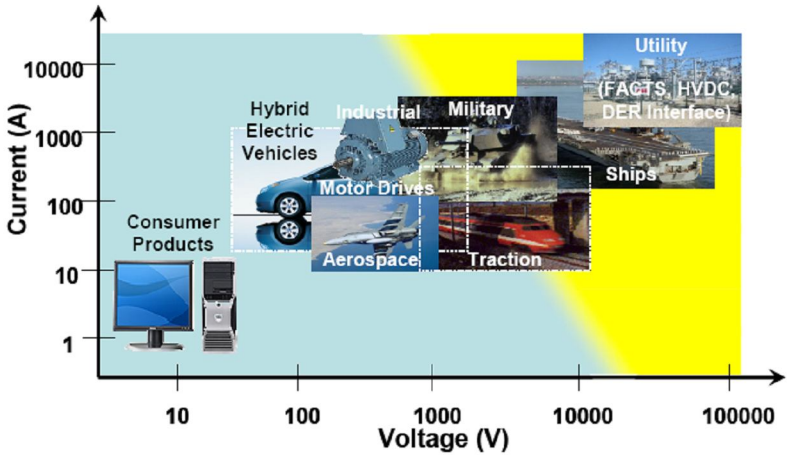


Figure 1-2: Power electronics applications and voltage / current ranges. Available semiconductors (blue), unavailable semiconductors (yellow) [TO-05].

Semiconductors with higher band gap than the Silicon have higher voltage blocking capability. In addition, those materials show better efficiency, higher reliability and lower thermal requirements. As an example, Silicon Carbide is very attractive to be used in High Voltage, high temperature and high efficiency applications. However, the high parasitic capacitances shown by Silicon Carbide semiconductors and their high level of impurities make current technologies unfeasible to this type of semiconductors. The state of the art of this technology will be briefly described in section 17.

In recent years, the use of multilevel converters is an interesting alternative in those applications where the blocking voltage of commercially available semiconductors is not sufficient to be used with well known two level converters [BA-05], [BA-07], [KR-07], [RO-07]. These converters can be connected at Medium Voltage without reductor transformers. In these converters, there are some power semiconductor and capacitor arrays whose connection or disconnection sets the output voltage level. The maximum voltage to be supported by each semiconductor is determined by the topology of the converter. However, the design of multilevel converters and their control become complex when large number of levels are considered.

Another choice is the use of few voltage levels or well known converter topologies in which the voltage blocking capability is achieved by means of the series connection of semiconductors. In this way, it is possible to create **switching valves** which will be able to operate at voltage levels higher than the supportable by one single semiconductor [PA-04], [SI-96], [GR-99b], [SA-04]. However, due to the parameter differences between the series

connected semiconductors, it is not possible to ensure a proper voltage balance between the series connected devices if some considerations are not taken into account. Therefore, inside the switching valve, there will be some semiconductors operating at higher voltages than other semiconductors. If the operating voltage of any semiconductor inside the switching valve exceeds its maximum blocking voltage, this device will fail. In addition, this failure could increase the failure possibility of the whole switching valve. This is why it is compulsory to take suitable measurements to guarantee the voltage balance in both steady state and transient state.

Classically, the steady state voltage balance has been achieved by means of resistive voltage dividers that impose the voltage during the blocking state. The transient voltage balance has been achieved by means of snubber networks that impose the voltage slope. Therefore, it is prevented that any semiconductor could reach its maximum voltage level. These snubber networks increase considerably the overall power losses of the converter. This is why it is desirable to avoid their use or at least minimize their size during the design process of the converter.

Therefore, the reduction of the number of needed components and the reduction of overall power losses can be achieved if the voltage balance is ensured without using any snubber network.

When IGCTs are connected in series, the use of snubber networks to ensure a proper voltage balance is compulsory. This is because the thyristor structure of the IGCT does not allow the control of the switching dynamics by means of the gate terminal. In consequence, the voltage slope has to be controlled using snubber networks [NA-00], [NA-01].

On the other hand, the IGBT allow the control of the switching dynamics by means of the gate terminal. This makes possible a proper voltage balance between the series connected IGBTs avoiding the use of snubber networks or at least minimizing their size. In addition, the low power requirements of the gate terminal of the IGBT make easier the integration of the power supply inside the gate driver in comparison with the IGCT. When a large number of semiconductors are connected in series, this makes the IGBT based switching valve more cost effective than the IGCT based ones [AL-05]. These facts explain why the IGBT is the chosen semiconductor for Medium / High Voltage applications where a large number of series connected semiconductors are needed. Among these applications there can be found HVDC converters rated at ±150kV / 300 MW, grid connected STATCOMs, etc...

There are many papers that propose some control strategies that aim the voltage balance between series connected IGBTs. In general, those strategies act on the gate terminal of the IGBT and avoid the use of snubber networks. These control methods are known as **Active Gate Control** methods [SH-06], [PA-04], [PA-95], [JA-03].

Over though many of the proposed control methods can satisfy the basic requirements of the series connection of IGBTs, in general, they present control loop stability problems, ineffectiveness of the power losses balance or even some dependency on the operating conditions. These facts make difficult the adoption of these control methods as standard solutions for the series connection of IGBTs.

In this context, the main aim of this PhD research work is the design and development of a gate driver, which should integrate the needed control strategies to guarantee the voltage balance in both steady state and transient state. This voltage balance should be achieved avoiding the use or at least minimizing the size of the needed snubber networks.

This work is divided in four main parts. The first part describes the main objectives of the work and shows a State of the Art of the most popular Power Semiconductor devices (Chapter 3). In addition, the advantages of the IGBT with respect to the IGBT for the series connection are detailed.

The second part describes the switching behaviour of the IGBT. Chapter 4 deals with the IGBT modelling while chapter 5 gives an analysis of the most important driving modes and their influence on the switching dynamics.

The third part deals with the series connection of IGBT/Diodes. Chapter 6 describes the problems related to the series connection of IGBTs when conventional IGBT gate drivers are used. Chapter 7 shows a short State of the Art of voltage balance methods for series connected IGBTs. Chapter 8 deals with the proposed solution in this research work while chapters 9 and 10 show the obtained results.

The fourth part is focused on potential applications for the switching valve based on the series connection of IGBT devices. Chapter 11 describes some utility grid applications where the switching valve can be used. Chapter 12 deals with the state of the art and modelling of most popular Voltage Source Converter topologies. Finally, chapter 13 compares Voltage Source Converters for STATCOM applications.

2 Objectives

The main objective of this PhD research work is the design and development of an IGBT gate driver which allows the series connection of IGBTs. Therefore, a proper voltage balance between series connected IGBT devices should be ensured without using snubber networks. In order to achieve the main objective the following sub-objectives are proposed:

- IGBT/Diode modelling
- Study of gate driving modes for the IGBT
- Control of the switching process of the IGBT
- Series connection of IGBTs
- Potential applications for High Voltage **switching valves**

3 State of the Art of Silicon based Power Semiconductors for Medium Voltage Applications

This chapter gives a synopsis of most popular self commutated Medium/High power switching devices: the IGCT and the IGBT. Section 3.2 shows a brief description of the IGCT (thyristor family) while section 3.3 deals with the IGBT description (transistor family). Advantages of the IGBT for the series connection with respect to the IGCT are given in section 3.4.

3.1 Introduction

As solid state switches, power semiconductors have become the actual replacement of electromechanical switches. These semiconductors have enough voltage blocking capability to operate up to 10kV without the series connection of switching devices. In addition, they can operate at high switching frequency so they allow an accurate control of the energy flow.

Nowadays, Silicon (Si) based semiconductor devices prevail on power electronic converters. Although this technology presents some advantages with respect to the electromechanical switches, it presents some electrical and thermal limitations that promote the research on other materials like Silicon Carbide (SiC) for power electronic applications, (section 17).

The development of power Electronic devices has been promoted as a result of the progress in the design and development of power semiconductors. Power electronics began when the bipolar transistor (BJT) was invented in the 50s. In the 60s appeared the thyristor as the first controllable High Power device. This device was used for electrical grid applications (first semiconductor based HVDC). During the 70s, the power bipolar transistor module (BJT) and the GTO (both are self commutated switching devices) were invented to satisfy the crescent demand of self commutated devices for chopper and inverters. At the same time, during the 70s the MOSFET appeared. This device made possible compact and efficient converter designs especially at low voltage applications (less than 200V). At the end of the 80s (beginning of 90s) the IGBT was invented as a mixture of voltage controlled devices (MOS) and high current capacity bipolar transistors (BJT). Because of the control simplicity shown by the IGBT, it became the favourite device for low voltage applications. At this time, the GTO became the preferred device for High Power applications. At the end of 90s the IGCT and the High Voltage IGBT were invented, which promote the Medium voltage and High power semiconductor market. Nowadays, both devices and the thyristor are the most suitable devices for High power applications. It could be said that the IGBT is the best choice for Low and Medium power applications (100 kW to 2-3MW), while the IGCT is more suitable for Medium and High power applications (1MW to 100MW). However, the 6.5kV rated IGBT and new

developments with blocking voltage capabilities up to 8kV [RA-06] strive for an extension in the application range of the IGBT, Figure 3-1.

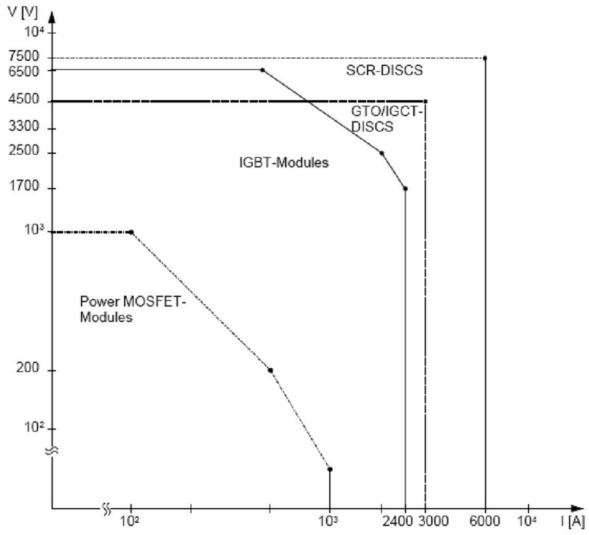


Figure 3-1: Current and Voltage limits of power semiconductors [SE].

In general, controlled Power Semiconductors can be classified in two main groups: Transistors and Thyristors, depending on the way that they react to the control signal, Table 3-1. Appart from those controlled Power Semiconductors, we have the diode that plays an important role in the transient behaviour of the controlled semiconductors.

THYRISTORs Family	TRANSISTORs Family
GTO (Gate Switch-Off Thyristor)	Bipolar Transistor
MCT (MOS-Controlled Thyristor)	MOSFET Transistor
FCTh (Field-Controlled Thyristor)	FCT (Field Controlled Transistor)
SITh (Static Induction Thyristor)	SIT (Static Induction Transistor)
MTO (MOS Switch-Off Thyristor)	IEGT (Injection Enhanced Gate Transistor)
EST (Emitter-Switched Thyristor)	IGBT (Insulated Gate Bipolar Transistor)
ETO (Emitter Switch-Off Thyristor)	
IGTT (Insulated Gate Switch-Off Thyristor)	
IGT (Insulated Gate Thyristor)	
IGCT (Integrated Gate-Commutated Thyristor)	

Table 3-1: Thyristor and Transistor families

Transistors act as amplifiers which can control the collector current and the switching speed by means of the gate terminal. Thyristors however, act as binary current valves where the gate signal has little, if any, influence on the switching speed (defined by external circuits).

Without any doubt, it could be said that the Thyristor, the IGCT and the IGBT have shown their suitability for High Power applications. For high frequency PWM converters self

commutated devices are demanded (IGCT, IGBT, etc). Thyristors can be controlled only while being switched on and therefore, their use is limited to line commutated converters.

3.2 Integrated Gate Commutated Thyristor (IGCT)

The thyristor was the first High Power controllable device, which was used for the first time in 1960 for traction applications and in 1970 for energy transmission applications (First semiconductor based HVDC).

The thyristor is a four silicon layer device ($P^+N^-PN^+$) as shown in Figure 3-2. The outermost layers (N^+ and P^+) are electrically accessible by the Cathode and Anode terminals while the p internal layer is connected to the gate terminal [AL-05].

The thyristor is a unidirectional current device [LI-91]. When the thyristor is forward biased (V_{AK} > 0) there are two possible states for the thyristor, low current-High Voltage off state and high current-low voltage on state. A positive gate current can trigger the change from the forward blocking state to the forward conducting state. However, a negative gate current is not effective to switch off the thyristor due to the high current gains of the internal NPN and PNP transistors, Figure 3-2. In the reverse direction, only the off state is available.

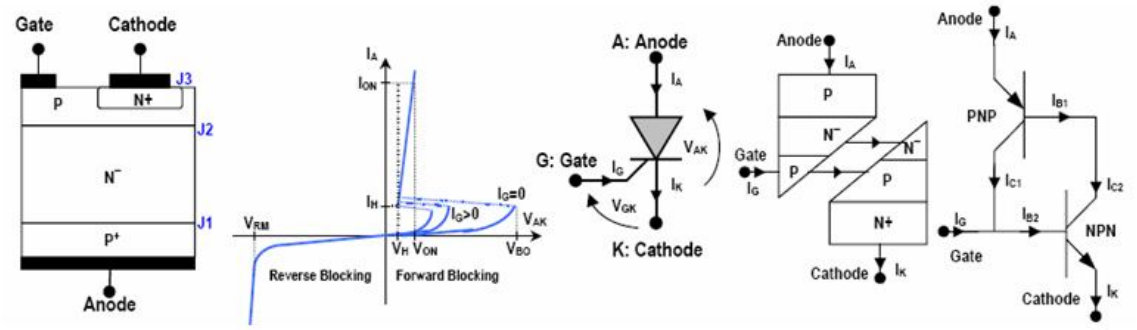


Figure 3-2: Thyristor structure, static characteristic, symbol and internal structure [AL-05].

As part of thyristor family, the GTO has a similar four layer structure ($P^+N^-PN^+$) (Figure 3-2). Therefore, the switch on process is the same than the thyristor switch on process. The main difference between them resides in that the GTO can be switched off if a negative gate voltage is applied at the gate terminal. This characteristic gives a better power control capacity to the GTO. This switch off capacity is achieved minimizing the gate current I_{B2}, which requires a higher gain in the NPN transistor and a lower gain in the PNP transistor, Figure 3-2. In consequence, the gate current is 3-5 times lower than the anode current. However, all the actions taken to obtain a controlled switch off have an adverse effect on the device's switch-on and conduction performance. Consequently, the resultant device is necessarily a compromise of switch-on, conduction and switch-off performance. This trade off requires the use of bulky RCD snubbers to limit the device dV/dt at switch off (typically 1000 V/μs). In fact, the maximum

switch off current of a GTO depends on the chosen snubber capacitance and on the stray inductance in the snubber network. In addition, dI/dt limitation at switch on is required to avoid excessive reverse recovery current on the associated free wheeling fast recovery diode (around 500A/μs).

In general, the switch on process of a GTO is similar to the switch on process of a thyristor, however, the main switching time constraints of GTOs appear especially at switch off. The GTO shows large storage times (≈25μs) before the decrease of the anode current. After the anode current has been extinguished (NPN transistor blocked), there exists a current flowing across the anode and gate terminals. This current is known as tail current and has a notable influence on the switch off losses (it takes place at high anode voltages). The GTO recovers the voltage blocking capacity when the tail current is totally extinguished.

Hard driving principle improves the switch off process of a GTO [WE-01a]. This principle relies on the application of a high gate current slope (dI_G/dt) to allow direct commutation of the total cathode current to the gate. This is done before gate to anode voltage changes. Therefore, the NPN transistor of the four-layer thyristor structure is inactive (Figure 3-2) and the semiconductor is switched off as a three layer switching device (transistor mode switch off).

Fast commutation of the GTO cathode current ($dI_G/dt > 3kA/\mu s$) depends basically on the gate parasitic inductance and the applied voltage. In a standard GTO housing the total gate inductance can be minimised to around 50nH acting over the gate driver and its cabling. In consequence, gate voltages values of 200V are required to achieve the required gate current slope. However, the use of such gate voltages can complicate the gate isolation and can increase the gate driver power supply requirements.

In order to avoid these problems 20V power supply voltage is used. This means that the total gate inductance should be less than 5nH to achieve the required gate current slope. To reach these figure the development of a coaxial GTO was considered and the GCT (Gate controlled Thyristor) concept appeared, which leaded to the minimisation of the inherent gate inductance of the component (around 2nH). Then, the interconnection of the gate driver with the GCT was optimised by using a coaxial printed circuit board configuration, leading to the so-called IGCT (Integrated Gate Controlled Thyristor).

In an IGCT, the maximum switch off current depends on the SOA and no on the external circuitry (snubbers, stray inductances, etc). In addition, due to the very low storage and fall times, the minimum on and off times can be reduced below 10μs (compared to 100μs for GTOs).

Figure 3-3: IGCT families [AL-05].

The transistor mode switch off of the IGCT avoids the need of snubber circuits to control the dV_{AK}/dt during the switch off. In addition, the switch on behaviour is improved and only the free wheeling diode limits the maximum dI_{AK}/dt. Because of its thyristor structure, the IGCT is not able to control the dI_{AK}/dt, therefore, an external inductance is needed to limit the switch on current slope. This snubber requires as well a clamp circuit (RCD) to limit the overvoltage during the switch off, Figure 3-4.

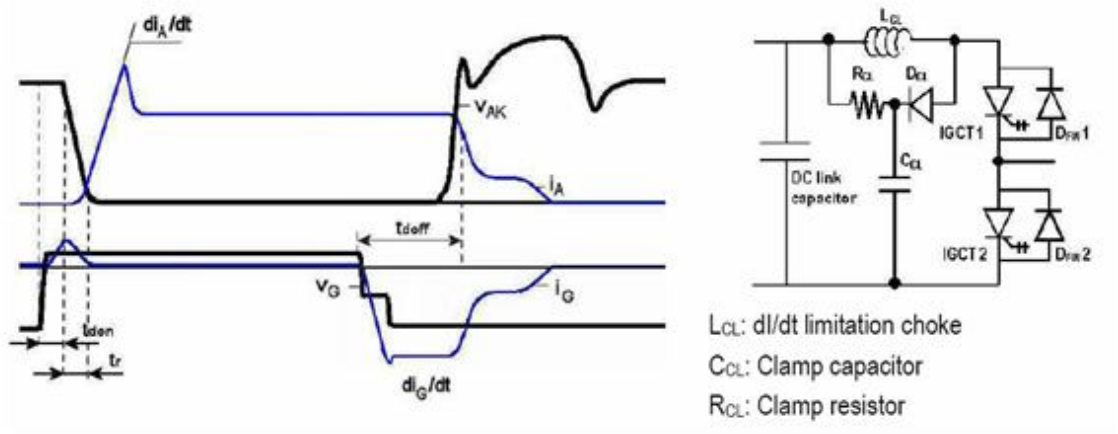


Figure 3-4: Typical switching waveforms of an IGCT. Current Clamp [AL-05].

The hard-drive principle reduces the conduction losses, the switch off losses and the gate current during the on the state [AL-05]. In addition, it allows the integration of an inverse diode in the same wafer without deterioring the device performance.

3.3 Insulated Gate Bipolar Transistor (IGBT)

Until the invention of the MOSFET in the 70s the bipolar transistor was the unique power transistor [BL]. The bipolar transistor needs high base currents and has a relatively slow switch off. In addition, the bipolar transistor has a negative temperature coefficient which increases the risk of thermal runaway. However, the low voltage drop during the on state causes low conduction losses. The MOSFET is a gate voltage controlled device. The gate terminal has high DC impedance and therefore the MOSFET shows lower gate energy requirements than the bipolar transistor. The positive temperature coefficient protects MOSFETs from the thermal runaway and makes them suitable for parallel connection with other MOSFETs.

During the 80s, the IGBT was invented as a combination of MOS and bipolar devices. The IGBT behaves as a bipolar transistor during the on state and during the switching but it is controlled as a MOSFET. This implies that it is able to operate at high currents (BIPOLAR) being easily controlled (MOSFET). It should be noted that it presents tail current at the end of the switch off process. This current increases the switch off losses. In addition the IGBT does not have the free wheeling diode that appears in the MOSFET structure.

The structural design of the IGBT [SE], as well as the MOSFET, consists of a silicon-micro-cellular structure of up to 100.000 cells per cm^2 and 820.000 cells per cm^2 for MOSFETs. These cells are distributed over a chip surface of 0.3..1.5 cm^2, Figure 3-5.

Figure 3-5: IGBT / Diode Chips [SE].

The internal structure of the IGBT is identical to the MOSFET structure including the n^- region, Figure 3-6. The main structural and functional differences are related to the third electrode (p region of the IGBT structure, Figure 3-7).

If enough voltage is applied between control terminals a conduction channel can be generated in the p^+ region close to the gate terminal. Therefore, electrons may be conducted from source or emitter to the n^- area via this channel.

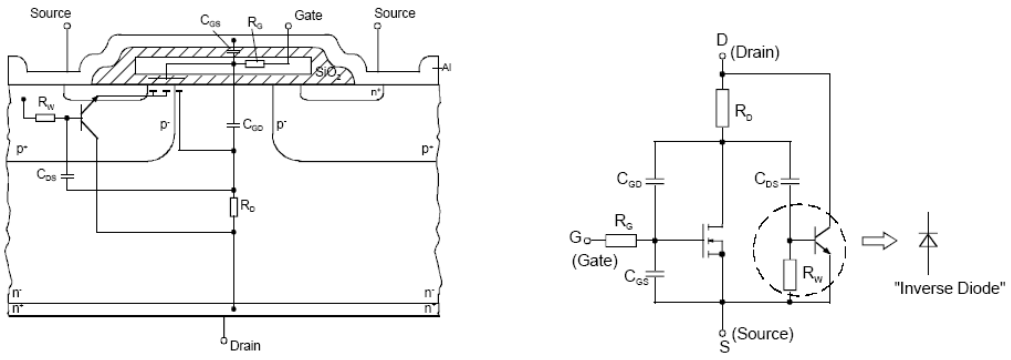


Figure 3-6: MOSFET structure and parasitic elements [SE].

Figure 3-6 shows the internal MOSFET structure and the parasitic components (interelectrode capacitances, channel resistances, reverse diode, etc). It should be noted that the forward voltage drop in a MOSFET depends on the drain current (I_{DS}) as well as on the drain-source resistance ($R_{DS(ON)}$).

$$V_{DS(ON)} = I_{DS} \cdot R_{DS(ON)} \tag{3-1}$$

$$R_{DS(ON)} = k \cdot \left(V_{(BR)DS}\right)^{n} \quad n = 2.4 \ldots 2.6 \tag{3-2}$$

Where k is $8.3e^{-9}$ per cm^2 of chip surface and $V_{(BR)DS}$ is the maximum blocking voltage of the device [SE].

From equation (3-2) it can be deduced that the greater the voltage blocking capacity of the MOSFET, the greater the channel resistance. Therefore, its current handling capacity will be limited in comparison to similar voltage blocking capacity bipolar devices (200..400V).

The MOSFET is a unipolar device (the current is conducted exclusively by electrons). In consequence, there is not any charge storage between different doped regions and in consequence it is possible to switch from one state (conduction or blocking state) to another very quickly. The interelectrode capacitances are the only ones which have influence on the switching dynamics and the needed gate current.

Unlike the MOSFETs, the IGBTs have an additional p^+ region close to the collector terminal (Figure 3-7). After having passed through the n^- region, the electrons enter the p^+ area arranging for positive charge carriers (holes) to be injected from the p^+ region to the n^- region. The injected holes will flow directly from the drift-area to the emitter p contact as well as laterally to the emitter passing the MOS-channel and the n^- well. In this way the n^- drift area will be flooded with charge carriers which are conducting the main current (collector current). This charge enhancement will lead to a space charge reduction and consequently to a reduction of the collector-emitter voltage. Although, compared to the pure ohmic on-state behaviour of the MOSFET the IGBT has an additional threshold voltage at the collector pn-junction layer, the on

state voltage of High Voltage IGBTs is lower than that of MOSFETs because of the enhancement of minority carriers in the highly resistive n^- region. In comparison to MOSFETs, IGBTs may be designed for considerably higher voltages and currents for similar chip surface areas.

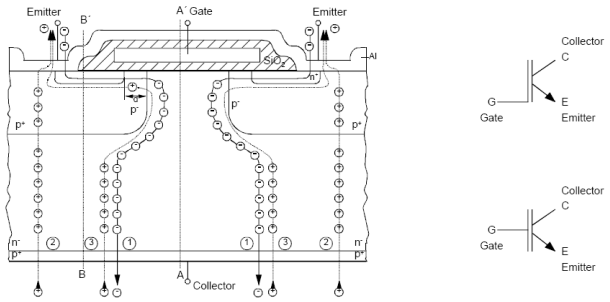


Figure 3-7: IGBT structure [SE].

However, the surplus p storage charge Q_s that has not been extracted during the collector-emitter voltage increase period has to recombine in the n^- region during switch off. This phenomenon causes the tail current which increases the power losses during the IGBT switch off.

Apart from the internal capacitances and resistances, the equivalent circuit of the IGBT shows a parasitic NPN transistor (n^+ / p^+ / n) and a PNP transistor (p^+ / n^- / p^+) which represents a thyristor structure (Figure 3-8). Latch up of this parasitic thyristor may happen basically during on state (when a critical current density is exceeded, which decreases with rising chip temperature) and also during switch off (dynamic latch up due to the increased hole current compared to on state operation), as soon as the required thyristor latch up preconditions are met.

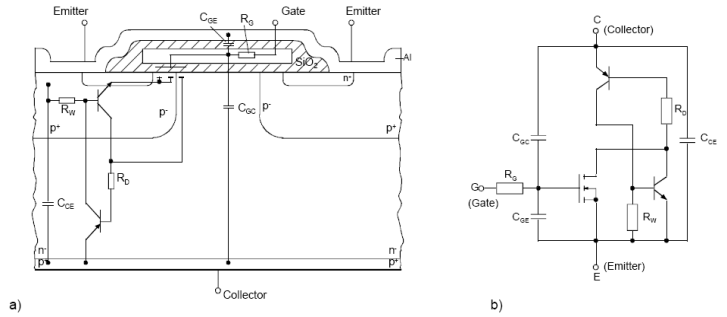


Figure 3-8: IGBT structure with main parasitic elements (a) and equivalent IGBT circuit (b) [SE].

This will lead to a loss of controllability of the IGBT and therefore to its destruction. In order to prevent the latch up, manufacturers make the dynamic switch off current density 15 times higher than the rated current density. In addition, the p^+ region is highly doped to maintain the base voltage of the NPN transistor below its threshold voltage under rated operating conditions.

Generally, the on state, blocking or switching behaviour of an IGBT can be described attending both static and dynamic characteristics.

3.3.1 Static characteristics

The static behaviour of the IGBT is determined by the transfer characteristic and the output characteristic, Figure 3-9.

The transfer characteristic gives the relation between the collector current and the gate voltage when the IGBT operates in its active region. A minimun gate voltage ($V_{GE(th)}$) is required to allow current flow across the IGBT. Once this gate threshold voltage is exceeded the current that can flow across the IGBT is determined by the gate voltage and the transfer characteristic of the IGBT. The transconductance (g_{fs}) is defined as the slope of the transfer characteristic.

However, the output characteristic shows more clearly the relation between the gate current, colector current and colector voltage of the IGBT, Figure 3-9. The first quadrant shows the forward area, where power transistor modules can block High Voltages and switch high currents. Acting on the gate terminal, the IGBT can switch between the blocking state and the on state. When the IGBT is in the blocking state there exists a leakage current which causes power losses in the transistor. During the on state, due to the forward voltage drop (V_{CESAT}) and the load current (I_C), there exist conduction losses in the IGBT.

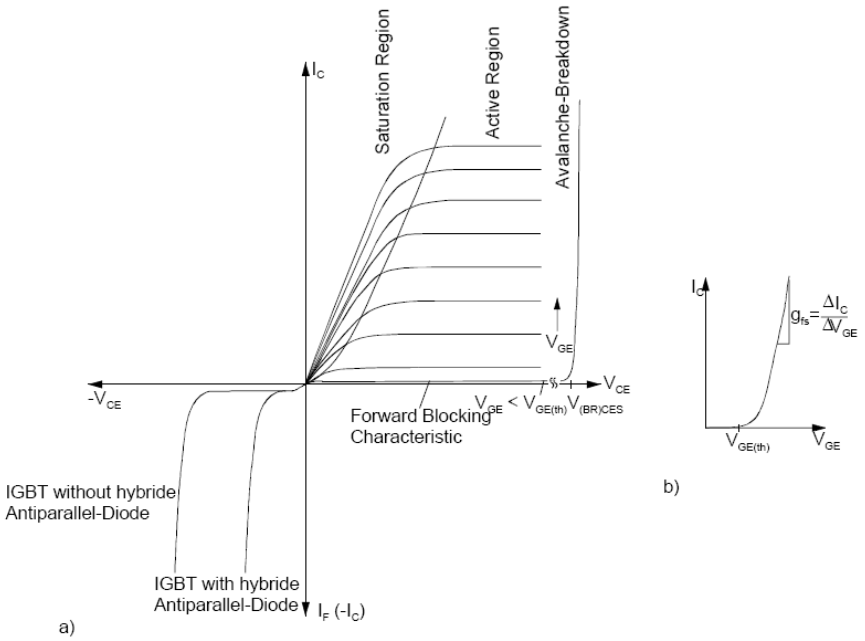


Figure 3-9: Output characteristic (a) and transfer characteristic (b) of the IGBT [SE].

The current-voltage characteristic in the 3rd quadrant of the output characteristic shows the reverse behaviour of power transistor modules in case a negative voltage is applied to the main terminals. This behaviour is determined by the individual characteristics of the transistors

(reverse blocking, reverse conducting) and the features of the diodes within the power module (connected in series or anti parallel to the transistors).

Forward off state

If the collector-emitter voltage (V_{CE}) is positive and the gate voltage is lower than the threshold voltage, the IGBT is in the forward off state. In this situation only a small leakage current (I_{CES}) can flow across the IGBT. The leakage current (I_{CES}) increases slightly when the collector-emitter voltage (V_{CE}) increases. When the maximum collector-emitter voltage is exceeded (V_{CES}) avalanche occurs in the p+/n-/n+ junctions. This voltage is the avalanche breakdown voltage ($V_{(BR)CES}$). As soon as the PNP transistor (p+/n-/n+ junctions) is switched on the avalanche phenomenon causes the failure of the device.

On state

The conduction state of the IGBT can be found in two different regions: The active operation region and the saturation region. In the active operation region, the gate voltage exceeds lightly the gate threshold voltage. The current saturation causes high collector-emitter voltage drop. The collector current can be controlled by means of the gate voltage and the transfer characteristic of the IGBT. The slope of the transfer characteristic (Figure 3-9 (b)) is known as the forward transconductance (g_{fs}) and can be defined as:

$$g_{fs} = {dI_C}/{dV_{GE}} \approx {I_C}/{\left(V_{GE} - V_{GE(th)}\right)} \tag{3-3}$$

In general, the transconductance increases proportionally with the collector current (I_C) and the collector-emitter voltage (V_{CE}) while its value decreases as the operating temperature increases.

The IGBT stay in this region during the switching. The permanent operation in this region leads to high power losses so, the IGBT shouldn't operate in this region permanently.

Saturation region

The saturation region is achieved as soon as the collector current is determined only by the external circuit. This operating region is characterized by the collector-emitter saturation voltage (V_{CESAT}), which depends on the applied gate voltage (V_{GE}), the output characteristic of the IGBT and the collector current (I_C).

Reverse operation

In this operation mode, the pn junction close to the collector terminal is polarized in reverse direction so there is no conductivity. In general, the maximum reverse blocking voltage is only some 10V. If higher reverse blocking voltage capacity is needed a diode must be

connected in series while if reverse conductivity is needed an antiparallel diode must be connected with the IGBT.

3.3.2 Dynamic characteristics

In general, power transistors (MOSFET, IGBT, BJT,…) switch inductive loads with continuous conduction of the current. During the switching, High Voltage levels (V_{CE}) are switched at high current levels (I_C), therefore, high power losses are generated inside the transistor (hard switching), Figure 3-10.

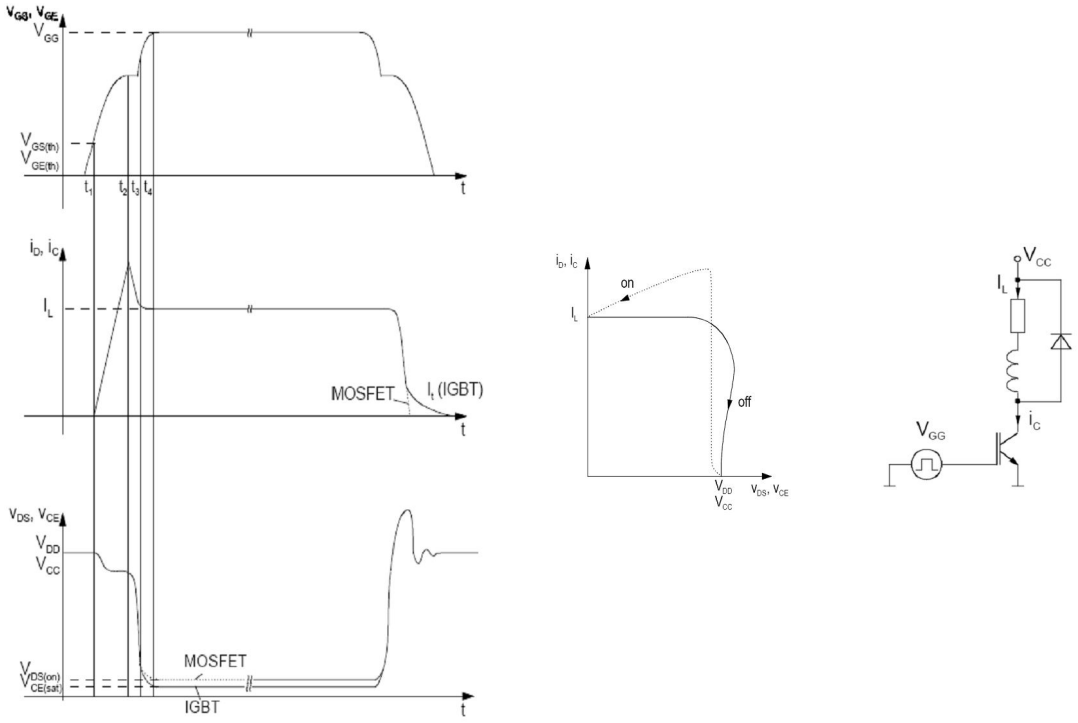


Figure 3-10: Typical hard switching waveforms, switching trajectory and test circuit [SE].

During the switching process, Figure 3-10, the current and voltage waveforms are dependent on the free wheeling diode. When the IGBT is switched on, the free wheeling diode must regain its voltage blocking capacity before the IGBT conducts the load current. Therefore, the IGBT collector current must equal the load current (plus the reverse recovery current of the diode) before the collector-emitter voltage (V_{CE}) begins to fall. When the IGBT is switched off, the free wheeling diode must be forward polarized before the diode can conduct the load current. This happens when the collector-emitter voltage of the IGBT (V_{CE}) exceeds the working voltage after the collector current begins to fall.

When the IGBT is in the on state, the saturation collector-emitter voltage (V_{CESAT}) depends on the collector current and the gate voltage, Figure 3-9. Unlike the MOSFET, which

conducts all drain-source current by means of negative charge carriers (electrons) across the resistive n^- region, the IGBT additionally floods this resistive region with positive charge carriers coming from the p doped region. This mechanism improves the conductivity of the resistive region maintaining the saturation voltage (V_{CESAT}) at relatively low levels even for High Voltage blocking capacity devices.

At the end of the switch off process, there exist some positive charge carriers (holes) in the resistive n^- region injected by the p doped region of the IGBT. The recombination process of those holes cause the tail current of the IGBT and additional switch off losses in the IGBT. Because of the MOSFET is a unipolar device (current is transported exclusively by electrons) there is not any tail current in the switch off characteristic of a MOSFET.

In general, the switching behaviour of the IGBT is determined by the interelectrode capacitances and the internal resistors that figure in the IGBT structure, Figure 3-8. During the switching process these capacitances must be charged/discharged and in consequence there is a power demand to control the voltage of the gate terminal. This power demand depends on the switching frequency (f_{sw}), the amount of injected/extracted gate charges (Q_G) and the driver output voltage (V_{CC}), equation (3-4).

$$P_{GATE} = V_{cc} \cdot Q_G \cdot f_{sw} \tag{3-4}$$

Usually, IGBTs are driven by a gate driver that applies a voltage at the gate terminal. The gate current is limited by means of a gate resistor. The applied gate voltage and the gate resistance (internal plus external) determine the charge extraction / injection speed from / to the interelectrode capacitances of the IGBT. This charge injection / extraction speed determines the switching speed and consequently the switching losses of the IGBT. Therefore, it is possible to limit the current slope (dI_C/dt) during the switch on as well as the voltage slope (dV_{CE}/dt) during the switch off if the gate voltage (V_{GE}) and the gate resistor are properly chosen. Stray inductances have important effects on the switching process causing oscillations and over voltages.

Assuming the IGBT model shown in Figure 3-8, the considered interelectrode capacitances during the switching process are three: The gate-emitter capacitance (C_{GE}), the collector-emitter capacitance (C_{CE}) and the gate collector capacitance (C_{GC}). This last capacitance (C_{GC}) is the one known as Miller capacitance because of it is which causes the Miller effect during the switching process of the IGBT. When the IGBT is in the blocking state, the Miller capacitance value is low and similar to the collector-emitter capacitance (C_{CE}). During the on state, the Miller capacitance has a higher value due to the polarity inversion in the gate region when the gate voltage exceeds the collector-emitter voltage (V_{CE}). During the switching process the value of the effective C_{GC} capacitance changes dynamically (increases abruptly) due to the Miller effect (3-5).

$$C_{GCdyn} = C_{GC} \cdot \left(1 - {dV_{CE}}/{dV_{GE}}\right) \tag{3-5}$$

The device manufacturers provide the value of those capacitances as a function of the collector-emitter voltage for a given zero gate voltage while the IGBT is excited with 1 MHz signal. These capacitances are given as the input capacitance (C_{iss}), output capacitance (C_{oss}) and the reverse transfer capacitance (C_{rss}).

$$C_{iss} = C_{GE} + C_{GC} \tag{3-6}$$

$$C_{oss} = C_{CE} + C_{GC} \tag{3-7}$$

$$C_{rss} = C_{GC} \tag{3-8}$$

However, it should be noted that the input capacitance (C_{iss}) and mainly the reverse transfer capacitance (C_{rss}) increase their values when the IGBT is switched on ($V_{CE} < V_{GE}$). This data is not reflected in the data provided by the manufacturer [SE]. In addition, the value of these capacitances does not consider the Miller effect, which implies that the shown data does not reflect the real charge requirements of the gate terminal.

In order to shown the real gate charge requirements the manufacturers provide a plot to understand the relation between the switching times, the collector-emitter (V_{CE}) voltage and the collector current (I_C). This plot is known as the gate charge plot, Figure 3-11 and Figure 3-12.

This charge plot shows the gate voltage evolution as a function of the injected / extracted charge during the switching process. Therefore, the duration of each time interval (Figure 3-11) can be calculated by the following equation:

$$i_G = {dQ_G}/{dt} \tag{3-9}$$

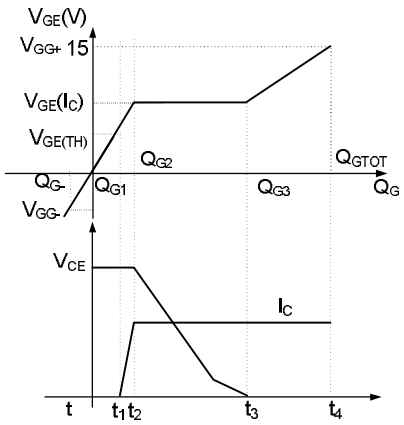


Figure 3-11: Gate voltage (V_{GE}) as a function of the gate charge (Q_G) during the switching.

Figure 3-11 shows the typical switching waveforms (V_{CE}, I_C and V_{GE}) of the IGBT. As it can be seen, the switching process can be divided in different time intervals (t_0-t_1, t_1-t_2, t_2-t_3, t_3-t_4) in which different IGBT behaviours could be found during the switching process (delay, dI_C/dt, dV_{CE}/dt, etc). Similarly, each time interval is related to a determined charge state (Q_G).

The switch on process begins when the gate driver changes the gate voltage from being negative (V_{GG-}) to being positive (V_{GG+}). At the first instant, the gate terminal is fully charged at Q_{G-}. In these conditions, the driver injects current to the gate terminal, changing in this way the gate charge state of the input capacitance and therefore the gate voltage. Since the gate voltage is lower than the gate threshold voltage of the IGBT ($V_{GE(th)}$), there is not any current flowing across the IGBT (interval t_0-t_1).

At the first t_1 time instant, the gate voltage reaches the gate threshold voltage ($V_{GE(th)}$). To achieve this gate voltage an amount of Q_{G1} charge must be injected by the gate driver. Starting from this time instant, the collector current begins growing until the load current level (the reverse recovery current is not considered) is reached at a t_2 time instant. The gate voltage increase is determined by the collector current and the transfer characteristic of the IGBT. Because the diode remains conductor until the t_2 time instant, the collector emitter voltage does not decrease until the t_2 time instant. At this instant, a Q_{G2} amount of charge has been injected by the driver.

In the t_2 – t_3 time interval, the free wheeling diode is switched off and the collector-emitter voltage (V_{CE}) begins to fall. During this time interval, the collector current and the gate voltage are still coupled by the transfer characteristic of the IGBT, so, assuming a constant collector current, the gate voltage (V_{GE}) remains constant. As the collector-emitter voltage falls, the Miller capacitance (C_{GC}) is charged by the gate current. As it can be seen, the collector-emitter voltage shows two different slopes due to the steep change in the Miller capacitance. This change happens when the gate region polarity is inverted because the gate voltage exceeds the collector-emitter voltage. The amount of injected charge during this time interval is ($Q_{G3} – Q_{G2}$).

At the t_3 time instant, the IGBT is considered to be switched on. In this state, the IGBT does not operate in the active operating region (Figure 3-9) and operates in the saturation region. In this region the collector current (I_C) and the gate voltage (V_{GE}) are not coupled by the transfer characteristic of the IGBT. The excess of injected charge at this moment increases the gate voltage at V_{GG} (output voltage of the gate driver). This gate voltage reduces the collector-emitter voltage drop (V_{CESAT}) for a given collector current (I_C) as shown by the output characteristic of the IGBT. In general, the amount of injected charge (Q_{GTOT}) to the gate terminal increases as the working voltage of the IGBT increases, Figure 3-12.

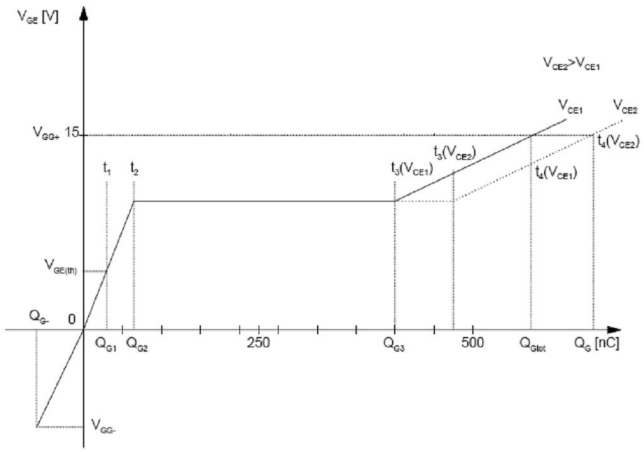


Figure 3-12: Gate charge plot [SE].

During the switching off, the described process is executed in the inverse order. The amount of injected charge during the switch on process (Q_{GTOT}) must be removed from the gate terminal. In consequence, the gate terminal starts the switching process with a positive gate voltage (V_{GG+}) and the gate current reduces the charge state of the gate terminal (Q_G). Each charge state is related to a different IGBT behaviour (dV_{CE}/dt, dI_C/dt, delay, etc) as described above.

3.4 Advantages of the IGBT for the series connection

The current and voltage limits of actual semiconductors, Figure 3-1, show that for switched power applications at Medium voltage the IGBT and the IGCT are the best suited devices. For a wide application range both devices can be suitable. The election between either one depends on criterions as reliability, robustness, market availability and cost. However, as a reference, it is possible to establish some power ranges in which the IGBT or IGCT are the chosen switching devices (Figure 3-13).

Low voltage IGBT modules (LVIGBT module) cover a wide application range for working voltages lower than 690 volts and some MVAs applications. The High Voltage IGBT module (HVIGBT module) is the preferred choice for application voltages from 1 kV to 7.2 kV and some MVAs. For power ranges from 5MVA to 100MVA and working voltages below 15 kV the IGCTs dominate the market. However, when the working voltage increases and the series connection of a high number of switching devices are required the IGBT press pack is probably the most suitable switching device.

In energy transmission and distribution applications, as well as drive applications, an important criterion for device selection is the availability of the device at the required voltage range. In spite of 8 kV IGBTs and IGCTs [RA-06] having been investigated and 10 kV semiconductors

being expected [BE-03] in the near future, there are some applications where these voltage blocking capacities are not enough to meet the requirements of the application. In High Voltage applications (for example HVDCs), the need of High Voltage switching valves makes compulsory the series connection of power devices. In this kind of applications, due to the reduced energy requirements of the gate terminal and its ability to control the switching dynamics by the gate terminal, the IGBT is the chosen device for the series connection [LI-03].

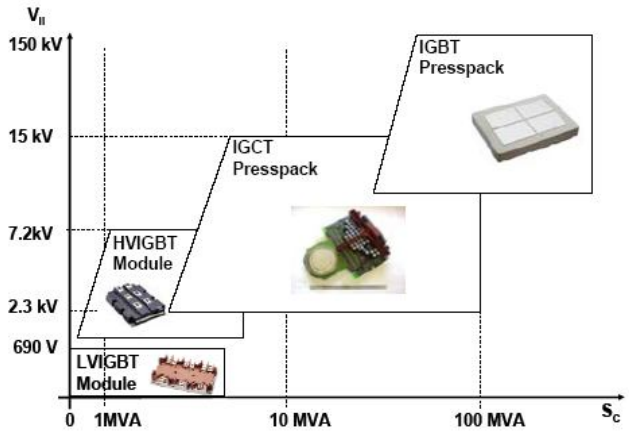


Figure 3-13: Power devices application range.

In contrast to the IGBT, the IGCT has the ability to switch higher current and voltages (wider SOA) than the IGBT. The conduction losses are also lower than the ones of the IGBT for a given operating current. The double side cooling of the IGCT gives a bigger capacity to extract the generated heat than the IGBT module. However, nowadays there are several commercially available IGBT presspacks so this is not a real advantage of the IGCT with respect to the IGBT. The IGCTs thermal cycling endurance is relatively high thanks to the simple press pack technology where the thermal and electrical contacts between the internal elements require high compressing forces. This force limits the eventual deformation of the contacts. In addition, the IGCT has a high I^2t which increases the reliability in failure situations. However, it is not possible to detect any failure by means of the driver of the IGCT.

On the other hand, the gate energy requirements of the IGBT are considerably lower than the gate energy requirements of the IGCT. This simplifies the integration of the power supply in the IGBT gate driver while the IGCT driver needs an external power supply. When several devices are connected in series this has an important influence on the final cost. This is an inconvenient of the IGCT when some devices are connected in series. In addition, the thyristor structure of the IGCT does not allow the control of the switching dynamics by means of the gate terminal. In consequence, when IGCTs are connected in series the use of snubber networks is compulsory to achieve a proper voltage balance [NA-00], [NA-01]. These networks increase the overall power losses of the converter decreasing the efficiency of the system.

The IGBT switching process can be controlled by means of the gate terminal, therefore, it should be possible to balance the voltage of series connected IGBTs without using bulky and lossy snubber networks. This is an advantage of the IGBT when several devices are connected in series. The amount of gate control techniques of the IGBT are known as active gate control methods. Therefore, this PhD research work will be mainly focused on the study of **active gate control methods** to achieve a proper **voltage balance** between **series connected IGBTs**.

Part 2: THE IGBT: MODELLING AND DRIVING MODES

4 Behavioural Model of the IGBT

This chapter shows a simple IGBT model and its parametrization. Therefore, section 4.1 contains a brief State of the Art of different IGBT models. Section 4.2 describes which characteristics are considered for the IGBT model. In Sections 4.3 and 4.4 both static and dynamic characteristics of the IGBT are modelled while section 4.5 is focused on the parameter extraction procedure. Finally, section 4.6 compares simulation results with experimental measurements in order to validate the proposed IGBT model.

4.1 State of the art of IGBT models

The IGBT has become one of the most widely used power blocks in real power systems. The IGBT presents high current handling capability, maintaining a good trade off between switching losses and conduction losses. In addition, over current can be detected by monitoring the collector-emitter voltage and therefore the gate driver can act to protect the IGBT. The switching speed of the IGBT can be controlled by means of the gate terminal. This gate terminal presents high DC-impedance and therefore low energy is needed to maintain the IGBT in on state or off state.

Nowadays, there are many IGBTs commercially available with current and voltage ratings up to 6.5kV / 600A [EU-02] and 4.5kV / 2.4kA [WE-05]. These IGBTs meet the needs of applications like Medium Voltage drives, Active Var controllers or even HVDCs.

IGBT models are needed to understand and predict the behaviour of the power module and to optimize the design of the power converter for a suitable operation. Although an accurate IGBT model classification is made in [SH-00], in general it could be said that there are two main types of semiconductor models, semiconductor physic based models and behavioural or compact models [MO-02].

Physic based semiconductor models [MO-02], [LA-01], [HE-91], [LA] describe the electric carrier behaviour and the effects of the temperature on this behaviour. The best description of the internal carrier transport mechanisms of the IGBT is achieved with these models and therefore high accuracy can be obtained. However, the complexity of the equations can make the simulation very time consuming and convergence problems can arise when these complex equations are solved. In addition, the parametrization of physic based models can be a difficult task which requires knowledge of semiconductor physics. Therefore, these type of models are more suitable for power semiconductor device manufacturers than for application engineers.

In [LA-01], a good approach is proposed in order to obtain an easy to parameterize and reasonably accurate IGBT model. The internal BJT of the IGBT is modelled with physically

based equations while the internal MOSFET of the IGBT is modelled with empirical equations. One of the main drawbacks of this approach is that the parameter extraction procedure is not described in detail. In addition, the physically based equations make the model difficult to understand or modify for application engineers if some change is needed in the model.

Behavioural models [CO-95], [BO-01], [TI-00], [HS-95] make the approach of the electrical behaviour of the device without considering semiconductor physics. Although not all switching phenomena are described, a reasonably accurate static and dynamic performance can be achieved with behavioural models. In general, the features of the device are approached with curve fitting methods. The needed data for the parametrization can be obtained from the data sheets provided by the manufacturer or from experimental measurements.

These type of models are the preferred choice when simplicity of model synthesis and parametrization are needed. These features make behavioural models suitable for application engineers.

Behavioural IGBT models are less accurate than physics-based models over wide ranges of operating conditions [HS-95]. However, a good trade off can be achieved for certain well known operating conditions between simulation time and accuracy using behavioural IGBT models. In [HS-95], satisfactory simulation results are obtained in terms of output current and voltage waveforms and needed CPU time. However, a physics-based IGBT model is used for extracting the needed model parameters. The described parametrization procedure can be complex if measurements have to be obtained experimentally from physical IGBT devices.

An IGBT model should present a good trade off between convergence, simulation time, accuracy, simplicity and comprehensibility. In addition, the model should be parameterized with an easy parameter extraction procedure. In general, the static characteristics can be approached easily and precisely with curve fitting methods. However, it is not easy to find an easy parameter extraction procedure for the dynamic model of the IGBT.

For this reason, a simple behavioural model of the IGBT is presented in this section. The parametrization of the static characteristics of the IGBT is based on curve fitting methods. Most of the needed parameters and curves are available in the data sheets. Parameters related to the dynamic model can be extracted from experimental measurements. The parameter extraction procedure described in this chapter is aimed to be as simple as possible.

The IGBT chosen to be modelled is the BSM200GB60DLC IGBT module (Eupec). The optimization routine for static curves is implemented in MATLAB and simulations have been carried out in SABER. Simulation results are compared with experimental measurements in order to validate the model.

4.2 Considered characteristics in the IGBT model

The current that can flow across an IGBT (collector-emitter current) is controlled by the applied gate voltage (V_{GE}). If the gate voltage (V_{CGE}) is lower than the gate threshold voltage there is not any collector-emitter current flowing across the IGBT. Only a small leakage current can be measured at the collector-emitter terminals. If the applied gate voltage exceeds the gate threshold voltage, a collector-emitter current can flow across the IGBT. In general, the relation between gate voltage, collector-emitter voltage and collector-emitter current is determined by the output characteristic of the IGBT. When the IGBT operates in the active region, the gate voltage and the transfer characteristic determine the collector-emitter current at any collector-emitter voltage. If the IGBT operates in the saturation region, the collector-emitter voltage is determined by the collector-emitter current and the gate voltage. During the switching, a gate current is injected to / extracted from the gate terminal. This current is mainly limited by the gate resistor and the applied gate voltage. This gate current charges / discharges the interelectrode capacitances during the switching and therefore, determines the switching speed of the IGBT.

In order to achieve a similar behaviour, the IGBT model shown in Figure 4-1, considers the static characteristics (transfer characteristic and output characteristic), the non linear interelectrode capacitances (C_{GC}, C_{GE}, C_{CE}), the internal gate resistor (Rg) and the leakage current (modelled as a resistor, R_{CE}). This model doesn't consider the tail current of the IGBT during the switch off.

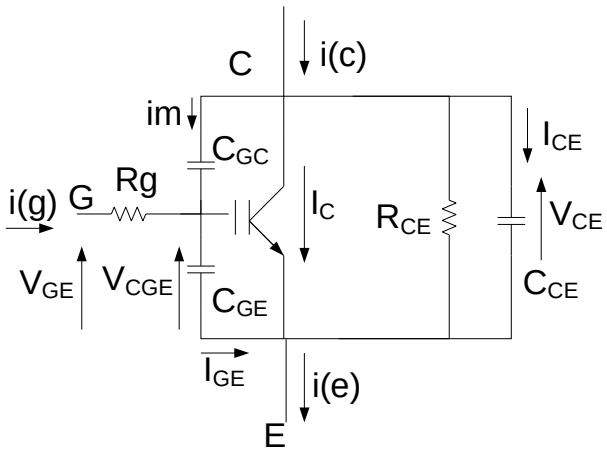


Figure 4-1: Considered IGBT model

4.3 Static Characteristics model

As shown in chapter 3.3.1, the main static characteristics of the IGBT are two: the transfer characteristic and the output characteristic. In Section 4.3.1 the transfer characteristic is modelled while in section 4.3.2 the output characteristic of the IGBT is modelled.

4.3.1 Transfer characteristic of the IGBT

The gate voltage determines the collector current ($I_C = f(V_{CGE})$) when the IGBT is working in the active region ($V_{CE} >> V_{CESAT}$ and $V_{CGE} > V_{GE(th)}$). The transfer characteristic gives the relation between the collector current (I_C) and the gate voltage (V_{CGE}). Typically this curve is given at 25ºC and 125ºC and can be approached with a quadratic function.

$$I_{CGE} = k \cdot \left(V_{CGE} - V_{GE(th)}\right)^2 \quad V_{CGE} \geq V_{GE(th)} \tag{4-1}$$

Where $V_{GE(th)}$ is the gate threshold voltage and k is a curve fitting parameter.

Both parameters are temperature dependent and can be expressed by the following equations:

$$V_{GE(th)} = v_{th25^o} \cdot \left(1 + \alpha_{GE(th)} \cdot \left(T_j - 25^o\right)\right) \tag{4-2}$$

$$k = k_{25^o} \cdot \left(1 + \alpha_k \cdot \left(T_j - 25^o\right)\right) \tag{4-3}$$

$\alpha_{GE(th)}$ and α_k are the temperature coefficients of k and $V_{GE(th)}$ respectively.

Figure 4-2 shows the modelled transfer characteristic and the transfer characteristic obtained from the data sheet. The obtained transfer characteristics closely match the actual measurements.

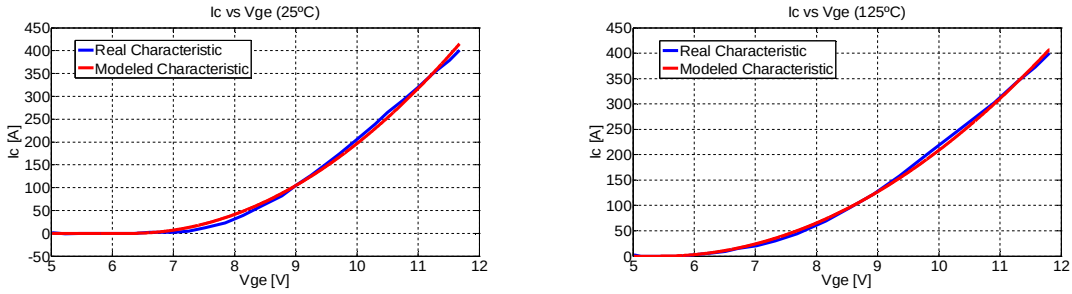


Figure 4-2: Transfer characteristics of the BSM200GB60DLC IGBT module at 25ºC and 125ºC.

4.3.2 Output characteristic of the IGBT

The output characteristic of the IGBT determines the relation between the collector current (I_C), the gate-emitter voltage (V_{CGE}) and the collector-emitter (V_{CE}) voltage ($I_C = f(V_{CE},V_{CGE})$), Figure 4-3. Three main operating regions can be found in the output characteristic of the IGBT: saturation region (during the on state), cut off region (during the off state) and active operation region (during the switching).

When the gate voltage (V_{CGE}) is lower than the gate threshold voltage ($V_{GE(th)}$), the IGBT is in the cut off region and therefore, there is no current (I_C) flowing across the IGBT. During the switching process, the gate voltage (V_{CGE}) is larger than the gate threshold voltage ($V_{GE(th)}$) and therefore a collector current can flow across the IGBT.

While the collector-emitter (V_{CE}) voltage is significantly larger than the saturation voltage, the IGBT operates in its active region. In this region, the collector current is controlled by the gate voltage of the IGBT as shown in equation (4-1). In the saturation region, the collector current is equal to the load current. The collector-emitter voltage (V_{CESAT}) depends on the collector current and the applied gate voltage.

The output characteristic of the IGBT is usually provided by the manufacturer. The switching trajectory over this characteristic depends on the load. The commutation process waveforms are dependent on this switching trajectory. This output characteristic can be approached by the following equation:

$$I_C = I_{CGE} \cdot \Delta I \cdot \left(\tanh\left(\left(v_{CE} - v_P \right) / v_S \right) + V_{CE0} \right) \tag{4-4}$$

The collector current (4-4) depends on the collector-emitter voltage (V_{CE}) and the gate voltage controlled conductance (4-1). Curve fitting parameters (V_p, V_s, V_{CE0}, ΔI, α_{vp}, etc.) are needed to adjust the curve over the V_{CE} axis. Those curve fitting parameters can be expressed with the following equations:

$$V_{CE0} = 1 - 2 \cdot \frac{e^{(v_{ceth} - vp)/vs}}{e^{(v_{ceth} - vp)/vs} + e^{-(v_{ceth} + vp)/vs}} \tag{4-5}$$

$$\Delta I = \Delta I_{test} \cdot \left(1 + \alpha_{AI} \cdot \left(V_{CGE} - V_{ge\_test}\right)\right) \tag{4-6}$$

$$vp = vp_{test} \cdot \left(1 + \alpha_{vp} \cdot \left(V_{CGE} - V_{ge\_test}\right)\right) \tag{4-7}$$

$$vs = \alpha_{vs} \cdot \left(V_{CGE} - V_{GE(th)}\right) \tag{4-8}$$

V_{ge_test} is the gate voltage at which the curves are fitted and V_{ceth} is the minimum collector-emitter voltage drop at which collector current can flow.

Figure 4-3 compares the modelled output characteristic with the data sheet characteristic for V_{GE} = 8 V, V_{GE} = 10 V, V_{GE} = 12 V and V_{GE} = 15 V. Figure 4-3 shows that the obtained output characteristics closely match the actual measurements.

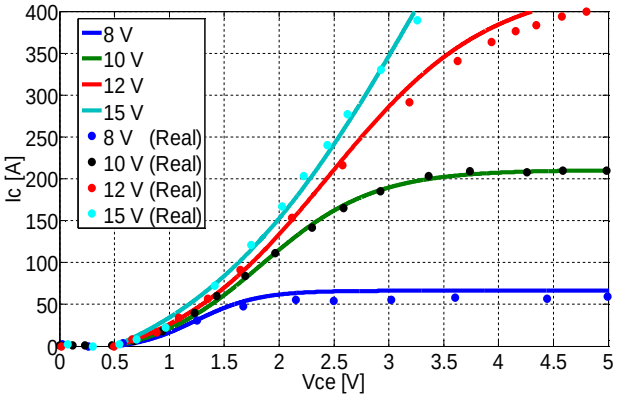


Figure 4-3: Output characteristic of the BSM200GB60DLC IGBT module

4.4 Dynamic characteristics model

The dynamic behaviour of the IGBT depends mainly on the currents which charge / discharge the interelectrode capacitances during the switching process. Section 4.4.1 describes this charging and discharging process. As detailed in section 3.3.2, the interelectrode capacitances depends mainly on the colector-emitter voltage. In order to simplify the dynamic model and its parametrization section 4.4.2 shows the considered simplifications for the interelectrode capacitances.

4.4.1 Dynamic characteristic of the IGBT

The dynamic behaviour of the IGBT is determined mainly by the currents that charge / discharge the interelectrode capacitances of the IGBT during the switching. The dynamic characteristic of the IGBT describes this charge / discharge process during the switching. In addition, this model calculates the collector current (i(c)), the emitter current (i(e)) and the gate current (i(g)) of the IGBT, Figure 4-1. These currents are needed to know how the IGBT interacts with the external circuit during its operation.

Applying Kirchhoff's laws to the IGBT model shown in Figure 4-1, the following dynamic model could be obtained:

$$I_G = \frac{v_{GE} - v_{CGE}}{Rg} \tag{4-9}$$

$$V_{CE} = V_{CGE} + V_{CGC} \tag{4-10}$$

$$im + I_G = I_{GE} \tag{4-11}$$

$$im = C_{GC} \cdot \frac{dv_{CGC}}{dt} \tag{4-12}$$

$$I_{GE} = C_{GE} \cdot \frac{dv_{CGE}}{dt} \tag{4-13}$$

$$I_{CE} = C_{CE} \cdot \frac{dv_{CE}}{dt} \tag{4-14}$$

$$i(c) = I_C + \frac{v_{CE}}{R_{CE}} + i_m + I_{CE} \tag{4-15}$$

$$i(e) = I_C + \frac{v_{CE}}{R_{CE}} + I_{GE} + I_{CE} \tag{4-16}$$

4.4.2 Interelectrode capacitances of the IGBT

As shown in Figure 4-1, three main capacitances are considered in this model (C_{GC}, C_{GE} and C_{CE}). These capacitances determine the switching behaviour of the IGBT (4-12), (4-13) and (4-14).

Usually, manufacturers provide a plot with the values of these capacitances as the input capacitance (C_{iss}), output capacitance (C_{oss}) and the reverse transfer capacitance (C_{rss}) for a zero gate voltage. The needed C_{GE}, C_{GC} and C_{CE} capacitance values can be deduced from the following equations:

$$C_{iss} = C_{GE} + C_{GC} \tag{4-17}$$

$$C_{rss} = C_{GC} \tag{4-18}$$

$$C_{oss} = C_{GC} + C_{CE} \tag{4-19}$$

The value of these capacitances is strongly dependent on the colector-emitter voltage and its value decreases as far the colector-emitter increases [GR-08]:

$$C_{xx}(V_{CE}) = \frac{A}{\sqrt{V_{CE} - V_{GE}}} \tag{4-20}$$

Where A is curve fitting coeficient, V_{CE} is the colector-emitter voltage and V_{GE} is the gate-emitter voltage.

In order to simplify both the IGBT model and its parametrization, this model considers that the interlectrodic capacitances can get discrete values depending on the colector-emitter voltage, Figure 4-4.

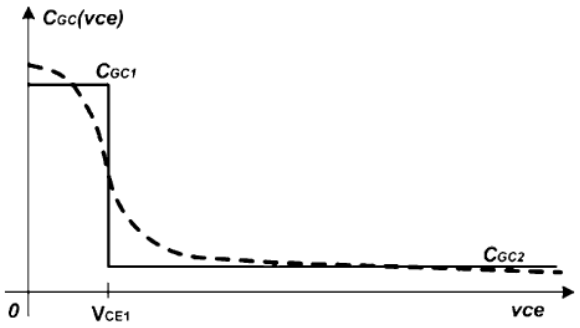


Figure 4-4: Interelectrodic capacitance value versus collector-emitter voltage. Real value (discontinue line) and modelled value (continue line) [GR-08].

Therefore, the interelectrode capacitance values can be expressed with the following equations:

$$C_{rss} = C_{rssf} \quad \text{if}\left(V_{CE} > \text{value}\right) \quad \text{else}\, C_{rss0} \tag{4-21}$$

$$C_{iss} = C_{issf} \quad \text{if}\left(V_{CE} > \text{value}\right) \quad \text{else}\, C_{iss0} \tag{4-22}$$

$$C_{oss} = C_{ossf} \quad \text{if}\left(V_{CE} > \text{value}\right) \quad \text{else}\, C_{oss0} \tag{4-23}$$

It should be taken into account that the values provided by the datasheets are given for a zero gate voltage. The value of these capacitances is substantially larger when the IGBT is active [JO-01]. Another aspect that is not usually included in IGBT models but has significant effects on the transient gate voltage waveforms is the large input capacitance variation for negative gate bias [SH-00]. Equations (4-21), (4-22) and (4-23) can be modified to consider the effect of the gate voltage on the value of these capacitances.

Since there is not any description of the evolution of these capacitances available in datasheets, these values have to be estimated with the help of experimental measurements. Although a more accurate parameter optimization can be done with identification methods like [SC-06], in the next section an easy parameter extraction procedure is described based on experimental measurements.

4.5 Parameter extraction procedure

As shown by equations (4-1), (4-12)-(4-14), the dynamic behaviour of the IGBT during the switching process depends on the gate current and the interelectrode capacitances. The gate current is limited by the external gate resistor (placed in the gate driver) as well as the internal gate resistor placed inside the IGBT module. The values of the interelectrode capacitances as well as the internal gate resistor are usually poorly specified by the

manufacturers. For this reason, some experimental measurements are needed for their proper parametrization.

In this section a simple method is described to estimate the value of interelectrode capacitances (4.5.2) as well as the value of the internal gate resistor (4.5.1).

4.5.1 Estimation of interelectrode capacitances

In the extraction procedure of the interelectrode capacitances a constant current is injected to / extracted from the gate terminal. The switching process is divided in several time intervals where a collector-emitter voltage slope (dV_{CE}/dt) or a gate voltage slope (dV_{GE}/dt) can be measured, Figure 4-5. The gate current has low amplitude in order to achieve a slow speed switching and in consequence each time interval can be easily identified. If the voltage slope and the gate current are known in each section, the value of the input capacitance for each time interval can be estimated.

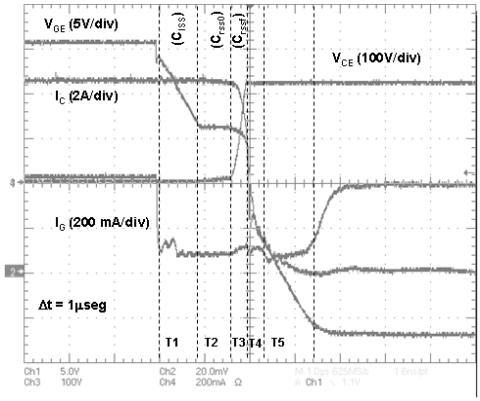


Figure 4-5: Switch off process and time intervals

During the T2 time interval (Figure 4-5) a collector-emitter voltage slope (dV_{CE}/dt) can be measured. During this time interval colector-emitter voltage is lower than the gate voltage and due to reverse polarization close to the n doped gate side region, the C_{GC} capacitance shows a big value. Due to the Miller effect, the gate voltage (V_{CGE}) remains almost constant. During the T3 time interval colector-emitter voltage exceeds the gate voltage. This decreases the value of the C_{GC} capacitance. During this time interval the gate voltage should be constant, however as shown in Figure 4-5, during the switching process the gate voltage changes. This phenomenon is caused by the dependence of the transfer characteristic of the IGBT on the colector-emitter voltage. Therefore, for a given colector current, the gate voltage (coupled with I_C by means of the transfer characteristic) changes as the colector-emitter voltage increases. This behaviour has not been considered in the proposed model, so the simulated gate voltage should be maintained constant during this time interval (assuming a constant colector current). Therefore, assuming that $dV_{CGE}/dt \approx 0$ during T2 and T3 time intervals the following relation can be found:

$$\frac{dv_{CE}}{dt} \approx \frac{dv_{CGC}}{dt} \tag{4-24}$$

In addition, according to (4-11), the gate current i(g) is equal to the current (im) that flows across the reverse transfer capacitance (C_{GC}):

$$I_G \approx -im \tag{4-25}$$

In consequence, when applying (4-12) it is possible to find a value for the Miller capacitance to be applied in those time intervals (C_{rss0} and C_{rssf}). Due to the C_{GC} capacitance change, it can be seen that at low collector-emitter voltages (interval T2) the collector-emitter voltage slope (dV_{CE}/dt) is lower than the collector-emitter voltage slope at high collector-emitter voltages (interval T3) for the same gate current, Figure 4-5.

During the T1 time interval the gate current charges the input capacitance (C_{iss}). This capacitance is the addition of the gate emitter capacitance (C_{GE}) and the gate collector capacitance ($C_{GC} = C_{rss}$). Applying the same method it is possible to find a value for C_{iss0}. Since C_{GC} (C_{rss}) has been estimated previously the value of C_{GE} can be calculated (4-22). During the T4 time interval the gate input capacitance (C_{issf}) is discharged by a constant gate current. The collector-emitter voltage (V_{CE}) is almost constant during this interval and therefore the Miller effect can be neglected. In addition, in this time interval the value of the reverse transfer capacitance (C_{rssf}) should be very small due to the High Voltage level. In consequence, with the gate voltage slope and the gate current the value of C_{issf} can be estimated. The same process can be applied to obtain a value for the input capacitance (C_{issf}) when the gate terminal is inversely biased (interval T5).

$$I_G = C_{iss0} \cdot \frac{dv_{CGE}}{dt} \tag{4-26}$$

The output capacitance (C_{oss}) of the IGBT can be estimated measuring the dV_{CE}/dt during the switch off at different gate currents and low collector currents. In general, the switch off speed (dV_{CE}/dt) is controlled by the gate current. If a large enough collector current is flowing across the IGBT the voltage slope of V_{CE} is determined by the gate current (4-12). However, if a low amplitude collector current is switched off the IGBT can be switched off before the collector-emitter voltage begins to rise. In this situation, the voltage slope is limited mainly by the collector current and the collector emitter capacitance.

Therefore, referring to (4-15), the current that flows across the IGBT (I_C) is zero and the leakage current is neglected. As shown in Figure 4-6, the gate current discharges the input capacitance ($C_{GE} + C_{rss}$). Due to that the gate emitter capacitance is substantially larger than the Miller capacitance ($C_{GE} > C_{rssf}$) only a little current (im) flows across the reverse transfer

capacitance during the voltage slope in this time interval (behaviour according to the proposed model). Therefore, the following can be assumed to estimate the C_{CE} capacitance value:

$$i(c) \approx C_{CE} \cdot \frac{dv_{CE}}{dt} \tag{4-27}$$

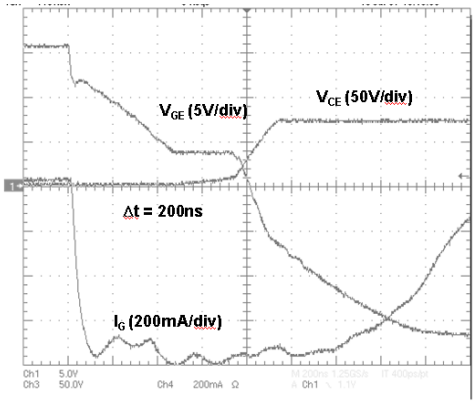


Figure 4-6: Switch off at low collector current (70 V_{CE}, 3 A I_C)

Figure 4-6 shows several measurements at different gate currents (ig) and different (low amplitude) collector currents (Ic). As it is shown, when low amplitude gate currents are extracted from the gate terminal, the switching speed (dV_{CE}/dt) increases linearly with the gate current (4-12). However, for a given collector current, there is a maximum collector-emitter voltage slope limit whatever the value of the gate current is. If this limit is found, the output capacitance of the IGBT can be estimated (4-27).

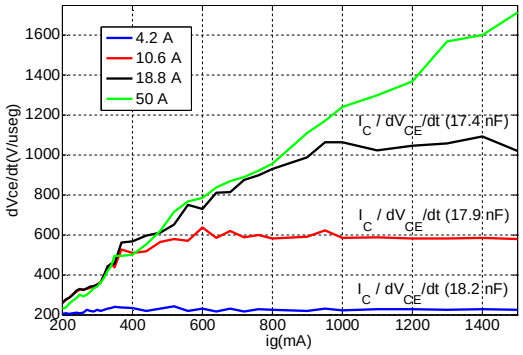


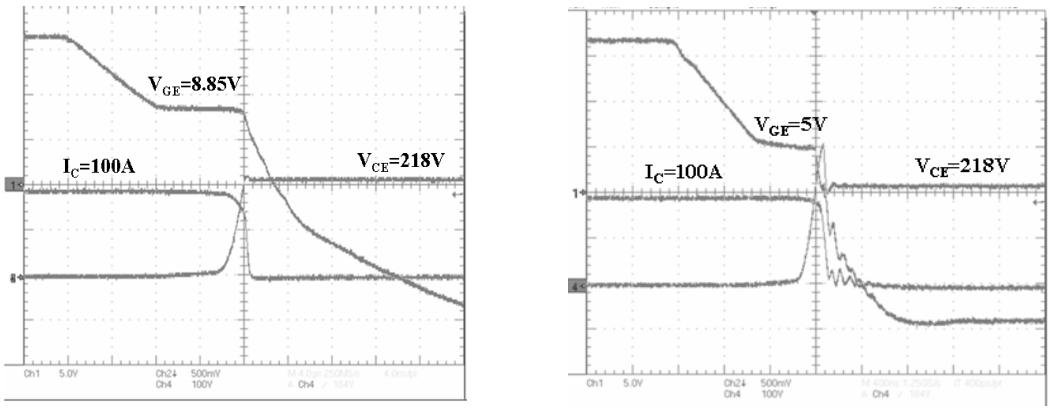
Figure 4-7: Switch off speed us gate current

4.5.2 Internal gate resistor

The massive chip parallelization inside an IGBT module forms a complex system of distributed gate inductances and gate capacitances which needs an internal gate resistor (Rg) in order to prevent oscillations. In addition, this internal gate resistor (Rg) has an important influence on the gate current during the switching (4-9). As the switching speed depends on the gate current, the value of this resistor should be considered in the IGBT model. However, the

value of the internal gate resistor (Rg) is not always available in the datasheets provided by the manufactures and therefore a suitable parametrization of this resistor is not possible.

Assuming the simplified IGBT model shown in Figure 4-1, the value of this resistor can be calculated if Miller plateau changes are measured under the same switching conditions (V_{CE}, I_C) and different gate currents (I_G). If the same collector current (I_C) is switched, the Miller plateau in the IGBT chip (V_{CGE}) should not change.



(a) (b)

Figure 4-8: Switch off at I_G= 24.2mA. V_{CE} = 218V I_C = 100 A (a), I_G= 813.3mA. V_{CE} = 218V IC = 100 A (b)

Therefore, any change in the measurable Miller plateau (V_{GE}) is associated to the voltage drop in the internal gate resistor. Figure 4-8 shows two different switch off processes at the same collector current (I_C) and the same collector-emitter voltage (V_{CE}). However, the first switch off has been performed at a constant gate current of 24.2 mA and the second switch off has been performed at a constant gate current of 813.3 mA. The measurable Miller plateau (V_{GE}) is different in both cases while the internal V_{CGE} voltage should be equal due to that the same collector current (I_C) is switched.

In consequence, the value of the internal gate resistor (Rg) can be calculated with two measurements at the same collector current (I_C) and different gate currents (I_G) applying the following equation:

$$\left|\Delta V_{GE}\right| = \left|\Delta I_G\right| \cdot R_g \qquad (4\text{-}28)$$

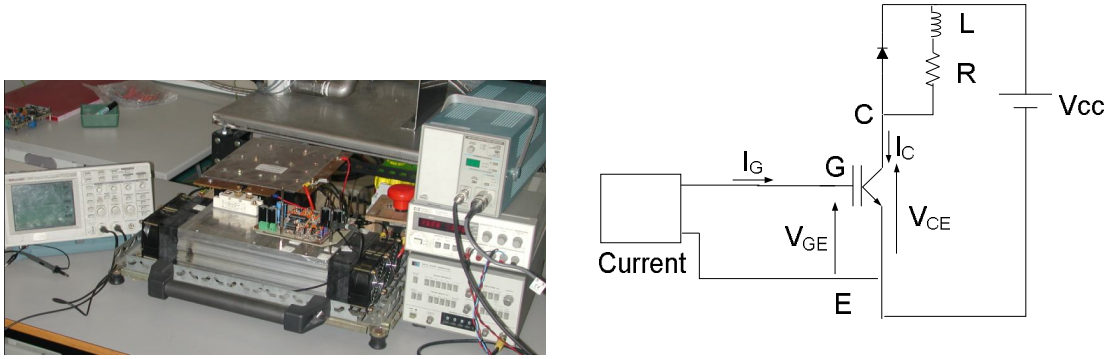
If these measurements are carefully performed, the estimated value can be close to the value provided by the manufacturer (Table 4-1). In the case of the BSM200GB60DLC IGBT module, the value of the internal gate resistor (provided by the manufacturer) is 5Ω.

I_G	V_{GE}	I_C	V_{CE}	Rg
100 mA	8.36 V	130 A	300V	**4.4 Ω**
0.5 A	6.6 V			
50 mA	6.7 V	6.54 A	157 V	**5.12 Ω**
0.5 A	4.4 V			

Table 4-1: Measurements of the internal gate resistor

4.6 Comparison of simulation results with experimental measurements

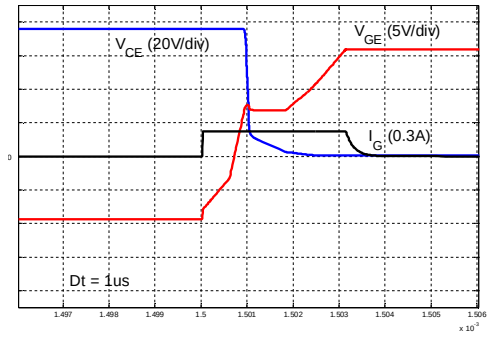
In order to validate the proposed model, simulation results are compared with experimental measurements. The IGBT chosen to be modelled is the BSM200GB60DLC IGBT module (Eupec). Static curves have been fitted using Matlab. The internal gate resistor and the interelectrode capacitances have been estimated with the explained methods. This model has been implemented in MAST and simulated in SABER. Experimental measurements have been carried out in the test bench shown in Figure 4-9.

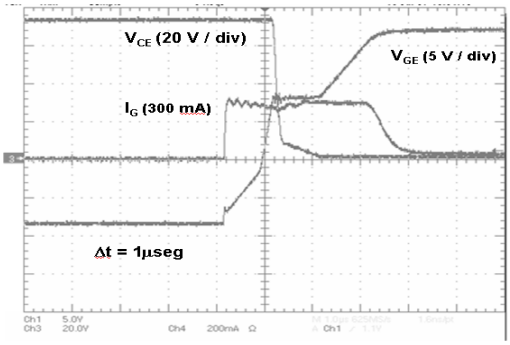


(a) (b)

Figure 4-9: Photograph of the test bench (a), Diagram of the test bench (b)

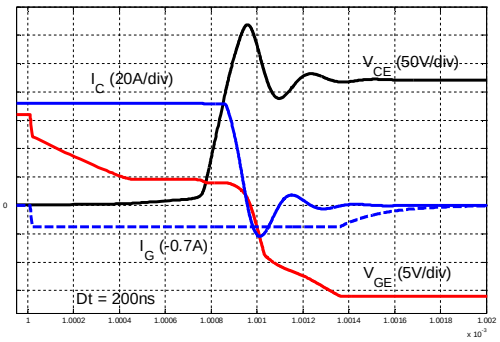
The proposed IGBT model has been verified by a reasonably good agreement with measurements. At switch on (Figure 4-10) and at switch off (Figure 4-11) the measured switching waveforms are very similar to the switching waveforms obtained with the proposed IGBT model.

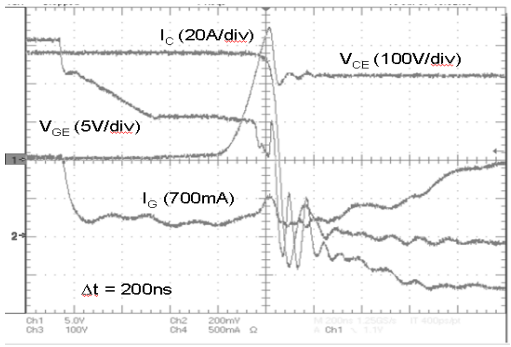




(a) (b)

Figure 4-10: Simulated switch on waveforms (a), measurements (b)





(a) (b)

Figure 4-11: Simulated switch off waveforms (a), measurements (b)

5 IGBT gate driving: Modes and Dynamics

This chapter deals with the different gate driving modes and their influence on the switching dynamics. Section 5.2 analyses current and voltage dynamics during the switching process. Section 5.3 deals with the current mode driving and the voltage mode driving of the IGBT. Advantages of the current mode driving with respect to the voltage mode driving for series connection of IGBT devices are summarized in section 5.4.

5.1 Introduction

The control of the IGBT's behaviour has become even more necessary as current and voltage limits of IGBTs increase (Figure 3-1) in order to ensure a safe and proper operation of any switching device [GE-96]. There are several reasons for the control of the switching process such as the dynamic avalanche, electromagnetic compatibility, series connection of IGBTs, switching losses optimization, etc.

The dynamic avalanche limits the maximum dV_{CE}/dt achievable during the switch off process. The depletion region (d_{dpl}) supports the blocking voltage. As the depletion region increases, the voltage blocking capability increases as well. While the IGBT is being switched off, the width of this region depends on some particular parameters of the semiconductor, especially the lifetime of minority carriers. The electrical field (E) applied to this region has to be lower than the maximum electrical field (E_{max}) to avoid dynamic avalanche (5-1). Therefore, if the growing rate of this region (dd_{dpl}/dt) is lower than the voltage slope (dV_{CE}/dt), the dynamic avalanche will occur.

$$E_{max} \geq \frac{V_{CE}}{d_{dpl}} \tag{5-1}$$

In hard switching applications, switching on an IGBT causes to switch off a free wheeling diode. The reverse recovery charge (Q_{rr}) of the diode, depends on the temperature, the current flowing across the diode and the current (switch off) slope (dI_C/dt). An increment on the current slope leads to the augmentation of the reverse recovery charges to be extracted. The reason for this behaviour is that for higher current slopes, the amount of charge which are naturally recombined is lower [WI-87]. In addition, the increment of the current slope while the IGBT is being switched off increases the reverse recovery current peak (I_{RRM}). This has a considerable influence on the overall power losses of the diode and the IGBT. For this reason the control or at least the limitation of the current slope during the switch on of the IGBT is important. In the case of a short circuit the gate driver should limit the current (switch off) slope to reduce the overvoltage caused by stray inductances.

The voltage and current slope control allows the semiconductor device to operate within the electromagnetic compatibility limits (EMI EN50081). In addition, if the converter drives an electrical machine (motors, transformers, etc) the isolation between coils suffers to high stress levels. Winding coils of electrical machines are isolated by an isolator which behaves as a stray capacitance. If High Voltage slopes are applied to these capacitances the resulting current damages the isolator and reduces the expected lifetime of the electrical machine. The maximum applicable voltage slope depends on the design of the machine and the type of the used isolator. [TH-03] reports 8.6 V/ns as the maximum voltage slope for machines driven by switched power converters.

In order to optimize the switching losses, both voltage slope (dV_{CE}/dt) and current slope (dI_C/dt) have to be controlled so that the transition time is minimized. Obviously, those switching slopes have to be maintained within the safe operating limits and electromagnetic compatibility limits.

In spite of the increase of switching losses, when some IGBTs are connected in series the voltage slope is limited in order to improve the voltage and power losses balance between the series connected devices.

5.2 Dynamics of the IGBT during the switching process

Figure 5-1 shows the relation between the gate charge state and each time interval of the switching process (dV_{CE}/dt, dI_C/dt, delay, etc). It should be noted that the IGBT is a charge controlled device during the switching, in consequence if the gate charging process is controlled, the switching process of the IGBT can be controlled.

In this section, the analytical expressions of the main switching dynamics are obtained (dI_C/dt and dV_{CE}/dt) when the IGBT operates with inductive loads and resistive loads.

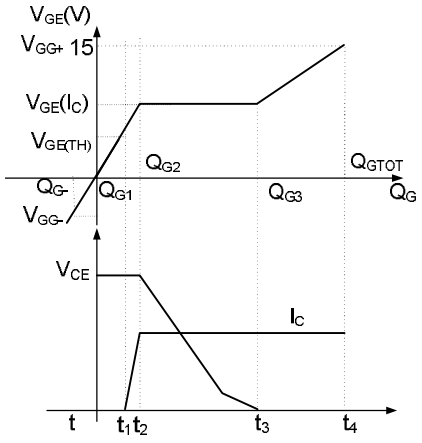


Figure 5-1: Gate voltage (V_{GE}) as a function of the gate charge (Q_G) during the switching.

Inductive load switching

In general, when a power converter drives inductive loads, there are some free wheeling diodes for the load current when the IGBTs are in blocking state, Figure 5-2. During the IGBT switch on process the free wheeling diode must be switched off before the IGBT reaches the saturation voltage (V_{CESAT}). While the free wheeling diode is conducting the IGBT collector-emitter voltage remains constant (ideally) at the bus voltage.

In order to switch off the free wheeling diode, the IGBT must conduct the current circulating across the diode. When the collector current is increasing, the collector-emitter voltage remains constant (Figure 5-2). Once the diode is switched off (it gains the reverse blocking capability) the collector-emitter voltage of the IGBT decreases until it reaches the saturation voltage. During this time interval, the collector current could be considered as remaining constant and the transfer characteristic of the IGBT does not depend on the collector-emitter voltage. Under these considerations the gate voltage remains constant due to the Miller effect. The switch off process is exactly the same as described in chapter 3.3.

In consequence, when an IGBT switches an inductive load, the voltage slope (dV_{CE}/dt) and the current slope (dI_C/dt) do not happen at the same time, so it seems possible to control independently each dynamic magnitude.

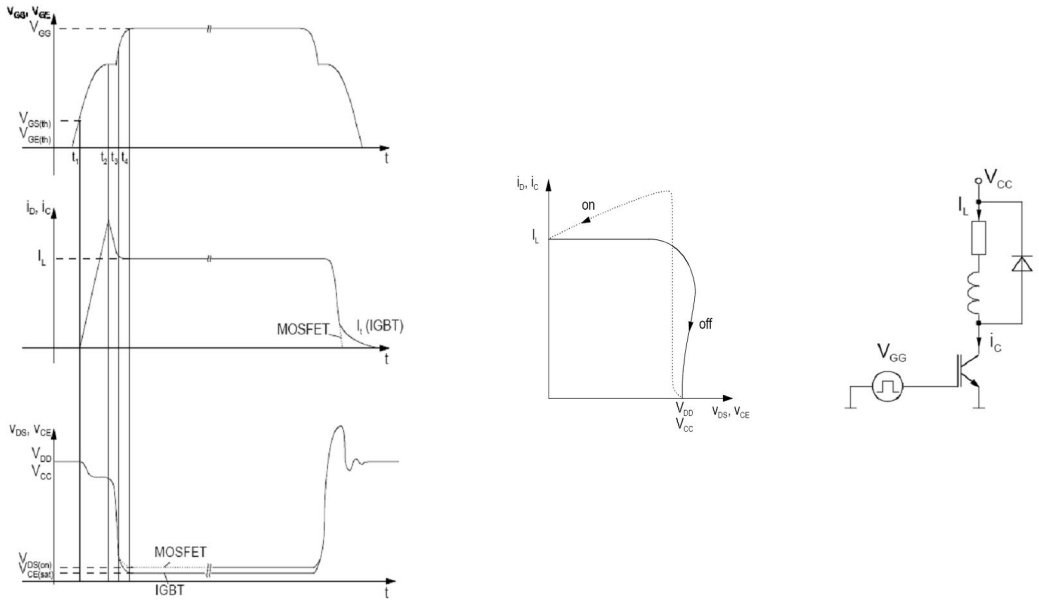


Figure 5-2: Typical hard switching waveforms, switching trajectory and test circuit [SE].

Analytical expression of dV_{CE}/dt for inductive loads

As shown in [GR-08], we could assume that the gate voltage remains constant ($dV_{GE}/dt \approx 0$) when the collector-emitter voltage slope occurs (t_2-t_3 time interval Figure 5-1). This

means that there is not any current flowing across the C_{GE} interelectrode capacitance. Therefore, the gate current is equal to the current flowing the C_{GC} interelectrode capacitance.

$$I_G \approx -im \tag{5-2}$$

During the switching process the IGBT operates in its active region. Therefore, the gate voltage and the collector current are coupled by means of the transfer characteristic. Therefore, the gate voltage (V_{CGE}) amplitude depends on the collector current (I_C). To represent this relation, in this section the gate voltage is called V_{CGE_IC}.

$$V_{CGE\_IC} = \sqrt{\frac{I_C}{k}} + V_{GE(th)} \tag{5-3}$$

From (5-2) the gate current is charging / discharging the C_{GC} interelectrode capacitance.

$$I_G \approx -\frac{dQ_{GC}}{dt} \approx -\frac{d(C_{GC} \cdot V_{GC})}{dt} \approx -C_{GC} \cdot \frac{dV_{CE}}{dt} - (V_{CE} - V_{CGE\_IC}) \cdot \frac{d(C_{GC})}{dt} \tag{5-4}$$

Where Q_{GC} is the amount of charge to be injected to the C_{GC} capacitance. This capacitance shows a nonlinear behaviour and its value decreases with the colector emitter voltage. This capacitance could be expressed as follows:

$$C_{GC} \approx \frac{A}{\sqrt{V_{CE} - V_{CGE\_IC}}} \tag{5-5}$$

Where A is a curve fitting parameter, V_{CE} is the colector-emitter voltage and V_{CGE_IC} is the gate emitter voltage. Replacing (5-5) in (5-4) the following expression is obtained:

$$I_G \approx -\frac{A}{2 \cdot \sqrt{V_{CE} - V_{CGE\_IC}}} \cdot \frac{dV_{CE}}{dt} \tag{5-6}$$

In consequence, the voltage slope can be approached as follows:

$$\frac{dV_{CE}}{dt} \approx -\frac{I_G}{C_{GC(V_{CE})}} \quad \text{for } C_{GC(V_{CE})} = \frac{A}{2 \cdot \sqrt{V_{CE} - V_{CGE\_IC}}} \tag{5-7}$$

The gate current can be calculated from equation (4-9), therefore:

$$\frac{dV_{CE}}{dt} \approx -\frac{I_G}{C_{GC(V_{CE})}} \approx -\frac{V_{GE} - V_{CGE\_IC}}{R_g \cdot C_{GC(V_{CE})}} \tag{5-8}$$

Analytical expression of dI_C/dt for inductive loads

In order to obtain an analitical expresion for dI_C/dt, the stray inductance which couple the gate circuit with the power circuit should be considered. This inductance is known as the common emitter stray inductance (L_e, Figure 5-3) due to the fact that this inductance shows the effect of the dI_C/dt on the gate circuit during the switching process.

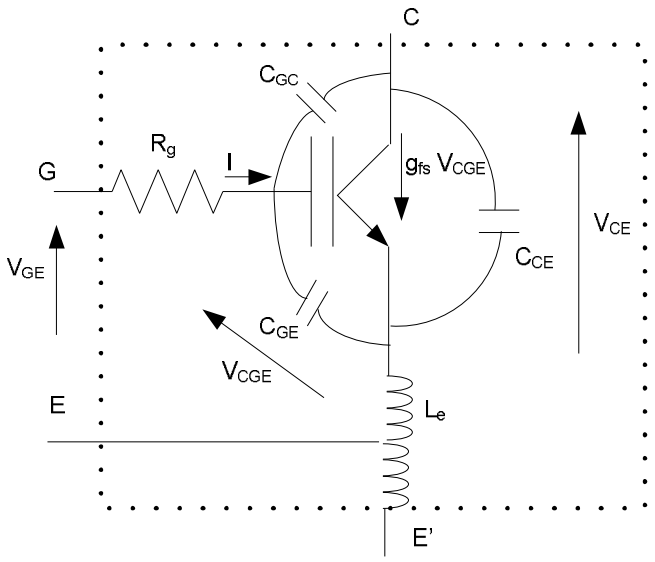


Figure 5-3: Simplified IGBT model with common emitter inductance.

Asuming the circuit shown in Figure 5-3 the following could be said:

$$V_{GE} = V_R + V_{CGE\_IC} + V_{Le} = Rg \cdot I_G + V_{CGE\_IC} + L_e \cdot \frac{dI_C}{dt} \tag{5-9}$$

During the switch on and switch off processes of the IGBT the colector-emitter voltage (V_{CE}) is equal (ideally) to the bus voltage. In general, at high operating voltages the C_{GE} capacitance is substantially larger than the C_{GC} capacitance. Therefore, during this time interval we can assume that all the gate current flows across the C_{GE} capacitance.

$$V_{GE} \approx Rg \cdot C_{GE} \cdot \frac{dV_{CGE\_IC}}{dt} + V_{CGE\_IC} + L_e \cdot \frac{dI_C}{dt} \tag{5-10}$$

In general, when the collector current changes (dI_C/dt) the IGBT is operating in its active region. In consequence, the gate voltage and the colector current are coupled by means of the forward transfer characteristic (g_{fs}) of the IGBT.

$$g_{fs} = \frac{dI_C}{dV_{CGE}} \tag{5-11}$$

And in consequence, the following expresion can be obtained:

$$V_{GE} \approx \frac{Rg \cdot C_{GE}}{g_{fs}} \cdot \frac{dI_C}{dt} + V_{CGE\_IC} + L_e \cdot \frac{dI_C}{dt} \tag{5-12}$$

Therefore, from (5-12) the expresion for the current slope is obtained:

$$\frac{dI_C}{dt} \approx \frac{V_{GE} - V_{CGE\_IC}}{\frac{C_{GE} \cdot R_g}{g_{fs}} + L_e} \approx \frac{I_G \cdot g_{fs}}{C_{GE}} \tag{5-13}$$

Resistive load switching

Unlike what happens with inductive loads, when a resistive load is switched, the collector-emitter voltage (V_{CE}) changes with the collector current as shown by (5-14). In consequence, during the switching of the IGBT, when the gate voltage exceeds the gate threshold voltage, the collector current starts to increase and the collector-emitter voltage decreases until the saturation voltage is reached, Figure 5-4. In this case, the Miller effect (caused by V_{CE} variations) does not occur at a constant gate voltage (V_{GE}) due to the collector current variation during the switching process.

$$V_{CE} = V_{cc} - R_L \cdot I_C \tag{5-14}$$

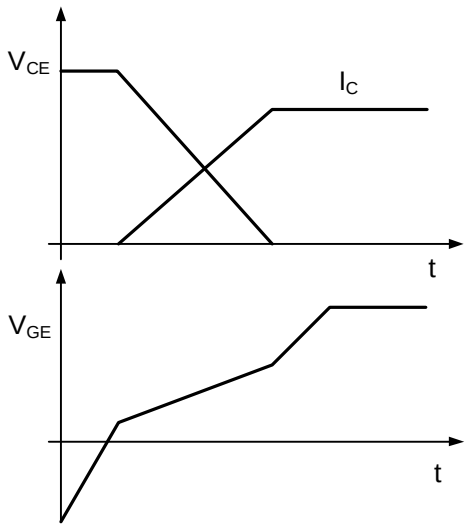


Figure 5-4: Resistive load switching

From (4-11), (5-5) and (5-11) the following expression could be obtained:

$$I_G \approx \frac{dI_C}{dt} \cdot \frac{\left(C_{GE} + \frac{1}{2} \cdot C_{GC}\right)}{g_{fs}} - \frac{C_{GC}}{2} \cdot \frac{dV_{CE}}{dt} \tag{5-15}$$

From (5-14) the relation between dV_{CE}/dt and the dI_C/dt is:

$$\frac{dV_{CE}}{dt} = -R_L \cdot \frac{dI_C}{dt} \tag{5-16}$$

Therefore, an analytical expression for the current slope (dI_C/dt) and voltage slope (dV_{CE}/dt) can be obtained:

$$\frac{dI_C}{dt} \approx \frac{I_G}{\frac{\left(C_{GE} + \frac{1}{2} \cdot C_{GC}\right)}{g_{fs}} + \frac{C_{GC}}{2} \cdot R_L} \tag{5-17}$$

$$\frac{dV_{CE}}{dt} \approx \frac{-I_G \cdot R_L}{\frac{\left(C_{GE} + \frac{1}{2} \cdot C_{GC}\right)}{g_{fs}} + \frac{C_{GC}}{2} \cdot R_L} \tag{5-18}$$

In consequence, when a resistive load is switched the voltage slope (dV_{CE}/dt) is coupled with the current slope (dI_C/dt) as shown by (5-16). Therefore, the independent control of both dynamic parameters is not possible.

However, in power electronic applications most of the loads present an inductive behaviour (transformers, inductances, electrical machines, etc). For this reason, from this point onwards, only inductive loads will be considered.

5.3 Gate driving modes

In section 5.2 the main dynamic characteristics of the IGBT have been deduced for inductive loads (5-19), (5-20):

$$\frac{dV_{CE}}{dt} \approx -\frac{I_G}{C_{GC(V_{CE})}} \approx -\frac{V_{GE} - V_{CGE\_IC}}{R_g \cdot C_{GC(V_{CE})}} \tag{5-19}$$

$$\frac{dI_C}{dt} \approx \frac{I_G \cdot g_{fs}}{C_{GE}} \approx \frac{V_{GE} - V_{CGE\_IC}}{\frac{C_{GE} \cdot R_g}{g_{fs}} + L_e} \tag{5-20}$$

These expressions show that the larger the gate current (I_G), the higher the gate capacitance charge / discharge process speed and therefore the IGBT switching speed. The gate terminal allows the control of the switching process speed.

There are three main methods to perform this charge / discharge process [SE]: Standard gate driving (voltage source plus a gate resistor), current mode gate driving (gate current control) and voltage mode driving (gate voltage control), Figure 5-5.

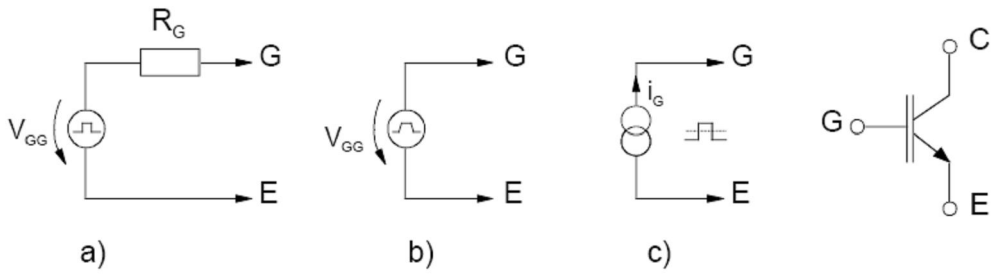


Figure 5-5: (a) Standard gate driving mode, (b) voltage mode driving, (c) current mode gate driving [SE].

While the standard driving mode is widely used by commercial IGBT drivers, the voltage mode driving and the current mode driving are mostly used by active gate control techniques that aim to improve the switching behaviour of the IGBT. Consequently, in [SC-03], [KA-01], [KR-05] voltage mode driving is used to control series connected IGBTs, whereas in [TH-03], [LI-97], [SI-95] current mode driving method is used to optimize the switching behaviour of the IGBT.

The reliability, effectiveness and complexity of the switching process control depend directly on the chosen driving mode. Therefore, the characteristics of those driving modes must be taken into account in order to choose the one that best fits the needs of the application. As the standard driving method can be considered a particular case of voltage mode driving where the applied voltage is constant, this section will be focused only on the less known voltage mode and current mode driving methods.

In this context, section 5.3.1 describes the current mode driving while section 5.3.2 deals with the voltage mode driving.

5.3.1 Current mode gate driving

The current mode driving consists in the use of a current source to control the amount of injected/extracted charges to/from the gate terminal during the switching process. In

consequence, the gate driver circuit controls the charge injected to/extracted from the gate terminal, Figure 5-6.

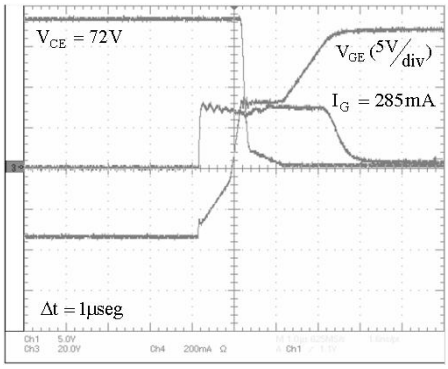


Figure 5-6: Switch on at constant gate current

As shows equation (5-20), with this driving mode the collector current slope (dI_C/dt) depends on the gate current (I_G), gate emitter capacitance (C_{GE}) and the transconductance (g_{fs}) of the IGBT (5-21).

$$g_{fs} = \frac{dI_C}{dV_{CGE}} \approx 2 \cdot K \cdot \left(V_{CGE} - V_{GE(th)}\right) \qquad (5\text{-}21)$$

During the switch on process, if the gate terminal is driven by a constant gate current, the collector current slope (dI_C/dt) increases with the time. This is caused by the increase of the transconductance (5-21) for higher gate voltages (V_{CGE}). In order to limit the maximum reverse recovery current (I_{RRM}) of the free wheeling diode, the average collector current slope (dI_C/dt) has to be reduced (by means of I_G). This undesired effect has a negative influence on the switch on losses of the IGBT.

The collector-emitter voltage slope (dV_{CE}/dt) depends on the gate current and the Miller capacitance (C_{GC}), (5-19). Therefore, the voltage slope (dV_{CE}/dt) is independent of the collector current (I_C) and depends mainly on the gate current (I_G), Figure 5-7.

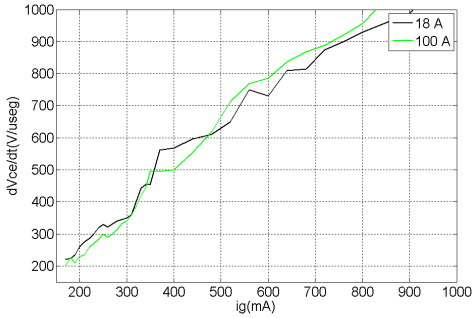


Figure 5-7: dV_{CE}/dt vs ig at I_C = 18 A and 100 A (Measurements)

In consequence, the current mode driving is suitable to control the voltage slope (dV_{CE}/dt) by means of open loop active gate control techniques [LI-97], [VI-99]. However, the interelectrodic capacitances, and the transfer characteristic of the IGBT depend on several variables such as the working temperature or the voltage to be switched. And therefore, the accuracy of the open loop switching control depends on these physical magnitudes.

5.3.2 Voltage mode gate driving

The voltage mode driving consists in the use of a voltage source to set the gate voltage (V_{GE}) at the gate terminal of the IGBT in order to control the charging process during the switching. Consequently varying the gate voltage, the amount of injected/extracted charges can be controlled and therefore the behaviour of the IGBT can be controlled. If the applied gate voltage is constant (+15 V or -15 V), this driving mode behaves like the standard driving mode.

Due to the internal gate resistor (R_{GINT}), the voltage applied by the gate driver at the gate terminal (V_{GE}) differs from the voltage on the IGBT chip (V_{CGE}) during the switching process, Figure 4-1. From equations (5-19) and (5-20) the gate current (I_G) results from the voltage applied on the gate resistance (V_{GE} - V_{CGE}). Figure 5-8 shows the gate current evolution during the switch on and switch off process of the IGBT. As the figure shows, the injected/extracted charge profile is not controlled by the applied gate voltage.

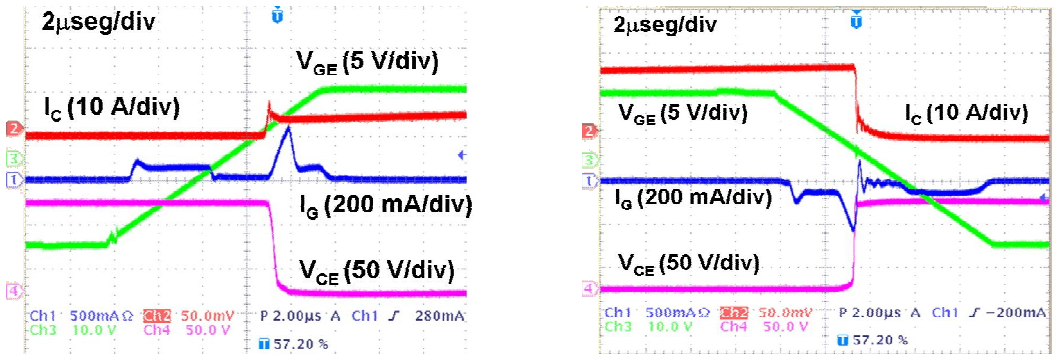


Figure 5-8: Switch on and switch off at a constant gate voltage slope

As states in equation (5-20) the collector current slope (dI_C/dt) depends on the voltage applied to the gate terminal (V_{GE}), the gate voltage at the IGBT chip (V_{CGE}), the internal gate resistor (R_g), the transconductance (g_{fs}) and the gate emitter capacitance (C_{GE}). During the switch on process, the collector current slope (dI_C/dt) should be limited to avoid an excessive reverse recovery current in the free wheeling diode.

Assuming that the input impedance of the IGBT is a capacitance (C_{iss}) in series with the gate resistor (R_g), for an applied gate voltage step (V_{GE}) the internal gate voltage (V_{CGE}) evolution could be expressed as follows:

$$V_{CGE} \approx \frac{V_{GE}}{C_{iss} \cdot R_g \cdot s + 1} \tag{5-22}$$

In consequence, the gate current (I_G) during the switch on process of the IGBT is given by equation (5-3):

$$I_G \approx \frac{V_{GE} - V_{CGE}}{R_g} \approx \frac{V_{GE} \cdot (C_{iss} \cdot R_g \cdot s)}{R_g \cdot (C_{iss} \cdot R_g \cdot s + 1)} \tag{5-23}$$

As it can be seen in equation (5-23), the gate current decreases exponentially until the saturation (beginning of Miller effect). This means that the collector current slope is maintained approximately constant in time [TH-03].

During the voltage slope (dV_{CE}/dt) time interval (Figure 3-10), the gate current depends on the driver output voltage (V_{GE}), the IGBT chip gate voltage (V_{CGE_IC}), the internal gate resistor (R_g) and the gate collector capacitance (C_{GC}). An undesired effect of the voltage mode gate driving resides in the coupling between the collector current (I_C) and the IGBT chip gate voltage (V_{CGE_IC}) (chapter 5.2). In consequence, the gate current amplitude during the Miller effect does not depend only on the applied gate voltage but it also depends on the collector current (I_C).

Figure 5-9 shows the collector-emitter voltage slope during the switch on process as a function of the IGBT chip gate voltage (V_{CGE_IC}) and the collector current (I_C) for different gate voltage steps (V_{GE}).

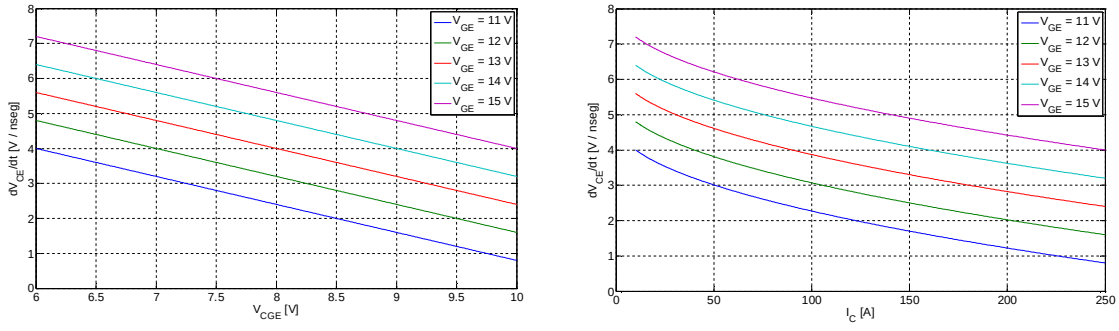


Figure 5-9: dV_{CE}/dt vs V_{CGE} (left), dV_{CE}/dt vs I_C (right) for different gate voltages (V_{GE}). Cgc = 0.5nF, Rg = 2.5Ω, K= 10 (Simulations)

This is the reason why the gate voltage driving mode is not the most suitable driving mode to be used by open loop active gate control methods oriented to collector-emitter voltage slope control.

5.4 Conclusions

As shown in previous sections current mode gate driving is more suitable than the voltage mode gate driving for the collector-emitter voltage slope control. This makes the current mode driving appropriate for applications as series connection of IGBTs in which the collector-emitter voltage control is mandatory for voltage balance purposes.

For this reason, during this research work the developed gate driver is based on current mode gate driving instead of the voltage mode gate driving. The implemented active gate control method is described in chapter 8.

Part 3: SERIES CONNECTION OF IGBTs

6 Effect of Parameter Differences on the Voltage Balance of Series Connected IGBTs

When several IGBTs are connected in series, the operation at higher blocking voltages is possible than the allowed voltage by a single IGBT. However, due to voltage slope differences and asynchronous switchings, the voltage balance is not guaranteed if some considerations are not taken into account. If any IGBT inside the switching valve exceeds its maximum blocking voltage or, if any IGBT is stressed due to its operation within the active region for a long time, the failure possibilities increases considerably. For this reason, all the IGBTs inside the switching valve should operate with the same voltage slope (dV_{CE}/dt) and synchronously. In addition, there are other parameters which have influence in the voltage balance of series connected IGBTs. These parameters are the tail current, leakage current and reverse recovery current (antiparallel diodes).

6.1 Differences on collector-emitter voltage slopes

In general, an IGBT is driven by a standard gate driver which applies a constant voltage at the gate terminal while the gate current is limited by means of a gate resistor.

Equation (5-19) shows that the dV_{CE}/dt depends on the voltage applied by the driver (V_{GE}), the gate voltage inside the IGBT chip (V_{CGE_IC}), the gate resistor (external and internal) and the gate collector (C_{GC}) capacitance.

As presented in previous chapters, the Miller plateau voltage depends on the collector current and the transfer characteristic of the IGBT. Similarly, the transfer characteristic depends on the operating temperature, operating voltage and individual characteristics of the IGBT. Therefore, even though the same collector current (I_C) circulates across all series connected IGBTs, the gate voltage inside the IGBT chip (V_{CGE_IC}) will be different from one IGBT to another if the operating temperature or the individual IGBT characteristics are not similar.

The internal gate resistor is usually made of silicon [JO-01] and its ohmic value is determined by its doping profile. In addition, the value of the internal gate resistor presents high temperature dependence (positive temperature coefficient). Therefore, the IGBT with the highest operating temperature has the highest internal gate resistance, slower switching speed and higher switching losses. This behaviour could cause the thermal runaway. In general, the tolerances of the internal gate resistance are notoriously high.

If unmatched IGBT devices are connected in series, parameter differences between gate collector capacitances (C_{GC}) will appear from one device to another.

Consequently, when the series connected IGBTs are driven by a conventional gate driver (the most used), the parameter differences cause deviations on the individual voltage slopes (dV_{CE}/dt).

Figure 6-1 shows the voltage slope as a function of the gate resistor assuming a 10% difference in the gate collector capacitance (C_{GC}) and 2 volts on the miller plateau (V_{CGE_IC}) for a given collector current (I_C).

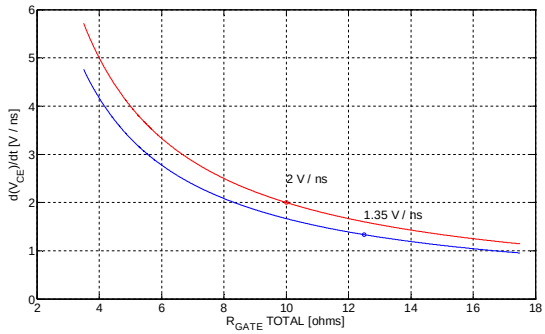


Figure 6-1: dV_{CE}/dt as a function of the gate resistor, ΔC_{GC}= 10%, Difference in V_{CGE_IC}=2V

Assuming that two IGBTs are connected in series and both are synchronously switched (not very probable) the voltage slope could be estimated with the following expression:

$$V_{CE2} = V_{CE1} \cdot \frac{dV_{CE2}/dt}{dV_{CE1}/dt} \tag{6-1}$$

Under the considered conditions one of the IGBT will reach a collector emitter voltage 30% higher than the other IGBT due to voltage slope differences, Figure 6-1.

6.2 Asynchronous switching

During the switch on process, the delay time is determined by the time required to reach the gate threshold voltage of the IGBT ($V_{GE(th)}$). If the voltages of series connected IGBTs do not start falling at the same time, voltage and power loss unbalances will be produced, Figure 6-3.

A synchronization error during the switch off process is more critical than a synchronization error during the switch on process. This is because the faster IGBT withstands higher voltages, Figure 6-3. At the beginning of the switch off process, the gate driver must extract the charge excess (6-2) injected during the switch on to ensure a good saturation level, Figure 6-2.

$$Q_{delay} = Q_{GTOT} - Q(I_C) \approx \left(V_{GG+} - \left(\sqrt{\frac{I_C}{k}} + V_{GE(th)} \right) \right) \cdot C_{iss} \qquad (6\text{-}2)$$

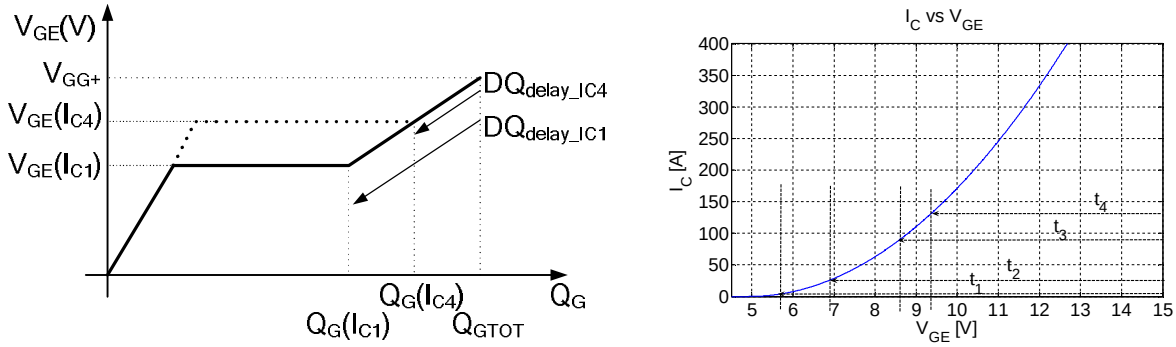


Figure 6-2: Amount of charge extracted during the switch off delay time.

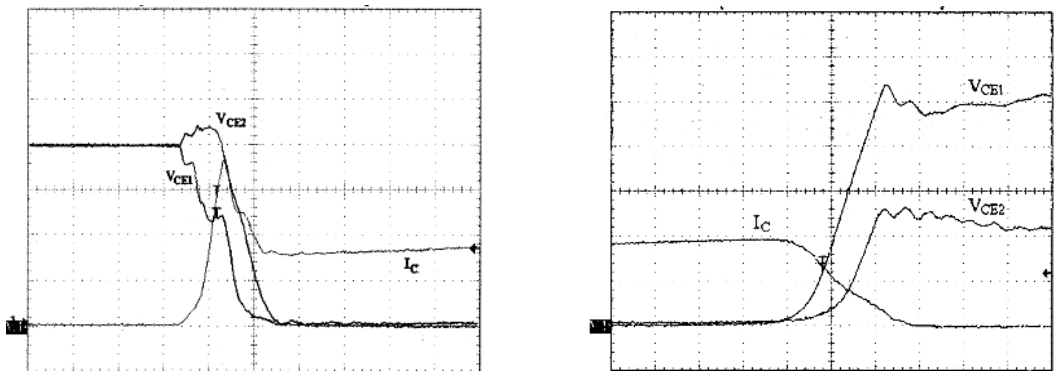
The amount of charges to be extracted (Figure 6-2) during the switch off process depends mainly on the collector current (I_C), the input capacitance (C_{iss}) and the transfer characteristic (k, $V_{GE(th)}$).

Consequently, the delay time during the switch off process depends on the charge extraction speed:

$$t_{delay} \approx \frac{Q_{delay} \cdot R_g}{V_{GE} - V_{CGE}} \quad \text{where } Q_{delay} \approx \left(V_{GG+} - \left(\sqrt{\frac{I_C}{k}} + V_{GE(th)} \right) \right) \cdot C_{iss} \qquad (6\text{-}3)$$

From equation (6-3) we can deduce that a higher gate resistance (R_g), a higher gate voltage (V_{GE}) or a higher amount of charges to be extracted (different k, $V_{GE(th)}$ or C_{iss}) during the switch off process affects the delay time of the IGBT.

Although an active clamp is enough to limit the maximum operating voltage of each IGBT (V_{CEMAX}), this is not a proper solution to balance switching losses, E_{on} and E_{off}. Therefore, when a high operating frequency is required, switching losses become important and the gate charge profile must be used to achieve the balance of switching power losses (E_{on} and E_{off}).



(a) (b)

Figure 6-3: Unbalanced switch on (a) and unbalanced switch off (b) of two series connected IGBTs [RA-01].

6.3 Differences in tail currents

The last time interval of the switch off process is characterized by an overvoltage caused by the collector current slope (dI_C/dt) across the stray inductance of the power circuit. Before the extinction of the collector current, there exists a tail current caused by the recombination of minority carriers in the p doped region of the IGBT. This tail current can not be controlled by means of the gate terminal. If the tail currents are the same in all series connected IGBT, there should not be any voltage balance problem. In contrast, if the tail currents are not exactly the same there is a differential current that charges the equivalent output capacitance (C_{eq}) of the IGBTs with the lower tail currents. This charging process causes a voltage unbalance between the voltages of series connected IGBTs, Figure 6 5.

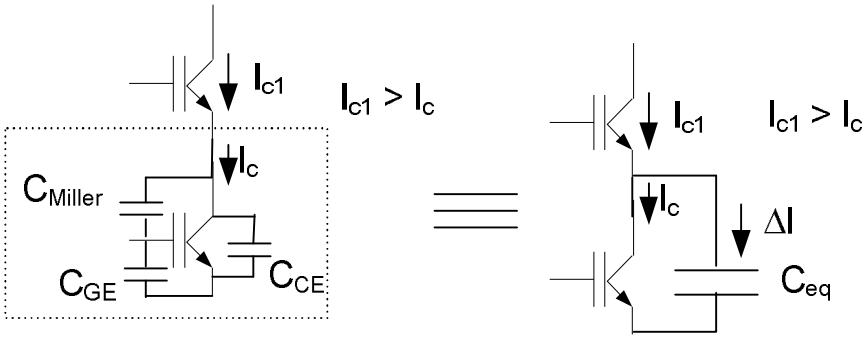


Figure 6-4: Equivalent output capacitance charged by tail current differences

6.4 Differences in leakage currents

During the blocking state of the IGBT, the gate voltage is lower than the threshold voltage, therefore only a small leakage current can circulate across the IGBT ($I_{leakage}$). This leakage current causes power losses during the blocking state. If the leakage currents of the

series connected IGBTs are not equal, there will exist a voltage unbalance between the series connected IGBTs. This voltage unbalance affects the blocking state power losses and the switch on power losses (higher voltage, higher losses). To improve the voltage balance during the blocking state, the use of parallel connected voltage sharing resistors is common. In order to minimize the power generated by these resistors high resistor values are desirable. However, the larger the resistor ohmic value is, the less the influence on the voltage balance.

These resistors are dimensioned assuming the worst case. In consequence, n series connected IGBTs are considered where (n - 1) IGBTs show the maximum leakage current ($I_{leakage(max)}$) while one of them has the minimum leakage current ($I_{leakage(min)}$), (Figure 6-5). The maximum blocking voltage supportable by this IGBT is V_D.

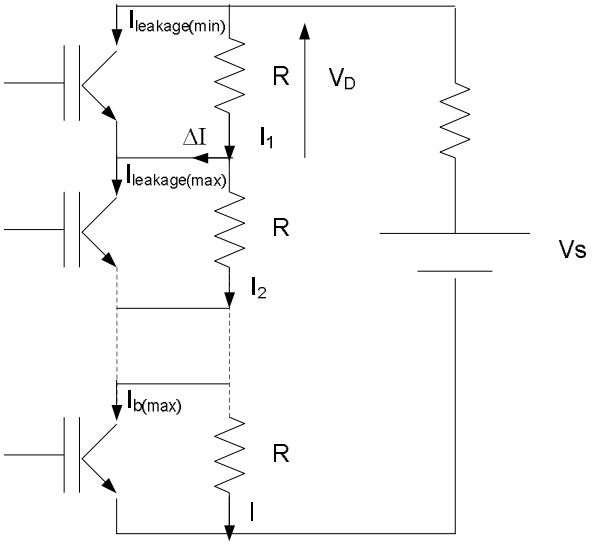


Figure 6-5: Static voltage balance network.

Consequently, the value of the parallel connected resistor to ensure a proper voltage balance is given by the following expression:

$$R \leq \frac{n \cdot V_D - V_S}{(n-1) \cdot \left(I_{leakage(max)} - I_{leakage(min)}\right)} \qquad (6\text{-}4)$$

The power dissipated by this resistor is given by equation (6-5).

$$P_D = \frac{V_D^2}{R} \qquad (6\text{-}5)$$

Equations (6-4) and (6-5) show that the higher the leakage current difference is, the lower the required resistor value and the higher the power losses on these resistors. The use of matched IGBTs should maintain the generated power losses within reasonable levels.

6.5 Differences on the amount of reverse recovery charges

Voltage source converters are based on bidirectional current switches. These bidirectional current switches are composed by a fully controlled switch (IGBT, IGCT, etc) and an antiparallel diode. In consequence, when some switches are connected in series to compose a switching valve, antiparallel diodes are also connected in series. During the switch off of those diodes, the voltage balance depends exclusively on the individual diode parameters and not on the active gate control of the IGBT.

When a forward conducting diode is abruptly reverse biased, a short time elapses before the device actually regains its reverse blocking capabilities. Most importantly, before the diode does regain blocking ability, it may be considered as a short circuit in its normally blocking direction [WI-87]. During forward conduction, there is an excess of minority carriers in each diode region. The holes in the n-region and electrons in the p-region must be removed at switch-off. During this time interval the charge excess (Q_r) is recovered in a time (t_{rr}) in which a reverse recovery current flows across the diode (I_{rm}).

When diodes are connected in series, differences on the amount of recovery charges could lead to voltage unbalances. Those elements with least recovery charge requirements recover first and support the reverse bias. The unrecovered devices recover slowly, since recovery now occurs as a result of the leakage current across the recovered devices and natural recombination. The reverse-blocking voltage can be shared more equally by placing a snubber in parallel with the diode. The snubber capacitor action is to provide a transient current path bypassing a recovered device allowing in this way a faster recovery of slower devices.

When some diodes are connected in series, in order to support a DC bus voltage (Vs) and the maximum supportable blocking voltage per diode is V_D, the required snubber capacitance to improve the voltage sharing is given by the following expression:

$$C \geq \frac{(n-1)\cdot \Delta Q}{n \cdot V_D - Vs} \tag{6-6}$$

As shown in [LI-03] [LI-04], in spite of the switching process of the IGBT is controlled by means of the gate driver, the use of small RC snubber networks in parallel with the IGBT in order to improve the voltage balance is advised.

7 Overview of Voltage Balancing Methods for Series Connected IGBTs

As seen in the previous chapter, dynamic voltage unbalances between series connected IGBTs are caused mainly by parameter differences that have influence on individual delay times and different collector-emitter voltage slopes (dV_{CE}/dt). Differences on interelectrode capacitances, transfer characteristics or differences on gate currents are the main cause of voltage unbalances. The voltages of series connected IGBTs must be balanced to avoid excessive thermal or/and electrical stress in some switching devices inside the switching valve. In consequence, the failure possibility can be reduced increasing the reliability of the valve.

There are several papers that present some solutions that are able to satisfy (fully or partially) the requirements of the series connection of IGBTs. Some of those methods act on the load side determining switching dynamics by means of passive components. Some other methods act on the gate side controlling the charging profile and therefore modifying the behaviour of the IGBT during the switching process. Those last methods are known as active gate control methods. On the other hand, there are some other methods that limit the maximum blocking voltage of the series connected IGBTs. Those circuits are known as clamps circuits. In this chapter, an overview of the different voltage balancing methods is presented, Figure 7-1.

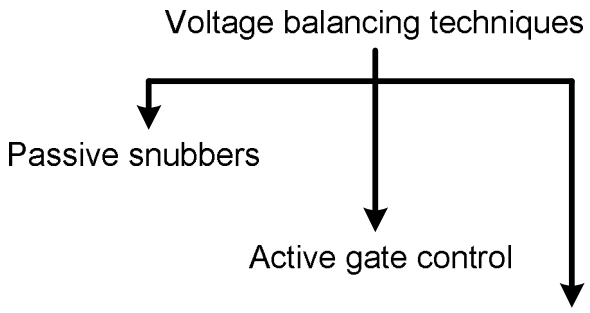
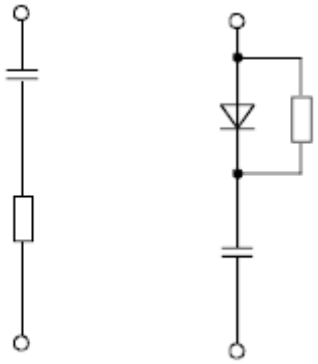


Figure 7-1: Voltage balancing techniques

7.1 Snubber networks

RC and RCD snubber networks limit the voltage slope (dV_{CE}/dt) of series connected IGBTs. The capacitor value of the snubber network is sized to limit the maximum voltage dynamic (ΔV_{CE}) at the maximum working current.



$$C_{snubber} \approx \frac{I_{max} \cdot \Delta t}{\Delta V_{CE}} \qquad (7\text{-}1)$$

Figure 7-2: RC Snubber and RCD Snubber [SE].

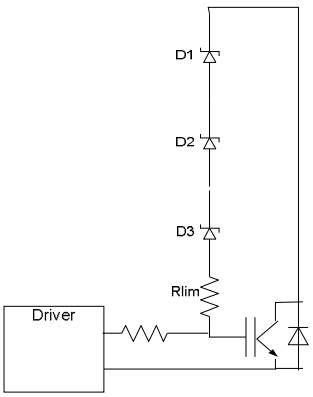
Although the use of snubber networks does not require any consideration for the gate driver (making this solution easy to implement), it presents some disadvantages that should be taken into account during the design of the converter.

The high reliability achieved by snubber networks is strongly penalized by the additional extra components which are subjected to the full current and working voltage. In addition, these networks generate power losses due to the fact that the energy stored during the switch off is dissipated during the switch on of the IGBT. This energy is usually converted to heat during the on state of the IGBT. To achieve a proper operation of those networks, the IGBT must be maintained switched on for a minimum time in which the stored energy in the capacitor is dissipated. Consequently, the maximum switching frequency is limited. Although some regenerative snubbers have been proposed [MA-99], [BU-98], their complexity makes them unattractive.

As shown from (7-1), the voltage increase (dV_{CE}/dt) depends on the collector current. Therefore, when the switched current is lower than the nominal current the measured voltage slope (dV_{CE}/dt) is lower. This means that the stored energy in the snubber at lower collector currents is higher than required to ensure a proper voltage balance. Obviously, this behaviour reduces the overall efficiency of the converter.

7.2 Clamp networks

The collector-emitter voltage clamping process starts when an excessive voltage is measured between collector and emitter terminals. In general, the clamping network injects current to the gate terminal causing the operation of the IGBT in its active region. In consequence, further increases of the collector-emitter voltage are avoided. In general, the feedback network is formed by some transils (D1, D2, D3 …) whose current is limited by a resistor (Rlim). The value of this resistor depends on the gate driver switch off voltage (V_{G-}), the switch off gate resistor (R_{off}), the amount of transils (n) and the clamp voltage (V_{clamp}), (7-2).



$$R_{lim} \approx \frac{Roff \cdot \left(V_{clamp} - V_{GE(th)} - n \cdot V_{transil}\right)}{V_{GE(th)} - V_{G-}} \qquad (7\text{-}2)$$

Figure 7-3: Clamping network

In spite of its simplicity, this method has some drawbacks that should be taken into account. If the parameter differences of the series connected IGBTs and gate drivers are too high, the IGBT will work for a long time in its active operation region. In this region the switching losses and consequently the thermal stress are high. This fact reduces the reliability of the system. In addition, when a short circuit occurs the junction capacitance could inject current across the gate terminal due to the High Voltage slope, making difficult the control of the switch off process of the IGBT.

There are some papers that propose different versions of this balancing method. In [PI-04] the clamping circuit is formed with transils and capacitors. Therefore, the voltage slope is limited when some voltage level is exceeded before the voltage clamp limits the maximum operating voltage. [JA-03] and [SI-96] propose the use of small snubber networks and clamp circuits to improve the voltage balance between the series connected IGBTs.

7.3 Gate signal delay control (synchronization)

This method tries to improve the voltage balance by controlling the switching instant of the series connected IGBTs. This method does not require any extra component in the gate driver and in consequence it does not generate any extra losses in the IGBT, however, high performance control circuitry is required.

In [GE-94], [GE-96b] a fast switching valve is tried (switching time less than 1μsecond). The valve switches 3.5kV and 300 amperes. Although this method theoretically does not affect the switching dynamics and therefore the switching losses, the used gate driver limits the voltage slope (dV_{CE}/dt) and the current slope (dI_C/dt) during the switching [GE-96] and in practice, there is an influence on the switching losses.

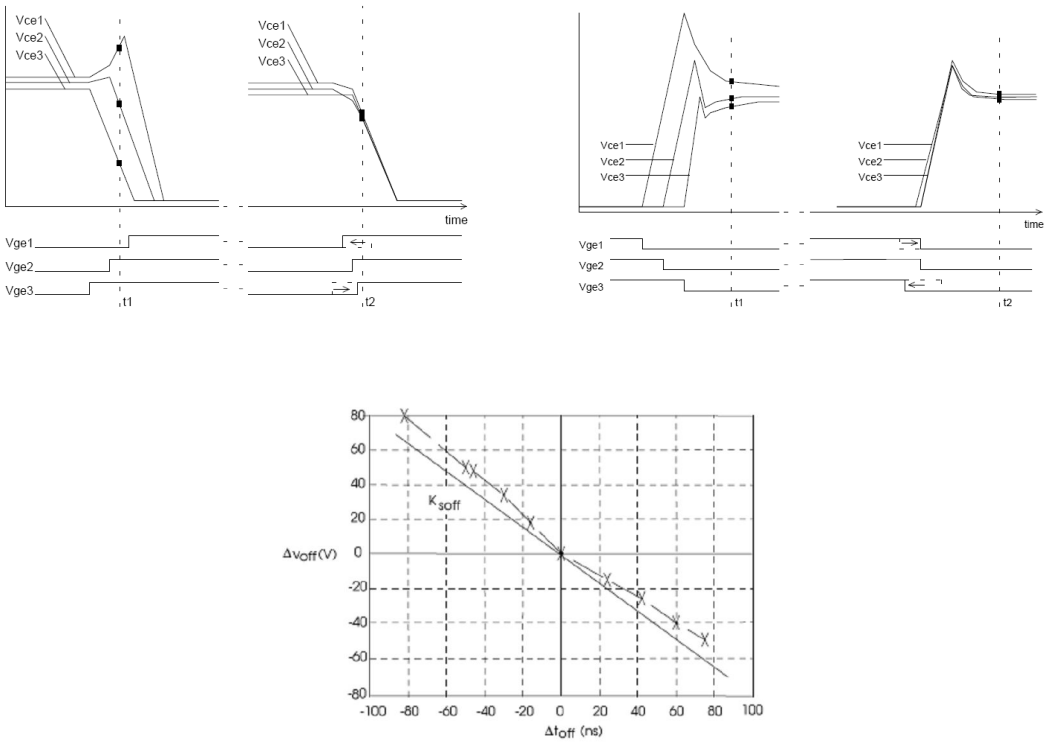


Figure 7-4: Synchronization during the switch on. Synchronization during the switch off. Transfer function to synchronize the switch off (Measurement (x)) [GE-94].

It is important to note, that this method is based on the knowledge of each collector-emitter voltage during the switching. This involves the need of high speed sampling and processing capability and measurements with high isolation. [NA-03] simplifies the required circuitry allowing to each individual driver the control of the switching instant. In consequence, the use of global sampling and processing circuitry is avoided.

7.4 Master slave control method

Master slave control method consists on the control of the collector-emitter voltage of slave IGBTs having as reference the collector-emitter voltage of the master IGBT [GR-99b]. Small compensation gate currents are added to the main gate current to control the evolution of collector-emitter voltages (V_{CE}). Collector-emitter voltage measurements are performed by means of resistive voltage dividers. When more than three IGBTs are connected in series the measurement of the operating voltage of the master IGBT becomes difficult. For this reason, this method is limited to the series connection of three IGBTs.

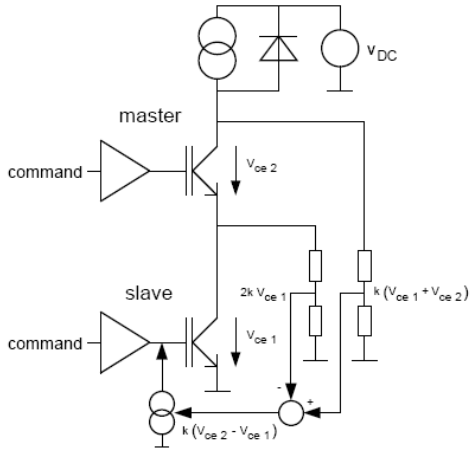


Figure 7-5: Master-Slave Voltage balancing method [GR-99b].

7.5 Reference voltage control method

[PA-95], [PA-04] present a closed loop collector-emitter voltage control. During the switch off process, before the collector-emitter voltage starts increasing, a considerable amount of charge has to be removed from the gate terminal. When this charge is removed the gate driver can control the collector-emitter voltage of the IGBT. Therefore, in order to achieve the controllability of the collector-emitter voltage, the collector reference voltage is applied with a step waveform before the voltage slope, Figure 7-6. During the step waveform time interval the IGBTs are desaturated and after that the IGBTs can follow the reference voltages of the IGBTs.

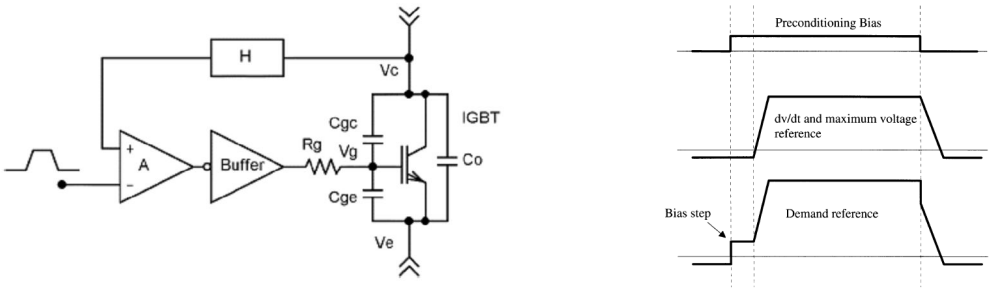


Figure 7-6: Closed loop control diagram. Reference voltage waveform [PA-95].

One of the main drawbacks of this control method resides on the switch on of the IGBT (switching inductive loads). While the free wheeling diode is forward biased it behaves as a short circuit. Therefore, any collector-emitter voltage change is caused by the stray inductances of the switching circuit. For a safe switch off of the diode, the voltage slope of the IGBT in the switch on should be low which causes high losses. When the diode is reversely biased it regains its blocking capability and the IGBT can follow the voltage reference of the gate driver.

The control circuit is formed by a high bandwidth operational amplifier and a current buffer. In order to ensure the control loop stability the use of a gate resistor is demanded. The Open Loop Transfer Function can be approximated assuming some simplifications and considering the gain of the Amplifier (k_{AOL}), the dominant pole of the Amplifier ($1/\tau_A$), the gate resistor (R_G), Miller capacitance (C_{GC}) and the feedback loop gain (α).

$$A_{OL}(s) \approx \frac{k_{AOL} \cdot \alpha}{R_G \cdot C_{GC} \cdot (\tau_A \cdot s + 1) \cdot s} \tag{7-3}$$

Due to the dominant pole of the Amplifier the control loop is not unconditionally stable. Consequently, the gains, gate resistor and Miller capacitance must be set to give the desired gain and phase margins.

7.6 Gate balancing Magnetic core method

[SA-04] present a method to balance the collector-emitter voltages equalizing the gate voltages of the series connected IGBTs. The gate driver circuits are coupled by means of a magnetic coil connected as shown in Figure 7-7.

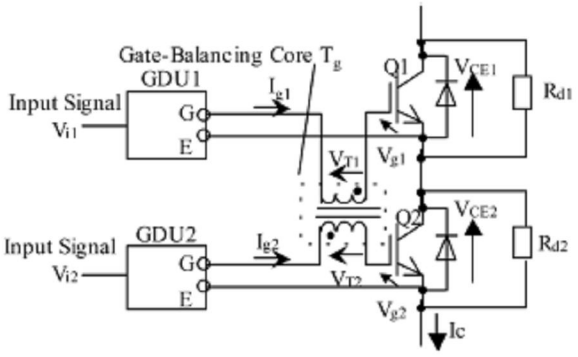


Figure 7-7: Magnetic coil based gate driver [SA-04].

Therefore, the proposed solution ensures that the gate voltages of the series connected IGBTs evolve similarly. If the connected IGBT characteristics are similar, a proper voltage balance can be achieved.

By means of a suitable coil design the gate currents can be equalized and in consequence the gate voltages. However, the coil should be designed taking into account the specific characteristics of the used IGBT. In addition, the stray inductances of the coil cause oscillations that must be dumped by means of gate resistors.

7.7 Discussion about the State of the Art of Voltage Balance Methods

The main problem related to the series connection of IGBTs is the voltage unbalance between the series connected IGBTs (chapter 6). There are several approaches that aim to solve this problem (chapter 7). The voltage unbalance problem is caused by the parameter differences of the IGBTs, therefore, a preselection of the used devices and gate drivers should minimize those problems [SH-06]. In addition, some additional circuitry should be added in order to guarantee the safe operation of the devices.

Table 7-1 shows a comparison between different approaches. This table has been extracted from [SH-06]. Reliability, complexity, balance quality, losses on the semiconductor and losses on the balance circuit are considered.

	Voltage Balance	**IGBT losses**	**Balancing circuit losses**	**Balancing circuit complexity**	**Reliability**
Snubber networks	Good	Low	Very High	Low	High
Clamp networks	Good	Very High	Low	Low	High
Gate signal delay control	Good	Moderate	Very Low	High	Low
Gate balancing core method	Good	Moderate	Low	High	Moderate
Reference voltage method	Good	Moderate	Low	Moderate	Moderate
Master Slave method	Good	Moderate	Low	High	Low

Table 7-1: Comparison of voltage balancing methods in series connected IGBTs.

Snubber networks are effective and reliable solutions to balance the voltages between series connected IGBTs, however, the increase on the overall power losses make them an unattractive solution.

Clamps are simple circuits that limit the maximum blocking voltage of any device. However, the extra losses generated when the IGBT operates in the active operating region make them unattractive to be used in High Power applications.

In general, most of the active gate control methods require a feedback loop for any controlled parameter (dV_{CE}/dt, overvoltage, etc). This loop must be designed attending the individual characteristics of the used IGBTs and the operating conditions.

Although these control methods are suitable to satisfy the basic requirements of the series connection of IGBTs (dV_{CE}/dt, synchronization, overvoltage), in general, they show problems like control loop stability, inefficiency on the power losses balance or even dependency on the operating conditions. In addition, when the IGBT is changed, the operating conditions are changed or additional functionalities are added (protections, limitations, etc) a new hardware must be designed in order to meet the needs of the application. This last one is probably the main reason that none of these solutions have been adopted as a standard solution to the problems related to the series connected IGBTs.

8 Active Gate Controller for the Series Connection of IGBT/Diodes

This chapter deals with the development of the gate driver for the series connection of IGBT/Diodes. Section 8.1 describes and discusses the reference active control technique used in this work. Section 8.2 details the requirements of the gate driver for the series connection while sections 8.3 and 8.4 shows how the reference active gate control technique has been changed to satisfy the needs of the series connection of IGBT/Diodes.

8.1 Reference active gate control technique discussion

There are several papers that propose active gate control methods to control the behaviour of the IGBT during the switching process (delay, overvoltage, voltage/current slope, etc) and in consequence, improve the voltage balance between series connected IGBTs. These methods are described in chapter 7.

Generally, most of the described active gate control methods are based on analogue control loops. These loops control the switch on and switch off process and protect the semiconductor device. Therefore, a parameter rich interaction between the IGBT device and the analogous functions of the driver takes place. In general, these drivers require the use of additional control circuitry with the main driver circuitry in order to achieve a specific functionality.

Different power semiconductor devices have unique properties and therefore, the analogue loops must be adjusted for each power semiconductor. This additional circuitry should be dimensioned attending the individual properties of the IGBTs and the operating conditions. In consequence, when the IGBT is changed by another with different characteristics or the operating conditions are changed, a new driver circuit with unique characteristics needs to be developed to satisfy the needs of the application. This is probably the main reason that makes the development of a universal gate driver difficult [BE-02].

The universal gate driver proposed by [LI-97] [BE-02] can adapt its behaviour to the individual IGBT properties, operating conditions and specific needs of the application modifying software parameters and maintaining always the same hardware circuitry. This driver is used to improve the switching losses of the IGBT in traction applications. In addition, it has some protection and limitation functions to reduce the switch off overvoltage, to reduce the reverse recovery current of the free wheeling diode and to protect the IGBT in case of a failure. Figure 8-1 shows an adaptation by [TH-03] of the universal gate driver proposed by [LI-97] [BE-02].

The driver uses an open loop control of the switching process. To that end, the switching process is divided in different time intervals (delay, dV_{CE}/dt, dI_C/dt, etc) and a pre-programmed constant gate current is applied to each time interval. As the IGBT is a charge controlled device during the switching, the use of current sources simplifies the control of the switching process to current levels and time. Applying a proper current level to each time interval (delay, dV_{CE}/dt, etc) the control of each individual magnitude is possible, Figure 8-1.

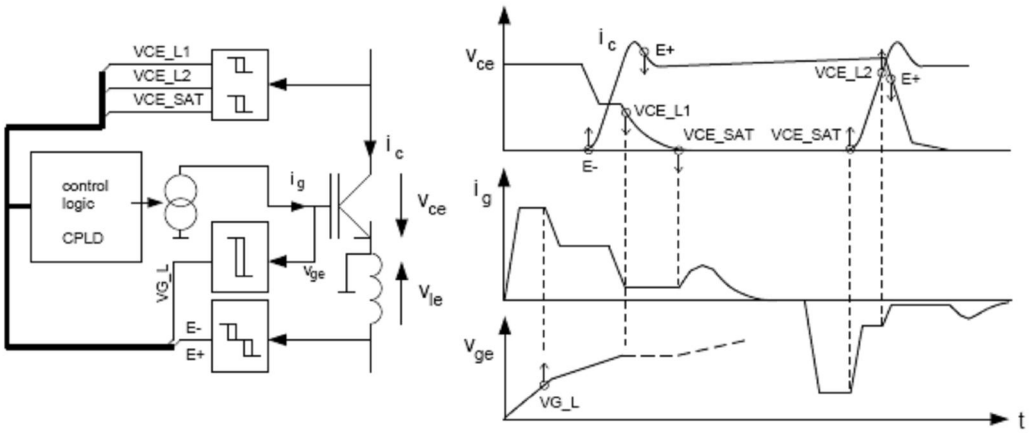


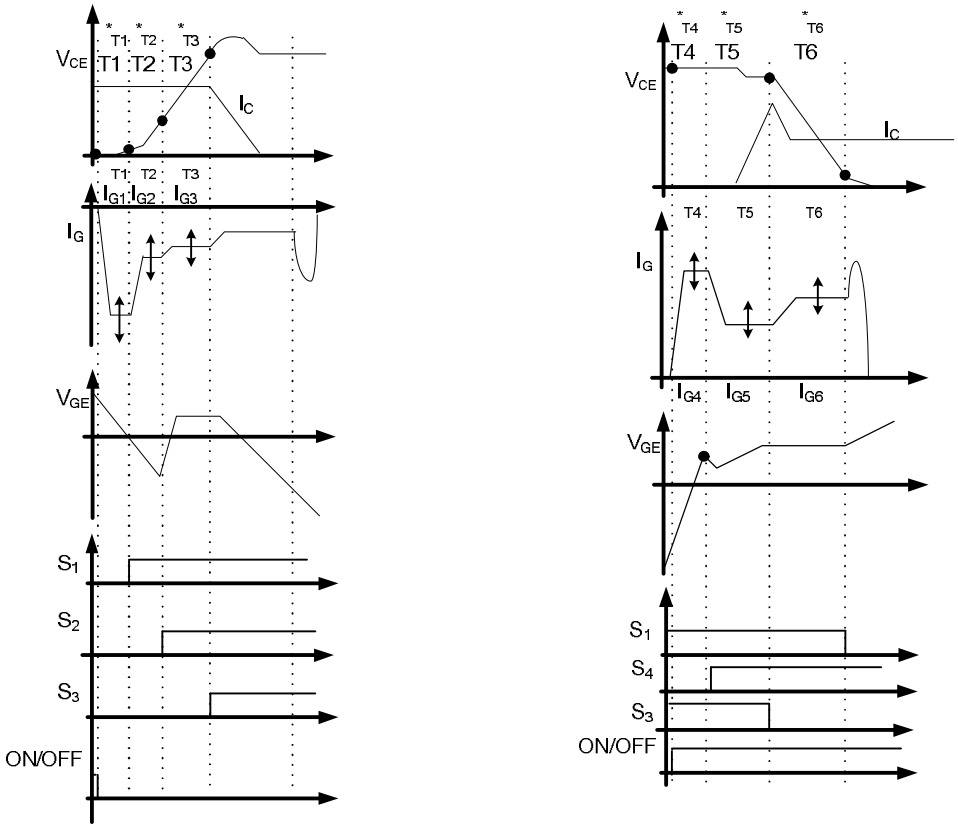
Figure 8-1: Block Diagram and operation waveforms [TH-03].

The proposed driver has three main parts: A control stage, a measurement stage and an output stage. The measurement stage measures the collector-emitter voltage, the gate voltage and the voltage between emitters (dI_C/dt). These measurements are compared with some reference values to determine if the measured value is higher or lower than a reference voltage (VG_L, E-, E+, VCE_L1, VCE_L2, VCE_SAT). This stage acts as an analog-digital converter. The control stage uses this digital information (VG_L, E-, etc) to determine in which time interval the switching process is and applies a pre-programmed constant gate current to each time interval. The output stage is composed by current sources that convert the digital output signal of the control stage (gate current reference) in a real gate current.

The switch on process begins with a high gate current in order to reduce the delay time. Once the gate threshold voltage is reached (VG_L) the gate current is reduced in order to avoid an excessive reverse recovery current of the diode and in consequence protect it. Once the collector-emitter voltage is lower than a certain voltage (VCE_L1) the driver applies another current to control the dV_{CE}/dt during the switch on.

Similarly, the switch off process begins with a high gate current level that reduces the switch off delay time. Once the IGBT is desaturated (VCE_SAT) the gate current is reduced to limit the voltage slope (dV_{CE}/dt). When the IGBT exceeds a VCE_L2 voltage the gate current is reduced to limit the dI_C/dt and therefore the overvoltage generated.

Even though the open loop control avoids an unstable behaviour during the switching process, an accurate characterization of the IGBT is required to program the control stage. Obviously, this is a disadvantage of this control proposal. In addition, some switching parameters depend on the operating temperature, the blocking voltage or even driver inaccuracies. In consequence, this control can not make sure that the switching speed of the IGBT is equal to some reference value at all operating conditions. Therefore, when several IGBTs are connected in series this control can not ensure that all devices will operate with the same voltage slope and at the same time instant.



(a) (b)

Figure 8-2: Switching off waveforms (a) and Switching on waveforms (b).

The control method proposed by [BO-05] can be implemented in this kind of gate driver. This method allows a stable and accurate control of the switching dynamics (especially the dV_{CE}/dt). Despite this control being designed to improve the switching losses and protect the IGBT, the ability to control accurately the voltage slope (dV_{CE}/dt) makes it a proper control method for series connection of IGBT devices.

This control method divides the switching process in several time intervals. Each time interval has a reference time duration and the driver modifies the applied gate current depending on the time difference (error) measured in the last switching between the desired

time duration and the obtained time duration. To achieve this, the control stage applies the proper gate current in each time interval and measures the time needed to finish each time interval. If the time length is higher than the reference value (too slow) the gate current (I_G) in this time interval is increased in one resolution unit (ΔI_G). If the time length is lower than the reference value (too fast) the gate current (I_G) is reduced in one resolution unit (ΔI_G). This process is repeated until a proper gate current which equals the measured time duration and the reference time duration is found, Figure 8-2.

Figure 8-2 shows typical switching waveforms of the IGBT. As mentioned above, the switching process is divided in several time intervals (T1 … T6) and a reference time duration is assigned to each time interval (t^*_{T1} … t^*_{T6}). During the switching process the driver detects the current time interval and applies the corresponding gate current (I_{G1} … I_{G6}). As a consequence, the duration of each time interval (t_{T1} … t_{T6}) is controlled. Table 8-1 shows the voltage levels compared by S1 … S4.

Comparator	Compared voltage level
S1	$\approx V_{CESAT}$
S2	$>> V_{CESAT}$
S3	$< V_{bus}$
S4	$\approx V_{GE(th)}$

Table 8-1: Compared voltage levels

As shown by Figure 8-2 the **T1 time interval** starts when the gate driver recives the “off” signal and finishes when the IGBT starts to desaturate. At this moment the S1 comparator changes its output value from a low logic value to a high logic value. The amount of charges to be extracted in this time interval depends not only on the applied gate current but depends also on the collector current, the transfer characteristic and the input capacitance of the IGBT (6-3). Therefore, the control of the moment when the IGBT starts desaturating is not possible if only the error measured in the last switching process is taken into account. Consequently, the synchronous switching between the series connected IGBTs can not be guaranteed.

The **T2 time interval** starts when the S1 comparator changes its output from a low logic value to a high logic value and finishes when the collector-emitter voltage reaches a voltage level notoriously higher than the saturation voltage. At the beginning of this time interval the C_{GC} capacitance has a large value due to the polarity inversion in the gate region (chapter 3.3.2). At the end of this time interval the value of the C_{GC} capacitance should decrease to its nominal value. This involves that during this time interval the collector-emitter voltage for the applied gate current (I_{G2}) should present two different slopes. The gate driver detects the end of this time interval by a change on the output logic state of the S2 comparator.

During the **T3 time interval** a collector-emitter voltage slope (dV_{CE}/dt) is measured. This time interval starts when the S2 comparator changes its output to a high logic value and finishes

when the collector-emitter voltage is close to the operating voltage of the IGBT. This event is measured by a change at the output level of the S3 comparator. As mentioned in chapter 5, the dV_{CE}/dt is determined mainly by the applied gate current (I_{G3}) and the gate-collector capacitance (C_{GC}). If the gate current is controlled the time to inject/extract the required gate charges can be controlled and in consequence, the dV_{CE}/dt can also be controlled, (5-19). We should note that the gate driver estimates the voltage slope measuring the time (t_{T3}) needed by the collector-emitter voltage changing from the collector-emitter voltage level measured by S2 to the collector-emitter voltage level measured by S3.

In general, for a given gate current, the switching process is faster when the IGBT operates in colder temperatures. In pulsed mode applications the IGBT usually operates at frequencies from some hundred hertz to several kilohertz. Assuming the operating conditions (as the junction temperature) change slowly, small changes in the gate current (ΔI_G) are enough to obtain a desired dV_{CE}/dt. In addition, due to the small gate current increments, the control of the voltage slope in a stable and accurate way is possible. Consequently, equal voltage slopes can be obtained between the series connected IGBTs easily. This behaviour is a notorious advantage of this control technique.

During the switch off process of the IGBT (Figure 8-2) an overvoltage can be observed caused by the collector current variation across the stray inductance of the power circuit. A fast switching leads to low power losses, however the overvoltage can exceed the maximum blocking voltage of the IGBT and in consequence cause the failure of the device.

As proposed by [TH-03] [LI-97], for simplification purposes, the limitation of the dI_C/dt can be done indirectly by monitoring the collector-emitter voltage (V_{CE}) of the IGBT. As shown in Figure 8-2, when the gate driver detects that the collector-emitter voltage exceeds a certain limit, the gate current decreases, the dI_C/dt is reduced (equation (5-20)) and consequently the overvoltage is reduced during the switch off.

This method is suitable to be used in series connected devices. Even though the proposed control can achieve a similar behaviour for each series connected IGBT, inevitably, there will be some differences between the different voltage slopes and switching instants. Once the IGBT exceeds a certain collector-emitter voltage (V_{CE}) the voltage slope can be reduced so that the fastest IGBTs waits for the slowest IGBTs. This way, the voltage balance between the series connected IGBTs can be improved, Figure 8-3.

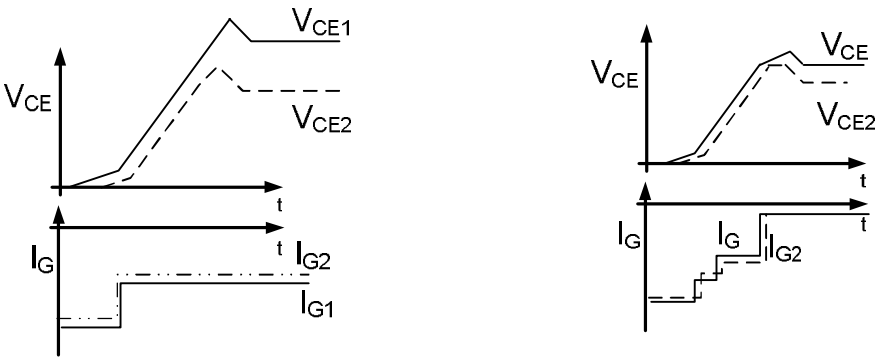


Figure 8-3: Switch off of series connected IGBTs without overvoltage limitation (left) and with overvoltage limitation (right).

In addition, clamp circuits and static voltage balance circuits are needed to improve the voltage balance during the switch off blocking state. Chapter 8.4.4 describes both functionalities.

The switch on process starts when the gate driver recives the “on” signal. This is the beginning of the **T4 time interval**. This time interval finishes when the gate-emitter voltage is close to the gate threshold voltage of the IGBT (S4 changes to a high output logic level). As the gate voltage during this time interval remains lower than the gate threshold voltage, there is not any collector current flowing across the IGBT and in consequence the collector-emitter voltage remains constant. We should note that this time interval is a pure delay whose duration (t_{T4}) depends on the gate current (I_{G4}) and the amount of charges to be injected. The measured gate voltage (V_{GE}) depends on the internal gate voltage (V_{CGE}) and the voltage drop caused by the gate current on the internal gate resistor (8-1). This is why the actual gate voltage in the IGBT chip is not known.

$$V_{GE} = I_G \cdot R_g + V_{CGE} \tag{8-1}$$

The value of this internal gate resistor is strongly dependent on the silicon doping level and the operating temperature [JO-01]. In consequence, for the same input capacitance and the same gate current, the measurement of different gate voltages due to differences on the value of this resistance is possible. Therefore, the control of the T4 time interval is not enough to ensure the synchronization of the IGBTs during the switching on process.

The universal gate driver proposed by [LI-97] [BE-02] considers that the **T5 time interval** starts when the gate threshold voltage is exceeded and finishes when the collector-emitter voltage starts falling, Figure 8-1. The control proposed by [BO-05] considers that this time interval finishes when the driver detects a change in the collector current (existence of a dI_C/dt). When the gate driver controls a single IGBT this control method is suitable to control the

instant when the collector current changes. However, when several IGBTs are connected in series this control is not suitable to synchronize them. The reason for this is that each driver will detect the change in the collector-current when the slower IGBT has reached the gate threshold voltage ($V_{GE(th)}$). In consequence, the faster IGBT can not control the gate current in this T5 time instant. This is the reason why this control is not suitable to synchronize series connected IGBTs.

At the end of this time interval (T5) a collector current (I_C) equal to the load current must go across the IGBT. As the collector current can change from one switching to another, the amount of injected charges during this time interval can vary (Q_{T5}) from one switching to another, (8-2). Therefore, the gate current (I_{G5}) applied during this time interval will vary if the collector current changes.

$$Q_{T5} \approx Q_{dI_C/dt} \approx C_{iss} \cdot \sqrt{\frac{I_C}{k}} \tag{8-2}$$

During the **T6 time interval** the collector-emitter voltage falls to the saturation level. The collector-emitter voltage slope is controlled by the gate current (I_{G6}), see equation (5-19). This time interval is detected by S1 and S3 comparators. The gate driver estimates the voltage slope measuring the time (t_{T6}) needed by the collector-emitter voltage changing from the collector-emitter voltage level measured by S3 to the collector-emitter voltage level measured by S1.

Consequently, this control alows to control the voltage slope (dV_{CE}/dt) in a simple and stable way which is necessary to ensure the voltage balance between the series connected IGBTs. However, as described above, this method is not able to ensure a synchronous switch off between the series connected devices when the load varies from one switching to another.

In this context, the rest of this chapter describes the proposed active gate control method focusing on the series connection of IGBTs.

8.2 Requirements of the active gate control

The implemented active gate control has to control the switching process in order to achieve a similar behaviour for all the series connected IGBT devices. Therefore, the driver has to ensure that the voltage slope (dV_{CE}/dt) is the same independently of the operating conditions of the IGBT. In addition, it has to guarantee that this voltage slope occurs at the same time instant for all the series connected devices. If these conditions are satisfied all the series connected IGBTs can share out the bus voltage properly (assuming equal tail currents, leakage currents and diode characteristics).

Additionally, the gate driver must guarantee the protection of the free wheeling diode during its switch off, the protection of the IGBT during the switch off or when a failure occurs.

We should note that when the switching valve operates as free-wheeling diode, the voltage balance depends on the recovery characteristics of the diodes. In this case, the driver can not act on the dV_{CE}/dt to achieve a voltage balance because it does not have influence over the switch off behaviour of the diode. However, the driver should limit the collector-emitter voltage by means of clamp functionality. [LI-04], [SG] demonstrate the validity of the clamping functionality to balance the voltage between series connected diodes without using snubber networks.

8.3 Description of the proposed gate driver

The developed gate driver is based on the universal gate driver proposed by [LI-97]. This driver has a measurement stage, a control stage and an output stage that sets the gate current determined by the control stage, Figure 8-4 (a).

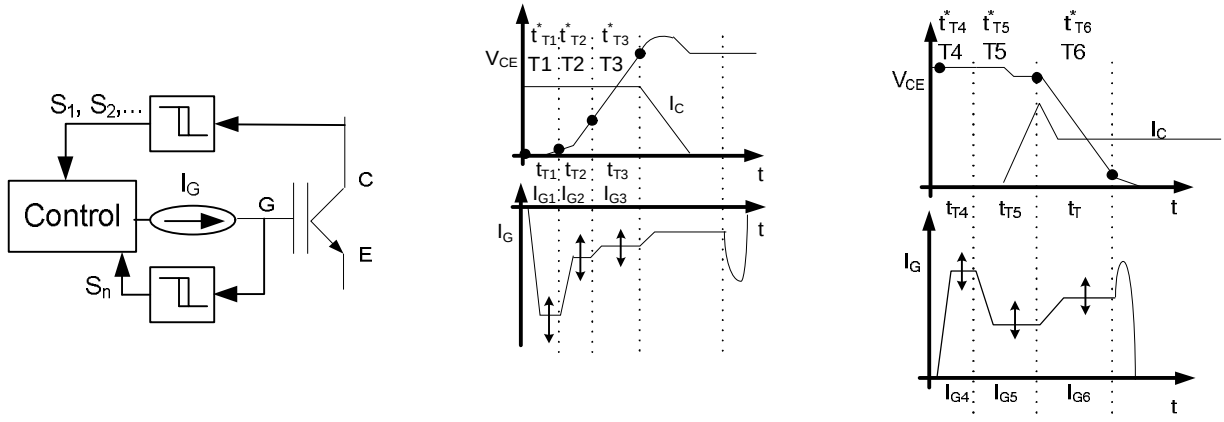


Figure 8-4: Simplified gate diagram and events sequences during the switching process.

The measurement stage obtains the collector-emitter voltage (V_{CE}) and the gate voltage (V_{GE}). Each measurement is compared with a reference value. Consequently, the information provided by the measurement stage denotes if the measured variable is higher or lower than a reference value (1 bit Analog Digital converter). Figure 8-2 shows the signal sequence provided by the measurement stage during the switching process (S_1 … S_4).

The control stage uses the digital information given by the measurement stage to determine in which time interval of the switching process the IGBT operates. A gate current (I_G) is assigned to each time interval (T1, T2…T6 in Figure 8-4). This way, each magnitude of the switching process (dI_C/dt, dV_{CE}/dt, overvoltage, etc) can be independently controlled. The control stage is composed by a FPGA where the current initialization and the switching behaviour control are programmed. The operating frequency of the FPGA is 50 MHz (20 ns).

The output stage is composed basically by constant current sources. Each current source is activated by the control stage. Consequently, the digital outputs of the FPGA are converted to gate current depending on the amount of activated current sources (Digital Analog converter). The developed gate driver can operate with (approximately) ± 6.5 A and a current resolution of (approximately) 15 mA. In theory, by means of this gate current the driver can control the gate charge profile independently from the IGBT characteristics or the operating conditions.

8.4 Control strategy of the switching process in series connected IGBTs

As described in previous sections, the control method used by [BO-05] to control the switching process modifies the gate current of each time interval depending on the error measured in the last switching. This process is repeated until the selected gate current (I_G) makes the time interval duration similar to a given reference duration.

During the switching process, there are some time intervals (especially the ones related to dV_{CE}/dt during the switch off) where this control method is very suitable because their duration depends mainly on the applied gate current, (chapter 5). However, there are other time intervals (delay during the switch off, dI_C/dt during the switch on) where the amount of charges injected to/ extracted from the gate terminal to obtain a determined time duration depends on the gate current and other parameters as the collector current (I_C), (chapter 6). Consequently, if the collector current changes from one switching to another, the computed gate current during the last switchings will not satisfy the time requirements for these time intervals.

In a High Voltage switching valve composed by series connected IGBTs all devices should operate with the same voltage slope (dV_{CE}/dt) and at the same instant (synchronization). If a voltage unbalance or an excessive overvoltage is detected, the driver must be able to clamp and improve the voltage balance between series connected devices.

There are characteristics than can not be controlled by means of the gate terminal (tail current, reverse recovery current, leakage current, etc) that have influence on the voltage balance of the series connected IGBTs. Without any doubt, the preselection of matched IGBT devices can minimize this problem. However, the gate driver should include clamp circuitry to limit the maximum blocking voltage of each device.

This chapter describes how the control proposed by [LI-97], [BE-02] has been modified to satisfy the needs of the series connection. In addition, as the implemented control is digital, the resolution and accuracy limits are also discussed.

8.4.1 Accuracy of the proposed control

As described above, the implemented digital control measures the time duration of each time interval and changes the gate current in a resolution unit. Because the current resolution is limited (15 mA), the deviations of each time interval that can be obtained are finite. The duration of each time interval (delay, dV_{CE}/dt, etc) depends on the extracted amount of charges and the applied gate current, (8-3).

$$t = \frac{Q_G}{I_G} \tag{8-3}$$

When the applied gate current does not cancel out the error, the gate driver modifies the applied gate current in one resolution unit. The time increment (Δt) achievable depends on the charge associated to the time interval (Q_G), the current applied in the last switching (I_G) and the applied current increase (ΔI_G), (8-4).

$$\Delta t = \frac{-Q_G \cdot \Delta I_G}{I_G \cdot (I_G + \Delta I_G)} \tag{8-4}$$

From equation (8-4) we can deduce the time increment produced by a gate current variation for a given gate charge. The minimum required current resolution can be obtained depending on the IGBT characteristics and the needed accuracy.

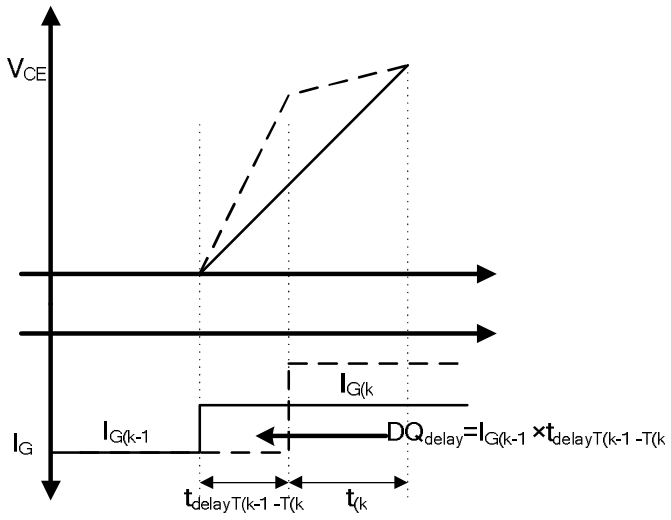


Figure 8-5: Effect of the delay on the switching. Effect of the time delay (line) and zero time delay (dashed line).

There is another characteristic that has a notable influence on the proposed control. This characteristic is the total delay measured since a time interval change condition is given to the gate current changes. As shown in Figure 8-5, when the time interval change conditions are

satisfied the driver needs certain time (mainly caused by control and output stages) to change the gate current from the previous time interval to the gate current needed for the new time interval.

If the amount of the extracted/injected charge by the previous time interval's gate current ($_{IG(k-1)}$. $t_{delayT(k-1)-T(k)}$) is negligible with respect to the charge of the actual time interval (Q_G) there is not any problem from the control point of view. However, if this charge ($_{IG(k-1)}$. $t_{delayT(k-1)-T(k)}$) is negligible, the required gate current in the actual time interval (I_k) can be considerably different from the one needed in the case of a constant gate current was applied in all the time interval, Figure 8-5.

$$t_{(k)} = \frac{Q_G - I_{G(k-\mathbf{1})} \cdot t_{delayT(k-\mathbf{1})-T(k)}}{I_{G(k)}} \tag{8-5}$$

This fact gains importance especially when the gate current applied in a time interval ($I_{G(k)}$) is very different from the current applied in the previous time interval ($I_{G(k-1)}$) and the gate charge in the current time interval is low.

In addition, the tolerances and inaccuracies of the measurement stage also influence the detection of time intervals and therefore on the voltage balance of the IGBTs. In consequence, the matching of all the measurement circuits and reference values with the used gate drivers is important.

8.4.2 Synchronization during the switch off process

In order to ensure that all devices inside a switching valve operate properly, all of them need to have the same dV_{CE}/dt at the same instant. This is especially important during the switch off process because too big a synchronization error could lead to High Voltage unbalances and in consequence to higher electrical and thermal stress in some devices.

One of the limitations of the active gate control proposed by [BO-05] to ensure that all devices operate synchronously resides in the difficulty to control the duration of the T1 time interval (Figure 8-4) using only the error measured in the last switching. This is especially true when the collector current (I_C) changes from one switching to another (chapters 6.2 and 8.1).

Consequently, if the collector required current (I_C) is unknown at the beginning of the switch off process, the control of the duration of the T1 time interval is not possible, Figure 8-2. Therefore, the control can not make that the end of the T3 time interval takes place at the same instant for all series connected IGBTs. In order to get a synchronous switching, the duration of T1 plus T2 time intervals must be always constant (Figure 8-4).

In [BO-07], a method is proposed to estimate the collector current depending on the time that the IGBT needs to reach the desaturation (end of T1 time interval Figure 8-4) for a constant gate current. As the amount of the extracted charge from the gate terminal depends on the collector current (Figure 6-2), the duration of this time interval for a given constant gate current is an image of the extracted charge and therefore, an image of the collector current. This idea could be used to synchronize all the series connected IGBTs during the switch off process.

During the T1 time interval a constant gate current can be applied to measure the duration of this time interval. Depending on the measured time (t_{T1}), the gate current applied on the T2 time interval ($I_{G\_T2\_n}$) can be controlled in order to that the total duration since the switch off signal is received until the end of the T2 time interval will be constant. Therefore, in a time ($t_{T1} + t_{T2}$) since the switch off signal is received the collector-emitter voltage of all the series connected IGBTs will be the same, Figure 8-6.

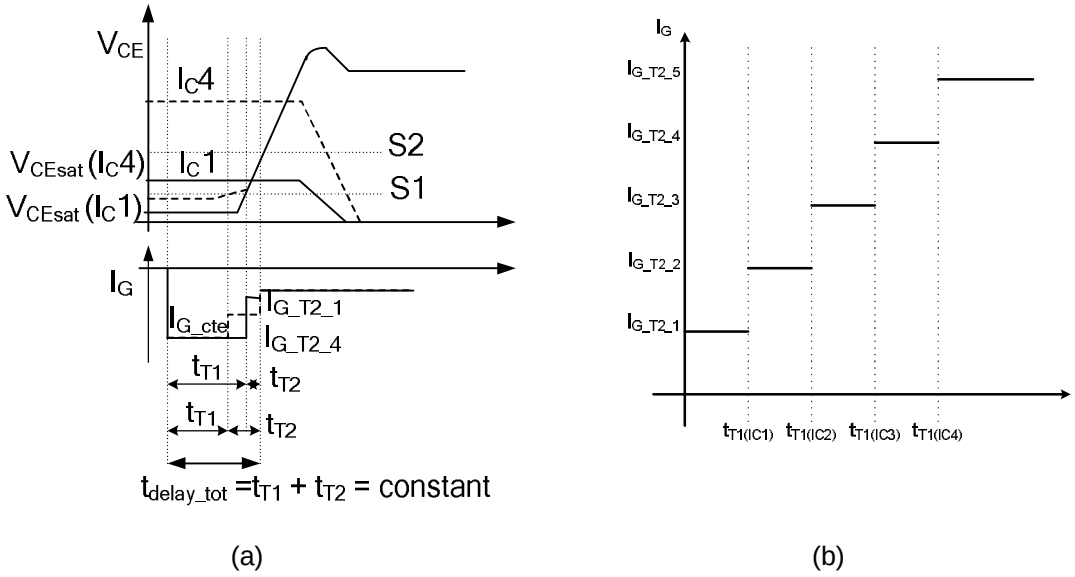


Figure 8-6: Synchronization method during the switch off process (a) and T2 time interval gate current selection criteria (b).

As shown by Table 8-2 and Figure 8-6 (b), depending on the duration of the T1 time interval (t_{T1}), different gate currents ($I_{G\_T2\_n}$) could be applied during T2 time interval in order to make the duration of T1 plus T2 time intervals constant ($t_{T1} + t_{T2}$).

t_{T1} Range	Applied Gate Current
$[0,t_{T1(IC1)}]$	$I_{G\_T2\_1}$
$(t_{T1(IC1)},t_{T1(IC2)}]$	$I_{G\_T2\_2}$
$(t_{T1(IC2)},t_{T1(IC3)}]$	$I_{G\_T2\_3}$
$(t_{T1(IC3)},t_{T1(IC4)}]$	$I_{G\_T2\_4}$
$(t_{T1(IC4)},\infty]$	$I_{G\_T2\_5}$

Table 8-2: T2 time interval gate current selection criteria.

8.4.3 Synchronization during the switch on process

During the switch on process all IGBTs must reach the gate threshold voltage ($V_{GE(th)}$) at the same instant. In consequence, all IGBTs start becoming conductor at the same instant and therefore a voltage unbalance is avoided during the switch on process, Figure 6-3.

The gate driver controls the duration of T4 time interval modifying the gate current until the time requirements of this interval are satisfied. This time interval (T4) finishes when the gate voltage reaches a value close to the threshold voltage of the IGBT (S4 in Figure 8-2). As described in chapter 8.1 the gate voltage (V_{GE}) depends on the internal gate voltage (V_{CGE}) and the voltage drop caused by the gate current on the internal gate resistor (8-1). This is the reason why the actual gate voltage in the IGBT chip is not known and consequently it is not possible to ensure that the series connected IGBTs will reach their threshold voltage synchronously.

This problem can be overcome controlling the duration of the T5 time interval (Figure 8-4). Although the gate threshold voltage is not reached at the same instant ($V_{GE(th)}$), the collector-emitter voltage at the end of the T5 time interval should be the same for all series connected devices (synchronization during switch on).

Although the results obtained with this control method have been satisfactory, the control could be improved if different gate currents were applied depending on the load current. Instead of using a current sensor, the global controller (converter controller) could report the load current to each individual driver at the beginning of the switch on process. In consequence, each individual driver could apply different gate currents as a function of the load current as shown in section 8.4.2.

During this time interval the free wheeling diode is switched off, so it is convenient to limit its reverse recovery current. As there is not any current measurement, the dI_C/dt can be limited controlling the duration of this time interval.

8.4.4 Voltage clamping and blocking state voltage balance

During the last stage of the switch off process of the IGBT there exists an overvoltage caused by the current slope (dI_C/dt) across the stray inductance of the power circuit. Before the collector current is extinguished, there is a tail current caused by the recombination of charge carriers to the p doped region. This current can not be controlled by the gate terminal. If the tail currents of the series connected IGBTs are equal, there should not be any voltage unbalance problem. However, it is possible to find different tail current behaviours that cause voltage unbalances between series connected IGBTs.

The equivalent output capacitance (C_{eq}) of the IGBT with lower tail current is charged with the differential tail current (ΔI). This phenomenon causes voltage unbalances between series connected IGBTs, Figure 8-7. As section 10.2.1a) will show, this persists for a long time after the collector current extinction.

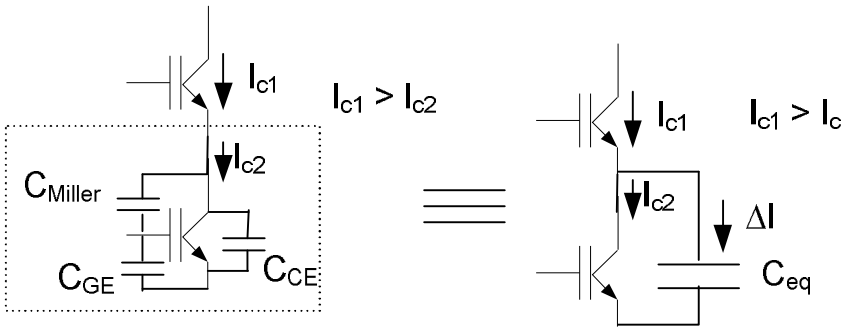


Figure 8-7: Charging process of the equivalent output capacitance.

Different switching dynamics (dV_{CE}/dt), asynchronous switchings (Δt) or different reverse recovery charges (Q_R) of the diodes are some other causes that have a negative influence on the voltage balance. When the antiparallel diodes inside the switching valve are conductors, the same current circulates across all of them. When those diodes are switched off, different reverse recovery charge characteristics lead to an unbalanced voltage distribution, Figure 8-8. The diodes with less recovery charges withstand higher voltages (in general they present higher dV_{CE}/dt). Therefore, some diodes may exceed their maximum reverse blocking voltage. Additionally, there is an unbalanced distribution of switching losses.

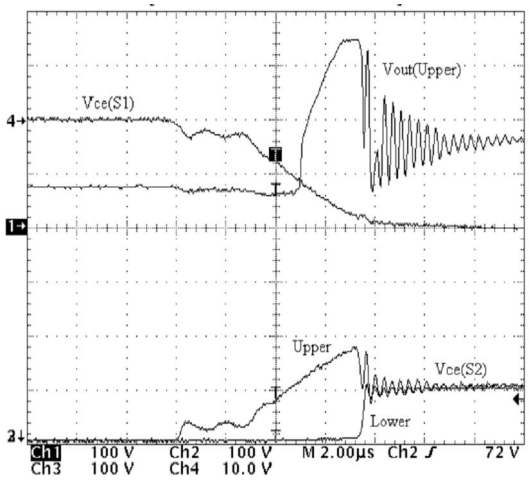


Figure 8-8: Voltage clamping in two series connected diodes [LI-04].

In this case, as mentioned before, the behaviour of the diode can not be controlled by means of the gate terminal and the driver circuit action is limited to clamp the maximum blocking voltage of the IGBT/Diode. This clamping function can be achieved by means of active gate control techniques (making the IGBT conductor) or by means of additional circuitry (in parallel

with the IGBT/diode). [TH-03] proposes the collector current control of the IGBT to control the differences in the reverse recovery currents. However, the difficulty to control this current makes this approach unattractive. The validity of the clamp circuit is shown in chapter 10.

During the blocking state, different leakage currents lead to voltage unbalances between the series connected IGBT / Diodes. The steady state voltage balance is achieved easily by means of voltage sharing resistors, chapter 6.

9 Simulation Results

In the following chapter the proposed control is validated by means of simulation results (chapter 9.1). Additionally, its validity is shown for voltage balance of series connected IGBTs (chapter 9.2).

9.1 Validation of the proposed active gate control

The active gate control described in chapter 8 has been simulated in the circuit shown by Figure 9-1. The considered IGBT model has an input capacitance of 30 nF while the reverse transfer capacitance is about 1 nF. The internal gate resistor is about 0.5 Ω. The collector current varies between 0 and 200 A and the bus voltage is 1000 V. As described in section 8.3 the control stage is based on a FPGA that operates at 50 MHz. Consequently the measurable time resolution is 20 ns per clock pulse.

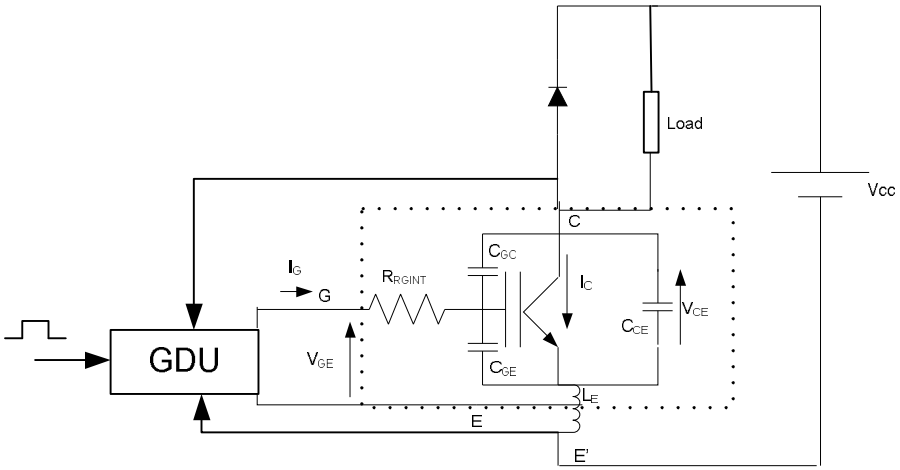
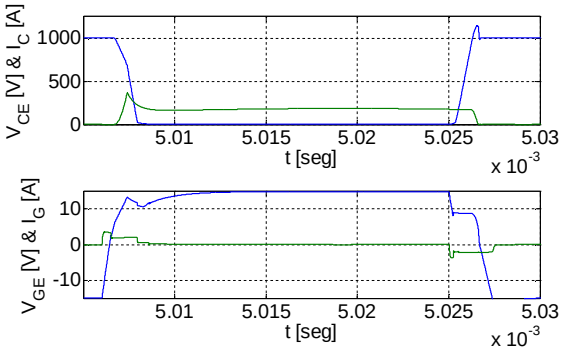
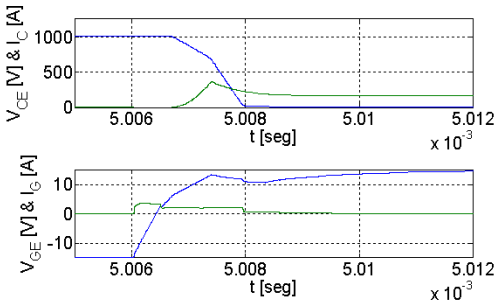


Figure 9-1: Test circuit.

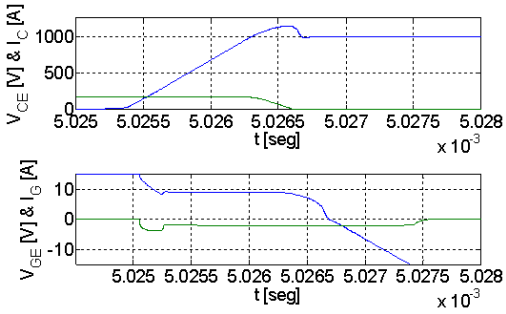
Figure 9-2 shows the obtained waveforms during the switching process of the IGBT at the switch on and the switch off. This plot shows the gate current (I_G), the gate voltage (V_{GE}), the collector current (I_C) and the collector-emitter voltage (V_{CE}).



(a)



(b)



(c)

Figure 9-2: Switching waveforms during the switching: V_{CE}, I_C, V_{GE} and I_G (a), switch on waveform detail (b) and switch off waveform detail (c)

The driver divides the switch on process in three different time intervals: T4, T5 and T6, Figure 8-4. T4 time interval begins when a switch on signal is received and finishes when the gate voltage reaches the gate threshold voltage (approximately). This time interval can be considered a simple delay time during the switch on process of the IGBT. The duration of the T4 time interval reference for these simulations is 500 ns (25 clock pulses).

T5 time interval begins when the IGBT reaches the gate threshold voltage and finishes when the collector-emitter voltage reaches 750 volts (approximately). During this time interval

the collector current begins growing. The duration of the T5 time interval reference for these simulations is 600 ns (30 clock pulses).

Finally, T6 time interval begins when the collector-emitter voltage is lower than 720 volts and finishes when the IGBT reaches the saturation voltage. During this time interval, the collector-emitter voltage falls causing the Miller effect. The duration of the T6 time interval reference for these simulations is 600 ns (30 clock pulses).

During the simulation, collector current varies from one switching to another switching. This has an important influence especially in T5 time interval. Figure 9-3 shows the obtained results where the duration of each time interval can be observed.

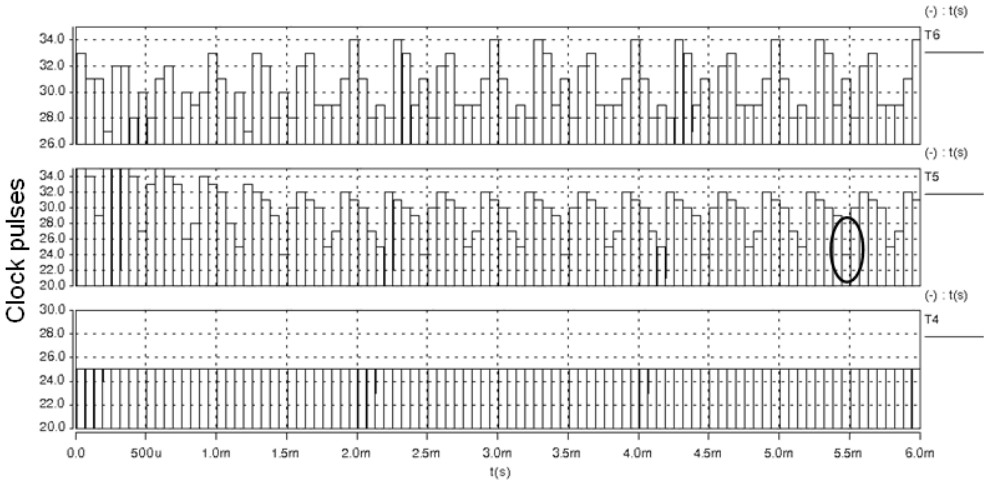


Figure 9-3: (Clock pulses) Duration of switching on time intervals in the IGBT

Some facts in figure: the duration of the T4 time interval is equal to the reference time (25 clock pulses – 500 ns). The duration of T5 and T6 time intervals is close to the reference time (30 clock pulses). In some switchings this time is quite different from the reference time (up to 120 ns, rounded in Figure 9-3) due to the variation of the collector current. In order to improve the accuracy in this time interval, a measurement of the switched collector current can be used. In consequence, depending on the collector current the driver can act in one way or another. Because of its complexity, this idea has not been implemented in this work. In addition, as shown in section 9.2, this behaviour does not have too negative an influence on the voltage balance of series connected IGBTs.

Similarly, the control divides the switch off process in three different time intervals: T1, T2 and T3, Figure 8-4. T1 time interval begins when the driver receives the switch off signal and finishes when the IGBT reaches the desaturation voltage ($V_{CE} \approx 10$ volts). This time interval can be considered a simple delay. The time reference for these simulations is between 220 ns (11 clock pulses) and 380 ns (19 clock pulses).

T2 time interval begins when the IGBT reaches the desaturation ($V_{CE} \approx 10$ volts) and ends when the collector-emitter voltage reaches 100 volts (approximately). The control stage must control the switching process to ensure a total duration for ($t_{T1} + t_{T2}$) of 560 ns (28 clock pulses). Finally, T3 time interval begins when the collector-emitter voltage exceeds 100 volts and ends when the collector-emitter voltage reaches 720 volts. The duration of the T2 time interval reference for these simulations is 700 ns (35 clock pulses).

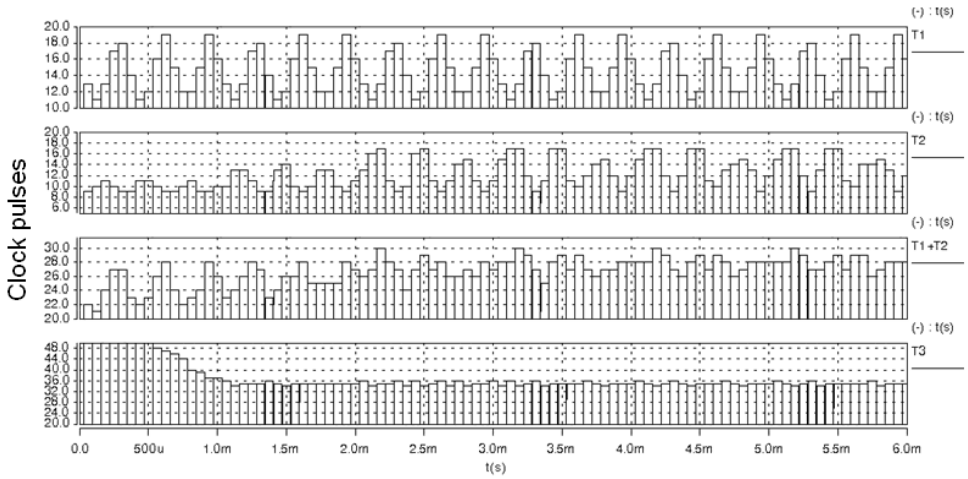


Figure 9-4: (Clock pulses) Duration of switching off time intervals of the IGBT.

As described in chapter 8, Figure 9-4 shows the changes in the duration of T1 time interval depending on the collector current for a given constant gate current. Depending on the duration of this time interval different gate currents are applied during the T2 time interval to get a constant duration for T1 + T2 time intervals. As it can be seen, the driver manages properly the gate current to achieve the required time duration until reach 100 volts. The duration of T3 time interval is close 35 clock pulses (700 ns) as desired.

9.2 Series connection of IGBT/Diode-s

In this section some simulation results are shown in order to validate the proposed active gate control for the series connection of IGBT / Diode devices. Therefore, section 9.2.1 shows the behaviour of the proposed gate control in series connection of two IGBTs, section 9.2.2 of four IGBTs and section 9.2.3 of two free wheeling diodes.

9.2.1 Series connection of two IGBTs

In order to validate the proposed active gate control for series connection of IGBTs some simulations have been performed in the circuit shown in Figure 9-5. In order to cause some voltage unbalances, additional capacitances (some nanofarads) have been added in one of the IGBTs. Both IGBTs must operate with voltage slopes about 1 V/nsec. The static voltage

balance is achieved by means of a resistive voltage divider while the dynamic voltage sharing is achieved by means of the proposed gate control.

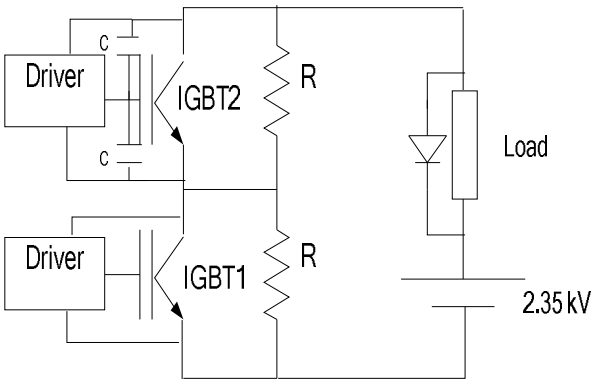
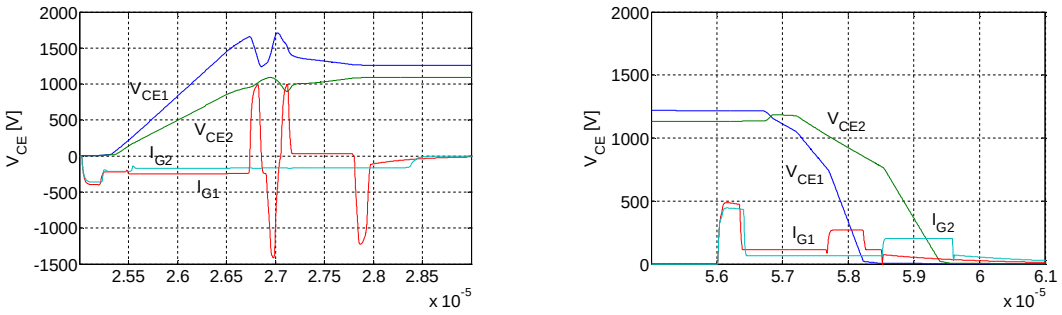


Figure 9-5: Test circuit for series connected IGBTs.

Figure 9-6 shows the first switching waveforms where the voltage unbalance (V_{CE}) can be observed. The voltage unbalance is caused by an asynchronous switching and different voltage slopes. For these simulations, an active clamp circuit has been used to limit the operating voltage of the IGBT to approximately 1500 volts.



(a) (b)

Figure 9-6: Voltage unbalances during switch off (a) and switch on (b) processes in the start-up of the active gate control.

Figure 9-7 shows the effectiveness of the proposed active gate control. After the control has reached reached a steady state, the modified gate currents (I_G) allow to obtain similar voltage slopes (dV_{CE}/dt) as well as synchronous switchings.

The switch off process of both series connected IGBTs may be observed in Figure 9-7. Both IGBTs operate with similar voltage slopes and similar switching instants. In consequence, the voltage balance is ensured during the switch off.

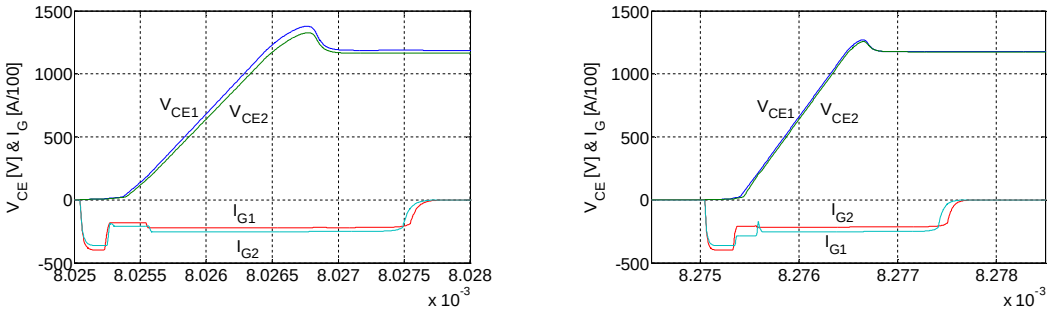
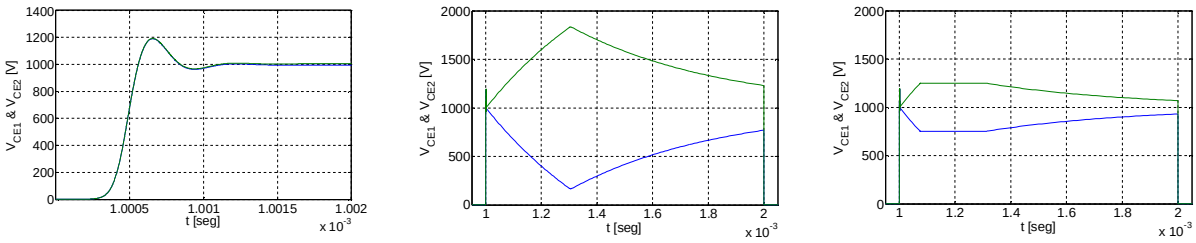


Figure 9-7: Balanced switch off processes of two series connected IGBTs in the steady state of the control.

After the end of the switch off process there is a voltage unbalance due to tail current differences. Figure 9-8 shows that in spite of the transient behaviour of the IGBTs is the same during the switch off process, Figure 9-8 (a), tail current differences cause strong voltage unbalances between the series connected IGBTs, Figure 9-8 (b). This unbalance obliges to design proper clamping circuitry to limit this uncontrolled behaviour, Figure 9-8 (c).



(a) (b) (c)

Figure 9-8: Balanced transient voltages of two series connected IGBTs (a), effect of tail current differences on the voltage balance (b), effect of clamping circuits on voltage unbalances (c).

Figure 9-9 shows the switch on process of two series connected IGBTs where the proposed active gate control achieves a proper voltage balance.

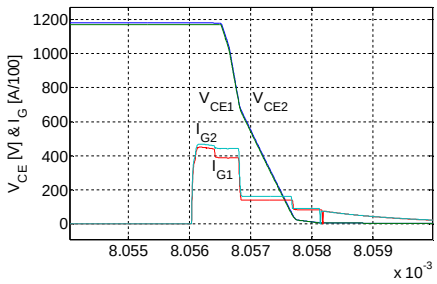


Figure 9-9: Switch on of two series connected IGBTs

9.2.2 Series connection of four IGBTs

As shown by Figure 9-10, in this section, four IGBTs are connected in series. To cause parameter deviations between the connected IGBTs, different interelectrode capacitances and internal gate resistors are added.

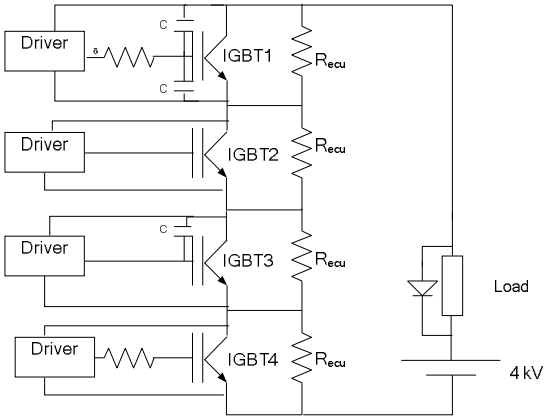


Figure 9-10: Simulation circuit

As shown by Figure 9-11, during the initial switchings, all the IGBTs operate with different voltage slopes and asynchronously.

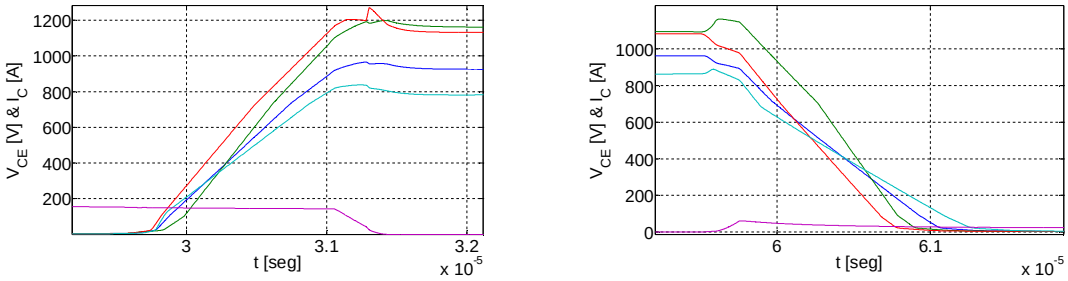


Figure 9-11: Unbalanced switch off and switch on waveforms in the initial stages of the active gate control

Figure 9-12 shows the effectiveness of the proposed active gate control. After some switchings, the gate current (I_G) is modified to obtain similar voltage slopes (dV_{CE}/dt) as well as synchronous switchings.

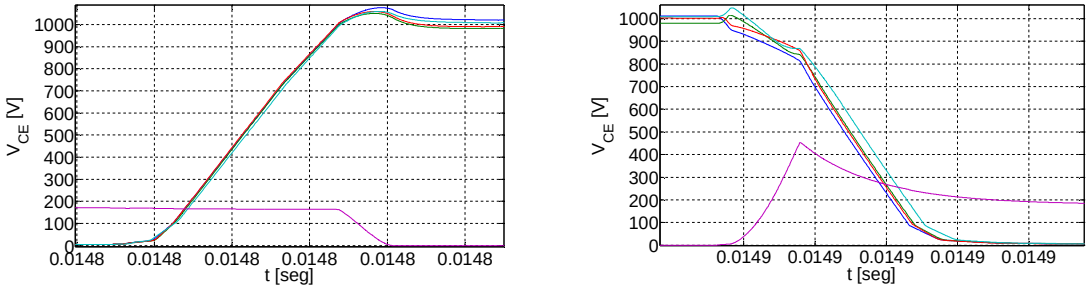


Figure 9-12: Balanced switch off and switch on waveforms.

9.2.3 Voltage balance of series connected diodes

When IGBTs are connected in series in a voltage source converter, inevitably, free wheeling diodes are also connected in series.

During the switch off process, these diodes acts as unmatched “current sources” and in consequence voltage unbalances appear. Although a clamping circuit can limit the maximum blocking voltage, it does not balance the switching losses.

Figure 9-13 shows the switch off waveforms of two series connected IGBT/Diode devices with and without a small RC snubber network (4 Ω, 30 nF). One of the diodes has a reverse recovery charge of 220 μCs and a reverse recovery current of 325 A. The other diode has a reverse recovery charge of 325 μCs and a reverse recovery current of 300 A.

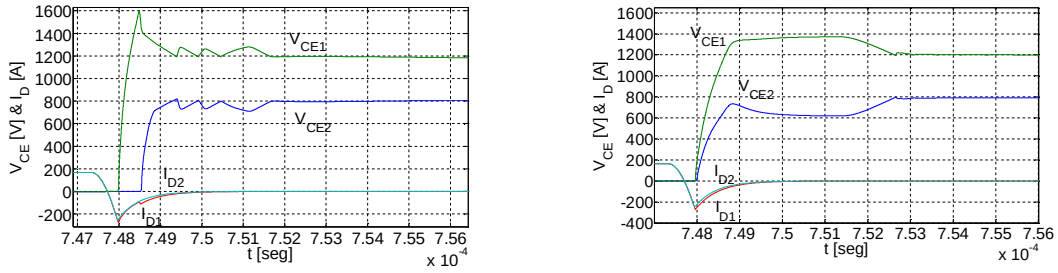


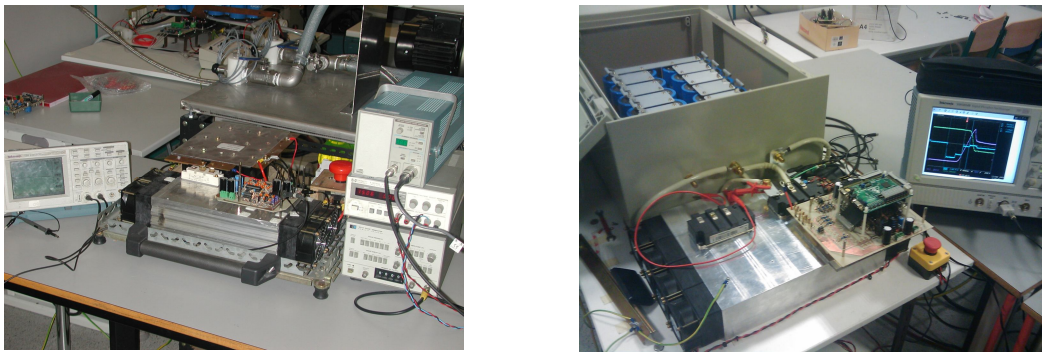
Figure 9-13: Switch off of free Wheeling diodes, without snubber (left) and with snubber (right).

Figure 9-13 shows that the switch off process of both two free wheeling diodes leads to High Voltage unbalances if snubber networks are not used. Therefore, the small snubber networks improve the voltage and power losses balance and additionally, it reduces the action of the clamp circuit that must only act to limit the maximum voltage reachable by each device.

10 Experimental Results

In this chapter the proposed control is validated experimentally. Section 10.1 validates the proposed active gate control with one IGBT while section 10.2 validates the proposed gate control for series connection of IGBT / Diode devices.

Two different test benches have been used, Figure 10-1. Low voltage IGBTs were tested in one of the test benches (BSM200GB60DLC Eupec, 200 A, 600 volts, Figure 10-1 (a)). In the second test bench, Figure 10-1 (b), higher voltage IGBTs were tested (FF200K33KF2C Eupec, 200 A, 3300 volts). The proposed control has been validated in both test benches with single IGBT operation. The series connection of IGBT/Diodes was tested only in the second test bench (FF200K33KF2C Eupec, 200 A, 3300 volts). In both cases the used load was an inductance (5 mH). The low voltage test bench has a DC bus able to supply up to 400 volts while the High Voltage test bench can supply up to 4000 volts.



(a) (b)

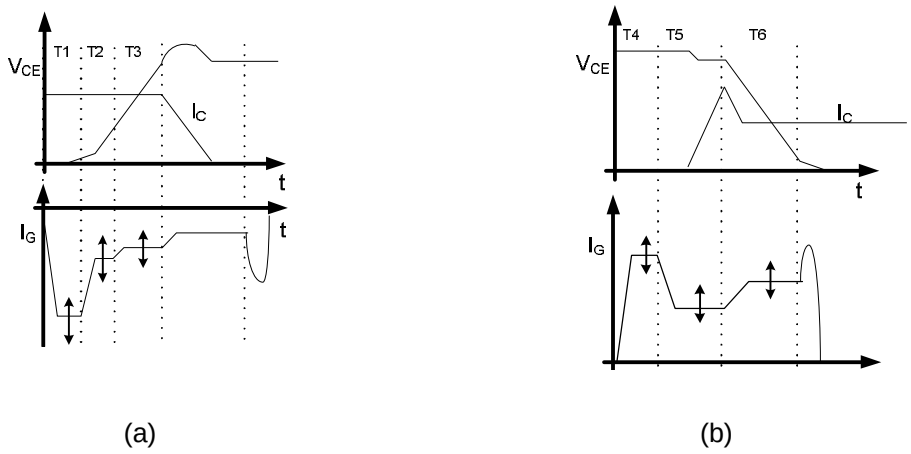
Figure 10-1: Test bench for low voltage IGBTs (a) and Medium voltage IGBTs (b)

To validate the proposed active gate control, a gate driver has been developed in which the functionalities described in chapter 8 have been implemented. The control stage is composed basically by a FPGA (50 MHz) while the measurement stage is composed by voltage dividers (V_{GE} and V_{CE}) and comparators. The output stage is composed by current sources which can inject / extract gate currents up to (approximately) 6.5 A with a current resolutions of (approximately) 15 mA.

10.1 Validation of the proposed active gate control for a single IGBT

Figure 10-2 shows the time intervals considered by the control during the switch on and switch off process. Section 10.1.1 deals with the experimental results obtained with low voltage

IGBTs while section 10.1.2 deals with the experimental results obtained with Medium voltage IGBTs.



(a) (b)

Figure 10-2: Time intervals during the switching process. Switch off process (a) and switch on process (b)

10.1.1 Validation of the control with Low Voltage IGBTs

Table 10-1 shows the conditions to detect the different time intervals and the duration for each time interval.

Time Interval	Comparison Thresholds	Duration (nano secs)
T1	OFF -> V_{CE} > 10V	920
T2	V_{CE} > 10V -> V_{CE} < 55V	
T3	V_{CE} > 55V -> V_{CE} < 288V	200
T4	ON -> V_{GE} > 5V	600
T5	V_{GE} > 5V -> V_{CE} < 254V	400
T6	V_{CE} > 254V -> V_{CE} < 10V	400

Table 10-1: Time intervals, events, duration

The total duration of T1 and T2 time intervals must be close to 920 ns. In order to achieve it, the delay time is characterized for a given gate current of 0.7 A (approximately). Therefore, depending on the switched collector current (I_C) different delay times will be measured in the T1 time interval. Depending on the delay time (t_{T1}) the gate current is controlled during the T2 time interval to achieve a total delay (t_{T1} + t_{T2}) of 920 ns. Table 10-2 shows the different time intervals considered by the gate driver.

Duration of t_{T1} (ns)	680	700	720	740	780	800

Table 10-2: Time duration (T1) and applied gate current (I_{G2}).

Figure 10-3 shows the switch off process of the IGBT for collector currents in the range of 15 to 150 amperes. If gate current levels are observed, the different time intervals can be recognised. The figures show the proposed control manages the voltage slope (dV_{CE}/dt) and the instant when this voltage slope begins (synchronization). The gate driver is also able to operate the IGBT satisfying the time references shown in Table 10-1.

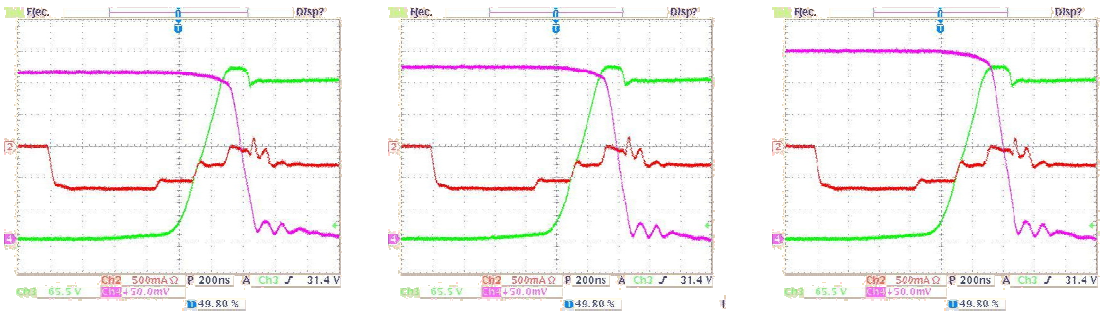


Figure 10-3: Secuence of switch off processes to observe the behaviour of the control in different operating conditions. Gate current (0.5 A /div), Collector-emitter voltage (65.5 V /div) and I_C @ 15A÷150A (25 A /div)

Similarly, Figure 10-4 shows the switch on process of the IGBT. Different time intervals can be recognized looking at the gate current waveforms. The gate driver is also able to operate the IGBT satisfying the time references shown in Table 10-1.

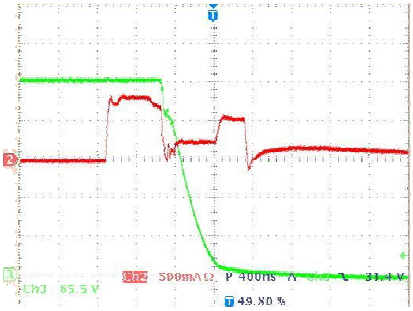


Figure 10-4: IGBT switch on. Gate current and collector-emitter voltage

10.1.2 Validation of the control with Medium Voltage IGBTs

Table 10-3 shows the definition of the different time intervals and the duration for each time interval.

Time Interval	Comparison Thresholds	Duration (nano secs)
T1	OFF -> V_{CE} > 10V	1100
T2	V_{CE} > 10V -> V_{CE} < 200V	
T3	V_{CE} > 200V -> V_{CE} < 780V	400
T4	ON -> V_{GE} > 5V	640
T5	V_{GE} > 5V -> V_{CE} < 700V	400
T6	V_{CE} > 700V -> V_{CE} < 10V	640

Table 10-3: Time intervals, events and durations

The total duration of T1 and T2 time intervals must be close to 1100 ns. In order to achieve this, the delay time is characterized for a given gate current of 2.3 A (approximately). Therefore, depending on the switched collector current (I_C) different delay times will be measured in the T1 time interval. Depending on the delay time (t_{T1}) the gate current is controlled during the T2 time interval to achieve a total delay (t_{T1} + t_{T2}) of 1100 ns. Table 10-4 shows the different time intervals considered by the gate driver.

Duration of t_{T1} (ns)	680	700	720	740	780	800

Table 10-4: Time duration (T1) and applied gate current (I_{G2}).

Table 10-4 shows the switch off process of the IGBT for collector currents in the range of 50 to 175 amperes. If gate current levels are observed, the different time intervals could be recognised. As it can be observed, the proposed control manages properly the voltage slope (dV_{CE}/dt) and the instant in which this voltage slope is given (synchronization).

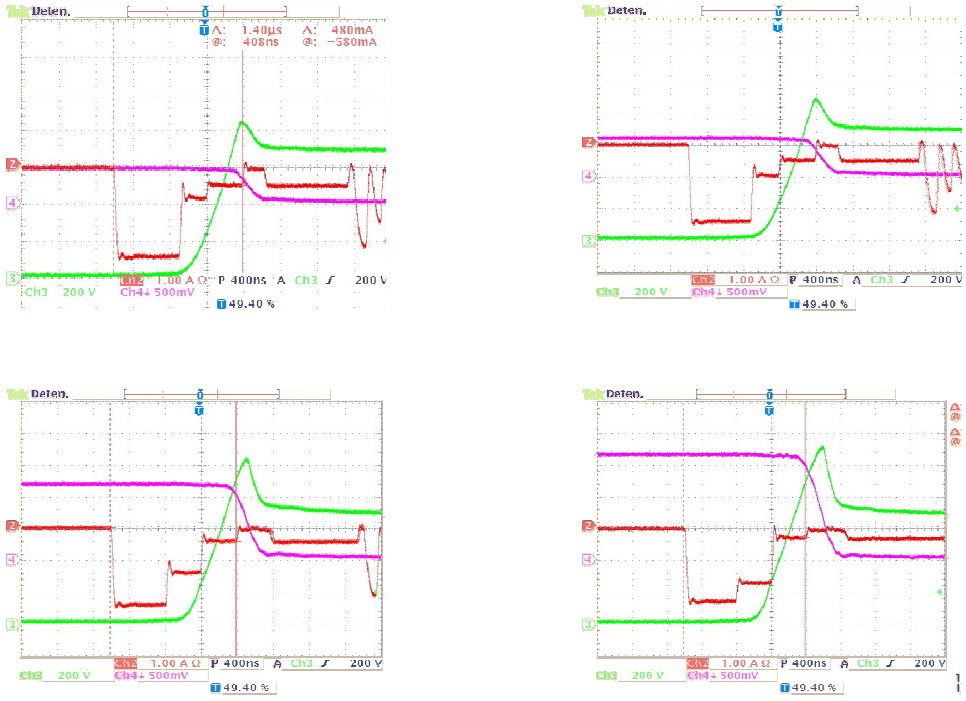


Figure 10-5: Secuence of switch off processes to observe the behaviour of the control in different operating conditions Collector current (1 A /div), collector-emitter voltage (200 V /div) and I_C @ 50A÷175A (50 A /div).

Similarly, Figure 10-6 shows the switch on process of the IGBT. Different time intervals can be recognized looking at the gate current waveforms.

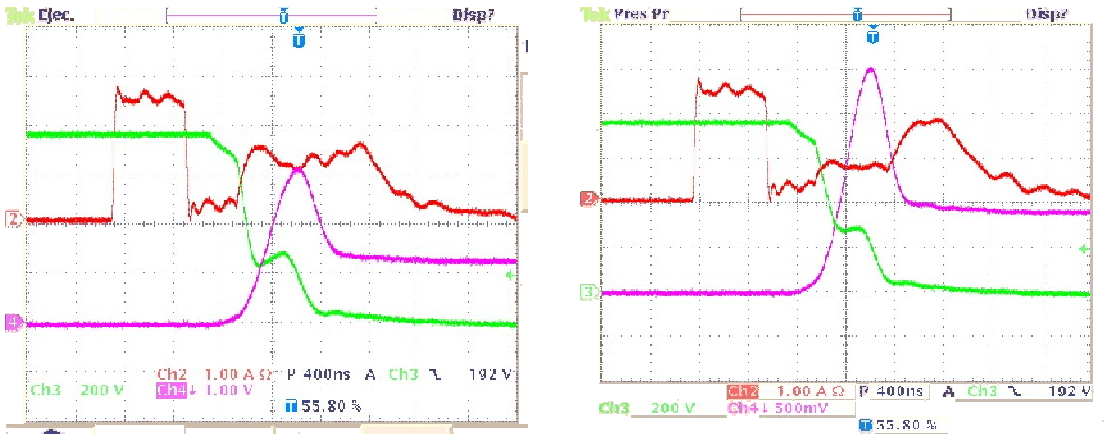


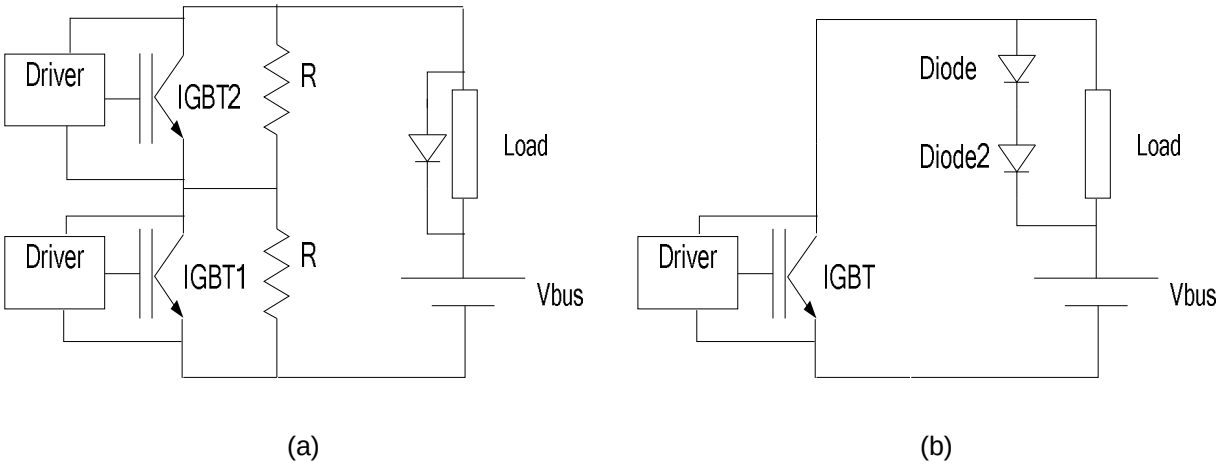
Figure 10-6: IGBT switch on. Gate current (red) and collector emitter voltage (green). Collector-emitter voltage (200 V /div) and I_C (50 A /div).

10.2 Validation of the proposed active gate control in the series connection of IGBT/Diode-s

In this section the validity of the proposed control for the series connection of IGBT/diode modules is tested. Therefore, section 10.2.1 deals with the series connection of two IGBT / Diode-s while section 10.2.2 shows the series connection of three IGBTs.

10.2.1 Validation with two IGBT / Diode-s

The voltage balance of the series connection has been tested in the test bench shown in Figure 10-1. Figure 10-7 shows the general block diagram of the used test bench for the series connection of two IGBT / Diode-s.



(a) (b)

Figure 10-7: Diagram of the test circuit for series connected IGBTs (a) and diodes (b)

a) Validation with two IGBTs

Figure 10-8 shows a balanced switch on of two series connected IGBTs. Both IGBTs operate synchronously and therefore, they achieve a proper voltage and power losses balance.

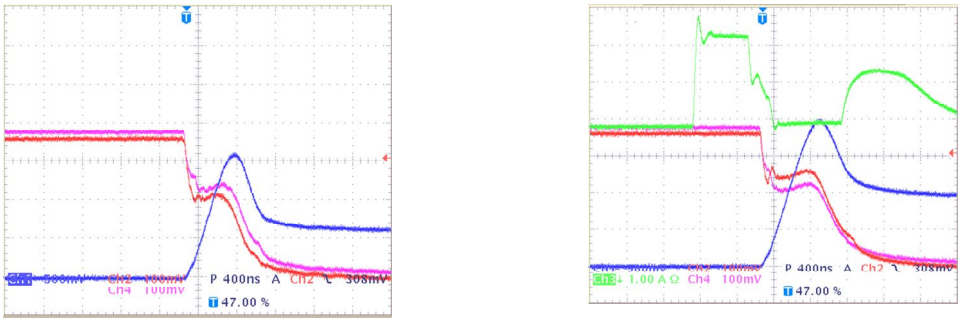


Figure 10-8: Balanced switch on of two series connected IGBTs. Vbus = 800V.

Figure 10-9 shows an unbalanced switch off of two series connected IGBTs. In this case, both IGBTs operate with different voltage slopes and asynchronously. Individual IGBT parameter differences and different gate driver currents are the cause of this voltage unbalance.

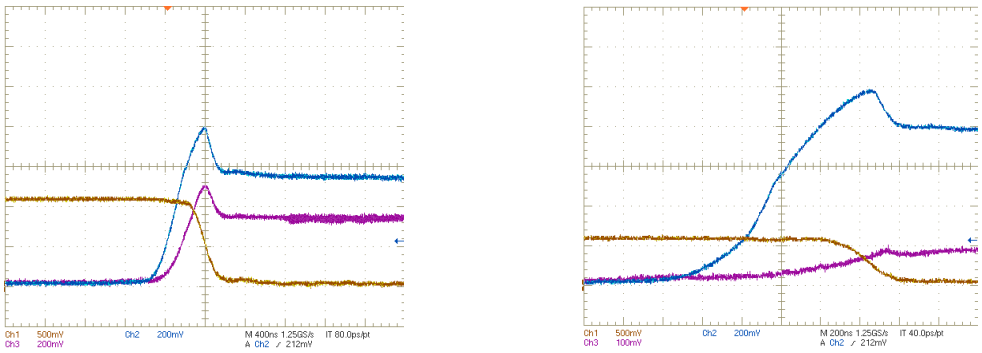


Figure 10-9: Unbalanced switch off waveforms of two series connected IGBTs in the start-up of the control. Vbus = 800 V, Ic = 115 A (left) and Ic = 60 A (right).

After reaching the steady state the gate drivers find the required gate currents to operate the IGBTs at the pre-programmed durations for each time interval. Therefore, the IGBTs operate with the same voltage slope and synchronously, Figure 10-10, Figure 10-11 and Figure 10-12.

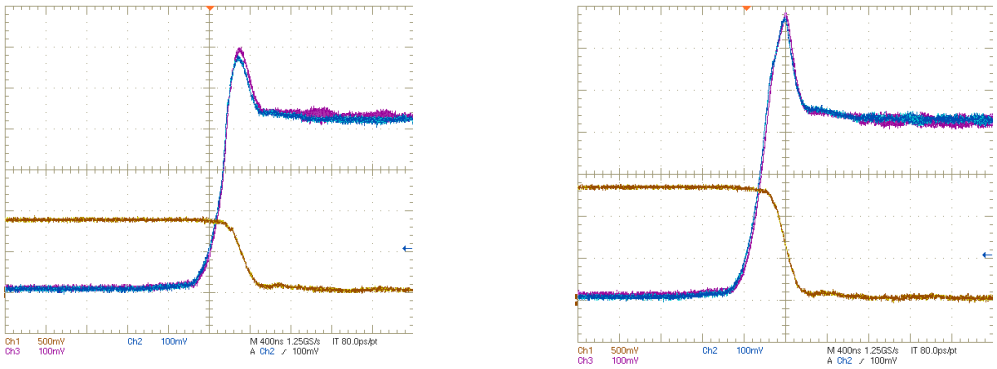


Figure 10-10: Balanced switch off waveforms of two series connected IGBTs in steady state. Vbus = 800 V, Ic = 90 A (left) and Ic = 140 (right)

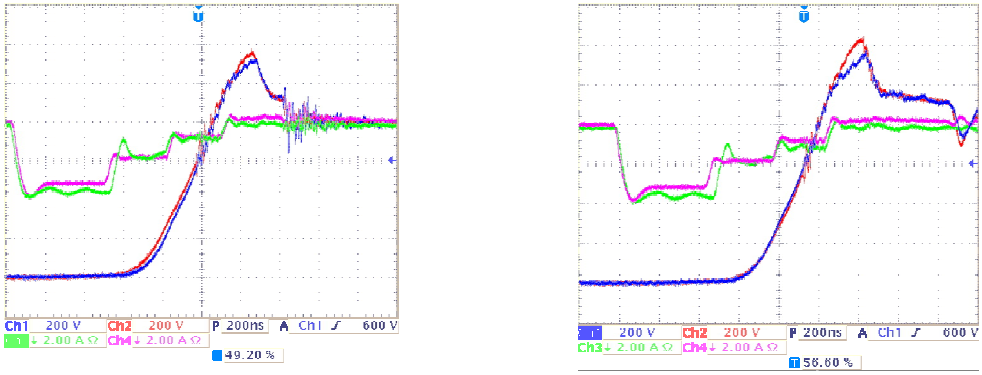


Figure 10-11: Gate currents (2 A/div) and collector-emitter voltages (200 V/div). Vbus = 1600 V.

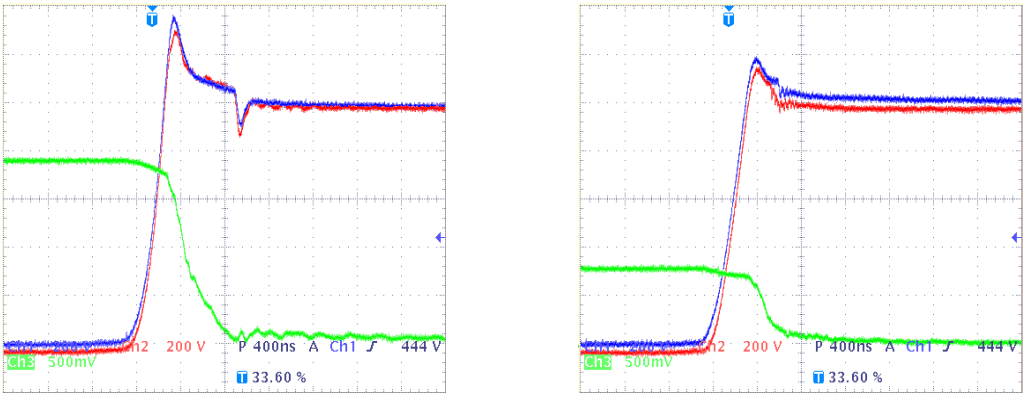
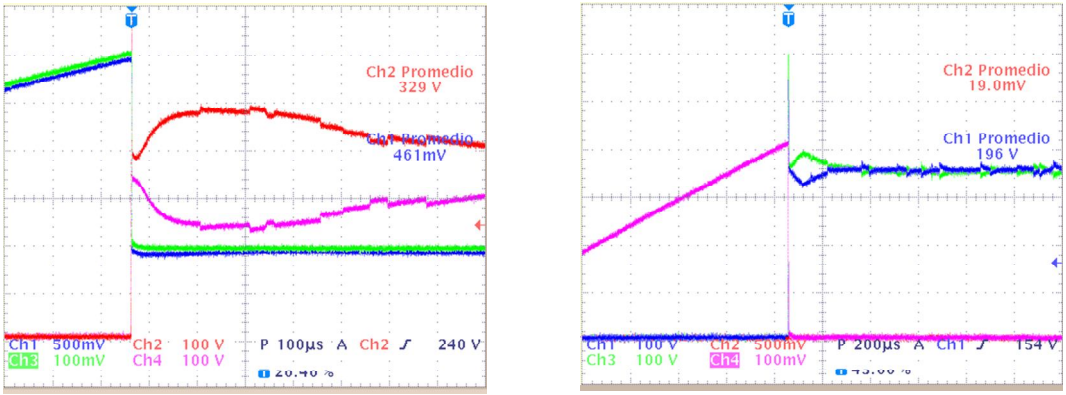


Figure 10-12: Balanced switch off waveforms of two series connected IGBTs in steady state. Vbus = 2000 V, Ic = 190 A (left) and Ic = 80 (right)

During the switch off process, although the series connected IGBTs operate synchronously, a voltage unbalance can be measured during the tail current period, see Figure 10-13. As shown in section 6.3, tail current differences are the main cause of voltage

unbalances after the collector current extinction. The main problem of this voltage unbalance is that it can not be controlled by means of the gate terminal and the amplitude of this voltage unbalance is unpredictable. In addition, this tail current has a notable influence for a long time in the voltage balance of the series connected IGBTs.

Section (c) of chapter 10.2.1 proposes a solution to deal with this problems.



(a) (b)

Figure 10-13: Effect of tail current differences in the blocking voltage of series connected IGBTs. (a) asynchronous switching and (b) synchronous switching.

b) Validation with two Diodes

Similarly, when free wheeling diodes are connected in series, the voltage balance must be guarantee under all operating conditions. Figure 10-2 shows the switch off behaviour of two series connected diodes without using any snubber network.

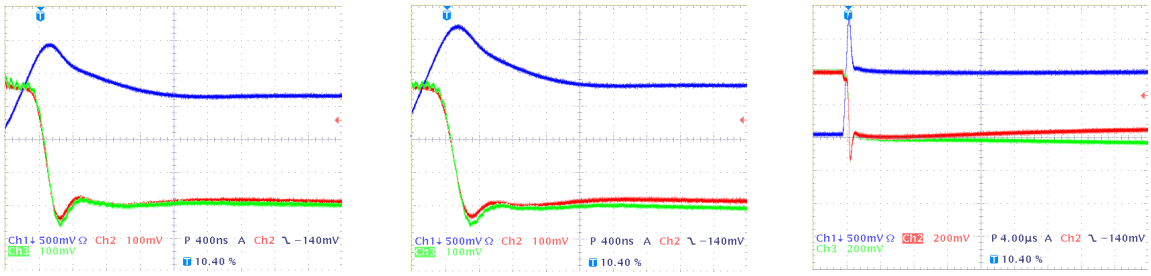


Figure 10-14: Dynamic voltage share of two series connected diodes at different operating conditions. Collector-emitter voltage (red and green) collector current (blue).

A proper dynamic voltage balance has been measured without using snubber networks. However, due to tail current differences, a voltage unbalance is observed due to differences in

their transient reverse blocking behaviours. As depicted by Figure 10-15, one diode (IGBT) blocks almost all the bus voltage.

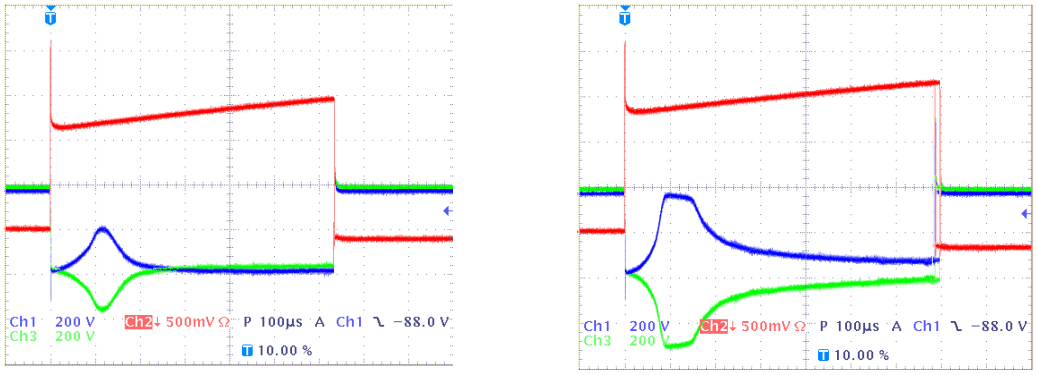
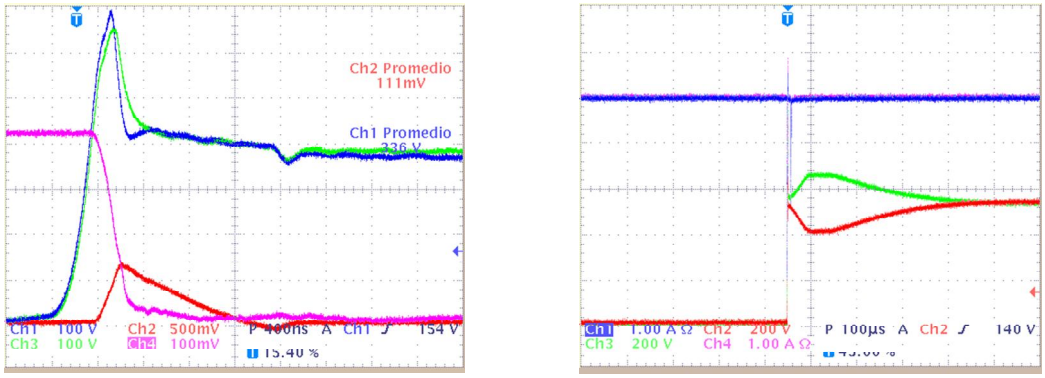


Figure 10-15: Effect of reverse recovery current differences in the blocking voltage of series connected diodes. Collector-emitter voltages (blue and green) and collector current (red).

c) Voltage limitation in the case of uncontrolled parameter differences

Based on experimental results, the use of relatively small snubber networks (< 100 nF) is a suitable solution to control voltage unbalances presented in the previous sections. However, the use of these networks has influence on the driver behaviour and of course on the overall power losses.

The energy that intervenes on these voltage unbalances is relatively low (low current amplitudes are measured during these unbalances). This means that instead of lossy snubber networks the use of clamping circuits should be much more efficient. These clamps do not compensate the voltage unbalances, but they limit the maximum operating voltage of the connected devices. The main advantage of this solution is that the clamp does not take any energy during the switching process but takes energy when an overvoltage is measured. Therefore, only a small amount of energy is taken by those clamp networks and the maximum operating voltage for each switching device is limited easily.



(a) (b)

Figure 10-16: Voltage limitation during the tail current period. Collector-emitter voltages (blue and green), collector currents (pink) and the clamp network current (red).

Figure 10-16 shows the switch off process of two series connected IGBT devices. Figure 10-16 (a) shows collector-emitter voltages (blue and green), collector currents (pink) and the clamp network current (red). The clamping network does not have any influence on the dynamic voltage balance. Only the driver circuit controls the switching process of both IGBTs. Once the voltage exceeds the clamping voltage, the clamping network operates and tries to limit the maximum operating voltage. At the end of the switch off process this clamp network effectively limits the maximum voltage unbalance caused by tail current differences, Figure 10-16 (b).

Similarly, the voltage unbalance caused by reverse recovery current differences can be limited with these clamping networks. Figure 10-17 shows the clamping effect with two series connected diodes. The maximum operating voltage of the diodes is effectively limited by the clamping networks.

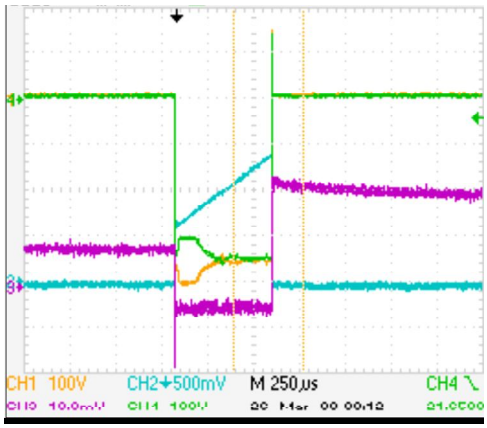
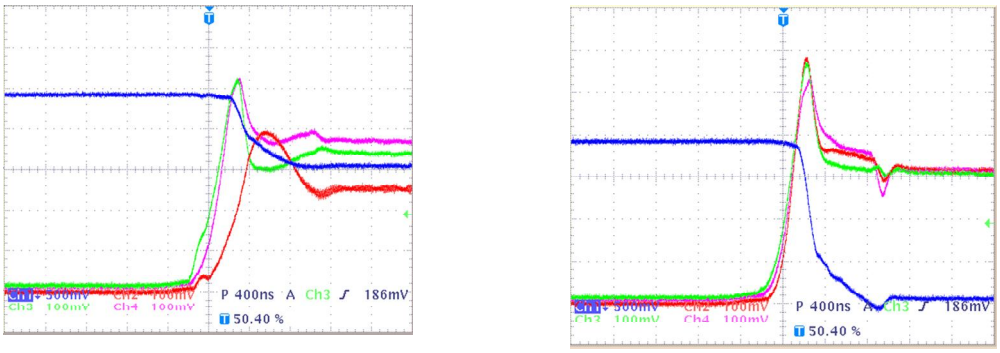


Figure 10-17: Voltage limitation during the reverse recovery current period. Collector-emitter voltage (green, orange) and collector current (blue).

10.2.2 Validation with three IGBT-s

The dynamic voltage balance has been achieved by means of the gate current while the tail current effect has been effectively limited by means of clamping networks, Figure 10-18.



(a) (b)

Figure 10-18: Unbalanced switch off (a) and balanced switch off (b)

Figure 10-19 shows the voltage unbalance caused by tail current differences.

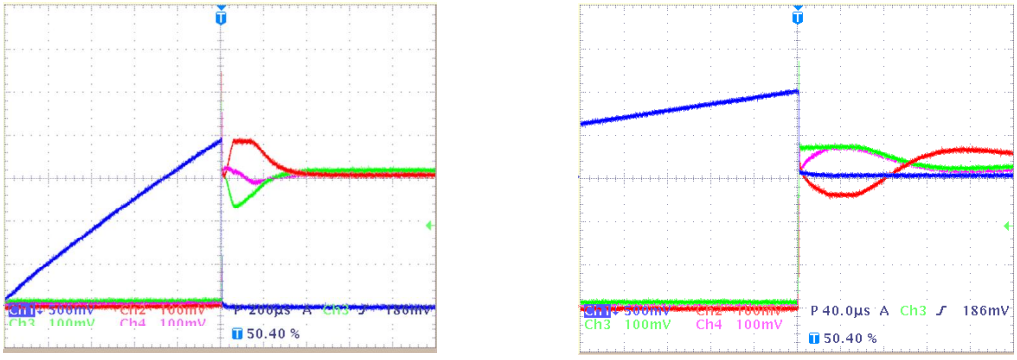


Figure 10-19: Voltage limitation during the tail current period. Collector emitter voltage (red, green, pink) and collector current (blue).

Part 4: POTENTIAL APPLICATIONS FOR MEDIUM VOLTAGE SWITCHING VALVES

11 Emerging Utility Grid Applications for Voltage Source Converters

Previous chapters have dealt with active gate control methods to achieve a proper voltage balance between series connected IGBT devices. As shown in chapter 10 the proposed control has been validated with reasonably good experimental results.

Series connection of IGBT devices promotes the use of Voltage Source Converters (VSC) in Medium Voltage utility grid applications. The advantages of this type of converters with respect to line commutated converters are detailed in appendix B (Chapter 16).

This chapter describes briefly some utility grid applications in which Voltage Source Converters (VSC) play an important role. Although many applications exist for VSC-s (Energy Storage, AC excitations for synchronous motor-generators, Industry applications, etc) only few utility grid applications will be described in the following sections.

11.1 High Voltage Direct Current transmission systems (HVDC)

In industrial drives the line commutated converter is almost totally replaced by Voltage Source Converters. The fundamental difference between these two technologies is that VSC uses semiconductors that can switch off the current (IGCT, IGBT, IEGT, GTO) and not only switch it on (thyristors) as in the case of line commutated converters. When a VSC converter operates at higher switching frequencies the use of Pulse Width Modulation (PWM) is possible and the size of the filter is also reduced.

In this application, VSC converters are used to transmit electrical energy from one point to another at High DC Voltage Ranges, Figure 11-1. This energy transmission system offers advantages with respect to the transmission at High AC Voltage systems.

Therefore, HVDC transmission systems are formed basically by two line ends VSC converters, a DC transmission line and AC side filters and transformers, Figure 11-1.

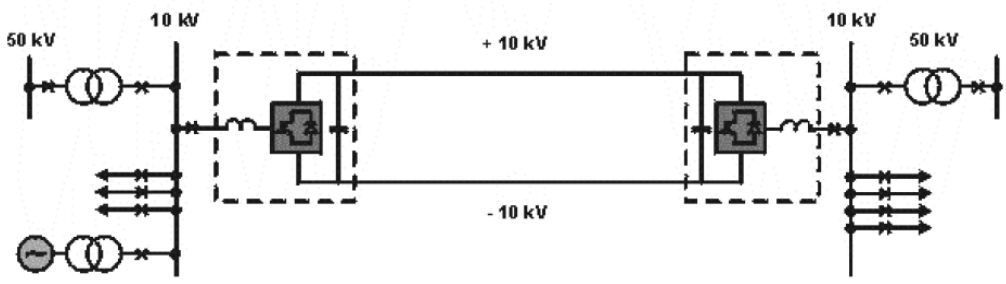


Figure 11-1: HVDC transmisión system

One VSC converter takes up energy from the alternating grid to inject it to the DC bus while the other one must extract energy from the DC bus to inject it to the electrical grid. Because of the phase and amplitude controllability of VSC converters, the operation of both converters with unity power factor is possible, Figure 11-2.

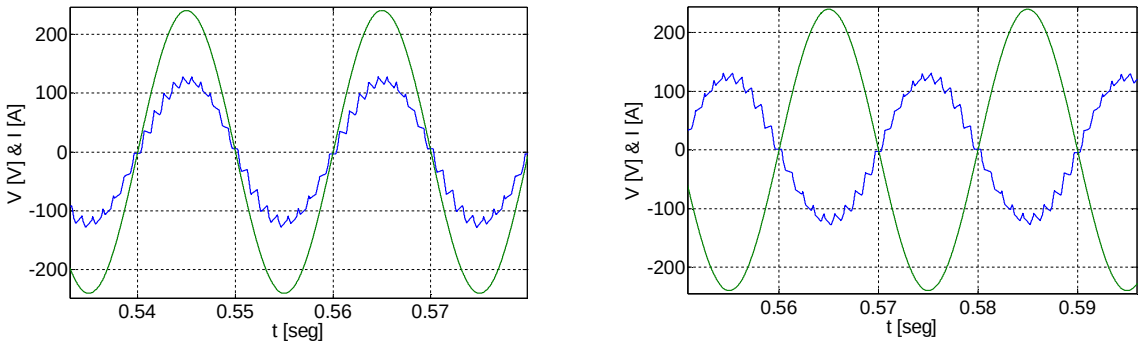


Figure 11-2: Power injection and extraction to / from the utility grid.

As the output voltage is determined by the VSC operation, VSC-HVDC systems can be connected to weak or isolated electrical grids while thyristor based CSC-HVDC systems can not be connected to weak or isolated electrical grids. In addition, these converters do not need reactive power to transmit active power due to the fact that they allow the independent control of active and reactive powers. Because of lower harmonic current distortion than in CSC-HVDC systems smaller filters can be used reducing the total size and cost of the installation.

As VSCs can deal simultaneously with energy transmission (HVDC) and reactive power compensation (SVC) the total size of the converter is lower than the case of CSC-HVDC systems, Figure 11-3.

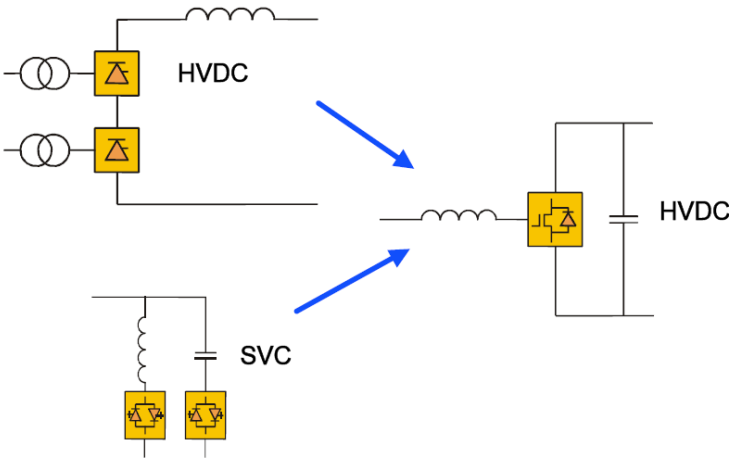


Figure 11-3: Comparison of classic HVDC and VSC-HVDC

One of the main drawbacks of these VSC-HVDC systems resides in the higher power losses due to higher switching frequency operation (switching losses) and the higher conduction losses of self commutated devices.

11.2 Static Var Compensator (STATCOM)

Power Quality standards have emerged as a figure of merit for the power distribution utility grids. Among the various Power Quality problems, voltage disturbances (steady state and transient) have been identified to have the maximum probability of occurrence. Critical industrial equipment like PLC-s (Programmable Logic Controllers) and ASD-s (Adjustable Speed Drives) are adversely affected by voltage dips of about 10% [SE-00]. In an electric power system, the balance of the supply and demand of active and reactive powers is compulsory. If the balance is lost, frequency and voltage variation may occur in the system resulting, in the worst case, in the collapse of the power system. Appropriate voltage and reactive power control is one of the most important factors for stable power system operation. Some approaches to the voltage disturbance problem, using active devices, involve a series injection of a voltage and/or a shunt injection of a reactive current.

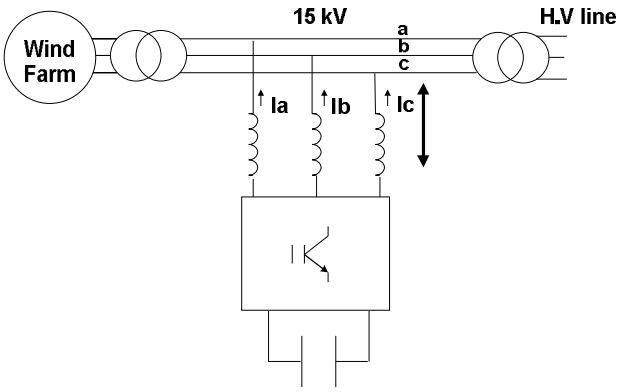


Figure 11-4: Basic structure of a STATCOM

A STATCOM (Static Var Compensator) is basically a Voltage Source Converter connected in parallel that injects reactive power to the utility grid in order to regulate the voltage in the connection point, Figure 11-4. Because of the output voltage controllability, a STATCOM can behave as an inductive load or a capacitive load, Figure 11-5.

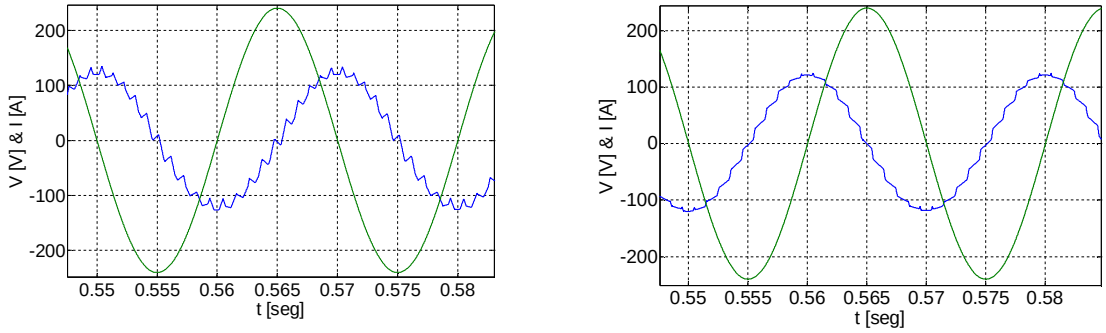


Figure 11-5: Capacitive behaviour and inductive behaviour of the VSC converter.

In reactive power compensation applications the most used power semiconductor is still the thyristor (SVC). However, self commutated devices promote the use of VSC converters for reactive power applications (STATCOM). These converters show a higher efficiency, a smaller size and higher flexibility. As described in [NO-03], STATCOMs show higher regulation capacity than SVCs under electrical voltage drops. This is because SVC converters are basically controlled reactances whose reactive power capacitance is dependent on the grid voltage.

11.3 Active Filter

The proliferation of nonlinear loads such as static power converters has deteriorated the power quality in power transmission and distribution systems. Voltage harmonics resulting from current harmonics produced by the nonlinear loads have become a serious problem in many countries [AK-96].

Passive filters and capacitor banks have been used extensively for harmonic mitigation and power factor correction in power systems. However, power capacitors and passive filters are responsible of causing resonances in power distribution systems. These resonances lead to the amplification of harmonic voltages. Several solutions have been proposed to damp out these harmonic voltages. Among them, the most effective solution is to install active filters. These filters have provided the required harmonic filtering in comparison to conventional shunt passive filters [IN-06].

Active filters can be classified into pure active filters and hybrid active filters. Most pure active filters use either a voltage-source PWM converter equipped as their power circuit with a DC capacitor or a current source PWM converter equipped with a DC inductor. At present, the voltage source converter is better than the current source converter in terms of cost, physical size and efficiency [AK-05]. Hybrid active filters consist of single or multiple voltage source PWM converters and passive components such as capacitors, inductors, and/or resistors. The hybrid filters are more attractive for harmonic filtering than the pure filters from both feasibility and economical points of view, particularly for High Power applications [AK-05].

Pure active filters can be classified into shunt (parallel) active filters and series active filters, Figure 11-6. The shunt active filter is controlled to draw a compensating current, i_{AF}, from the utility grid, so that it cancels current harmonics on the AC side of a general-purpose non linear load. The shunt active filter has the capability of damping harmonic resonances between an existing passive filter and the supply impedance. Series active filters are connected to the utility grid through a matching transformer. Basically, the series active filter controller measures the supply current harmonic content and then, the filter applies a compensating voltage across the primary of the transformer to reduce the supply current harmonic content.

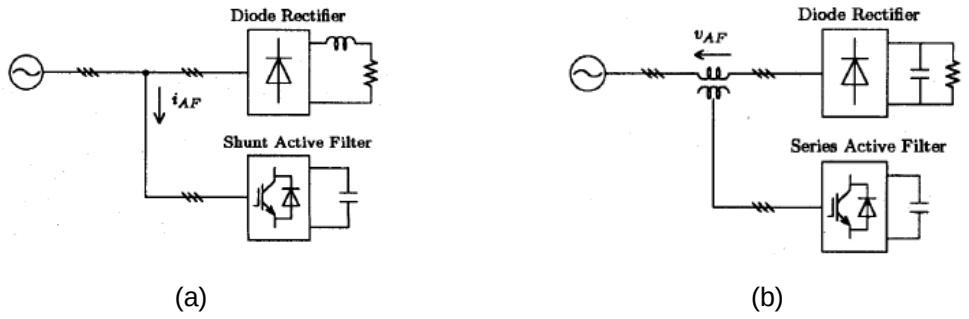


Figure 11-6: Pure shunt active filters. Shunt filters (a), series filter (b).

Figure 11-7 shows hybrid active / passive filters, whose main purpose is to reduce initial costs and to improve efficiency. Although different hybrid filter configurations can be found, they basically share the same operating principle and they also have similar filtering performance.

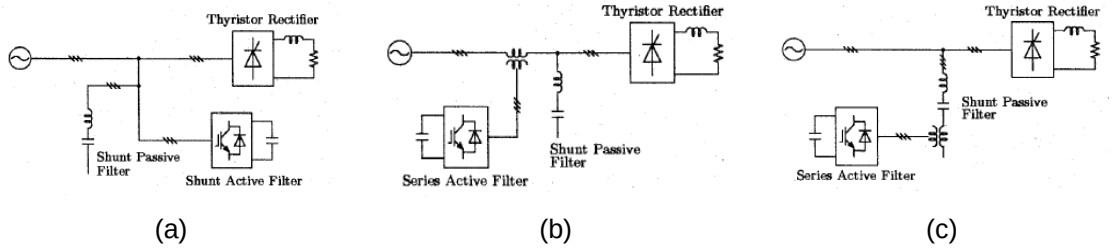


Figure 11-7: Hybrid active filters. Shunt active filter with shunt passive filter (a). Series active filter with shunt passive filter (b). Shunt passive filter with series active filter (c).

11.4 Dynamic Voltage Restorer (DVR)

The dynamic voltage restorer is a series connected device whose voltage injection controls the load voltage [GO-02]. The main fuction of a DVR is to mitigate the voltage dip, although sometimes, additional functions such as harmonics compensation and reactive power compensation are also integrated into the device. In the case of a voltage dip the DVR injects the missing voltage and it avoids any trip in the load, Figure 16-4.

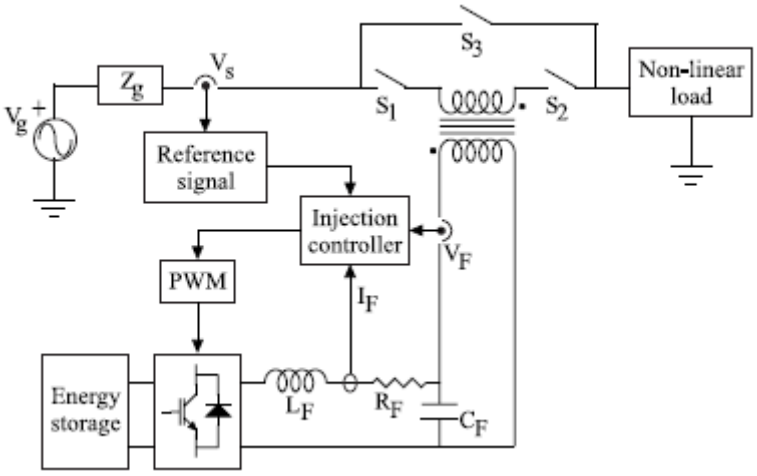


Figure 11-8: Diagram of a DVR

As a series connected device, one of the drawbacks of the DVR resides in the difficulty to protect the device during short circuits and avoid interference with the existing protection equipment.

11.5 Unified Power Flow Controller (UPFC)

Among advanced FACTS (Flexible AC Transmission System) devices the UPFC (Unified Power Flow Controller) is considered one of the newest and the most powerful FACT devices [MA-04]. The basic hardware configuration of a UPFC can be seen as the combination of a STATCOM and a SSSC (Static Series Synchronous Compensator) [MA-04] or as the combination of a series active filter and a shunt active filter [AK-96].

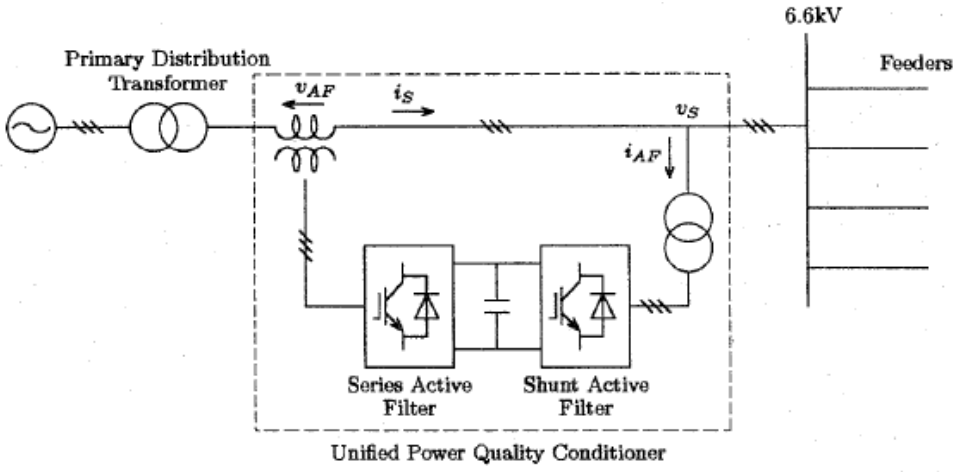


Figure 11-9: Block diagram of an UPFC.

Basically, the functions being performed by the series active filter are harmonic isolation between the transmission subsystem and the distribution system, voltage regulation and the

voltage unbalance compensation at the point of common coupling. The functions being performed by the shunt active filter are harmonic current compensation and DC link voltage regulation between both active filters.

Therefore, the series active filter measures the supply current (i_s) and it is controlled to present zero impedance for the fundamental frequency and to act as a high value impedance G (Ω) for the harmonic frequencies.

Similarly, the shunt active filter is intended for harmonic compensation. Hence, the shunt active filter detects the bus voltage at the connection point, v_s, and it is controlled to present infinite impedance for the fundamental frequency and to act as a resistor with low resistance of 1 / K(Ω) for the harmonic frequencies.

$$v_{AF} = G \cdot i_{sh} \tag{11-1}$$

$$i_{AF} = K \cdot v_{sh} \tag{11-2}$$

In (11-1) and (11-2), i_{sh} and v_{sh} are the harmonic current and voltage which are extracted from the detected supply current i_s and the bus voltage v_s. G and K are the feedback gains of the series and shunt active filters, respectively.

12 Voltage Source Converters: State of the Art and Modelling

As described in chapter 11, power electronic converters play an important role in many real power applications. Especially, Voltage Source Converters are widely used for industrial and utility grid applications. For this reason, this chapter focuses on the analysis and modelling of Voltage Source Converter topologies.

12.1 Power Electronic Converters Classification

Figure 12-1 shows a simplified classification of High Power electronic converters, where direct and indirect converters can be easily distinguished.

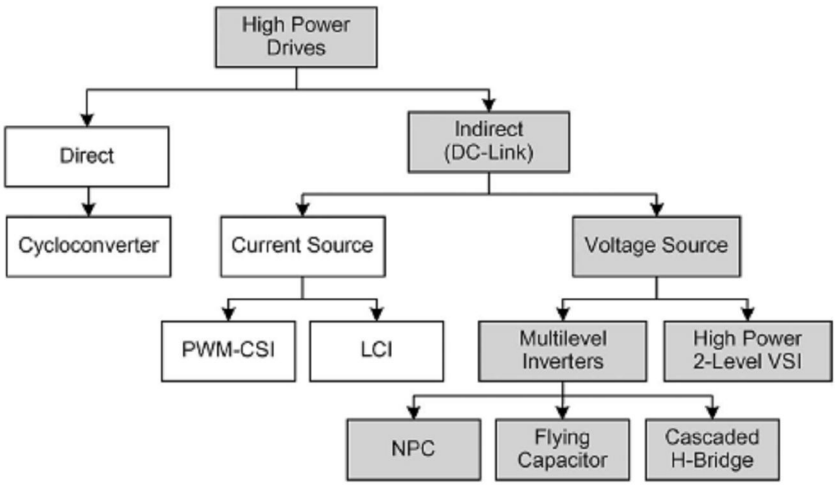


Figure 12-1: AC/AC (> 1MW) High Power converter classification [RO-07]

Direct power converters connect the load directly to the main energy source by means of power semiconductor devices. The cyclo converter is one of the better known topologies for Medium voltage and High power applications. This converter uses a semiconductor array to connect the electrical grid directly to the electrical machine. Therefore, it can convert a three phase voltage with constant phase and amplitude to a three phase voltage with variable phase and amplitude. In addition, this converter is reversible and has a high operating efficiency. One of the main drawbacks of this converter is its limited dynamic response. The Matrix converter belongs to this classification, however this converter is only available up to 150 kW [RO-07].

Indirect converters perform the power transference in two different steps: Rectification and Inversion. To make this conversion indirect converters need an energy storage element. These converters can be divided in current source converters or voltage source converters depending on the type of energy storage element used in the DC bus.

Figure 12-2 shows the general block diagram of an indirect converter. Usually, a transformer with multiple secondary windings is used to reduce the harmonic distortion of the line current. The rectifier transforms the alternating voltage to direct voltage with fixed or variable amplitude depending on the type of rectifier (controlled, non-controlled). The DC filter, can be a capacitor (smoothes the DC bus voltage) for voltage source converters or an inductor (smoothes the DC bus current) for current source converters.

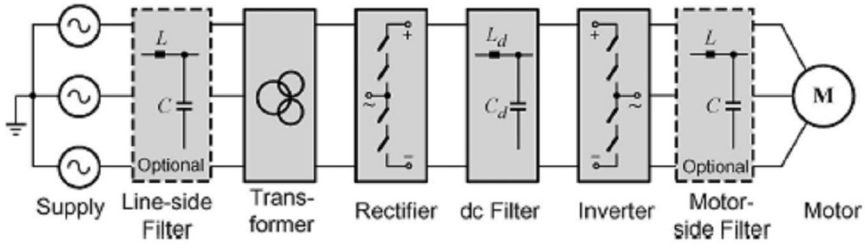


Figure 12-2: Block diagram of an indirect AC/AC converter loaded with an electrical machine [RO-07].

For High Voltage applications, two current source converter topologies can be found: Line commutated converters (LCC) and PWM (Pulse Width Modulation) converters (PWM-CSC). The LCC converter has been used for decades because of its simplicity, low cost and high reliability. Its higher drawback resides in the poor operating power factor and the AC side current distortion. PWM-CSC converters do not present these problems.

In comparison with current source converters, High Power voltage source converters have experienced a bigger market penetration and a bigger development during the last decades. The classical two level converter was limited to Low-Medium power applications due to the limited voltage blocking capability of the switching devices. The series connection of switching devices makes the use of this topology in High Voltage applications possible. If some diodes and capacitors are added to the two level converter, multilevel converter topologies are formed. These topologies improve the output voltage waveform. The output voltage is composed by small voltage steps, with lower harmonic content, lower dv/dt applied to the load and lower common mode voltage. These characteristics have made multilevel converters a widely accepted converter topology for Medium voltage applications. The Neutral Point Clamp converter (NPC), the Flying Capacitor (FC) converter and the cascaded H bridge converters are the most known.

Nowadays, two level and three level converter topologies are used in (commercial) applications up to 34 kV and 32 MVA. Manufactures like ABB or SIEMENS, use two level converters [JA-06] (section 12.3.3) for energy transmission applications at High Voltage DC current (HVDC) (±150kV, 300MW). ABB uses three level NPC converters (section 12.3.5) for STATCOM applications (SVC-Light) and HVDC applications (Murraylink). Converteam uses this NPC topology for High Power drive applications [CO]. Three level NPC converters are used mainly in drives, pumps, fans, etc. Flying Capacitor (FC) converters (section 12.3.6) are mainly

used in applications that require high switching frequencies [RO-07]. Cascaded H bridges (section 12.3.4) are used in High Power applications, active filter applications, reactive power compensation applications, electric vehicles, solar energy, etc [RO-07], [BE].

Currently, there is a tough competition between the use of classic power converter topologies using High Voltage semiconductors and new converter topologies using Medium Voltage devices [FR-08]. This idea is shown in Figure 12-3, where multilevel converters built using mature Medium Power semiconductors are fighting in a development race with classic power converters using High Power semiconductors that are under continuous development and are not mature.

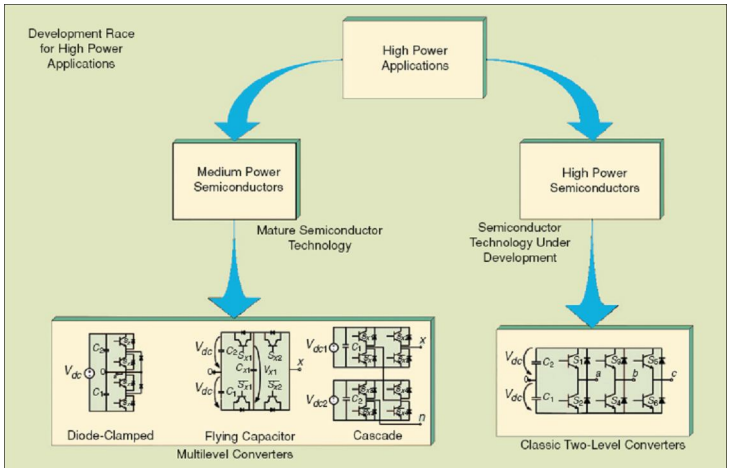


Figure 12-3: Two Level converter vs Multilevel converters [FR-08].

According to [FR-08], multilevel converters are a good solution for power applications because of the fact that they can achieve High Power using mature Medium Power semiconductor technology. In addition, multilevel converters present great advantages compared with conventional and very well known two level converters. These advantages are fundamentally focused on improvements in the output signal quality and a nominal power increase in the converter. These properties make multilevel converters very attractive to the industry and, nowadays, researches all over the world are spending great efforts trying to improve multilevel converter performances such as the control simplification and the performance of different optimization algorithms in order to enhance THD of the output signals, dc capacitor voltage balances and current ripples.

However, in spite of the advantages shown by multilevel converters, the inherent problems to the multilevel topology such as the reliability or higher control complexity, has slowed their adoption for High Voltage applications.

12.2 State of the Art of Voltage Source Converters

12.2.1 Two Level VSC Converter

The two level converter is a well known topology in low, Medium and High Power applications. The most used power devices with this converter are the 3.3, 4.5 and 6.5 kV IGBTs. To increment the power level of the converter the series connection of semiconductors could be used. Each phase of this converter is composed by two switches (or series connected switching devices, Figure 12-4). Depending on the bus voltage, some capacitors may be connected in series. Section 12.3.3 describes the behaviour and modelling of this type of converter.

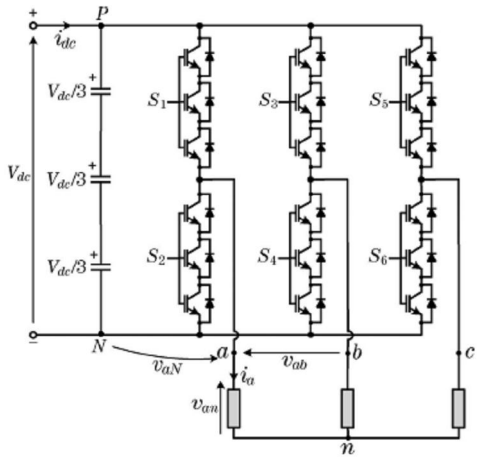


Figure 12-4: High power two level converter [RO-07].

The most used modulation schemes in this type of converter are the bipolar PWM including the third harmonic (12-1), the Space Vector Modulation (SVM) and the Selective Harmonic Elimination (SHE).

$$V_{ref} = V_{max} \cdot \left(\sin(\omega \cdot t) + \frac{1}{6} \cdot \sin(3 \cdot \omega \cdot t) \right) \qquad (12\text{-}1)$$

12.2.2 Multilevel converters

In this section the most used and commercially available multilevel topologies are described [KR-07], [RO-07]: The three level NPC converter, the flying capacitor converter and the H bridge cascaded connected converter.

a) NPC Converter

The three level NPC converter was presented for the first time in the early 1980s [RO-07]. Figure 12-5 shows this converter. As it can be observed, the amount of needed semiconductor devices per phase is higher than the required by two level converters. In addition, this converter needs clamp diodes to connect the middle point of the bus with the output. In consequence, the bus must be divided to obtain a middle point and therefore, a higher number of capacitors are needed.

In this NPC three level converter, the operating voltage of the semiconductors is a half of the operating voltage of the semiconductors in a two level converter. Therefore, this converter can increase the bus voltage and in consequence the output power with respect to two level converters. This topology can be extended to a higher number of voltage levels, however, there is not any commercially available NPC converter with more than three levels. Section 12.3.5 describes the behaviour and the modelling of this converter.

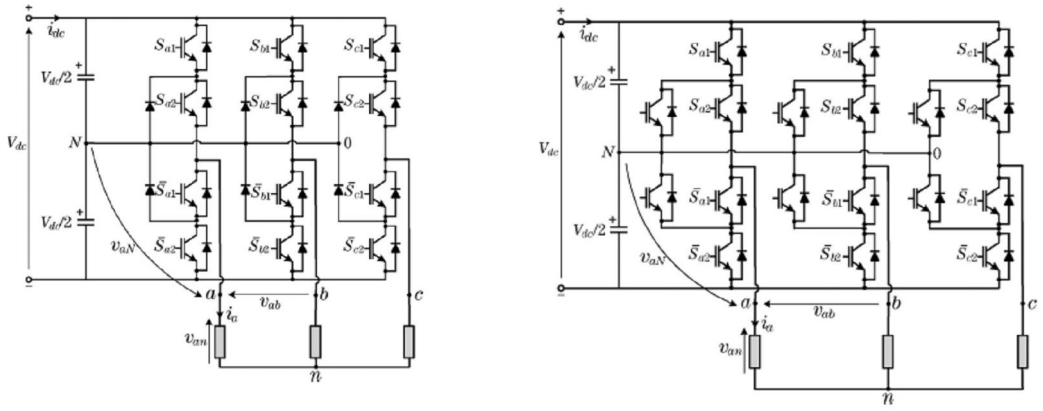


Figure 12-5: Three Level NPC converter. Active Three Level NPC converter (A-NPC) [RO-07]

One of the main drawbacks of the NPC converter is the asymmetrical power loss distribution among the semiconductors. As a consequence, there is a non equal junction temperature distribution which requires specific thermal dimensioning for each device. This drawback could be fixed if self commutated devices are used instead of clamp diodes, Figure 12-5. This topology is called Active NPC converter [RO-07]. The power losses balance, improves the junction temperature balance and in consequence leads to an increment of the achievable output power or the switching frequency.

This converter is mainly used in applications up to 4.16 kV_{DC}- 30MVA (with 5.5 kVs IGCTs) or 3.4kV_{DC} – 32 MVA (with 4.5 kVs IGBTs).

b) Cascaded H Bridge Converter

The cascaded H Bridge multilevel converter was presented for the first time in 1988 [RO-07]. In 1997 it began to be seriously considered after been used for High Power drive applications.

This converter is composed by the series connection of H bridge converters (section 12.3.2), Figure 12-6.

The output voltage of this converter is the sumation of the individual cell output voltages (all of them connected in series). Each cell can synthesise three different voltage levels (V_{dc}, 0, -V_{dc}), however, as the 0 voltage level does not add any extra voltage level the total output voltage levels are determined by the following expression:

$$\text{levels} = 2 \cdot \text{N} + 1 \tag{12-2}$$

Where N denotes the number of series connected cells.

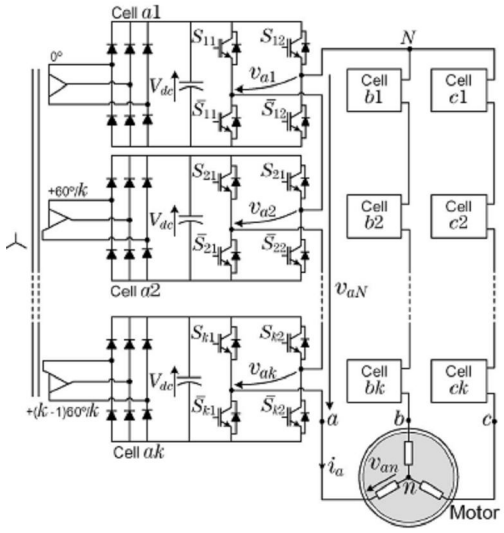


Figure 12-6: Seven level cascaded H bridge converter [RO-07].

This converter has some variants in which each switching cell has different bus voltages. These converters are known as hybrid or asymmetric converters. These converters are similar to the one described in Figure 12-6, however, in these converters each DC bus voltage has different voltage levels, Figure 12-7.

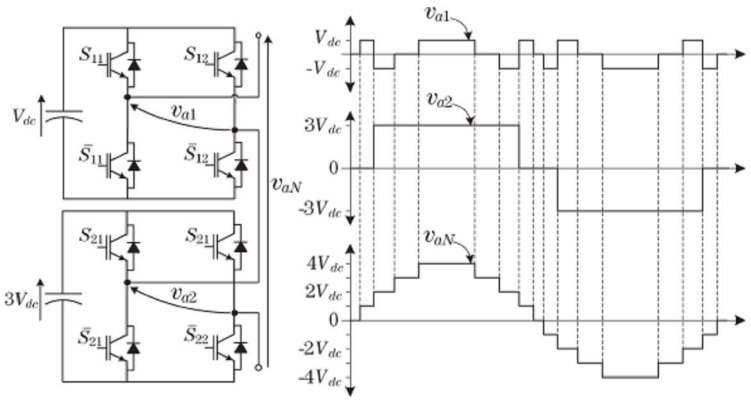


Figure 12-7: Nine Level Hybrid converter [RO-07].

When different voltage levels are chosen for each DC bus, some switching state redundancies are excluded and more output voltage levels are achieved with the same number of switching cells. This reduces the size and the cost of the converter and improves the reliability of the converter because of the less number of used semiconductors and capacitors. One of the main drawbacks of these converters is the lack of modularity because each cell must be designed for its individual characteristic.

The maximum number of voltage levels can be obtained when the different bus voltages are scaled by a factor of 3 (V_{dc}, $3V_{dc}$, etc). For k cells connected in series, this asymmetry produces 3^k voltage levels at the output terminals of the converter. As shown in Figure 12-7 the converter with higher voltage can operate at a very low switching frequency which reduces the switching losses.

Depending on the chosen voltage relation and the modulation index, the converter with lower voltage can operate in regenerative mode even if the converter is transmitting power to the load. Therefore, some considerations must be taken into account to avoid an uncontrolled increase of the bus voltage in the lower powered converter and in consequence an increase of the harmonic distortion of the output waveform.

c) Flying capacitor Converter

The flying capacitor multilevel converter was presented at the beginning of 1990. Nowadays, four level FC converter is the most popular converter based on this topology [RO-07]. Figure 12-8 shows the four level flying capacitor converter.

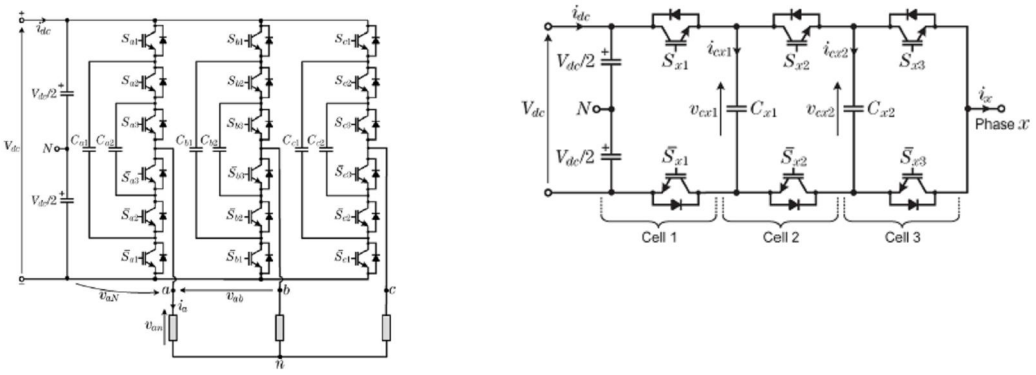


Figure 12-8: Four Level flying capacitor converter. Switching cell of the converter [RO-07].

Each converter leg is composed by the series connection of three switching cells, Figure 12-8. The nominal voltages for each capacitor (C_{x1}, C_{x2}) are $2/3V_{dc}$ and $1/3V_{dc}$ respectively. These capacitors must be charged before the operation of the converter.

This converter is commercially available for power ranges up to 8MVA [FR-08] [RO-07]. One of the main drawbacks of this topology is the high cost and size of the flying capacitors for low and medium frequency applications.

12.3 Voltage Source Converter Modelling

In following sections the most used voltage source converters are modelled: One phase H bridge converter, two level three phase converter, multilevel NPC converter, cascaded H bridge converter and flying capacitor converter.

12.3.1 Single phase half bridge converter

The single phase half bridge converter has only two switches (T1 and T1'). These switches can not be switched on at the same time as a result of what this will cause a short circuit in the DC bus. Therefore, these switches must operate complementarily, Figure 12-9.

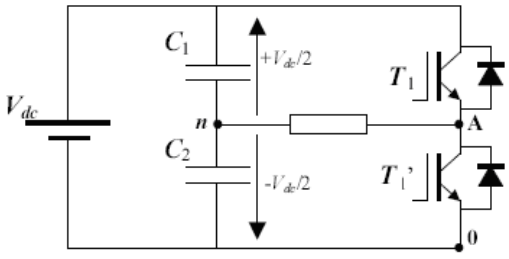


Figure 12-9: One phase half bridge converter.

Depending on the direction of the current, when T1 switch is switched on (T1' is switched off) the current will flow across the controlled switch or across its free wheeling diode. In consequence, if the voltage drop across the switch is neglected, the load voltage V_{An} will be $+V_{dc}/2$. When T1' is conducting the load voltage V_{An} will be $-V_{dc}/2$.

In consequence, depending on the control signal (S_1) the voltage applied to the load will be $+V_{dc}/2$ or $-V_{dc}/2$. Assuming that $S_1=1$ implies the conduction of T1 and $S_1=0$ implies the no conduction of T1 (T1' conducts) the following expression is obtained:

$$v_{A0} = S_1 \cdot V_{dc} \tag{12-3}$$

Or:

$$v_{An} = (2 \cdot S_1 - 1) \cdot \frac{V_{dc}}{2} \tag{12-4}$$

12.3.2 Single phase full bridge converter

If a second leg is added and the load is connected between both legs the single phase full bridge converter is obtained, Figure 12-10.

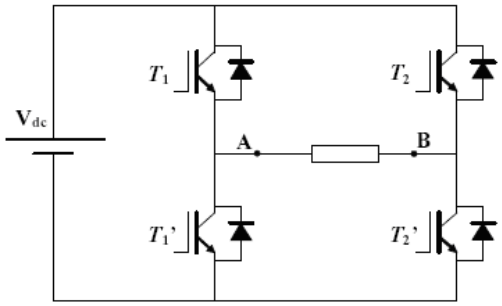


Figure 12-10: H bridge converter.

In this converter, depending on the conduction state of the switching devices the following voltages can be applied to the load (V_{AB}): $+V_{dc}$, 0 and $-V_{dc}$, Table 12-1.

Active switches	Output voltages, v_{AB}
T_1 and T_2'	$+V_{dc}$
T_1' and T_2	$-V_{dc}$
T_1 and T_2	0
T_1' and T_2'	0

Table 12-1: Conduction states

The voltage applied to the load in a single phase full bridge converter is given by the following expression:

$$v_{AB} = (S_1 - S_2) \cdot V_{dc} \tag{12-5}$$

12.3.3 Three phase two level converter

If another leg is added to the single phase full bridge converter the three phase two level converter is obtained, Figure 12-11.

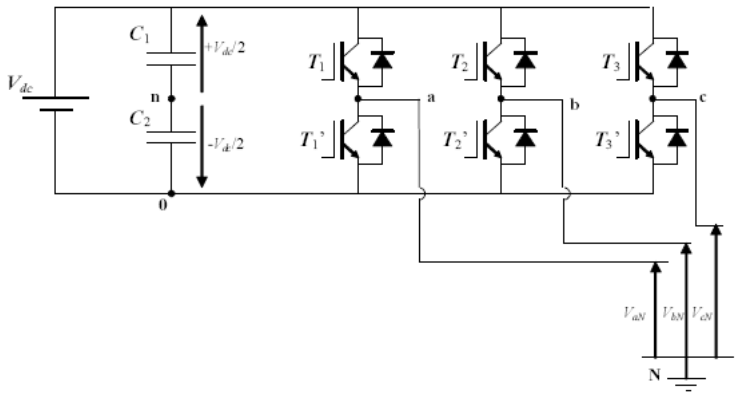


Figure 12-11: Two level – Three phase converter

In this converter, the phase voltages with respect of the 0 terminal (of the DC bus) depend on the conduction state of the switches:

$$v_{a0} = S_1 \cdot V_{dc} \tag{12-6}$$

$$v_{b0} = S_2 \cdot V_{dc} \tag{12-7}$$

$$v_{c0} = S_3 \cdot V_{dc} \tag{12-8}$$

As it is known:

$$v_{aN} = v_{a0} - v_{N0} \tag{12-9}$$

$$v_{bN} = v_{b0} - v_{N0} \tag{12-10}$$

$$v_{cN} = v_{c0} - v_{N0} \tag{12-11}$$

Assuming a balanced three phase system the following expression can be obtained:

$$v_{N0} = \frac{v_{a0} + v_{b0} + v_{c0}}{3} \tag{12-12}$$

Therefore, it is possible to obtain the phase voltages respect of the neutral point:

$$v_{aN} = \frac{V_{dc}}{3} \cdot (2 \cdot S_1 - S_2 - S_3) \quad (12\text{-}13)$$

$$v_{bN} = \frac{V_{dc}}{3} \cdot (2 \cdot S_2 - S_1 - S_3) \quad (12\text{-}14)$$

$$v_{cN} = \frac{V_{dc}}{3} \cdot (2 \cdot S_3 - S_2 - S_1) \quad (12\text{-}15)$$

From these equations it can be said that the three phase two level converter can synthesise 2^3 different output voltage levels depending on the conduction state of each leg, Table 12-2. As it could be noted, among these 2^3 states, six states are active while two of them apply 0 volts at the load. It can be observed also that the maximum phase amplitude is $2V_{dc}/3$.

S_1	S_2	S_3	V_{aN}	V_{bN}	V_{cN}
0	0	0	0	0	0
0	0	1	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$\frac{2 \cdot V_{dc}}{3}$
0	1	0	$-\frac{V_{dc}}{3}$	$\frac{2 \cdot V_{dc}}{3}$	$-\frac{V_{dc}}{3}$
0	1	1	$\frac{-2 \cdot V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$
1	0	0	$\frac{2 \cdot V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{3}$
1	0	1	$\frac{V_{dc}}{3}$	$\frac{-2 \cdot V_{dc}}{3}$	$\frac{V_{dc}}{3}$
1	1	0	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{-2 \cdot V_{dc}}{3}$
1	1	1	0	0	0

Table 12-2: Conduction states

12.3.4 Cascaded H bridge converter

This multilevel converter uses series connected single phase H bridge converters, Figure 12-12. Each converter can synthesise three different voltage levels (12.3.2), so the output voltage is obtained by voltages addition of each individual converter. Two additional voltage levels are obtained per one extra converter added to the phase. Therefore, if N_H is the number of connected cells the number of different voltage levels per phase is $2N_H+1$.

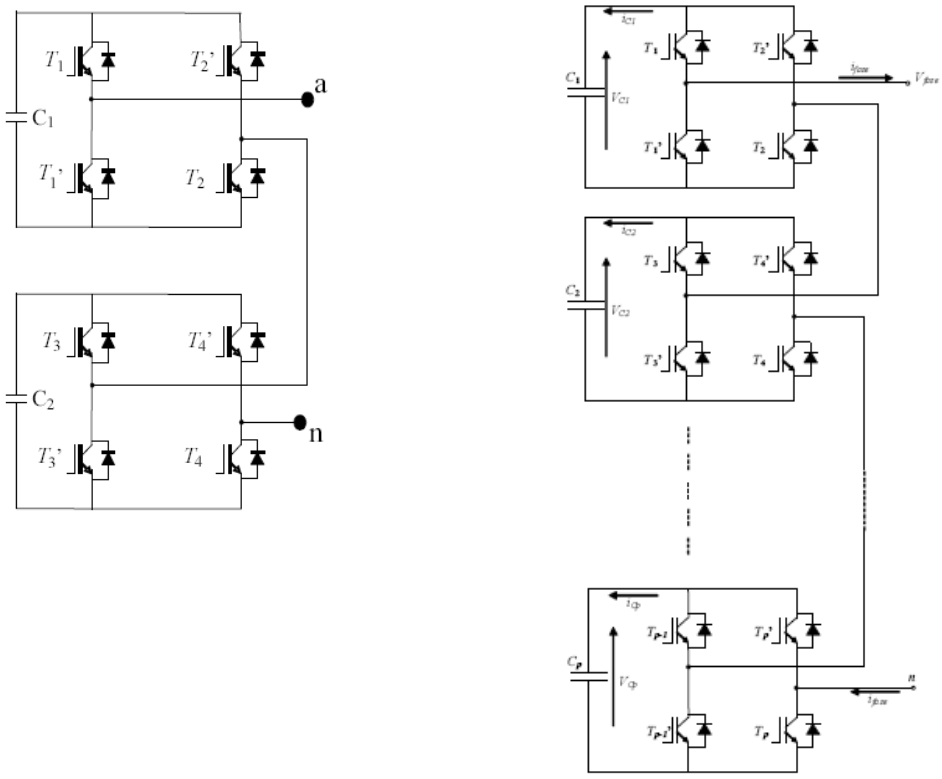


Figure 12-12: Cascaded H bridge converter. Five Levels (Leith) and n levels (right)

For a five level multilevel converter, the different conduction states are the followings:

$v_{an} = 2V_{dc}$

- When T_1, T_2, T_3 and T_4 switches conduct

$V_{an} = V_{dc}$

- When T_1, T_2, T_3 and T_4' switches conduct

- When T_1, T_2, T_3' and T_4 switches conduct

- When T_1, T_2', T_3 and T_4 switches conduct

- When T_1', T_2, T_3 and T_4 switches conduct

$V_{an} = 0$

- When T_1, T_2, T_3' and T_4' switches conduct

- When T_1, T_2', T_3 and T_4' switches conduct

- When T_1', T_2, T_3 and T_4' switches conduct

- When T_1, T_2', $T_{3'}$ and T_4 switches conduct

- When T_1', T_2, T_3' and T_4 switches conduct

- When T_1', T_2', T_3 and T_4 switches conduct

$V_{an} = -V_{dc}$

- When T_1', T_2', T_3' and T_4 switches conduct

- When T_1', T_2', T_3 and $T_{4'}$ switches conduct

- When T_1', T_2, T_3' and T_4' switches conduct

- When T_1, T_2', T_3' and T_4' switches conduct

$v_{an} = -2V_{dc}$

- When T_1', T_2', T_3' and T_4' switches conduct

Three converters can be connected in Y or Δ configurations to get a three phase voltage system.

The main advantage shown by this cascaded H bridge topology is its high modularity and flexibility to increment the number of voltage levels. In this converter, this can be achieved without increasing the complexity of the circuit.

One of the main drawbacks is the need of isolated power supplies for each DC bus. This is especially true for applications where active power is transmitted. For reactive power compensation applications this should not be a problem since there is not energy transmission to the load.

Assuming ideal DC buses and that the bus voltage of each DC bus is constant:

$$V_{c1} = V_{c2} = V_{c3} = ...V_{Cn} = V_{bus} \tag{12-16}$$

The output phase voltage respect the 0 point of the DC bus can be defined as follows:

$$V_{a0} = \left(S_{a1} + S_{a2} + S_{a3} + ... + S_{an} - n\right) \cdot V_{bus} \tag{12-17}$$

Finally, if the converter is connected to a balanced three phase system, the following single phase voltage equations are obtained:

$$V_{aN} = \frac{Vbus}{3} \cdot \left[2 \cdot \left(S_{a1} + S_{a2} + S_{a3} + ... + S_{an}\right) - \left(S_{b1} + S_{b2} + S_{b3} + ... + S_{bn}\right) - \left(S_{c1} + S_{c2} + S_{c3} + ... + S_{cn}\right)\right] \quad (12\text{-}18)$$

$$V_{bN} = \frac{Vbus}{3} \cdot \left[2 \cdot \left(S_{b1} + S_{b2} + S_{b3} + ... + S_{bn}\right) - \left(S_{a1} + S_{a2} + S_{a3} + ... + S_{an}\right) - \left(S_{c1} + S_{c2} + S_{c3} + ... + S_{cn}\right)\right] \quad (12\text{-}19)$$

$$V_{cN} = \frac{Vbus}{3} \cdot \left[2 \cdot \left(S_{c1} + S_{c2} + S_{c3} + ... + S_{cn}\right) - \left(S_{a1} + S_{a2} + S_{a3} + ... + S_{an}\right) - \left(S_{b1} + S_{b2} + S_{b3} + ... + S_{bn}\right)\right] \quad (12\text{-}20)$$

12.3.5 Neutral point clamped (NPC) – Diode Clamped converter (DCC)

The DCC or NPC topology uses series connected capacitors to divide the DC bus voltage in different levels. For n different output voltage levels, the DCC converter requires n-1 DC bus capacitors.

Figure 12-13 shows a phase of a three level NPC converter. In this scheme, the bus voltage is divided by two capacitors, C1 and C2. The middle point of the capacitors can be defined as the neutral point (n). The output voltage respect this neutral point has three different possible values depending on the conduction state of the semiconductors: $V_{dc}/2$, 0 and $-V_{dc}/2$, Table 12-3.

The presence of D_1 and D_1' diodes are the main difference between this three level converter and the well known two level converter. These diodes are the clamping diodes. By means of these diodes the neutral point can be connected to the output when T_1 and T_2' are in the blocking state and T_2 y T_1' are in conduction state.

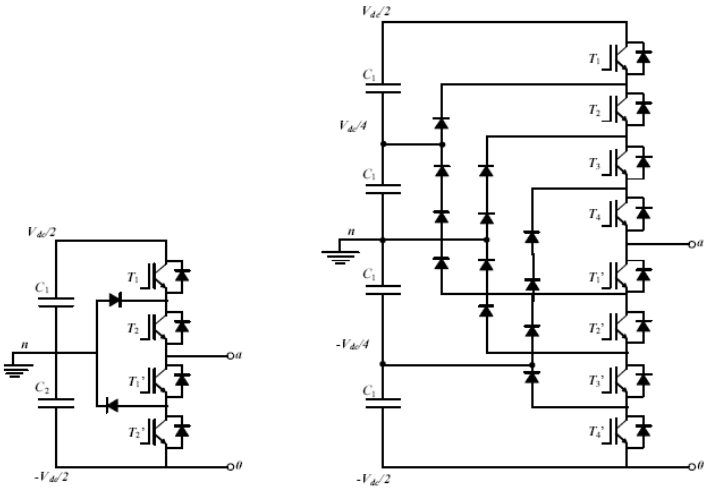


Figure 12-13: DCC topology. (a) Three level phase. (b) Five level phase.

It can be observed that there are two complementary switch pairs that can not be in conduction state at the same time. These switch pairs are T_1-$T_{1'}$ and T_2-$T_{2'}$. Besides this restriction, there are other prohibited conduction states as the simultaneous conduction of T_1

and $T_{2'}$ switches. In this condition, it is not possible to ensure the output voltage because of it will depend on the direction of the current. In addition, some switches support all DC bus voltage. This is why that the allowed conduction states of this NPC converter are the shown by Table 12-3.

Output	Switching state			
V_{an}	T_1	T_2	T_1'	T_2'
$V_{dc}/2$	1	1	0	0
0	0	1	1	0
$-V_{dc}/2$	0	0	1	1

Table 12-3: Switching state of the three level converter

In addition, there is another restriction related to the switching order. For example, in this NPC converter it is not possible to switch from an output voltage $V_{dc}/2$ to an output voltage $-V_{dc}/2$ because two series connected devices will be switched simultaneously and a voltage unbalance problem will appear.

The voltage to be supported by T_1, T_2, T_1' and T_2' switches is $V_{dc}/2$. D_1 and D_1' clamping diodes must block this voltage.

Figure 12-13 (b) shows a phase of a five level NPC converter. Four capacitors are needed to get these five voltage levels: C_1, C_2, C_3 and C_4. Each capacitor will have an operating voltage of $V_{dc}/4$. Table 12-4 shows all possible conduction values in this converter. Depending on the conduction state, the output can be connected to each DC bus capacitor voltage level.

Output	Switching state							
V_{an}	T_1	T_2	T_3	T_4	T_1'	T_2'	T_3'	T_4'
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/4$	0	0	0	1	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

Table 12-4: Switching state of the five level converter

In this way, the NPC converter can be extended to any voltage levels. However, as the number of voltage levels increases the complexity of the converter increases and the reliability decreases. In addition, the following disadvantages can be listed:

- This topology requires fast diodes able to conduct all the load current. In addition, as the number of levels increases, the reverse blocking voltage of some diodes increases, Figure 12-13.

- The duty cycle of the switches depends on the position inside the converter. As it can be seen in Table 12-4, in the five level converters the T_1 switch conducts only if the output voltage (V_{an}) is equal to $V_{dc}/2$. Similarly, T_4' switch conducts only if the output voltage (V_{an}) is equal to $-V_{dc}/2$. T_1' and T_4 show the inverse behaviour. Therefore, the outer switches conduct for less time than the inner switches. This causes an unbalanced loss distribution and in consequence the dimensioning of each switch is different.

- Similarly, the conduction cycles of the DC bus capacitors are also unequal. In consequence, if the converter is transmitting active power to the load, the discharge of these capacitors will be also unequal and voltage balance problems will appear.

If the DC bus voltages are maintained constant, the output voltage model is the same as the shown in section 12.3.4.

12.3.6 Flying Capacitor Converter

Figure 12-14 (a) shows a phase of the three level flying capacitor converter. Figure 12-14 (b) shows a single phase of the five level flying capacitor converter. In this topology the output voltage is given by the addition and subtraction of the DC bus capacitors. These capacitors are not connected to any fixed voltage point (flying capacitors).

In the Figure 12-14 (a) each capacitor has a $V_{dc}/2$ operating voltage. In consequence, the output waveform (v_{an}) can get three different values: $V_{dc}/2$, 0, $-V_{dc}/2$.

$V_{an} = V_{dc}/2$

- When T_1 and T_2 switches conduct

$V_{an} = 0$

- When T_1 and T_2' switches conduct ($+V_{dc}/2$ with C_1 and $-V_{dc}/2$ with C_2)

- When T_1' and T_2 switches conduct ($-V_{dc}/2$ with C_1 and $+V_{dc}/2$ with C_2)

$V_{an} = V_{dc}/2$

- When T_1' and T_2' switches conduct

If some switches and capacitors are added the number of voltage levels can be increased. In consequence, Figure 12-14 (b) shows one phase of the five level flying capacitor converter. In this converter, each flying capacitor operates at a $V_{dc}/4$ voltage. Therefore,

depending on the conduction state of the switches the output voltage (V_{an}) can get each of these values: Vdc/2, Vdc/4, 0, -Vdc/2, -Vdc/4.

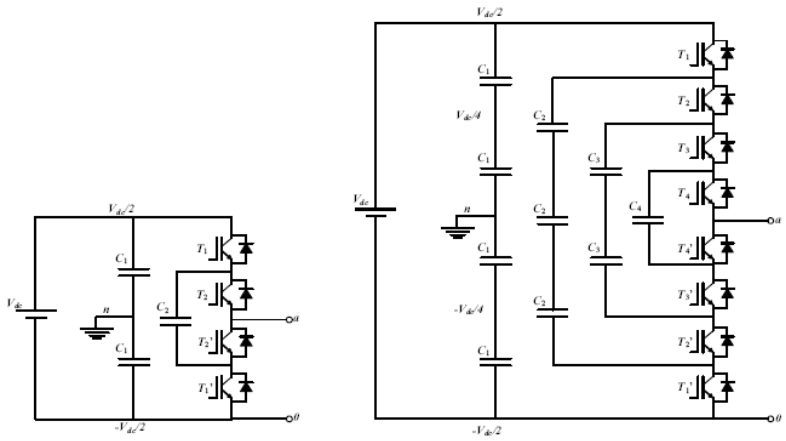


Figure 12-14: Three level phase (a), Five level phase (b)

As it can be observed above, in this topology there are redundancies for each conduction state. This increases the degrees of freedom of this topology with respect to of the DCC topology. If the conduction states are chosen properly the bus voltage balance can be achieved, even when single phase operation is required. With this topology it is possible to operate even with loads that require direct current. This topology does not need any clamp diodes, and in consequence the reverse blocking voltage of these diodes is not a problem. However, the required number of capacitors in this topology increases as the number of voltage levels increases.

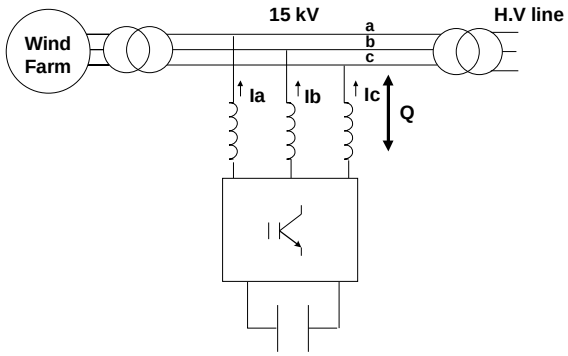
The main drawbacks of this topology can be summarized in the following points:

- The high number of redundancies makes difficult the modulation and the control of the converter.
- This topology requires higher number of capacitors than the DCC topology. On the other hand, the load current circulates across these capacitors so the RMS current value is high. Therefore, the size of the required capacitors and in consequence the size of the converter is high.

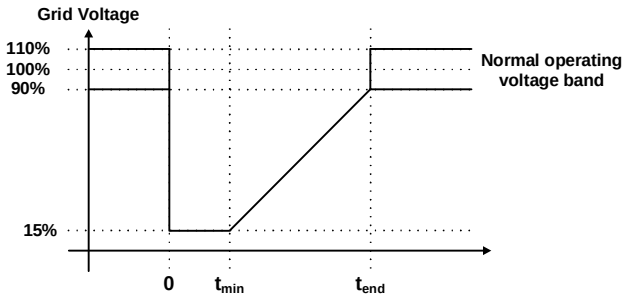
If the DC bus capacitor voltages are maintained constant (ideally) the output voltage model is equal to the shown in section 12.3.4.

13 Comparison of Voltage Source Converters for Medium Voltage STATCOM Applications

As shown in chapters 11 and 16, shunt controllers (SVCs and STATCOMs) have shown effectiveness increasing the transmittable power through transmission lines and improving the voltage profile along the transmission lines. This is achieved controlling the amount of reactive power injected to the electrical grid. In general, SVCs are based on thyristor switched reactors and/or capacitors. In consequence, the SVC provides a too slow respond to fast transient problems. In addition, the amount of compensated reactive power by a SVC is dependent on the grid voltage.



(a)



(b)

Figure 13-1: Simplified diagram of the Grid connected STATCOM (a) and LVRT requirement (b).

On the other hand, Voltage Source Converter (VSC) based STATCOMs employ self commutated semiconductors operating at higher frequencies and providing faster response to fast transient problems. This is why VSC based STATCOMs are an important part in FACTS controllers. For example, in wind energy generation, many generators use directly connected asynchronous squirrel cage machines and therefore, the use of some reactive power compensator (SVC or STATCOM) is mandatory in order to support the system voltage. However, in wind generation applications, STATCOMs have shown a better performance than SVCs as solution of the challenging Low Voltage Ride Through (LVRT) grid code requirements

in terms of transient stability margin and enhanced LVRT capability, Figure 13-1 (a) and Figure 13-1 (b) [MO-07]. A STATCOM is composed basically by a VSC, an output inductor filter and a controller. This system is connected in parallel with the load. The overall efficiency of the system and the size of the inductor are determined mainly by the type and characteristics of the used VSC.

Standard cascaded multilevel VSCs (CMC) with isolated DC capacitors as shown in Figure 13-2 (a), have demonstrated their suitability for reactive power compensation applications [BA05], [RO-07], [KO-08]. This kind of converter is formed connecting several identical H-bridge converters in series. Each H-bridge converter is a power cell. If more voltage levels are needed to work at higher voltages, more power cells should be connected in series. For reactive power compensation applications isolated power supplies are not necessary, however the complexity of the control increases specially regarding to the DC capacitors bus balance [BA-07].

In the last years, hybrid cascaded multilevel converters (HCMC) have been presented [DU-07], [MA-00]. These converters can synthesize multilevel waveforms with less power cells than classic cascaded connected converters. This can be achieved if different voltage levels are used in each series connected power cell as shown in Figure 13-2 (b). Another advantage of this kind of converter is that the highest power converter works at the output voltage fundamental frequency. Therefore, low conduction voltage drop semiconductors such as IGCTs could be used to improve the performance of the converter. The lowest power cell can use fast switching devices such as IGBTs. In consequence, this converter could show an improvement on the system efficiency compared with standard cascaded connected converters.

However, there is not any comparison that demonstrates the superior characteristics, limitations, advantages or disadvantages of the hybrid cascaded multilevel converters. For this reason, in this chapter standard and hybrid seven level VSCs are analyzed and compared for 26 MVA STATCOM applications in a 15 kV utility grid. Because of the limited voltage-blocking capability of actual power semiconductors (IGBTs, IGCTs and diodes) the use of series connected devices is assumed. Therefore, the converter could operate at High Voltages without increasing the number of power cells and therefore the control and design complexity. In addition, these converters are also compared with commercially available 2 Level VSC [WE-01], Figure 13-2 (d) and 3 Level NPC VSC [GR-99], Figure 13-2 (c).

In consequence, this chapter is divided in two main parts. The first part deals with the design of the converters while the second part deals with the comparison of the converters.

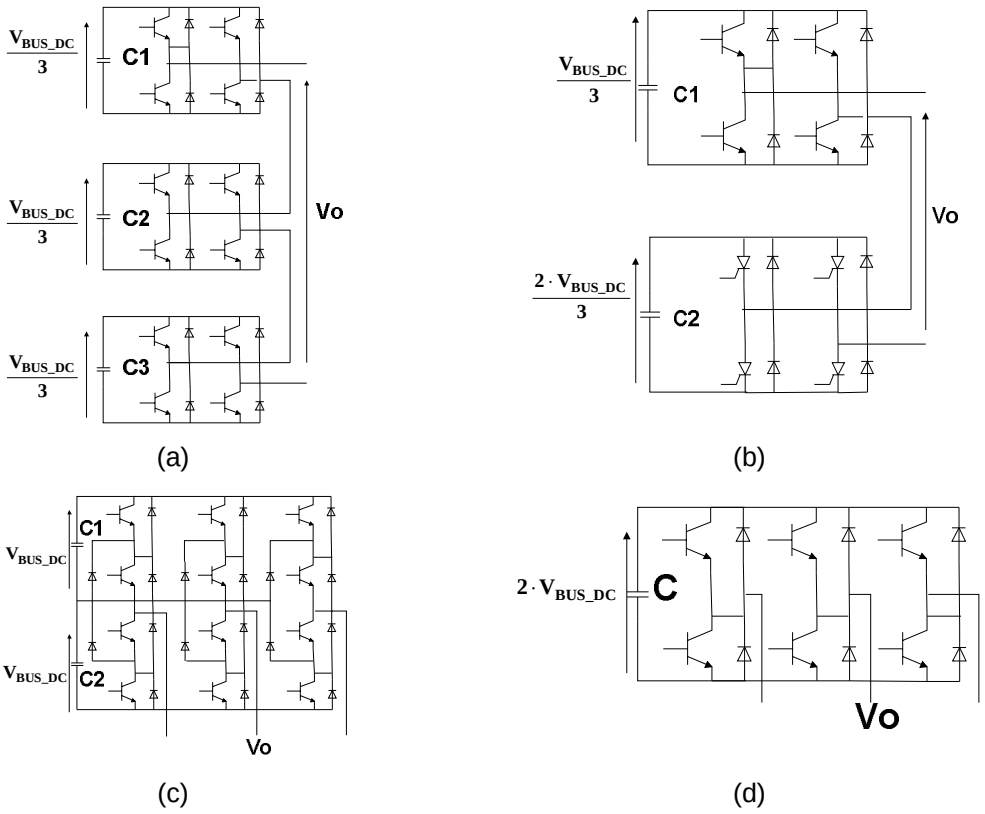


Figure 13-2: 7L CMC –1phase, 7L HCMC–1phase, 3L NPC-3phase, 2L-3phase VSCs.

13.1 Compared converters

Figure 13-2 shows the compared VSC topologies. Each phase of the Seven Level CMC converter is composed by three switching cells. Each cell has a DC bus capacitor and four fully controlled switching devices (IGBTs) with their free wheeling diodes. In this work, it is considered that this converter operates with a PSPWM modulation [LE-07]. Each phase of the Seven Level HCMC converter has only two switching cells. However, the bus voltage of one cell is two times higher than the voltage in the other cell. Therefore, it is possible to obtain 7 voltage levels in the output voltage waveform. This High Voltage cell operates at output waveform fundamental frequency while the lowest voltage cell is modulated with a high frequency PWM [LU-99]. For comparison purposes, commercially available three phase two level and three level VSC converters are also analyzed and compared. Table 13-1 shows the chosen semiconductor devices to be used in the compared converters.

13.2 Converter dimensioning

The converters are dimensioned in order to operate as 26 MVA STATCOMs at 15 kV utility grids (8.6 kV_{RMS}, 1000 A_{RMS} per phase). A potential 10% overvoltage is assumed for the grid voltage. During the dimensioning of the converters the effect of the control in the size of passive components is not considered. It means that the size of calculated passive components

could be optimized considering the control of the converter. A PWM modulation has been assumed to obtain the following analytical expressions.

a) Output inductor filter dimensioning

The output inductor filter is calculated in order to minimize the output current ripple. Equivalent output switching frequency (f_{sw}), number of voltage levels (N), DC bus voltage (V_{DC}), the current ripple (ΔI) and the duty cycle (α) are the needed parameters. A 10% current ripple is considered for a 50% of duty cycle which is the worst case [BA-05].

$$L_{min} \approx \frac{2 \cdot V_{DC} \cdot (1-\alpha) \cdot \alpha}{3 \cdot (N-1) \cdot \Delta I \cdot f_{sw}} \tag{13-1}$$

From (13-1) it can be seen that the output filter size can be reduced increasing the number of voltage levels or increasing the output switching frequency.

b) Bus voltage calculation

The DC bus voltage can be estimated assuming the steady state expressions related to the VSC operating as reactive power compensator. It can be seen that a lower sized output filter allows a lower DC bus voltage.

$$V_{BUS\_DC} \approx \left(V_{ph\_max} + I_{ph\_max} \cdot L \cdot \omega\right) \tag{13-2}$$

c) DC Bus Capacitors

The DC bus capacitor value has influence on the control bandwidth, the DC bus voltage ripple and the output voltage and current harmonic content [BA-05]. It can be demonstrated that in the DC bus voltage of a 2 Level three phase converter there is not any voltage ripple because of the reactive power exchange. Therefore a small capacitor is enough for maintain the DC bus voltage constant. In general, this capacitor is dimensioned to provide the maximum power (P_n) for a switching period ($1/f_{sw}$).

$$C \approx \frac{2 \cdot P_n}{\left(V_{BUS\_max}^2 - V_{BUS\_min}^2\right) \cdot f_{sw}} \tag{13-3}$$

However, in the other compared converters the reactive power (Q) exchange has an influence on the voltage ripple (V_{rx}) and therefore those capacitances have to be dimensioned attending the compensated reactive power. Equations (13-4) to (13-7) are used to calculate the

required capacitor values for 3 Level NPC (3LNPC), 7 Level Standard (7LCMC) and 7 Level Hybrid (7LHCMC) multilevel converters respectively [BA-05].

$$C_{3LNPC} \approx C_1 \approx C_2 \approx \frac{Q_{3ph}}{3 \cdot \omega \cdot V_{dcx} \cdot V_{rx}} \tag{13-4}$$

$$C_{7LCMC} \approx C_1 \approx C_2 \approx C_3 \approx \frac{Q_{ph}}{3 \cdot \omega \cdot V_{dcx} \cdot V_{rx}} \tag{13-5}$$

$$C_{1-7LCHMC} \approx \frac{Q_{ph}}{3 \cdot \omega \cdot V_{dc1} \cdot V_{r1}} \tag{13-6}$$

$$C_{2-7LCHMC} \approx \frac{2 \cdot Q_{ph}}{3 \cdot \omega \cdot V_{dc2} \cdot V_{r2}} \tag{13-7}$$

It should be noted that the capacitor for 2 and 3 Level converters is dimensioned for three phase operation while in cascaded converters the capacitor is dimensioned for a single phase operation.

d) Number of needed semiconductors

Because of the bus voltage levels, each switching valve is composed by series connected semiconductors. The IGBTs are connected in series by an active gate control method described in [BA-08]. Small snubbers are used (220nF) to improve voltage unbalance caused by non controllable parameters such as tail current, diode recovery charge, etc. IGCTs are connected in series by 1μF snubber.

When semiconductors are connected in series the voltage balance in the blocking state is not perfect. For this reason, the maximum blocking voltage of each semiconductor (V_{100FIT}) uses to be derated by a security factor (f_s) to ensure that all semiconductors operates under their 100 FIT (Failure In Time) reliability voltage. In addition, at least one redundancy (r) is considered to guarantee that the switching valve still operates when a failure in any semiconductor occurs. This is only useful when short circuit failure mode occurs, which is guaranteed only by press pack housings. In consequence, the number of semiconductors per switching valve (n_s) is determined by the following expression:

$$n_S = \frac{Vbus}{V_{100FIT} \cdot f_s} + r \tag{13-8}$$

The considered semiconductors in this comparison are shown in Table 13-1. The installed switching power gives us an idea of the expense for the semiconductors. According to [BE-07] the installed switching power can be calculated with:

$$S_S = V_{CE} \cdot I_C \cdot n_s + 0.5 \cdot V_{RRM} \cdot I_F \cdot k \tag{13-9}$$

Device	Model	Manufacturer	Vmax (V)	V_{100FIT} (V)	I_c (A)
$Diode_{IGBT}$	T1800GA45A	Westcode	4500	2800	1800
IGBT	T1800GA45A	Westcode	4500	2800	1800
$Diode_{IGCT}$	5SDF 13H4501_5SYA	ABB	4500	2800	1200
IGCT	5SHY35L4512	ABB	4500	2800	4000

Table 13-1: Considered semiconductors

For the 3 Level NPC converter the switching power of the clamp diodes should be considered. In the same way, the relative installed switching power (S_{SR}) allows a fast comparison between the required switching powers by the compared converters (13-10). While S_S denotes the installed switching power, $S_{Sreference}$ denotes the installed switching power of the reference converter.

$$S_{SR} = \frac{S_S}{S_{Sreference}} \cdot 100 \tag{13-10}$$

e) Power losses estimator

There is no doubt that one of the most important comparison aspects between several converters is the efficiency. In order to evaluate the overall power losses of each VSC, a power losses estimator has been developed, which has been programmed in MAST and simulated in SABER.

Basically, the power losses estimator finds the operating point of each semiconductor (on state, off state, switch on, switch off) and calculates the losses concerning to that operating point. The estimation is performed using the information provided by manufacturers and the current and voltage measured in the simulation circuit. The addition of the losses of each operation state gives an estimation of the overall real power losses. Conduction losses are estimated assuming a first order approach for the output characteristic of the semiconductor. Then, the instantaneous conduction losses can be estimated if the dynamic resistance (r_d), the threshold voltage (v_{th}) of the output characteristic and the current (I_F) across the semiconductor are known.

$$p_{cond}(t) \approx v_{th} \cdot I_F(t) + I_F^2(t) \cdot r_d \tag{13-11}$$

Once the switch on or switch off process has been started the estimator measures the current to switch and uses it to calculate the switching losses of the device. If the switched voltage is not the same than the used by the manufacturer during their tests, switching losses can be linearly adapted to the switched voltage. Therefore, switching losses can be calculated with the following expressions:

$$P_{on} \approx \frac{I_{sw}^2 \cdot C_{on\_2} + I_{sw} \cdot C_{on\_1} + C_{on\_0}}{t_{on}} \cdot \frac{V_{sw}}{V_{test}} \quad (13\text{-}12)$$

$$P_{off} \approx \frac{I_{sw} \cdot C_{off\_1} + C_{off\_0}}{t_{off}} \cdot \frac{V_{sw}}{V_{test}} \quad (13\text{-}13)$$

f) Thermal Model

The average overall power losses can be calculated if the instantaneous power losses are known (13-14).

$$P_{AV} = \frac{1}{T} \cdot \int \left(P_{cond} + P_{on} + P_{off}\right) \cdot d\tau \quad (13\text{-}14)$$

If the thermal resistance between the junction and the case (R_{thJC}) and the case temperature (T_C) are known, it is possible to estimate the average junction temperature (T_J).

$$T_J = T_C + P_{AV} \cdot R_{thJC} \quad (13\text{-}15)$$

Table 13-2 shows the considered parameters for the simulations. Losses generated by snubber circuits are also considered during simulations but they are not shown in Table 13-2.

Device	$Diode_{IGBT}$	IGBT	$Diode_{IGCT}$	IGCT
Model	T1800GA45A	T1800GA45A	5SDF 13H4501	5SHY35L4512
v_{th} (V)	1.27	1.86	1.3	1.1272
r_d (mΩ)	1.48	1.483	0.48	0.216
Coff_1	0.00178	0.0028	0.00125	9.2529e-3
Coff_0	0	-0.0519	0	0.1656764
Con_2	0	-3.2297e-6	0	0
Con_1	0	0.0047	0	3.75e-4
Con_0	0	0.0073	0	0
Rthjc (ºK/Kw)	13.8	7.7	12	8.5

Table 13-2: Semiconductor parameters

13.3 Converter comparison

In this section, the converters are compared in terms of designing aspects, output voltage waveform quality and efficiency. The output filter, the energy stored in DC bus capacitors, the efficiency at different conditions and the effect of a second redundancy in the switching valves are analyzed and compared.

a) Output filter size

The output filter inductance has been designed for an 1800 Hz output apparent switching frequency for each converter. According to the analytical expressions described in

section 13.2 the highest number of voltage levels allows the lowest output inductor size. This can be verified in the values shown in Table 13-3. It can be seen that 7 level converters need an output filter inductor size 3 times lower than 3 level converters and 6 times lower than 2 level converters. This provides us an idea of the relative cost and size of the required filters.

b) Installed switching power

A lower inductor size causes a lower voltage drop when the output current circulates across it. According to (13-2), the DC bus voltage has to be high enough to make possible the circulation of this current. Because of the lowest output inductor size and the phase structure of the converter, 7 Level converters need the lowest DC voltage, followed by 3 Level converters and 2 Level converters, Table 13-3. It is interesting to observe how the Hybrid 7 level converter is composed by the lower number of components in order to operate at the required DC bus voltages. In general, this is an advantage in terms of reliability. However, due to the use of IGCTs (high current capacity devices) the installed switching power is considerably higher in this converter. Generally, the installed switching power can be considered an image of the cost of the installed semiconductors. 2 Level and CMC 7 Level converters have the lowest installed switching power (40.3% less than the HCMC converter). Due to the clamps diodes, the 3 Level NPC converter has an 18.5 % higher installed switching power than 2 Level converters as shown in Table 13-3.

	2L	3L NPC	7L CMC	7L HCMC
L_{output} (mH)	17.6	8.8	2.9	2.9
V_{bus}DC (kV)	42.6	34.7	15.4	15.4
$n_{s\text{-}perphase}$(total)	72 (216)	80 (240)	72 (216)	64 (192)
S_{Sphase}(MVA)	437.4	518.4	437.4	613.8
S_{Rphase}(%)	100	118.5	100	140.3
$Energy_{DC}$ (KJ)	65	275.868	413.802	413.802

Table 13-3: Calculated parameters

c) Energy stored in DC bus capacitors

The energy stored in the DC bus gives an idea of the expense of the DC bus capacitors. Ideally, 2 Level converters do not need any bus capacitor for reactive power compensation so it can be used with small capacitances. 3 Level NPC converter needs only 2 capacitors per three phase operation while standard and hybrid cascaded converters need 9 and 6 capacitors respectively for three phase operation. Both converters store the same amount of energy, Table 13-3.

d) Efficiency and loss distribution at equal first carrier band frequency

Without any doubt, the power losses and efficiency are two of the most important parameters to be compared between converters. Overall power losses can be divided mainly in two groups: Conduction and Switching losses. In general, at low switching frequency operation conduction losses are dominant while at high frequency operation, switching losses become more important. In this first comparison an equal output switching frequency (1800 Hz) is assumed for all converters. Assuming that the switching frequency is an image of the dynamic performance of the converter, the efficiency of each converter for a given dynamic performance is compared. Table 13-4 shows the power losses distribution of each converter. 7 Level Hybrid VSC, 3L NPC VSC and 2 Level VSC have higher switching losses than conduction losses for the given operating conditions. At the test conditions the 7 Level CMC shows bigger conduction losses than switching losses.

	2L	3L NPC	7L CMC	7L HCMC
$P_{Total1phase}$ @ 1.8 Khz (Kw)	344	177.6	82.432	76.33
P_{cond} (Kw)	51	44.2	51.880	31.93
P_{sw} (Kw)	276	129.8	29.241	42.77
$P_{Total3phase}$ @ 1.8 Khz (Kw)	1023.7	533.28	247.29	229.0
η (%)	96.06	97.94	99.09	99.12

Table 13-4: Efficiency comparison at 1.8 kHz

Figure 13-3 shows the overall losses for each converter. As it is shown, 7 Level VSCs have similar power losses which are approximately 2 times lower than the losses of the 3 Level VSC and 4 times lower than the losses of the 2 Level converter. An important aspect of this first comparison resides in the efficiency obtained for both 7 Level cascaded converters. Theoretically, due to the less number of components, the hybrid multilevel converter should show a considerably better performance than the Standard converter, but at the considered operating conditions the losses are almost equal. Table 13-5 shows the loss distribution for both converters. As it could be expected, conduction losses are considerably lower in the hybrid converter. However, the bigger switching losses (IGBT losses plus IGCT losses) make the overall efficiency of both converters almost equal.

	7L CMC	7L HCMC
IGBT / Diode $_{Conduction}$	51880	17430
IGBT / Diode $_{Switching}$	29241	34780
IGCT / Diode $_{Conduction}$	0	14500
IGCT / Diode $_{Switching}$	0	8000

Table 13-5: Power losses distribution on 7 Level converters

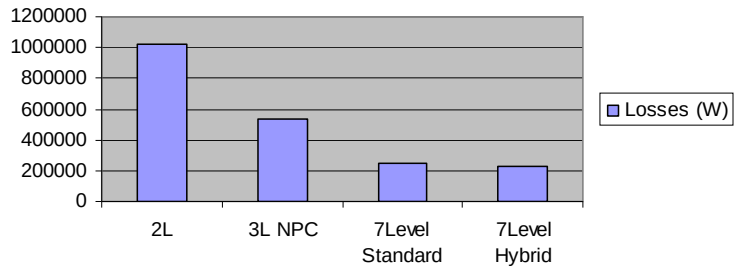


Figure 13-3: Power losses at 1800 Hz.

e) Maximum switching frequency for a given junction temperature

Table 13-5 shows that one IGBT switching cell in the hybrid converter generates more than three times higher switching losses than each IGBT cell of the Standard VSC. This power losses concentration in few components makes the junction temperature of IGBT/Diode-s of the hybrid converter higher than the temperature of the IGBT/Diodes in the Standard converter. Therefore, in order to operate with a junction temperature lower than the maximum recommended by the data sheet, the maximum switching frequency of the converter has to be limited.

In this case several simulations have been performed maintaining the maximum output current and increasing the switching frequency of the semiconductors until one semiconductor reaches its maximum junction temperature (125ºC). The heat sink temperature has been maintained constant at 80ºC [KR-07].

	2L	3L NPC	7LCMC	7LHCMC
$f_{semiconductor}$(Hz)	1250	3400	2000	1725
f_{output}(Hz)	1250	3400	12000	3450

Table 13-6: Semiconductor Switching Frequency and Output Switching Frequency for a given T_{JMAX}

As it can be seen in Table 13-7 and Figure 13-4, the Standard 7 Level converter has a maximum switching frequency of 2 kHz per switching cell. In consequence, due to the PSPWM modulation the output switching frequency is 12 kHz, which can be considered a very high apparent output switching frequency. A similar maximum switching frequency per switching cell is obtained in the hybrid converter, however, in this case the apparent output switching frequency is only 3.4 Khz, which is considerably lower than in the standard converter. In the 3 Level converter the maximum switching frequency is limited to 3.4 Khz while in the 2 Level converter only 1.2 kHz are obtained.

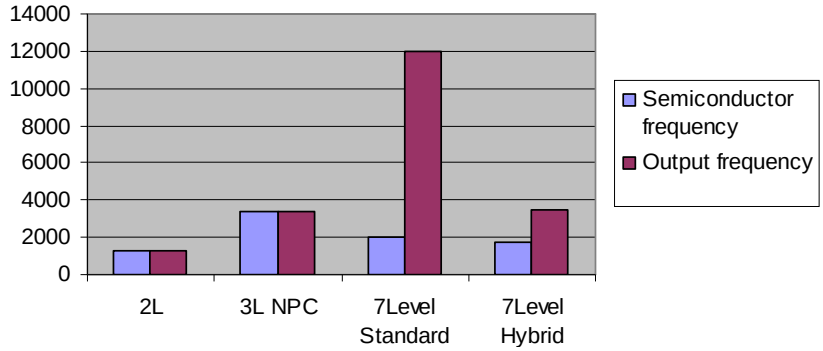


Figure 13-4: Semiconductor Switching Frequency (Hz) and output switching frequency (Hz) for a given T_{JMAX}.

	2L	3L NPC	7L CMC	7L HCMC
$F_{99\%}$(Hz)	187.5	556	2082	2282
$f_{96\%}$(Hz)	1821.7	4322	17588	18244

Table 13-7: Maximum output switching frequency for a given efficency

f) Maximum output switching frequency for a given efficiency

The switching frequency is related to the system dynamic and the output waveform quality. In this section, the maximum output switching frequency for a given efficiency is calculated and compared.

Several simulations have been performed in order to find the switching frequency in which 99% and 96% efficiency are obtained. Table 13-7 and Figure 13-5 show the obtained results. As shown in Figure 13-5, the hybrid converter allows the maximum output frequency for a given efficiency closely followed by the standard cascaded converter. 3 Level and 2 Level converters have a much lower operating frequency than the 7 Level converters.

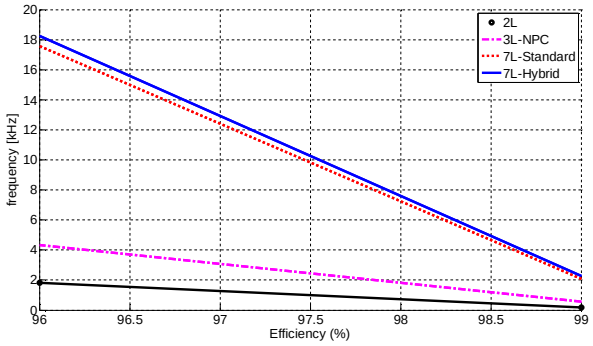


Figure 13-5: Maximum switching frequency for η = 96 %.

g) THD / WTHD at a given efficiency

Total Harmonic Distortion (THD) reflects energy of the waveform harmonic content. High order harmonics in general are easier to filter than low order harmonics. However THD does not consider the difference between harmonic orders. Weighted THD (WTHD) gives a better measure of harmonic pollution by using the order of each harmonic component as its weight factor. In this section the THD and WTHD are calculated for each converter at given efficiencies of 99% and 96%. This can give an idea of the expense in terms of efficiency of the waveform quality. Figure 13-6 shows the line to line voltage waveforms and their harmonic content. As it could be expected, a higher number of voltage levels and a higher apparent switching frequency lead to a lower harmonic content and therefore to an improved waveform quality.

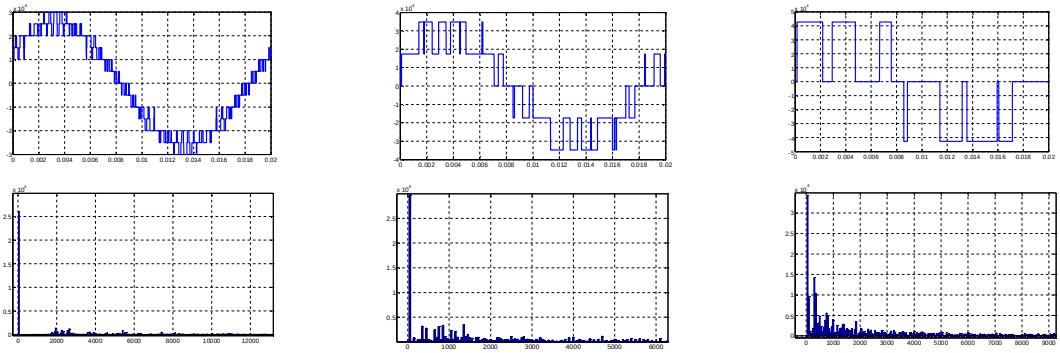


Figure 13-6: 7L, 3L and 2L line to line voltage waveform and Harmonic content for 99% efficiency.

Table 13-8 shows the THD and WTHD for each converter at 99% and 96% of efficiency. It is observed that the WTHD of 7 Level converters are much lower than the 2 Level and 3 Level converters. The reason could be found in the number of levels and the higher switching frequency in which these efficiencies are measured.

	2L	3L NPC	7L CMC	7L HCMC
THD (96%)	68.1	43.56	14.096	14.091
WTHD (96%)	1.33	0.27	0.044	0.045
THD (99%)	76.298	35.33	14.97	15.01
WTHD (99%)	16.7	2.6	0.3	0.27

Table 13-8: Harmonic distortion for a given efficiency

h) Increase of overall losses due to a second redundancy

When high reliability is required, more than one redundancy could be used per switching valve. Due to the different number of switching valves in each topology, an increase of redundancies could have a different influence in the overall efficiency. In consequence the 7

Level Standard converter has 12 switching valves, the 7 Level Hybrid converter has 8 valves, the 3 Level NPC converter has 6 valves and the 2 Level converter has 2 valves per phase. Therefore, 12, 8, 6 and 2 components are added respectively to get the second redundancy. Table 13-9 shows the installed switching power and the efficiency when two redundancies are used per switching valves. It can be seen again that the hybrid 7 Level converter has still the highest installed switching power while the 2 Level converter has the lowest installed switching power. In addition, it could be observed that with two redundancies the hybrid converter has still the highest efficiency. It is very interesting to observe how the efficiency of the 7 Level Standard converter is lower even than the efficiency of the 3 Level converter. This can be understood taking into account the high number of extra components added for the second redundancy.

	2L	3L NPC	7L CMC	7L HCMC
S_{Sphase} (MVA)	461.7	583.2	583.2	756
η (%)	96.06	97.9	97.06	98.6

Table 13-9: Installed switching power and efficiency with 2 redundancies

i) Spider Chart Comparison

Finally, the obtained results have been normalized and fitted between 0 and 5 points. These values have been plotted in a Spider Chart in order to make the comparison between all converters easily. A compared parameter is better when the score is close to 5 and worse if the score is close to 0. Therefore, it could be said that a converter is better as it takes bigger area in the chart. The Spider Chart shown by Figure 13-7 depicts the magnitudes compared in chapter 13.3 from section (a) to section (h).

Both 7 Level Converters have a considerably bigger area in the chart than the commercially available converters. It shows the superior characteristics of these 7 Level converters. Although better values could be expected of the Hybrid converter due to the reduced number of components, it does not show a clearly better Spider Chart than the Standard Converter. In terms of efficiency, the Hybrid converter is only slightly better than the Standard converter while in terms of installed switching power (semiconductor cost) and maximum allowable dynamic performance for a given junction temperature the hybrid converter shows a worse score. Only when two redundancies are considered the hybrid converter shows clearly the best performance in terms of efficiency.

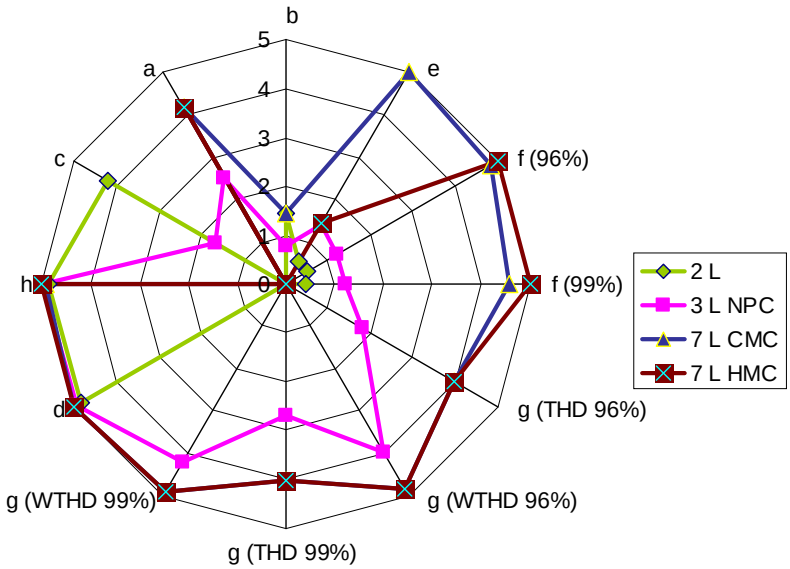


Figure 13-7: Spider Chart for each converter.

13.4 Conclusion

In previous chapters the series connection of IGBT devices has been analyzed. In addition, a gate driver has been designed to achieve a proper voltage balance. In this chapter different converter topologies have been analyzed for STATCOM applications. In these applications the series connection of power devices is necessary due to the operating voltage level. This analysis links the previous study of series connection of power semiconductors with several possible applications and converter topologies.

For this study, four Voltage Source Converters operating as 26MVA STATCOMs at 15 kV utility grids have been dimensioned and compared. The compared converters are 2 Level VSC, 3 Level NPC, 7 Level Cascaded VSC and 7 Level Hybrid VSC. The comparison has been done mainly in terms of components size, waveform quality and efficiency.

The high number of voltage levels of cascaded converters, Standard and Hybrid, makes possible the use of small output inductor filters. This is an advantage not only on the size and cost of the filter itself, but the required DC bus voltage is lower than 2 Level and 3 Level converters. This has a direct influence on the number of required components and the overall power losses. The hybrid cascaded converter needs the lowest number of components which is beneficial in terms of reliability. However, the use of IGCTs increases the installed switching power which could be understood as an image of the cost of the used semiconductors. Both Cascaded 7 Level converters have the same amount of energy in their DC bus capacitors. This energy is higher than the energy in 3 Level and 2 Level converters. It means that the most

expensive DC buses belong to Cascaded converters. In terms of efficiency the Hybrid 7 Level VSC is the best choice. According to the considered power losses, this converter shows a slightly better efficiency than the Standard 7 Level converter when one redundancy is considered. 2 Level converter is not a competitive choice to operate at this voltage and power levels. Although the 3 Level converter shows a better performance than the 2 Level converter, its performance is considerably worse than the performance of Cascaded 7 Level converters. It is interesting to note that in the 7 Level hybrid converter almost all switching losses are concentrated in few semiconductors, which limits the maximum switching frequency of the converter. In this aspect, the Standard 7 Level converter is without any doubt which shows the best performance. On the other hand, when high reliability is required and more than one redundancies are used (for example 2), the Cascaded multilevel converter has a worse performance even than the 3 Level converter. This is due to the high number of switching devices used in this topology. In terms of output voltage waveform quality, as it could be expected, 7 Level Converters are the best choice. Thanks to the number of voltage levels and higher switching frequency they show a much better waveform quality at a given efficiency than 3 and 2 Level converters. In general, it could be said that the hybrid converter has some operating advantages and limitations compared with the Standard cascaded converter. The selection of one or another converter depends on the final cost, required dynamic performance, reliability etc.

14 Conclusions & Future Prospects

The contributions of this PhD are related to the development of an active gate driver to achieve a proper voltage balance between series connected IGBT devices. The main work has been focused on the modelling, analysis and the control of the switching behaviour of the IGBT.

The IGBT and the IGCT are the preferred power devices for Medium Voltage Applications. Their market penetration has been higher than the others semiconductor structures as ETO thyristors (Emitter Switch Off Thyristor) or IEGT transistors (Injection Enhanced Gate Transistor). Due to its controllable switching behaviour and low gate energy requirements the IGBT is the preferred choice when a high number of power devices must be connected in series. These characteristics allow the series connection of several IGBTs without using lossy snubber networks. Most of the commercially available devices are based on Silicon technology. Although Silicon has worse thermal and electrical characteristics than other materials with higher bandgap (as Silicon Carbide), the current technology is not able to commercially exploit all the possibilities of those newer materials.

The proposed behavioural IGBT and diode models have been validated by a reasonable good agreement with measurements. Those models are relatively simple to synthesise and parameterize. Simulation speed and convergence are acceptable especially if few elements are used. However, both characteristics should be improved to simulate high number of IGBT and diode components at the same time. In addition, the IGBT tail current, the diode forward recovery voltage, improvements on the interelectrode capacitance models, etc should be also considered for future models.

From the analysis of the dynamic behaviour of the IGBT it is concluded that the IGBT is a charge controlled device during the switching process and therefore, if the gate charging process is controlled the switching behaviour is controlled. The voltage driving modes comparison unveils that the current mode gate driving is better suited to control the charge profile of the gate terminal during the switching process. Ideally, if the gate current is controlled, the switching speed can be controlled independently of the IGBT characteristics or operating conditions. This makes current mode driving suitable for the series connection of IGBTs where the voltage slope control is required.

In this work, a gate driver has been designed and developed which is able to control the switching process of the IGBT. The developed gate driver determines the gate charge profile during the switching process to satisfy the reference time requirements. This control idea has been successfully experimentally validated during this PhD and promising results have been obtained.

However, further improvements should be performed in the gate driver layout and FPGA implementation to achieve higher relialability. In addition, the excessive number of current levels to control during the switching process should be reduced to obtain a faster convergence. The reduction in the number of current levels would simplify the pre-programmed gate currents initialization and in consequence, improve the reliability of the driver.

Exhaustive tests and improvements should be performed to guarantee that the switching process is controlled under all operating conditions. This is probably the most challenging future prospect of this work.

Switching valves formed by series connected semiconductors have high applicability in Medium and High Voltage applications. Utility grid and Industrial applications can exploit the voltage blocking capacities of these switching valves. If these devices are used in multilevel Voltage Source Converters, high waveform quality, good performance and relatively low converter control and design complexity can be achieved. Future work should be focused also on the experimental validation of the switching valve in real power applications.

During the development of this PhD research work, the following papers have been presented:

- Baraia I, Galarza J., Barrena J.A., Canales J.M. "**An IGBT Behavioural model base on curve fitting methods**". PESC 2008. Island of Rhodes (Greece).

- Baraia I, Galarza J., Barrena J.A., Canales J.M. "**Control Activo por puerta para la conexión en serie de IGBTs**". SAAEI 2008. Cartagena (Spain).

- Baraia I, Galarza J., Barrena J.A., Sanzberro M. "**Comparison of Voltage Mode Driving and Current Mode Driving of IGBTs**". SAAEI 2008. Cartagena (Spain).

- I.Baraia, J.L.Thomas, J.A.Barrena, J.Galarza, M.A.Rodriguez. "**Efficiency Comparison between a Hybrid Cascaded Connected Seven Level Converter and a Standard Cascaded Connected Seven Level Converter for STATCOM Applications at 15 kV Utility Grids**". EPE 2009. Barcelona (Spain).

- I.Baraia, J.A Barrena, J.M Canales, J. Galarza. "**Review and Analysis of the Problems Related to the Series Connection of IGBTs**". ECMS 2009. Mondragón (Spain).

15 Appendix A: Behavioural Diode Model

The behavioural diode model considers the forward characteristic and the reverse recovery characteristic. This model does not consider the junction capacitance which has influence on switching oscillations. Similarly, this model does not consider the forward recovery behaviour of the diode. The required parameters for characterization are available on data sheets.

In a diode, the conductance is determined by the operation point over the output characteristic. This characteristic can be described as an exponential function [ECE-570] [CO-95] that depends basically on the leakage current (I_S) and the anode-cathode voltage (V_{AK}):

$$I_d \approx I_s \cdot \left(e^{\frac{V_{AK}}{n \cdot V_T}} - 1 \right) \tag{15-1}$$

The reverse recovery characteristic describes the behaviour of the diode when being forward biased is abruptly reverse biased. The recombination process of the carriers in each p-n Silicon region causes the ciculation of an inverse current. This current is known as the reverse recovery current (Irm).

15.1 Forward Characteristic

The forward characteristic of the diode determines the operating voltage as a function of the current across the diode, Figure 15-1.

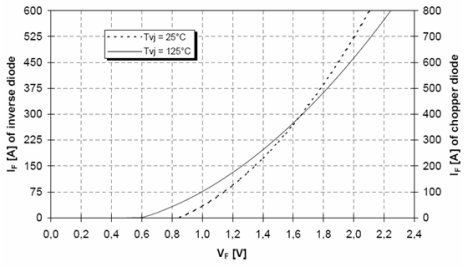


Figure 15-1: Forward characteristic of the Diode (FD300R12KE3)

This curve can be approached by means of a quadratic function:

$$I_{f\_ak} = k \cdot \left(v_{ak} - v_{th} \right)^2 \Rightarrow \forall \left(v_{ak} \geq v_{th} \right) \tag{15-2}$$

Where K is a curve fitting parameter and v_{th} is the threshold voltage of the diode. Both parameters are temperature dependent and can be expressed by the following equations:

$$v_{th} = v_{th\_25} \cdot \left(1 + \alpha_{vth} \cdot \left(T_j - 25^o\right)\right) \quad (15\text{-}3)$$

$$k = k_{25} \cdot \left(1 + \alpha_k \cdot \left(T_j - 25^o\right)\right) \quad (15\text{-}4)$$

Where α_k and α_{vth} are the temperature coefficients of k and v_{th} respectively.

15.2 Reverse recovery characteristic

The reverse recovery characteristic model used in this PhD research work is based on [CO-95].

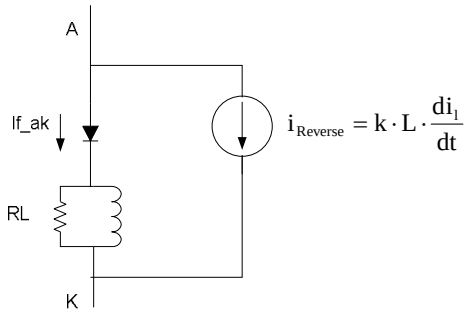


Figure 15-2: IGBT model considering the reverse recovery behaviour

The reverse recovery model proposed by [CO-95] uses a resistor (RL), an inductor (L) and a current source ($i_{Reverse}$). During the conduction state the forward characteristic of the diode imposes the circulating forward current (I_{f_ak}) depending on the operating voltage (V_{AK}). The values of L and RL must be low enough to get a negligible voltage drop in RL.

During the switch off process, the current slope causes a voltage drop in the inductor (L). If this voltage drop is high enough (hard switching), the diode voltage becomes negative and the forward current (i_{f_ak}) is extinguished. The inductance current circulates across the resistor (RL) and the current source injects a current ($i_{Reverse}$) proportional to the inductor voltage (which is an image of the current slope). This is the reverse recovery current.

When the reverse recovery current has been extinguished, the diode recovers its voltage blocking capacity. This behaviour is modelled by the following equations:

$$I_{f\_ak} = i_L + \left(\frac{L}{RL} \cdot \frac{di_L}{dt}\right) \quad (15\text{-}5)$$

$$i_{Reverse} = K \cdot L \cdot \frac{d(i_L)}{dt} \tag{15-6}$$

Where K and L/RL are given by the following expressions:

$$\frac{L}{RL} = \frac{1}{\ln 10} \times (t_{rr} - I_{rm}(\frac{dI_r}{dt})^{-1}) \tag{15-7}$$

$$K = \frac{I_{rm}}{L} \cdot \left(\frac{dI_r}{dt}\right)^{-1} \cdot \left[1 - \exp\left(\frac{-I_{Fo} - I_{rm}}{L \cdot \frac{dI_r}{dt} \cdot \left(K + \frac{1}{RL}\right)}\right)\right]^{-1} \tag{15-8}$$

Most datasheets provide the required information for a proper characterization of this reverse recovery behaviour. In order to guarantee that the proposed model has solution the following conditions must be satisfied ((15-9), (15-10) and (15-11)):

$$Qrr < \frac{t_{rr}^2}{2} \cdot \frac{dI_r}{dt} \tag{15-9}$$

$$I_{rm} < t_{rr} \cdot \frac{dI_r}{dt} \tag{15-10}$$

$$Qrr > \frac{I_{rm}^2}{2} \cdot \left(\frac{dI_r}{dt}\right)^{-1} \tag{15-11}$$

If the forward and reverse currents are known the total diode current can be calculated:

$$I_{AK} = I_{f\_ak} + I_{Reverse} \tag{15-12}$$

15.3 Simulation results

Figure 15-3 shows the used circuit to simulate the proposed diode model. In these simulations the diode is abruptly reverse biased with the current slope given by the data sheets. The modelled diode is the FD300R12KE3 (Eupec). Once the diode is switched off, the extracted charges are measured to make a comparison with the data given by the manufacturer.

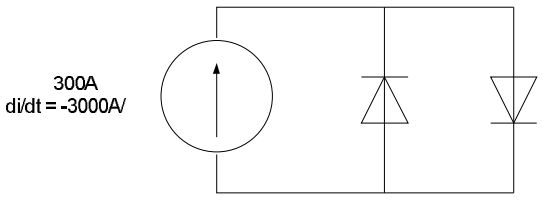
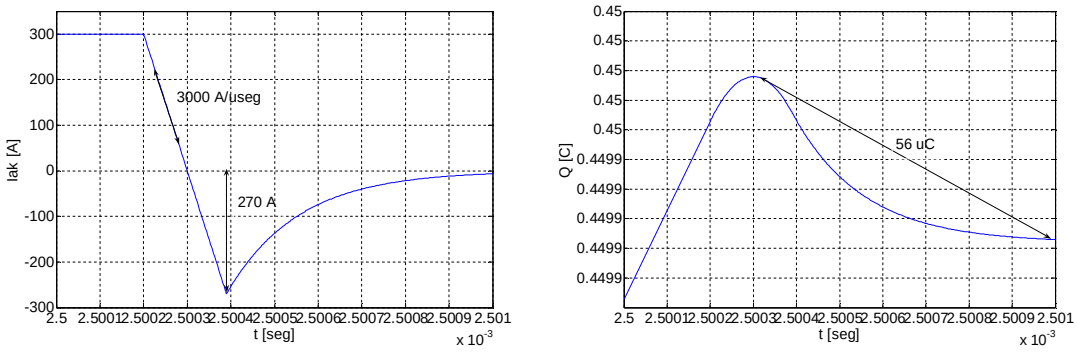


Figure 15-3: Simulation circuit (FD300R12KE3)

Figure 15-4 shows the reverse recovery current and the extracted charge during the switch off process. The extracted charge (56 μC) as well as the reverse recovery current (270 A) are equal to the data given by the datasheets at the simulated conditions (300 A, -3000 A/μs).



(a) (b)

Figure 15-4: Reverse recovery current (a) and the amount of extracted charges (b).

16 Appendix B: Influence of Self Commutated Semiconductors on Utility Grid Applications

16.1 Evolution of Static Converters for Utility Grid Applications

Electrical energy transmission was carried out for the first time in 1882 [AN-07] employing High Voltage Direct Current (Miesbach-Munich 2kV, 50km). In 1885 the transformer was invented which promoted Alternating Current Energy Transmission systems. These systems allowed energy transmission at higher voltages and in consequence with lower power losses. Three phase energy transmission systems were used for the first time in 1893. In addition, the first induction machines were developed making three phase transmission systems cheaper. This was the dominant transmission system during the 20th century.

The development of the direct current technology continued with the invention of the diode (1904), the vacuum tube (1910) and mercury arc valves (1928) to convert alternating current to direct current. In 1928, thanks to the emergence of power electronic converters (based on mercury arc valves), High Voltage Direct Current (HVDC) transmission systems started to show their capabilities.

The main advantages of High Voltage Direct Current (HVDC) transmission Systems with respect to High Voltage Alternating Current (HVAC) transmission systems can be summarized in the following points:

- In an alternating current transmission line (P_{AC}), the power transmission capacity is lower than in a direct current line (P_{DC}). The relation between both powers is given by equation (16-1).

$$\frac{P_{DC}}{P_{AC}} = \frac{\sqrt{2}}{\cos\varphi} \tag{16-1}$$

- For a given transmitted power, equal line power losses and equal operating voltage, the required cable section in direct current systems (S_{DC}) is lower than the required by alternating current systems (S_{AC}), (16-2).

$$\frac{S_{DC}}{S_{AC}} = \frac{\cos^2\varphi}{2} \tag{16-2}$$

- The energy transmission by direct current allows the use of the earth ground as a current return path. The resistance of the earth ground current return path depends exclusively on the earth electrode resistance at the two ends of the line, rather than on the line length.

- The required DC insulation level in DC transmission systems for the same power transmission is likely to be lower than the corresponding level in AC. Also the line will only need two conductors whereas three conductors (if not six to obtain the same reliability) are required for AC. In consequence both electrical and mechanical constraints are met with a smaller tower.

- In AC systems, the phase difference between the voltages at the two ends of the line should not exceed 30 degrees to ensure system stability. This problem does not exist in DC systems.

- In an AC system, both ends of the line must operate with the same frequency (synchronous system) while with a DC system there is no such need.

- DC Systems make the control of the power flow easier than AC systems.

- There are other factors as the lower short circuit fault levels, less corona and radio interferences, inexistence of skin effects that make HVDC systems very attractive for energy transmission application.

However, HVDC systems need power electronic converters at both ends of the DC line which increases the cost of the system. In addition, depending on the converter used, the reactive power injected by the converter and the current harmonic distortion are important. Finally, due to the absence of a natural zero current with D.C, circuit breaking is difficult [MO].

The most significant contribution to HVDC systems came when the Gotland Scheme in Sweden was commissioned in 1954 to be the World's first commercial HVDC transmission system. This was capable of transmitting 20MW of power at a voltage of 100 kV and consisted of a single 96 km cable with sea return. In 1970 the first semiconductor based HVDC (150 kV – 30 MW) was constructed. This converter used series connected thyristors.

Since the development of the first semiconductor based HVDC, most HVDCs use thyristor based line commutated converters. In these converters, the thyristors commutate once per line cycle. The thyristor is a unidirectional current valve and therefore, the thryristor based converter operates as Current Source Converters (CSC). This implies that the DC current in the converter flows only in one direction and the current amplitude depends on the voltage balance of both line end converters.

Figure 16-1 shows two electrical grids (G1, G2) connected by a HVDC (CSC) system. This HVDC system consists on a rectifier (close to G1), a transmission line (R) and an inverter (close to G2).

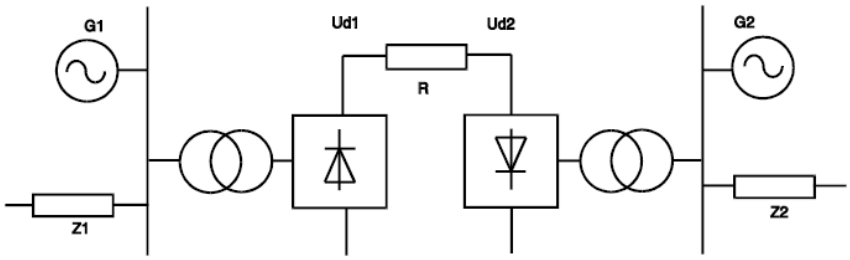


Figure 16-1: CSC based HVDC topology.

The power transferred from the first grid to the second grid depends on the voltage differences at both line ends (Ud1 and Ud2) and the ohmic resistance of the line (R). These voltages depend on the switching angle of both line end converters.

$$P \approx \frac{Ud1 \cdot (Ud1 - Ud2)}{R} \tag{16-3}$$

The value of Ud is controlled by means of the switching angle (α) of each converter:

$$Ud \approx k \cdot Uv \cdot (\cos \alpha) \tag{16-4}$$

As equation (16-3) shows, the transmitted power does not depend on the line frequency or the phase differences between the connected electrical grids. Therefore, it is possible to connect two electrical grids that operate at different line frequencies.

In the alternating side, thyristors control the power factor by means of the delay angle (α) between the voltage and the fundamental line current. In consequence, the reactive power consumption of the converter (Q) is given by the following expression:

$$Q \approx P \cdot \tan(\alpha) \tag{16-5}$$

As equation (16-5) shows, the amount of required reactive power (Q) can not be controlled independently of the transmitted active power (P). Therefore, an active power transmission is inevitably related to reactive power consumption.

The impedance of the alternating line is mainly inductive because of the presence of transformers, generators, transmission and distribution lines etc. In consequence, the reactive power flux has an important influence in the line voltage regulation which requires the compensation of the reactive power generated by the HVDC (CSC).

Assuming an electrical grid as shown by Figure 16-2 where the equivalent line impedance is inductive, an increment of the consumed reactive power causes a decrease on the load voltage (U_R).

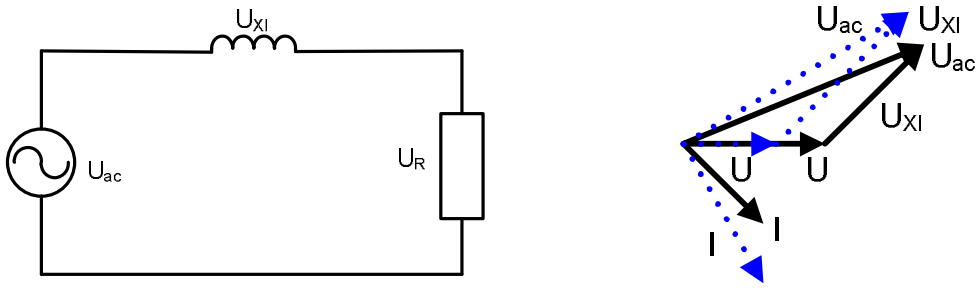


Figure 16-2: Influence of the reactive power on the voltage regulation

Most of the systems connected to the grid use capacitor banks to fix the power factor. These capacitors are connected and disconnected by means of mechanical switches to maintain the power factor close to the unity. A unity power factor improves the line voltage regulation and minimizes the required current to transmit a given active power. Therefore, the line losses (I^2R) are reduced and the system capacity (measured in terms of current handling capacity) is used more effectively.

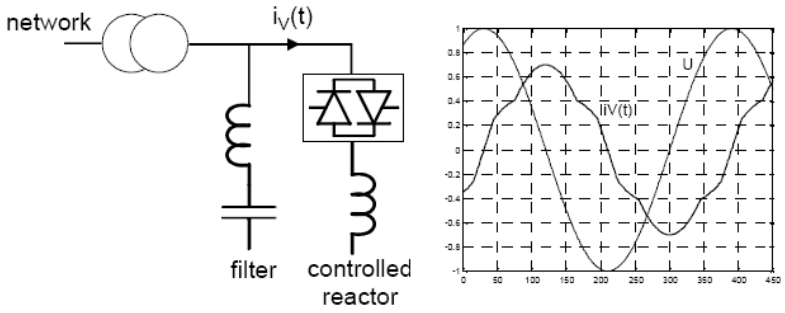


Figure 16-3: TCR based SVC and reactor current waveform

In general, the response time required by the converter is faster for reactive power control than for active power control. This is the reason why, since the emergence of the thyristor in the 70s, these devices were used in the first converters designed for reactive power (Q) control. These converters are known as SVC (Static Var Compensator) and use thyristor controlled reactances (TCR). These converters are formed by capacitor banks and thyristor controlled inductances connected in parallel. The capacitor bank can generate the maximum reactive power while the controlled inductance consumes the excess of generated reactive power. This is done controlling the fundamental current component across the inductances, Figure 16-3. In general, air core or iron core inductances are bulky and generate important power losses.

With the emergence of self commutated switches (IGBTs, IGCTs, GTOs, etc), the development of Voltage Source Converters (VSC) was promoted. With these type of converters the control of the amplitude and phase of an output voltage is possible. With these two degrees of freedom (amplitude and phase) almost independent control of the amount of active and reactive power exchanged with the electrical grid, section 16.2. In addition, these converters allow high frequency PWM modulations to improve the output voltage waveform with respect to thyristor based converters (line commutated converters). Therefore, a VSC can operate transmitting energy from one point to another and at the same time regulating the voltage amplitude at the connection point. This makes possible the construction of smaller installations than thyristor based installations. Additionally, the lower harmonic distortion of the output waveforms makes the reduction of the filter size possible and in consequence the volume of the installation.

However, the higher switching frequency and the higher conduction losses of self commutated devices lead to higher power losses. This has a negative influence on the overall efficiency of the converter.

To sum up advantages of **Voltage Source Converters** give cause for the development of power electronic converters oriented to energy transmission (VSC-HVDC) and power quality improvement (STATCOMs, UPFC and active filters). In following sections, these applications will be briefly described.

16.2 Power Flow Control with Voltage Source Converters

As described in section 16.1 a voltage source converter is able to create an output voltage (U_{conv}) with controlled amplitude and phase. In general, the converter is connected to an alternating grid (U_{ac}) by means of an inductor, Figure 16-4.

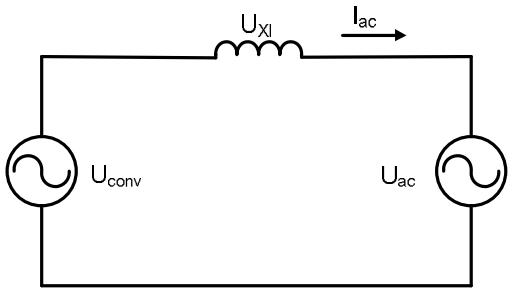


Figure 16-4: Simplified diagram of a converter connected to the utility grid.

When the phase and amplitude of the converter output voltage are equal (U_{conv}) to the phase and amplitude of the grid voltage (U_{ac}) there is not any power flux between the converter and the grid, Figure 16-5 (a) and Figure 16-6 (a).

If both voltages are maintained with the same phase ($\delta = 0$) and the amplitude of the converter output voltage (U_{conv}) is modified, the converter exchanges reactive power (Q) with the electrical grid, Figure 16-5.

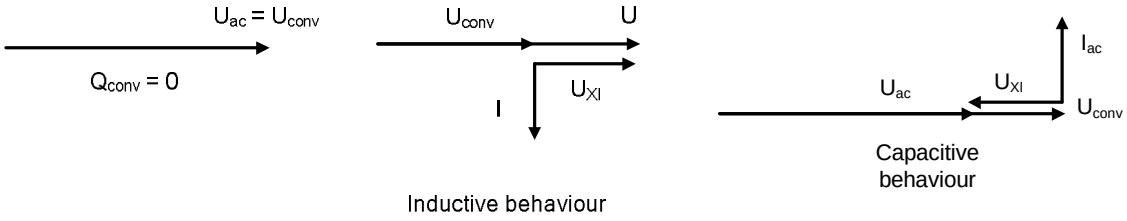
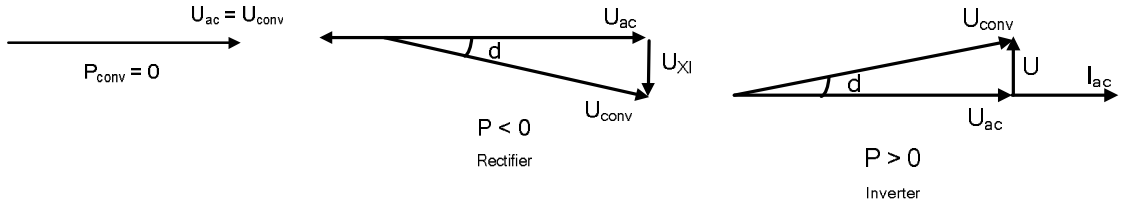


Figure 16-5: Reactive power control (Q)

If a phase (δ) difference between both voltages is forced, the converter exchanges active power (P) with the electrical grid, Figure 16-6.



(a) (b) (c)

Figure 16-6: Active power control (P)

In consequence, the exchanged active power is controlled by modifying the phase difference of the converter output voltage and the grid voltage. Similarly, the exchanged reactive power is controlled mainly by means of the amplitude differences of voltages, (16-6) and (16-7).

$$P = \frac{U_{ac} \cdot U_{conv}}{Xl} \cdot \sin(\delta) \qquad (16\text{-}6)$$

$$Q = \frac{U_{ac} \cdot (U_{conv} \cdot \cos(\delta) - U_{ac})}{Xl} \qquad (16\text{-}7)$$

As the voltage source converters allow an independent control of the exchanged active power (P) and reactive power (Q), these converters are suitable (among other applications) for energy transmission applications and for reactive power compensation applications.

17 Appendix C: Overview of Silicon Carbide based Power Devices

Silicon power devices have reached the limits imposed by nature and not by technology. This means that in order to increase the power ratings, operating temperature and efficiency of actual power semiconductor devices, new materials should be considered. The use of Silicon Carbide (SiC) is a promising way to extend the actual limits imposed by Silicon devices.

17.1 Description

Silicon Carbide (SiC) is a compound of Silicon and Carbon that traditionally has been used as an abrasive. Because of its properties, nowadays, it is being increasingly considered in semiconductor electronics.

Silicon Carbide is found in certain types of meteorites, it means that most of the Silicon Carbide available in the world is synthetic. Usually, SiC is maden by means of furnace techniques. Silicon Carbide exists not as a single crystal type but as a whole family of crystals known as polytypes. Polytypes differ not in the relative numbers of Si and C atoms but in the arrangement of these atoms in layers. The polytypes are named according to the periodicity of these layers. One of the commonest polytypes is called 6H, this means a hexagonal type lattice with an arrangement of 6 different Si+C layers before the pattern repeats itself. More than 200 different polytypes of SiC can be found, some of them with patterns that do not repeat for hundreds of layers. The exact physical properties of SiC depend on the adopted crystal structure. Some of the most common structures used are 6H, 4H and 3C.

SiC is a “Wide Bandgap” semiconductor type. Mainly, this implies that these materials are less sensitive to increased temperatures and are able to withstand higher electric fields for a given layer thickness. There is not any reason why a SiC device should not operate at 500ºC or higher temperatures. This is a figure of merit unreacheable by silicon (Si) devices. The thermal conductivity is higher than the thermal conductivity of copper and therefore, any heat produced by a device is quickly dissipated.

The inertness of SiC to chemical reaction implies that SiC devices have the potential to operate even in the most caustic of enviroments and extreme pressure conditions. Because of SiC is extremely radiation hard it can be used close to reactors or for space electronic hardware. In addition high electric field strength and high saturation drift velocity allows the construction of smaller and more efficient power electronic devices.

However, in spite of the advantages of SiC technology with respect to the Si technology some difficulties have contained the development of most wide bandgap materials. The main difficulties can be summarized as follows:

- The availability of a suitable substrate or bulk material.
- The growth of high quality single crystal films over large enough areas.
- Well controlled doping, both n and p type.
- An appropriate and available dielectric.
- A developed technology for contacts and etching.

Although for SiC most of these problems have been solved, the technology is not yet at commercial production standard. In consequence the best gauge of the maturity of material development is to look at the range and performance of the devices that have been made using it.

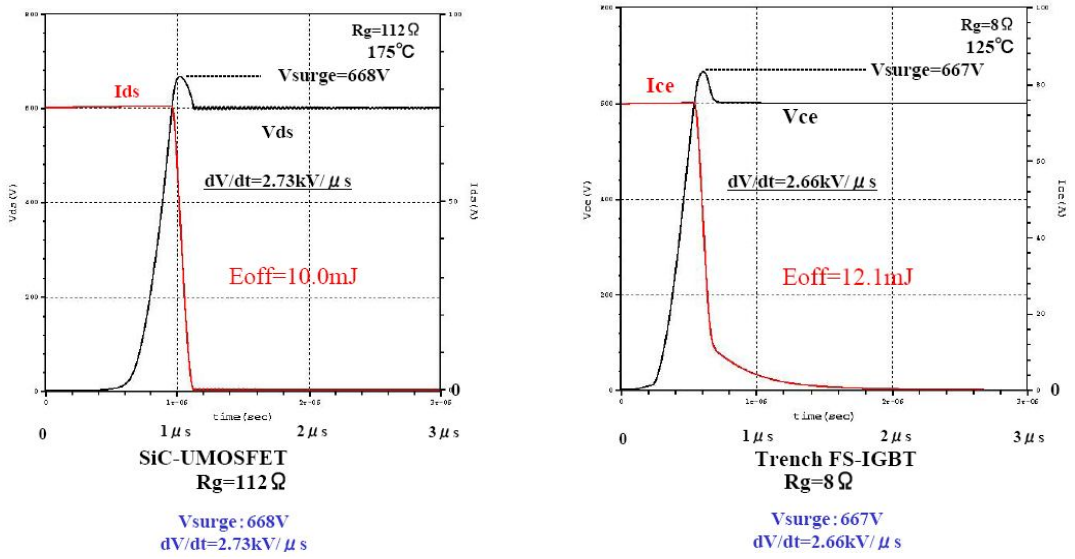
The power handling capabilities and high operation temperature make SiC an ideal material for the production of rectifiers. Both Schottky (up to 1 kV) and pn diode rectifiers (up to 4.5 kV) have been produced. Operating temperatures in excess of 350 ºC have also been shown. Blue LEDs, high temperature thyristors for High Power switching devices have been also presented.

Self Switching devices constitute perhaps the largest current area of device activity. The largest effort are concentrated on unipolar devices. These include Field Effect Transistors as JFET, MOSFET and MESFET. Problems with the interface of SiC with silicon dioxide have hampered the development of SiC based power MOSFET and IGBTs.

In spite of potential advantages of Silicon Carbide devices with respect to Silicon devices, there are several drawbacks that make difficult the development of SiC power devices at ratings reached by Si devices. Mainly, the cost-performance ratio and impressive technological improvements like thin wafer processing or charge compensated technologies strengthened the position of silicon as leading base material for power semiconductor components today and in the future. In addition, the reduction of the material cost per area and the defect density as well must be achieved if higher power ratings need to be addressed [FR-07].

17.2 Current SiC power devices

Unipolar Silicon Carbide power devices seem to be able to substitute bipolar Silicon devices in the voltage classes from 600V to 3300V. Because of the absence of minority charge carriers which would need time for generation and recombination, unipolar devices can switch from on state to off state (and viceversa) with much less dynamic energy loss than bipolar devices do [PE], Figure 17-1. This fact allows an increment of the operating frequency with respect to actual bipolar IGBT devices.



(a) (b)

Figure 17-1: Comparison of switch-off waveforms between a SiC MOSFET (a) and Silicon based Trench FS-IGBT (b).

In addition, SiC devices can operate at higher junction temperatures assuming that the packaging is enabled to stand it. Therefore, the heat sink temperature can be extended and additional cooling circuits can be skipped. Therefore, new concepts for packaging technology are necessary. The big challenge for the packaging technology is to connect lots of SiC chips having very low on resistance, high current ratings under extended junction temperatures conditions and heavy fluctuations in temperature in a reliable way [PE].

In following paragraphs main characteristics of SiC Shottcky Diodes (17.2.1), SiC JFETs (17.2.2) and SiC MOSFETs (17.2.3) are briefly described.

17.2.1 SiC Shottcky Diodes

Power diodes are a key component in modern power applications. Regarding SiC, the ability to fabricate unipolar Schottky barrier diodes with blocking voltages up to 2 kV offers new degrees of freedom in the design of power circuits. Due to virtually zero reverse recovery, Figure 17-2, dynamic losses of typical circuits can be reduced drastically [FR-07], in addition, the extremely fast tun on performance is a feature which can be favourably used in many applications.

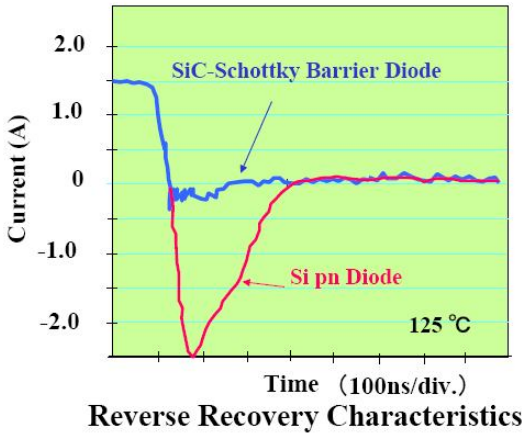


Figure 17-2: Reverse recovery behaviour of a SiC Shottky diode and a Si pn diode.

In spite of Schottky diodes are nowadays commercially available, their maximum current capacity does not exceed few tens of amperes [IN]. It means that for High Power applications (high current demanding applications) this technology is still unmature.

17.2.2 SiC JFET

Among all available SiC power switching prototypes, the SiC JFET is the most reliable one and has the lowest on resistance. SiC JFET devices are used in those industrial applications where a very high switching frequency leads to energy efficient and compact system solutions. Mainly above 1 kV the SiC JFET can outperform the Si MOSFET due to its lower specific on resistance. Similarly, the SiC JFET can outperform the Si IGBT due to its more efficient switching behaviour. A high current rating related to a small chip size leads to an excellent dynamic performance since both the input capacitance and the Miller capacitance are very small. However, the device is normally “on” and implies an alternative gate control and safety precautions. This fact has hampered the use of JFET devices in power applications.

17.2.3 SiC MOSFET

The SiC MOSFET has the same application field as the JFET. The acceptance is better since the device is normally “off” and matches standard gate driver circuitry. However up to now the SiC MOSFET suffers from low inversion channel mobility due to carbon related interface states. In addition, the long time stability of the MOS system might cause concerns due to the high field stress in the oxide. However, new reliability tests show encouraging results regarding the so called intrinsic stability of the gate oxide. In spite of it all, it seems that JFET technologies may be released first on the market place due to the difficulties to solve the problems related to the gate oxide.

Another challenge in commercialization of SiC MOSFET resides in the control of the threshold voltage. The room termperature threshold voltage is approximately 3.5V [AG-06] and decreases to 2.2V at 150ºC. However, for power switches, the drain current should be less than 1 μA in off state. The low current threshold voltage of this device is very close to zero. Therefore, the noise margin of this device is extremely small. This is a disadvantage for power switching applications.

As shown by Figure 17-1 thanks to the absence of any tail current, power SiC MOSFETs are intended to replace bipolar Si IGBT devices in the voltage range up to 1700 V. In addition, in the voltage range up to 1700 volts, the on voltage drop is lower than SiC IGBT devices, Figure 17-3. It means that up to this voltage level SiC MOSFET should be the most efficient choice. High voltage MOSFET devices will have too high on state voltage drop so bipolar devices as SiC IGBTs should be better suited to operate at this voltage ranges, Figure 17-3.

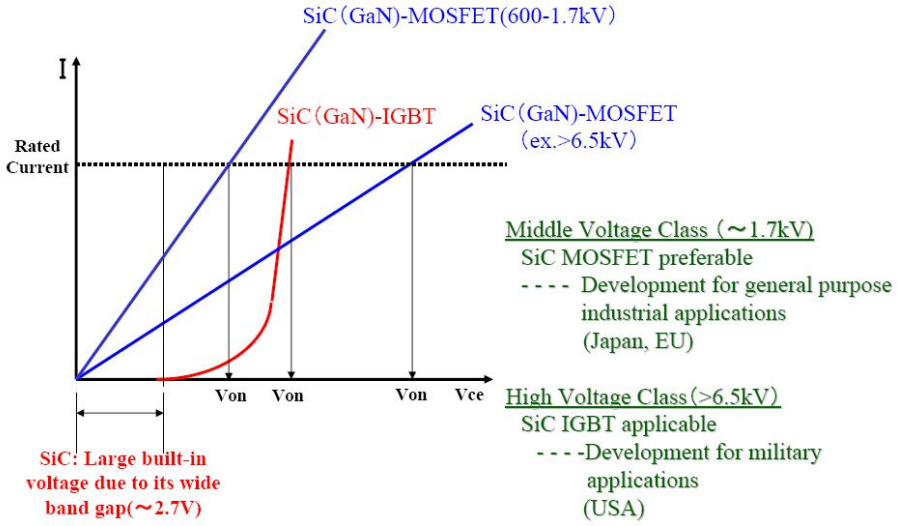


Figure 17-3: Forward characteristic of SiC MOSFET and SiC IGBT devices.

In spite of the ability of SiC MOSFETs to perform the switching process quickly, laboratory measurements show that to fast dI_C/dt-s leads to excessive oscillations, Figure 17-4. In order to avoid this behaviour higher gate resistances are required with lead to higher switching losses.

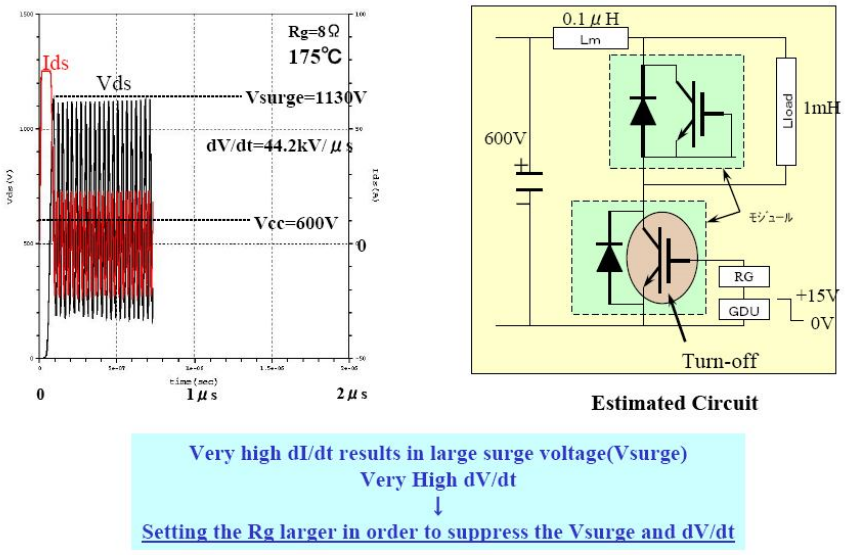


Figure 17-4: Effect of too fast switching behaviour

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19 Corrigenda

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