Quantum simulation investigation of work-function variation in nanowire tunnel FETs

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Abstract

The variability induced by the work-function variation (WFV) in p-type ultra-scaled nanowire Tunnel FET (TFET) has been studied by using the Non-Equilibrium Green's Function module implemented in University of Glasgow quantum transport simulator called NESS. To provide a thorough insight into the influence of WFV, we have simulated 250 atomistically different nanowire TFETs and the obtained results are compated to nanowire MOSFETs. Our statistical simulations reveal that the threshold voltage (V_{th}) variations of MOSFETs and TFETs are comparable, whereas the On-current (I_{on}) and Off-current (I_{off}) variations of TFETs are smaller and higher, respectively in comparison to the MOSFET. Based on the results of the simulations, we have provided a physical insight into the variations of the I_{on} and I_{off} currents. Then, we compared the nanowire and Fin structure in TFETs with different oxide thickness in terms of the WFV-induced variability. The results show that WFV has a strongest impact on the I_{off}, and moderate effect on the I_{on} and V_{th} in nanowire TFET with smaller oxide thickness. Lastly, it is found that compared with the random discrete dopants, WFV is a relatively weaker variability source in ultra-scaled nanowire TFETs, especially from the point of view of I_{on} variation.

Keywords: nanowire, quantum simulation, tunnel FETs (TFETs), variability, work-function variation (WFV)

1. Introduction

Tunnel FETs (TFETs) have been widely investigated over the last decade due to their potential for overcoming the 60mV/decade limit of the subthreshold swing (SS) at room temperature which limits the MOSFETs operation [1]. Therefore, TFETs are being considered as promising candidates for low power applications in future technology nodes. However, the low on-current (I_{on}) is one of the main bottlenecks in TFETs. Many methods have been proposed to improve the I_{on} of TFETs, such as using III-V material with small effective mass, adopting heterostructure [2]-[5] in source/channel junction, and using dual-material gate [6].

Recently, the group from Lund university fabricated the III-V heterostructure gate-all-around nanowire TFETs and the experiment results are encouraging with sub-thermal operation, reaching down to 48 mV/dec, combined with high current of 10.6 μA/μm at source-to-drain bias of 0.3V [4]. In addition to the current booster such as heterostructures, the use of the high-*k*/metal-gate and the scaled nanowire with 20 nm diameter in [4] also attribute to the high current since they together provide the excellent electrostatic control ove the channel [7]. It is, therefore, important to understand how the metal gate work-function variations (WFV) affects the scaled nanowire TFET performance and its performance-induced variability [8].

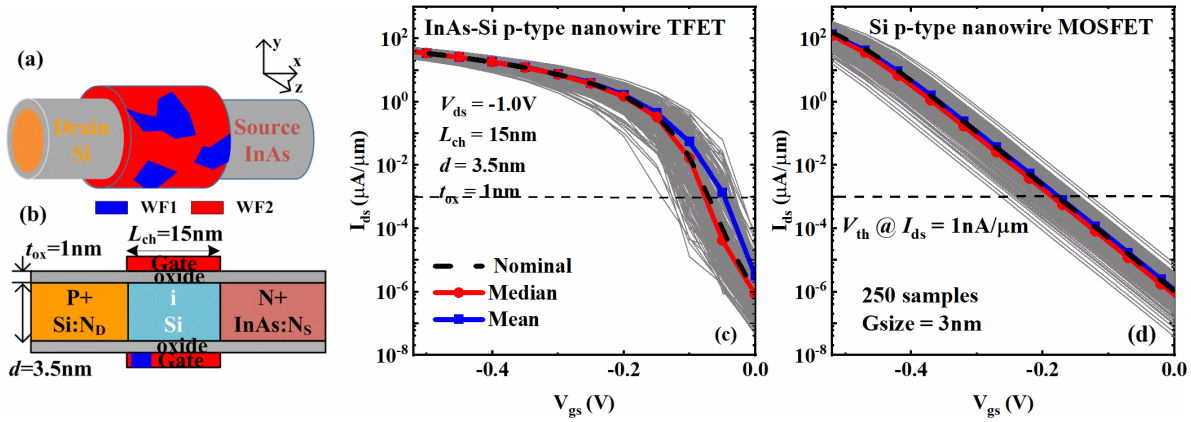

Figure 1. (a) 3D view of the nanowire InAs-Si p-type TFET with WFV. (b) Schematic cross section along the channel of the TFET. The I_{ds}-V_{gs} curves of 250 samples of (c) TFET and (d) MOSFET with the average and median data. The parameters adopted are d = 3.5 nm, t_{ox} = 1 nm, L_{ch} = 15 nm, N_S = 5×10^{19} cm^{-3}, and N_D = 2×10^{20} cm^{-3}. The TiN metal is used as the metal gate with two possible grain granularities. The Si p-type MOSFET has the identical geometry except that N_S = N_D = 10^{20} cm^{-3} with p-type doping in source/drain. V_{th} is defined as the gate voltage yielding the current of 1 nA/μm. The current is normalized by the nanowire cross section perimeter (πd). The I_{off}@V_{gs} = 0 is set to 1 pA/μm by adjusting work function values in nominal MOSFET and TFET.

Previous works related to the WFV in bulk-like planar TFETs have been conducted by performing semi-classical simulations [9]-[13]. However, as process developments have shown, diameters of III-V nanowires can be reduced down to a few nanometers [14], such as it reaches up to 7 nm in III-V TFETs by using digital etching technique [15]. These truly nano-scaled or ultra-scaled devices are dominated by quantum mechanical effects and the device physics should therefore be captured by a full quantum mechanical description, especially for TFETs since the band-to-band tunneling is a pure quantum phenomenon [16]. In ultra-scaled TFETs, the current obtained from quantum mechanical approach was found to be visibly lower than the one from the semi-classical approach, as reported in Ref. [17]. Thus, the inclusion of quantum effects is mandatory in order to improve the accuracy of simulation predictions, as was done here for the study of WFV in ultra-scaled nanowire TFETs. Although Avci *et al.* [18] has compared the WFV in MOSFET and TFET using quantum simulations, the result seems to be obtained by changing the value of the gate work function rather than adopting the granularity nature of the metal gate, and the number of sample device seems to be limited. To the best of our knowledge, a statistical study of the WFV in ultra-scaled nanowire TFETs has not been reported yet.

In this paper, using quantum transport simulation methodology we investigate the impact of the WFV on the p-type gate-all-around extremely narrow nanowire TFETs. This work sheds light on the physics of performance variation and fundamental reliability limit in achievable truly nanometric size TFETs, which is beneficial for the application and design of low-power circuit with TFETs in the future technology node.

In order to present our main findings, this paper is organized as follows. In Section 2, the simulation methodology is described and the device and material parameters are provided. In Section 3, a comparative study of the influence of the WFV between nanowire TFETs and nanowire MOSFETs, nanowire TFETs and Fin-TFETs are presented, followed by the comparison between the impact of WFV and random discrete dopants (RDD) in nanowire TFETs. Finally, in Section 4 the conclusions are drown.

2. Simulation Methodology and Device parameters

Simulations are carried out by employing the quantum transport solver implemented in NESS from the University of Glasgow [19], [20]. Figure 1(a) describes the 3D structure of a p-type InAs-Si heterostructure TFET default considered in this work. Note that the default type of the studied TFET is a kind of point-TFETs, being capable of delivering significant performance after optimization [4], [21]. They have the advantage of using effortless fabrication techniques compared to line-TFETs [21], especially in the case of heterostructures with small body thickness. The cross-section along the channel is shown in figure 1(b). The nanowire is 3.5 nm in diameter (d) and the channel length (L_{ch}) is 15 nm. The high-k oxide thickness (t_{ox}) is 1nm with relative dielectric constant $\varepsilon = 9.0$. The donor-type source and acceptor-type drain regions are doped with $N_{\mathrm{S}} = 5 \times 10^{19}$ cm^{-3} and $N_{\mathrm{D}} = 2 \times 10^{20}$ cm^{-3}, respectively. The channel is intrinsic Si material (i-Si) and the doping profiles are assumed to be abrupt between the contacts and the channel. The device we studied has 3.5 nm diameter and it is beyond the status of the art of nanowire growth, i.e. diameter of 7 nm [15]. The fabrication steps of the device which we are simulating can refer to the flow chart of processing reported by Lund group where the vapor–liquid–solid growth method combined with digital etching technique is utilized [15].

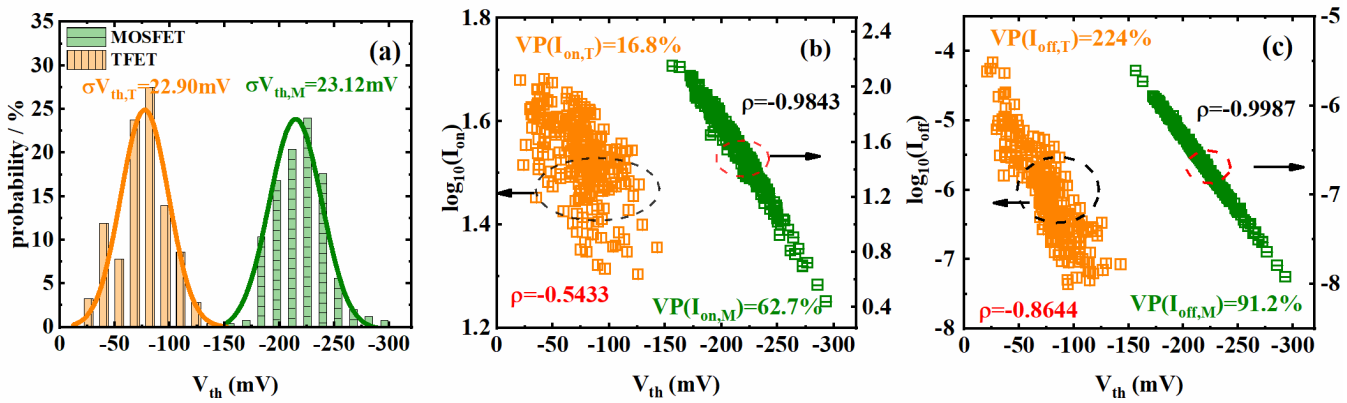

Figure 2. The comparisons of (a) V_{th} distributions, (b) I_{on} vs. V_{th}, and (c) I_{off} vs. V_{th} between InAs-Si TFETs and Si MOSFETs. All data are extracted from figure 1(c) and (d). The normalized deviation VP=σ/μ is the ratio of the standard deviation value by the mean value (μ) of the corresponding FoM.

In order to study the WFV effects, TiN metal gate is employed. The TiN has two possible grain orientations (<200> and <111>) with a work function difference of 0.2 eV [13]. The occurrence probabilities of each orientation are 60% and 40%, respectively. The grains are generated by using a realistic Voronoi pattern [10], as implemented in NESS [22]. The WFV-induced variability is introduced by the random grain orientations found in the TiN gate-all-around contact, as shown in figure 1(a). Unless otherwise specified, the default value of the average grain size (G_{size}) is set to 3 nm and the source-to-drain bias to $V_{\mathrm{ds}} = -1.0$ V.

Non-Equilibrium Green's Function (NEGF) formalism allows the quantum treatment of charge transport to capture quantum phenomenon in nano-devices. In order to accurately compute the band-to-band tunneling (BTBT) current in the ultra-scaled nanowire, the two-band Flietner model of the imaginary dispersion is used in combination with the couple mode-space NEGF approach, as implemented in NESS [23], [24]. In the latter, the electron and hole band structures are described by the one-band effective mass approximation (EMA). After the self-consistency with Poisson equation is reached, both bands are then coupled through the two-band Flietner model to compute the BTBT current. It should be noted that the electron-phonon interactions are neglected since the tunneling in the studied devices are mainly direct, as reported in Refs. [25] and [26].

It has been shown that NESS can reproduce the BTBT $I_{\mathrm{ds}} - V_{\mathrm{gs}}$ characteristics obtained by the atomistic tool OMEN [27], as long as the proper effective masses are used [25]. Thus, the values of the effective mass in [25] are adopted for InAs and Si materials. Note that the accuracy of OMEN has been verified by the agreement with experimental results [28], and consequently the findings from NESS should be reliable.

3. Results and Discussion

3.1 The influences of WFV on nanowire TFETs

As benchmark, the impacts of WFV in p-type Si nanowire MOSFETs, with identical nominal geometrical features, are also simulated to better observe the influence of WFV on nanowire TFETs performance. The acceptor-type source/drain and donor-type channel regions are doped with $10^{20}\mathrm{cm}^{-3}$ and $10^{18}\mathrm{cm}^{-3}$, respectively in MOSFETs. Notice that the channel is highly doped as suggested by the ITRS [29].

For fair comparison, we have adjusted the work function of the nominal TFET and MOSFET to make them deliver the same off-current (I_{off}) of 1 pA/μm at $V_{\mathrm{gs}} = 0$ V, as done in Refs. [10] and [30], which meets the ultra-low power technology requirement [31], as shown in figure 1(c) and (d). The average SS = 23.3 mV/decade of the nominal TFET is computed over three orders of magnitude (from 1 pA/μm to 1 nA/μm), being approximately 40 mV/decade smaller than the one reported for MOSFET. Regarding the I_{ON} (defined as the current at $V_{\mathrm{gs}} = -0.5$ V)), it is 33.6 μA/μm and 97.2 μA/μm in the case of the TFET and MOSFET, respectively. However, for $0\ \mathrm{V} < |V_{\mathrm{gs}}| < 0.4\ \mathrm{V}$, the InAs-Si nanowire TFET outperforms its MOSFET counterpart, providing higher current, high I_{ON}/I_{OFF} ratio, and sub-thermal SS.

In order to carry out a reliable statistical analysis of variability introduced by the WFV, ensembles of 250 TFETs and MOSFETs have been simulated. Figure 1(c) and (d) shows the $I_{\mathrm{ds}} - V_{\mathrm{gs}}$ characteristics of each of the 250 TFETs and MOSFETs subject to the WFV variability, respectively. The mean and median $I_{\mathrm{ds}} - V_{\mathrm{gs}}$ characteristics are also shown. It can be seen that the WFV induces strong variations of the SS in case of TFETs, whereas in MOSFETs, the SS has a negligible dependence on the WFV [32]. In contrast to the constant SS in conventional MOSFETs, the SS in TFETs has a dependence on V_{gs} in the subthreshold region due to the complex dependency of the tunnel current on the transmission probability as well as the number of available states [1]. Actually, the effect of WFV can be regarded as the change of gate voltage along the channel. Thus, the WFV of

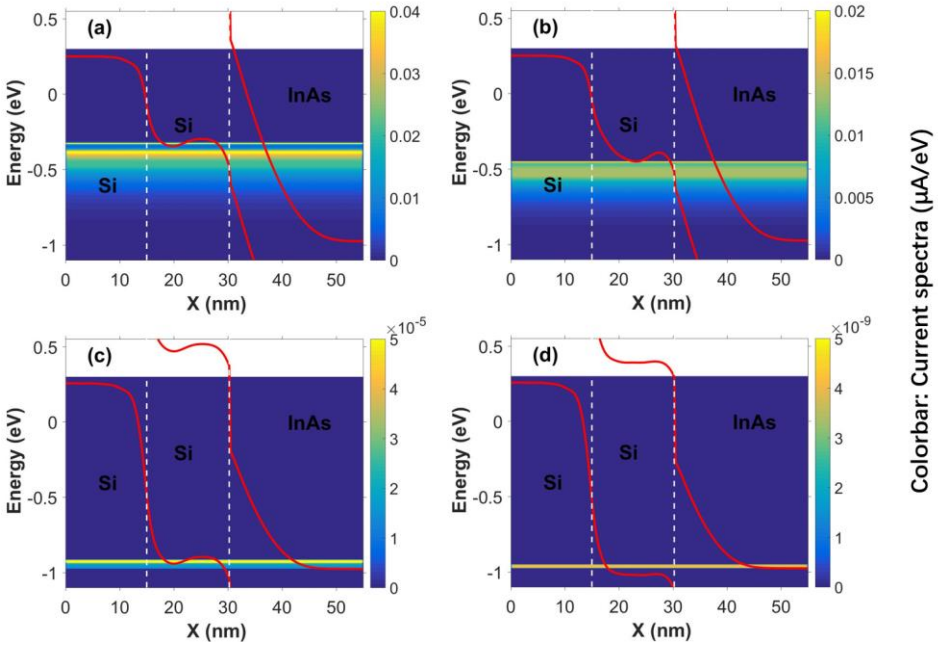

Figure 3. Current spectra of InAs-Si nanowire TFETs with maximum and minimum $I_{on(off)}$ under the WFV. (a) and (b) correspond to the On-state bias condition, and (c) and (d) are for the OFF-state. The red lines are the corresponding conduction and the valence band edges in TFETs. The unit of the current spectra is μA/eV.

gate will significantly and barely influences the SS feature in TFETs and MOSFETs, respectively.

In both cases, the WFV introduced a shift in threshold voltage (V_{th}). The V_{th} is defined as the gate voltage where $I_{\mathrm{ds}} = 1\ \mathrm{nA/\mu m}$ [12], [33]. Figure 2(a) shows the V_{th} probability distribution of TFETs and MOSFETs with comparable standard deviations $\sigma(V_{\mathrm{th}})$, of 22.90 mV and 23.12 mV, respectively. However, it can be found that the median $|V_{\mathrm{th}}|$ value in the TFETs is at lower voltage in comparison to the MOSFETs one. The lower $|V_{\mathrm{th}}|$ value in TFETs comes from the sub-thermal behavior of SS, which avails to the supply voltage scalability. The scattered plots showing the correlation of I_{on} and I_{off} with the V_{th} are presented in figure 2(b) and (c). It should be noted that the scales on the double-y axes are not the same. VP, the coefficient of variation to performance, is defined as σ/μ and is a normalized measure of dispersion when considering the performance difference under different conditions, as adopted in Refs. [34] and [35]. μ is the mean value of the corresponding figures of merits (FoM). From the definition of VP, it is obvious that the smaller the VP, the weaker the relative variation is. The correlation coefficients (ρ) are extracted by means of Spearman's correlation method. As expected, strong correlation between the $I_{on(off)}$ and V_{th} in MOSFETs is observed. For TFETs, the correlation is lower. The latter might result from the complex dependence of the SS on the tunneling barrier [36].

In order to gain a physical insight and understanding about the influence of the WFV, we present in figure 3(a)-(d) the current spectra (unit μA/eV) of the highest and lowest $I_{on(off)}$ cases from our 250 TFETs simulations with $N_S = 10^{19}\ \mathrm{cm}^{-3}$, which are not shown here. We believe that the doping should not influence the analyses below. Figure 3 also shows the highest valence and lowest conduction sub-bands (red lines). For each sub-figure in Figure 3, from left to right, the components of the device are drain (0 < X < 15 nm), channel (15 nm < X < 30 nm), and source (X > 30 nm) regions. Because of the quantum confinement effect, the band gaps of both Si and InAs are larger than their bulk values, but the influence on InAs with small effective mass is much stronger, as presented in Figure 3. Furthermore, by comparing Figure 3(a)/(b) to 3(c)/(d), it can also be observed that the p-type TFET is switched from off-state to on-state with the decrease of gate voltage, due to the widened tunneling window (the overlap between the valence band in channel and the conduction band in source), and the increased electric field and thus the tunneling probability.

Notice that the impact of the WFV is within the channel region. By comparing the on-state current spectra in figure 3(a) and (b), one can infer that the region near source/channel junction plays a major role in the BTBT mechanism, leading the WFV to 'locally' affecting TFETs performance. From Figure 3(a) and (b), one can also find how the WFV impacts the effective tunneling windows, the sub-band profiles, and hence, modifies the tunneling paths. However, since the BTBT mainly occurs between the channel and source regions, the I_{on} is weakly affected by the WFV. The opposite happens in case of MOSFETs, where the WFV directly modify the electrostatic potential barrier within the channel, leading to the results shown in figure

2(b). In Figure 2(b), VP(I_{on}) is 16.8% and 62.7%, respectively, in TFETs and MOSFETs. It should be noted that (in this study) MOSFETs work within the sub-threshold region, as shown in Figure 1(d), and the variation in I_{on} will decrease when the on-state of MOSFET is within inversion region. However, from Figure 2(c), one can see that the VP(I_{off}) in TFETs reaches up to 224%. I_{off} in TFETs has the strongest variation. This can be explained by inspecting Figure 3(c) and (d) where the current spectra of off-state are shown. In Figure 3(c), one can see that BTBT occurs from the source to the beginning of the gated channel, where the tunneling distance is around 10 nm. Whereas, in Figure 3(d), the BTBT occurs from the source to the end of the gated channel, where the tunneling distance is more than 20 nm. Thus, in case of TFETs, the WFV-induced variability in I_{off} is much stronger on account of the exponential dependence of current on the tunneling distance [1].

3.2 How the scaled nanowire structure influences the WFV-induced variability in TFETs?

Although the scaled nanowire structure provides the satisfactory performance in TFETs [4], the variability characteristics of nanowire TFETs when compared with other scaled structures-based TFETs is still unknown and should be investigated to reveal the reliability of TFETs based on nanowire structures. In this subsection, the performance WFV-induced variability in nanowire and Fin-TFETs are compared for different values of t_{ox}.

For Fin-TFETs, the fin width and fin height are both of 3.5 nm with the oxide thickness $t_{ox} = 1$ nm, as plotted in Figure 4(a), and the other device parameters are identical to those of in nanowire TFETs from Figure 1(a). Note that $N_S = 10^{19}$ cm^{-3} in all devices studied in this subsection.

Figure 4(b) shows the nominal $I_{ds} - V_{gs}$ characteristics under three legend set. The I_{on}'s are 0.009, 0.19, and 0.26 μA/μm for nanowire with t_{ox} of 2 nm and 1 nm, and Fin architecture with t_{ox} of 1 nm, respectively, by shifting the curves to achieve the same I_{off} of 1 pA/μm at $V_{gs} = 0$ V. For the comparison between nanowires with different t_{ox}, quantum confinement reduces as t_{ox} increases. However, at the same time, the ability of gate controlling over the channel also reduces. These two aspects lead to opposite effects on the current, i.e. the former enhances the current, and the latter reduces the current. The higher I_{on} for the smaller t_{ox} indicates that the effect from the former is weaker than that from the latter when we change oxide thickness. However, the lower current from the nanowire compared to that from the Fin architecture with same t_{ox} shows that the effect from quantum confinement rather than gate control dominates. Fortunately, the use of nanowire in TFETs can relax the body thickness to improve the performance further [37] due to its superior SS characteristic.

Figure 4(c) shows the dependence of the V_{th} and I_{on} variations induced by the WFV on the device parameters.

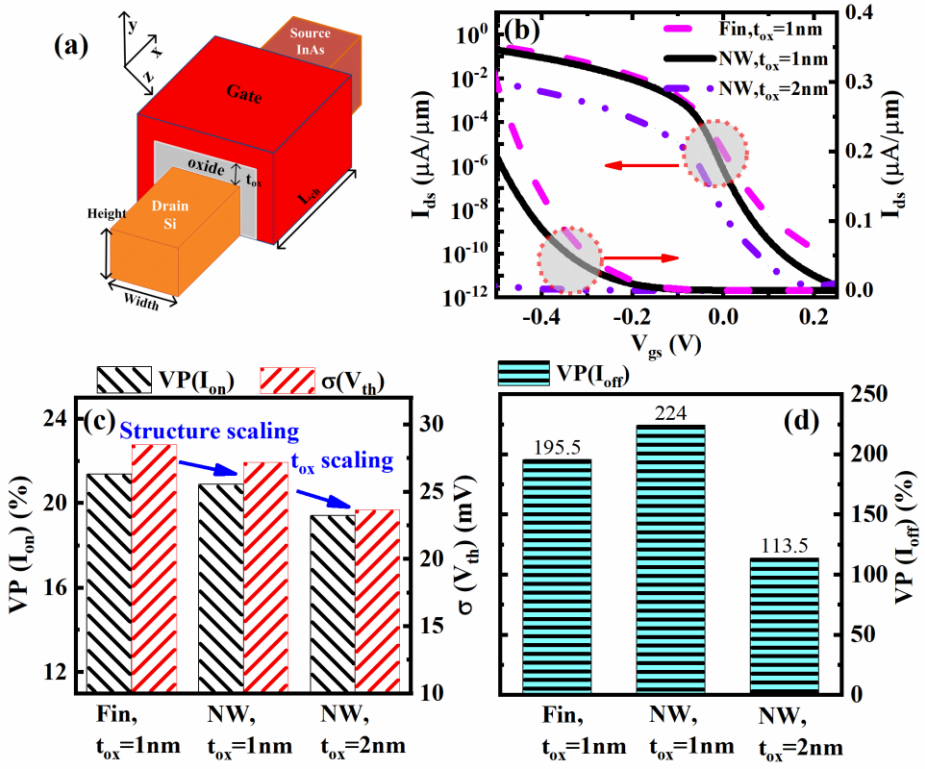

Figure 4. (a) The nominal structure of Fin-TFET used here. (b) Comparison of the nominal I_{ds}-V_{gs} characteristics between Fin-TFET and nanowire (NW) TFET with t_{ox} =1nm and 2nm under the same set. The dependence of the (c) I_{on}, V_{th} and (d) I_{off} variations under the WFV on the structure parameters of TFET. $N_S = 10^{19}$cm^{-3}.

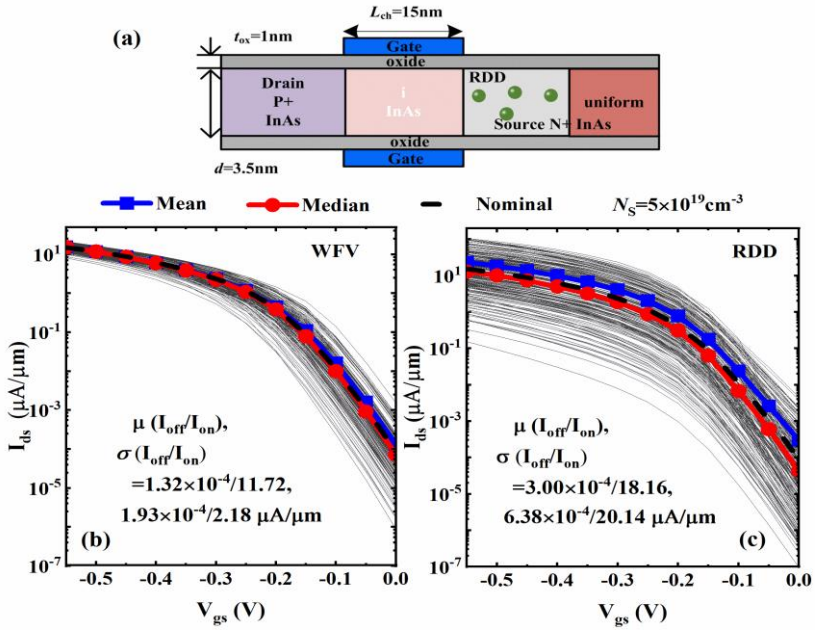

Figure 5. (a) The schematic cross section of the InAs nanowire TFET with RDD influence. The individual influence of (b) WFV and (c) RDD on the I_{ds}-V_{gs} characteristics of InAs nanowire TFET. The RDD region is 10 nm long and N_D=N_S=5×10^{19} cm^{-3}.

Whereas the variation of I_{off} is presented in Figure 4(d). From Figure 4(c), it can be seen that adopting the gate-all-around nanowire instead of the fin structure can reduce the effect of the WFV on both of V_{th} and I_{on}. This is because the nanowire has a larger gate area than the Fin-TFET in our case. Note that increasing the gate control and increasing gate area play an opposing role in variability [9], and thus the reduced WFV-induced variation in nanowire indicates that the influence by the latter is stronger when the devices are in on-state. However, from figure 4(d), the severer variation of I_{off} is observed when the nanowire instead of the Fin structure is used, implying that the influence from the former, i.e. enhanced gate control, is dominant when TFETs are in off-state. Furthermore, as shown in figure 4(c) and 4(d), the oxide thickness scaling up from 1 nm to 2 nm in the nanowire can alleviate the whole variations since it attenuates the gate control and increase the gate area simultaneously. Note that VP(I_{off}) of each case in figure 4(d) is larger than 1, which is another confirmation of the extreme sensitivity of I_{off} to the WFV.

3.3 What is the role of WFV among the variability sources in nanowire TFETs?

This subsection aims to find out what is the overall effect of WFV among the variability sources in nanowire TFETs. On the one hand, it has been reported that WFV is the dominant source of statistical variability in nanowire MOSFETs [22], [38]. On the other hand, RDD has been reported to have a strong influence on nanowire TFETs figures of merits [25]. Therefore, it should be interesting for the reader to see the comparison of the influence of both WFV and RDD sources of variability on nanowire TFETs.

The device under studied here is shown in Figure 5(a) with RDD influence. The InAs homojunction nanowire with $N_S = N_D = 5 \times 10^{19}$ cm^{-3} is adopted. Other device parameters are the same as those in figure 1(a), as well as the configuration of WFV. Details of the RDD configuration and random generation can be found in Refs. [22] and [25]. The RDD region is only considered in the source region, being 10 nm long. The individual influence of the WFV and RDD on the $I_{ds} - V_{gs}$ characteristic of a InAs nanowire TFET is shown in Figure 5(b) and (c) with the nominal, mean, and median characteristics, respectively. For each source of variability, an ensemble of 200 TFETs have been simulated. Comparing the nominal curves in Figure 1(c) and Figure 5(b), the advantages of the InAs-Si heterojunction TFET are highlighted. It increases the I_{on} and simultaneously keeps a low SS, being a direct consequence from reducing the effective BTBT barrier height and in agreement with the previous report in Ref. [28]. The latter also demonstrates the validity of NESS.

From Figure 5, it can be seen that the variations caused by the RDD in both I_{off} and I_{on} are stronger than those caused by the WFV. Being a major factor determining the tunneling current, the electrical field across the source/channel tunneling junction is highly sensitive to the number and the position of the dopants in the source [25], [34]. Thus, RDD is a more damaging source of variability than WFV in TFETs, especially for I_{on} because the WFV has a weaker influence on it.

Note that the observations about the influences of WFV and RDD differs from that in previous works [18], [39],

where the WFV is reported to be the leading source of variability in TFETs. This difference may come from three reasons. Firstly, the nanowire sizes used in our work ($d = 3.5$ nm) and previous work (5×5 nm^2) [18] are different, since the variations are dependent on the size. The smaller the size, the severer the variation [9], [34]. Secondly, the simulation methodologies are different, since in previous work it seems that only the number of the dopants is considered in RDD and WFV is performed by changing the work-function value. Thirdly, the numbers of sample device may also be different. Thus, from our statistical result, compared to the WFV, it is clear that the RDD is the dominant source of variability in TFETs with extremely narrow nanowire in future technology nodes.

4. Conclusion

In summary, WFV-induced variability in p-type ultra-scaled nanowire TFETs has been studied. Quantum transport simulations were carried out by using the NEGF module of NESS computational framework developed at the University of Glasgow. First, compared to a Si nanowire MOSFET counterpart and considering the ultra-low power application, the V_{th} variation is comparable, the $\mathbf{I_{on}}$ variation is weaker, and the SS and $\mathbf{I_{off}}$ variations are stronger in TFETs. A weaker correlation between the V_{th} and current is observed, and the variation of $\mathbf{I_{off}}$ is much larger than that of $\mathbf{I_{on}}$ in the case of TFETs. Then, by comparing Fin and nanowire architectures with various t_{ox}, it is found that adopting the nanowire with smaller t_{ox} causes most serious $\mathbf{I_{off}}$ variation since this structure has excellent electrostatics which plays dominant role on variability under off-state. Last, contrary to the MOSFETs case, it is observed that compared to the RDD, the WFV is a less damaging source of variability in ultra-scaled nanowire TFETs. It should be noted that the conclusion is obtained under a high V_{ds}. Considering that drain-source voltage has some influences on the variability [12], the effect of V_{ds} on the variability of such scaled devices should be investigated in the future.

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