CHARACTERISATION AND STABILITY OF MESFETS FABRICATED ON AMORPHOUS INDIUM-GALLIUM-ZINC-OXIDE

By

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ABSTRACT

Indium-Gallium-Zinc-Oxide (a-IGZO) is an amorphous oxide semiconductor that has been attracting increasing attention for use in flat panel display and optoelectronic applications. This is largely due to IGZO's high mobility at low processing temperatures. In this thesis, IGZO films were successfully grown on polyethylene naphthalate (PEN) substrates by RF magnetron sputtering at room temperature. These films were flexible, transparent and had a good Hall mobility (5-12 cm^2/Vs). High quality metal oxide Schottky contacts were fabricated on these as-grown IGZO/PEN films with on-off rectification ratios of up to 10^8. These were then used as the gate contacts in transparent metal semiconductor field effect transistors (MESFETs). The performance and device stability of these IGZO/PEN MESFETs were investigated via a series of stress tests in both dark conditions and under illumination at different wavelengths in the visible spectrum. During constant voltage stress testing under illumination, the threshold voltage shifted by -0.54 V and 0.38 V for negative and positive gate biasing, respectively. These shifts proved reversible when devices were left in dark conditions for extended periods of time. The effect of persistent photoconductivity after exposure to different illumination sources was examined, with three potential passivation coatings to reduce this unwanted effect explored. Transparent IGZO/PEN MESFETs with an absolute transmission of up to 75% were achieved with the use of ITO ohmic contacts. These devices survived mechanical bending down to a radius of 7 mm with negligible variation in on-current and threshold voltage. This allows for the possibility of incorporating their use in future applications such as flexible transparent electronics.

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CHAPTER 1

Introduction

Today, silicon dominates the semiconductor industry. From cellular phones and laptops to TVs and dishwashers, everything runs on silicon – and for good reason, as silicon is a cheap, effective time proven technology. Consequently, considerable research and development effort is devoted to pushing silicon to its limits; however for at least one important application those limits will soon be reached: Flat-panel displays. Flat panel displays have continuously grown in size with higher and higher resolutions, and in response silicon based fabrication techniques have grown more complex to keep up with growing requirements. Unfortunately, silicon is just not able to keep up with demand.

Historically, amorphous silicon (a-Si) has been used in all flat-panel displays, and is currently still the most widely used material. While a-Si has a significantly lower mobility than polycrystalline silicon, <1 cm^2/Vs [1] compared to >100 cm^2/Vs [2], it is widely used because the main factors in material choice for flat-panel displays are cost and uniformity. A-Si has a reduced cost due to its fabrication at temperatures as low as 150 ºC [1], unlike the high temperatures of 340 ºC required for polycrystalline silicon [2]. However the main disadvantage of polycrystalline silicon that prevents its wide spread adoption are its grain boundaries that cause an unacceptable lateral variation of electrical properties, introducing uniformity issues. Unfortunately, while

its low processing temperature results in significant savings, a-Si typically has a low mobility and is unstable under both illumination and stress [3].

Silicon has served the flat-panel display industry well over the years, but nothing lasts forever. As the reign of silicon comes to an end, a new material must be sought out to fulfil the demand. The next generation of displays will be 4K screens with resolutions of at least 7680 x 4320 pixels, and high refresh rates of at least 120Hz. These requirements demand a field effect mobility of at least 3 cm^2/Vs [4], which typical a-Si cannot reliably deliver. This is where amorphous oxide semiconductors (AOS) step in.

In 1996, a conducting amorphous semiconductor [5] was discovered. Since then, these semiconductors have been extensively used as transparent conducting electrodes for solar cells in the form of indium tin oxide (ITO) and zinc tin oxide (ZTO). As these transparent conductors were widely adopted, the focus of amorphous semiconductor research changed slightly; if we have transparent conductors, can we have fully transparent electronics? The first answer to this question came in 2004 when Nomura [6] first reported on the room-temperature fabrication of indium-gallium-zinc-oxide (IGZO). This opened the doors to the first potential replacement of amorphous silicon as a pixel driver for the flat-panel display industry. While initial interest in IGZO was slow, as shown in Figure 1.1, in recent years there has been a significant increase in interest. In 2012, the first IGZO LCD TV provided by Sharp [7] went into production.

Nomura [6] showed this new AOS could not only be fabricated on glass for flat-panel displays, but could also be fabricated on polymers for use in flexible electronics. Previously, the notion of transparent flexible electronics was more of a

science fiction dream, but is now stepping closer to reality. Most transparent semiconductors, such as zinc oxide (ZnO), require high annealing temperatures [8] to achieve acceptable uniformity, which is not compatible with the low melting temperature of most flexible substrates. AOS's such as IGZO can be grown at room temperature with a sufficient mobility to act as a functional transistor. When combined with transparent electrodes such as ITO, it is then possible to make a fully transparent circuit.

The motivation behind this work was to fabricate and investigate the performance of metal-semiconductor field-effect transistors (MESFET) on IGZO. There has been a significant amount of research on the properties of metal-oxide-semiconductor field-effect transistors (MOSFET) fabricated on IGZO, but very little on MESFETs. By combining the transparency of thin gate layers with transparent electrodes such as ITO, a fully transparent MESFET was realised. As these devices could be fabricated at low processing temperatures, a flexible polymer was chosen as the substrate. A final goal was the production and characterisation of a fully transparent flexible MESFET.

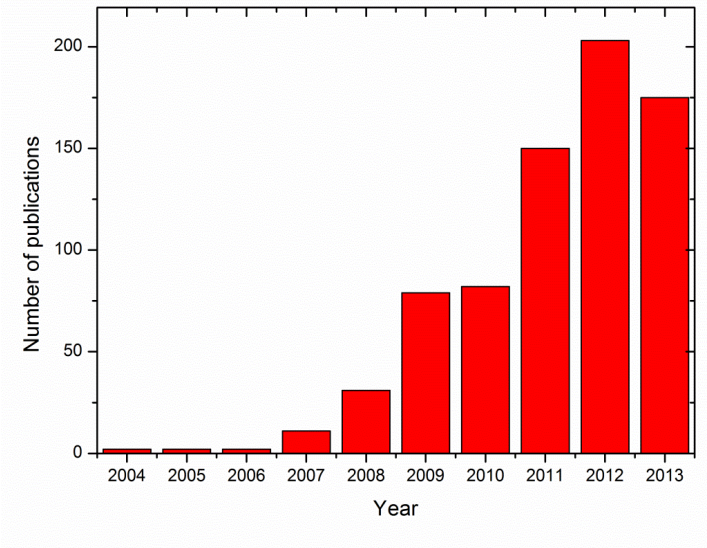

Figure 1.1 - Publications by year with the topic 'IGZO' as reported by web of science.

In this thesis, the following material is covered:

- Chapter 2: IGZO as a semiconductor is discussed along with its conduction mechanisms. A basic introduction into MESFETs is also given.
- Chapter 3: Covers film growth, device fabrication techniques and processes.
- Chapter 4: Several MESFET devices are characterised and their parameters are compared. There is a comparison between AgO_x, IrO_x and PtO_x gates as well as devices fabricated on co-sputtered films.
- Chapter 5: The devices are stress tested and their stability is analysed.
- Chapter 6: Different surface passivation layers are examined and their effectiveness characterised.
- Chapter 7: Devices are fabricated on a flexible transparent substrate with transparent electrodes. The optical transmission of the devices is investigated as well as their ability to withstand bending.

CHAPTER 2

Background Information

2.1 Oxide Semiconductors

Initially, oxide semiconductors were investigated in order to find a transparent conductor for liquid crystal displays and solar panels. This led to the discovery of the first few oxide semiconductors; indium oxide ($In_2O_{3)}$, tin oxide (SnO_2) and zinc oxide (ZnO) [9]. It wasn't until 1996 [5] that the possibility of a whole field of amorphous oxide conductors capable of delivering sufficient electrical performance to be useful in devices started to emerge. Until this point, the only amorphous oxide conductor that had attracted any attention was amorphous-In_2O_3 [10], however its structure and properties were poorly understood.

When interest in flexible electronics increased, oxide semiconductors were considered as the semiconductor material. Polycrystalline ZnO was one obvious choice, as it was possible to produce semiconductor devices at temperatures as low as 300 ºC. Unfortunately, these devices suffered from instability and uniformity issues due to grain boundaries present in the polycrystalline material. This need for better oxide semiconductors led to the discovery of $2CdO.GeO_2$ [11], zinc tin oxide (ZTO) [12], indium zinc oxide (IZO) [13], zinc indium tin oxide (ZITO) [14] and indium gallium zinc oxide (IGZO) [6]. As these materials are amorphous semiconductors, they do not suffer grain boundary instabilities, and can be fabricated at low temperatures with high uniformity.

Typically, amorphous materials do not conduct nearly as well as single crystal materials, as the bonding angle usually plays an important role in the conductivity. AOSs do not suffer this malady as the conduction path is composed of the extended spherical s orbitals of heavy metal cations [5], which leads to an insensitivity to bonding angle. The special ionic bonding structure of AOSs results in a conduction path without degradation even in an amorphous state [15]. The conduction path of a-Si however is based on covalent bonding with sp3 orbitals, resulting in a strong sensitivity to bonding angle. This leads to a significant degradation of mobility when compared to single crystal silicon. These different structures are illustrated in Figure 2.1.

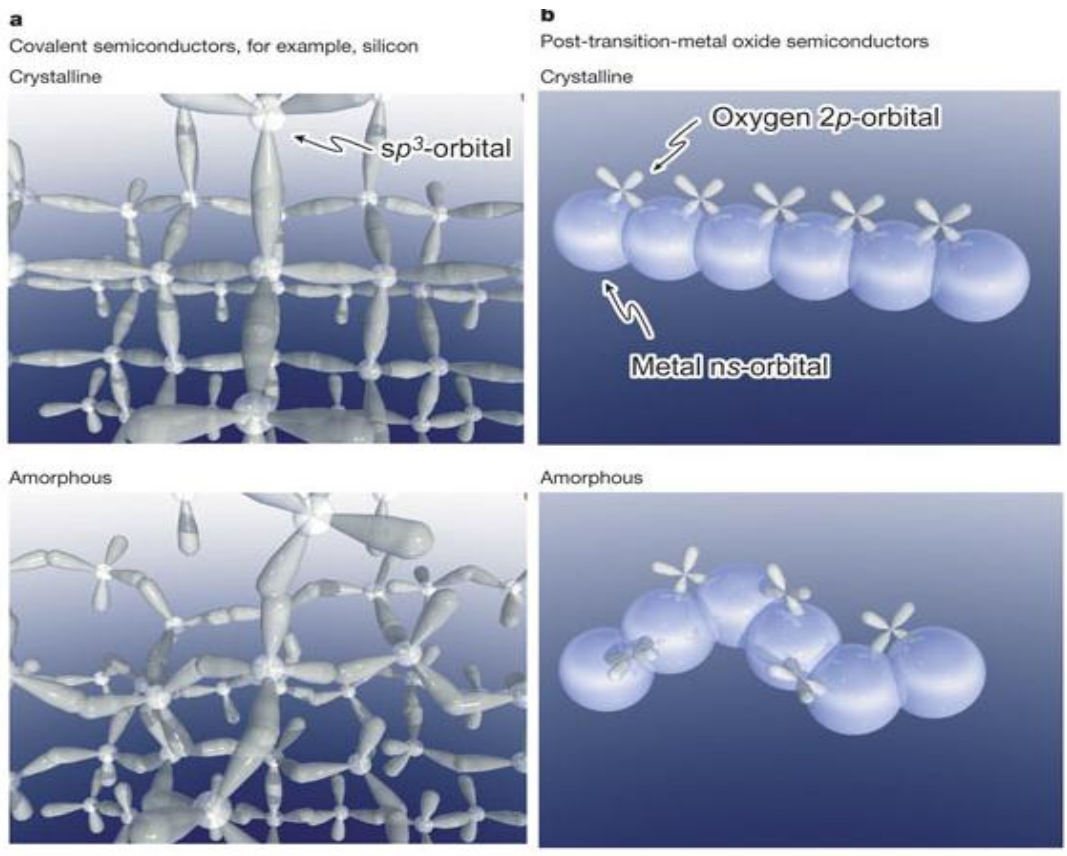

Figure 2.1 – Examples of conductions paths for a) covalent bonding such as silicon and b) ionic bonding such as IGZO [6].

2.2 Indium-Gallium-Zinc-Oxide (IGZO)

IGZO is formed from three different oxides, In_2O_3, Ga_2O_3 and ZnO. In_2O_3 and ZnO have been shown to have mobilities > 19 cm^2/Vs, however when grown at room temperature both are highly polycrystalline with high carrier concentrations that are difficult to control without compensation doping [16]. Ga_2O_3 has the opposite problem; it can be grown amorphously at room temperature but carrier doping is problematic. By combining these three materials, a conducting amorphous structure can be formed where each element plays a critical role. In_2O_3 has a large electron density and carrier concentration that can be supressed by adding Ga_2O_3. ZnO has a small atomic radius, which helps disperse the conduction band energy while also promoting an amorphous structure [16]. These three components allow for the production of thin films that can be tailored for different applications, by varying the composition to control the mobility and carrier concentration, as shown in Figure 2.2.

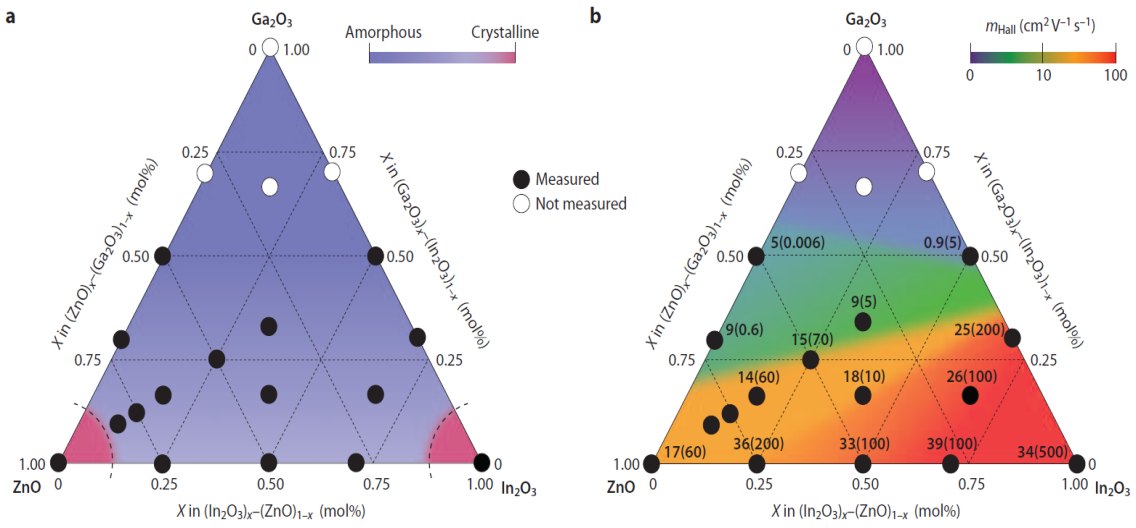

Figure 2.2 – a) Structure of different compositions of IGZO b) Electrical properties of IGZO Mobility (Carrier concentration 10^{18}) **[16] [17]**.

Initially, IGZO was investigated as a single crystal semiconductor [18], and it wasn't until 2004 [6] that IGZO became proven as an AOS. It was shown that there was a negligible difference in effective electron mobility between amorphous and crystalline IGZO [19], which supports the theory that large s-orbitals form a conduction path that is insensitive to bonding angle.

In crystalline IGZO (c-IGZO), the structure consists of alternating stacks of InO_2 and GaO(ZnO)+ layers [20]. The InO_2 layer found within crystalline IGZO form InO_6 octahedra, with separation distances much like that found within pure InO_2 crystals. The Ga and Zn ions on the other hand form trigonal-bipiramidal sites within the GaO(ZnO)+ layer. A comparison between these different structural elements can be seen in Figure 2.3. When the structure of c-IGZO was compared to that of a-IGZO, it was found that the distances between atoms were similar. It was also noted that the edge sharing network of InO_6 found in c-IGZO was also present in a-IGZO. However, as the InO_6 octahedra are more dispersed in a-IGZO than its crystalline counterpart, a-IGZO has a density approximately 5% lower than that of c-IGZO.

One of the issues with many AOSs such as IGZO is the photoresponse observed when exposed to photon energies above 2.3 eV, which is lower than its band gap of 3.1 eV [21]. The films become highly conductive when exposed to this illumination [22]. It is believed that this increased conductivity is due to the presence of oxygen vacancies (V_0) forming gap states near the valance band. When exposed to illumination, these oxygen vacancies become ionized, generating up to two electrons that are free to roam [23]. This causes an increase in conductivity, and also serious instabilities in transistor performance such as negative threshold voltage shifts [24].

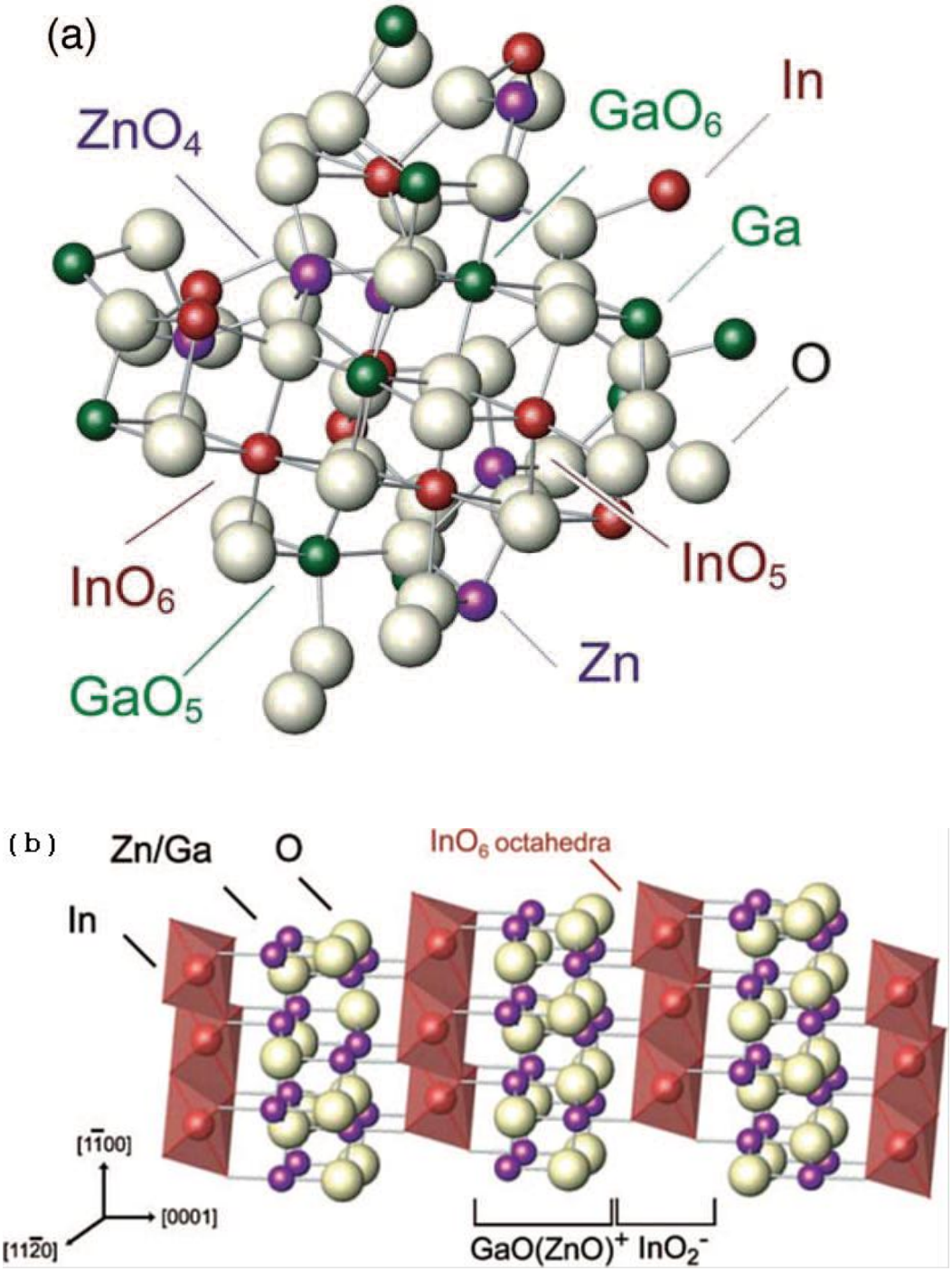

Figure 2.3 – The structure of a) amorphous IGZO showing the dispersed nature and b) crystalline IGZO showing alternating stacked layers **[20]**.

Both the increased conductivity and threshold voltage shift are recoverable, however the recovery time is typically very long (up to 20 hours in cases), although this can be reduced by low temperature thermal annealing [24].

2.3 Field Effect Transistor

The field effect transistor (FET) is the cornerstone of modern electronics, so much so that the average person owns billions of FETs without even knowing it. While a single FET by itself is just an electronic switch that can turn a single bit on or off, when thousands or millions of these switches are connected then complex operations can be performed. This is the cornerstone of the computer industry. In accordance with Moore's Law [25], FETs have been continually shrinking in size, and thus increasing their speed. This has allowed for ever more complex circuits to be built.

As mentioned earlier, a FET is just a simple switch. The FET works by modulating a current flowing through a predefined channel by applying a voltage to a gate covering the channel. The gate voltage generates an electric field, which is then used to modulate the conductivity of the channel. In depletion mode FETs, as the name implies, a depletion region exists that is depleted of free charge carriers, leaving none to carry a current. The gate voltage can be set in such a way so that the depletion region is removed, allowing current to flow freely between the drain and the source, or by increasing the size of the depletion region so that it fully blocks the channel preventing any current from flowing.

One of the key points of a FET is to keep the gate current as low as possible, as the gate is intended to be a trigger that allows or denies current flow between the source and drain. There are several different ways of reducing this gate current, and each type of FET uses a different method. The most common transistor structure used in

the semiconductor industry today is the metal-oxide semiconductor FET (MOSFET). The MOSFET uses a physical barrier in the form of an oxide layer between the channel and the gate to prevent any current flow. While oxides are typically used, in actuality the MOSFET is just a type of metal-insulator semiconductor FET (MISFET), as any high quality insulating dielectric can be used, such as Ge_3N_4 [26] or SiN_x [27].

Adding a physical barrier isn't the only way to prevent current flowing to the gate however. The junction FET (JFET) uses a reversed biased p-n junction to isolate the gate from the channel. By doping a portion of the channel with the opposite type dopant, a p-n junction is formed. Typically a JFET is normally on when no bias is applied to the gate, and when a bias is applied the depletion region formed by the p-n junction expands switching the FET off. A MESFET is similar to a JFET, except that a Schottky barrier is used instead of a p-n junction to isolate the gate. There are also several other more complicated FET configurations, however for this work MESFETs were fabricated as the FET of choice.

The MESFET has a key advantage over the more commonly used MOSFET, and that is a lower voltage operating range. The typical MOSFET has an operational voltage range of 20-40 V, while for a MESFET this can be reduced to 3-5 V. This significant reduction is due to the removal of the gate insulator, which effectively acts as a spacer for the electric field. As the electric field has to be larger in order to reach the channel to deplete it, a larger voltage is required. The MESFET also has a higher theoretical channel mobility. In a MOSFET, the charge carrier wavefunction extends into the oxide layer, and as the oxide layer is insulating, this reduces the mobility significantly. MESFETs however do not have this insulating layer and the depletion region keeps the charge carriers away from the gate interface, which can act as a

scattering centre significantly reducing mobility. This higher mobility allows for higher currents using the same cross-sectional area, as well as a higher transconductance and operational frequency of the device. However, advanced processing techniques along with improved quality films have reduced the mobility difference significantly. As with everything, the advantages of the MESFET come at a cost. While the presence of the Schottky barrier increases the mobility of the devices, it also limits the operational voltage of the device. As the gate voltage increases, it will reach a point where the gate is forward biased, which is not ideal, as current will flow through the gate as opposed to the desired drain-source route.

2.4 MESFET

Typically FETs are fabricated on a bulk substrate, using doping to generate prescribed areas of allowed conduction while creating reversed biased p-n junctions where conduction is not allowed. This prevents any lateral conduction, forcing the current to flow under the gate that can be used to modulate the flow. A thin film transistor (TFT) is a device that is fabricated on a thin film that has been deposited onto an insulating substrate. By removing the bulk material and replacing it with an insulating substrate, there is no longer any concern about unwanted lateral conduction paths circumventing the desired FET structure.

The best known application of TFT devices is in LCDs, where they are used as pixel drivers. TFTs have the advantage in this application because the transistors are fabricated directly on the panel, typically glass, as opposed to being attached to the panel. This can reduce crosstalk between pixels, which leads to improved image stability.

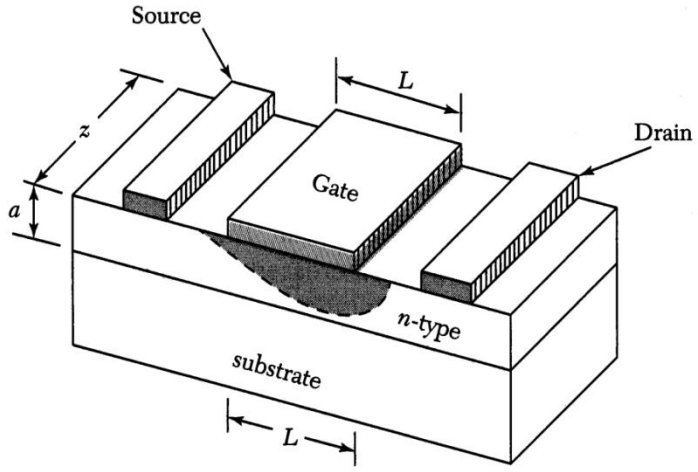

Figure 2.4 - Cross-section of a typical MESFET showing the linearity of the depletion region **[28]**.

The MESFET structure, as shown in Figure 2.4, is a thin film device with a source and drain separated by a gate. Depending on the fabrication process, the channel material outside the desired path is typically removed via etching or lift-off, leaving only the channel material to be modulated by the gate. While all three contacts are shown as one solid block of metal in Figure 2.4, these contacts can actually consist of multiple layers. Each layer has its own purpose, such as promoting good adhesion with the semiconductor, preventing contact oxidation or ensuring low resistance.

The following is a brief description of MESFET operation, as can be found in any semiconductor textbook such as [28]. The operation of a MESFET is controlled by the gate, therefore the section of the device under the gate is considered. Under normal operating conditions for a normally on device, the gate voltage (V_G) is either negative or set at 0 V, while the drain voltage (V_{DS}) is either set positive or 0 V. These voltages are given with respect to the source voltage. The channel has a resistance of

$$R = \rho \frac{L}{A} = \frac{L}{q\mu_n N_D Z(d-W)} \tag{2.1}$$

where L is the channel length, q is the charge of an electron, μ_n is the electron mobility of the channel, N_D is the donor concentration, Z is the channel width, d is the channel thickness and W is the width of the depletion region which can be expressed as

$$W = \sqrt{\frac{2\varepsilon_s(V_{bi}-V_G)}{qN_D}} \tag{2.2}$$

where V_{bi} is the built-in voltage of the Schottky junction and ε_s is the permittivity of the semiconductor. At any drain voltage, the voltage across the channel increases from V_S at the source (which is usually grounded) to V_D at the drain. This causes the Schottky junction to become increasingly reversed biased towards the drain, producing a sloped depletion region as shown in Figure 2.4.

When $V_G = 0$ and V_D is small, the drain current I_D is linear and can be expressed using Ohms law as

$$I_D = \frac{V_D}{R} \tag{2.3}$$

As V_D increases, the depletion region W also increases which in turn increases the resistance in the channel. As a result, the relationship between I_D and V_D is no longer linear. If V_D is increased enough such that W = D, the drain is completely pinched off by the depletion region. This voltage is known as the saturation voltage and can be described by:

$$V_{Dsat} = \frac{qN_D d^2}{2\varepsilon_s} - V_{bi} - V_G \tag{2.4}$$

At this point, the current flowing through the channel is known as the saturation current, I_{Dsat}, and is the maximum current that will flow through the channel before it

reaches breakdown. Any drain voltage in excess of V_{Dsat} will not result in any further increase in current, because increasing V_D just moves the point where the depleted region fully depletes the channel closer to the source. At this point the voltage is always V_{Dsat}, therefore the number of electrons moving past this point per unit time remains constant, thus the current remains at I_{Dsat}.

By applying a gate voltage in order to reverse bias the gate contact the depletion width increases as shown by Equation 2.2. For small V_D, the current is given by Equation 2.3; however the channel resistance increases as the depletion width increases. By increasing the gate voltage, eventually the depletion region will reach the substrate and the device will be fully depleted. This gate voltage is called the threshold voltage and can be found by rearranging Equation 2.2 to:

$$V_T = V_{bi} - \frac{qN_D d^2}{2\varepsilon_s} \tag{2.5}$$

To calculate the current at this point, we must first consider how the voltage drops across a section dy of the channel, this is given by:

$$dV = I_D dR = \frac{I_D dy}{q\mu_N N_D Z[a - W(y)]} \tag{2.6}$$

The depletion width at this point is:

$$\mathrm{W(y)} = \sqrt{\frac{2\varepsilon_S[\mathrm{V(y)} - V_G + V_{bi}]}{\mathrm{qN_D}}} \tag{2.7}$$

Since the drain current is constant and independent of distance, Equation 2.6 can be rewritten as

$$I_D dy = q\mu_n N_D Z[a - W(y)]dV \tag{2.8}$$

Differentiating Equation 2.7 to obtain dV gives

$$dV = \frac{qN_D}{\varepsilon_S} W dW \tag{2.9}$$

Substituting this into Equation 2.8 we obtain:

$$I_D = \frac{1}{L}\int_{W_1}^{W_2} \frac{q^2 \mu_n N_D^2 Z(a-W)}{\varepsilon_S} W dW \tag{2.10}$$

As W is linear with respect to y, this integration is trivial and results in:

$$I_D = \frac{Z\mu_n q^2 N_D^2}{2\varepsilon_S L}\left[a(W_2^2 - W_1^2) - \frac{2}{3}(W_2^3 - W_1^3)\right] \tag{2.11}$$

This can be rewritten in terms of pinch-off voltage V_P and pinch off-current I_P as:

$$I_D = I_P\left[\frac{V_D}{V_P} - \frac{2}{3}\left(\frac{V_D+V_{bi}+V_G}{V_P}\right)^{3/2} + \frac{2}{3}\left(\frac{V_G+V_{bi}}{V_P}\right)^{3/2}\right] \tag{2.12}$$

Where

$$I_P \equiv \frac{Z\mu_n q^2 N_D^2 a^3}{2\varepsilon_S L}, \quad V_P \equiv \frac{qN_D a^2}{2\varepsilon_S} \tag{2.13}$$

In the saturation region, I_{Dsat} becomes

$$I_{Dsat} = I_P\left[\frac{1}{3} - \left(\frac{V_{bi}+V_G}{V_P}\right) + \frac{2}{3}\left(\frac{V_G+V_{bi}}{V_P}\right)^{3/2}\right] \tag{2.14}$$

And the corresponding saturation voltage is

$$V_{Dsat} = V_P - V_G - V_{bi} \tag{2.15}$$

Equation 2.5 can then be simplified to

$$V_T = V_{bi} - V_P \tag{2.16}$$

which allows us to compare the threshold voltages in a more convenient manner.

CHAPTER 3

IGZO Growth and Device Fabrication

This chapter describes the growth and fabrication processes predominantly used in this work. It is assumed that the reader has a basic understanding of the photolithography and further background reading can be found here [29].

3.1 Substrate Preparation

Throughout this work, two different substrates were used in every film growth. The first substrate was quartz squares of both 10 mm and 20 mm square sizes. These were used as a general purpose substrate. The second substrate was a 0.5 mm thick polyethylene naphthalate (PEN) obtained from Goodfellow Cambridge Limited cut into 30 mm squares. PEN is one of the two main substrates that are used in flexible electronics today, the other being polyethylene terephthalate (PET) [30]. Both of these substrates are transparent polymers with good solvent resistance and temperature stability. PEN was chosen because although it is slightly less transparent, it has higher temperature stability and provides a more effective barrier to oxygen [30].

As each substrate arrived in a paper sleeve, they required cleaning before each film growth to remove surface carbon contamination. This is required as any dirt or contaminant on the surface of the substrate can cause defects in the films growth. Also, contamination can cause errors in the photolithography processes used in the fabrication steps. The substrates were cleaned using common solvents; acetone,

methanol and isopropyl alcohol (IPA). An ultrasonic bath was used in conjunction with each solvent in order to maximise the removal of contaminants from the surface.

3.2 Sputtering

In the semiconductor industry today, the two most widely used techniques to deposit films onto a substrate are chemical vapour deposition (CVD) and physical vapour deposition (PVD). The deposition method used in this work was sputtering, which is a type of PVD. There are four main steps to the sputtering process, 1) ejection of material from the target, 2) transportation of the ejected material to the substrate, 3) reaction of the ejected material with any gases, and 4) deposition of the ejected material on to the substrate [31].

The ejection of material from the target is achieved by ion bombardment from a plasma discharge. By setting up a large potential between two electrodes, electrons are discharged into the sputtering chamber. These ejected electrons interact with the working gas in between the electrodes, usually argon (Ar) due to its price and sputtering efficiency. The ejected electrons approach an Ar atom with enough energy to ionize the atom. This leaves the Ar atom as a positively charged ion. As the Ar^+ ion is in an electric field, it is accelerated towards the cathode. The Ar^+ ion striking the surface of the cathode transfers part of its energy to the target. Depending on the amount of energy transferred, atoms, ions or clusters can be ejected from the target into the chamber. This collision also generates additional electrons which are ejected as well, allowing the glow discharge to be self-sustaining. However, not all Ar^+ ions reach the cathode. Some of the Ar^+ ions recombine with the ejected electrons in the plasma, a process which releases a photon. This gives the appearance that the plasma is glowing, which explains why it is also known as a glow discharge.

Figure 3.1 - Sputtering system used for the majority of depositions performed in this work.

After the material has been ejected from the target, it travels through the chamber towards the substrate. Depending on the material being sputtered, it is possible to add in reactive gases into the chamber. By adding in O_2, N_2, or H_2, oxides, nitrides, or hydrogenated materials can be grown using this technique. Once the material reaches the substrate, it is absorbed on the surface, allowing a film to be grown.

Two different sputtering modes can be used: DC sputtering which requires a conducting target and RF sputtering with which an insulating target can also be used. Many of the targets used in the fabrication of AOS devices are insulating and if used in DC mode a positive charge build up will form on the surface of the target. This is turn means that not enough secondary electrons would be generated by the glow

discharge to allow it to be self-sustaining. This can be overcome by using a RF plasma source instead of a DC source.

RF sputtering is similar to DC sputtering in that it uses a glow discharge to bombard the surface of the target with ions in order to eject material and transport it to a substrate [32]. However, the main difference is in how the glow discharge is formed. By applying an RF frequency, typically 13.56 MHz, to the electrodes, the electron oscillations have enough energy to cause ionising collisions with the Ar atoms. As electrons have a higher mobility than the Ar^+ ions in the glow discharge, more electrons than ions reach the target in half a cycle. This causes a negative self-bias at the target surface, which is turn attracts more ions and repels electrons, allowing a self-sustaining sputtering process to be achieved.

Due to the different method of powering the sputtering process, RF sputtering can be achieved at a much lower pressure than DC sputtering. This lower pressure results in fewer collisions between the ejected materials and the plasma gases, resulting in a more direct path of travel between the target and the substrate. Therefore, while these two sputtering systems appear similar, the optimisation needed for each system can be significantly different.

Those interested in further reading on the subject of sputtering and recent sputtering advances can find more information on the topic at the following references [32]- [36].

3.3 IGZO Film Growth

As with any fabrication process, the films grown using RF sputtering can have significantly different properties depending on the parameters used in the growth.

There are several different factors that can cause film variations, including base pressure, processing pressure, oxygen pressure, power and substrate temperature. Varying any one of these factors by a small amount can cause a significant change in the mobility and carrier concentration of the resulting film. For this work, the devices were intended to be fabricated on a plastic substrate which has a low melting point, so a room temperature growth recipe was employed.

As every sputtering system behaves differently, the parameters that produce good results for one system may not be directly reproducible in another system. Therefore, while it is useful to read the literature to determine the parameters others have used to grow successful films, it is also necessary to optimise these parameters in the sputtering system used. The first parameter to be investigated was base pressure. All the films grown in this study used a molar 1:1:1 Ga_2:In_2:Zn:O_x target purchased from research and PVD Materials Corp (USA). The target was 3 in in diameter and ¼ in thick with a ¼ in copper backing to prevent target cracking during the sputtering process. All growths were conducted using the same RF recipe of a 3 W/min ramp to the target power, followed by a growth to a specific thickness as determined by a crystal monitor. Once the required thickness had been achieved, the power was ramped down at 3 W/min to 30 W before being turned off.

For these initial experiments, the power was 100 W, the process pressure $3.4x10^{-3}$ mbar of Ar, with no added oxygen. After several growths, it became apparent that any growth at a base pressure above that of $7x10^{-6}$ mbar, regardless of thickness, resulted in fully resistive films. It was also determined that the lower the base pressure, the greater the conductivity of the resultant film. This fact sets a maximum base pressure for all following experiments. The second parameter to be examined was oxygen

introduced during growth. It has been shown that additional oxygen can be an important tool in tuning the properties of AOS films, especially at low annealing temperatures [37], such as those used for films grown on plastic substrates. It was discovered, that even at the smallest partial pressure of O_2 measurable in the sputtering equipment used of $1x10^{-4}$ mBar, any film regardless of thickness was fully resistive. This eliminated the use of oxygen as a tool to modulate the properties of the films grown in our system. The final parameter examined in the growth of these films was the RF power used. There was very little difference in the properties of films grown at 75 W and 100 W. Films grown below 75 W showed an increasing resistance measured diagonally across each film, with 60 W films being twice as resistive as 75 W films while 50 W films were fully resistive.

Table 3.1 shows the results of these experiments. With the exception of growths A and E, the chamber was allowed to pump down for the same amount of time. The variance in base pressure can be explained by several possible reasons; i) how long the chamber was left open while the targets were swapped which could affect the amount of water vapour in the chamber, ii) the humidity of the day, iii) the temperature, or iv) the previous use of the chamber. As these factors cannot be completely controlled in a general research environment it was not always possible to get the exact same base pressure.

The films grown as part of the power series were examined using x-ray photoelectron spectroscopy (XPS) as shown in table 3.1. A detailed explanation of how XPS is used lies outside the scope of this work. For more information on XPS a standard spectroscopy textbook such as [38] can be used.

Growth	Power	Base Pressure (mbar)	Resistance (Ω)	Thickness (nm)
A	RF 100W	$1.4x10^{-5}$	∞	150
B	RF 100W	$6.0x10^{-6}$	110K	55
C[1]	RF 100W	$5.0x10^{-6}$	∞	46
D	RF 100W	$5.5x10^{-6}$	42K	60
E[2]	RF 100W	$4.6x10^{-6}$	11k	50
F	RF 75W	$5.5x10^{-6}$	44K	60
G	RF 60W	$6.0x10^{-6}$	90K	60
H	RF 50W	$6.0x10^{-6}$	∞	60
I	RF 25W	$6.0x10^{-6}$	∞	66
J[3]	DC 100W	$6.0x10^{-6}$	-	-

Table 3.1 - Growth comparison of IGZO over a range of settings. Notes: 1) in this growth 0.14SCCM of O_2 was added to the growth. 2) Liquid N_2 was used to further reduce the base pressure. 3) The plasma for this and subsuquent growths was unstable, so no film was produced.

Sample	C 1s	Ga 2p 3/2	In 3d 5/2	O 1s	Zn 2p 3/2	Ga/Zn	In/Zn	O/Zn	Ϛ (eV)
as-grown 100W	46	6	10	35	3	2.00	3.33	11.67	2.11
annealed 100W 120ºC 1h	48	5	8	37	2	2.50	4.00	18.50	2.02
25W	58	3	6	32	1	3.00	6.00	32.00	0.09
50W	47	6	9	36	2	3.00	4.50	18.00	0.004
60W	53	4	7	34	2	2.00	3.50	17.00	1.54
75W	44	6	10	37	3	2.00	3.33	12.33	2.63
100W	51	5	7	34	3	2.67	2.33	11.33	2.02

Table 3.2 – XPS results for IGZO films grown using various RF sputtering power, rounded to the nearest percent. The values of Ϛ were estimated from the valance band regions of the survey scans which consist of 2 to 3 data points for each linear fit.

The main conclusions from the XPS quantification data is that In:Ga:Zn ratios are significantly different compared to the composition of the molar 1:1:1 target. The expected ratios of films grown using a molar 1:1:1 target would be 1:1:0.5 In:Ga:Zn. However, the extracted results from the XPS analysis showed a ratio of approximately 1.6:1:0.5 In:Ga:Zn. A possible explanation is that preferentially sputtering of In over Ga and Zn has occurred in this sputtering system.

3.4 Co-sputtered IGZO Films

From table 3.2, it is clear that there is comparatively less Zn in all the samples than expected compared to In and Ga. Referring back to Figure 2.2 in Section 2.2, it is predicted that the less Zn in a film relative to Ga, then the lower the resulting mobility. The sputtering system described in the previous section has the ability to simultaneously co-sputter RF and DC targets. In this experiment, IGZO films were fabricated using the same RF sputtering recipe in Section 3.3, while at the same time an Al:ZnO (2% Al) target was sputtered using DC mode at 40 W. This co-sputtering process took approximately 40 minutes to deposit 70 nm of Al:IGZO, and the substrates were rotated during this time to evenly disperse the ejected material from the two targets. The substrates were arranged in the sequence shown in Figure 3.2. After the deposition was complete, it was discovered that only the films on the inner quartz substrates were conductive, while the middle and outer quartz substrates as well as most of the PEN substrates were fully resistive. This is believed to be due to the outer samples receiving more ZnO than the inner samples, causing sections of the films to be purely polycrystalline ZnO, disrupting the current flow mechanisms of a-IGZO.

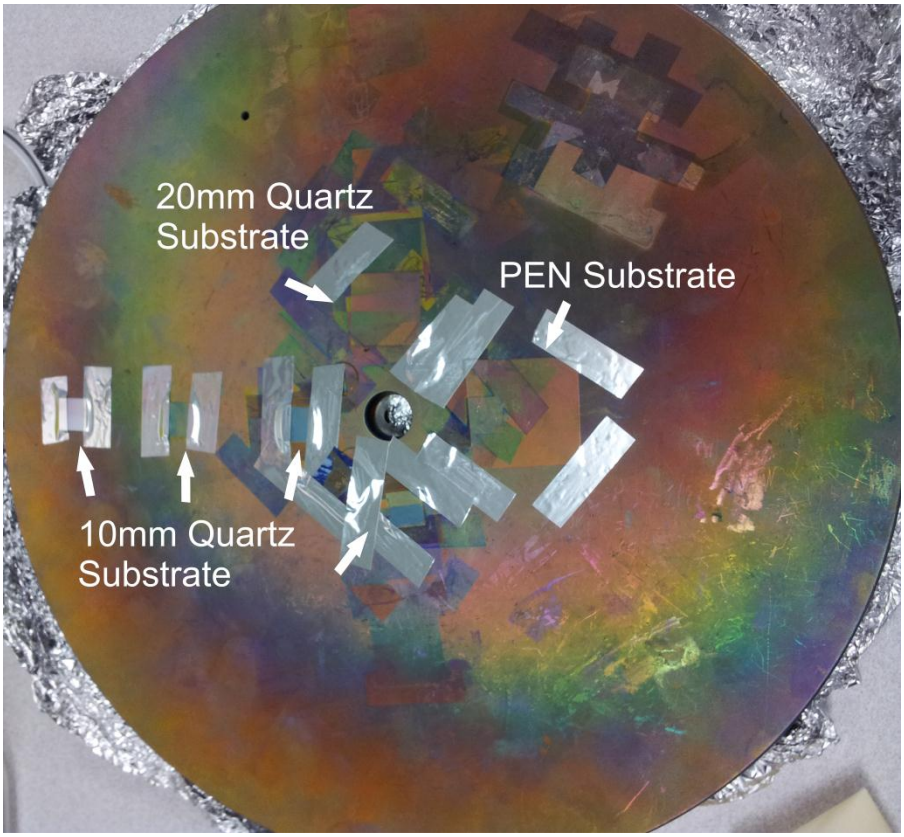

Figure 3.2 - Substrate layout prior to co-sputtered deposition. The small substrates are 10x10 mm quartz while the large substrate is 30x30 mm PEN.

The resultant films on the inner substrates had an initial resistivity of 112 kΩ, a measured Hall mobility of 5.5 cm^2/Vs and a carrier concentration of $4x10^{18}$ cm^{-3}. These results were not significantly different from purely RF sputtered IGZO films, potentially indicating that there was perhaps little additional ZnO added to the film, or that the ZnO was added in a way that disrupts the IGZO structure as opposed to aiding it.

3.5 Device Fabrication

For this work, a simple top gate TFT structure was fabricated on one of each of the grown film. While the layout of the structure can be changed to suit the required need for a specific application, the fabrication steps remain the same.

Once the film has been deposited onto a substrate, the first step in the fabrication process is to isolate each transistor. Isolation is required to define the specific gate width and length for each individual transistor, and to prevent current leaking outside of the desired conduction channel. In a typical MOSFET transistor this is done using junction isolation, which is where each transistor is surrounded by an opposite doping type. The opposite doping is then connected to a voltage source to create a reverse diode p-n region, and the depletion region created isolates the transistor from the rest of the circuit.

However, as there are currently no reliable methods to create p-type IGZO, a different type of isolation is required. Mesa isolation is where the conducting material is etched away down to the insulating substrate layer, thus preventing lateral conduction. An example of etching can be seen in Figure 3.3. There are several different methods to etch IGZO, such as dry etching with CH_4 [39] or SF_6 [40], and wet etching with NH_4Cl or HCl [41]. Each etching method has different etch rates, selectivity and ease of use, so selecting the correct etching method is important. While dry etching can give greater etch selectivity, it is a more complicated process both in the time involved and set up. Wet etching on the other hand is more suitable for mass production, and is widely used in flat-panel display fabrication lines. For these reasons, a wet etching approach was more desirable for fabricating devices used in this research.

Initial attempts with various concentrations of NH_4Cl (a successful etchant for ZnO) proved unsuccessful, so a stronger acid was tried. Successful etching was achieved using a 5% HCl solution. Etch rate experiments showed that this solution has an etch rate of 2.75-3 nm/sec. It is important to get the etch time right, as over-

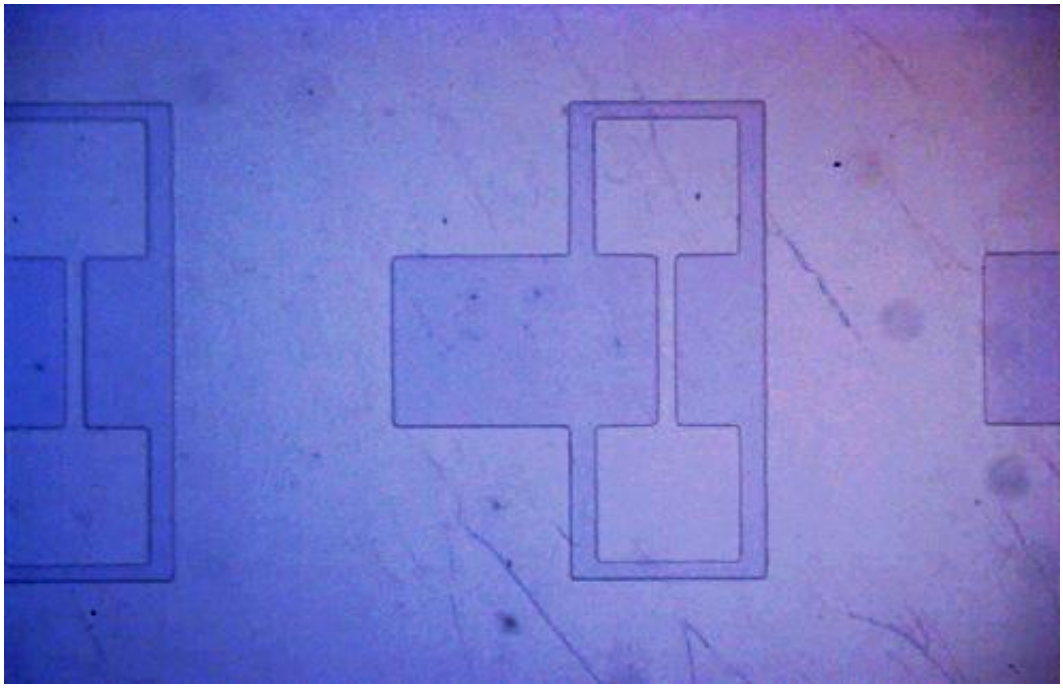

Figure 3.3 - Row of devices after Mesa etching on a PEN substrate.

etching will cause excessive undercutting, which can degrade or completely remove small features, while under-etching can cause excessive leakage of the device if the device is not fully isolated.

Once the etching has been completed, the next step is to fabricate the contacts of the MESFET. The ohmic and Schottky contacts can be fabricated in either order, however for this study the Schottky contacts were usually fabricated first as they are more sensitive to impurity contamination. The reasoning behind this is that the Schottky contact on a MESFET device is more important than the ohmic contacts in determining the ultimate performance.

The Schottky contact material used for the majority of this work was silver oxide (AgO_x). More details about choice of this material can be found in Section 4.4. The Schottky contact was deposited using reactive RF sputtering, with an RF power of 50 W in an Ar/O_2 atmosphere, at a pressure between $1.0x10^{-5}$ and $1.8x10^{-5}$ mbar

producing a contact thickness of either 10 nm, 30 nm or 50 nm, depending on the experiment performed. A capping layer of either indium tin oxide (ITO) or gold (Au) was then deposited on top. This capping layer was required because it achieves a lower sheet resistance for the contact, as well as providing an extra layer of protection between the measuring probes and the Schottky contact.

There are several possible materials to create ohmic contacts on IGZO [42] [43], however for the majority of this work the ohmic contacts used were a Ti/Au bi-layer. It is worth noting that in Section 7.1 ITO was used instead. The Ti/Au ohmic contacts were deposited using electron beam evaporation, while the ITO ohmic contacts were deposited using RF sputtering. In electron beam evaporation, the target crucible containing the desired metal is locally heated up above its boiling point using an electron beam. The heated target metal evaporates producing an atomic metal beam that is projected on to the semiconductor material.

For the Ti/Au bi-layer, 40 nm of titanium was deposited at a pressure range of $1.0x10^{-5}$ and $1.8x10^{-5}$ mbar. This deposition can cause the chamber temperature to increase to between 50-60 ºC, however as the fabrication is intended to be at room temperature a time gap was introduced between the two depositions to allow the chamber to cool down before 30 nm of Au was deposited. As the Ti was not exposed to the atmosphere very few oxidised Ti atom impurities are initially involved in the contact, which improves the contact resistance.

In order to remove the excess metal from the areas that were not designated by the contact mask, a lift-off process was used. This was chosen as opposed to an etch based approach because the majority of the chemicals used in etching would also

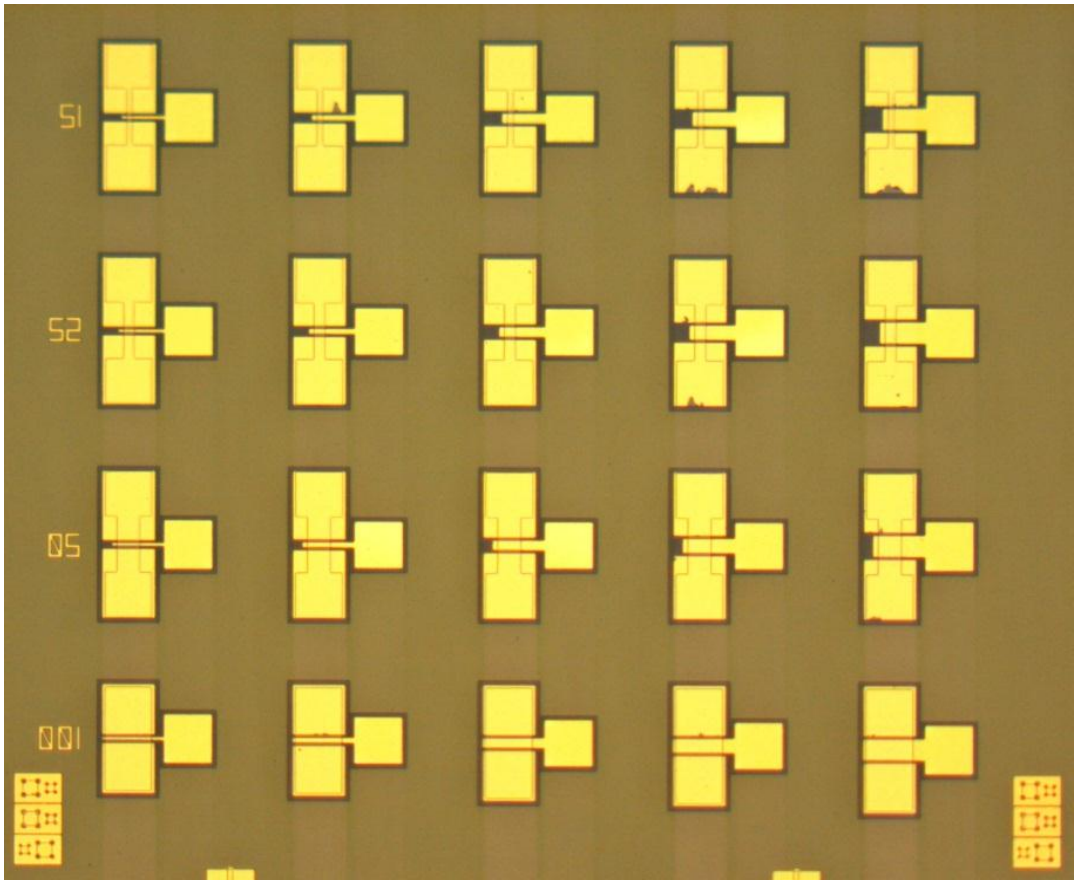

Figure 3.4 - Finished array of devices featuring a gold cap.

affect the material under the metal, potentially causing undercuts and reducing or impeding device operation. A lift-off process removes this problem. A lift-off process involves masking the semiconductor with a light sensitive polymer photoresist (AZ1518 in this case), so that the metal is deposited on top of the photoresist everywhere apart from the contact area defined by the mask. Once the contacts have been deposited, the sample is placed in an acetone solution until there is visible buckling of the excess surface metal. This shows that the photoresist below the metal has dissolved, so the metal is no longer supported. While it is possible for this process to completely remove all the excess metal, it is rare for all the unwanted material to be removed without using external agitation such as boiling the acetone or the use of an ultrasonic bath.

CHAPTER 4

Device Characterisation

This chapter outlines the steps required to characterise a specific MESFET device. The specific device chosen in this case is a MESFET fabricated on a PEN substrate with an AgO_x gate. The chosen device has a width to length ratio of 100/10 µm. There is also a comparison of the various device fabrication choices made throughout this work. These include:

1) The impact made on performance of the choice between substrate between quartz and PEN,
2) Changing the gate material between AgO_x, IrO_x and PtO_x,
3) Co-sputtered IGZO and Al:ZnO compared to pure RF grown IGZO.

All measurements were performed using a Hewlett Packard 4155B semiconductor parameter analyser. The devices were placed in a shielded probe station to prevent any outside interference such as stray electric fields and light to affect the results. The probes were positioned under illumination from a 20 mW/cm^2 halogen lamp. This was later discovered to cause an extreme photo-illumination effect in the devices, as discussed in Chapter 6. As the different samples were all tested in the same order and thus took approximately the same amount of setup time, this effect is believed to not have adversely affected the results gathered in this chapter.

4.1 Schottky Gate Analysis

The Schottky gate plays a dominant role in the operation of MESFETs, and as such its performance characteristics provide an important diagnostic of MESFET quality. As mentioned in Section 2.4, the drain and gate of a MESFET form a Schottky diode. By applying bias voltages across this diode and measuring the resulting current, several key parameters concerning the Schottky gate can be extracted from the subsequent data. In this case, the measurements were done in two parts. First, the voltage was swept from 0 to 2 V in 10 mV steps, and then the voltage was swept from 0 to -2 V using the same increments. This was done to reduce noise integration errors introduced by the parameter analyser when measuring extremely low currents.

By plotting the measured data in a linear I-V curve, the first figure of merit can be extracted. Although the I-V curve initially increases as an exponential, the current is quickly limited by the total series resistance present. Figure 4.1 shows the measured I-V curve for the selected device. As expected, the linear I-V curve displays typical diode characteristics, with the current being determined by the series resistance above 0.8 V. This total series resistance can be extracted from the curve by plotting the trend line of the linear region, and extracting the inverse of the slope, 180 kΩ in this case. Total series resistance is the combined effect of the material resistance and the contact resistance present in both the ohmic and Schottky contacts. Ideally this value should be as low as possible to ensure optimal device performance, however further attempts to reduce series resistance values were not the subject of this thesis.

The reverse leakage resistance can be calculated in a similar manner using the reverse current instead of the forward current. In the ideal case, this current would be negligible until the device reaches the breakdown region, at which point the device

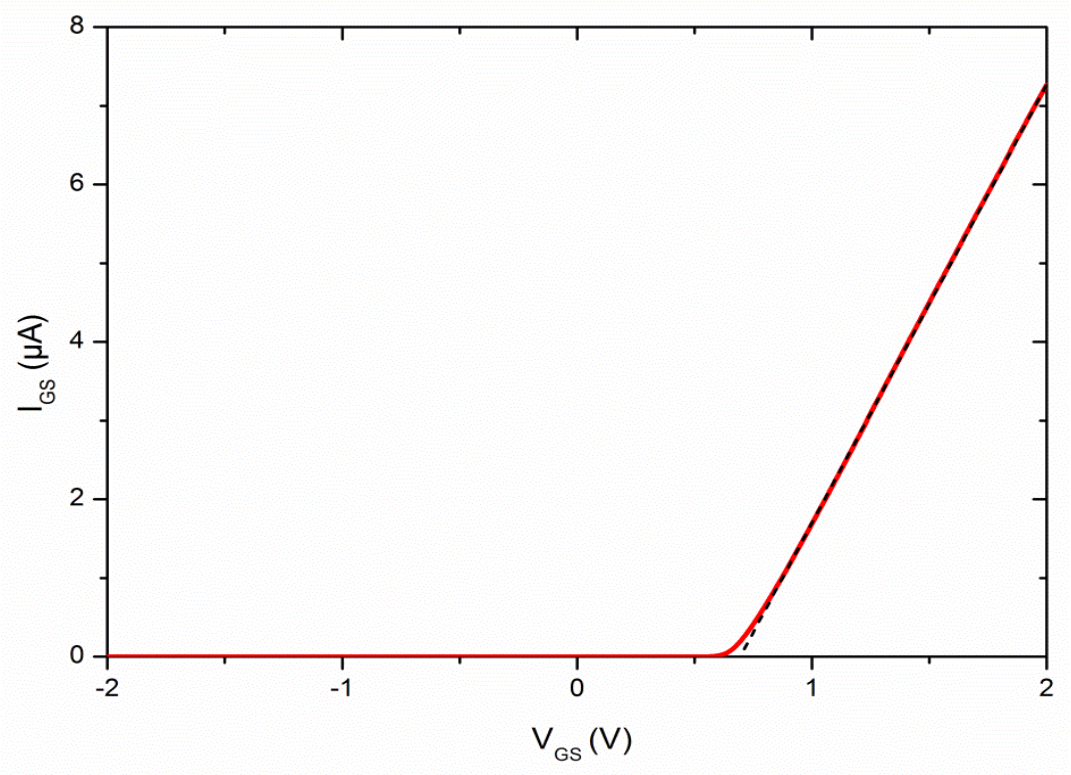

Figure 4.1 – Schottky diode current-voltage curve depicting forward current becoming essentially linear. The dashed line indicated the slope used to determine series resistance.

current would increase exponentially in the reverse direction. While not shown in Figure 4.1 as there is very little information to be gained past -2 V, until it reaches breakdown at 5.6 V. The reverse leakage resistance in this case was 220 GΩ.

While the linear I-V curve does show typical diode behaviour, it is not the most useful representation of the data. By plotting the data in a semi-log plot, two more useful parameters can be extracted from the data; the ideality factor η and the effective barrier height ϕ_B. The ideality factor is effectively a comparison between how the diode is behaving in practice versus how it would behave in the ideal thermionic emission approximation without tunnelling. In the absence of tunnelling, then the ideality factor should be very close to unity. Larger ideality factors indicate compromised device performance and laterally inhomogeneous Schottky contacts.

Typically, a MESFET Schottky contact would have an ideality factor between 1 and 2; however defects in the IGZO material and device fabrication processes can cause ideality factors greater than 2. To calculate the ideality factor, we must first look at how the device would function in the ideal case by looking at the ideal Schottky diode equation, a derivation of which can be found in most semiconductor textbooks [28]. The ideal diode equation is:

$$J = J_s\left(e^{qV/kT} - 1\right) \tag{4.1}$$

where q is the charge of an electron, V is the applied voltage, k is the Boltzmann constant, T is the temperature and J_s is the saturation current density which can be calculated by:

$$J_s = A^*T^2e^{-q\emptyset_B/kT} \tag{4.2}$$

where A* is the effective Richardson constant, and ϕ_B is the effective barrier height.

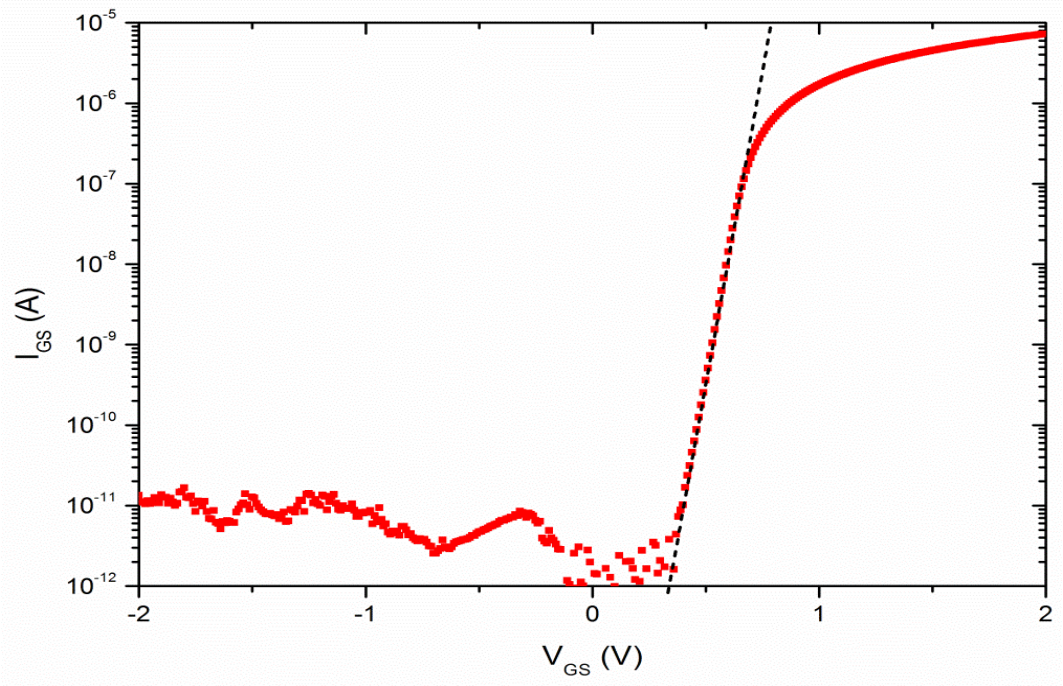

Figure 4.2 – Schottky diode current-voltage semi-log plot. The dashed line indicates the region where Equation 4.1 is valid.

From Equation 4.1, the slope of the line in Figure 4.2 for the ideal case would be q/kT, and any derivation from that is included in the ideality factor η. The slope is 35.39 V^{-1}, which corresponds to an ideality factor of 1.1.

The intercept of the slope gives the saturation current, I_s, which can be used to calculate the saturation current density, J_s, by dividing by the contact area A. By using an effective mass of $0.34m_e$ [19], the effective Richard constant can be calculated to be 41 $Acm^{-2}K^{-2}$ [44]. Substituting these values back into Equation 4.2 and solving for ϕ_{Bn} gives a barrier height of 1.07 eV for this particular diode.

4.2 MESFET output curve

The typical method of comparing FET operations is to consider the generated set of output curves, such as those shown in Figure 4.3. This set of curves was generated by setting a specific gate voltage value and then sweeping the source-drain voltage V_{DS} from 0 to 5 V. The gate voltage range was chosen to run the FET through all its operational modes without driving the device into breakdown. There are several key regions to this set of curves, as they show how well a device operates. The key considerations when analysing a set of FET output curves are: 1) Can the channel be completely turned off? 2) Is there a linear region? 3) Does the channel fully saturate?

To determine the functionality of this device as a MESFET, the above questions can be answered. There is a clear linear region to the MESFET curves depicted in Figure 4.3 for all visible curves. In the linear region, the current is proportional to V_{DS}/R_c, where R_c is the channel resistance. However, as V_{DS} increases, the cross-sectional area of the current path also increases, until it reaches the maximum area defined by the channel cross section. This point marks the saturation current, which for an ideal MESFET should be flat. The device shown has a positive gradient to its

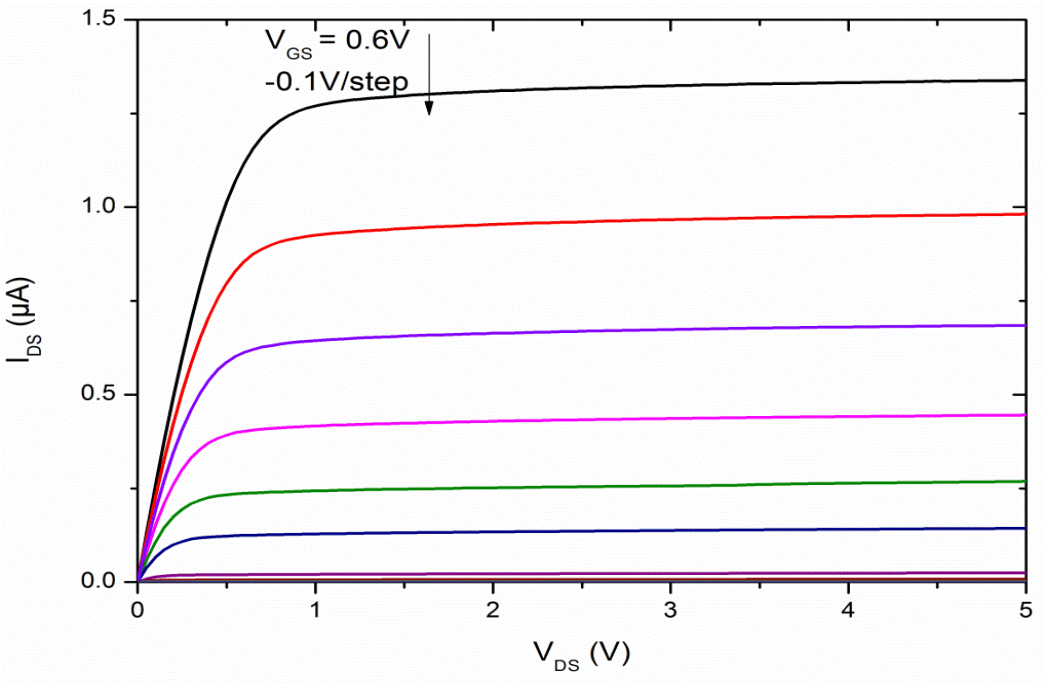

Figure 4.3 - Output MESFET curves for the tested device.

saturation region, which can be accounted for by current leaking from the gate. Finally, it can be seen that as the gate voltage decreases below -1 V, there is negligible current flowing, showing that the channel is fully depleted.

4.3 Transfer Curve

While the MESFET output curves give a nice visualisation to the operation of the device, it is not the most useful data set. The most useful representation of the MESFET operation is the transfer curve, in which V_{DS} is held steady at 2.5 V and the gate voltage V_G swept from 1.5 V to -3 V. The subthreshold swing (S), which is a measure of how fast the device can be switched on and off, can be extracted from the steepest region of Figure 4.4 by using the following equation:

$$S = \left(\frac{\partial \log(I_D)}{\partial V_{DS}}\right)^{-1} \tag{4.3}$$

The subthreshold swing for this device was measured to be 120 mV/dec, which is significantly lower than the 600 mV/dec of a typical a-Si MOSFET device [45] and

comparable to the 112 mV/dec and 123 mV/dec of similarly fabricated IGZO MESFETs reported by other groups [46]. This switching speed is congruent with the inherent switching advantages of MESFETs, including a reduced voltage range required to switch the device from on to off. Figure 4.4 also shows off-currents as low as $1x10^{-13}$ A and an on-off ratio of 7.5.

By taking the square root of the transfer curve as shown in Figure 4.5, the threshold voltage V_T and the channel mobility μ_n can be calculated. The threshold voltage is the point at which the transistor has started to significantly move from its off state, and is given by the x-intercept of the line of best fit as shown in Figure 4.5. In this case, the threshold voltage is -0.22 V. While a negative threshold voltage typically implies that the transistor is usually on, this was only the case when these devices have been exposed to illumination, details of which are explained further in Chapter 6.

The channel mobility is an important measure of the performance of a transistor, and is typically used to compare different channel materials. While largely dependent on the material used for the channel, fabrication processes can also impact the channel mobility. The channel mobility can be calculated by analysing the current in the saturation region, using:

$$I_{Dsat} = \frac{W\mu_n\varepsilon_s}{2aL}(V_G - V_T)^2 \tag{4.4}$$

Rearranging for μ_n gives:

$$\mu_n = \frac{2aL}{W\varepsilon_s}\left(\frac{\sqrt{I_{Dsat}}}{V_G - V_T}\right)^2 \tag{4.5}$$

where a is the channel thickness, L is the gate length, W is the gate width, ε_s is the

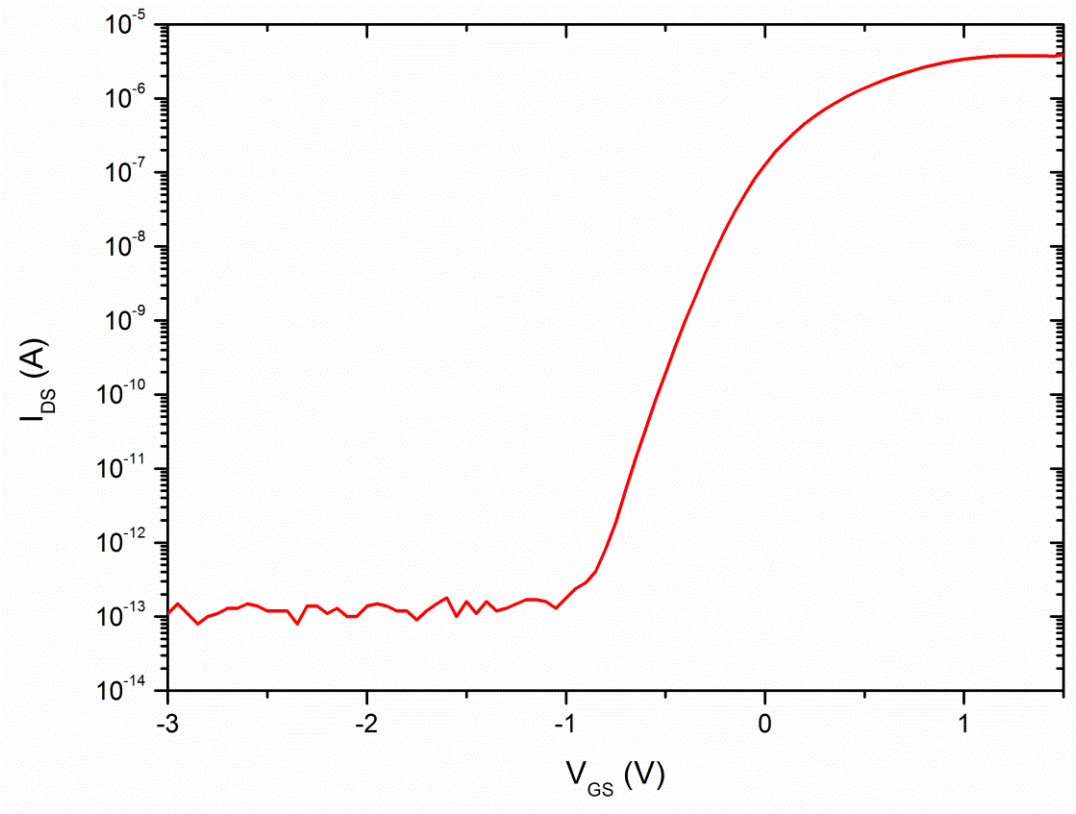

Figure 4.4 - Transfer curve of selected device.

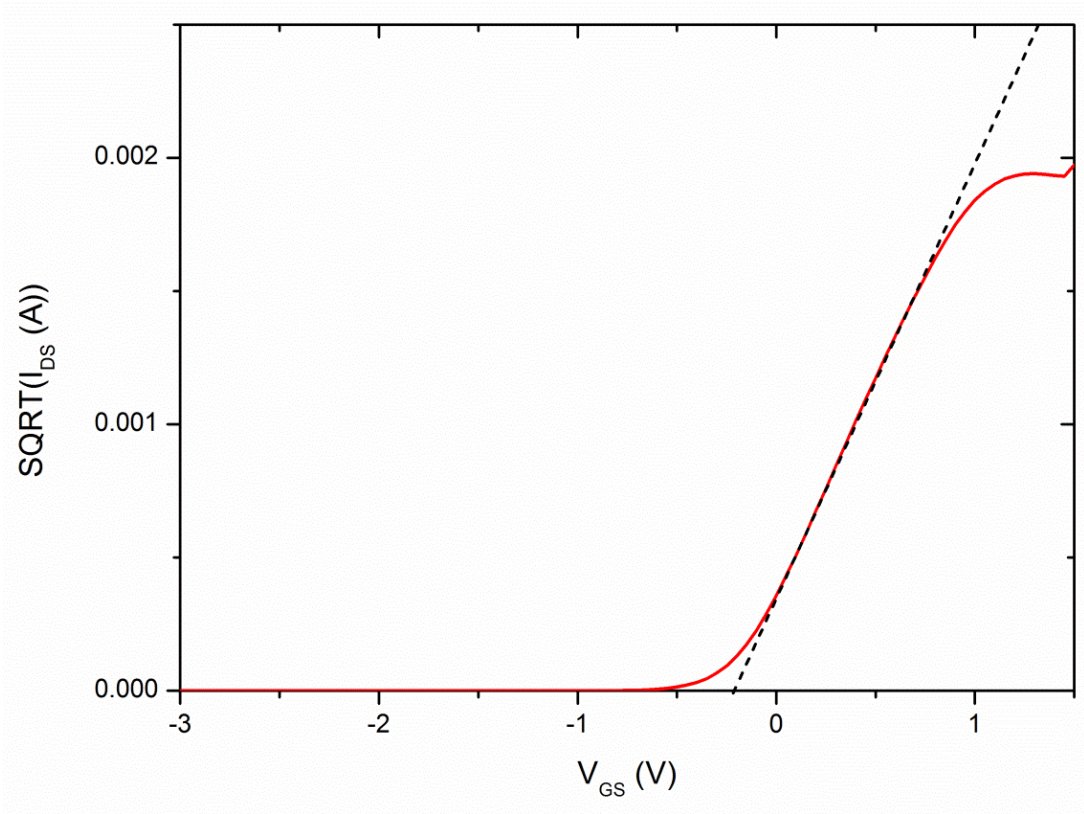

Figure 4.5 - Square-root of I_{DS} verse V_{GS}. The intercept of the dashed line gives threshold voltage while its slope allows for mobility to be calculated.

relative permittivity, 11.5 for IGZO [47], and the bracketed region is the slope of Figure 4.5. Substituting these values into Equation 4.5 gives a mobility of 3.1 cm^2/Vs, which while lower than the Hall mobility of the IGZO material of 6 cm^2/Vs, it is within the expected range and a possible explanation is that the channel mobility has been affected by material degradation during the fabrication process.

4.4 Initial Gate Comparison

In this comparison, three different Schottky materials were compared; silver oxide (AgO_x), iridium oxide (IrO_x) and platinum oxide (PtO_x). In order to reduce any potential variation in the fabrication process, the fabrication steps of each device were, where possible, performed concurrently. The IGZO material was grown on a 10 mm square quartz substrate by RF magnetron sputtering at a base pressure of $5.5x10^{-6}$ mbar. The substrate was then cut into 5 mm squares, followed by the MESFET fabrication processes described in Chapter 3. The AgO_x gate was deposited using RF magnetron sputtering, while the IrO_x and PtO_x gates were deposited using eclipse pulsed laser deposition (PLD) [48]. These depositions were performed using at a partial oxygen pressure of 100 mTorr. All three gates were capped with an Au layer to increase conduction and to increase the mechanical durability of the contact.

The same analysis as previously outlined was performed on the three different gate compositions. In this comparison shown in Figure 4.6, there are two examples of PtO_x gate devices but only one each of devices with IrO_x and AgO_x gates. This is due to the fact that the PtO_x gates suffered some damage during the fabrication process, producing a variation in performance. The PtO_x MESFET with the same gate dimensions as the IrO_x and AgO_x devices had a short across the contacts from an

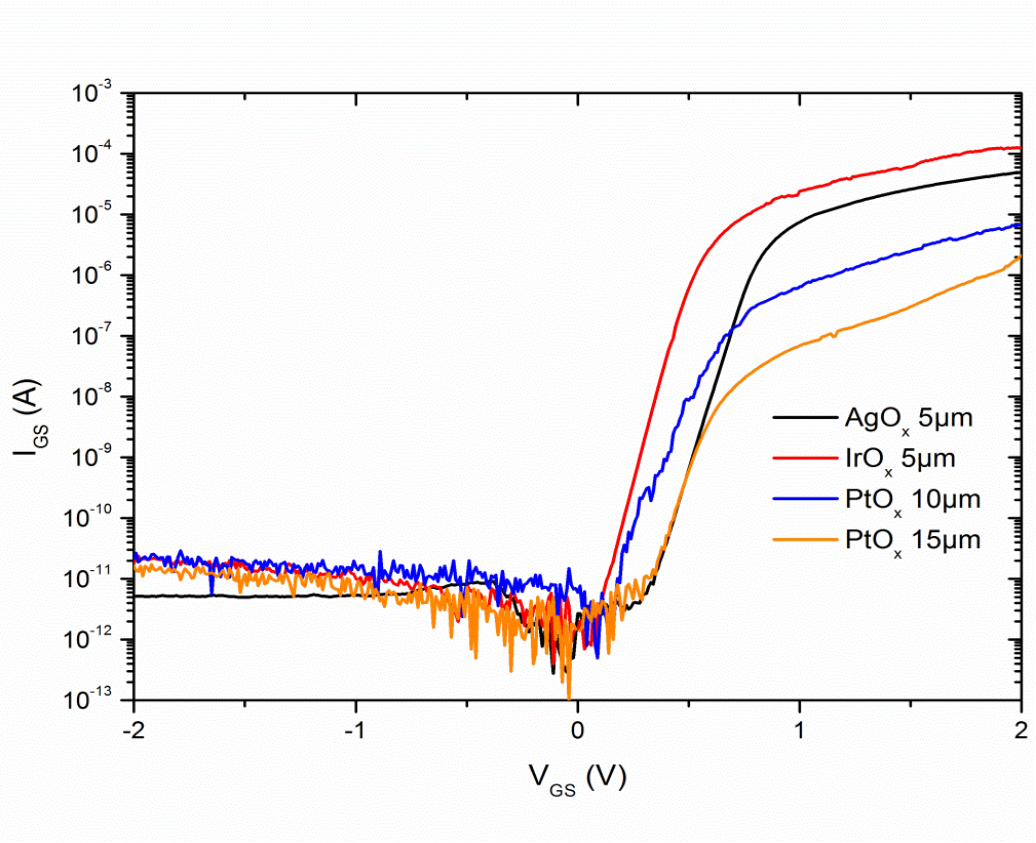

Figure 4.6 – Comparison of Schottky diodes with channel width 100 µm and varying gate lengths and metals.

incomplete the lift-off process. It can be seen in Figure 4.6 that the next transistor, which has a gate length of 10µm instead of 5 µm, had a poor Schottky contact resulting in a noisy signal, and an ideality factor of 2.1. Transistor 53, which has a gate length of 15µm, represents one of the better devices formed using PtO_x gates, with an ideality factor of 1.6.

Comparing the series resistance values, it can be seen that the PtO_x gates have significantly higher series resistances, 100-106 kΩ, compared to those of the AgO_x and IrO_x gates at 24 kΩ and 16 kΩ respectively. This suggests that the PtO_x gates made a poor contact with the IGZO, or that the PtO_x itself is not as conductive as the other gate materials. The high series resistance of the PtO_x gates is also responsible for the lower forward currents. The ideality factors of the IrO_x and AgO_x gates, at 1.2

and 1.4 respectively, suggest that a good contact has formed with the IGZO. The calculated effective barrier height for the AgO_x gate is slightly lower than that reported earlier in this Chapter (0.97 eV vs 1.07 eV), however it is still within the range reported elsewhere [46]. Similarly, the calculated effective barrier height of 0.81 eV for the PtO_x gate device is also consistent with a reported value of 0.91 eV [49]. Currently, no IGZO devices have been published using an IrO_x Schottky gate, therefore no comparison can be made to the 0.84 eV calculated here.

Considering the set of MESFET output curves generated for each gate type as shown in Figure 4.7, it is apparent that the underlying IGZO was too conductive for the devices to fully deplete the channel. This is most readily seen for the AgO_x and IrO_x output curves. This is also shown in the MESFET transfer curves, which have a maximum on-off ratio of 2 orders of magnitude for the AgO_x gate, and less than 1 for the IrO_x and PtO_x gates. This effectively means that the transistors cannot be turned off regardless of the gate voltage.

While not entirely useful given the poor performance of the MESFETs, the threshold voltage and channel mobility can be extracted from these devices for comparisons purposes. The channel mobility for all three gates, 1.28, 1.06 and 2.17 cm^2/Vs for AgO_x, IrO_x and PtO_x respectively, are all lower than that of the IGZO material Hall mobility of 6 cm^2/Vs. This is expected as the Hall mobility is a representation of the material while the channel mobility is a representation of the completed device, which has additional contact resistances and scattering effects that lower the effective mobility. A comparison of the extracted values can be seen in Table 4.1.

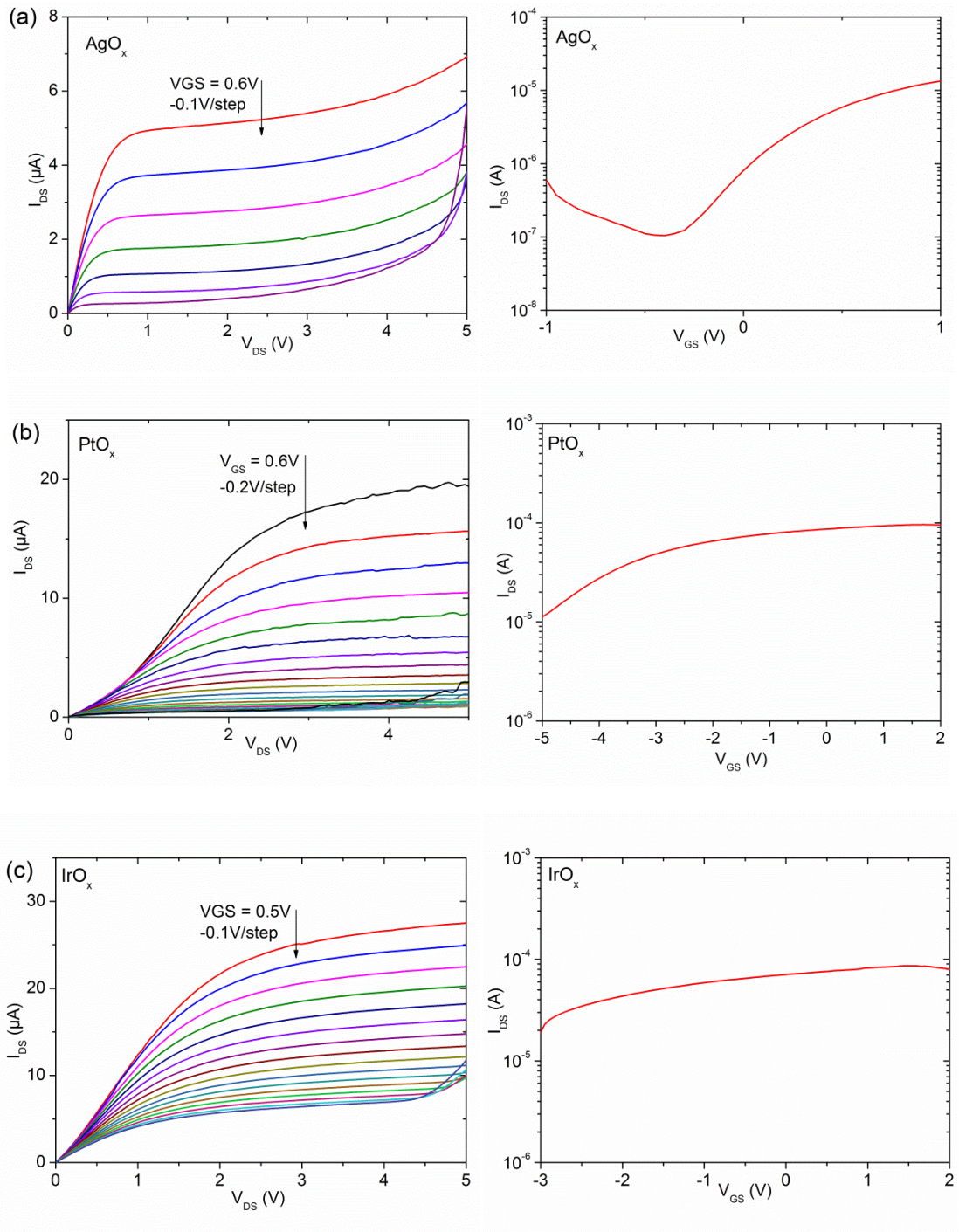

Figure 4.7 – MESFET output curves and corresponding transfer curves for a) silver oxide, b) platinum oxide and c) iridium oxide.

Sample	Series Resistance (Ω)	Ideality Factor	Barrier Height (eV)	Threshold Voltage (V)	Channel Mobility (cm^2/Vs)	Subthreshold Swing (mV/dec)
AgO_x	24K	1.4	0.97	-0.90	1.28	337
IrO_x	16K	1.2	0.84	-6.89	1.06	2449
PtO_x	100K	2.1	0.81	-6.71	2.17	2287

Table 4.1 - Gate comparison information.

4.5 Aging Gate Comparison

Upon completion of the measurements in Section 4.4, the devices were covered in photoresist to slow down oxygen absorption, which is known to adversely affect IGZO transistor performance. The devices were covered and left in the dark for a full year, at which point the photoresist was removed and the devices were characterised again to check if they were still operational.

Once the devices were remeasured, it became apparent that while the aging process was slowed by the use of photoresist, it was not completely prevented. All the devices suffered a Schottky gate forward current reduction of approximately one order or magnitude. This reduction actually proved beneficial to the device performance, and was most likely caused by a reduction in the carrier concentration in the film caused by the absorption of oxygen filling oxygen vacancies. Unfortunately device PtO_x 53 was not operational upon being measured again.

The aging process produced an increase in the series resistance of all three gate types. There was a 525% increase in the series resistance of the AgO_x gate, a 468% increase in the series resistance of the IrO_x gate, and a 74% increase in the series

resistance of the PtO_x gate. This shows that all three of the gate types continued to oxidise while aging, reducing the conductivity of the gate contacts. The ideality factor of the IrO_x gate improved slightly, from 1.2 to 1.1, while the ideality factor of the PtO_x gate improved significantly from 2.1 to 1.3. The AgO_x device however showed an increase in ideality factor from 1.4 to 1.7. This is largely due to the introduction of a second barrier for the AgO_x device. This second barrier suggests the AgO_x gate had oxidised at different rates. The barrier height of both the IrO_x and PtO_x gates increased, while the barrier height of the AgO_x device remained relatively constant.

Another interesting point of note is that the reverse current of the gates' Schottky diode characteristic (shown in Figure 4.8) now has a hump in it. This was initially thought to be a measurement integration error, however the hump appeared in the same position while measuring the current in both directions and turned out to be a consistently observed feature. While thought to be a charging effect, further attempts to verify the cause proved unsuccessful.

A remarkable improvement is evident in the MESFET output and transfer characteristics of the aged MESFETs as shown in Figure 4.9. Considering the aged MESFET output curves it can be seen the all three gate types now have well defined saturation regions, clear linear regions, and little gate leakage even at higher source-drain voltages. This is a significant improvement over the original testing, as the devices now act as fully operational transistors. There is also a significant improvement in on-off ratios, with the AgO_x gate increasing to 8 orders of magnitude from the original 2, while the on-off rations of the IrO_x and PtO_x gates increased to 7 orders of magnitude from less than 1. Since these devices now have a recognisable field effect, their figures of merit can be extracted with increased accuracy. The threshold voltage of the three gate types were -0.25 V, -0.35 V and 0.27 V for AgO_x,

IrO_x and PtO_x respectively. The AgO_x V_T is comparable to the initial result found in earlier in section 4.2. The channel mobilities were all approximately the same as the values measured earlier at 1.1, 3.1 and 1.4 cm^2/Vs for AgO_x, IrO_x and PtO_x respectively.

Sample	Series Resistance (Ω)	Ideality Factor	Barrier Height (eV)	Threshold Voltage (V)	Channel Mobility (cm^2/Vs)	Subthreshold Swing (mV/dec)
AgO_x	126K	1.7	0.99	-0.25	1.1	119
IrO_x	75K	1.1	0.96	-0.35	3.1	135
PtO_x 52	174K	1.3	1.10	0.27	1.4	108

Table 4.2 - Gate comparison upon aging.

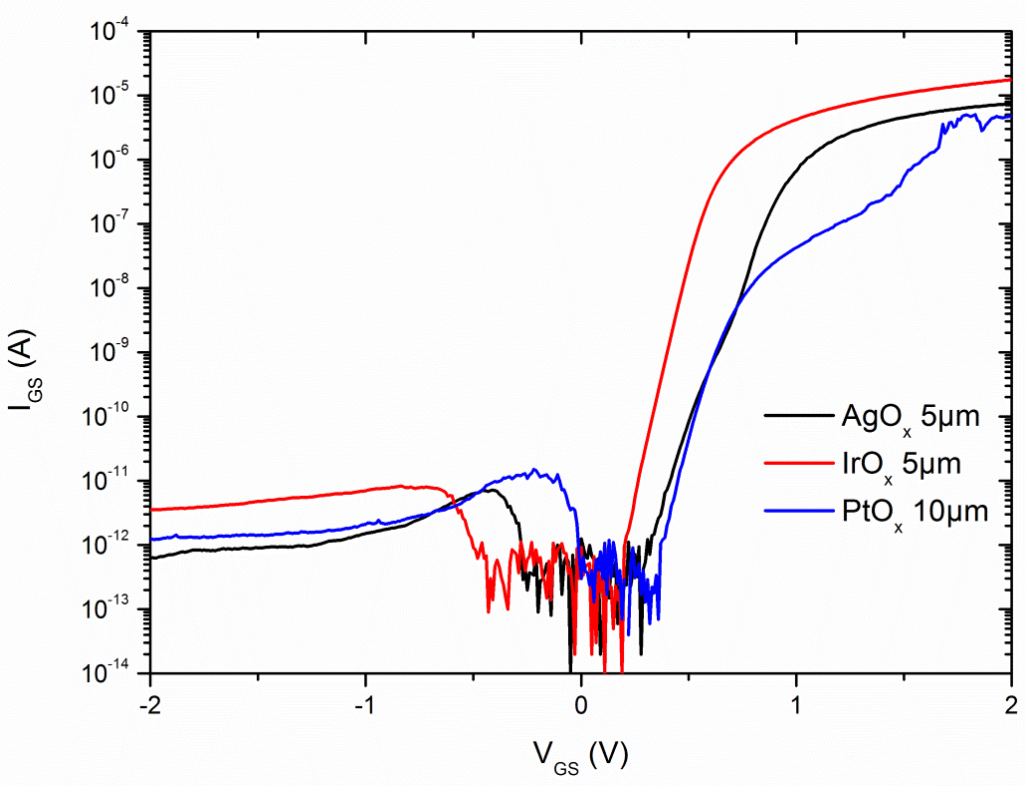

Figure 4.8 – Current-voltage characteristics of Schottky devices aged for one year under photoresist in a dark draw.

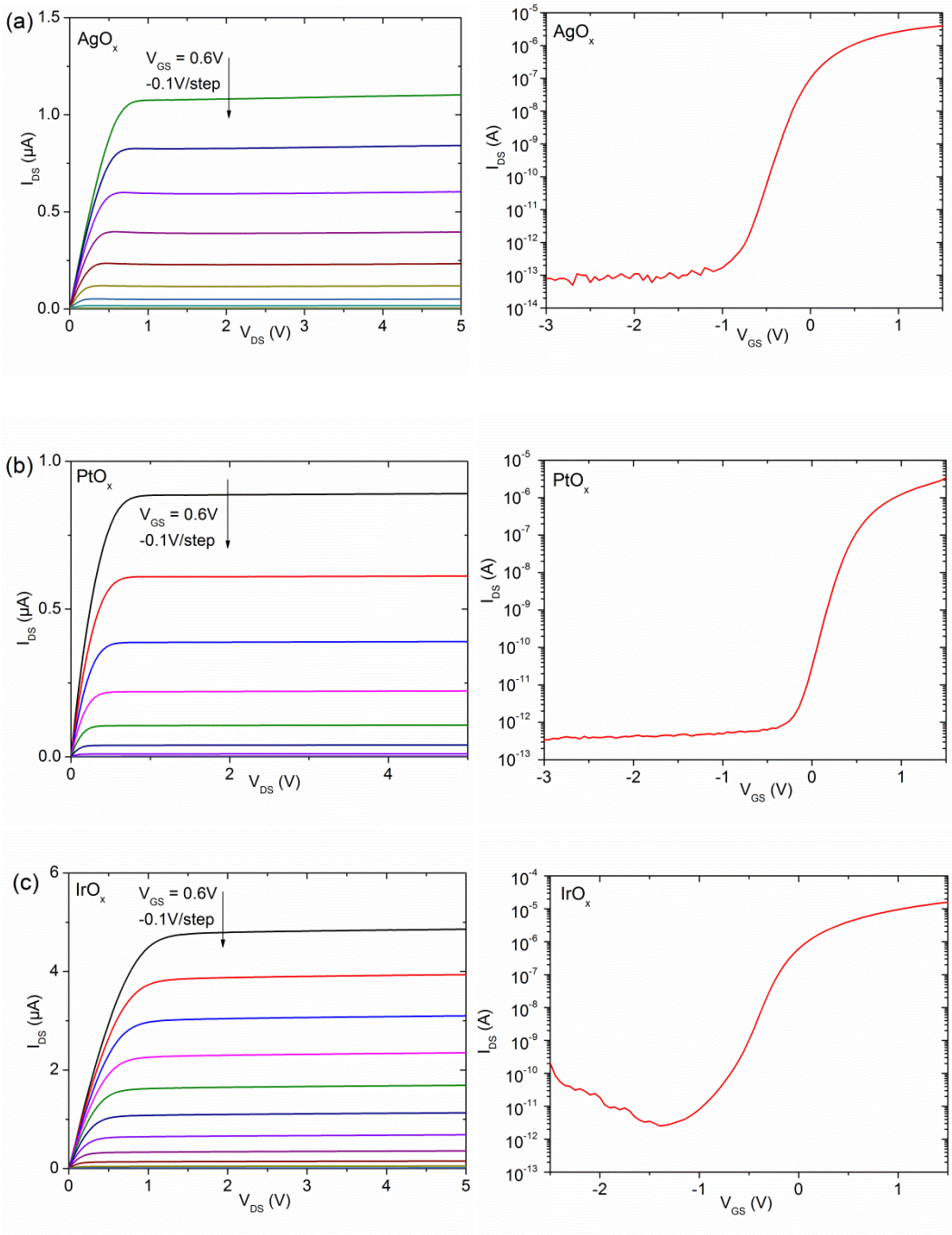

Figure 4.9 - MESFET output curves and corresponding transfer curves after the devices were aged for 1 year for a) silver oxide, b) platinum oxide and c) iridium oxide.

4.6 Co-sputtered and annealing

Devices fabricated on the co-sputtered films described in Section 3.4 have also been characterised. These devices have an AgO_x gate, with an active channel width of 100 µm and a gate length of 5 µm. The sample was initially tested after fabrication and then left exposed to air for 4 days, after which it was tested again. Upon completion of this testing, the substrate was annealed for 15 minutes at 120ºC in air, and characterised for the final time.

The devices were subjected to the same characterisation process mentioned previously in this chapter. From Figure 4.10, it can be seen that the initial 4 days of aging had a minimal effect on the Schottky contact, which is confirmed by the extracted figures of merit. The barrier height extracted from the initial measurement was 1.06 eV, compared to 1.10 eV for the 4 day aged device. The ideality factor showed a slight improvement, decreasing from 1.7 initially to 1.5 after aging. The series resistance showed a similar pattern, increasing from 11.0 kΩ to 12.7 kΩ. While this shows that the device is changing slowly with time, over 4 days there was a minimal impact. Annealing the devices however resulted in a remarkable decrease in forward current, as well as introducing a double barrier as seen in the forward bias region of Figure 4.10. The initial slope of the diode has an improved ideality factor of 1.3; however this increases to 3 at a forward bias of approximately 0.7 V. The barrier height also changes after this point from 1.12 eV to 0.82 eV. Additionally, there is also a reverse current hump, as observed in the previous section for the one year aged devices. This suggests that the annealing process produces similar effects to that of aging but on a much smaller time scale. The likely cause of both these changes is the reduction of carrier concentration of the IGZO material due to the absorption of

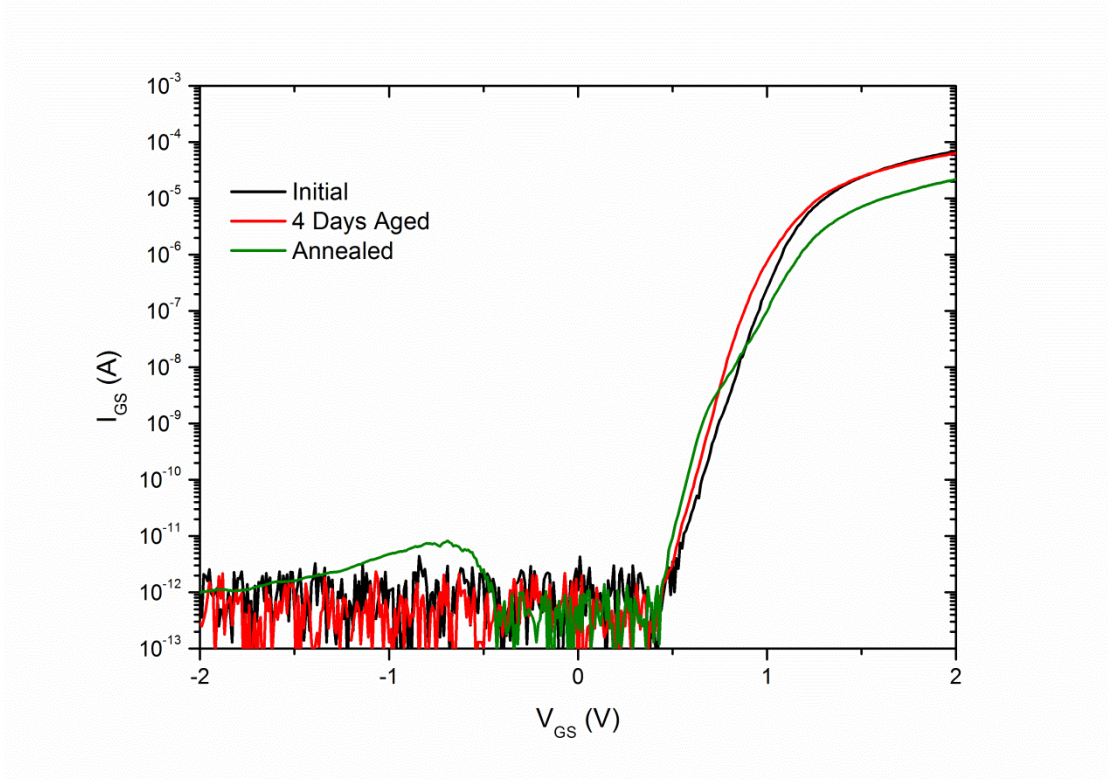

Figure 4.10 - IV comparison of a device after aging and annealing with dimensions W = 100 µm, L = 5 µm.

oxygen which fills oxygen vacancies within the channel.

Immediately after fabrication, as well as after aging, the devices showed a clear field effect but would not completely pinch-off. This is shown in Figure 4.11, where it can be seen that the transfer curves have a poor on-off ratio of 2 and 2.5 respectively. As before, the mobility and threshold voltages can be extracted. The threshold voltage after initial testing was -3.1 V, while after 4 day aging this decreased to -1.6 V. The extracted channel mobility was 11.7 cm^2/Vs, and with aging this increased to 14.9 cm^2/Vs. This was surprising, as all previous devices mentioned in this thesis had channel mobility's significantly lower than the measured Hall mobility, while this device has a channel mobility twice that of the Hall mobility of 5.5 cm^2/Vs. As the Hall mobility is measured on IGZO material with completely bare surfaces, it is likely that there is a surface layer lowering the overall mobility. As the calculated mobility

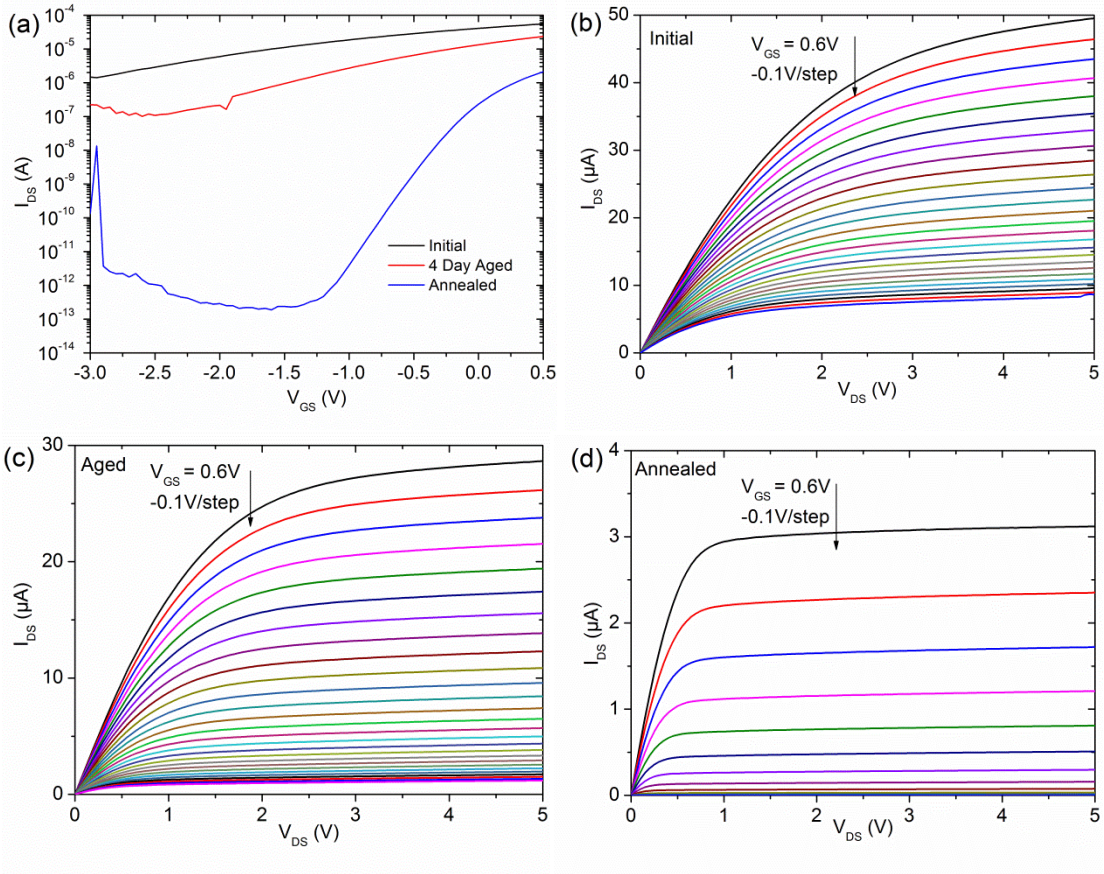

Figure 4.11 – a) Transfer curves depicting initial aging and annealing of the device, b) family of output curves for the initial device, c) the device after 4 days of aging, d) the device after annealing.

of this device is more than double that of earlier devices, it can be assumed that the additional Zn in the film resulted in fewer defects being formed during its growth.

After annealing, there is a remarkable improvement in the devices' transfer curve as shown in Figure 4.11. While there is a decrease in the on-current of one order of magnitude, the off-current has decreased to 200 pA. Consequently, this has increased the devices on/off ratio from 1 to 7.7 orders of magnitude. The extracted channel mobility was 11.7 cm^2/Vs, which is the same as the initial testing, and the threshold voltage is -0.21 V. Compared to the initial and 4 day aging tests, the output curves of the annealed device show much improved linear and saturation regions.

This is interesting because unlike devices reported elsewhere [46] which show

improved performance on films annealed up to 300 ºC, the devices here showed improved performance at annealing temperatures as low as 120 ºC. A likely candidate for this change is that annealing the films, even at relatively low temperatures of 120 ºC causes the films to absorb oxygen, which in turn decreases the number of oxygen vacancies in the film. As described in Chapter 2.2, oxygen vacancies are thought to be the dominant donor in IGZO, so a reduction in their concentration would cause a decrease in carrier concentration. This then increases the depletion region of the Schottky gates allowing the devices to be fully turned off.

CHAPTER 5

MESFET Stress Testing

As devices are operated, it is possible that their electrical performance can change over time. While undesirable, this is largely unavoidable. In order to minimise the impact of this change in performance, the amount and cause of this deviation must first be evaluated. In this chapter, two different methods of testing the stability of MESFETs were carried out: 1) gate bias stress testing and 2) constant voltage bias stress testing. The constant voltage bias stress stresses the device under normal operation, while the gate bias stress stresses the gate operation. All stress tests were performed on the same device, which has an AgO_x gate with dimensions of width 50 µm and length 10 µm, and in the order presented here with a week between each test.

5.1 Gate Bias Stress Testing

The gate bias stress testing is a test to determine how the gate 'holds up' over long periods of time when biased in a certain direction. In this test the gate-source and gate-drain are always biased in the same direction, resulting in a constant depletion width over the entire channel. Therefore, the MESFET is biased like two back to back Schottky diodes, with both biased in the same direction during the stress.

The gate bias stress tests were automated on the Hewlett Packard 4155B semiconductor parameter analyser using the program in appendix A. The test starts by

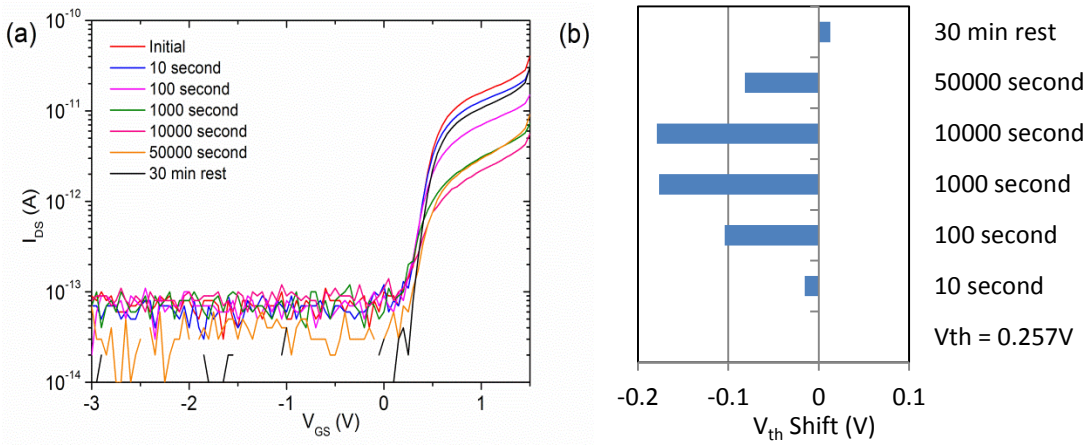

Figure 5.1 – Negative gate bias stress measurement results for a) transfer curves observed during stress measurements and b) threshold voltage shifts.

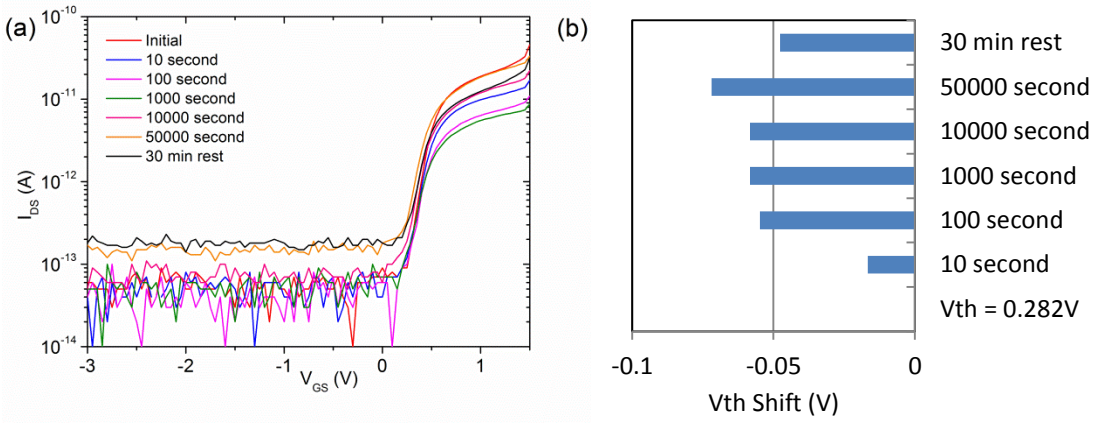

Figure 5.2 – Positive gate bias stress measurement results for a) transfer curves observed during stress measurements and b) threshold voltage shifts.

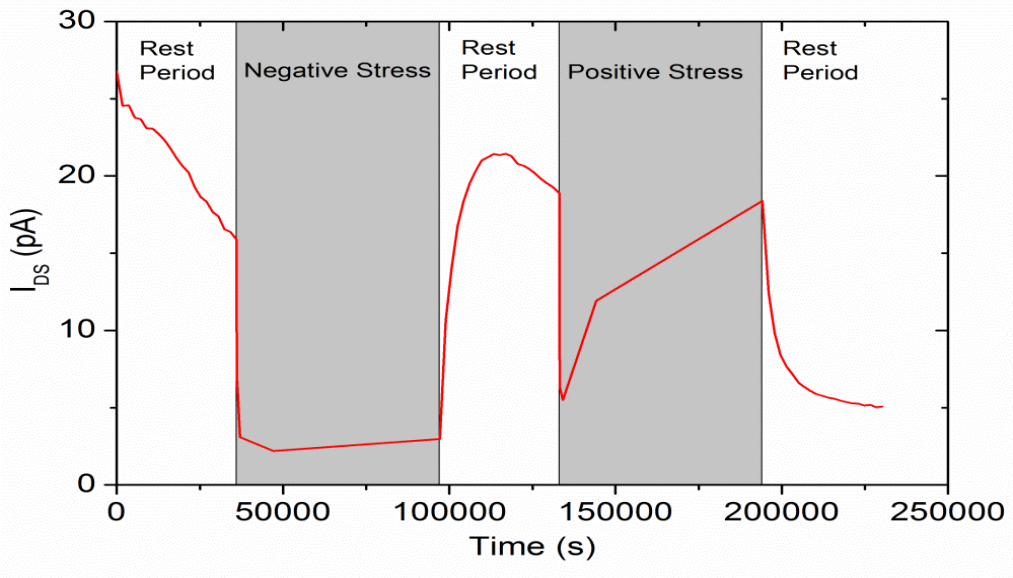

Figure 5.3 – On-current change over the course of the gate bias stress tests.

placing the device at rest in the dark with $V_G = V_D = V_S = 0$ V, while measuring the transfer curve of the device every 30 minutes for 10 hours. This initial rest period is used to verify that photoconductivity effects introduced during probe alignment are minimised during the main part of the stress test. Once this rest period is complete, the device is subjected to negative gate bias stress testing. The negative gate bias stress testing is set up with V_G = -1.5 V and V_{DS} = 0 V. The stress testing was performed for increasing periods of time, initially 10 seconds, then 100 seconds, 1000 seconds, 10000 seconds and finally 50000 seconds. After each stress test time period a transfer curve was measured, using V_{DS} = 2.5 V. No rest time was allowed between the stress time periods. Upon completion of the final stress test, the device was allowed to rest (under identical conditions as those at the start of the test) and (partially) recover from any shifts introduced by the previous stress test. The positive bias stress test was performed in the same way as the negative bias stress test except V_G = 1 V, followed by an identical rest period to check for recovery.

Over the 10 hour rest period, the drain-source current decreased by 33%, indicating that even the 5 μW/cm^2 of 625 nm light used to align the testing probes introduced a persistent photoconductivity (PPC) effect. There was a negligible threshold voltage shift during the period. The reference transfer curve used for the negative stress test was taken after the rest period. Figure 5.1(a) shows the transfer curves generated by the negative stress tests, while Figure 5.1(b) shows the threshold voltage shift. As the negative stress tests continued, there was a continuous negative shift in the threshold voltage up to 10,000 seconds at which the maximum shift was -0.17 V. After the 50,000 second test there was some indication of recovery, and 30 minutes after the stress tests ended the devices had fully recovered. During the rest period after the negative stress test, the on-current increased for 5 hours up to 87% of the initial

measurement, before slowly decreasing again down to 77% of the initial measurement.

The positive gate bias stress test also showed a tendency to introduce negative shifts in the threshold voltage. For the positive gate bias stress test however, each subsequent test showed an increasingly negative threshold voltage shift with a maximum shift of -0.07 V, shown in Figure 5.2. The positive stress test resulted in a slower threshold voltage recovery, taking 120 minutes to fully recover to the pre-stress state. The recovery period for the positive stress test showed decay in forward current as soon as the stress test ended, shown in Figure 5.3. This was the expected behaviour, however it is vastly different to that shown by the negative stress test recovery period. All measurements after the 10,000 second mark showed an increase in off-current by one order of magnitude. This increase in off-current was recovered once the device was left in the dark for one week.

5.2 Constant Voltage Bias Stress Testing

The constant voltage bias stress follows the same procedure as used in the previous section. That is, there was a 10 hour wait before the initial setup and after both the negative and positive bias stress tests. The difference occurs during the stress tests, where V_{DS} was set to 2.5 V, and V_G was set to either 1 V or -2.5 V depending on the stress test being performed.

5.2.1 Constant Voltage Bias Stress Testing in Dark

As with the gate bias stress test, the on-current initially decays over time during the initial rest period. This on-current decrease can be attributed to the recovery after light

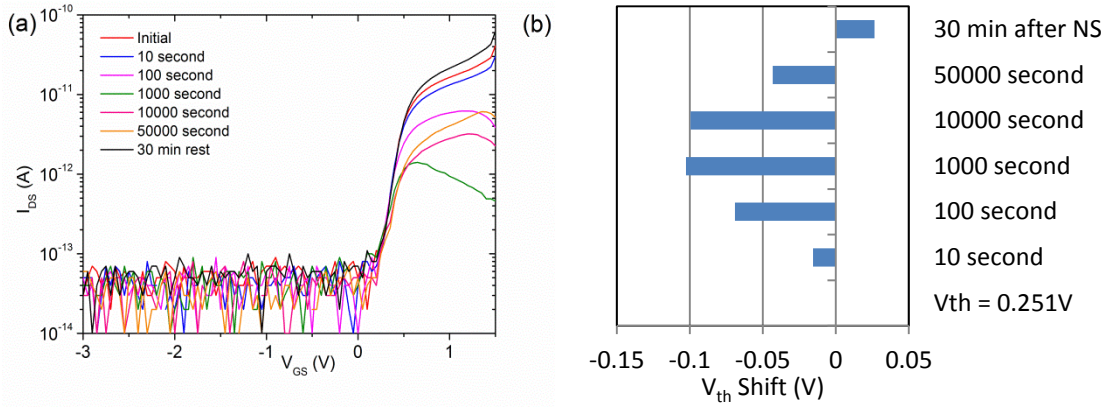

Figure 5.4 – Negative constant voltage bias stress measurement results for a) transfer curves observed during stress measurements and b) threshold voltage shifts.

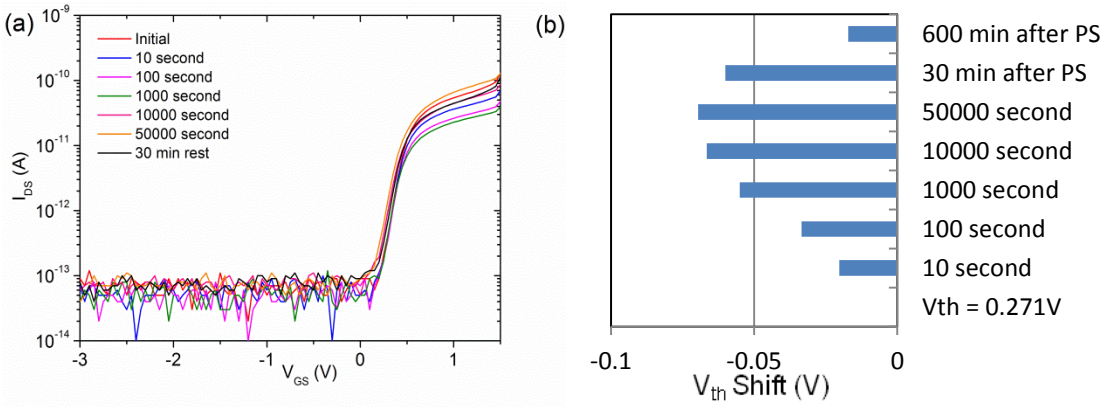

Figure 5.5 – Positive constant voltage bias stress measurement results for a) transfer curves observed during stress measurements and b) threshold voltage shifts.

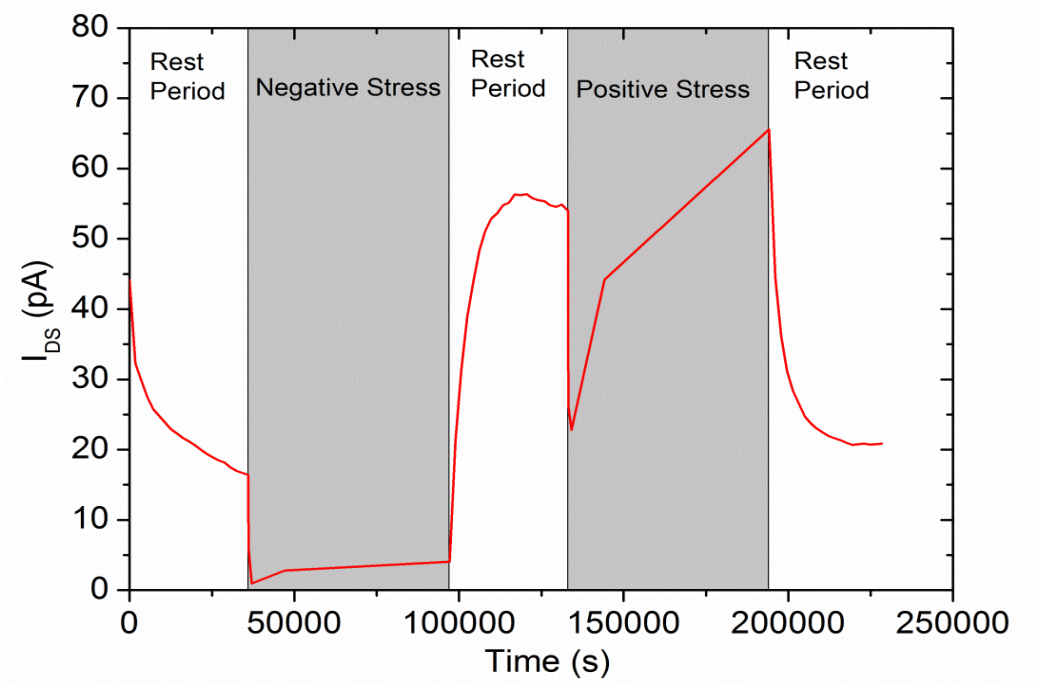

Figure 5.6 – On-current change over the course of the constant voltage bias stress tests.

exposure (during probe set up) which causes additional carrier generation as initially explained in Section 2.2 and further explored in Section 6.1. The negative stress test showed degradation in on-current up to 44% after the completion of the 1000 second test; however the 10,000 and 50,000 second stress tests showed some recovery, as shown in Figure 5.4. An important fact to note is that throughout these stress tests, the off-current remained constant, while only the on-current changed.

An increasingly negative threshold voltage shift was observed, with a maximum shift of -1 V after 1000 seconds. After this, the device showed signs of recovery towards the starting conditions, especially after the 50,000 second stress period. After 30 minutes of rest, the on-current and threshold voltage had not only fully recovered, but showed signs of improvement with a higher on-current and a small positive V_T shift.

The positive constant voltage bias stress test was performed 10 hours after the negative stress test, allowing the device to rest before the measurements were done. Figure 5.6 shows the on-current during this time, which was shown to increase exactly as during the gate bias stress, except that it took 6 hours to reach the maximum value as opposed to 5 hours. As with the gate bias stress, the initial stress tests caused a decrease in current up to the 1000 seconds of stress, after which each subsequent stress test showed a recovery in current. The threshold voltage shift for the positive constant voltage bias stress showed similar results to that of the positive gate bias stress, where the threshold voltage shift became progressively more negative, up to a maximum shift of -0.7 V. After 10 hours of rest, the devices had a threshold voltage within 4 mV of the initial threshold voltage used as the negative stress baseline, indicating that this may be a point of stability for the device.

5.2.2 Constant Voltage Bias Stress Testing under illumination

The same test as in Section 5.2.1 was repeated, but this time while the device was under illumination. Dark stress measurements are useful as a baseline comparison, however under normal operating conditions in display and optoelectronic applications, the devices will not be confined to dark conditions. Therefore, it is important to examine the differences between stress tests performed in the dark with those performed under illumination. For these measurements a blue light of wavelength 470 nm and intensity 250 μW/cm^2 was used as the illumination source. The hysteresis of the device was also examined throughout these stress measurements, with each measurement starting at V_{GS} = 1.5 V, sweeping to V_{GS} = -3 V and then returning to V_{GS} = 1.5 V, with no rest periods.

As with the measurements performed in the dark, these measurements commenced with a 10 hour rest period. However, as there was now constant illumination during this period, the on-current increase continuously, with an increase of 975% at the end of the 10 hour period. This effect is due to the ionisation of oxygen vacancies, and is explained in Section 2.2 and further investigated in Section 6.1. During the illuminated negative stress test, there was a sharp increase of 24% in on-current up to 10,000 seconds of stress, after which the on-current plateaued as shown in Figure 5.9. Throughout this time, there was no noticeable change in the off-current. Figure 5.7(b) shows that the threshold voltage shift during the illuminated negative stress was increasingly negative until 1,000 seconds of stress, as which point there was a maximum shift of -0.54 V. After this there was a slight recovery in threshold voltage

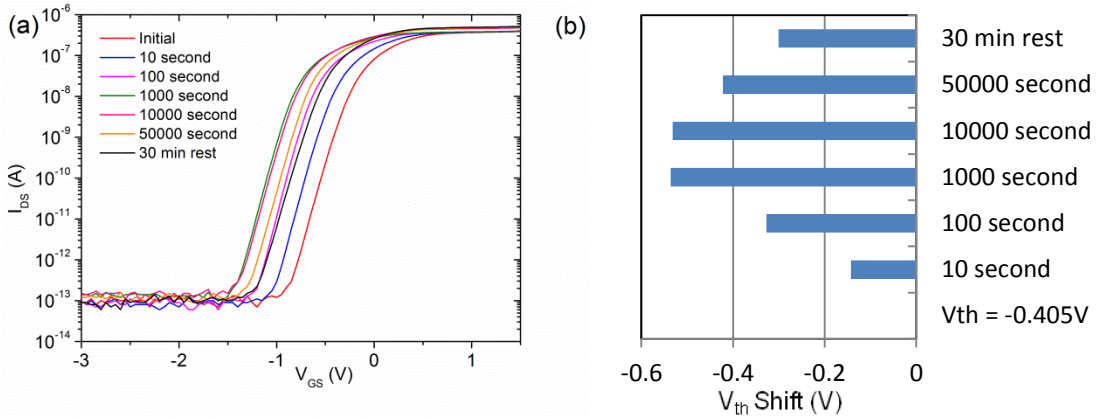

Figure 5.7 – Negative constant voltage bias stress while under 250 µW/cm^2 illumination from a 470 nm source measurement results for a) transfer curves observed during stress measurements and b) threshold voltage shifts.

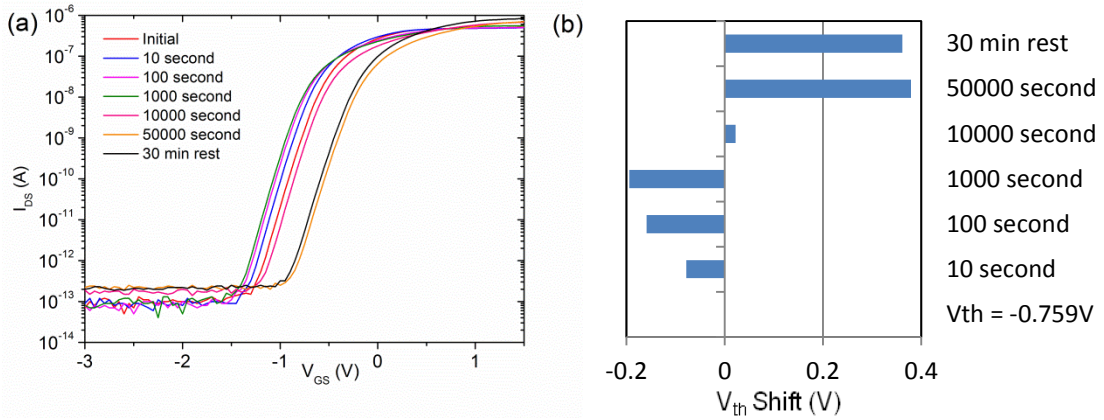

Figure 5.8 – Positive constant voltage bias stress while under 250 µW/cm^2 illumination from a 470 nm source measurement results for a) transfer curves observed during stress measurements and b) threshold voltage shifts.

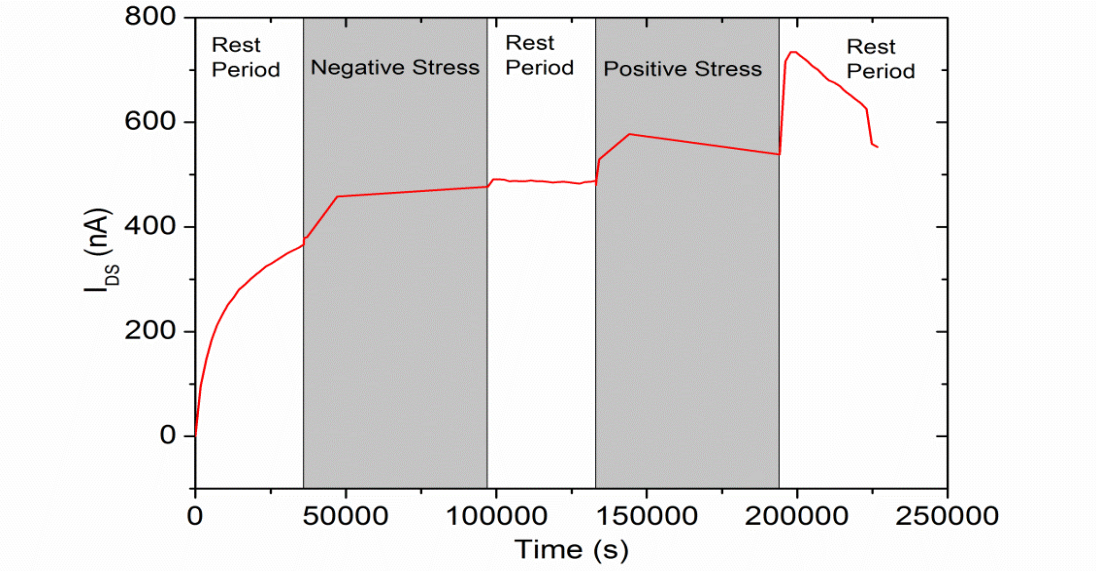

Figure 5.9 – Current change over the course of the constant voltage bias stress illumination tests.

for both the 10,000 and 50,000 second stress tests. During the 10 hour rest period (but still under illumination) following the completion of the negative stress tests, the devices were remarkably stable. There was a negligible change in both threshold voltage and on-current during the rest period.

The positive stress tests under illumination produced a significantly different trend compared to the same test performed in the dark. The threshold voltage under illumination shifted in the positive direction after 10,000 seconds of stress, reaching a maximum positive shift of almost 0.4 V after 50,000 seconds of positive stress. Before this, each stress test had shifted the threshold voltage in the negative direction up to -0.17 V as shown by Figure 5.8(b). Possible reasons for this are examined in Section 5.3. After an extended 750 minute rest period, there was a partial recovery in the positive threshold voltage shift to 0.19 V.

Throughout the positive stress test under illumination, there was a slight decrease in the on-current as shown by Figure 5.9. However, as soon as the positive stress test was concluded, there was a sharp increase in the on-current followed by a slow linear decay. This is a significant deviation from the exponential decay seen after the positive stress test in dark conditions.

Hysteresis effects were also investigated during the illumination stress tests. There are two types of hysteresis that can be explored, gate-voltage hysteresis and drain-current hysteresis. Gate-voltage hysteresis is the difference in gate voltage at a constant drain current, while drain-current hysteresis is the difference in current at a constant gate voltage. As the measurements were completed by varying the gate voltage at constant steps, drain-current hysteresis is the most obvious choice. For

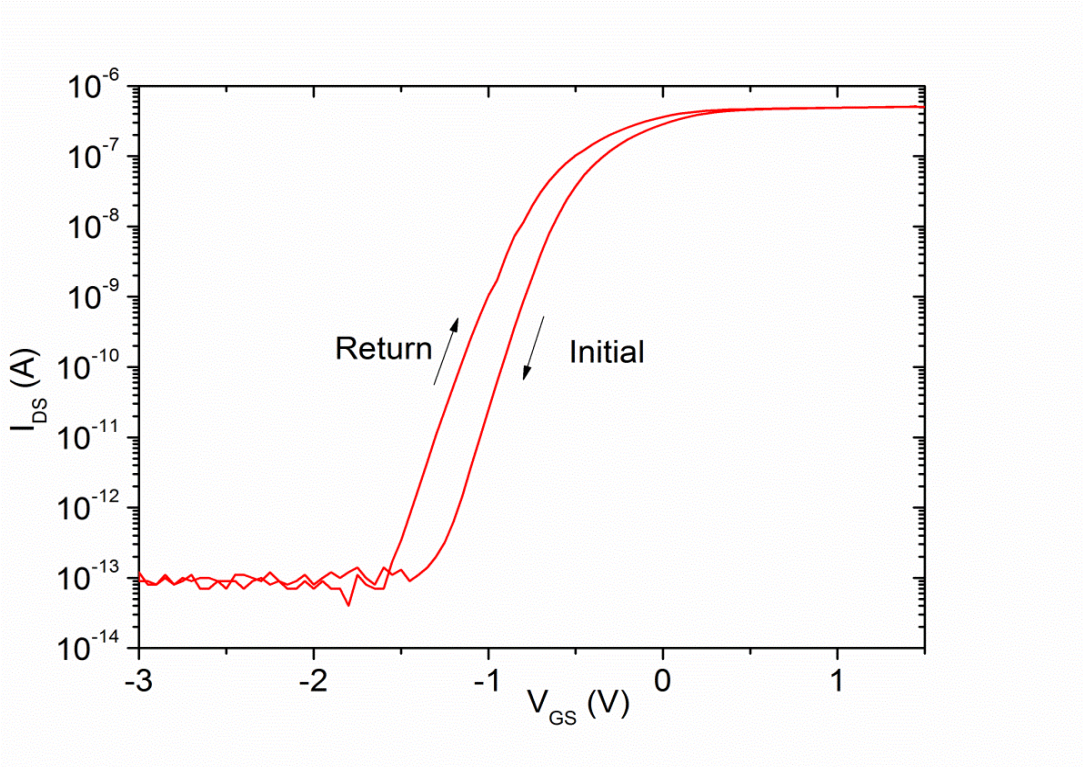

Figure 5.10 – Typical example of hysteresis during an illuminated constant voltage bias stress test.

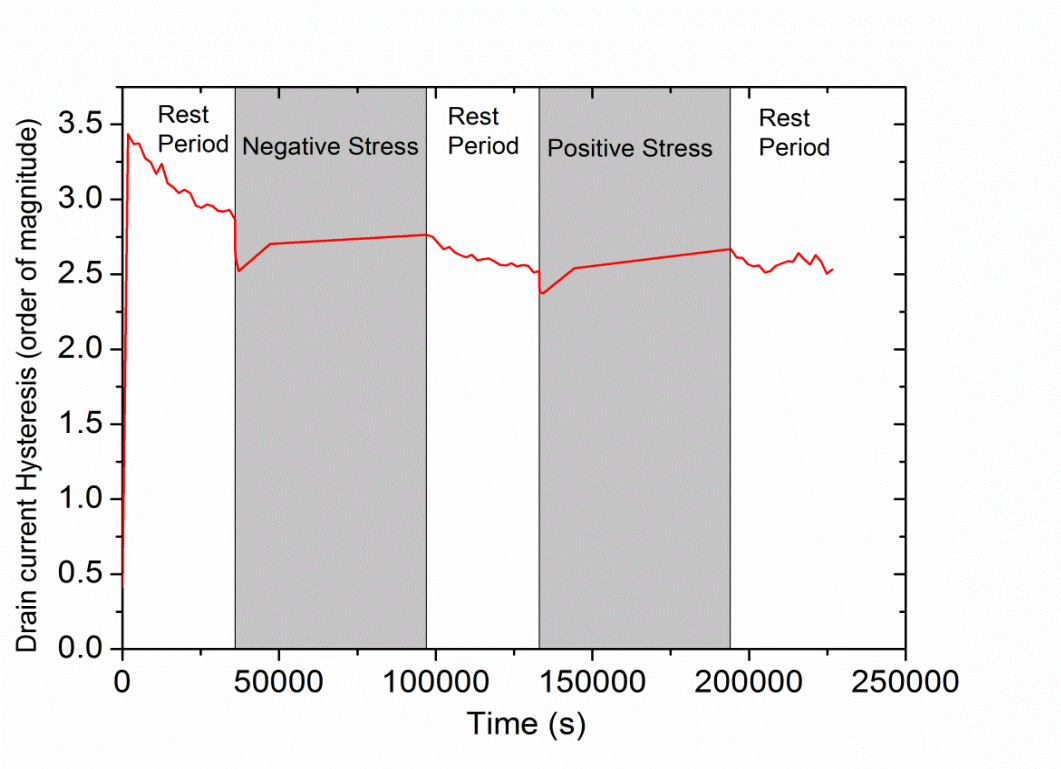

Figure 5.11 – Maximum drain current hysteresis over time.

every stress measurement, drain-current hysteresis was found to occur in a clockwise direction as shown in Figure 5.10; i.e. the return current is to the left of the initial sweep. The hysteresis is typically a measure of trapping within the gate interface and channel [50]. As the gate voltage is swept in the negative direction, the electron trap density decreases, which in turn causes the threshold voltage to shift negatively. Conversely, as the gate voltage is swept in the positive direction, the electron trap density increases, causing a positive shift in the threshold voltage [51].

Initially, there was very little hysteresis before the illumination source was turned on, as shown in a plot of the maximum drain-current hysteresis for each measurement verses time in Figure 5.11. Once under illumination, hysteresis increased significantly, followed by a slow decay with time. During the rest periods between stress tests, the hysteresis decreased slightly. For both the positive and negative illumination stress tests, the hysteresis effect increased slightly. This suggests that when there is a gate voltage applied before each measurement, the electron trap density is more sensitive to the gate voltage applied during the transfer measurements.

5.3 Possible Causes of Stress shifts

In a typical MESFET, the standard trapping issues that cause threshold voltage shifts such as those observed in this thesis are: charge trapping at the gate/semiconductor interface and trapping in the channel. Both trapping locations generally follow the same mechanisms, and for the remainder of this discussion channel trapping is considered.

As there was no significant change in the subthreshold swing (S) of the device throughout the stress measurements, the shift in threshold voltage can be attributed to simple hole trapping within the channel and channel/gate interface. It has been

suggested that oxygen vacancies (V_0) in the channel can act as hole traps, and have the ability to diffuse at room temperature [24]. As these V_0 diffuse to the channel/gate interface, there is a reduction in the built-in potential voltage. This in turn causes a reduction in the threshold voltage resulting in a negative shift. The slight increase in off-current observed in several of the positive bias stress tests can also be explained by oxygen vacancies [52]. Typically, an increase in off-current is attributed to an increase in either bulk-states or conduction band tail states. However, this should cause a positive shift in the threshold voltage, which was not observed in these experiments. Therefore, the increase in off-current must instead be associated with a lower channel resistivity caused by induced V_0 [52].

The positive shift of the threshold voltage observed during the positive bias illumination stress tests must have a different cause from that responsible for the negative threshold voltage shifts. It has been shown that significant threshold voltage shifts can occur depending on the pressure and oxygen concentration present during device measurements [53]. This is consistent with another theory suggesting that in an electric field, oxide semiconductors have the ability to absorb and desorb oxygen from their exposed surfaces [54] [55]. As V_{GS} is positive during the positive stress tests, the electron density within the channel increases, resulting in an increase in the absorbed surface oxygen concentration [54]. This in turn results in a positive shift in the threshold voltage. As the device tested was not passivated with any surface coating, this could explain the positive threshold voltage shift.

CHAPTER 6

PPC and Passivation

6.1 Persistent Photoconductivity

All devices fabricated on IGZO films showed an increased on-current and negative voltage shift when exposed to light. This chapter attempts to characterise the magnitude of this effect, and also explores the effectiveness of potential recovery methods. Finally, three passivation layers, silicon nitride (Si_3N_4), silicon dioxide (SiO_2), and hafnium oxide (HfO_2) were applied to the devices in an attempt to prevent or mitigate the persistent photoconductivity (PPC) effect.

6.1.1 Persistent Photoconductivity Effect

As mentioned in section 2.2, it has been suggested that the main cause of the photocurrent effect in IGOZ is the ionisation of oxygen vacancies (V_0). Ionised V_0 have a lower formation energy than neutral V_0. Consequently the ionisation is maintained after the illumination source is removed, causing a persistent photoconductivity (PPC) effect. This effect was investigated by shining a quartz halogen lamp with a spectrum shown in Figure 6.1 at an intensity of 20 mW/cm^2 onto a device with no surface passivation layer.

Figure 6.2 shows the current I_D of a MESFET device with a width to length ratio of 5. At t = 500 seconds, the illumination source was turned on for one hour, after which

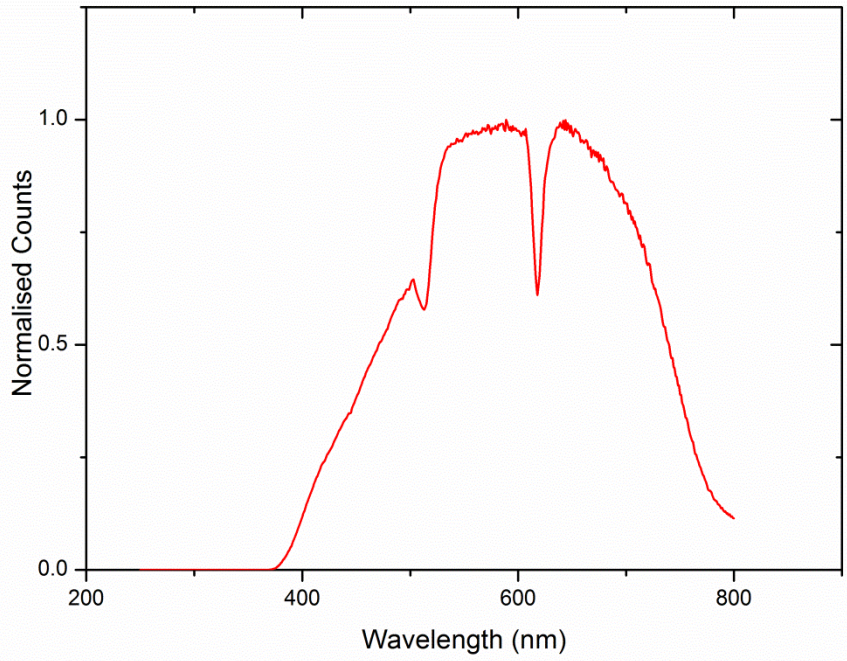

Figure 6.1 – Spectrum of the quartz lamp used as illumination source for PPC measurements with optical power density 20 mW/cm^2.

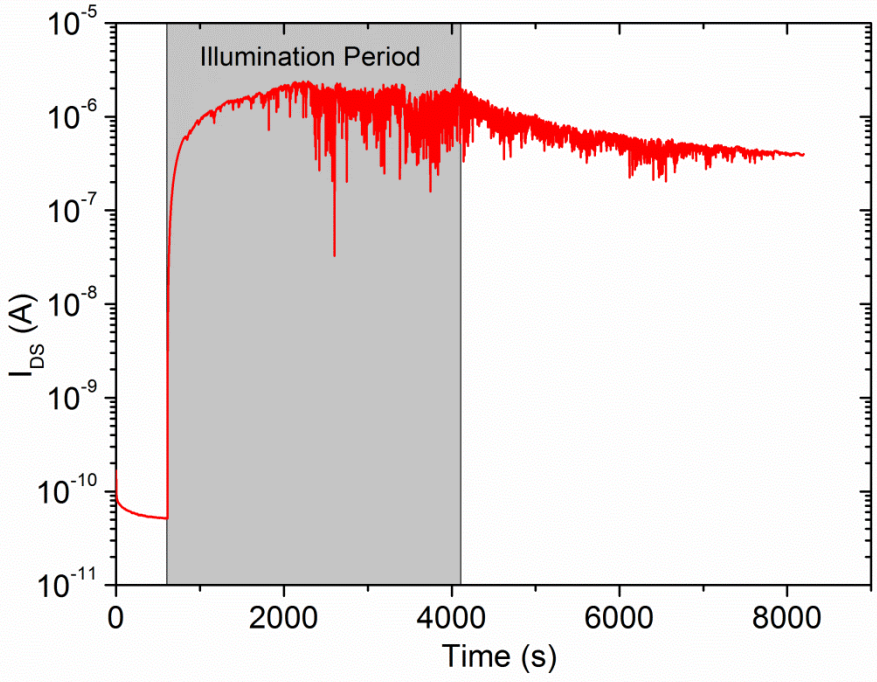

Figure 6.2 – Current response of a device exposed to 20 mW/cm^2 of illumination.

the illumination was removed and the device was allowed to relax towards its initial state. The device has a relatively fast illumination response, increasing its on-current by 4 orders of magnitude in 200 seconds. The on-current reached a peak value of 2.5 μA after 2100 seconds, at which point the noise in the measurement began to increase with no further increase in on-current. The device had an extremely slow relaxation time, i.e. after 4,000 seconds the current had only decreased by 0.8 orders of magnitude.

It has been suggested that a stretched exponential can be used to evaluate the photoresponse of amorphous systems [56] [57]. Such a response follows the form of:

$$I_D(t) = I_{D0} e^{-(t/\tau)^{\beta}} \tag{6.1}$$

where I_{D0} is the current at the instant the illumination source was removed, τ is the effective time constant, and β is the stretching exponent. A least mean square fit for the response in Figure 6.2 gives τ = 432 s and β = 0.36, which corresponds to days for the device to recover to its original dark state. This is consistent with the experimentally observed time frame required for the full recovery of the device. The advantage of using this method is that the fit is valid up to month-long time scales in amorphous systems, and thus the on-current due to photoresponses can be extrapolated by at least an order of magnitude [57].

This extended recovery time is not ideal, and makes the device performance very sensitive to the amount of light that it has been exposed to. Therefore, a method is needed to reduce the sensitivity of devices to illumination such as the use of surface passivation coatings or an electronic technique to speed up recovery.

6.1.2 Attempted recovery test

As the recovery time of these devices can be in excess of several days, an accelerated recovery method is highly desirable. In this section, such a method is attempted. It was suggested by Jeon [58] that for oxide semiconductors suffering from PPC it should be possible to accelerate recovery. This would be done by applying a positive gate voltage which should induce electrons into the channel thus accelerating the recombination of electrons with ionized oxygen vacancy sites. By this reasoning, a negative bias would deplete the channel and reduce the recombination rate, thus extending the recovery time. This theory was tested, with the results shown in Figure 6.3.

The recovery test began with a device with a width-length ratio of 1 set up in the dark with I_D measured with a constant gate voltage of -1.5 V. This voltage was chosen as it is approximately half way between the on and off regions of the device as shown in Figure 6.4. The device was then exposed to 100 seconds of light from a 20 mW/cm^2 quartz-halogen light source, which caused a significant change in the output current. After illumination, the device was then left to rest for 400 seconds before being exposed to another 100 seconds of light illumination. This was done to show the fast charge and slow recovery rate of the exposed device. The device was then pulsed with -3 V gate voltage for 100 seconds, which if the theory was correct should cause a reduction in the rate of recovery. The first negative pulse induced an increased recovery rate of the current by 1 order of magnitude; however the second pulse showed no significant effect. The device was then re-exposed to light from the same source to return the current to the same starting point for the negative bias test. Once

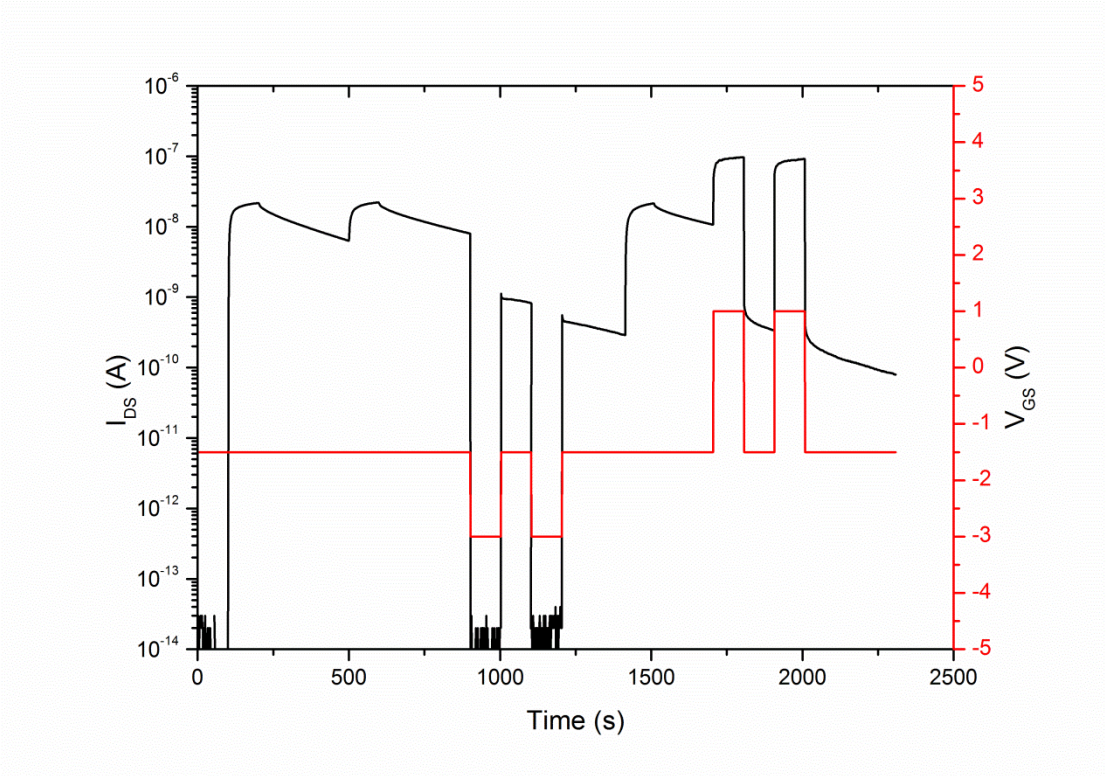

Figure 6.3 – Drain-source current response of a device exposed to a 20 mW/cm^2 illumination source, where a gate pulse is used to attempt recovery.

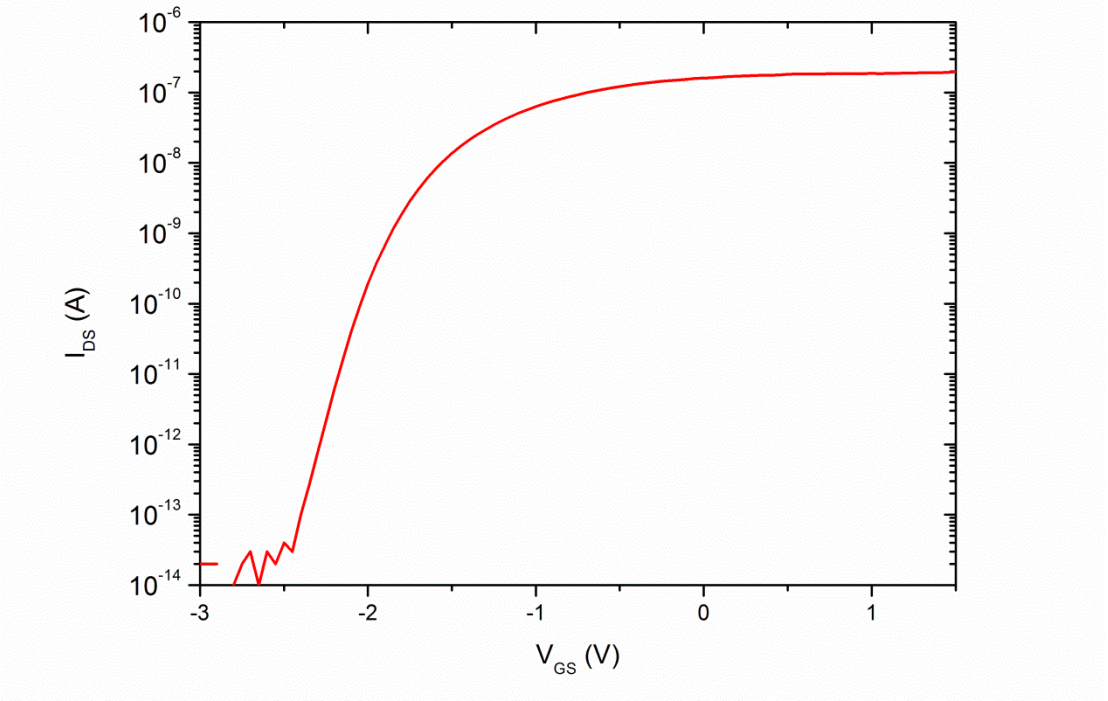

Figure 6.4 – Transfer curve of the device used for the recovery test.

again, the first pulse showed an increased recovery of the output current by 1.5 orders of magnitude while the second pulse produced no significant further change.

In comparison to the results of similar experiments [58] [59] which showed no effect when a negative gate bias pulse was applied, the results here disagree with the theory that a negative pulse slows recombination. These results however do agree that a positive gate bias pulse can be used to speed up recovery, even if by a smaller margin than those reported elsewhere, for which even a short 1 µs pulse reset the current to that of the dark state [59]. This suggests that the recovery period of the on-current induced via PPC has two recovery rates, the first which can be increased by applying a positive gate voltage pulse, and a second recovery rate which is considerably slower and is unaffected by the use of gate voltage pulses.

6.2 Passivation Layers

The passivation layers used in this experiment were SiO_2, Si_3N_4, and HfO_2. The MESFET devices before passivation were all fabricated from adjacent sections of the same IGZO on PEN film. The devices were then passivated and tested under illumination to determine the effectiveness of each passivation layer.

6.2.1 Device fabrication

Four sets of devices were fabricated simultaneously, three were coated with the different passivation layers and one was used as a reference spare. As it turned out, this spare had to be used as a replacement HfO_2 passivated device, as due to difficulties in the etch patterning of HfO_2. The HfO_2 was deposited using RF sputtering from an HfO_2 target in a pure argon atmosphere at a power of 180 W. The deposition time was 70 minutes to deposit 100 nm. Initial attempts to etch the

passivation layer using dry etchants CHF_3 and SF_6 proved unsuccessful, as were typical wet etchants such as 33% HCl. HF proved a successful etchant, however the contact pads did not survive the process. The mask was redesigned to allow a lift-off process to be used with HfO_2 which produced comparable results to that of etched Si_3N_4 and SiO_2. Both the Si_3N_4 and SiO_2 layers were deposited in pure Ar at an RF sputtering power of 150 W, to a thickness of 120 nm. Both were etched successfully using CHF_3 gas as a dry etchant. The mask design for the passivation layers is such that the entire substrate is covered with each passivation layer and only a small region within each contact pad is exposed. Therefore, the entire device is under the passivation layer with only a small portion of the gold capped contact pads exposed, effectively sealing the device from atmosphere exposure.

6.2.2 Passivation comparison

Before each passivation layer was deposited, the devices were characterised to determine their initial characteristics. This involved measuring MESFET characteristics under exposure from different single wavelength LEDs at set intensities. By using single wavelength LEDs instead of a full spectrum lamp such as used earlier, it was possible to investigate any wavelength dependence in the PPC effect and its subsequent passivation. Each measurement was performed by exposing the device to 50 seconds of illumination, after which the devices' transfer curve was measured with the illumination still present. Once the measurement was complete, the illumination source was removed and the device was allowed to relax for 500 seconds, with a transfer measurement taken at 50 second intervals.

The before and after passivation transfer curves for all three passivation layers can be seen in Figure 6.5. The before passivation responses for all three sets of devices

were remarkably similar, which was to be expected as their fabrication was identical. Figure 6.5(a) shows that there is very little threshold shift and on-current increase when exposed to wavelengths of 625 nm and 610 nm at an intensity of 250 μW/cm^2. There are however significant changes when exposed to wavelengths of 505 nm and 470 nm at the same intensity. These wavelengths correspond to photon energies above 2.3 eV, which has been linked to the energy required to ionise oxygen vacancies [60]. It is worth noting that there are no significant differences between the 470 nm wavelength response at 250 μW/cm^2 and 500 μW/cm^2. Both illumination intensities increase the magnitude of the on-current and negative threshold voltage shift by approximately the same amount. Therefore, it is likely that illumination wavelength plays a more important role than intensity in the photocurrent response. When exposed to the broad spectrum lamp at an intensity of 20 mW/cm^2 all devices showed a dramatic increase in off-current, making the devices inoperable. Remarkably, after only 50 seconds of relaxation, the off-current of the devices had returned to their dark state, while the large negative threshold voltage shift was still present.

It is interesting to note that each set of devices had a different response depending on the passivation layer applied to it. First, it can be seen that the Si_3N_4 passivation layer had little effect on the illumination induced effects on the device transfer curve. Therefore, it can be concluded that Si_3N_4 is not an appropriate passivation layer for the prevention of PPC effects. Similarly, the devices passivated using HfO_2 showed little effect with the shorter wavelength illumination sources. There was however a dramatic decrease in dark on-current to the point where the device is an insulator, followed by a smaller increase in on-current when exposed to light of wavelengths 625 nm and 610 nm. The devices passivated using SiO_2 showed a significant change

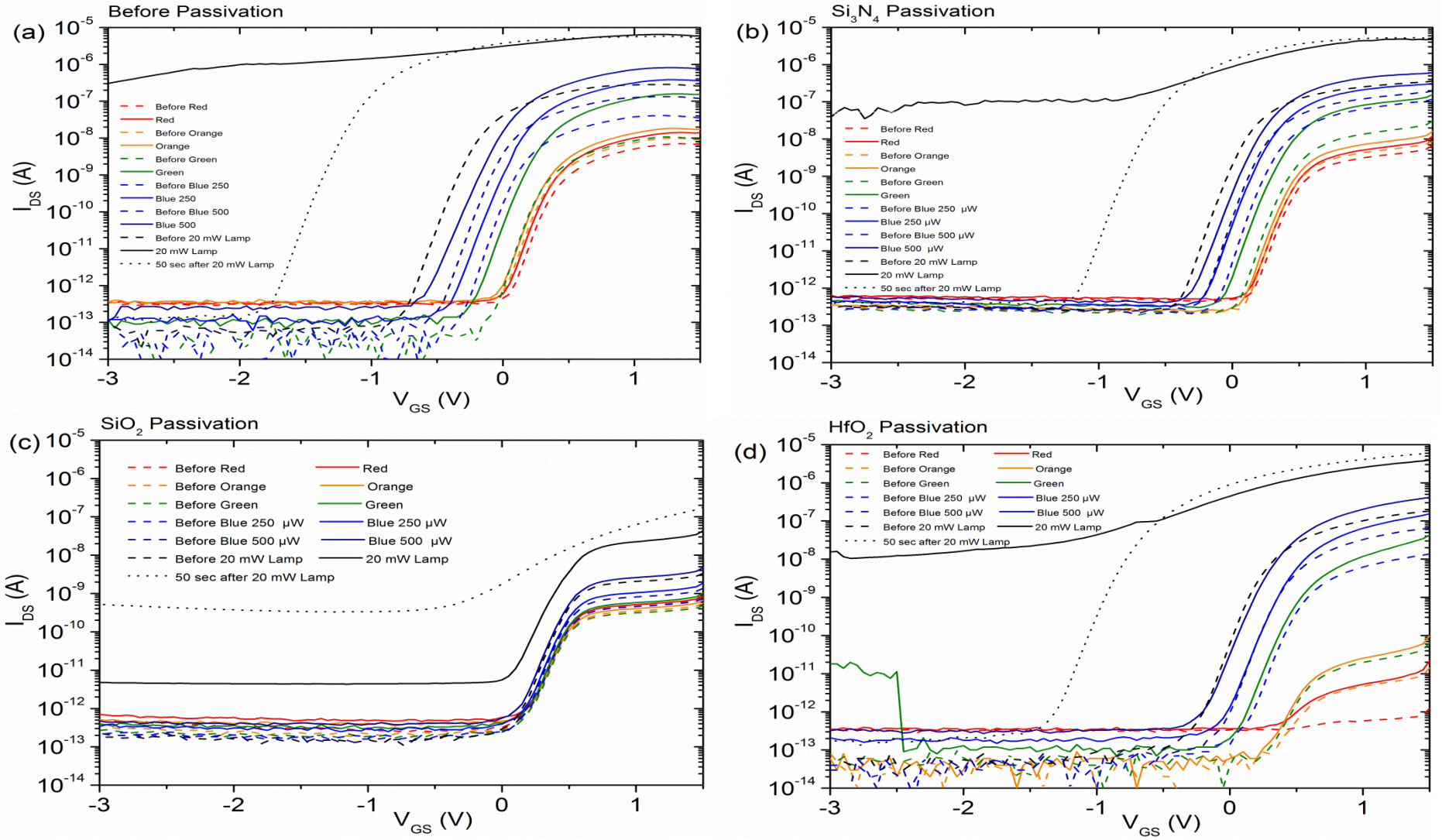

Figure 6.5 – Transfer curves depicting the change due to light for a) no passivation, b) Si_3N_4 passivation, c) SiO_2 passivation, and d) HfO_2 passivation.

in their photoconductivity. There is a slight decrease in on-current in the initial measurements, followed by a significant decrease in induced photocurrent for all wavelengths from 625 nm to 470 nm. There is even a significant reduction in the photocurrent generated when exposed to the illumination from the 20 mW/cm^2 quartz-halogen lamp. After this exposure however, the off-current increased by 3 orders of magnitude compared to the LED illumination. Another anomaly displayed by the SiO_2 passivation was that following the 20 mW/cm^2 illumination, the device did not recover in the same manner as the other passivated devices. The off-current increased dramatically, while the on-off ratio decreased to less than 2 orders of magnitude.

There are two possible explanations for the significant deviation from the original behaviour after passivation for the SiO_2 covered devices. The first possibility is that the passivation blocks a portion of the undesirable wavelengths from reaching the channel. However, as the passivation layer is visibly transparent with a similar transmission to that of Si_3N_4 (refer to Section 7.2 for transmission results) this is an unlikely scenario. The second possibility is that as the passivation layer was being deposited, some of the oxygen from the SiO_2 was transferred to the IGZO, filling some of the oxygen vacancies in the IGZO channel. Without oxygen vacancies to ionise, there is a significant reduction in on-current and threshold voltage shift. The problems with this explanation are that i) the same results would be expected from the HfO_2 passivation if this was the case, and ii) the HfO_2 passivation only showed a decrease in on-current for illuminations below the oxygen ionisation threshold. Also, if the IGZO was absorbing oxygen at such a rate, it would be expected that there would be a similar reduction during the deposition of the AgO_x Schottky contact, which uses an oxygen environment to oxidise the Schottky metal.

It is worth noting that devices coated with all three passivation layers showed little to no further change in their characteristics with time. In comparison with devices that were not passivated, this is a significant improvement. Typically for all devices fabricated in this study that were not passivated, there was a significant decrease in on-current when the device was left exposed to atmosphere even after only a few days. This was attributed to absorption of oxygen filling oxygen vacancies in the IGZO material, thus reducing its carrier concentration. As all passivated devices had a physical barrier in place preventing this absorption, it can be expected that there was a significant reduction in this effect with time.

CHAPTER 7

Transparent Flexible MESFETs

In this section, fully transparent devices are fabricated on a flexible polyethylene naphthalate (PEN) substrate. To determine how transparent these devices could be made, the transmission spectra of each individual layer used in the fabrication was characterised. As the devices were fabricated on a flexible PEN substrate, the devices were subject to a series of bending tests to determine how well they could withstand mechanical strain.

7.1 Transmission

The transmission spectra of different films used in the production of transparent MESFETs on PEN substrates were measured and then compared. The films were all grown at the same time to eliminate any variation in fabrication process between film growths. The transmission spectra were measured using a Cary 6000i spectrophotometer. In each case, the baseline used was air, so all transmission measurements are absolute transmission values in air. Transmission measurements were made across the entire visible spectrum starting at 800 nm down to 200 nm. At 350 nm the illumination source was automatically changed, but there was no significant data below 370 nm.

Figure 7.1 shows the transmission measurements of single materials grown on PEN substrates. The PEN itself has a transmission of approximately 86% across

the entire visible spectrum (400 nm to 700 nm), and has a sharp absorption point at 380 nm. Below this point the transmission drops to 0.5%, and light can be considered to be fully absorbed. Unfortunately this also prevents and optical band gaps to be obtained from the transmission spectra, as the materials all had larger band gaps than the substrate and were subsequently obscured. When IGZO, grown using the standard 100 W recipe described in Section 3.3, was deposited on the PEN substrate the average absolute transmission over the visible region decreased to 83% which is comparable to the 95% relative transmission of IGZO grown elsewhere [61]. The passivation layers used chapter 6 were also compared. It is apparent that there was some measurement error, as the Si_3N_4 and SiO_2 films both have regions that have higher transmission that that of blank PEN. Both films have an average transmission of 86%. HfO_2 was slightly less transparent, averaging 81% over the visible region. The ITO film grown for this experiment was significantly less transparent compared to those fabricated in industry, which can have an average transparency of up to 95% [62]. This led to the conclusion that our ITO film growth was not optimized; however for this purpose the electrical properties were adequate.

There was little difference optically between MESFET devices with gates 10 nm thick and those 30 nm thick, shown in Figure 7.2, and an electrical comparison can be found in Section 7.2. The 10nm film has an average transmission of 70%, while the 30 nm thick film has an average transmission of 65%. The 30 nm film has a much lower transmission in the UV region, and begins to decrease before the absorption cut-off of the PEN substrate. The 10nm film has the same trend, however it appears later.

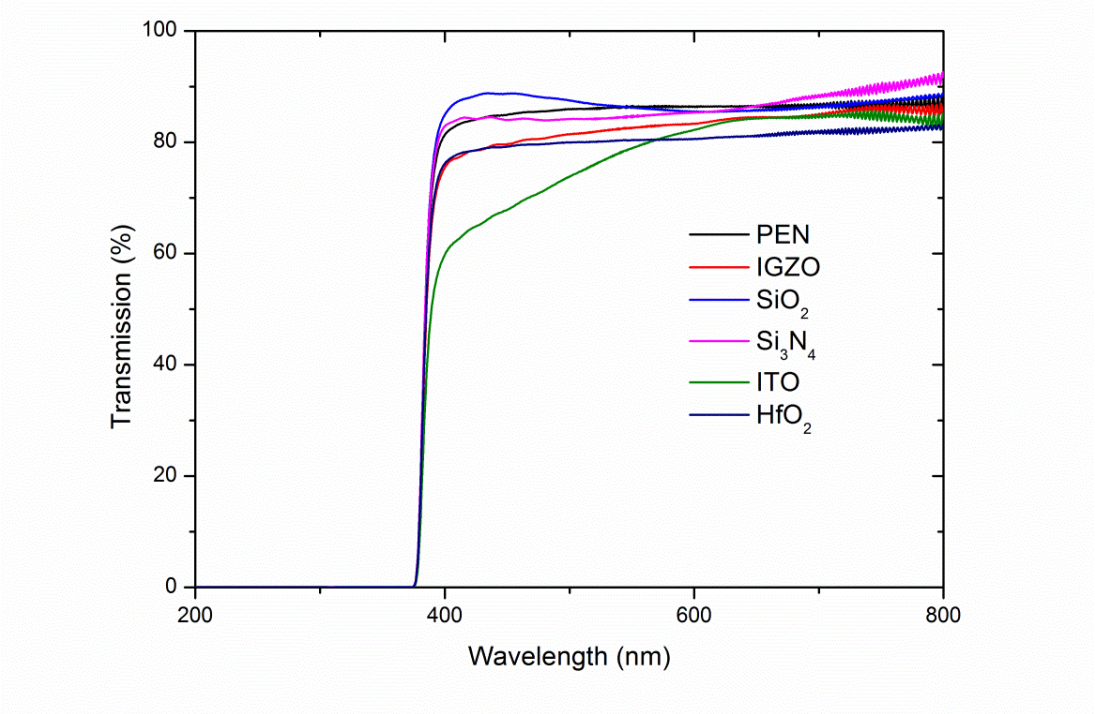

Figure 7.1 - Transmission spectra of various films grown on a PEN substrate.

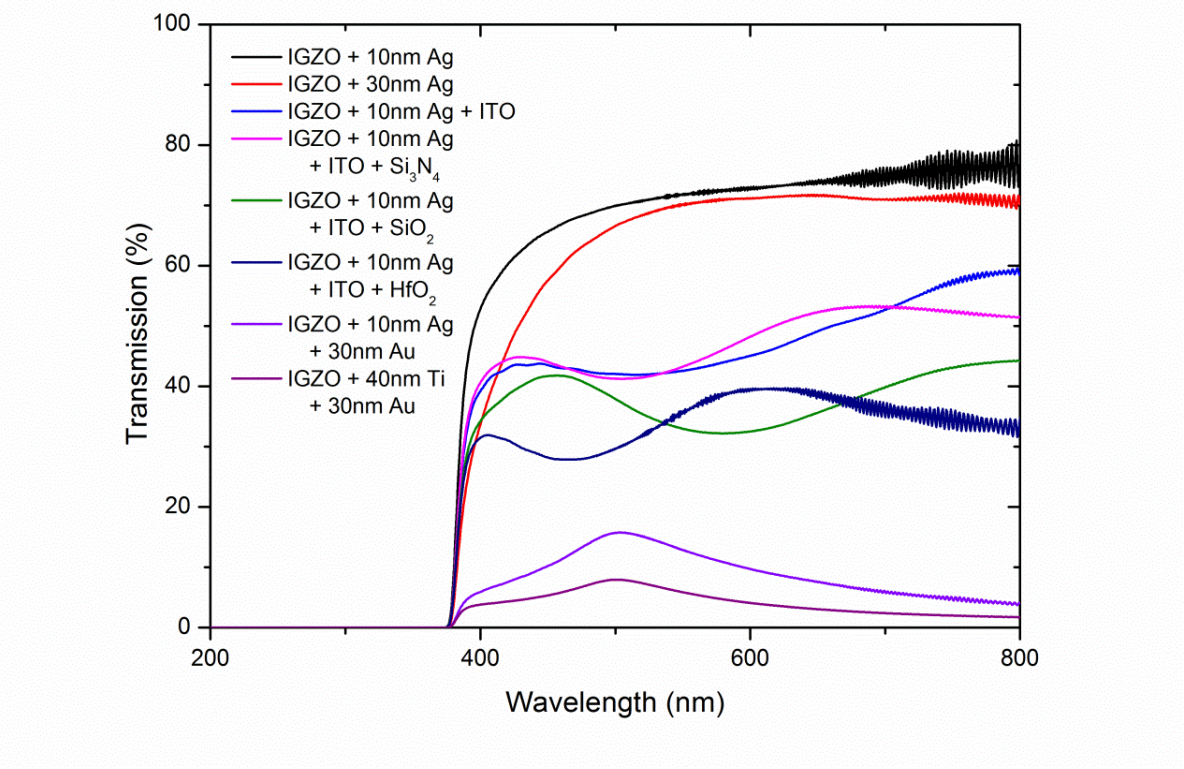

Figure 7.2 - Comparison between films fabricated on different thicknesses of silver. All films used a PEN substrate that fully absorbs all wavelengths below 380nm.

100 nm thick ITO, along with the three passivation layers which ranged between 100-120 nm each, were also deposited onto the 10 nm thick Ag film to determine how the materials interacted. It can be seen that the Si_3N_4 has a minimal difference from the ITO film without a passivation layer. However the SiO_2, which had similar transmittance to the Si_3N_4 when grown on PEN, showed a significant drop in transmittance. Is it therefore possible that there was some interaction between the ITO film with the SiO_2 grown on top. Interestingly, the HfO_2 film showed a similar response to the SiO_2 film, even though it had a lower transmission when grown on a blank PEN substrate. In comparison to the typical metal contacts of Ti and Au, it can be seen that even this non-optimised ITO film has significant advantages in terms of transmission and is highly suitable for in use in transparent devices

7.2 Transparent Devices

In an effort to increase the transparency of these MESFET devices, the thickness of the AgO_x Schottky gate was reduced from 30 nm to 10 nm. It was shown in Section 7.1 that this produces an improvement in the optical properties of the devices; however this is only useful if the electrical properties are not degraded by the reduction in gate thickness. The Ti/Au bilayer ohmic contacts also had to be replaced as they were not transparent. Therefore, a replacement was found in the form of ITO. ITO was used as a replacement for the Ti/Au ohmic contacts and also as a replacement for the Au capping layer on the Schottky contacts. An image of the fabricated devices is shown in Figure 7.3. In this section, the electrical properties of MESFETs fabricated with each of these AgO_x Schottky gate thicknesses are compared.

Sample	Series Resistance (Ω)	Ideality Factor	Barrier Height (eV)	Threshold Voltage (V)	Channel Mobility (cm^2/Vs)	Subthreshold Swing (mV/dec)
10nm AgO_x + ITO	315K	1.1	0.95	-0.60	1.65	134
30nm AgO_x + ITO	487K	1.3	0.99	-1.15	1.23	162
30nm AgO_x + Ti/Au	180K	1.1	1.07	-0.22	3.1	120

Table 7.1 - Comparison between devices fabricated using different contact thicknesses.

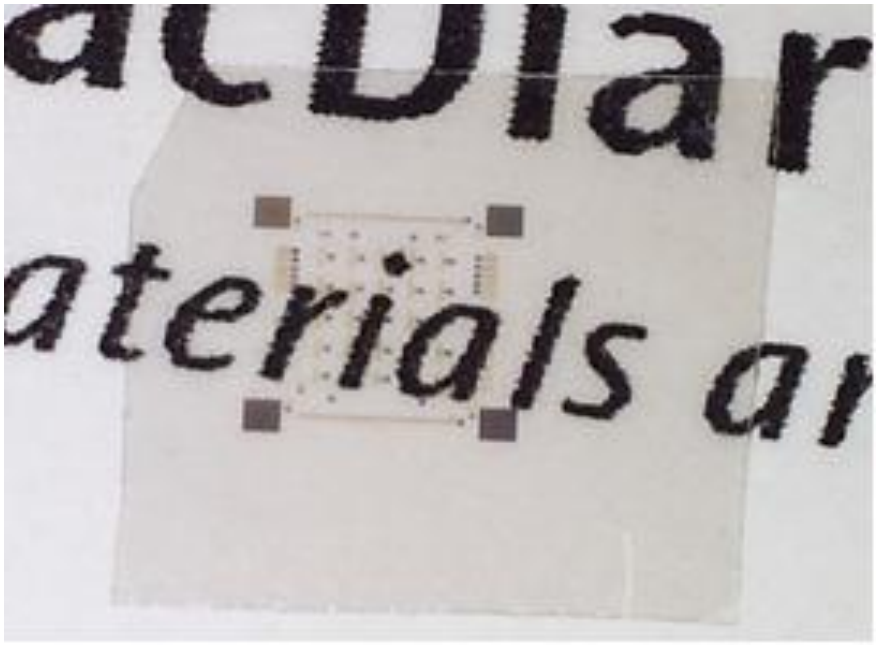

Figure 7.3 – Transparent MESFET devices fabricated using 10 nm AgO_x Schottky gates capped with 100 nm of ITO. The drain and source contacts are 100 nm of ITO.

Figure 7.4 shows the Schottky gate I-V curves associated with each gate thickness, while the extracted figures of merit are given in Table 7.1. It can be seen that the 10 nm Schottky gate has a significantly higher forward current compared to the 30 nm Schottky gate. This is expected as AgO_x has a lower conductivity than ITO; therefore by using a thinner AgO_x layer in the gate composition, the overall series resistance of the gate contact is reduced, resulting in a larger forward current. It can also be seen that the 10 nm AgO_x Schottky gate has formed a better contact with the IGZO film, as evident from an ideality factor of 1.1 compared to 1.3 for the 30 nm AgO_x gate. The barrier heights for both gate thicknesses were similar, and comparable to the device characterised in Chapter 4 that was fabricated on the same film using Ti/Au ohmic contacts instead of ITO.

Figure 7.5 shows the transfer curves for both devices. Both devices have similar subthreshold swings, 134 mV/dec for the 10 nm AgO_x Schottky gate compared to 162

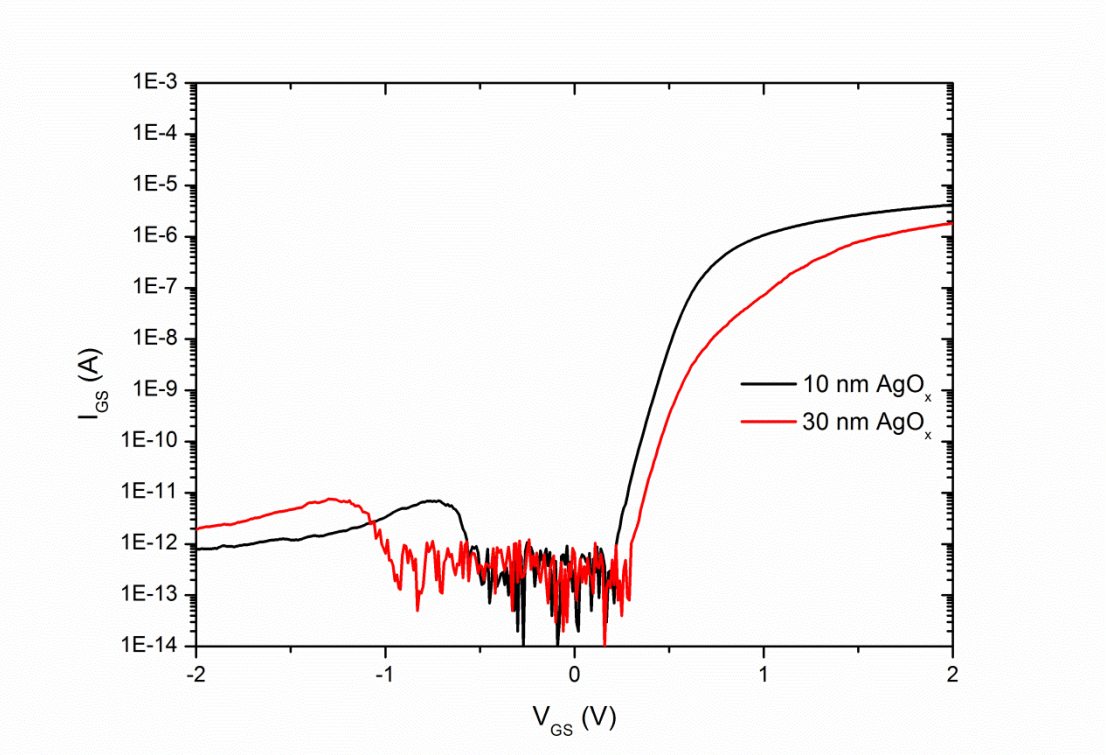

Figure 7.4 – I-V comparison between devices with different thickness Schottky gate contacts. Devices have channel width 50 µm and Schottky gate length 5 µm.

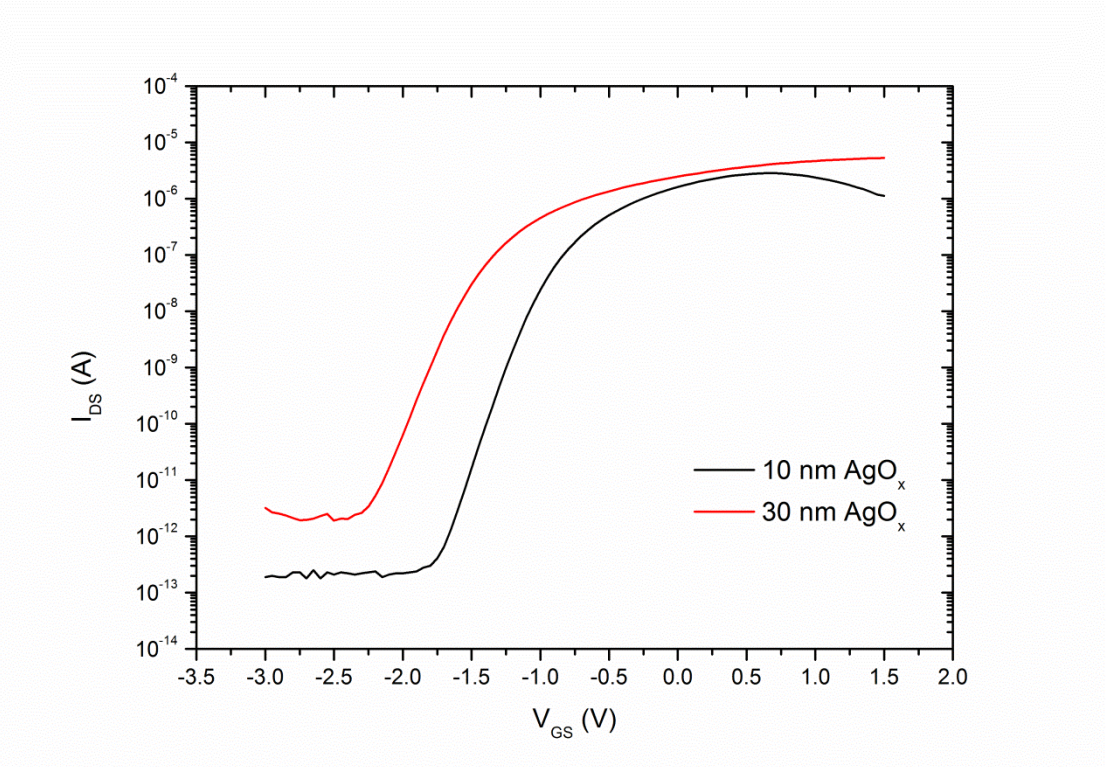

Figure 7.5 – Transfer curve comparison between devices with different thickness Schottky gate contacts. Devices have channel width 50 µm and Schottky gate length 5 µm.

mV/dec for the 30 nm AgO_x Schottky gate. However, there is a significant difference in the threshold voltage with the thicker device having a more negative value, although the exact cause of this effect is uncertain, it is expected to be due to differing amounts of illumination during probe setup. Overall, there is no degradation in electrical performance when reducing the AgO_x Schottky gate thickness to 10 nm.

7.3 Flexibility

As these devices were fabricated on a flexible plastic substrate, it is only natural to also determine how they respond to bending. Nomura [6] has shown that IGZO MOSFETs are capable of being bent at a radius of 30 mm without any significant degradation in electrical properties. This section explores how MESFETs survive such an encounter.

The device characterisations were performed in a dark environment to prevent any photoconductivity effects from obscuring the results. The initial measurements were performed on a flat surface to act as a baseline for the bending experiment. Initially, the device was bent on a surface with radius 30 mm as depicted in Figure 7.6. The main figure of merit used to determine the performance change for each bending experiment was the device transfer curve. As single bending had no effect on the transfer curve, the substrate was bent 30 times, followed by an additional 70 times. This process was then repeated with surface radii of 18 mm, 12 mm and 7 mm. Due to limitations of the stage used to perform the measurements, only the 30 mm radius results were tested while the device was being bent. The remaining results were measured on a flat surface after being bent at the specified radii.

The results of the bending experiments can be seen in Figure 7.7. This figure shows that even after bending the device 100 times at a radius of 7 mm, very little deviation in device performance was observed. There was a slight shift in the threshold voltage, which can be explained in two ways. The first explanation is that the shift is a photoconductivity effect caused by the 40 $\mu W/cm^2$ red light of wavelength 625 nm used to align the probes for each measurement. However, as mentioned in Chapter 6, this wavelength should not be of sufficient energy to ionize oxygen vacancies which are the main cause of negative threshold voltage shift under illumination. The second explanation is that the mechanical bending causes a physical change in the film [63]. The theory states that as the device is bent at increasingly sharper radii, the distance between the atoms increases marginally. This in turn decreases the energy level splitting of the bonding and anti-bonding orbital's between the atoms in the semiconductor layer [63]. The lowered energy level splitting allows

Figure 7.6 – Testing setup for the mechanical bending of substrates at a radius of 30 mm.

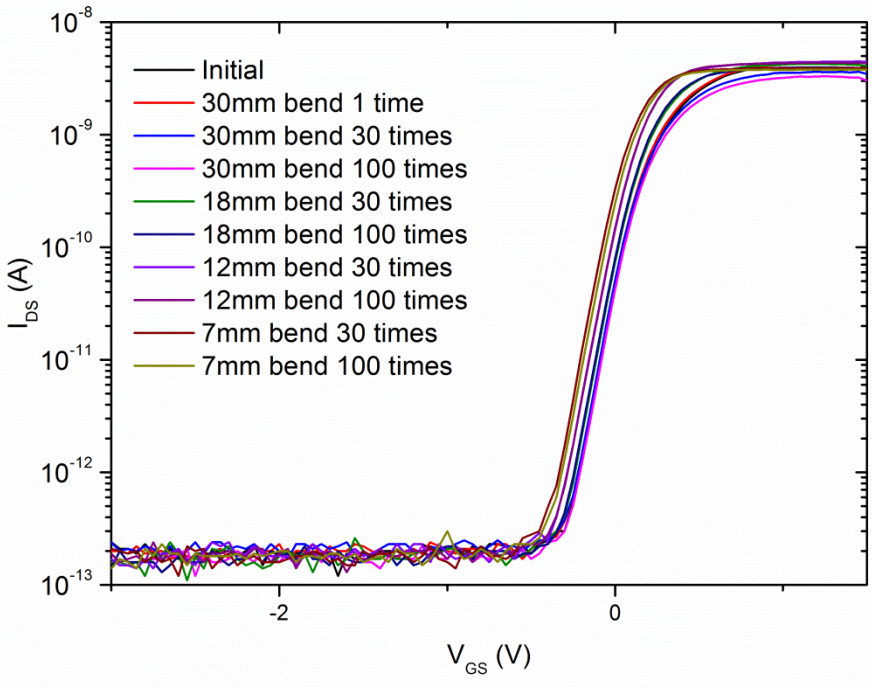

Figure 7.7 – Current-voltage characteristics from flexible IGZO MESFET gate contact (with dimensions 50 µm x 10 µm) after bending at indicated radii/repetitions.

for more electrons to be excited to the anti-bonding state while the film is under tensile strain. As with ionised oxygen vacancies, the increase in electron concentration causes an increase in the channel conductivity as well as a negative threshold voltage shift.

CHAPTER 8

Conclusion and Future work

8.1 Conclusion

The aim of this thesis was to examine the device performance of flexible transparent MESFETs fabricated using IGZO films. A range of sputtering conditions were examined in order to optimise the properties of IGZO films grown on flexible PEN substrates using a molar 1:1:1 In:Ga:Zn sputtering target. Compared to a-Si:H TFTs, the fabricated devices showed excellent electrical properties with an on-off ratio in excess of 7 orders of magnitude, a subthreshold swing of 120 mV/dec, and an effective channel mobility of 5-12 cm^2/Vs. A variety of Schottky gate materials were investigated for use in these MESFETs, including AgO_x, IrO_x and PtO_x. All MESFET devices with these different gate materials showed a remarkable increase in device performance after one year of aging. The same effect was achieved by annealing the devices for 20 minutes at 120 ºC in atmospheric conditions. This change in device performance was most likely due to the absorption of atmospheric oxygen filling in oxygen vacancies. As oxygen vacancies are thought to be the major donor in IGZO, a reduction in oxygen vacancies reduces the carrier concentration, allowing the devices to display improved switching performance.

The fabricated devices were subjected to various 61,110 second stress tests to investigate device stability. In dark conditions, the devices proved stable with

threshold voltage shifts of less than -0.17 V, while under illumination this increased to -0.54 V. These shifts proved to be recoverable after the devices were left for several days. These effects are associated with the oxygen vacancies in the IGZO channel and gate interface, which act as hole traps. These oxygen vacancies are able to diffuse at room temperature; therefore as the stress tests proceed oxygen vacancies are attracted or repelled from the gate-semiconductor interface depending on the polarity of the gate bias, which shifts the threshold voltage.

As many of the potential applications for a-IGZO films are in optoelectronics, device performance was studied under the effects of illumination. It was discovered that light exposure tends to significantly increase the on-current of IGZO MESFET devices, with photon energies above 2.3 eV producing the largest effects. This energy is associated with the ionisation energy of oxygen vacancies in IGZO. The increase in on-current was partially recoverable using gate voltage pulses, however full recovery required the devices to be left for several days. It was demonstrated that passivation layers could be used to prevent device degradation caused by atmospheric exposure, however their effectiveness in reducing persistent photoconductivity effects was relatively low. Flexible MESFET devices fabricated on PEN substrate were shown to suffer minimal performance loss even after being subjected mechanical bending at radii as low as 7 mm. This suggests significant promise for the use of a-IGZO MESFETs in future flexible transparent electronics.

8.2 Future Work

The focus of future work can be categorised into several different areas:

- IGZO Film quality.

All the films used in this thesis were grown from the same 1:1:1 molar In:Ga:Zn

target. However this may not be the most optimal target composition, as the measured Hall mobility was relatively low (5 cm^2/Vs) compared to literature reports. The use of a different target composition such as a 2:1:2 molar In:Ga:Zn target should improve the mobility of the resultant films by reducing the gallium fraction.

- Different Schottky gates

It was shown via a dramatic aging process, that there was a significant change in the Schottky gate contact over time. This is an undesirable effect and needs to be fully characterised. It is possible a different Schottky contact composition may improve the electrical performance of IGZO MESFET devices.

- Stability testing

Further stability tests such as temperature stability would be useful as would further investigations into the effect of different passivation layers on device stability, both in the dark and under illumination.

- Passivation

Additional passivation layers could include Al_2O_3, $HfAlO_x$ and polymers such as SU-8. A more detailed look at the passivation layers, including AFM, SEM and leakage measurements may determine why some layers are better than others.

- Mechanical Stress

Further mechanical stress tests should also be considered, such as comparing the effects of compression as well as tensile strain. It would also be worth discovering the limits these devices can withstand before being destroyed.

- Device Structure

By changing the device structure, these MESFETs may be used in optical display applications such as transparent pixel drivers. By fabricating single pixel circuits the viability of MESFETs as display drivers could be investigated.

Bibliography

[1] H. Gleskova, P. I. Hsu, Z. Xi, J. C. Sturm, Z. Suo and S. Wagner, "Field-effect mobility of amorphous silicon thin-film transistors under strain," *Journal of Non-Crystalline Solids,* vol. 338, pp. 732-735, 2004.

[2] S. Higashi, D. Abe, Y. Hiroshima, K. Miyashita, T. Kawamura, S. Inoue and T. Shimoda, "High-quality SiO2/Si interface formation and its application to fabrication of low-temperature-processed polycrystalline Si thin-film transistor," *Japanese Journal of Applied Physics Part 1,* vol. 41, no. 6A, pp. 3646-3650, 2002.

[3] C. S. Chiang, J. Kanicki and K. Takechi, "Electrical Instability of Hydrogenated Amorphous Silicon Thin-Film Transistors for Active-Matrix Liquid-Crystal Displays," *Japanese Journal of Applied Physics Part 1,* vol. 37, no. 9A, pp. 4704-4710, 1998.

[4] J. Y. Kwon, K. S. Son, J. S. Jung, T. S. Kim, M. K. Ryu, K. B. Park, B. W. Yoo, J. W. Kim, Y. G. Lee, K. C. Park, S. Y. Lee and J. M. Kim, "Bottom-Gate Gallium Indium Zinc Oxide Thin-Film Transistor Array for High-Resolution AMOLED Display," *Ieee Electron Device Letters,* vol. 29, no. 12, pp. 1309-1311, 2008.

[5] H. Hosono, M. Yasukawa and H. Kawazoe, "Novel oxide amorphous semiconductors: Transparent conducting amorphous oxides," *Journal of Non-Crystalline Solids,* vol. 203, pp. 334-344, 1996.

[6] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature,* vol. 432, no. 7016, pp. 488-492, 2004.

[7] Sharp, 13 April 2012. [Online]. Available: http://www.sharp-world.com/corporate/news/120413.html. [Accessed 5 Feburary 2014].

[8] S. Elzwawi, H. S. Kim, M. Lynam, E. L. H. Mayes, D. G. McCulloch, M. W. Allen and J. G. Partridge, "Stable n-channel metal-semiconductor field effect transistors on ZnO films deposited using a filtered cathodic vacuum arc," *Applied Physics Letters,* vol. 101, no. 24, 2012.

[9] K. L. Chopra, S. Major and D. K. Pandya, "Transparent Conductors - a Status Review," *Thin Solid Films,* vol. 102, no. 1, pp. 1-46, 1983.

[10] J. R. Bellingham, W. A. Phillips and C. J. Adkins, "Electrical and Optical-Properties of Amorphous Indium Oxide," *Journal of Physics-Condensed Matter,* vol. 2, no. 28, pp. 6207-6221, 1990.

[11] H. Hosono, N. Kikuchi, N. Ueda, H. Kawazoe and K. Shimidzu, "Amorphous Transparent

Electroconductor 2cdo-Center-Dot-Geo2 - Conversion of Amorphous Insulating Cadmium Germanate by Ion-Implantation," *Applied Physics Letters,* vol. 67, no. 18, pp. 2663-2665, 1995.

[12] H. Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong and D. A. Keszler, "High mobility transparent thin-film transistors with amorphous zinc tin oxide channel layer," *Applied Physics Letters,* vol. 86, no. 1, 2005.

[13] N. L. Dehuff, E. S. Kettenring, D. Hong, H. Q. Chiang, J. F. Wager, R. L. Hoffman, C. H. Park and D. A. Keszler, "Transparent thin-film transistors with zinc indium oxide channel layer," *Journal of Applied Physics,* vol. 97, no. 6, 2005.

[14] M. S. Grover, P. A. Hersh, H. Q. Chiang, E. S. Kettenring, J. F. Wager and D. A. Keszler, "Thin-film transistors with transparent amorphous zinc indium tin oxide channel layer," *Journal of Physics D-Applied Physics,* vol. 40, no. 5, pp. 1335-1338, 2007.

[15] A. Takagi, K. Nomura, H. Ohta, H. Yanagi, T. Kamiya, M. Hirano and H. Hosono, "Carrier transport and electronic structure in amorphous oxide semiconductor, a-InGaZnO4," *Thin Solid Films,* vol. 486, no. 1-2, pp. 38-41, 2005.

[16] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano and H. Hosono, "Amorphous oxide semiconductors for high-performance flexible thin-film transistors," *Japanese Journal of Applied Physics Part 1,* vol. 45, no. 5B, pp. 4303-4308, 2006.

[17] T. Kamiya and H. Hosono, "Material characteristics and applications of transparent amorphous oxide semiconductors," *Npg Asia Materials,* vol. 2, no. 1, pp. 15-22, 2012.

[18] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano and H. Hosono, "Electron transport in InGaO3(ZnO)(m) (m = integer) studied using single-crystalline thin films and transparent MISFETs," *Thin Solid Films,* vol. 445, no. 2, pp. 322-326, 2003.

[19] A. Takagi, K. Nomura, H. Ohta, H. Yanagi, T. Kamiya, M. Hirano and H. Hosono, "Carrier transport and electronic structure in amorphous oxide semiconductor, a-InGaZnO4," *Thin Solid Films,* vol. 486, no. 1-2, pp. 38-41, 2005.

[20] K. Nomura, T. Kamiya, H. Ohta, T. Uruga, M. Hirano and H. Hosono, "Local coordination structure and electronic structure of the large electron mobility amorphous oxide semiconductor In-Ga-Zn-O: Experiment and ab initio calculations," *Physical Review B,* vol. 75, no. 3, 2007.

[21] K. Nomura, T. Kamiya and H. Hosono, "Interface and bulk effects for bias-light-illumination instability in amorphous-In-Ga-Zn-O thin-film transistors," *Journal of the Society for Information Display,* vol. 18, no. 10, pp. 789-795, 2010.

[22] A. Janotti and C. G. Van de Walle, "Oxygen vacancies in ZnO," *Applied Physics Letters,* vol. 87, no. 12, 2005.

[23] K. Takechi, M. Nakata, T. Eguchi, H. Yamaguchi and S. Kaneko, "Comparison of Ultraviolet Photo-Field Effects between Hydrogenated Amorphous Silicon and Amorphous InGaZnO4 Thin-Film Transistors," *Japanese Journal of Applied Physics,* vol. 48, no. 1, 2009.

[24] B. Ryu, H. K. Noh, E. A. Choi and K. J. Chang, "O-vacancy as the origin of negative bias illumination stress instability in amorphous In-Ga-Zn-O thin film transistors," *Applied Physics Letters,* vol. 97, no. 2, 2010.

[25] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics,* vol. 38, no. 8, pp. 114-117, 1965.

[26] K. P. Pande and C. C. Shen, "A GaAs Misfet with Ge3n4 Gate Dielectric," *Applied Physics a-Materials Science & Processing,* vol. 28, no. 2, pp. 123-124, 1982.

[27] T. P. Ma, "Making silicon nitride film a viable gate dielectric," *Ieee Transactions on Electron Devices,* vol. 45, no. 3, pp. 680-690, 1998.

[28] S. Sze, Semiconductor Devices Physics and Technology, New York: Wiley, 2002.

[29] H. J. Levinson, Principles of Lithography, SPIE Publications, 2005.

[30] V. Zardetto, T. M. Brown, A. Reale and A. Di Carlo, "Substrates for Flexible Electronics: A Practical Investigation on the Electrical, Film Flexibility, Optical, Temperature, and Solvent Resistance Properties," *Journal of Polymer Science Part B-Polymer Physics,* vol. 49, no. 9, pp. 638-648, 2011.

[31] K. Reichelt and X. Jiang, "The Preparation of Thin-Films by Physical Vapor-Deposition Methods," *Thin Solid Films,* vol. 191, no. 1, pp. 91-126, 1990.

[32] J. George, "Sputtering," in *Preparation of Thin Films*, New York, CRC Press, 1992, pp. 41-100.

[33] K. Wasa, M. Kitabatake and H. Adachi, Thin Film Materials Technology: Sputtering of Compound Materials, Norwich: William Andrew, 2004.

[34] K. Wasa, Handbook of Sputter Deposition Technology: Fundamentals and Applications for Functional Thin Films, Nano-Materials and MEMS, Waltham: William Andrew, 2012.

[35] P. Kelly and R. Arnell, "Magnetron sputtering: a review of recent developments and applications," *Vacuum,* vol. 56, no. 3, pp. 159-172, 2000.

[36] U. Helmersson, M. Lattemann, J. Bohlmark, A. P. Ehiasarian and J. T. Gudmundsson, "Ionized physical vapor deposition (IPVD): A review of technology and applications," *Thin Solid Films,* vol. 513, no. 1-2, pp. 1-24, 2006.

[37] H. Q. Chiang, B. R. McFarlane, D. Hong, R. E. Presley and J. F. Wager, "Processing effects on the stability of amorphous indium gallium zinc oxide thin-film transistors," *Journal of Non-Crystalline Solids,* vol. 354, no. 19-25, pp. 2826-2830, 2008.

[38] S. Hüfner, Photoelectron Spectroscopy Principles and Applications, Berlin: Springer, 2010.

[39] Y. B. Zheng, G. Li, W. L. Wang, X. C. Li and Z. G. Jiang, "Dry Etching Characteristics of Amorphous Indium-Gallium-Zinc-Oxide Thin Films," *Plasma Science & Technology,* vol. 14, no. 10, pp. 915-918, 2012.

[40] J. C. Park, O. G. Jeong, J. K. Kim, Y. H. Yun, S. J. Pearton and H. Cho, "Comparison of chlorine- and fluorine-based inductively coupled plasmas for dry etching of InGaZnO4 films," *Thin Solid Films,* vol. 546, pp. 136-140, 2013.

[41] C. Y. Lee, C. Chang, W. P. Shih and C. L. Dai, "Wet etching rates of InGaZnO for the fabrication of transparent thin-film transistors on plastic substrates," *Thin Solid Films,* vol. 518, no. 14, pp. 3992-3998, 2010.

[42] W. S. Kim, Y. K. Moon, K. T. Kim, J. H. Lee, B. D. Ahn and J. W. Park, "An investigation of contact resistance between metal electrodes and amorphous gallium-indium-zinc oxide (a-GIZO) thin-film transistors," *Thin Solid Films,* vol. 518, no. 22, pp. 6357-6360, 2010.

[43] M. W. Allen, S. M. Durbin and J. B. Metson, "Silver oxide Schottky contacts on n-type ZnO," *Applied Physics Letters,* vol. 91, no. 5, 2007.

[44] A. Chasin, S. Steudel, K. Myny, M. Nag, T. H. Ke, S. Sohols, J. Genoe, G. Gielen and P. Heremans, "High-performance a-In-Ga-Zn-O Schottky diode with oxygen-treated metal contacts," *Applied Physics Letters,* vol. 101, no. 11, 2012.

[45] M. H. Lee, B. F. Hsieh and S. T. Chang, "Electrical properties correlated with redistributed deep states in a-Si:H thin-film transistors on flexible substrates undergoing mechanical bending," *Thin Solid Films,* vol. 528, pp. 82-85, 2013.

[46] M. Lorenz, A. Lajn, H. Frenzel, H. V. Wenckstern, M. Grundmann, P. Barquinha, R. Martins and E. Fortunato, "Low-temperature processed Schottky-gated field-effect transistors based on amorphous gallium-indium-zinc-oxide thin films," *Applied Physics Letters,* vol. 97, no. 24, 2010.

[47] H. J. Chung, J. H. Jeong, T. K. Ahn, H. J. Lee, M. Kim, K. Jun, J. S. Park, J. K. Jeong, Y. G. Mo and H. D. Kim, "Bulk-limited current conduction in amorphous InGaZnO thin films," *Electrochemical and Solid State Letters,* vol. 11, no. 3, pp. H51-H54, 2008.

[48] M. W. Allen, R. J. Mendelsberg, R. J. Reeves and S. M. Durbin, "Oxidized noble metal Schottky contacts to n-type ZnO," *Applied Physics Letters,* vol. 94, no. 10, 2009.

[49] D. H. Lee, K. Nomura, T. Kamiya and H. Hosono, "Diffusion-Limited a-IGZO/Pt Schottky Junction Fabricated at 200 degrees C on a Flexible Substrate," *Ieee Electron Device Letters,* vol. 32, no. 12, pp. 1695-1697, 2011.

[50] S. W. Tsao, T. C. Chang, S. Y. Huang, M. C. Chen, S. C. Chen, C. T. Tsai, Y. J. Kuo, Y. C. Chen and W. C. Wu, "Hydrogen-induced improvements in electrical characteristics of a-IGZO thin-film transistors," *Solid-State Electronics,* vol. 54, no. 12, pp. 1497-1499, 2010.

[51] K. Hoshino, D. Hong, H. Q. Chiang and J. F. Wager, "Constant-Voltage-Bias Stress Testing of a-IGZO Thin-Film Transistors," *eee Transactions on Electron Devices,* vol. 56, no. 7, pp. 1365-1370, 2009.

[52] T. C. Fung, K. Abe, H. Kumomi and J. Kanicki, "Electrical Instability of RF Sputter Amorphous In-Ga-Zn-O Thin-Film Transistors," *Journal of Display Technology,* vol. 5, no. 12, pp. 452-461, 2009.

[53] D. Kang, H. Lim, C. Kim, I. Song, J. Park, Y. Park and J. Chung, "Amorphous gallium indium zinc oxide thin film transistors: Sensitive to oxygen molecules," *Applied Physics Letters,* vol. 90, no. 19, 2007.

[54] J. K. Jeong, H. W. Yang, J. H. Jeong, Y. G. Mo and H. D. Kim, "Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors," *Applied Physics Letters,* vol. 93, no. 12, 2008.

[55] K. Nomura, T. Kamiya, M. Hirano and H. Hosono, "Origins of threshold voltage shifts in room-temperature deposited and annealed a-In-Ga-Zn-O thin-film transistors," *Applied Physics Letters,* vol. 95, no. 1, 2009.

[56] S. Yasuno, T. Kita, S. Morita, T. Kugimiya, K. Hayashi and S. Sumie, "Transient photoconductivity responses in amorphous In-Ga-Zn-O films," *Journal of Applied Physics,* vol. 112, no. 5, 2012.

[57] J. J. Luo, A. U. Adler, T. O. Mason, D. B. Buchholz, R. P. H. Chang and M. Grayson, "Transient photoresponse in amorphous In-Ga-Zn-O thin films under stretched exponential analysis," *Journal of Applied Physics,* vol. 113, no. 15, 2013.

[58] S. Jeon, S. E. Ahn, I. Song, C. J. Kim, U. I. Chung, E. Lee, I. Yoo, A. Nathan, S. Lee, J. Robertson and K. Kim, "Gated three-terminal device architecture to eliminate persistent photoconductivity in oxide semiconductor photosensor arrays," *Nature Materials,* vol. 11, no. 4, pp. 301-305, 2012.

[59] S. E. Ahn, I. Song, S. Jeon, Y. W. Jeon, Y. Kim, C. Kim, B. Ryu, J. H. Lee, A. Nathan, S. Lee, G. T. Kim and U. I. Chung, "Metal Oxide Thin Film Phototransistor for Remote Touch Interactive Displays," *Advanced Materials,* vol. 24, no. 19, pp. 2631-2636, 2012.

[60] K. Ghaffarzadeh, A. Nathan, J. Robertson, S. Kim, S. Jeon, C. Kim, U. I. Chung and J. H. Lee, "Instability in threshold voltage and subthreshold behavior in Hf-In-Zn-O thin film transistors induced by bias-and light-stress," *Applied Physics Letters,* vol. 97, no. 11, 2010.

[61] J. H. Shin and D. K. Choi, "Effect of Oxygen on the Optical and the Electrical Properties of Amorphous InGaZnO Thin Films Prepared by RF Magnetron Sputtering," *Journal of the Korean Physical Society,* vol. 53, no. 4, pp. 2019-2023, 2008.

[62] D. A. Zuev, A. A. Lotin, O. A. Novodvorsky, F. V. Lebedev, O. D. Khramova, I. A. Petuhov, P. N. Putilin, A. N. Shatohin, M. N. Rumyanzeva and A. M. Gaskov, "Pulsed laser deposition of ITO thin films and their characteristics," *Semiconductors,* vol. 46, no. 3, pp. 410-413, 2012.

[63] N. Munzenrieder, K. H. Cherenack and G. Troster, "The Effects of Mechanical Bending and Illumination on the Performance of Flexible IGZO TFTs," *Ieee Transactions on Electron Devices,* vol. 58, no. 7, pp. 2041-2048, 2011.

[64] H. Hosono, Y. Yamashita, N. Ueda, H. Kawazoe and K. Shimidzu, "New amorphous semiconductor: 2CdO center dot PbOx," *Applied Physics Letters,* vol. 65, no. 5, pp. 661-663, 1996.

APPENDIX A

The following is the code used on the Hewlett Packard 4155B semiconductor parameter analyser to perform the stress measurements in Chapter 5.

```
10   COM @Hp415x
20   ASSIGN @Hp415x TO 800
30   OUTPUT @Hp415x;":MMEM:LOAD:STAT 0,'WAIT30.STR','DISK'"
40   OUTPUT @Hp415x;":MMEM:LOAD:STAT 0,'AMFTMATT.MES','DISK'"
50   FOR I=1 TO 20
60   OUTPUT @Hp415x;":PAGE:SCON:STR:STAR"
70   OUTPUT @Hp415x;"*OPC?"
80   ENTER @Hp415x;Complete
90   OUTPUT @Hp415x;":PAGE:SCON:MEAS:SING"
100  OUTPUT @Hp415x;"*OPC?"
110  ENTER @Hp415x;Complete
120  Filename$="BN"&VAL$(I)&".DAT"
130  EXECUTE ("SAVEDATA FILENAME$")
140  File2$="BN"&VAL$(I)
150  OUTPUT @Hp415x;":MMEM:STOR:SSH:DEL SPACE"
160  OUTPUT @Hp415x;":MMEM:STOR:SSH:LIND 1,MAX"
170  OUTPUT @Hp415x;":MMEM:STOR:SSH:SMARK NONE"
180  OUTPUT @Hp415x;":MMEM:STOR:SSH:UNIT OFF"
190  OUTPUT @Hp415x;":MMEM:STOR:SSH ";CHR$(39)&File2$&CHR$(39)
200  NEXT I
210  OUTPUT @Hp415x;":MMEM:LOAD:STAT 0,'STRTSN.STR','DISK'"
220  REAL Durtim(1:5)
230  DATA 10, 100, 1000,
240  DATA 10000,
250  DATA 50000
260  READ Durtim(*)
270  FOR I=1 TO 5
280  !
290  Dur=Durtim(I)
300  !
310  OUTPUT @Hp415x;":PAGE:STR:SET:DUR";Dur
320  OUTPUT @Hp415x;":PAGE:SCON:STR:STAR"
330  OUTPUT @Hp415x;"*OPC?"
340  ENTER @Hp415x;Complete
350  OUTPUT @Hp415x;":PAGE:SCON:MEAS:SING"
360  OUTPUT @Hp415x;"*OPC?"
```

```
370  ENTER @Hp415x;Complete
380  Filename2$="NS"&VAL$(Dur)&".DAT"
390  File3$="NS"&VAL$(I)
400  OUTPUT @Hp415x;":MMEM:STOR:SSH:DEL SPACE"
410  OUTPUT @Hp415x;":MMEM:STOR:SSH:LIND 1,MAX"
420  OUTPUT @Hp415x;":MMEM:STOR:SSH:SMARK NONE"
430  OUTPUT @Hp415x;":MMEM:STOR:SSH:UNIT OFF"
440  OUTPUT @Hp415x;":MMEM:STOR:SSH ";CHR$(39)&File3$&CHR$(39)
450  EXECUTE ("SAVEDATA FILENAME2$")
460  NEXT I
470  OUTPUT @Hp415x;":MMEM:LOAD:STAT 0,'WAIT30.STR','DISK'"
480  FOR I=1 TO 20
490  OUTPUT @Hp415x;":PAGE:SCON:STR:STAR"
500  OUTPUT @Hp415x;"*OPC?"
510  ENTER @Hp415x;Complete
520  OUTPUT @Hp415x;":PAGE:SCON:MEAS:SING"
530  OUTPUT @Hp415x;"*OPC?"
540  ENTER @Hp415x;Complete
550  Filename3$="AN"&VAL$(I)&".DAT"
560  EXECUTE ("SAVEDATA FILENAME3$")
570  File4$="AN"&VAL$(I)
580  OUTPUT @Hp415x;":MMEM:STOR:SSH:DEL SPACE"
590  OUTPUT @Hp415x;":MMEM:STOR:SSH:LIND 1,MAX"
600  OUTPUT @Hp415x;":MMEM:STOR:SSH:SMARK NONE"
610  OUTPUT @Hp415x;":MMEM:STOR:SSH:UNIT OFF"
620  OUTPUT @Hp415x;":MMEM:STOR:SSH ";CHR$(39)&File4$&CHR$(39)
630  NEXT I
640  OUTPUT @Hp415x;":MMEM:LOAD:STAT 0,'STRTSP.STR','DISK'"
650  REAL Durtim(1:5)
660  DATA 10, 100, 1000,
670  DATA 10000,
680  DATA 50000
690  READ Durtim(*)
700  FOR I=1 TO 5
710  !
720  Dur=Durtim(I)
730  !
740  OUTPUT @Hp415x;":PAGE:STR:SET:DUR";Dur
750  OUTPUT @Hp415x;":PAGE:SCON:STR:STAR"
760  OUTPUT @Hp415x;"*OPC?"
770  ENTER @Hp415x;Complete
780  OUTPUT @Hp415x;":PAGE:SCON:MEAS:SING"
790  OUTPUT @Hp415x;"*OPC?"
800  ENTER @Hp415x;Complete
810  Filename4$="PS"&VAL$(Dur)&".DAT"
820  File5$="PS"&VAL$(I)
830  OUTPUT @Hp415x;":MMEM:STOR:SSH:DEL SPACE"
840  OUTPUT @Hp415x;":MMEM:STOR:SSH:LIND 1,MAX"
850  OUTPUT @Hp415x;":MMEM:STOR:SSH:SMARK NONE"
```

```
860  OUTPUT @Hp415x;":MMEM:STOR:SSH:UNIT OFF"
870  OUTPUT @Hp415x;":MMEM:STOR:SSH ";CHR$(39)&File5$&CHR$(39)
880  EXECUTE ("SAVEDATA FILENAME4$")
890  NEXT I
900  OUTPUT @Hp415x;":MMEM:LOAD:STAT 0,'WAIT30.STR','DISK'"
910  FOR I=1 TO 20
920  OUTPUT @Hp415x;":PAGE:SCON:STR:STAR"
930  OUTPUT @Hp415x;"*OPC?"
940  ENTER @Hp415x;Complete
950  OUTPUT @Hp415x;":PAGE:SCON:MEAS:SING"
960  OUTPUT @Hp415x;"*OPC?"
970  ENTER @Hp415x;Complete
980  Filename5$="AP"&VAL$(I)&".DAT"
981  EXECUTE ("SAVEDATA FILENAME5$")
982  File6$="AP"&VAL$(I)
983  OUTPUT @Hp415x;":MMEM:STOR:SSH:DEL SPACE"
984  OUTPUT @Hp415x;":MMEM:STOR:SSH:LIND 1,MAX"
985  OUTPUT @Hp415x;":MMEM:STOR:SSH:SMARK NONE"
986  OUTPUT @Hp415x;":MMEM:STOR:SSH:UNIT OFF"
987  OUTPUT @Hp415x;":MMEM:STOR:SSH ";CHR$(39)&File6$&CHR$(39)
988  NEXT I
989  END
```