Implementation of Four Real-Time Software Defined Receivers and a Space-Time Decoder using Xilinx Virtex 2 Pro Field Programmable Gate Array

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Abstract

This paper describes the concept, architecture, development and demonstration of a real time, high performance, software defined 4-receiver system and a space time decoder to be implemented on a Xilinx Virtex 2 Pro Field Programmable Gate Array. It is designed and developed for research into receiver diversity and multiple input and multiple output (MIMO)wireless systems. Each receiver has a Freescale DSP56321 digital signal processor (DSP) to run synchronization, channel state estimation and equalization algorithms. The system is software defined to allow for flexibility in the choice of receiver demodulation formats, output data rates and space-time decoding schemes. Hardware, firmware and software aspects of the receiver and space time decoder system to meet design requirements are discussed.

The current system implementation is an enhancement to an existing Smart Antenna Software RAdio Test System (SASRATS) platform [5, 6] designed to test and verify various space time architectures and algorithms. Our original receivers, developed in 2000 [5] were designed for low bandwidth (270 KBauds) and beamforning/smart antenna work. The latest enhancement allows high bandwidth performance (4 MBauds), parallel 16-bit IQ baseband data outputs and greater programmability. The 4 receivers complement a 4 transmitter space time (ST) encoding platform designed and developed for real-time testing of ST coding schemes developed by Alamouti [1] and others mentioned in [4]. The primary objective is to increase system capacity and performance through the use of multiple antennas, employing spatial multiplexing and ST coding and decoding.

The focus of this paper is on the digital and baseband portion of the system. The analogue portion consists of an RF amplifier, a phase locked local oscillator, a mixer and intermediate frequency (IF) bandpass filters and high gain IF amplifiers whose purpose is to amplify, translate and filter a received radio frequency signal at 915 MHz or 2.4 GHz to an intermediate frequency (IF) of 70 MHz where digitization and bandpass sampling occurs. The architecture of the digital IF and baseband portion of the receivers is shown in Figure 1.

The 70 Mhz IF signal is digitised using bandpass sampling techniques using a high speed Analog Devices analog-to-digital convertor (ADC) AD6640 at a sampling clock frequency of 65 MHz. The sampling clock frequency is fully programmable and is generated from a Direct Digital Synthesizer (DDS) from a AD9857 Upconvertor integrated circuit (IC) working in fixed tone mode. This allows us the flexibility to change the sampling clock frequency for various experiments. The output of the ADC is then fed into a versatile Analog Devices AD6620 Digital Down Converter (DDC) which digitally downconverts, decimates and filters the input data to baseband IQ signals for further processing. The AD6620 is fully programmable and together with the AD9857, makes the receiver software defined. However, one is restricted by the chip design to resolution of the output data words to 16-bits and the sequential parallel 16-bit output format of the in-phase (I) and quadrature phase (Q) signals. The 16-bit sequential I and Q data are stored in 2 sets of 32-bit buffers. A Data_Valid pulse is generated after the IQ data are latched into the buffers. The IQ data can then be accessed as a simultaneous parallel 32-bit output pair or as separate I and Q data words, using memory mapped addressing under DSP or FPGA control. Simultaneous 32 bit parallel transfer is normally used between the DDC and a National Instruments Data Acquisition (NIDAQ) card which is used with the SASRATS platform to perform batch or pseudo real-time processing of data using MATLAB. This feature is useful during development and testing stages of the design.

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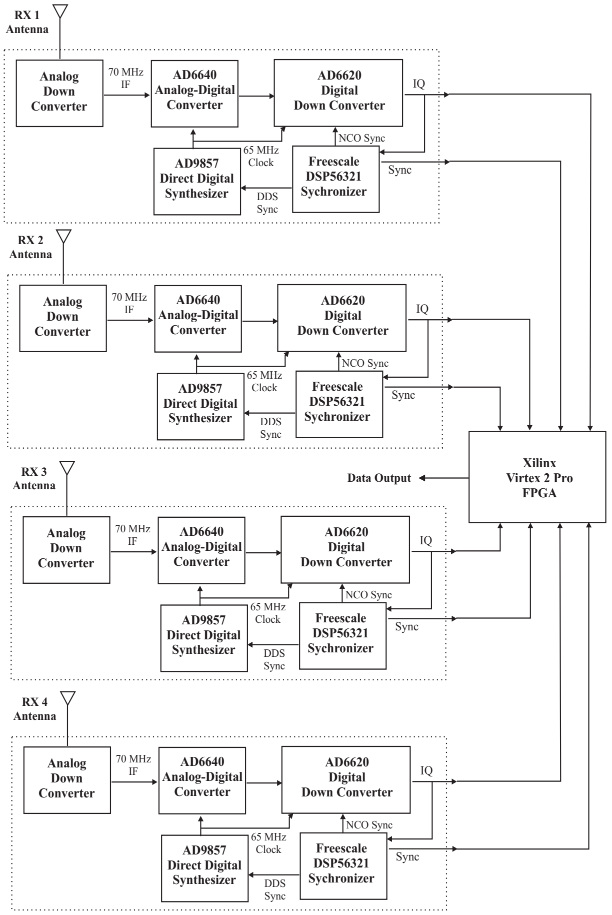

Figure 1. SASRAT 4 receiver system architecture with Xilinx space-time decoder

One set of buffered IQ signals are fed back into a Freescale DSP56321 platform through Port A which performs synchronization and channel estimation algorithms. The software for the DSP56321 is written in assembly language for optimum high speed performance. The output of this algorithm can dynamically control the Numerical Control Oscillator (NCO) in the AD6620 down convertor via Port B of the DSP or the AD9857 DDS through Port C to achieve synchronization.

In any digital receiver design, the major issues that must be solved involve the adjustment of gain in the receiver structure to work within the dynamic range of the signal processing algorithms, the ability to synchronize to the carrier frequency and phase, the ability to synchronize the time at which to sample the received symbols and the type of filtering needed for best possible bit-error performance. This paper does not cover the issues of gain control.

Carrier synchronization is required as the transmitter and the local oscillator (LO)in the receiver are derived from independent clock sources and will thus have a frequency offset. Doppler shift in the channel will also affect the received carrier frequency. Frequency offset will cause carrier phase rotation and correct decisions cannot be made on the rotating symbols. The local oscillator must be adjusted to stop this carrier rotation and continously track and correct any frequency offset that will occur over time.

We use a decoupled approach to carrier and timing synchronization. This allows the receiver to correct for carrier frequency offsets even when the symbol timing is not known. Wherever possible, we adopt a feedforward approach through the use of known training symbols (data-aided) or preambles to resolve phase ambiquity. This will also work in Rayleigh flat fading channels.

In our implementation to assist the receiver in correcting the frequency offset, a sync preamble is sent by the transmitter before data is sent. At the receiver, the I and Q data is processed by an algorithm depicted in Figure 2 which will adjust the frequency of the NCO to negate the frequency offset. On initialization and after a Data_Valid signal appears on the Interrupt Request (IRQ) line of the DSP, the DSP reads the I and Q data stored in the 32-bit buffer. The

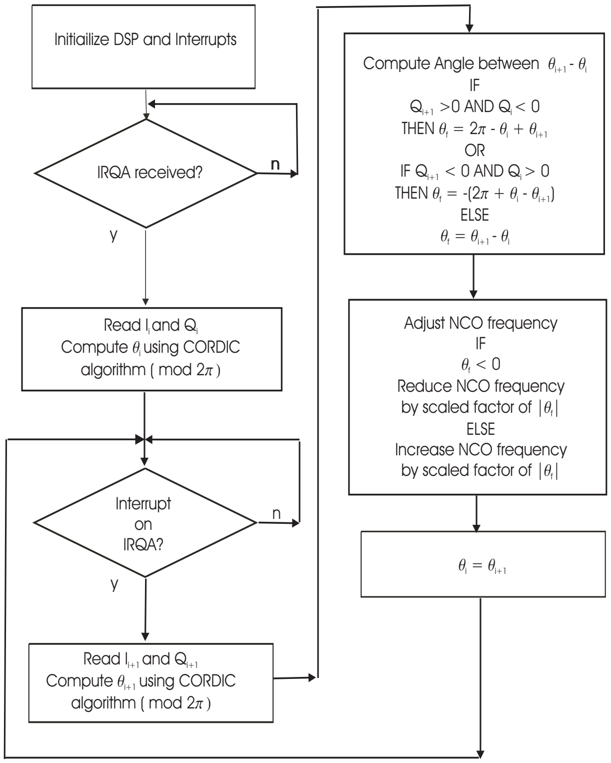
Initiailize DSP and Interrupts
IRQA received?
n
y
Read I_i and Q_i
Compute θ_i using CORDIC algorithm (mod 2π)
Interrupt on IRQA?
n
y
Read I_{i+1} and Q_{i+1}
Compute θ_{i+1} using CORDIC algorithm (mod 2π)
Compute Angle between θ_{i+1} - θ_i
IF
Q_{i+1} >0 AND Q_i < 0
THEN $\theta_f = 2\pi - \theta_i + \theta_{i+1}$
OR
IF Q_{i+1} < 0 AND Q_i > 0
THEN $\theta_f = -(2\pi + \theta_i - \theta_{i+1})$
ELSE
$\theta_f = \theta_{i+1} - \theta_i$
Adjust NCO frequency
IF
$\theta_f < 0$
Reduce NCO frequency by scaled factor of $|\theta_f|$
ELSE
Increase NCO frequency by scaled factor of $|\theta_f|$
$\theta_i = \theta_{i+1}$

Figure 2. Algorithm for Carrier Frequency Offset Compensation

algorithm then computes the phase angle of the vector using the Coordinate Rotation Digital Computer (CORDIC) algorithm [2]. The CORDIC algorithm is an iterative shift-add algorithm which can perform rectangular to polar conversions in DSPs' quickly and efficiently. This value is stored and the next IQ pair is then read and the new phase angle computed. The current and previous phases are compared and taking into account modulo 2π operation, the difference is computed. As the timing period between the current and previous samples is known, the frequency offset can be estimated. A positive estimate indicates that the NCO frequency is below the TX carrier and the converse is true. Knowing the direction and speed of the rotating vector, the NCO is then programmed to correct for this. A new IQ pair is read and the process is repeated over the duration of the sync preamble.

A symbol sync preamble follows the carrier sync preamble. The symbol sync preamble allows the receiver to estimate and track the time at which to sample the received waveform. Symbol timing recovery will be implemented on the DSP56321 based on an all digital maximum likelihood symbol timing recovery algorithm by Watkins and Taylor [9]. The Watkins timing error detector (TED) works at baud rate and has performance comparable to the fractionally sampled (2× baud rate) Gardner TED or the Amplitude Directed TED by Verdin and Tozer [3]. The Watkins TED also works well in Rayleigh flat fading channel.

In our complementary SASRATS transmitter platform [7] running a 2 transmit Alamouti encoding scheme, two symbols, s_0 and s_1 are transmitted simultanously from two transmitters at time instant t. At time instant $t + T$, the symbols $-s_1^*$ and s_0^* are transmitted simultanously from the transmitters where * represents the complex conjugate. This is depicted in Figure 3. The transmitted symbols travel through 2 independent channels h_0 and h_1 to a receiver where noise and interference n_0 and n_1 are added to the received signal. h_0 and h_1 are complex multiplicative distortions assumed constant across two consecutive symbols. It is shown in [1] that at the input of the combiner, the receive signals are given by $r_0 = r(t) = h_0 s_0 + h_1 s_1 + n_0$ and $r_1 = r(t + T) = -h_0 s_1^* + h_1 s_0^* + n_1$. A channel estimator algorithm estimates h_0 and h_1 and this information is also fed to the combiner to yield two combined output signals $\tilde{s}_0 = (\alpha_0^2 + \alpha_1^2)s_0 + h_0^* n_0 + h_1 n_1^*$ and $\tilde{s}_1 = (\alpha_0^2 + \alpha_1^2)s_1 - h_0 n_1^* + h_1^* n_0$ where α_0 and α_1 are the magnitudes of h_0 and h_1 respectively. The signals $\tilde{s}_0$ and $\tilde{s}_1$ together with the channel state information h_0 and h_1 are sent to the maximum likelihood (ML) detector so that ML estimates $\hat{s}_0$ and $\hat{s}_1$ can be made of s_0 and s_1. As we use PSK modulation of the symbols at the transmitter, the decision rule in the ML detector is to choose s_i iff $d^2(\tilde{s}_0, s_i) \leq d^2(\tilde{s}_0, s_k), \forall i \neq k$ for $\hat{s}_0$ and choose s_i iff $d^2(\tilde{s}_1, s_i) \leq d^2(\tilde{s}_1, s_k), \forall i \neq k$ for $\hat{s}_1$ where $d^2(x, y)$ is the squared Euclidean distance between signals x and y.

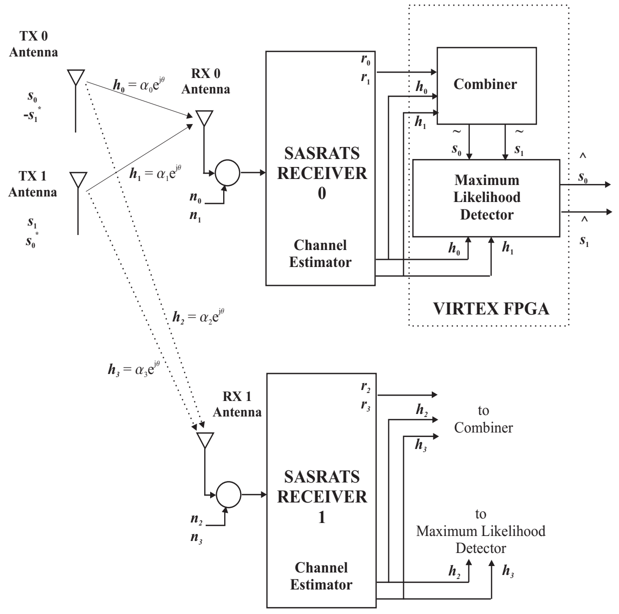

Figure 3. Block diagram of Alamouti decoding implementation on SASRATS platform

The Alamouti scheme can be extended to more than one receiver but to implement a 2 transmitter and 2 receiver system for example, requires the estimation of 4 channels (h_0, h_1, h_2 and h_3), 2 at each receiver as shown in Figure 3. The decoding of the Alamouti encoded signals is a linear process and our SASRATS receiver system design will implement the combiner and maximum likelihood detection on the Xilinx Virtex 2 Pro FPGA board using the *Xilinx Integrated System Enviroment (ISE) Foundation* design tool. The channel estimation is carried out on the DSP platforms.

The channel estimation algorithm will be based on a feedforward data-aided (DA) technique based on a set of training symbols sent after the carrier and timing sync preambles where optimal minimum mean square error (MMSE) from the received training symbols can be performed via ML estimation. Data aided reception is of relatively low complexity since channel estimation (carrier synchronization) and detection are totally decoupled [8]. Each transmitter will have orthogonal preambles to enable the receiver to estimate the different channels h_0 and h_1 needed in the 2 TX 1 RX Alamouti decoding scheme mentioned above.

The hardware architecture allows high speed IQ and synchronization signals from up to 4 receivers to be combined into the FPGA board for processing. For more sophiscated space-time decoding experiments that require a Viterbi decoder or other decoding algorithms, the *Xilinx Core Gener-*

ator modules can be used. The *Xilinx Core Generator Intellectual Property (IP)* modules [10] include math functions, correlators, filters, modulators, memory and storage elements incorporated into the ISE Foundation software. However, the Viterbi algorithm require an additional license.

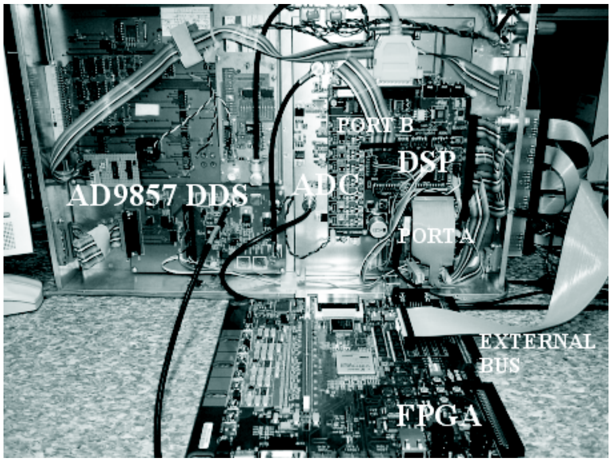

Figure 4. Photo of one SASRATS receiver with external FPGA board

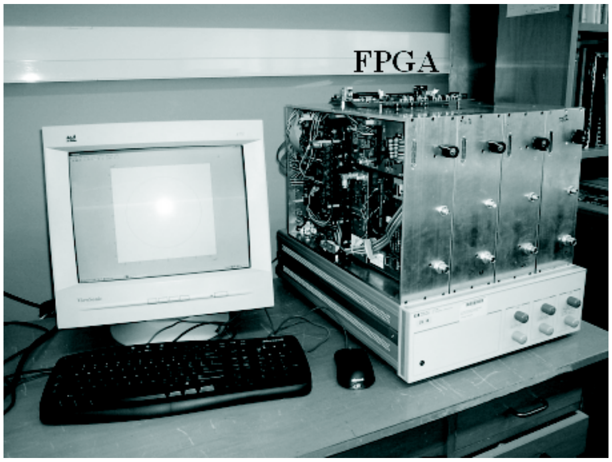

Figure 5. Photo of 4 SASRATS receivers with external FPGA board on top

Figure 4 shows the internal digital hardware of one receiver and Figure 5 shows the complete system consisting of 4 receivers. They are fully operational up to 5 Mbauds and fully software defined.

1 Conclusions

We have described the design and development of a real time software defined 4-receiver system and an Alamouti decoder to be implemented on an FPGA. Synchronization and decoder algorithms are fully defined with DSP software and FPGA firmware currently undergoing development and testing.

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