

ANALYSIS OF THE DUAL-FED DISTRIBUTED POWER AMPLIFIER

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Abstract

The dual-fed distributed amplifier is a variation of the conventional single-fed distributed amplifier. Namely, the input signal is fed to both ends of the input line and the power appearing at the ends of the output line is combined. This approach has the advantages of utilising power in both the forward and backward travelling waves on the output line, and the drain output power can be equalised among the FETs. In this paper, the operational behaviour of the dual-fed distributed power amplifier is investigated and the optimum operating conditions are identified. It has been shown that uniform power distribution can be achieved when the spacing between each FET has to be of the order guide wavelength and is dependent on the phase difference of the two input signals.

I. Introduction

The conventional distributed amplifier has proven highly successful for small-signal applications. However, its success in power applications has been limited for a number of fundamental reasons such as: uneven output power distribution among the FETs [1][2], and output power wastage in the back-ward waves [3][4][5]. The first problem results in under utilisation of some of the FETs, whilst the second problem results in lowered efficiency. Even under the most ideal circumstances of zero loss: half of the output power delivered by the FETs is wasted in the backward waves to be subsequently dissipated in a termination; and the distribution of output power among the FETs is non-uniform with the FETs nearest the output terminal typically contributing the most power. In fact, over some frequency ranges, some of the FETs sink rather than source power [1].

Methods such as output line tapering [5] may be used to minimise power in the backward waves and improved circuit optimisation [2] may be used to improve the output power distribution among the FETs. However, their success is limited as the problems they aim to cure are fundamental in nature.

A variation to the distributed amplifier topology, the dual-fed distributed amplifier, has been proposed as a means to recover power in the backward waves [3][4]. The circuit diagram of the modified distributed amplifier is shown in Fig. 1 and essentially involves a dual-feed at both the input and output lines. Briefly, the input signal is fed to both ends of the input line using a hybrid, with a view to ensure equal voltages at the drains of the FETs. Power delivered to both ends of the output line is then combined using another hybrid. Despite the promise that such feeding should provide, the previous work [3][4] only considered a small-signal analysis and electrically small spacing between FETs, and did not lend insight into the operational behaviour. It is therefore the purpose of this work to investigate the operational behaviour of the dual-fed distributed amplifier and determine its optimum operating conditions. In particular, large electrical spacing between the FETs will be considered, and as will be shown, equal power distributed can be obtained with the dual-fed distributed amplifier.

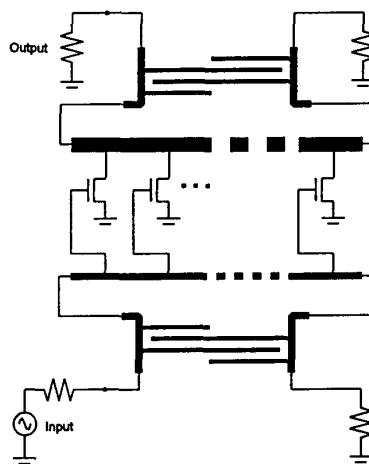


Fig. 1. Distributed amplifier variant using Lange couplers [4].

II. Dual-Fed Amplifier Analysis

In the analysis that follows, we will represent the circuit of Fig. 1 by a simplified circuit so that the salient aspects of circuit operation may be identified. As with the analysis of conventional distributed amplifiers [6], the FET input and output parasitics are absorbed into the input and output transmission lines based on the low frequency assumption for artificial transmission lines. The input coupler may be replaced by a pair of Thevenin sources representing the output signals from the input divider. The output coupler may be replaced by the loads it presents to the ends of the output transmission line. For argument sake, we will further assume that the input and output transmission line sections have equal length, both have effective characteristic impedance Z_o and propagation constant γ . The effective transmission line parameters Z_o and γ account for the effects of FET input and output parasitic parameters. It will be assumed that the couplers are both matched to Z_o at the frequencies of interest. The result of these assumptions is the equivalent circuit shown in Fig. 2.

The voltages and currents in Fig 2 are rms values and refer to signals and do not include dc bias. It will be assumed that the FETs are all identical, are operated in class A mode, and have high linearity so that the drain current of the i^{th} FET is approximately related to its gate voltage by:

$$I_{d_i} = G_m V_{g_i} \quad \dots 1$$

where G_m is the large-signal transconductance. We will assume, as many other such analyses assume, that feedback may be neglected.

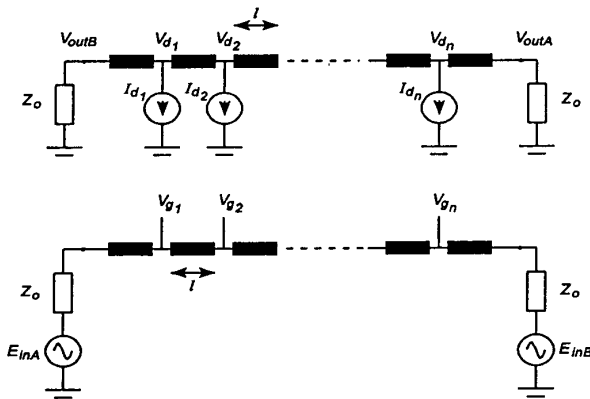


Fig. 2. Equivalent circuit of dual-fed distributed amplifier.

The amplified version of the input voltage E_{inA} will appear

at the right most output port and hence the corresponding output voltage is labelled V_{outA} . Likewise, for E_{inB} and V_{outB} . In the conventional single-fed case, E_{inB} is zero whilst in the dual-fed case, E_{inB} will be equal to $E_{inA} e^{j\phi}$ where ϕ is the phase difference between the input voltages. Both the input and output transmission lines will be effectively matched at both their ends.

We shall replace the $exp(-\gamma l)$ terms in the analysis that follows by the complex variable z (not unlike the delay variable z in sampled data systems). The gate voltages will therefore be related to the input voltages:

$$\begin{bmatrix} V_{g_1} \\ V_{g_2} \\ \cdot \\ \cdot \\ V_{g_n} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} z & z^n \\ z^2 & z^{n-1} \\ \cdot & \cdot \\ \cdot & \cdot \\ z^n & z \end{bmatrix} \begin{bmatrix} E_{inA} \\ E_{inB} \end{bmatrix} \quad \dots 2$$

and the total drain voltages will be related to the gate voltages by:

$$\begin{bmatrix} V_{d_1} \\ V_{d_2} \\ V_{d_3} \\ \cdot \\ \cdot \\ V_{d_n} \end{bmatrix} = \frac{-G_m Z_o}{2} \begin{bmatrix} 1 & z & z^2 & z^3 & \dots & z^{n-1} \\ z & 1 & z & z^2 & \dots & z^{n-2} \\ z^2 & z & 1 & z & \dots & z^{n-3} \\ \cdot & \cdot & \cdot & \cdot & \dots & \cdot \\ \cdot & \cdot & \cdot & \cdot & \dots & \cdot \\ z^{n-1} & z^{n-2} & z^{n-3} & z^{n-4} & \dots & 1 \end{bmatrix} \begin{bmatrix} V_{g_1} \\ V_{g_2} \\ V_{g_3} \\ \cdot \\ \cdot \\ V_{g_n} \end{bmatrix} \quad \dots 3$$

similarly, the output voltages will be:

$$\begin{bmatrix} V_{outA} \\ V_{outB} \end{bmatrix} = \frac{-G_m Z_o}{2} \begin{bmatrix} z^n & z^{n-1} & z^{n-2} & \dots & z \\ z & z^2 & z^3 & \dots & z^n \end{bmatrix} \begin{bmatrix} V_{g_1} \\ V_{g_2} \\ \cdot \\ \cdot \\ V_{g_n} \end{bmatrix} \quad \dots 4$$

Equations (3) and (4) account for the fact that each drain current source causes waves to propagate in both directions along the output transmission line, and hence, the total voltage at a given point on the output transmission line will be a

superposition of a number of wave voltages each attributed to a drain current source. If E_{inA} and E_{inB} have equal magnitude, then from (2) and (4) we see that V_{outA} and V_{outB} will have equal magnitude and phase difference equal to the phase difference between E_{inA} and E_{inB} . Equation (3) is important as it allows one to determine values of z so that the drain voltages are equal.

Finally, the output power by the i^{th} drain current source is given by:

$$P_{out_i} = \text{Re}(-V_{d_i} I_{d_i}^*) \quad \dots 5$$

III. Numerical Results and Discussion

In this investigation, it is further assumed that the transmission lines are lossless and hence z will lie on the unit circle and have an argument of $-\beta l$ where β is the effective phase constant of the transmission lines. In the analysis Z_o was set to 40Ω and G_m was set to 50 mS , giving $G_m Z_o / 2$ equal to unity; and the input voltage magnitudes were both set to unity. We considered a 4-stage ($n = 4$) amplifier of which output powers and output voltages were calculated as a function of βl for the case of in-phase inputs (Fig. 3) and quadrature phase inputs (Fig. 4). The numbering of the traces in Figs. 3b and 4b correspond to the FET numbering with 1 being the left most FET and 4 being the right most FET.

For the case of equal phase inputs, Fig. 3 reveals that the output voltages (and hence load power) will be maximum, and the FET output powers equal, for βl equal to integer multiples of 2π . Under this condition, the total load power to total input power is 6dB greater than the single ended case, as predicted in reference [3], and illustrates the ability of this configuration to utilise power in both the forward and backward travelling waves.

For the case of quadrature phase inputs, Fig. 4 reveals the output voltages (and hence load power) will be maximum, and the FET output powers equal, for βl equal to integer multiples of π . However, in this case, the maximum load power is 3dB lower than for the in-phase case. It is interesting to note that the output voltages vary by only 3dB with respect to βl for the quadrature phase case compared to infinite variation for the in-phase case.

Similar observations were made for other values of n ; except that for odd n and in-phase inputs, output voltages were maximum and FET output powers were equal for βl equal to multiples of π .

It is clear from this analysis that the minimum optimum spacing between FETs will be either half or one guide-wavelength and that optimum performance can only be obtained over a narrow bandwidth. Such spacing would result in physically large circuits and the assumptions underlying the conventional approach of "absorbing" FET capacitances into the transmission lines would be inaccurate. However, these problems could be overcome by realising artificial transmission lines with periodic capacitive loading at intervals considerably less than one guide-wavelength [7]. Such lines are expected to have lower values of attenuation per unit length than in conventional distributed amplifiers where periodic lossy capacitive loading is always associated with lossy loading.

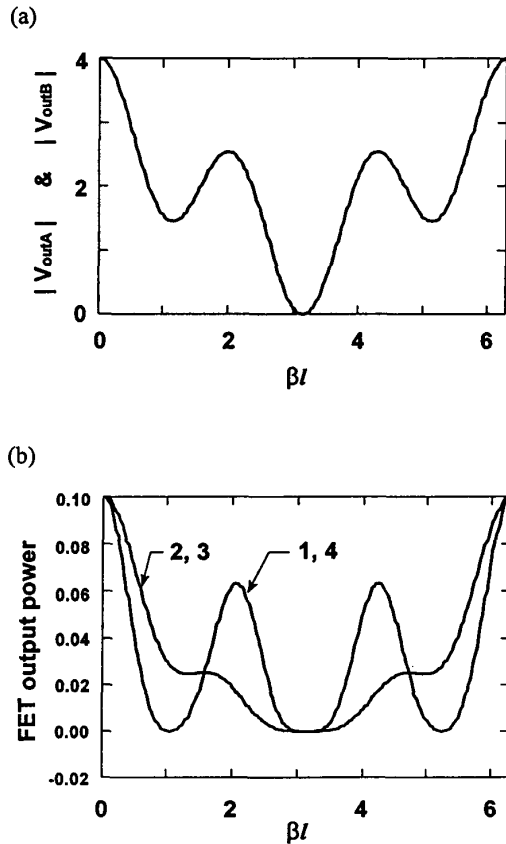


Fig. 3. Output voltages and FET output powers for $n = 4$ and $\phi = 0^\circ$.

IV. Conclusion

In conclusion, we have developed equations that give insight into the operational behaviour of the dual-fed distributed amplifier and determined the conditions under which maximum load power and equal FET output power is obtained. This information has illustrated the benefits of this configuration compared to the conventional single-fed distributed amplifier and is useful in the design and operation of such amplifiers.

Work is continuing to investigate the application of the above results when realising such dual-fed amplifiers using both MMIC and hybrid MIC technologies.

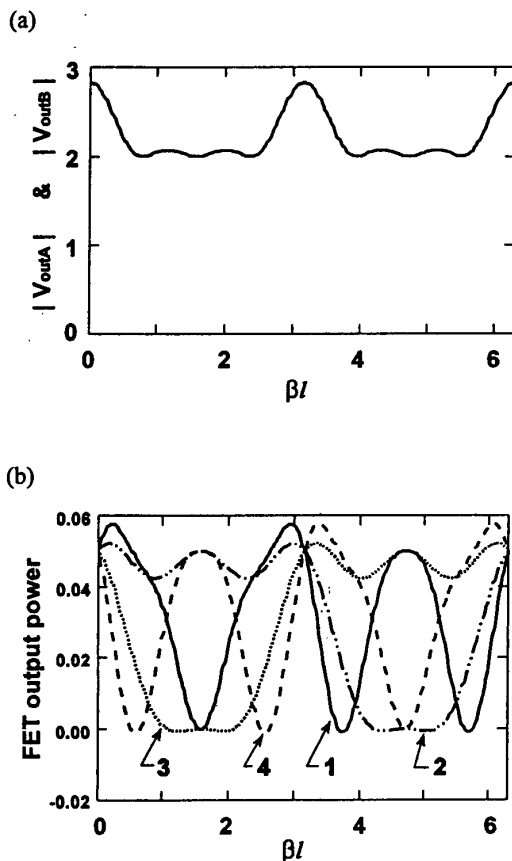


Fig. 4. Output voltages and FET output powers for $n = 4$ and $\phi = 90^\circ$.

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