The Fabrication of Metallic Nanotransistors

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***Abstract*— Extensive research studies have been devoted into the field of scaling down transistor size for ultra high density integrated circuits over the last three decades. It has been suggested that for the smallest possible scale of MOS transistor channel, a channel conductance close to that of a metal is required [1]. Metallic nanotransistors are based on field effect transistor made from metallic nanowires. This type of transistor operates by governing the flow of electrons through a narrow channel. In the fabrication of metallic nanotransistors, an electron beam lithography process has been developed to fabricate structures at the sub30nm scale using silver nanowires on SiN substrate. The single pass line exposure technique in electron beam lithography has been employed to define patterns of transistor structure as small as 20.2nm dimensions. This paper details the design and fabrication techniques of metallic nanotransistors. The limiting issues for writing sub30nm structures using EBL such as the charging effect of insulating materials, the proximity effects, and the single pass exposures are discussed.**

Keywords: Metallic FET, Y-Branch, EBL, nanotransistor

I. INTRODUCTION

In order to fabricate ultra small devices beyond the edge of optical lithography for the next decade, new types of electronic devices have been researched and explored. Metallic nanotransistors are transistor structures made from a single layer of metal with dimensions in the sub 30nm scale. The primary advantages of a metallic transistor over MOSFETs are its smaller dimensions and simple structures that require fewer fabrication steps. The one dimensional structure of metallic transistors allows the use of nanoimprint technology in terms of rapid and economical fabrications. Two types of metallic transistors have been explored and fabricated, the field-effect and the Y-branch metallic transistors.

The metallic field-effect transistor operates similarly to the depletion type MOSFETs. The current flow from source to drain is controlled by voltages apply to the side gates. Unlike conventional MOS transistors, the source-drain channels of metallic nanotransistors are made from metallic nanowires. However, the channel could also be made from semiconductor material. The operating principle of metallic field-effect transistor can be illustrated in Fig. 1. By biasing the drain and source channel, the transistor is switched on and acts as a conducting wire when there is no voltage applied to the side gates, as shown in Fig 1(a). However, when a negative voltage is applied to the side gates, electric fields that repel electrons from passing through the nanowire will be set up, and no current will flow in the channel, as shown in Fig. 1(b). It is predicted that the zero current switching will only occur when the diameter of the nanowire is close to the electron mean free path. At this stage, due to the fact that the diameter of nanowire fabricated using EBL is around 20nm, only an increase of resistance when the gate voltages are applied is expected. However, valuable information regarding conduction mechanisms in metallic nanowires will be deduced which will help in understanding the nature of carriers flow and in optimising the transistor operation and design.

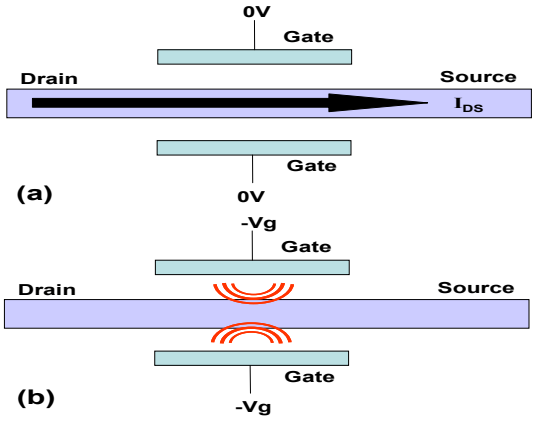

Figure 1. Operation principle of metallic field-effect transistor

The metallic Y-branch transistor was made based on the design of Y-branch switch proposed by J. J. Wesström in 1999 [2]. In the Y-branch switch design, there are two drains branching from the source, and two side gates beside each of the drains, as shown in Fig. 2. When no voltage is applied to the side gates, current will flow unimpeded through both drains, as shown in Fig. 2(a).

The switching operation of the transistor can be done by what is known as push pull operation. One side gate will have a positive voltage applied while the other has a negative voltage applied. The positive field will encourage current flow while the negative field will discourage it. When voltage is applied to the side gates, current will flow through the drain which is beside the gate which has the positive voltage applied, as shown in Fig. 2(b). The Y-branch design can also be used to

amplify signals. By steering electrons down either drain, the voltage difference between the inputs is amplified, which results a larger voltage difference between the branches [2].

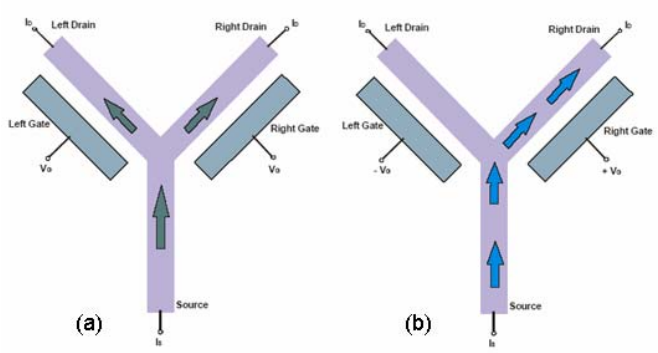

Figure 2. Operating principle of metallic Y-branch transistor

II. FABRICATION TECHNIQUES

S. V. Rotkin and K. Hess have proposed the fabrication of metallic field effect transistors (METFET) in 2004, in which the channel between drain and source were made from a metallic carbon nanotube [1]. However, the fabrication process involved in the nanotube metallic transistor is rather complicated and has low yield. A much simpler fabrication process for making metallic nanotransistor with nanowire as the drain and source channel has been developed. Due to the one-dimensional and metallic structures of this device, nanoimprint technique can be employed in terms of rapid and mass production [3] [4]. Fig. 3 shows the fabrication process of metallic nanotransistors.

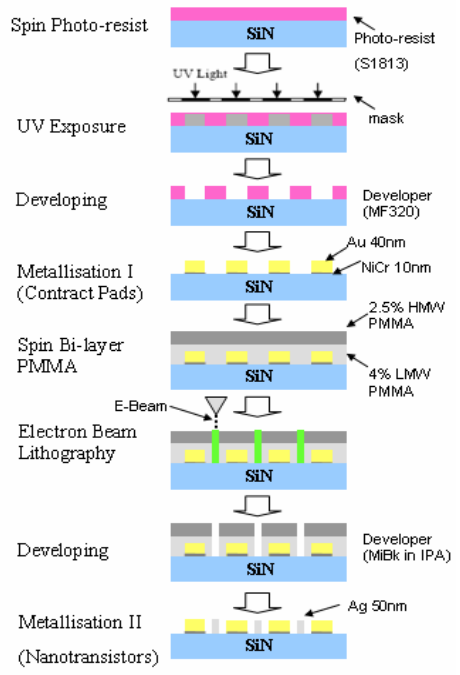

Figure 3. Fabrication process of metallic nanotransistors

The metallic nanotransistors made from nanowires are fabricated on insulting materials of SiN-coated Si substrates to ensure conduction through the metal wire only. The key fabrication techniques used for creating this type of metallic nanotransistors consist of metal deposition, photolithography, electron beam lithography, metal lift-off, and reactive ion etching. The three main steps for making metallic transistors are; contact pads creation, the EBL patterning of the nanowire, and the metallisation.

A. Contact pads creation

Fig. 4 shows the SEM image of a silver metallic transistor (middle feature) connected to a set of gold contact pad tracks. A 40nm thick Au and 10nm of NiCr were thermally evaporated onto insulating SiN substrates to form gold contact pads that facilitate electrical connections and characterisations for the device. The photolithography process for making contact pads were carried out using the MA6 mask aligner and a positive photoresist was used. Gold is the ideal material for making contact pads due to its high conductivity and resistance to oxidation. Another advantage for using gold is due to its high emission rate of secondary electrons that is especially suitable for EBL alignments. Gold contact pads tend to be more visible to the scanning electron microscope (SEM) when the EBL is carried out. This allows very accurate alignment between the nanotransistor pattern and the contact pads. Metallization was carried out using thermal evaporator and a thin layer of NiCr was pre-deposited to enhance the adhesion between the SiN substrate and the gold layer.

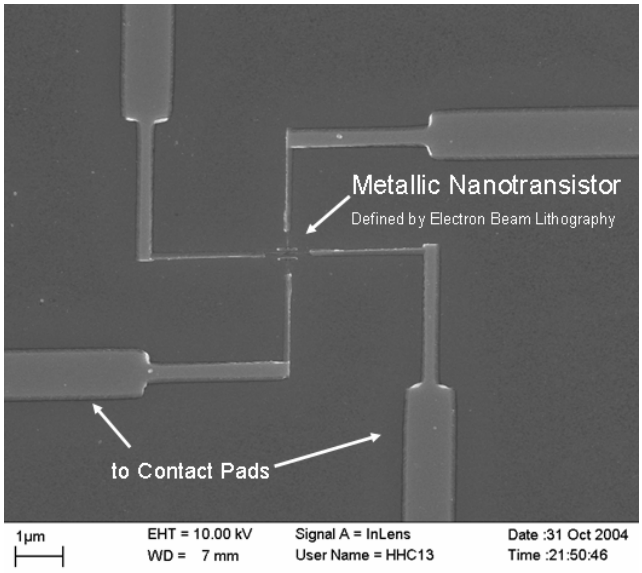

Figure 4. SEM image taken at 6,790X showing a silver metallic field effect transistor connected and aligned to the gold contact pads

B. EBL Patterning and Metallisation

The successful production of a metallic nanotransistor requires accurate alignment, high resolution pattern transfer, development that preserves the pattern, and a successful metallisation with good lift-off.

One of the most widely used techniques for fabricating ultra small devices is electron beam lithography (EBL). Unlike optical lithography techniques, EBL is capable of creating sub 20nm features on electron sensitive resists. Practically, the resolution of EBL is not limited by the beam spot size, but by the secondary electron cloud formed on the electron sensitive resist during exposure [5]. For the fabrication of metallic nanotransistors, Polymethylmethacrylate (PMMA) has been employed as a positive EBL resist, and a bi-layer PMMA scheme is used to create the undercut profile for metal lift-off [6][7]. The bottom layer was spin coated using 4wt.% solution of low molecular weight (120k) PMMA dissolved in chlorobenzen and the top layer was spin coated using a 2.5% concentration of high molecular weight (996) PMMA dissolved in xylene. A 30 minutes pre-exposure bake at 185C was performed following the application of each layer.

The RAITH-150 electron beam lithography machine was used to write and to align the transistor patterns with contact pads. A beam voltage of 10KV and an aperture of 30μm were used. The micrometer-scale alignment between the nanotransistor patterns and the gold contact pads on the substrate can be easily achieved in RAITH-150 due to its high accuracy laser interferometric stage.

Originally the patterns of metallic transistors were designed using L-Edit. In L-Edit, the finest parts of the transistors including the nanowires and gates between source and drain can only be drawn using rectangle blocks ranging from 20nm to 100nm. The exposure results have shown that the use of rectangle blocks has made the line widths of those fine structures become much wider than expected due to the proximity effect. The proximity effect is a result of backscattered electrons which lead to exposing areas of resist outside the desired area. The proximity effect has become even more obvious in this case due to the fact that rectangle areas are formed by exposing a series of single path lines in EBL. To address this problem, the GDS-2 editor in the RAITH-150 system was employed to design the finest structures of the transistor including the drain and source channel made from a 20nm wide, 800 nm long nanowire and the gate electrodes which are 20 nm wide and separated from the channel by 40nm gap. By using this CAD software, structures including the nanowire can be defined by only one single pass line in EBL. The line widths can be controlled by the actual dosage calculated in Raith-150. This allows sub 30nm lines and structures to be easily achieved on PMMA with a line dosage of approximately 500 pC/cm. This writing method has given much better results than scanning the beam using multiple line scheme where proximity effects dominates and degrade the resolution.

Once the transistor patterns have been defined on the resist, metallisation and lift-off were carried out. The choice of metallisation metal can strongly affect the functionality and performance of the device. In general, the metallisation material must have good electrical properties, strong surface adhesion, and minimum reactivity to the chemicals used in the fabrication process. Evaporation and sputtering are two common processes for metallisation. Although the lateral offers fast processing time and low temperature environment, it is not ideal for the metallisation of nanoscale patterns due to the shadowing effect. As a result, 40nm of silver was thermally evaporated forming the required nanotransistors.

III. RESULTS AND DISCUSSIONS

Originally, gold was considered to be the most appropriate material for making metallic nanotransistors due to its excellent conductivity and strong adhesion to contact pads. However, like most high-conductivity metals, they form weak adhesions to insulating materials such as SiN. In order to metallise the nanotransistor with gold, a thin layer of NiCr or titanium must be pre-deposited to promote adhesion between gold and the substrate [8]. From experiments, the deposition of two metal layers can result in greater shadowing effect on the nanoscale pattern, producing disjointed or missing metal parts on the device after lift-off, as shown in Fig. 5. As a result, gold was considered to be an inappropriate material for this device. Other metals like silver, aluminium and gold palladium have also been tried for the metallisation of this device. Among these three metals, silver has proven to be an excellent material in terms of ease of evaporation and lift-off. Fig. 6 shows the SEM image of a silver Y-branch metallic transistor.

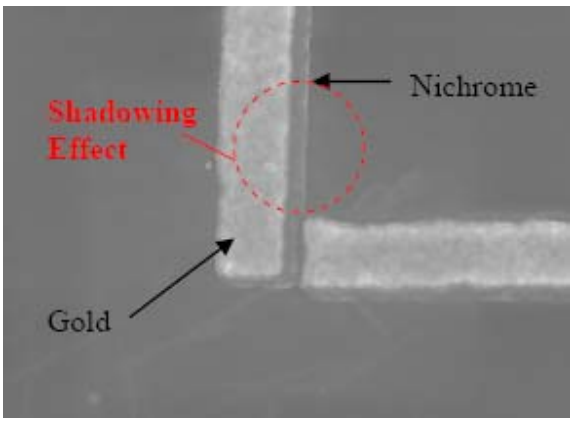

Figure 5. SEM image taken at 66,080X magnifaction illustrating shadowing effect caused by the dual evaporation of gold and NiCr

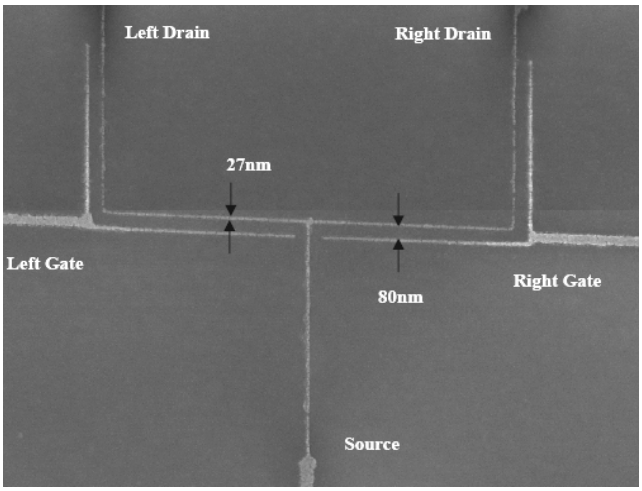

Figure 6. SEM image taken at 19,150X showing a silver Y-branch metallic transistor on SiN with drain and source branch width of 27nm

During E-beam exposure, proximity effect caused by electron scattering imposes a severe limitation on the ultimate spatial resolution attainable by E-beam lithography [9]. It has been found that, depending on the size of the patterns and nearby patterns, some parts of the bottom layer of PMMA were exposed unintentionally due to the proximity effect. To address this problem, the 20nm wide gates defined by single pass lines were made shorter (400nm long) in order to avoid severe undercut problems caused by their proximity to the 100nm wide connecting trackes and to reduce their field interference with the gate voltage.

One of the key challenges encountered while patterning the nanotransistor structure with EBL was the surface charging. The surface charging problem arises from the use of insulating material as the substrate or the lack of metal parts that could dissipate charges that remained inside the resist after E-beam exposure. The surface charging effect during EBL has been reduced by using a Si substrate with a 200nm thin layer of SiN coating. This help discharging of the beam electrons through the Si substrate. Another approach is by using a full 100mm wafer as substrate to increase the area covered by metal contact pads and to facilitate the fabrication of a higher density of transistors on a single chip.

Another solution that has greatly minimised the surface charging problem was the pre-deposition of 10 nm of tungsten onto the substrate before contact pad creation. The pre-deposition of tungsten onto the substrate was carried out using DC sputtering. For this structure, plasma etching was required to remove the tungsten layer after the metallisation and lift off process is completed. This technique has proven most effective and the finest field effect metallic transistor has been fabricated even on quartz substrate with a drain-and-source channel width of 20.2nm. Fig. 7 shows the SEM image of the metallic nanowire transistor made from silver wire 20.20 nm wide by employing a predeposited layer of 10 nm thick tungsten on highly insulating substrate of quartz.

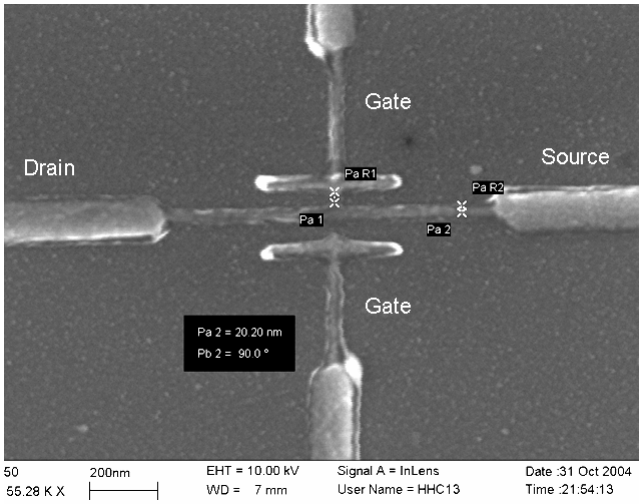

Figure 7. SEM image taken at 55,280X showing a silver field effect metallic transistor on Quartz with a drain-source channel width of 20.20nm.

IV. CONCLUSION

In order to meet the demands for the continuous shrinking of MOS transistors, new types of transistors must be explored [10]. Metallic nanotransistors with dimensions of sub 30nm are promising candidates that might be considered to replace current MOS transistors.

During the fabrication of metallic nanotransistors, surface charging and proximity effects have been encountered. The use of a tungsten layer prior to the contact pads creation has greatly minimised the surface charging effect on insulating materials during the EBL process. The single pass line exposure of finest structures of the transistor has reduced the proximity effect enabling 20 nm features to be defined and transferred to metallic structures reliably.

In this work, the field effect metallic transistor and the metallic Y-branch transistor have been successfully fabricated on insulating materials using electron beam lithography. A minimum drain-source width of 20.20nm of the field effect transistor made from silver was achieved. The electrical characterisations and testings for these devices are next to be performed. These metallic transistors are well suited for mass production due to their single level structure ideal for low cost fabrication technique such as nanoimprint lithography.

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