DISSERTATION

DEVELOPMENT OF $Cd_{1-x}Mg_xTe$ THIN FILMS FOR APPLICATION AS AN ELECTRON REFLECTOR IN CdS/CdTe SOLAR CELLS

Submitted by

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ABSTRACT

DEVELOPMENT OF $Cd_{1-x}Mg_xTe$ THIN FILMS FOR APPLICATION AS AN ELECTRON REFLECTOR IN CdS/CdTe SOLAR CELLS

Efficiencies of CdS/CdTe photovoltaic cells significantly lag behind their theoretical limit, primarily because open-circuit voltage (V_{OC}) of record efficiency cells (872 mV) is well below what is expected for the CdTe band gap (1.5 eV). A substantial V_{OC} improvement can be achieved through addition of an electron reflector (ER) layer to CdTe devices. The ER layer forms a conduction-band barrier that reflects minority-charge carriers (i.e. electrons in p-type CdTe) away from the back surface. Similar to back-surface fields in c-Si, III-V, and CIGS solar cells, the ER strategy is expected to reduce back-surface recombination and is estimated to increase CdTe V_{OC} by about 200 mV based on numerical simulation.

The presented research investigates the addition of a thin layer of wider band gap $Cd_{1-x}Mg_xTe$ (CMT) to achieve a CdTe ER structure. First, a novel co-sublimation process was developed for deposition of $Cd_{1-x}Mg_xTe$ thin films that demonstrates excellent experimental capabilities, commercial viability, and improved alloy control over other techniques. Next, the effects of processing on material properties of CMT deposition onto CdS/CdTe structures were investigated. It was discovered that substrate temperature during CMT deposition is a critical parameter for achieving uniform CMT film coverage on polycrystalline CdTe. Furthermore, CMT film growth was found to be epitaxial on CdTe where the CMT films retain the same microstructural features as the underlying CdTe grains. Despite film uniformity, significant Mg loss from the CMT film, oxide formation, and a reduction of the optical band gap was found after $CdCl_2$-based passivation treatments. Preliminary process optimization found that band gap degradation can be minimized by utilizing $MgCl_2$ in addition to $CdCl_2$ as a treatment source material. Finally, development of CdS/CdTe/$Cd_{1-x}Mg_xTe$ electron reflector devices demonstrated a barrier behavior at high voltage bias and improved voltage when CdTe thickness is held below 1 μm. Additional electro-optical characterization and device

modeling was used to understand the source of this device behavior. The results suggest the $CdTe/Cd_{1-x}Mg_xTe$ interface is likely free of detrimental electronic defects and the barrier behavior comes from a larger than expected valence band offset for the material system. Finally, future work to improve ER device performance is suggested.

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Chapter 1

Motivation

1.1 Current Energy Picture

The relatively recent prosperity of humans can be directly attributed to their ability to capture, harness, and use energy. From development of controlled use of fire during the Early Stone Age to the ubiquitous use of fossil fuels today, humans have relied on energy to improve their lives. Expanded use of fossil fuels (coal, petroleum, and natural gas) as an energy source began in earnest during the mid 20th century (see Fig. 1.1), when energy from petroleum and natural gas started to become abundant after World War II. The boom in energy consumption corresponds closely to a large population boom (see Fig. 1.2). The availability of energy enabled improvements in water quality, sewage, medicine, and food production which led to population growth worldwide and thus more fuel consumption.

A deeper look into current energy use and generation in the US (see Fig. 1.3) reveals that about 40% of total energy is used for electricity generation, while the rest is used primarily for transportation and directly in industrial, commercial, and residential applications. Of the energy spent for electricity production, 67% comes from fossil fuels. Solar generated energy makes up just 0.1% of total energy generation and 0.25% of electricity generation. Although solar energy generation share is quite small, it has been increasing substantially over the last decade [2].

By all indications, the global supply of energy from fossil fuels will not run out in the near future. Despite increasing world population and increasing per capita energy consumption, fossil fuels reserves are expected to meet those demands. In fact, fossil fuel reserve access and extraction methods are improving, leading to continuous supply for several lifetimes. In this case, the energy supply is not a significant problem for the human population. Notwith-

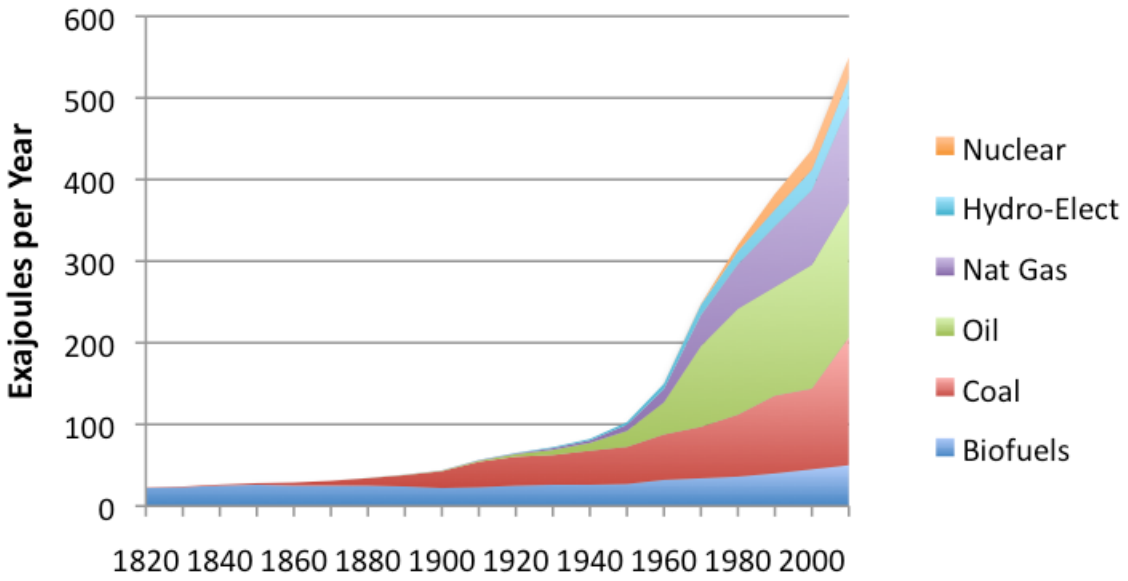

Figure 1.1: World energy consumption by fuel type by year. Figure reproduced from Ref. [1].

standing, the energy security provided by fossil fuels comes with environmental costs that can be detrimental to continued survival and prosperity of humans and many other species.

1.2 The Case for Renewable Energy

The use of fossil fuels has led to significant short term changes on our planet. The changes are both local, impacting our direct environments, and global, impacting worldwide weather patterns and climate. The environmental and climate impacts of fossil fuel use have been studied extensively and reveal severe implication to human health, food production, and sever weather patterns.

It is well known that burning fossil fuels can produce significant air and water pollution locally. As just one example, high air pollution from coal-burning power plants in northern China have significantly reduced life expectancy of people in that region [3, 4]. People in the northern region of China have life spans an average of 5.5 years lower compared to people living in less polluted southern China. The decrease in life expectancy are attributed to higher cardiorespiratory diseases and similar health issues associated with air pollution.

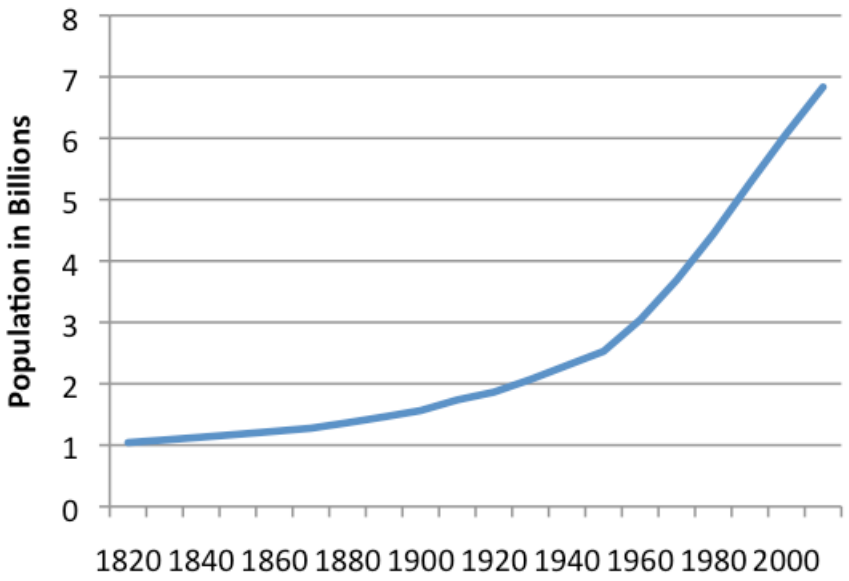

Figure 1.2: World population by year. Figure reproduced from Ref. [1].

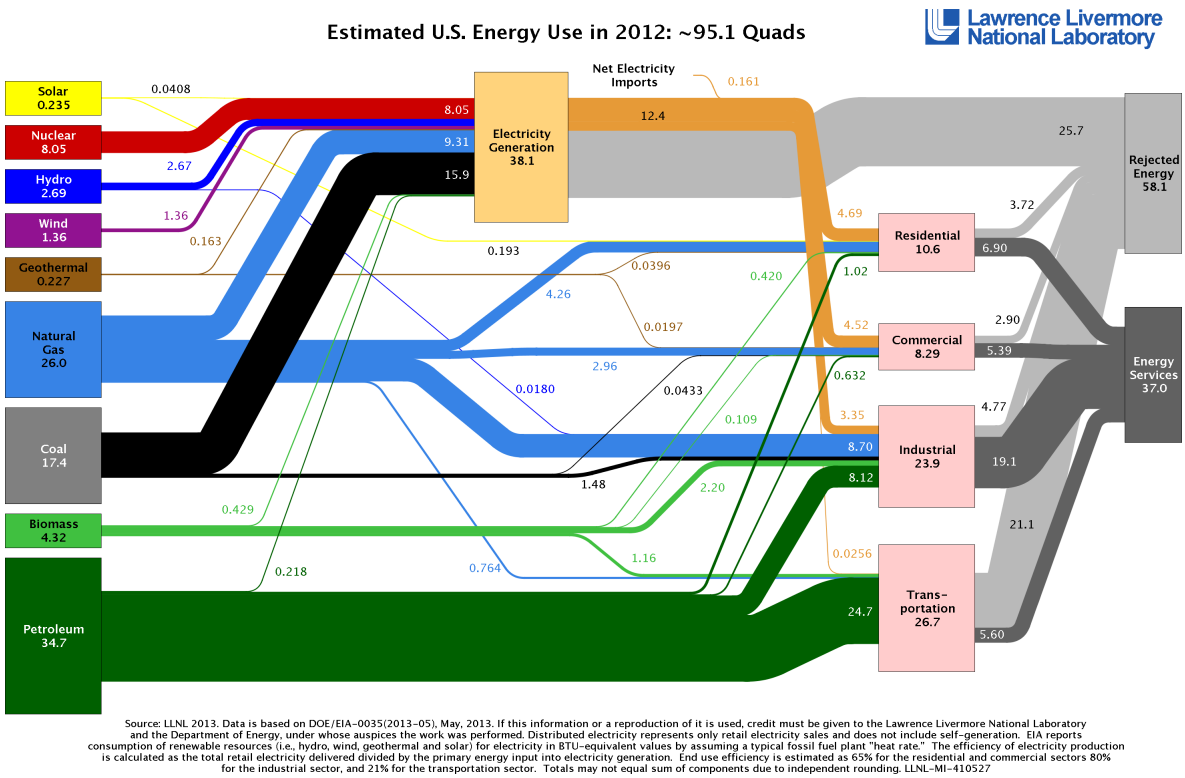

Figure 1.3: 2012 US energy use and generation. Figure reproduced from Ref. [2].

The increase in pollution related health problems in the northern China is correlated to concentrations of air particulates in the region. The particulates are a by-product of coal burning in power plants and as a heat source in residential application. The locally occurring problems, such as this example from China, are small in comparison to the global effects of fossil fuels on our planet.

The impact of fossil fuel use on our global environment has become increasingly apparent in the last decade. As climate scientists study our atmosphere, a correlation between greenhouse gasses (GHGs) in our atmosphere and average world temperature can be made. GHGs are gasses present in our atmosphere that can generally transmit most solar energy from the sun, which is in the near ultraviolet (UV), visible, and near infrared (IR) ranges, but absorb thermal energy emitted by the Earth's crust, which is in the mid to far IR range. The presence of GHGs, such as water vapor, carbon dioxide, methane, etc., in our atmosphere has benefits, as it keeps Earth warm enough to be habitable. Increasing the concentration of GHGs, however, increases the greenhouse effect and increases atmospheric temperatures. The correlation between CO_2, the major by-product of fossil fuel use, and temperature levels over the last millennium is captured in Fig. 1.4 [5]. The large increase of CO_2, starting around year 1850, is consistent with growing fossil fuel use at that time (see Fig. 1.1). After a few decades, the increased CO_2 concentration begins to raise atmospheric temperature (around year 1900). As of this publication, CO_2 concentrations have surpassed 400ppm in our atmosphere [6] and temperatures are rising dramatically [7].

Rising CO_2 levels and temperature produces significant challenges of human survival. For example, the changing climate can produce more severe weather patterns and significantly disrupt food production. A warming planet will see significant rise in sea levels, endangering low lying areas with flooding, and increases in severe storms, leading to property destruction. Extremely high levels of CO_2 could make breathing difficult for most humans, further affecting their health. Although humans may learn to adapt to their changing world, the cost of these changes could be catastrophic. Billions of humans could die from famine as food production is impacted by climate. Large populations will be displaced from low ly-

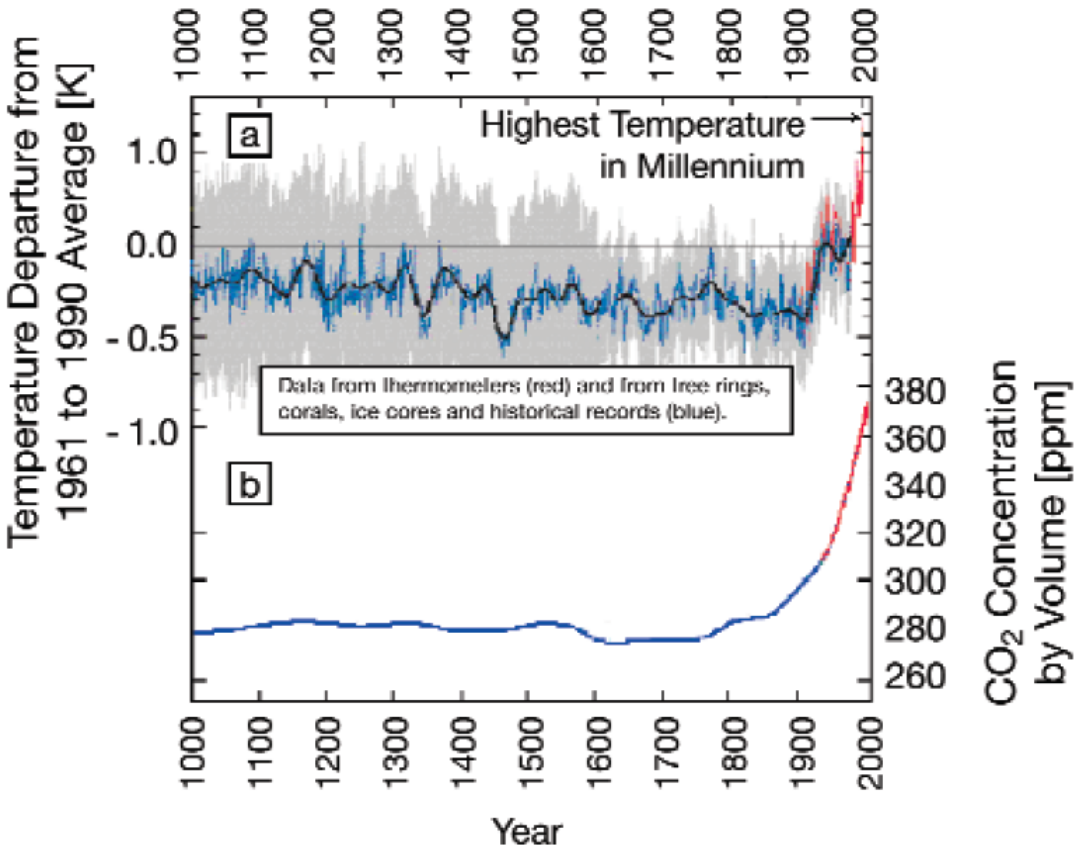

Figure 1.4: Temperature and CO_2 levels over the last millennium. (a) Temperature data from thermometers (red) and from tree rings, corals, ice corals, and historical records (blue); (b) CO_2 data from Mauna Loa Observatory, HI (red) and ice core records (blue). Figure reproduced from Ref. [5].

ing coastal areas, causing significant stress on our infrastructure. To alleviate some of these problems, energy sources that do not produce GHGs are needed to replace fossil fuels. These sources, such as solar, wind, geothermal, and hydropower, are characterized as "renewable energy", due to their ability to produce emission-free energy from sources that will not cease to exist.

Despite our changing climate, the sun will shine everyday, rivers and oceans will continue to flow, the Earth's core will continue to be hot, and winds will continue to blow. These energy sources can be captured and used by our population without adding GHGs to the atmosphere. Despite the benefits, these renewable energy sources are often expensive and

intermittent. The worldwide adoption of these energy sources depends greatly on humans' ability to reduce renewable energy implementation costs, finding methods for large-scale energy storage, and development of an agile grid able to cope with supply intermittency.

1.3 Role of CdTe Photovoltaics in Our Energy Future

As described in Section 1.2, renewable energy sources are needed to reverse the course of climate change. However, the amount of energy the renewable energy sources can provide can also be limited by their inherent potential. For example, there is a finite amount of rivers and accessible oceans in the world to develop hydropower, thus reducing the potential of this resource. Solar energy, specifically photovoltaics (PV) for electricity generation, has the greatest potential of all renewable energy sources primarily due to the abundance of sunshine on a daily basis. In fact, the potential of PV is so large that a relatively small fraction of land-mass is needed to provide for all our energy needs [5].

The cost of electricity from PV technology implemented at large scale is also competitive with traditional fossil fuels. The Levelized Cost of Energy (LCOE) is a cost metric of the total produced energy (in cents per kilowatt-hour) over the life of a PV power plant. In recent years, the LCOE for PV technologies has dropped significantly (see Fig. 1.5) and is expected to continue to reduce further in the next decade [8]. Even at current levels, the LCOE of PV systems is competitive with current electricity prices. For example, large scale PV power plants in southwest United States have demonstrated grid parity [9].

There are numerous types of PV technology, however, crystalline-silicon (c-Si) PV technology currently dominates the market. This is in part due to the longer development time of silicon semiconductor devices, which resulted in c-Si devices being better understood and a allowing for well-developed manufacturing processes to be put in place. For these reasons, c-Si PV dominates over thin-film PV (such as CIGS and CdTe), which are not as well understood and which do not have as much manufacturing infrastructure in place. Despite less understanding, thin-film CdTe PV can be produced at lower cost compared to c-Si [8].

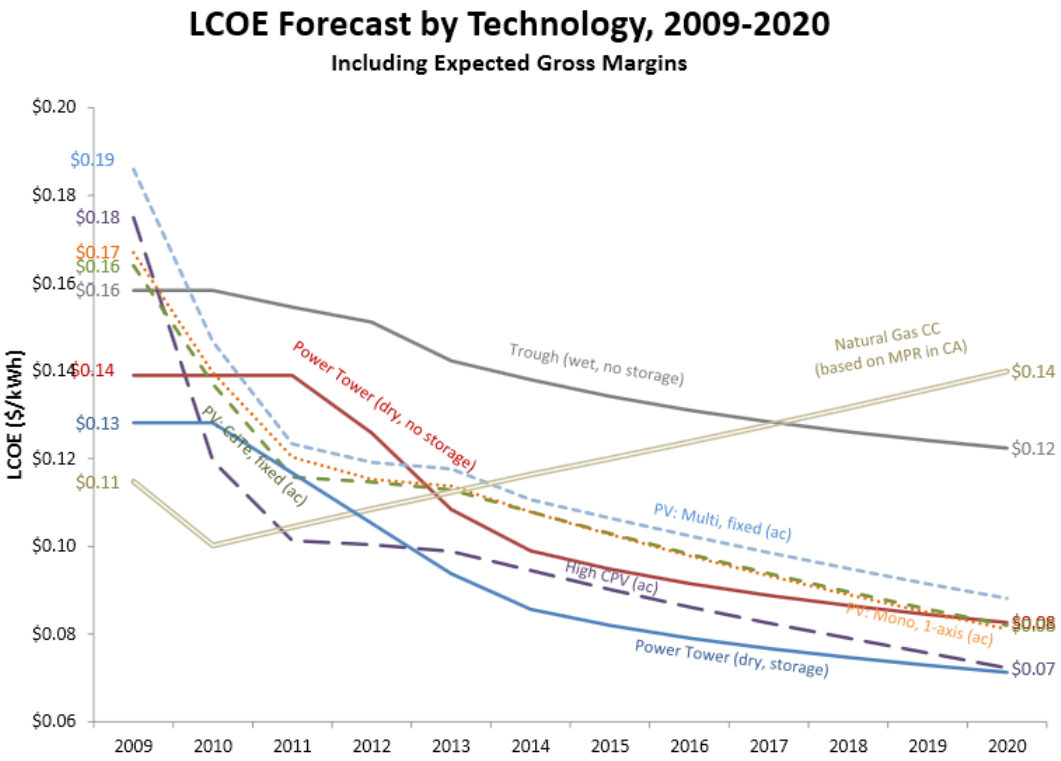

Figure 1.5: LCOE Forecast by Technology, 2009-2020. Figure reproduced from Ref. [8].

The lower costs of thin-film PV comes from several factors. First, CIGS and CdTe PV materials have higher absorption coefficients than c-Si, thus requiring almost 100 times less thickness. Thin-film absorbers require less raw materials, saving costs, but also allow for a lower quality of material to be used, as charge carriers have less distance to travel. Furthermore, thin-film PV absorbers (such as CdTe) can be deposited directly on low-cost front glass. This process reduces assembly costs found in c-Si module manufacturing. Furthermore, thin-film modules can be manufactured in continuous, in-line systems with significant automation, which further reduces costs and provides large throughput.

Of the thin-film PV technologies, CdTe has the lowest cost to manufacture. The advantage comes from a wide array of possible deposition processes [10] and lower complexity than other thin films (e.g. CIGS and III-V cells). Another benefit of CdTe PV is its ideal band gap match to the solar spectrum [11]. Due its band gap, CdTe can produce the highest

theoretical efficiency of single-junction solar cells. Currently, however, record CdTe cell and module efficiencies are significantly lower than the theoretical limit [12]. The already low-cost, and competitive, processing of CdTe modules and high efficiency potential make CdTe solar cells an ideal PV technology for large scale implementation and energy generation. CdTe PV technology could be a transformative renewable energy solution to our long term energy needs.

1.4 Paths to Improve CdTe PV Efficiencies

There are several possible methods to improve efficiency of CdTe-based PV cells and modules. Figure 1.6 shows the CdTe device structure roadmap developed by Colorado State University's Center for Next Generation Photovoltaics. Improvements in CdTe efficiency can be realized in multiple ways. For a single junction CdTe device, a more transparent glass, front contact, buffer, and window layers can be used to improve the short-circuit current of the device. Additionally, an electron reflector layer could be added to the back of CdTe to improve open-circuit voltage of single junction devices. Combining these two changes is expected to improve single junction CdTe efficiencies to 20%. Further development of multi-junction CdTe based solar cells are expected to improve efficiencies to 30%.

One important aspect of developing these more efficient CdTe device structures is to preserve the low-cost manufacturing of CdTe modules. By improving the efficiency of CdTe cells and modules with relatively small changes to processing, manufacturing costs can be further decreased and PV fields can be made smaller while perserving the desired energy production level. These improvements can provide a dramatic impact to the energy picture by enabling CdTe PV to become a major source of energy.

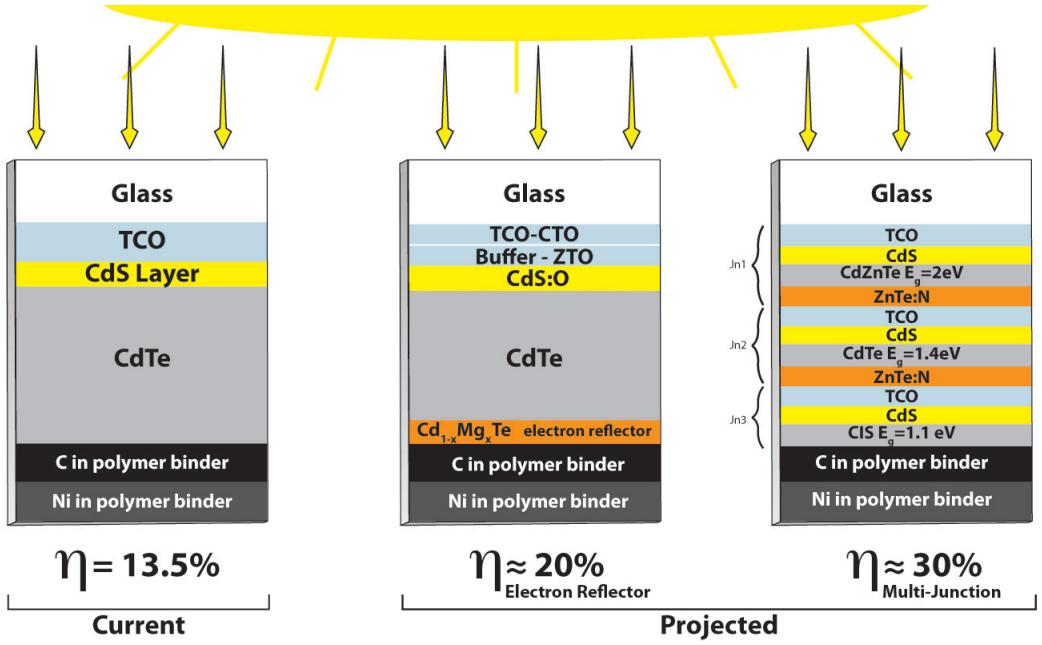

Figure 1.6: CdTe device structure efficiency roadmap developed by the CSU's Center for Next Generation Photovoltaics.

1.5 Contributions of This Work

This dissertation focuses on improving CdTe solar cell efficiency with minimal changes to processing. Specifically, the dissertation investigates the use of thin-film $Cd_{1-x}Mg_xTe$ as an electron reflector (ER) layer in CdTe solar cells to improve efficiency. In order to achieve this novel device structure, several significant development steps are needed. First, a production-ready manufacturing process for deposition of $Cd_{1-x}Mg_xTe$ thin films was developed. Once the deposition method was optimized, deposition of CMT thin films onto CdTe was investigated and effects of passivation treatment were analyzed. Finally, CdS/CdTe/CMT ER devices were fabricated and analyzed. This manuscript presents the process development, thin-film material properties, and device results.

This dissertation is split into chapters describing different aspects of the research. Chapter 2 introduces the electron reflector concept, provides examples of similar structures in other PV devices, and discusses selection of $Cd_{1-x}Mg_xTe$ as the electron reflector layer. In

Chapter 3, a novel deposition method for formation of the $Cd_{1-x}Mg_xTe$ thin film is presented and results of film characterization are discussed. Chapter 4 focuses on deposition of CMT films onto CdS/CdTe structures and investigates the CdTe/CMT interface. Passivation treatment effects of $Cd_{1-x}Mg_xTe$ thin films is presented in Chapter 5. Chapter 6 shows results of developed CdS/CdTe/$Cd_{1-x}Mg_xTe$ ER structures and investigates their electronic behavior. Finally, the work presented in this manuscript is summarized in Chapter 7 and future work is suggested.

For readers looking for additional background information, a detailed background section is provided in Appendix A. This section includes information on PV device physics, device operation, electro-optical characterization, material characterization, a general description of CdS/CdTe PV devices, and introduction to manufacturing methods used at Colorado State University. Appendix B provides parameters used for computational modeling of ER structures.

Chapter 2

Introduction: The Electron Reflector Strategy

2.1 The Electron Reflector Concept

The n-CdS/p-CdTe photovoltaic cell structure has significant advantages to its counterparts. The CdTe absorber has an almost ideally matched band gap ($E_g \approx 1.5$ eV) to our solar spectrum and has a high CdTe absorption coefficient, greater than 1×10^4 cm^{-1}, for photon energies above the band gap [13]. Due to the high absorption coefficient, a CdTe thin film of only a few micrometers is needed to absorb virtually all of the solar spectrum above the band gap. This low material utilization, coupled with numerous low-cost methods to deposit and treat these films [10] and continuous production of stable modules [14, 15], has accelerated the adoption of CdS/CdTe solar cells. CdTe module production also experiences the lowest energy payback and emissions compared to other PV technology [16, 17].

There are, however, disadvantages to CdTe PV that have restricted its growth, the primary being lower module efficiency compared to c-Si PV. Record CdTe module efficiency of 16.6% significantly lags behind that of c-Si (22.9%), mc-Si (17.85%), and single junction GaAs (21.1%) [12]. Additionally, CdTe module efficiencies lag significantly behind efficiencies of record laboratory cells, primarily due to poor current and fill factor [11, 12, 18]. Furthermore, record-efficiency laboratory CdTe cells lag behind the theoretical limits for CdTe absorber films [11, 19], primarily due to deficiencies in open-circuit voltage, V_{OC}. The V_{OC} of record efficiency cells (0.872 V) is significantly below what is expected for the CdTe band gap (1.5 eV). The electron reflector strategy aims to increase the voltage of the CdS/CdTe solar cell by creating a back-surface field inside the device and reducing the recombination

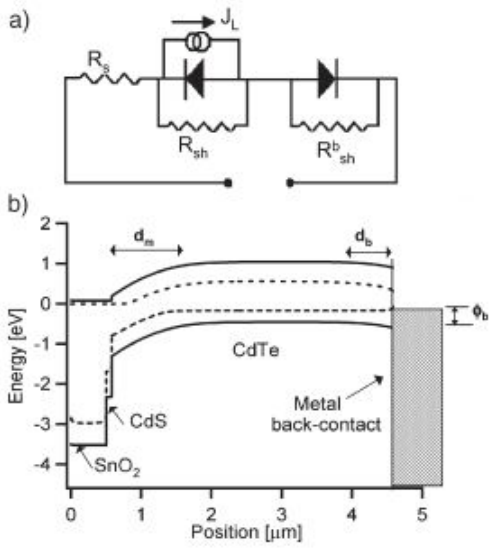

Figure 2.1: (a) Two-diode equivalent circuit model, and (b) band diagram of two non-interacting diodes in the light at zero bias, showing blocking barrier ϕ_b. Figure from Ref. [20].

at the back surface.

One primary mechanism for efficiency losses in CdS/CdTe devices has been associated with back-surface recombination between the CdTe film and the back electrode. This interface often forms a Schottky barrier with a blocking valence-band barrier, ϕ_b. The back-surface barrier has been modeled using a non-interacting two-diode model (Fig. 2.1), where minor variations in ϕ_b have indicated changes in fill factor but not open circuit voltage [20]. Generally, when the minority-carrier diffusion length, L_n, is smaller than thickness of the absorber, d, as is the case in $p-$type CdTe ($L_n \approx 0.43$ μm [21]; $d \approx 1$ - 8 μm), it is assumed that the back-contact recombination is negligible to device performance. However, additional simulations where the front and back diodes can interact indicate that increases in ϕ_b produce incremental decreases in V_{OC}, even when $L_n < d$, because of an increased back-contact recombination current [22]. Device changes that decrease the back-surface recombination should, therefore, increase the V_{OC} of the CdTe device.

2.1.1 How Does an Electron Reflector Improve Voltage?

There have been several suggestions on how to improve open circuit voltage of the CdS/CdTe solar cell. For example, one idea is to increase the majority carrier concentration of both the CdS and CdTe by one order of magnitude each, which is expected to improve the V_{oc} by over 100 mV [19]. Another idea is to reduce the back-surface recombination velocity, S_b, by implementing a back-surface field (BSF). The BSF creates a conduction-band barrier to the electron flow in forward bias [23–25]. In solar cells where $L_n > d$, such as Si-based PV cells, this built-in field increases the collection probability of carriers generated near the back surface by driving these carriers away from the back contact and, therefore, reduces recombination velocity and improves both V_{oc} and J_{sc}. In cells where $L_n < d$, such as CdTe cells, the BSF will allow the formation of thinner, fully depleted absorbers by also driving generated carriers away from the back contact and thus decrease back-surface recombination velocity and improving V_{oc}. This latter case is similar to an $n-i-p$ structure since the entire cell is under an electric field. In recent years, the BSF strategy in CdTe thin-film solar cells has been referred to as an electron reflector (ER). This nomenclature is more descriptive of how the BSF improves the CdTe device.

A schematic of the ER structure in a CdTe solar cell is given in Fig. 2.2. The conduction-band barrier shown in Fig. 2.2c, with height ϕ_e, is the primary definition of the electron reflector. At zero bias (Fig. 2.2a), the built-in field in the depleted region forces generated charge carriers (i.e. electrons in the conduction band) away from the back surface. However at forward bias, V in Fig. 2.2b, the field is reduced and more carriers can now approach the back surface and recombine. The electron reflector structure (Fig. 2.2c) creates a conduction-band barrier to the generated minority-carrier electrons, thus reducing the probability that they will drift to the back surface and recombine, even at forward bias.

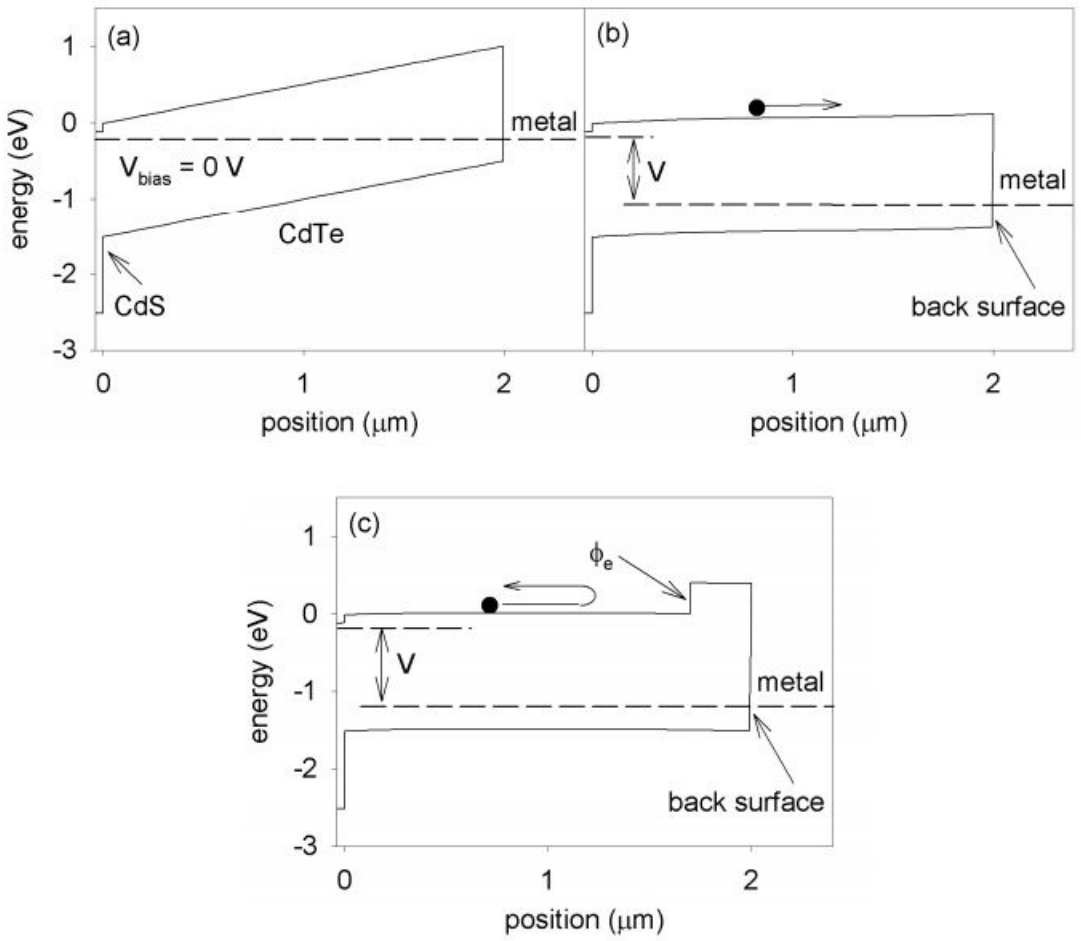

Figure 2.2: Band diagrams of a baseline CdTe solar cell at (a) zero bias and (b) V_{bias}=V. (c) The band diagram of a CdTe cell with an electron-reflector layer at the back surface. Figure from Ref. [26].

2.1.2 Comparison of Mechanisms to Create an Electron Reflector

There are three primary ways to create an ER structure in a CdTe device. For convenience, they are shown in Fig. 2.3. The first is to use an expanded band-gap film (Fig. 2.3a) where the ER film has a higher band gap than the bulk absorber. It is important that the increase is primarily in the conduction band and a barrier in the valence band is reduced. This mechanism to form an ER layer can be achieved by either (a) increasing absorber band gap at the back of the device or (b) reducing the bulk absorber band gap while keeping the band gap of a back-surface layer unchanged. Changing CdTe band gap (up or down) can

Figure 2.3: Schematics of mechanisms to create an electron reflector: (a) expanded-band-gap layer, (b) reversed back barrier, and (c) heavily-doped back surface. Figure from Ref. [26].

be accomplished by alloying CdTe thin films with magnesium, manganese, zinc, or mercury. A detailed discussion of selecting the appropriate alloy is presented in Section 2.2.1 of this manuscript, while a detailed review of alloying techniques is presented in Section 2.2.3. Without changing band gap, one can create a conduction-band barrier by bending the bands at the rear of the device. Such mechanisms include reversing the back-contact barrier (Fig. 2.3b) and creating a heavily-doped back surface (Fig. 2.3c).

The reversed back-contact barrier strategy is easily understood by comparing the direction of the back-barrier in typical cells (ϕ_b in Fig. 2.1b) to the band diagram shown in Fig. 2.3b. Making a reversed back-contact barrier requires a metal contact with a higher work function than the relatively high work function of the CdTe absorber. Historically, finding a back metal with high enough work function has been difficult [10]. Recent developments have shown that non-metal films, such as MoO_x [27], could be used to make this contact.

A heavily-doped back surface of the CdTe device increases the carrier density, ρ, at the back of the device. An example of this is already in practice. The standard method of forming a CdTe back contact typically uses selective etching to form a Te-rich layer, which is then reacted with Cu. This forms a p^+ Cu_xTe layer that is then contacted with a metal or graphite [10]. The doping increase from CdTe to Cu_xTe is not very large, but is effective in reducing some of the back-contact recombination. Simulations of the heavily doped back surface structures have indicated that a higher doped back surface can improve the V_{oc} when the lifetime is relatively good [26, 28]. However, achieving higher doping levels in $p-$type CdTe is problematic because it is heavily compensated.

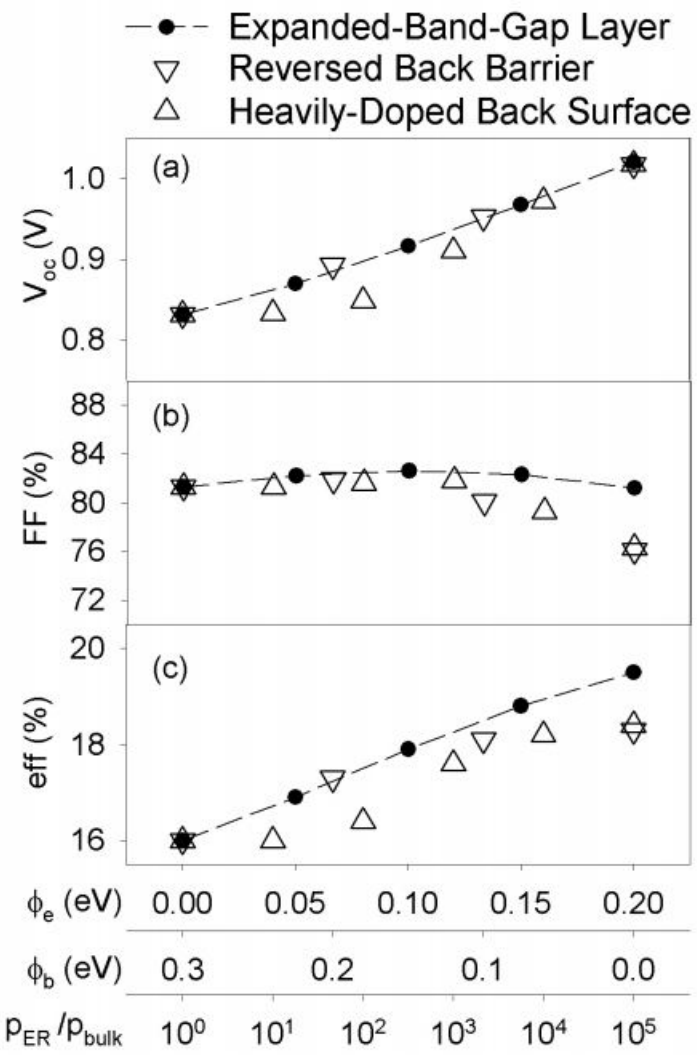

Figure 2.4: Comparison of the three electron-reflector mechanisms. Fits shown are for the expanded-band-gap strategy. Figure from Ref. [26].

A comparison of these ER mechanisms was made by K. J. Hsiao [26] and is shown in Fig. 2.4. This figure shows the V_{OC}, FF, and efficiency, η, of the three mechanisms against their respective parameters: ϕ_e for an expanded band gap, ϕ_b for a reversed back barrier, and carrier density ratio ρ_{ER}/ρ_{bulk} for the heavily-doped back surface. The figure indicates that the expanded-band-gap strategy is the best in improving both the voltage and the efficiency of the device. The expanded-bang-gap strategy is also the easiest to implement, since alloying CdTe for higher band-gap is well established (see Section 2.2.3) and only a small conduction-

band barrier of 0.20 eV is needed. The other mechanisms require unrealistic changes in the CdTe material, such as doping the back-surface five orders of magnitude higher or finding a material with a higher work function than CdTe. For these reasons, the expanded-band-gap mechanism is the main focus of implementing the ER strategy.

2.1.3 Examples of ER Structures in Photovoltaics

Examples of photovoltaic structures with back-surface fields have existed for a few decades. Furthermore, examples of BSF structures exist in both crystalline silicon (c-Si) and thin-film Cu(In,Ga)Se_2 and group III-V solar cells.

The BSF technique has been used to improve efficiency in c-Si solar cells since the 1970s [23–25, 29]. Because changing the band gap of Si wafers is typically difficult, BSFs in c-Si utilizes the heavily-doped back surface mechanism (Fig. 2.3c). The $n^+ - p - p^+$ structure of the c-Si BSF cell, where the p^+-layer forms the BSF, passivates the back contact and reduces back-surface recombination [30]. Different arrangements of c-Si with a BSF layer are shown in Fig. 2.5. The p^+ BSF layer can be made with either aluminum or boron doping. In the former, an aluminum paste is screen printed onto the device and diffused into the c-Si wafer by thermal annealing. Similarly, boron doping is accomplished by thermal diffusion [30] or by treatment with boric acid [31]. Another example of a c-Si BSF solar cell is in the popular HIT cell made by Sanyo. The HIT (Heterojunction with InTrinsic layer) cell uses $n-$type c-Si as the absorber and amorphous silicon layers (a-Si) as the $p-$type window layer and an n^{++} layer as the BSF layer [32]. The HIT cell has improved interface passivation due to the use of intrinsic a-Si layers between the doped a-Si layers and the c-Si wafer (see Fig. 2.6). Amorphous Si, and more recently micro-crystalline silicon (μc-Si) [33], can be easily used as a BSF layer for both $n-$ and $p-$type c-Si cells. Regardless of how they are implemented, back-surface fields in c-Si solar cells are necessary to achieve efficiencies close to their theoretical limits.

For Cu(In,Ga)Se_2 solar cells, the formation of a BSF may not be as deliberate as in c-Si, but is just as useful. Research has suggested the BSF in Cu(In,Ga)Se_2 cells is formed by

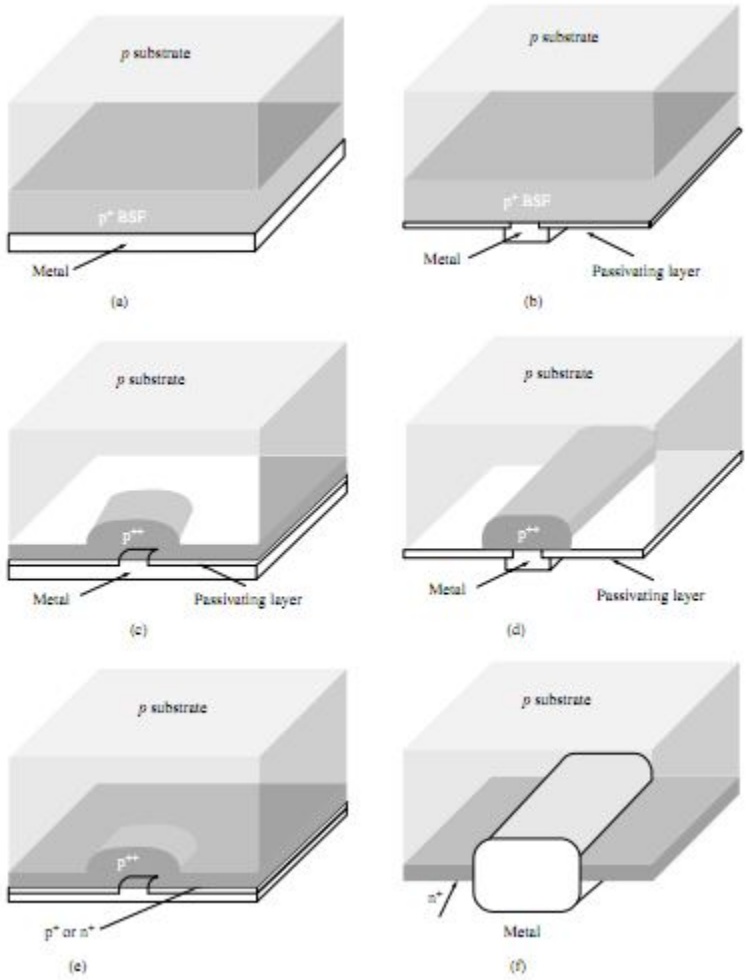

Figure 2.5: Rear contact structures: (a) continuous BSF; (b) bifacial cell; (c) local BSF; (d) local BSF, bifacial cell; (e) selective emitter or floating junction passivation; and (f) shorted junction at the back face of industrial cells. Figure from Ref. [30].

band gap grading in the absorber [34–40]. The grading comes from varying the Ga/(Ga+In) ratio to higher values towards the back. The increased band gap towards the back contact of the devices creates a BSF (Fig. 2.7) by creating a conduction-band barrier for minority-carrier electrons. Back-surface band gap grading suppresses the back-contact recombination and can add up to 90 mV to the V_{OC} [39]. Additionally, experimental and theoretical analyses indicate increases in V_{OC} and FF when the CIGS layer is thinned and an improved

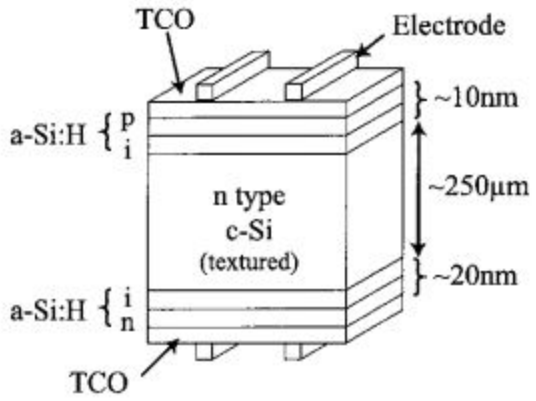

Figure 2.6: The structure of the c-Si HIT cell. Figure from Ref. [32].

carrier collection in thicker cells when Ga-grading is used [34,35]. This techniques has led to formation of highly efficient Cu(In,Ga)Se_2 solar cells, with efficiency in excess of 19.5% [12].

As with c-Si and Cu(In,Ga)Se_2, high-efficiency III-V solar cells incorporate back-surface fields to boost performance. The semiconductor materials used in these cells are composed of group III elements (e.g. aluminum, gallium, indium) alloyed with group V elements (e.g. phosphorous, arsenic, antimony). Due to their chemical nature, III-V materials can be easily doped and alloyed for changes in carrier density and band gap, respectively. Band gap and doping flexibility has enabled formation of single-junction GaAs cells with efficiencies in excess of 27% [12,41] and multijunction GaInP/GaAs/Ge cells with 32% efficiency measured with the global AM1.5 spectrum (1000 W/m^2) at 25°C [12]. III-V cells also show record efficiencies at high solar concentration, such as 29.1% for single junction GaAs or in excess of 40% for multijunctions [12, 42]. In order to achieve these high efficiencies, III-V cells use BSF films of both higher band gap and higher doping to achieve improved performance [43]. As an example, the $n-$type absorber material $Ga_{0.5}In_{0.5}P$:Zn, which is often used for top cells in multijunction structures [44], uses a two-layer BSF structure of first a higher band gap n^+ GaInP and a second layer of AlGaInP or AlInP [43–46]. For $p-$type GaAs absorbers in single or multi-junction devices, several BSF layers, such as a higher band gap GaInP [45] or a C-doped AlGaAs [47], have been used. Fig. 2.8 shows the conduction-band and valence-band offsets associated with AlGaAs and GaInP BSF layers on $p-$type GaAs absorbers. In

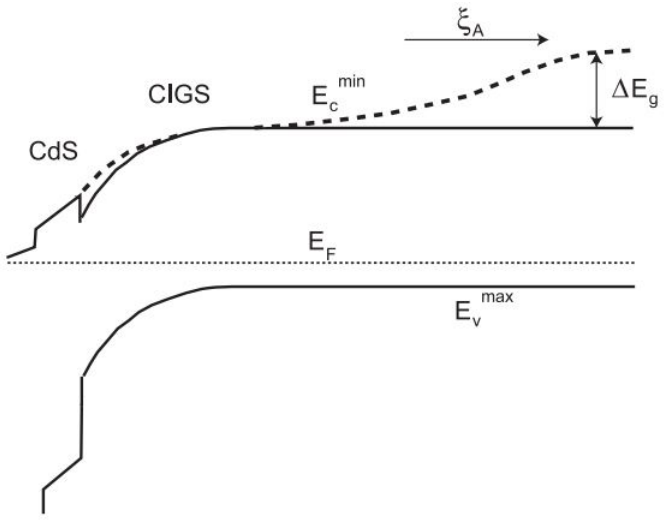

Figure 2.7: Band edge diagram of a CIGS thin film solar cell where the dotted line illustrates how the conduction band minimum (E_c^{min}) is changed for a CIGS layer with an increased Ga/(In+Ga) ratio towards the back contact and in the SCR. An additional electric field, ξ_A, is obtained due to the band gap variation. Figure from Ref. [34].

both cases, the BSF films passivate the recombination at the back contact of the absorber by providing a minority-carrier barrier in the conduction band. This is consistent with BSF strategies in c-Si and CIGS cells and with the proposed ER strategy in CdTe devices.

2.1.4 Calculated Potential of the ER Strategy in CdTe Solar Cells

The potential of an ER in CdTe solar cells has been evaluated in detail by K. J. Hsiao [26]. Prior to his work, minimal investigations into the use of a BSF in CdTe were made. The idea of an electron reflector was first investigated by J. R. Sites and J. Pan in the form of an $n-i-p$ structure [48]. In this article, they compared CdS/CdTe devices with a typical carrier density, a high density structure, and a low density structure with an electron reflector (Fig. 2.9) to an adjusted "GaAs" model. The "GaAs" model is based on the record GaAs cell but adjusted for difference in band gap. The effect of the $n-i-p$ structure (i.e. effectively the same as the ER structure presented in section 2.1.1) is shown in Fig. 2.10. A clear voltage

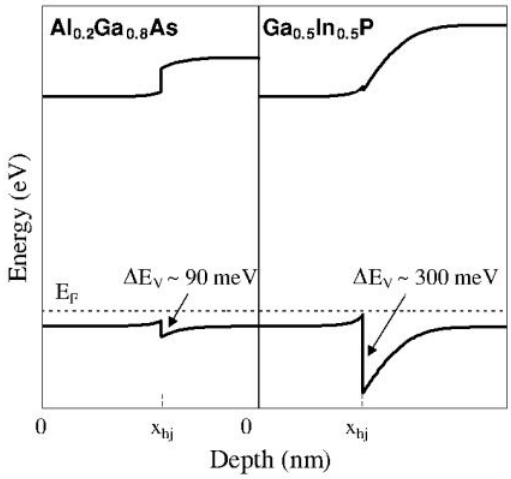

Figure 2.8: (Left) band diagram of a p-GaAs/p-$Al_{0.2}Ga_{0.8}As$ heterojunction. (Right) band diagram of a p-GaAs/p-$Ga_{0.5}In_{0.5}P$ heterojunction. In both cases the doping level is constant through the heterojunction and equals $N_A = 3$ x 10^{17} cm^{-3}. Figure from Ref. [47].

increase is evident at relatively high carrier lifetime, $\tau_n = 10$ ns, from Fig. 2.10a. However, at a more typical carrier lifetime of CdTe devices, $\tau_n = 0.5 - 1.0$ ns [10], a significant V_{OC} increase of approximately 200 mV is still possible with an ER of conduction-band barrier height, $\phi_e = 0.2$ eV (Fig. 2.10b). The 200 mV increase translates into about a 3% gain in absolute device efficiency.

Building on these initial results, Hsiao calculated how V_{OC} would be affected by the back-surface recombination velocity, S_b [49]. These calculations (Fig. 2.11) show the ER structure can improve device performance even when recombination velocity is high. Fig. 2.11a shows that the addition of a 0.2 eV electron reflector can improve the voltage when lifetime is at an attainable 1 ns. Fig. 2.11b summarizes these results by indicating that the effect S_b has on decreasing V_{OC} is greatly reduced when an 0.2 eV ER barrier is used.

Additional studies done by Hsiao pinned the recombination velocity to 10^7 cm/s, a reasonable assumption based on the record CdTe device at the time. With a constant S_b, the magnitude of ϕ_e needed to improve voltage can be investigated based on other factors. Fig. 2.12 shows the interaction between carrier lifetime of a typical 2 μm thick, $\rho = 10^{13}$ cm^{-3}

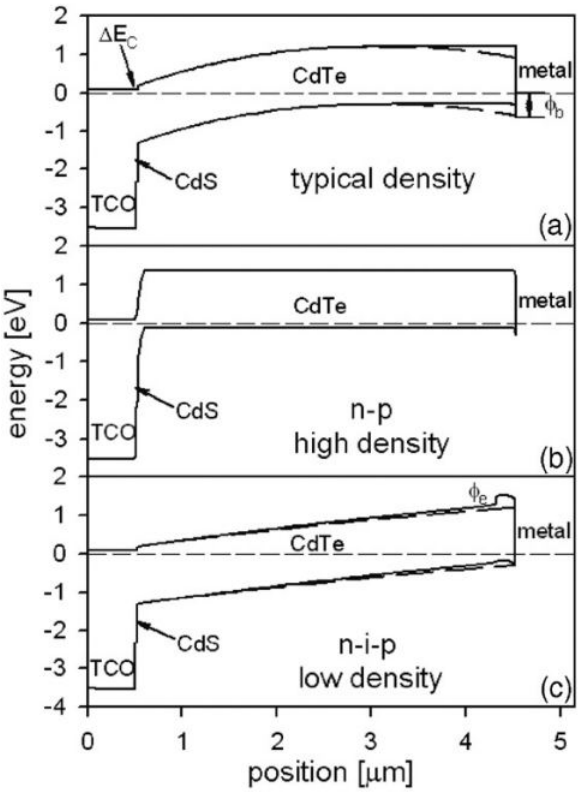

Figure 2.9: (a) Band diagram of typical CdTe solar cell with and without a significant back-contact barrier. (b) Band diagram for significantly higher hole density. (c) Band diagram for lower density with and without an electron reflector. Figure from Ref. [48].

CdTe device and conduction-band barrier height, ϕ_e. For an attainable CdTe minority-carrier lifetime ($\tau_n = 1.0$ ns), $V_{OC} > 1000$ mV and $\eta > 19\%$ can be expected with a $\phi_e = 0.2$ eV barrier. The performance parameters do not change for $\phi_e > 0.2$ eV, indicating that this barrier height may be the ceiling for improving performance at these setting.

A thin layer of metal at the back surface can act as an optical mirror. Light that is not absorbed by CdTe on its first pass can be reflected back through the CdTe absorber, where it has another opportunity to generate photo-carriers. Hsiao refers to this property as optical back reflection, R_b, and makes a reasonable estimate that $R_b = 20\%$ for these structures. However, since absorption in CdTe is high, a thinned device is needed to obtain the beneficial effects of optical back reflection. A comparison of these is presented in Fig. 2.13 [26, 50].

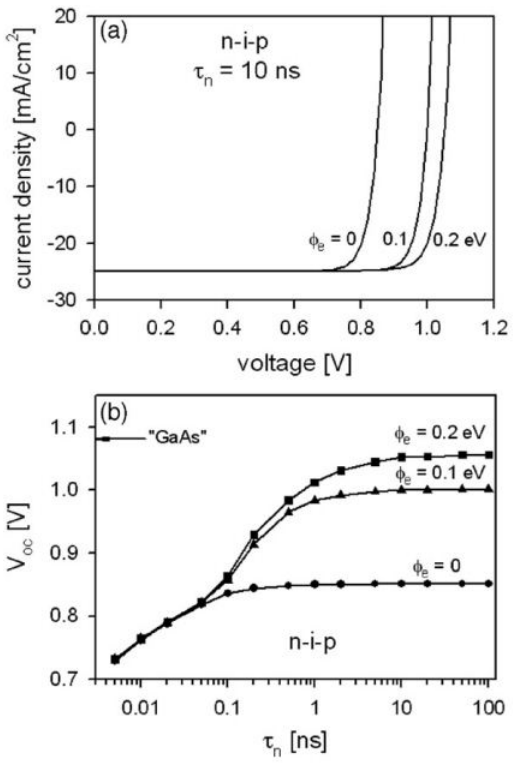

Figure 2.10: (a) Simulated JV curves for nip structure, and (b) resulting voltage dependence on lifetime and back electron barrier. Figure from Ref. [48].

From Fig. 2.13b, it is evident that a cell with $\eta > 19\%$ is possible, with improvement in FF and a 100 mV V_{OC} increase from the baseline device. The importance of thinning the CdTe layer in order to pull the ER layer into the depletion width of the device is shown in Fig. 2.14. The best performance from an $\phi_e = 0.2$ eV ER layer is achieved at a device thickness of 1 μm, where the primary gain in efficiency is associated with V_{OC} greater than 1,000 mV.

This simulation work indicates that incorporation of a 0.2 eV conduction-band barrier into the current CdS/CdTe structure could yield cell efficiency greater than 19% and open-circuit voltages greater than 1 V. An expanded band gap ER layer is the most efficient approach to realize the ER structure in practice. A practical plan to develop CdTe cells with ER layers is outlined in the next section.

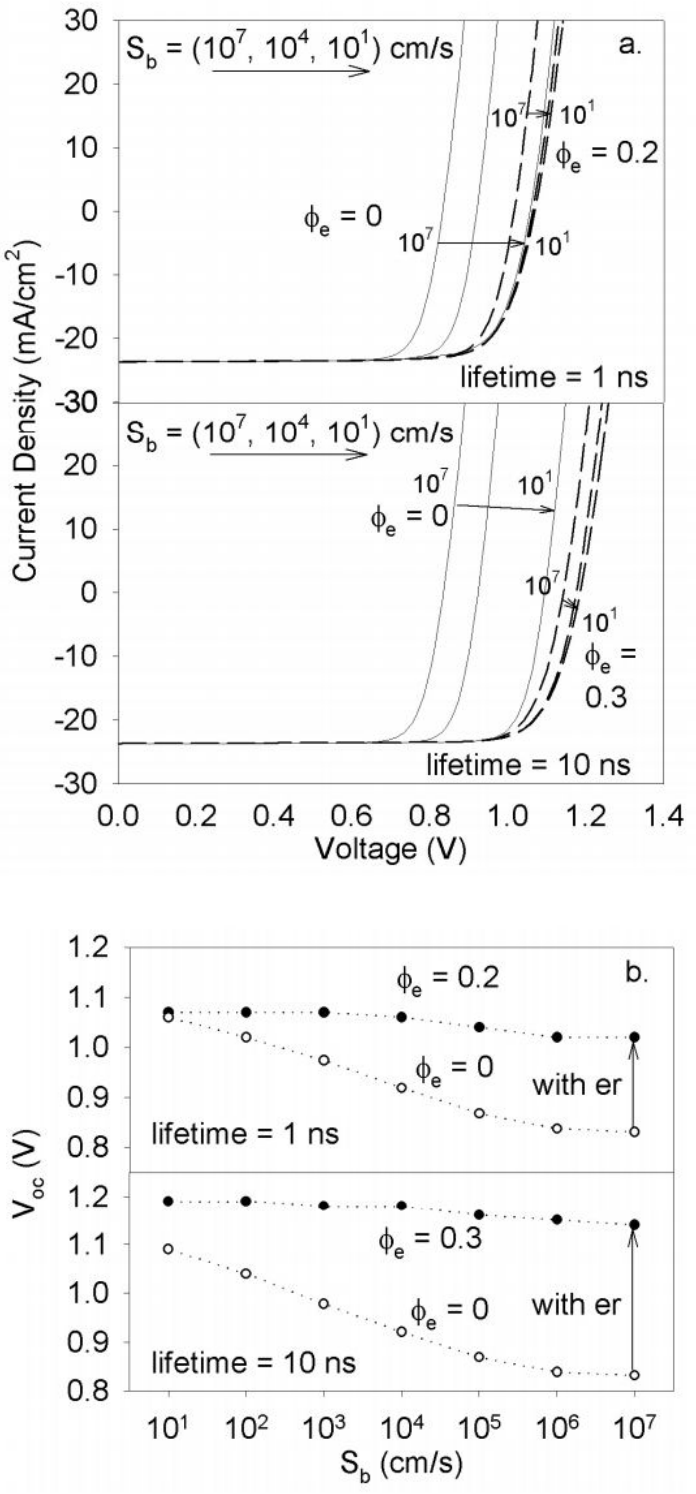

Figure 2.11: (a) Calculated J-V curves with and without an electron reflector for different values of S_b. (b) The effect of S_b variation on V_{oc}. Figure from Ref. [49].

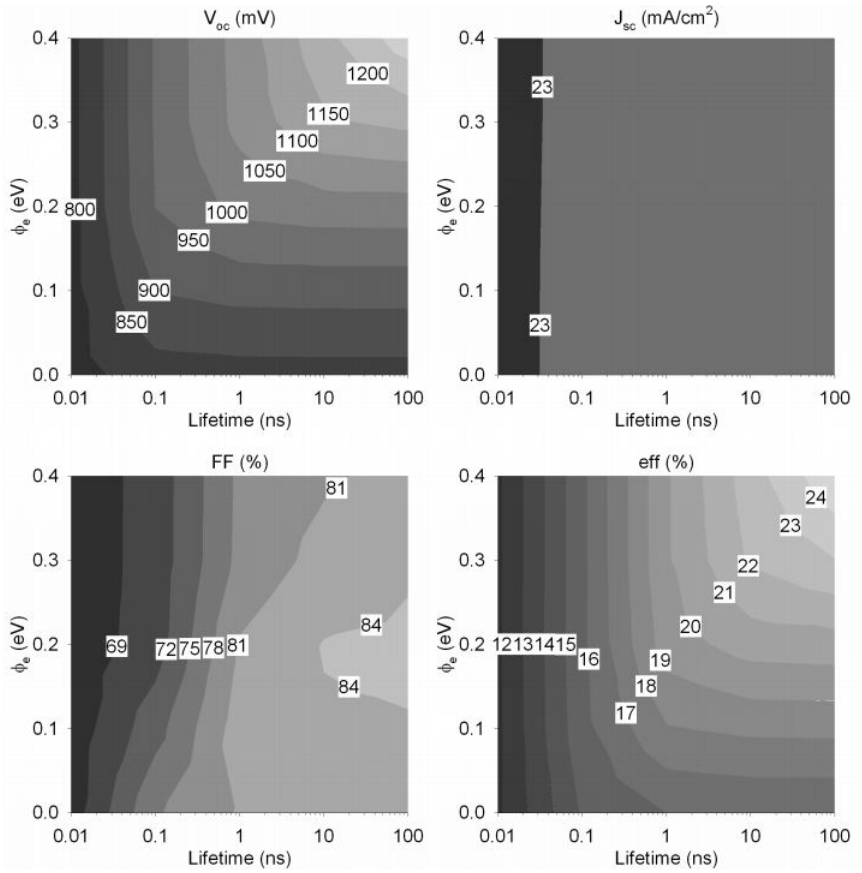

Figure 2.12: Contour plots of calculated parameters of a typical CdTe device (a 2 μm thickness, a 10^{13} cm^{-3} carrier density) based on barrier height, ϕ_e, and carrier lifetime. Figure from Ref. [26].

2.2 $Cd_{1-x}Mg_xTe$Thin Films as Electron Reflectors

In Section 2.1 it was established that an expanded-band-gap structure (Fig. 2.3) is the best option for incorporating the ER strategy into CdTe solar cells. The best devices use an ER layer with a conduction band that is 0.2 eV higher than the CdTe absorber. An expanded-band-gap material can be made by alloying CdTe with other Group II metals, such as Mg or Zn. In both cases the Mg or Zn atom replaces the Cd cation to form $Cd_{1-x}Mg_xTe$ or $Cd_{1-x}Zn_xTe$. Each material has unique advantages and disadvantages for the ER function. Reasons for selecting $Cd_{1-x}Mg_xTe$ as the primary focus of CdTe ER development is described

in detail in the next section. Disadvantages, previous development, and a new strategy for deposition of $Cd_{1-x}Mg_xTe$ is discussed thereafter.

2.2.1 Advantages of Using $Cd_{1-x}Mg_xTe$ Alloys as Elector Reflector in CdTe Solar Cells

One major aspect of making a good ER structure is to reduce the potential recombination at the CdTe/ER layer interface. A study by Hsiao indicated that if this interface had a recombination velocity, S_i, similar to that of the back-surface, S_b, the benefit of the ER is reduced [26]. This is seen visually in Fig. 2.15, where the J-V curve with both S_i and ϕ_e is worse than the CdTe baseline. One way to reduce interface recombination is to reduce the lattice mismatch between adjacent layers. Interfaces with a large lattice mismatch create deep-level defect sites that allow the photogenerated charge carriers to recombine easily. Reducing these sites, through better lattice matching, would reduce the interface recombination velocity, S_i, and improve performance of the ER structure.

A comparison of lattice constants with band gaps of several binary II-VI semiconductors is shown in Fig. 2.16. For ternary alloys made from two binary compounds (e.g. $Cd_{1-x}Mg_xTe$ is an alloy of CdTe and MgTe), this relationship is estimated to be linear. From Fig. 2.16, it is evident that MgTe has a lattice constant more closely matched to CdTe than any other compound. Furthermore, because MgTe has a higher band gap than ZnTe, less alloying will be needed to obtain the same band gap energy. For these reasons $Cd_{1-x}Mg_xTe$ is the best choice for reducing the lattice mismatch between CdTe and the ER layer and therefore reducing possible interface recombination. In addition, deposition of $Cd_{1-x}Mg_xTe$ thin films has been demonstrated using mass production friendly techniques, as described in Section 2.2.3.

2.2.2 Disadvantages of $Cd_{1-x}Mg_xTe$

The choice of $Cd_{1-x}Mg_xTe$ is not without a downside. The primary disadvantage of using $Cd_{1-x}Mg_xTe$ is a formation of a valence band hole barrier. From literature, it is

expected that the change in band gap from CdTe to $Cd_{1-x}Mg_xTe$ has a 70/30 percent split between the conduction band and valence band respectively [52]. In order to achieve a 0.2 eV conduction band barrier, the total band gap change required is 0.2 eV/0.7 = 0.28 eV, with 0.08 eV as the valence-band barrier. Therefore, a $Cd_{1-x}Mg_xTe$ ER layer with $E_g = 1.78$ eV (assuming E_g of CdTe is 1.5 eV) is needed for the ER layer. However, the experimentally obtained 70% CB/30% VB split ratio is poorly understood and needs additional analysis. For example, recent calculations of CdTe based ternary alloys shows the split to be 50/50 [53] or 65/35 [54, 55] depending on the method. Development of the $Cd_{1-x}Mg_xTe$ ER will need to include better understanding of the VB barrier.

Unlike $Cd_{1-x}Mg_xTe$, $Cd_{1-x}Zn_xTe$ does not create a VB barrier. In fact, $Cd_{1-x}Zn_xTe$ has a slightly reverse barrier in the valence band (Fig. 2.17) when paired with CdTe [56]. Although this advantage makes alloying CdTe with Zn appealing for the benefit of a slightly better band structure, lower interface problems with $Cd_{1-x}Mg_xTe$ make it a better option.

Both alloys also experience potential processing disadvantages. The affinity of both Mg and Zn to oxygen and water, make it difficult to process these materials without oxidizing the material. Effective deposition with these elements requires high vacuum systems and hardware that minimizes water adsorption. Although these are potential difficulties, both ternary alloys have been deposited successfully using physical vapor deposition methods (e.g. sputtering, evaporation, sublimation) when these factors were implemented.

2.2.3 Previous Development of $Cd_{1-x}Mg_xTe$ Alloys

Thin-film $Cd_{1-x}Mg_xTe$ has received some attention, in part because the band gap of CdTe is easily changed with Mg. Some early work demonstrated successful formation of $Cd_{1-x}Mg_xTe$ based $p-n$ junction diodes [57]. Deposition of $Cd_{1-x}Mg_xTe$ thin films began in the 1990s for quantum confined structures, such as quantum wells [58–60], where the films are grown by molecular beam epitaxy (MBE) [61–63]. More recently $Cd_{1-x}Mg_xTe$ development has progressed to quantum dots [64, 65] also made by MBE. Formation of $Cd_{1-x}Mg_xTe$ has also been shown at the interfaces of CdTe/MgTe superlattices grown by atomic layer epitaxy

(ALE) [66]. Although MBE and ALE are good techniques for making high quality materials, they are not yet suitable for commercially viable mass production.

More recent development into $Cd_{1-x}Mg_xTe$ alloys for top cells in CdTe-based multijunction solar cells has demonstrated that low-cost techniques can be used. Pursuit of tandem solar cells has been under discussion since modeling of thin-film polycrystalline cells indicated that efficiencies above 25% can be realized [67]. CdTe based cells are a good option for tandems because it is relatively easy to tune their band gap [68], thus making higher band gap $Cd_{1-x}Mg_xTe$ films useful for the top cell in tandem structures. $CdS/Cd_{1-x}Mg_xTe$ cells have been made and evaluated by several research groups, including Compaan's group at University of Toledo (UT), Dhere's group at the National Renewable Energy Laboratory (NREL), and Mathew's group at Centro de Investigacion en Energia, Universidad Nacional Autonoma de Mexico (CIE-UNAM).

The work done at UT utilized RF sputtering of $Cd_{1-x}Mg_xTe$ alloys from two source targets of 20% or 40% by weight MgTe in CdTe [69]. The sputtering yielded films with $E_g = 1.58$ eV and $E_g = 1.86$ eV, respectively. The Mg fractions of $x \approx 5\%$ and $x \approx 20\%$, respectively, were estimated by the equation [66, 69]:

$$E_g(x) = 1.5 + 0.3x(1 - x) + 2x \tag{2.1}$$

Energy dispersive x-ray spectroscopy (EDS) found the atomic composition of 5% and 16% respectively. The films were found to have high resistance that decreased when the deposition temperature increased. Additional studies of varying the RF power and the deposition pressure showed changes in crystallinity and Mg incorporation [70,71]. Decreasing deposition pressure and increasing RF power separately increased Mg atomic concentration. Atomic concentration of Mg and the band gap decreased sharply after only 10 minutes of $CdCl_2$ treatment annealing in air and Ar [69,72], leading to a common "Mg loss" problem. Nonetheless, this group was able to make a $CdS/Cd_{1-x}Mg_xTe$ cell with 3.8% efficiency.

Parallel to this work, the NREL group was pursuing co-evaporation of $Cd_{1-x}Mg_xTe$ thin-films. The term "co-evaporation" is actually a misnomer because deposition vapor was generated by solid-to-gas sublimation rather than liquid-to-gas evaporation. In this manuscript,

the term "co-evaporation" refers to two side-by-side sublimation sources. The best results of co-evaporating $Cd_{1-x}Mg_xTe$ films were achieved from Mg metal and CdTe source materials using two side-by-side effusion cells [73]. Other precursors, such as CdTe/MgF and $CdTe/MgCl_2$, were tried but did not produce good or repeatable results. The Mg fraction, x, in the films was varied by changing Mg and CdTe fluxes with source temperature. Films with band gaps ranging from 1.53 to 2.2 eV were made by varying x from 0 to 60%, which was verified by electron probe micro analysis (EPMA). Unlike the curved relationship (Eq. 2.1) estimated by Hartmann et al [66], Dhere et al found the optical relationship to be linear:

$$E_g(x) = 1.1x + 1.54 \tag{2.2}$$

Films near the desired 1.7 eV band gap were made at approximately 400°C substrate temperature, 400°C Mg source temperature, and 560°C CdTe source temperature at a pressure of $2x10^{-6}$ Torr [73–75]. Similar to UT's results, degradation of band gap with $CdCl_2$ heat treatment in a presence of oxygen was observed [74]. Heat treatment in 80 Torr O_2/320 Torr He at 400°C for 5 minutes showed a significant reduction in the band gap, a large change in the sub-gap transmission spectra, and significant changes in film microstructure. Conversely, identical treatment in 400 Torr He showed only a minor change in the transmission spectra and no microstructural changes. Alloying decomposition, through Mg loss, was controlled by varying the oxygen concentration during passivation treatment. Addition of $MgCl_2$ to the $CdCl_2$ source material during treatment reduced Mg loss when low oxygen concentrations were used [75]. Further optimization of passivation and the use of ZnTe:Cu back contact produced cells with efficiency close to 10% and V_{OC} near 800 mV [76]. Results of varying substrate temperature and Cu concentration during ZnTe:Cu deposition show that Cu can effectively dope $Cd_{1-x}Mg_xTe$ alloys, and similar to CdTe thin films, Cu can be used to form a back contact to the ER film.

The CIE-UNAM group also used co-evaporation to form $Cd_{1-x}Mg_xTe$ films [77]. Films of x =0 to 0.35 were deposited and treated with either $CdCl_2$, $MgCl_2$, or a mixture of the two. Back contact was made by sputtered Cu-Au films. The lattice constant, studied by X-ray diffraction (XRD), decreased by 0.02 $\AA$ from x =0 to 0.35, which is about 0.003% lattice

mismatch. Band gap stability was improved with use of $MgCl_2$ during post treatment. Devices with $\eta = 7.6\%$ were obtained on TEC7 substrates with 10 minute $CdCl_2$ treatment in air and 40 minute Cu annealing at 150°C [78]. Lower efficiency could be due to presence of air during passivation treatment.

2.3 Strategy for Development of $Cd_{1-x}Mg_xTe$ as an Electron Reflector

The schematic of the ER structure is shown as the center panel in Figure 1.6. It is a standard CdS/CdTe structure that includes a thin layer of $Cd_{1-x}Mg_xTe$ at the back surface. As discussed earlier, there are several important characteristics of the ER structure that are needed to obtain the expected improvement in V_{OC}. This includes having a clean CdTe/CMT interface without significant recombination, a conduction-band offset of 0.2 eV or higher, and a low valence-band offset. Furthermore, the underlying CdS/CdTe cell should be fully depleted to optimize the voltage performance of the structure.

In order to accomplish these device parameters, several careful steps need to be taken during the development of the ER structure. These are described in more detail below.

2.3.1 Deposition of $Cd_{1-x}Mg_xTe$ Thin Films

First, an experimentally efficient method for deposition of $Cd_{1-x}Mg_xTe$ thin films is needed. Previous work on deposition of $Cd_{1-x}Mg_xTe$ thin films has shown that PVD style methods are useful in alloying the film. Although co-evaporated makes good quality CMT, film growth is slow and has poor spatial uniformity. To speed up optimization of ER structures, a fast, reliable, and easily tunable process to deposit CMT films is needed. Close-space sublimation (CSS) is a good candidate for deposition of CdTe-based thin films due to its fast deposition rate and good spatial uniformity. A novel co-sublimation deposition process can be used to deposit CdTe and Mg onto a single substrate. This design stacks two thermally

independent sublimation sources and connects them by a vapor feed. The vapor feed provides a conduit for flux of the bottom source to reach the substrate. Source temperatures control both vapor fluxes and the overall growth rate. This stacked source design is referred to as "co-sublimation" in this manuscript. The development of the co-sublimation method, hardware, and deposition of CMT films is described in detail in Chapter 3.

2.3.2 Characterization of CdTe/$Cd_{1-x}Mg_xTe$ Structures

Once deposition of $Cd_{1-x}Mg_xTe$ thin films is possible, it is important to optimize deposition of CMT films on polycrystalline CdS/CdTe structures. ER devices can work only when the CdTe/CMT interface is nearly free of defects. Substrate temperature, surface cleaning, and other deposition parameters can impact this interface. Since the lattice mismatch between CMT films and CdTe films is expected to be low, the deposition could result in a clean interface if certain conditions are met. To investigate the quality of the interface and optimal process parameters, several CdS/CdTe/CMT structures were made and characterized with SEM, EDS, and cross-sectional TEM and EBSD measurements. This work is presented in Chapter 4.

2.3.3 Investigation of Passivation Treatment for $Cd_{1-x}Mg_xTe$ Thin Films

Doping of the deposited CMT film is also an important parameter in the functionality of the device. A treatment step will likely be necessary to make the polycrystalline CMT films electronically active. The material effects of $CdCl_2$ passivation treatment and optimization of this process were investigated on both CdS/CdTe/CMT ER and CdS/CMT structures. This work is presented in Chapter 5.

2.3.4 Development of CdS/CdTe/$Cd_{1-x}Mg_xTe$ ER Devices

A full CdS/CdTe/CMT electron reflector structure can be produced once the CMT films can be deposited, CMT deposition on CdTe is understood, and an effective passivation treatment is found. The device structure can then be made into electronic devices and investigated further for efficiency improvements and electronic behavior. Device characterization and investigation of device properties is presented in Chapter 6 of this manuscript.

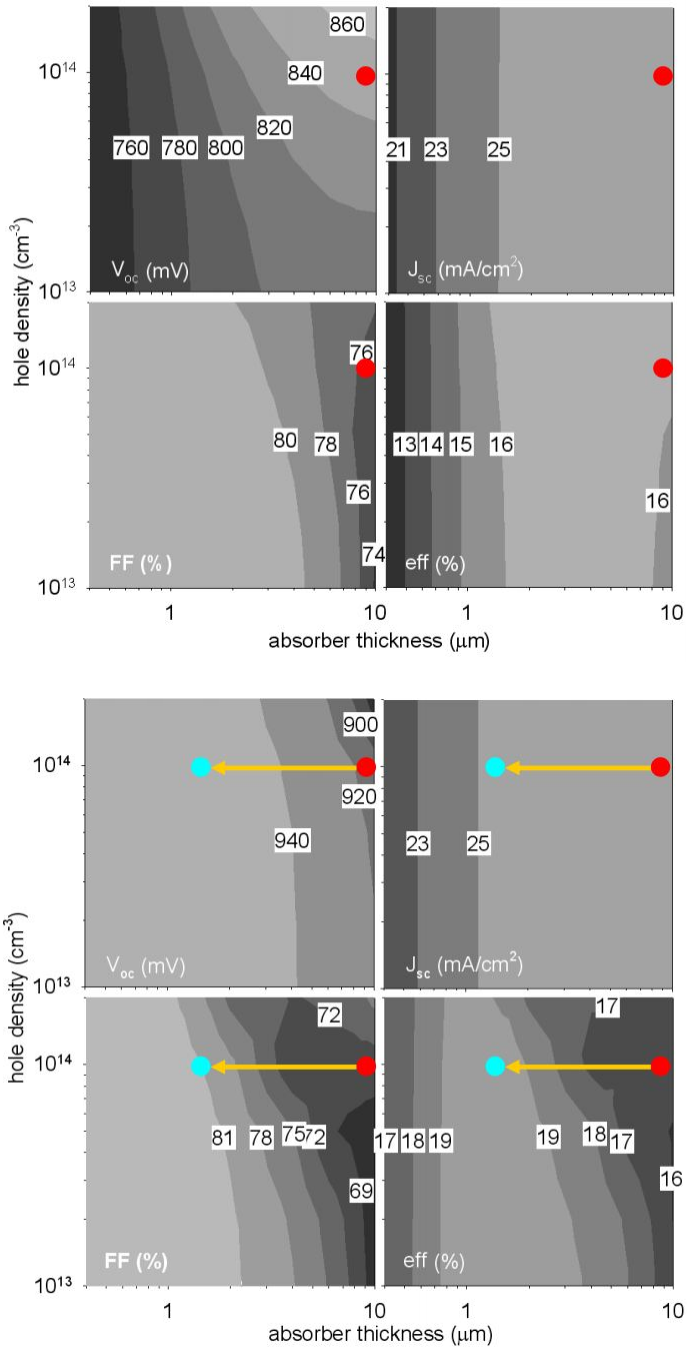

Figure 2.13: Contour plots of calculated solar-cell parameters with variations in carrier density (10^{13} - 2 x 10^{14} cm^{-3}) and absorber thickness (0.4-10 μm) for (a) the record-CdTe-cell baseline (red dots) and (b) CdTe cells with a 0.2-eV electron reflector and 20% optical back reflection of record-cell baseline model (red dots) and thinned record-cell baseline model (blue dots). Figure from Ref. [26].

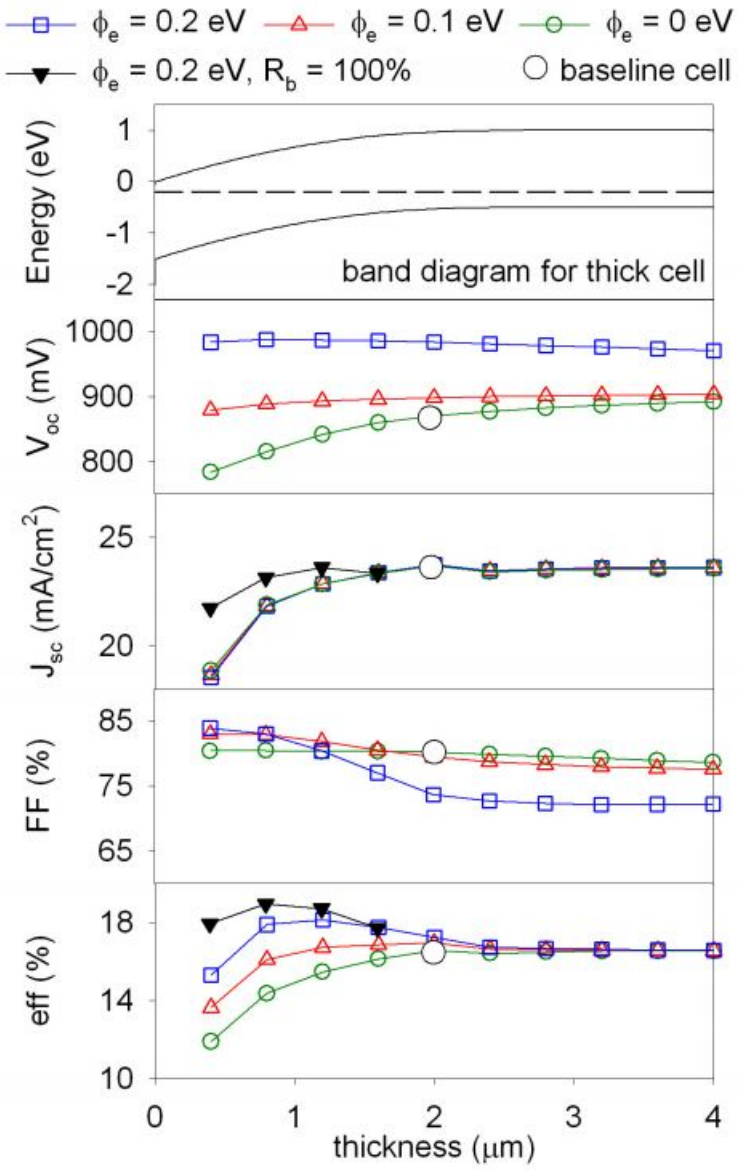

Figure 2.14: Band diagram of a thick CdTe cell and calculated parameters of cells with a range of thicknesses and electron reflector barrier heights. Parameters for cell with $\phi_e = 0.2$ eV and $R_b = 100\%$ also shown. Baseline cell marked with circle. Figure from Ref. [26].

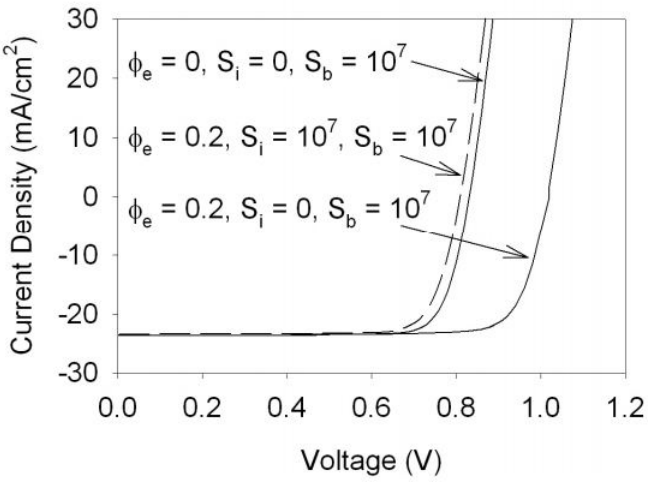

Figure 2.15: Calculated J-V curves with different values of S_b, S_i, and ϕ_e. Figure from Ref. [26].

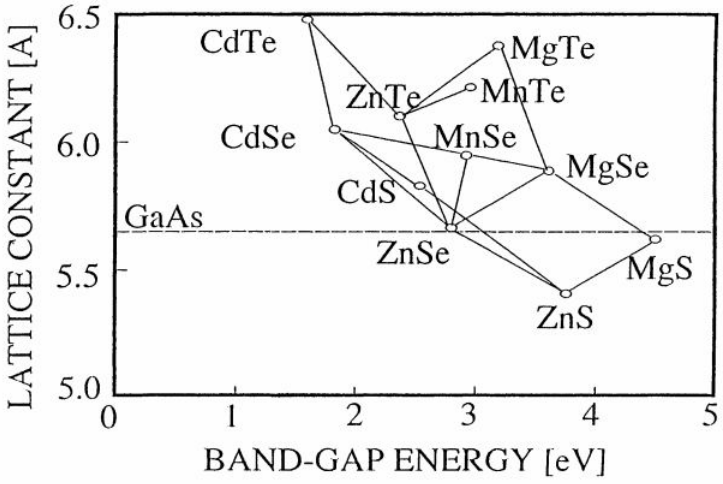

Figure 2.16: Energy band gaps and lattice constants for the family of II-VI compounds. Figure from Ref. [51].

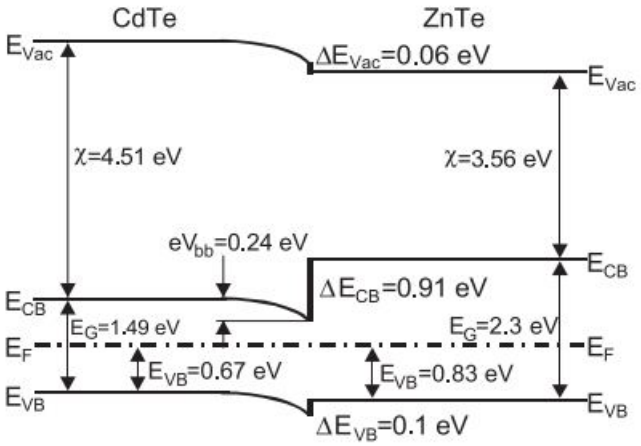

Figure 2.17: Band diagram of the CdTe/ZnTe interface as determined by photoelectron spectroscopy. The shift of the core level lines in the XP spectra corresponds to the band bending of 0.24 eV in CdTe. It is typically induced by charged interface states. Figure from Ref. [56].

Chapter 3

Deposition and Characterization of $Cd_{1-x}Mg_xTe$ Thin Films Grown by a Novel Co-sublimation Method[1]

[1]This chapter in its entirety was published as a journal article as:

P.S. Kobyakov, A.Moore, J.M. Raguse, D.E. Swanson, and W.S. Sampath, "Deposition and characterization of $Cd_{1-x}Mg_xTe$ thin films grown by a novel cosublimation method," *Journal of Vacuum Science & Technology A* **32** (2014), 021511.

Below is a list of authors and their contribution to the presented work:

P.S. Kobyakov: For this work, Mr. Kobyakov was the primary developer of the novel deposition tool. He designed, procured, and assembled the primary components of the co-sublimation deposition source and the vacuum deposition system. He optimized the deposition process to produce $Cd_{1-x}Mg_xTe$ thin films. For this study, he made the samples, prepared the samples for material analysis, and performed optical, SEM, EDS, and GAXRD characterization, data analysis, and interpreted the results. Additionally, he prepared the figures in the publication, wrote and edited the manuscript, and submitted the work to the journal.

A.M. Moore: Mr. Moore helped with process optimization steps during process development and performed optical characterization of the samples. He also helped with interpretation of results and edited the manuscript.

J.M. Raguse: Mr. Raguse performed optical measurements, analyzed the optical data, helped interpret the results, and contributed to editing of the manuscript.

3.1 Overview

Photovoltaic cells utilizing the CdS/CdTe structure have improved substantially in the past few years. Despite the recent advances, the efficiency of CdS/CdTe cells is still significantly below their Shockley-Queisser limit. CdTe based ternary alloy thin films, such as $Cd_{1-x}Mg_xTe$ (CMT), could be used to improve efficiency of CdS/CdTe photovoltaic cells. Higher band gap CMT films can be the absorber in top cells of a tandem structure or an electron reflector layer in CdS/CdTe cells. A novel co-sublimation method to deposit CMT thin films has been developed. This method can deposit CMT films of band gaps ranging from 1.5 to 2.3 eV. The co-sublimation method is fast, repeatable, and scalable for large areas, making it suitable for implementing into large-scale manufacturing. Characterization of as-deposited CMT films, with x varying from 0 to 0.35, reveals a linear relationship between Mg content measured by Energy Dispersive X-Ray Spectroscopy (EDS) and the optical band gap. Glancing Angle X-Ray Diffraction (GAXRD) measurements of $Cd_{1-x}Mg_xTe$ films show a zinc-blende structure similar to CdTe. Furthermore, increasing Mg content decreases the lattice parameter and the grain size. GAXRD shows the films are under mild tension after deposition.

3.2 Introduction

Despite recent improvements in efficiency [12], CdS/CdTe heterojunction solar cells perform significantly below the theoretical limit for their band gap [11, 13]. Several ways to improve device efficiencies have been proposed, including development of a tandem junction

D.E. Swanson: Mr. Swanson helped with process development, sample preparation, result interpretation, and editing of the manuscript.

W.S. Sampath: Prof. Sampath provided significant guidance on process development, tool design, sample preparation, and material characterization. He also helped to interpret the results, and edited the manuscript.

cell [67] or by incorporating an electron reflector (ER) into the device to increase open-circuit voltage [50]. Both cases can use a CdTe based ternary alloy with higher band gap, such as $Cd_{1-x}Mg_xTe$ (CMT). In tandem cells, higher band gap $Cd_{1-x}Mg_xTe$ can be used as a *p*-type absorber of the top cell. The ER structure is an incorporation of a back-surface field into the CdS/CdTe device and aims to improve the open-circuit voltage (V_{OC}) by reducing back-surface recombination. The V_{OC} of CdS/CdTe devices (typically around 840 mV), is significantly lower than what is expected for the band gap of CdTe (E_g = 1.45 eV). For a similar band gap (1.42 eV), single junction GaAs cells demonstrate higher efficiencies in part due to higher V_{OC}, above 1.0 V [12]. As proposed by Hsiao and Sites [11, 50], the ER structure is expected to improve V_{OC} to above 900 mV by adding a conduction band barrier at the rear of the device to reduce back-surface recombination. The conduction band barrier can be made using a higher band gap $Cd_{1-x}Mg_xTe$ thin film. In this work, we present a co-sublimation method to grow CMT films that is both fast and potentially scalable to module size areas.

Growth of $Cd_{1-x}Mg_xTe$ thin films has been shown by both RF sputtering [72] and co-evaporation [74]. While both techniques produce $Cd_{1-x}Mg_xTe$ films, their slow deposition rate and poor spatial uniformity makes them unsuitable for large scale manufacturing. Spatial uniformity is an important aspect of producing high efficiency photovoltaic modules because small variations in thickness and band gap over the module area can produce significant losses in total efficiency. For example, band gap fluctuation in the ER layer could lead to local voltage variation and thus reduce total cell and module V_{OC}. Therefore, development of methods to uniformly deposit large areas of CMT thin films is an important step toward realizing and commercializing potential efficiency improvements. In our recent work [79], we have replicated $Cd_{1-x}Mg_xTe$ co-evaporation deposition made by Dhere *et al.* [74] with comparable results. Similar to their work, a gradient of band gap was found on the deposited films. We have developed a new sublimation source design that improves spatial uniformity of deposited $Cd_{1-x}Mg_xTe$ films and improves the deposition rate. Due to the relative symmetry of the deposition hardware, this process, and the improved uniformity, can be scaled to

module size areas to improve cell and module efficiency. A description of this novel thin-film deposition method and film results are described.

3.3 Experimental Details

$Cd_{1-x}Mg_xTe$ thin films were grown by a co-sublimation process, based on the heated pocket deposition (HPD) method used for deposition of CdTe thin films [80]. The co-sublimation hardware design combines the ternary thin-film deposition of co-evaporation with the spatial uniformity and high deposition rate of HPD hardware. A schematic of the co-sublimation source design is shown in Fig. 3.1. The design contains heaters and a graphite top plate that maintains the temperature of the horizontal substrate. CdTe source material sublimates in the upper graphite crucible and begins approaching the colder substrate. Meanwhile, Mg vapor is generated in the lower, independently heated crucible from evaporation grade Mg metal pellets. Mg vapor is introduced to the heated pocket through manifolds in the CdTe sublimation source. At the cooler substrate, the Cd, Te, and Mg vapors combine and form an alloyed $Cd_{1-x}Mg_xTe$ film. Similar to HPD, the co-sublimation process can achieve deposition rates of up to 1 μm/min, suitable for a fast manufacturing process developed previously [80]. Scalability of this source design comes from ability to pattern the Mg manifolds in the CdTe crucible. The associated symmetry of the source allows for large area deposition sources to be designed. However, critical design steps will be needed to optimize the film alloy uniformity and thickness over larger areas. In addition to making $Cd_{1-x}Mg_xTe$ thin films, the co-sublimation hardware and process can be used to deposit other materials.

The deposition of $Cd_{1-x}Mg_xTe$ thin films was performed in the Deposition Research Chamber (DRC) at the Materials Engineering Laboratory of Colorado State University. The DRC, shown in Fig. 3.2, was outfitted with the co-sublimation deposition source, a substrate preheater, a load lock and gate valve for quick sample introduction, and a magnetic transfer arm for substrate motion. Base pressure below 10^{-5} Torr in the DRC is accomplished with a diffusion pump equipped with both water baffle and a liquid nitrogen trap. $Cd_{1-x}Mg_xTe$

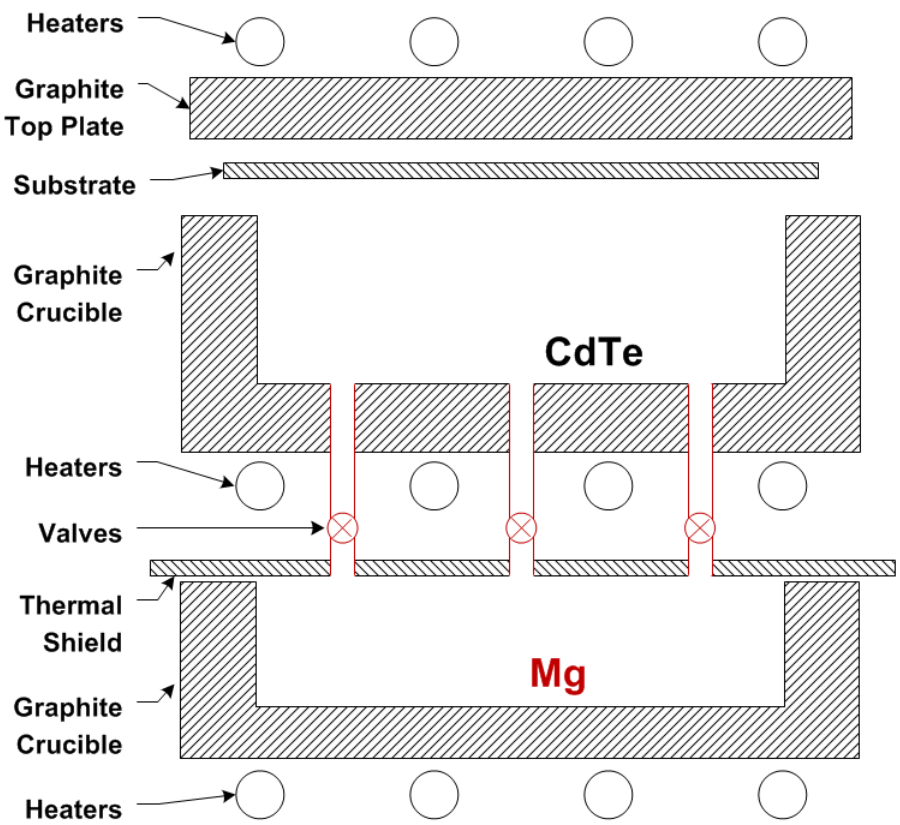

Figure 3.1: Schematic of co-sublimation deposition source design.

thin films were deposited onto commercially available TEC10 substrates coated with approximately 130 nm of CdS grown by close space sublimation using our previously described process and hardware [81, 82]. The TEC10 substrate consists of a 3.2 mm sheet of soda-lime glass coated with two layers of SnO_2 and SiO_2, each about 20 nm thick, and an approximately 400 nm thick fluorine-doped tin oxide (SnO_x:F) as the transparent conductive layer. CMT is deposited in 20-60 mTorr of Argon, measured using a thermal conductivity vacuum gauge utilizing a MEMS vacuum sensor. The substrate temperature during deposition was held between 450 and 520°C, measured with a pyrometer. CdTe source and Mg source temperatures were controlled independently to optimize the growth rate and Mg content. CdTe source temperature was controlled between 550 and 600 ℃, measured using thermocouples embedded in the graphite source. Similarly, Mg source temperature was controlled between 440 and 500°C by thermocouples embedded in the graphite crucible. The CdTe source tem-

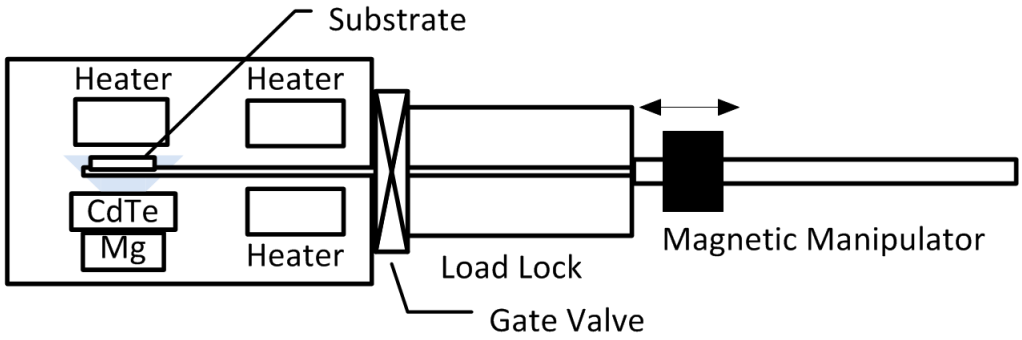

Figure 3.2: Side-view schematic of Deposition Research Chamber (DRC) setup for co-sublimation.

perature was used to control film growth rate, while Mg temperature was used to control Mg content in the film. $Cd_{1-x}Mg_xTe$ films about 1 μm thick were deposited in 2 minutes (a growth rate of approximately 500 nm/min). The samples were cooled in the load lock in about 80 Torr of Argon gas. Samples were removed when substrate temperature cooled to below 150°C, which was measured by a pyrometer.

Optical properties of deposited films were analyzed with a Cary 500 UV-visible (VIS)-near-infrared (NIR) spectrophotometer. Band gap uniformity was studied with a Mikropack DH-2000-BAL UV-VIS-NIR Lightsource and an Ocean Optics USB4000-VIS-NIR spectrometer. Band gaps were calculated using the Tauc plot method, where $(\alpha h\nu)^2$ is plotted against photon energy, $h\nu$, and the linear portion of $(\alpha h\nu)^2$ is extrapolated to where $\alpha = 0$ cm^{-1} (i.e., the x-axis). The absorption coefficient, α, was estimated from the measured transmission curves using the relation $\alpha(\lambda) = -ln(T(\lambda))/l$, where $T(\lambda)$ is the transmission, and l is the thickness of the film. A JEOL JSM-6500F field emission scanning electron microscope (SEM) was used for imaging and energy dispersive x-ray spectroscopy (EDS). Glancing angle x-ray diffraction (GAXRD) was performed at an incidence of 2° with a Bruker D-8 Discover utilizing Cu K_α radiation ($\lambda = 1.5418\mathring{A}$). Film thickness was measured with a Tencor Instruments Alpha Step Profilometer.

3.4 Results and Discussion

3.4.1 Processing of $Cd_{1-x}Mg_xTe$ Thin Films

Initial optimization of film deposition using the co-sublimation process revealed several important processing steps necessary to produce CMT films. First, it was discovered that a naturally formed MgO coatings on the Mg pellets needed to be removed prior to Mg sublimation by raising the source temperature to 530-560°C for up to an hour before Mg began to sublimate. Exact time and temperature needed for oxide removal depends on the oxide thickness on the Mg pellets. After the oxides are removed, the Mg source temperature is then reduced to typical process temperature between 440°C and 500°C to obtain desired Mg concentration in the $Cd_{1-x}Mg_xTe$ film. Second, the deposition pocket needs to be at least partially open during both film deposition and in-between samples. By allowing excess material to leave the pocket, the CdTe and Mg sublimation rates can be maintained for repeatable deposition characteristics. Finally, the water and oxygen levels in the deposition chamber and in the deposition pocket need to be reduced to below 0.1% for stable deposition of CMT films. Excess water and oxygen react quickly with Mg vapor and lead to poor film properties and process repeatability, resulting in large band gap and film thickness fluctuations at nominally identical process settings. Once the co-sublimation process is up and running, continuous production of nominally identical CMT films is achievable with a cycle time of about 20 minutes, which includes loading the sample, film deposition, cooling, and unloading the sample. This relatively fast processing speed is useful for research scale process optimization and also enables the co-sublimation method to be used in a continuous in-line production process suitable for manufacturing PV modules [80].

3.4.2 Optical Properties of $Cd_{1-x}Mg_xTe$ Thin Films

As stated earlier, the band gap of $Cd_{1-x}Mg_xTe$ films can be controlled by varying the Mg and CdTe flux ratio during the deposition. Increasing CdTe flux independently of Mg flux

increases film growth rate and reduces the band gap, since less Mg is alloyed into the film. Alternatively, varying the Mg flux independently changes Mg incorporation into the film, thus changing the band gap, but does little to change the film thickness. A desired growth rate and band gap are achieved first by optimizing the CdTe flux for desired film thickness, followed by optimizing the Mg flux for desired film band gap. Transmission data for various $Cd_{1-x}Mg_xTe$ thin films grown by co-sublimation are shown in Fig. 3.3 [83]. The curves indicate that a tight control of CMT film band gap can be achieved with the co-sublimation design. The transmission spectra were used to estimate the absorption coefficient of the film. To determine the band gap, the Tauc plot method of plotting $(\alpha h\nu)^2$ versus $h\nu$ was used (an example Tauc plot of one CMT film is provided in Fig. 3.4 inset). The band gap is determined by extrapolating the linear section (marked with a red line in Fig. 3.4 inset) to the x-axis. The x-intercept of the extrapolation, i.e. where $(\alpha h\nu)^2$ equals zero, is the film's band gap. In addition to optical measurements (Fig. 3.3), the CMT films were characterized with planar EDS to quantify the atomic concentrations of Cd, Te, and Mg and to calculate the Mg/(Cd+Mg) ratio, x. The relationship between EDS measured Mg ratio and calculated band gap is shown in Fig. 3.4. A linear fit of collected data is identified in red and indicates the following relationship:

$$E_g(x) = 1.86 * x + 1.5. \tag{3.1}$$

The data and the fit are well behaved with an R^2 value of greater than 0.95. Also shown in Fig. 3.4 by the blue line is a similar relationship derived by Dhere *et al.* [73] from their co-evaporation deposited $Cd_{1-x}Mg_xTe$ thin films. The discrepancy between the two relationships is not immediately clear. As suggested in their paper, one possibility could be that analysis methods overestimated the Mg content for that band gap [73]. The discrepancy arises because optical measurements identify the lowest band gap in the measured area, while atomic concentration measurements take an average over the area, thus overestimating the Mg content for that band gap. Both relations show a good approximation of CdTe band gap (at $x = 0$), but differ significantly at x of unity (i.e., MgTe). Experimentally extrapolated literature values for MgTe band gap vary significantly from 3.5 eV [84] to as low as 2.9 eV [61].

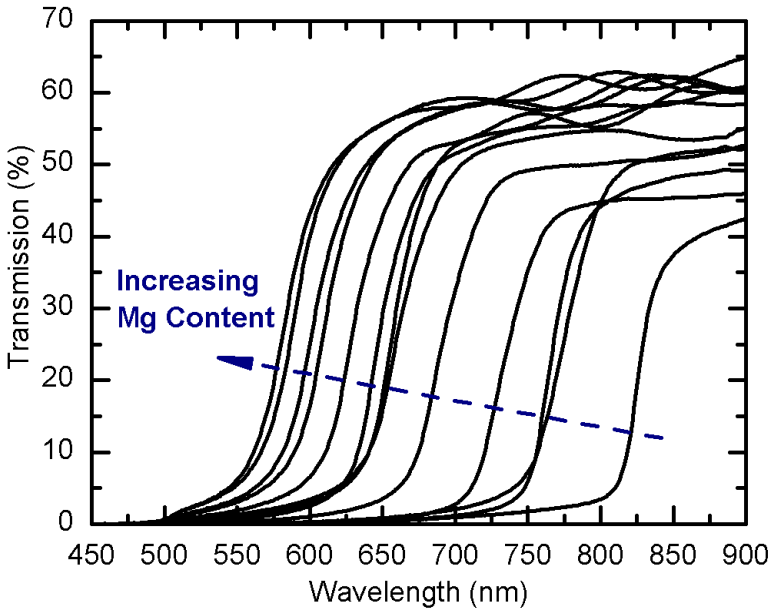

Figure 3.3: Transmission of various $Cd_{1-x}Mg_xTe$ thin films [83].

$Cd_{1-x}Mg_xTe$ is highly hygroscopic and phase unstable when x exceeds 0.8 [55]; thus, direct optical measurements of MgTe films have not been made.

Band gap uniformity over the substrate area was studied using transmission measurements. Figure 3.5 shows a contour map of the band gap of one $Cd_{1-x}Mg_xTe$ film deposited on our 3.1 x 3.6 inch sample. A significant spatial variation in the E_g is seen over the deposited film. While the center area of the film is at the desired band gap of 1.65 eV, the band gap drops off quickly when approaching the edges of the film. The central zone of the film, between 0.5 and 2.0 inches on both axes, show an acceptable level of uniformity (about a 2.5%, or 0.04 eV, difference). A lower band gap at the edges is attributed to positioning of the Mg vapor feeds in the CdTe source and the shallow depth of the intermixing pocket. Although the poor uniformity is not desirable for large scale manufacturing, it has been useful in our research of CMT films in PV cells. The uniformity can be improved by deposition at higher pressures, to force more scattering of the vapor flow, or by manipulating the source geometry to allow a larger intermixing volume for the vapors.

The effect of pressure on growth rate and band gap uniformity was investigated during one set of experiments (Fig. 3.6). The process pressure was varied from 5 to 160 mTorr

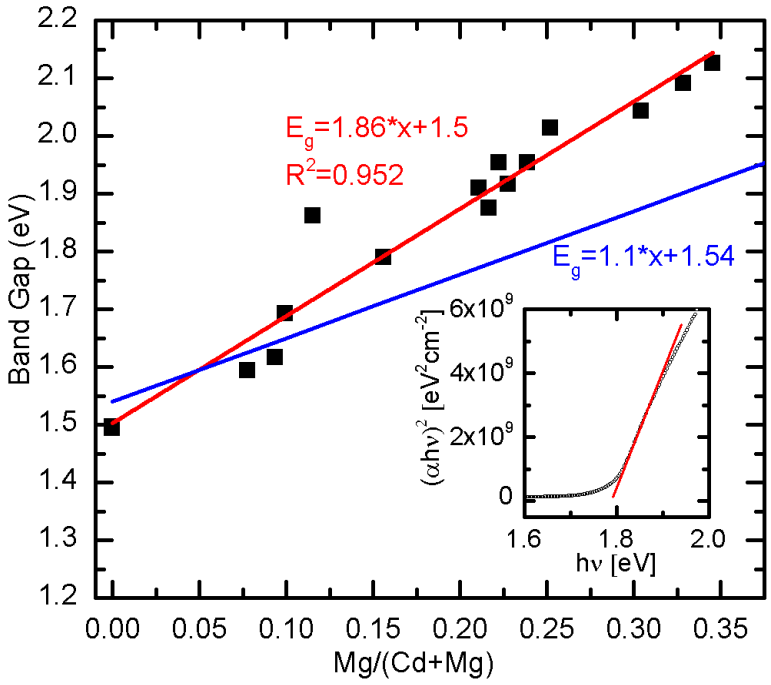

Figure 3.4: Band gap as a function of Mg content of co-sublimation deposited $Cd_{1-x}Mg_xTe$ thin films (black squares, red line) compared to the relationship found by Dhere *et al.* of co-evaporated $Cd_{1-x}Mg_xTe$ films (blue line) [73]. Inset shows example of a Tauc plot and the linear extrapolation (red line) used to calculate the band gap of a CMT film.

of Argon. As process pressure increases to 120 mTorr, the growth rate decreases due to a reduction of both CdTe and Mg sublimation fluxes (Fig. 3.6, top). The band gap also decreases [Fig. 3.6(c)] at higher pressure, indicating the Mg flux is reduced more than CdTe flux and therefore leading to lower Mg incorporation. Increasing process pressure additionally improves the CMT band gap uniformity [Fig. 3.6(c)]. As pressure is decreased to our standard process condition of 40 mTorr, the uniformity [Fig. 3.6(b)] decreases while band gap and growth rate increase. Decreasing the pressure further to 5 mTorr produces films with significant pockets of high Mg content [Fig. 3.6(a)]. This beaming behavior of Mg vapor in the co-sublimation source is attributed to lower vapor scattering and intermixing in the deposition pocket. When the pressure is low and vapor scattering is reduced, Mg vapor rises out of the manifold between the two sources and goes directly to the substrate for deposi-

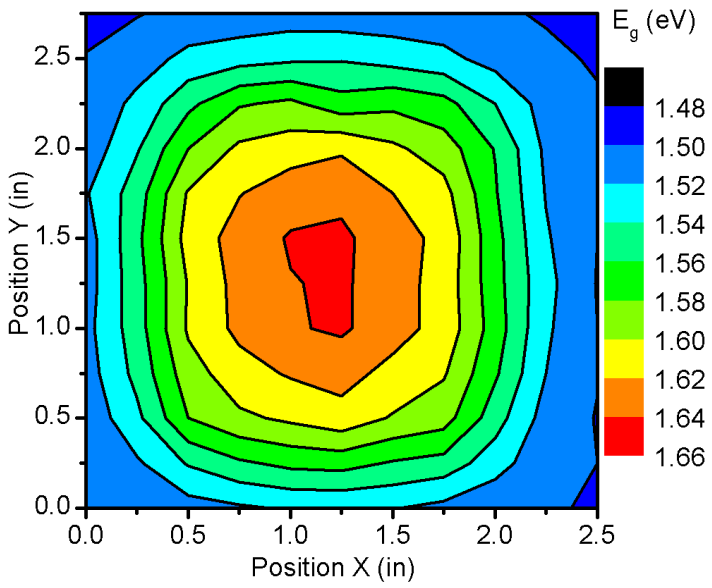

Figure 3.5: Spatial band gap uniformity of one $Cd_{1-x}Mg_xTe$ thin film deposited on TEC10/CdS.

tion, thus replicating the pattern of the manifold. By incorporating hardware changes (e.g., a deeper pocket for more vapor scattering) and optimizing the deposition pressure, we expect to improve the $Cd_{1-x}Mg_xTe$ film uniformity and make it suitable for large area deposition.

3.4.3 Structural Properties of $Cd_{1-x}Mg_xTe$ Thin Films

Figure 3.7 shows SEM images of CMT films with various measured band gaps and Mg composition. These films are nominally of similar thickness and grown at approximately 480°C substrate temperature onto premade TEC10/∼120 nm CdS structures. A clear change in film crystallinity due to Mg incorporation is evident from the images, where the band gaps and compositions are labeled. The grain size tends to decreases with increased Mg content. The CdTe film ($x = 0$) has grains about 1 μm in size, which is typical for our process. The high band gap $Cd_{0.65}Mg_{0.35}Te$ film ($E_g = 2.13$ eV), however, shows a much smaller grain size (about 0.3 μm). The higher band gap films appear to have structural defects inside the grains, but seem to be smoother than the CdTe film. All films are coalesced, indicating substrate temperatures are appropriate for this process.

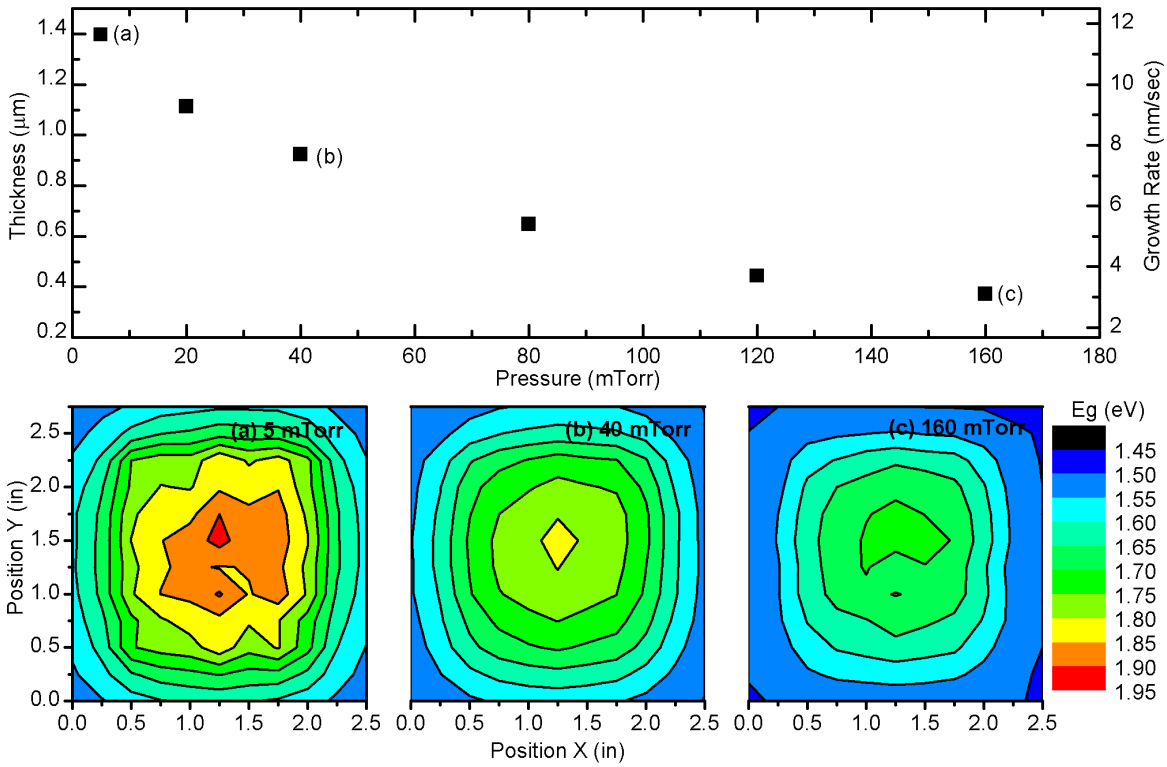

Figure 3.6: Top: Thickness and growth rate of $Cd_{1-x}Mg_xTe$ films grown at various process pressures for 120 seconds. Bottom: Corresponding band gap uniformity of CMT films grown at (a) 5 mTorr, (b) 40 mTorr, and (c) 160 mTorr of Argon process pressure.

Similarly made CMT films were studied by GAXRD. Figure 3.8 shows GAXRD spectra of four CMT films of varying composition after smoothing and subtraction of background and $K_{\alpha 2}$ peaks. Each spectrum is labeled with the film band gap and calculated Mg composition, x. The peaks are labeled with the diffraction planes of cubic zinc blende lattice (JCPDS 15-0770). The similarity of $Cd_{1-x}Mg_xTe$ diffraction spectra to zinc blende CdTe indicates that the films are of similar crystal structure. The preferred orientation of the thin films can be found using the texture coefficient for each (hkl) diffraction plane, given by [85]:

$$P_i = \frac{N(I_i/I_{i0})}{\sum_{i=1}^{N}(I_i/I_{i0})} \tag{3.2}$$

where I_i is the measured intensity of the ith plane, I_{i0} is the JCPDS powder diffraction intensity of the ith plane, and N is the number of diffraction planes considered for the anal-

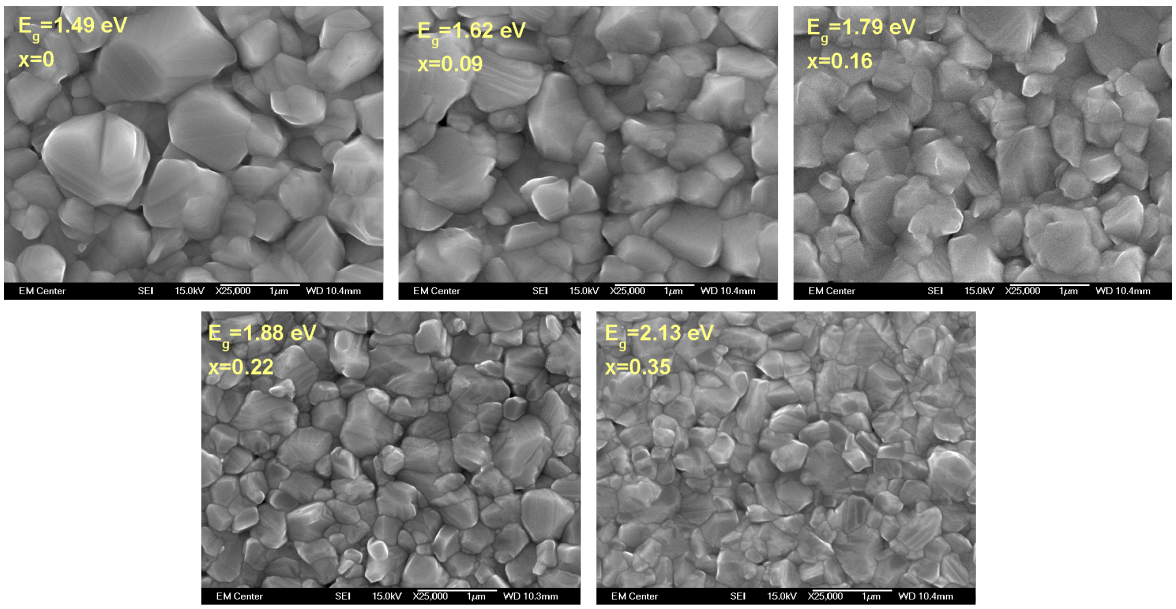

Figure 3.7: SEM images of various $Cd_{1-x}Mg_xTe$ thin films. Band gap and Mg composition are noted. Scale is kept constant for all images.

ysis. Randomly oriented thin films will have texture coefficients of unity for each reflection plane. Texture coefficients above unity indicate a preferred orientation of crystallites to that reflection plane. The degree of preferred orientation, σ, can be used to compare films to each other and is given by:

$$\sigma = \sqrt{\frac{\sum_{i=1}^{N}(P_i/P_{i0})^2}{N}} \tag{3.3}$$

where P_{i0} is the powder texture coefficient (unity). A sample with completely random orientation will have σ equal to zero. Table 3.1 provides the texture coefficient and degree of preferred orientation for the four CMT films shown in Fig. 3.8. Low σ values indicate none of the films are highly orientated. The texture coefficients show the (400) and (511) are the more preferred orientations. The orientation of CMT films do not change significantly with additional Mg incorporation.

The GAXRD peak locations can be used to learn about the lattice parameter of the alloy films. Figure 3.9 plots the (111) peaks for $Cd_{1-x}Mg_xTe$ films and their respective location. The (111) peaks (plotted in Fig. 3.9inset) move to higher 2θ values when the band gap of the film increases, which is associated with a decrease in lattice parameter. The lattice constant

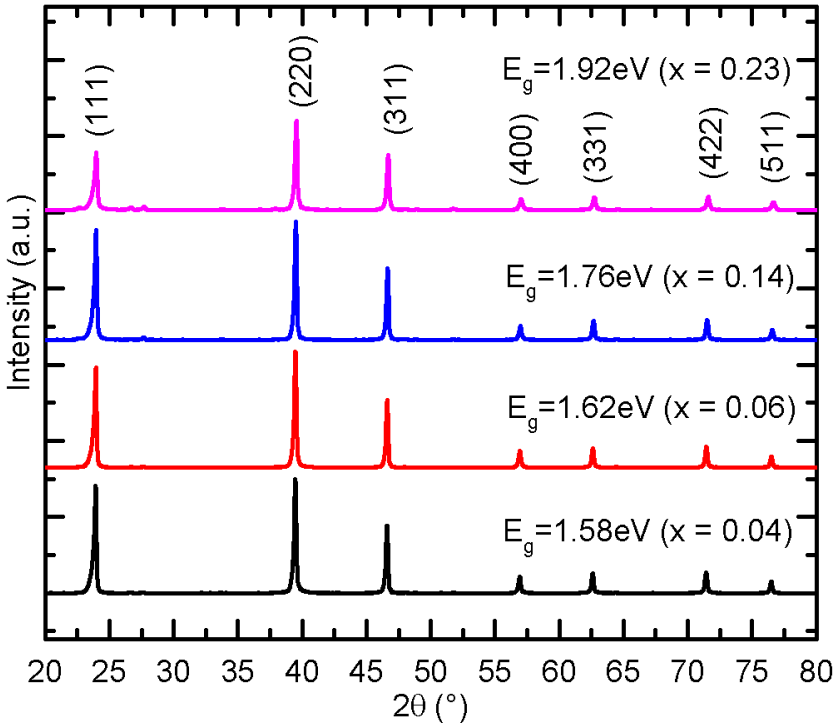

Figure 3.8: GAXRD spectra of TEC10/CdS/$Cd_{1-x}Mg_xTe$ thin films of various compositions. Zinc blende peaks are labeled with their Miller indices.

for these films was calculated using the Nelson-Riley method [86] and are shown in Fig. 3.10. In the Nelson-Riley method, the lattice parameter, calculated for each peak by

$$a_{hkl} = \frac{\lambda}{2\sin\theta}\sqrt{h^2+k^2+l^2} \tag{3.4}$$

where λ is the wavelength of incident x-ray beam ($\lambda_{K_{\alpha 1,Cu}} = 1.5405\mathring{A}$), is plotted against $(\cos^2\theta/\sin\theta + \cos^2\theta/\theta)$. The lattice constant of the film is found by linearly fitting the data and extrapolating to $\theta = 90°$, i.e., where $(\cos^2\theta/\sin\theta + \cos^2\theta/\theta) = 0$. Figure 3.10 shows the calculated lattice parameters and the impact of Mg incorporation on the lattice constant of the deposited films along with the powder lattice constants of CdTe ($a_{CdTe} = 6.481\mathring{A}$) and MgTe ($a_{MgTe} = 6.420\mathring{A}$). The dashed line in Fig. 3.10 indicates the lattice constant of $Cd_{1-x}Mg_xTe$ if the transition is assumed linear. As the Mg content increases, the lattice constant of $Cd_{1-x}Mg_xTe$ decreases, which is expected because the ionic radius of Mg is smaller than that of Cd. The measured lattice constants follow a linear path similar to the assumed

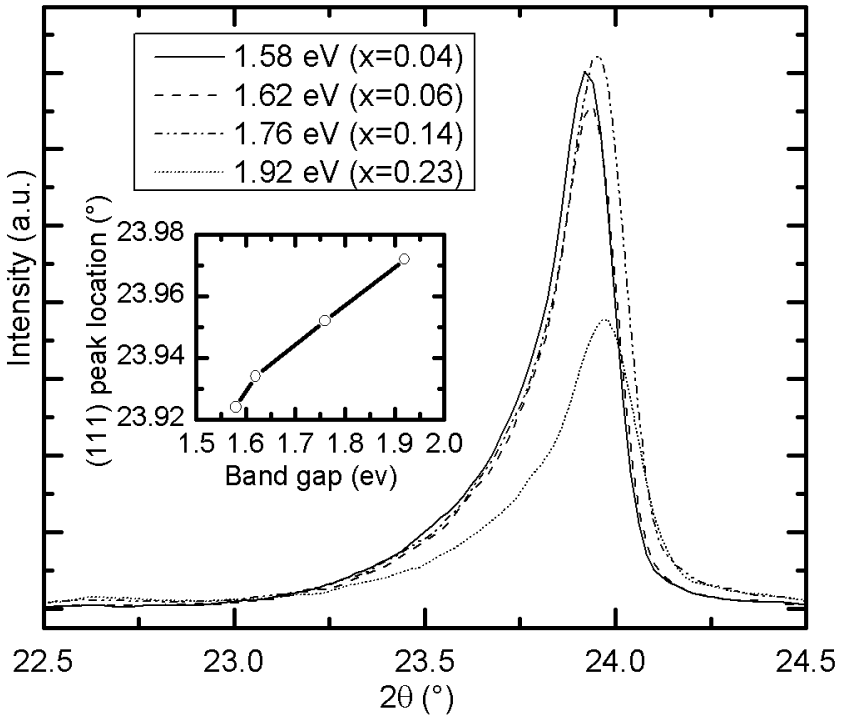

Figure 3.9: (111) peaks of various band gap $Cd_{1-x}Mg_xTe$ films. Peak locations by band gap are shown in inset.

Table 3.1: Texture coefficients and grade of preferred orientation of various band gap $Cd_{1-x}Mg_xTe$ films.

		Texture coefficient							
E_g	x	(111)	(220)	(311)	(400)	(331)	(422)	(511)	σ
1.58	0.04	0.51	0.84	0.92	1.37	0.88	1.03	1.45	0.30
1.62	0.06	0.45	0.86	0.98	1.46	0.88	1.03	1.43	0.32
1.76	0.14	0.58	0.87	1.05	1.16	0.94	0.99	1.27	0.21
1.92	0.23	0.34	0.73	0.90	1.17	0.75	0.80	1.27	0.32

relationship and to work by others [87]. Furthermore, the calculated plane spacing is smaller than the lattice constant of powder samples, indicating the films are under tension.

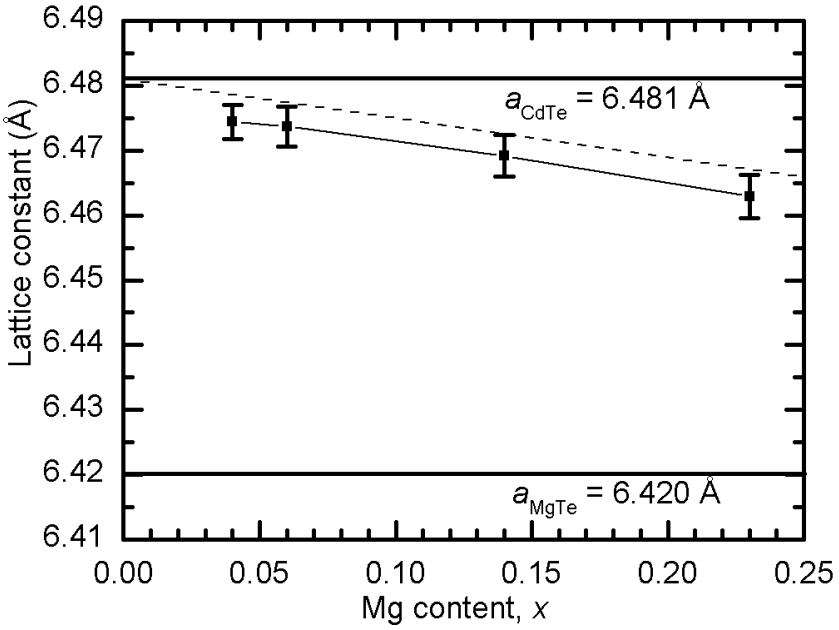

Figure 3.10: Lattice constant of $Cd_{1-x}Mg_xTe$ as a function of calculated Mg content. Lattice constants of powder CdTe and MgTe are noted. Dashed line is the lattice constant of powder $Cd_{1-x}Mg_xTe$ if transition from CdTe to MgTe is assumed to be linear.

3.5 Conclusions

A novel co-sublimation method of growing $Cd_{1-x}Mg_xTe$ thin films from independently controlled CdTe and Mg sources has been presented. During deposition of the $Cd_{1-x}Mg_xTe$ thin-film alloy, the Mg content, and therefore the band gap, is easily tunable by controlling the CdTe and Mg fluxes with source temperature. The co-sublimation process is repeatable, fast, and scalable to large areas, making it suitable for manufacturing. Additional development is needed to improve spatial band gap uniformity of films grown with current deposition hardware. Optical, morphological, and structural properties of co-sublimation grown $Cd_{1-x}Mg_xTe$ films were studied to investigate the impact of Mg incorporation. The relationship between Mg composition of the films, measured using EDS, and the optical band gap shows a linear correlation similar to previous work. SEM images of $Cd_{1-x}Mg_xTe$ films

show a decrease of grain size with Mg incorporation. GAXRD measurements of $Cd_{1-x}Mg_xTe$ films indicated a zinc blende structure with consistent preferred orientation as x increases. Furthermore, the lattice constant decreases with Mg incorporation and the $Cd_{1-x}Mg_xTe$ films are deposited with a small tensile stress.

Chapter 4

Grain-Level Epitaxial Growth of CdMgTe Thin Films onto CdS/CdTe Solar Cells for Electron Reflector Applications[1]

[1]This chapter in its entirety has been submitted for publication as a journal article as:
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Below is a list of authors and their contribution the presented work:

P.S. Kobyakov: For this study, Mr. Kobyakov helped make the samples, prepared the samples for material analysis, performed SEM, EDS, GAXRD, and SWLI characterization, analyzed data, and interpreted the results. Additionally, he prepared the figures, wrote and edited the manuscript, and submitted the work to the journal.

A. Abbas: Mr. Abbas performed the TEM, EDS, and EBSD material characterization, analyzed the data, and interpreted the results. He also helped with manuscript editing and figure preparation.

D.E. Swanson: Mr. Swanson helped with sample preparation, result interpretation, and editing of the manuscript.

J.M. Raguse: Mr. Raguse was involved with preparation of the studied samples, helped interpret the results, and helped to edit the manuscript.

4.1 Overview

The efficiency of CdS/CdTe solar cells could be improved by incorporating an electron reflector (ER) film at the back surface of the CdTe absorber. One strong candidate for the electron reflector layer is the higher band gap $Cd_{1-x}Mg_xTe$ (CMT) alloy. CMT thin films were deposited onto $CdCl_2$-treated polycrystalline CdS/CdTe films at different substrate temperatures. The CMT films and CdTe/CMT interfaces were characterized using SEM, EDS, XRD, SWLI, TEM, and EBSD. At low deposition temperatures, where the underlying CdS/CdTe device performance does not degrade, the CMT films show non-uniform coverage on CdTe. Higher deposition temperatures improve the CMT coverage, but the underlying devices degrade in performance. TEM and EBSD analyses show the deposited CMT grains having the same grain orientation, grain boundaries, and even continuation of structural defects as the underlying CdTe grains, suggesting CMT growth on polycrystalline CdTe is epitaxial at the grain level. While epitaxial growth is beneficial to reduce recombination at the CdTe/CMT interface, J-V measurement of ER cells demonstrate decreased performance at higher CMT deposition temperatures and no significant improvements at lower temperatures. The data suggests an optimized passivation treatment after CMT deposition will be necessary to activate CMT films and improve CdS/CdTe/CMT electron reflector device performance.

J. Drayton: Dr. Drayton helped with sample preparation, result interpretation, and editing of the manuscript.

J.M. Walls: Prof. Walls provided guidance to the material characterization portion of the study, contributed to interpretation of the result, and edited the manuscript.

J.R. Sites: Prof. Sites provided guidance on sample development, material characterization, contributed to interpretation of the result, and edited the manuscript.

W.S. Sampath: Prof. Sampath provided guidance on sample development and material characterization. He also helped to interpret the results and edited the manuscript.

4.2 Introduction

The record efficiency of CdS/CdTe solar cells [12] is significantly below its Shockley-Queisser limit for the band gap of CdTe [13]. The efficiency is limited primarily due to the low open-circuit voltage, V_{OC}, of record cells (0.8573 V) [12], which is low for the approximately 1.5 eV band gap of CdTe. For a similar band gap, GaAs solar cells have higher efficiency in part due to V_{OC}'s above 1 V [12]. One way to improve the V_{OC} of CdS/CdTe cells is to implement an electron reflector (ER) layer into the device [11]. The ER layer adds a conduction-band barrier to the back of the device to reduce back-surface recombination [50], which leads to higher voltages. Only a 0.2 eV conduction band barrier is needed to improve the voltage by up to 200 mV [26,50]. Although there are numerous ways to add a conduction-band barrier, one way would be to deposit a higher band gap film at the back of CdTe [26,50]. One suitable higher band gap material is the alloy $Cd_{1-x}Mg_xTe$ (CMT), whose band gap increases with a rise in Mg content [51]. An ideal ER structure includes a fully depleted CdS/CdTe cell with an added CMT layer about 50 to 150 nm thick and a band gap of about 1.7 to 1.9 eV [26]. For the CdS/CdTe/CMT ER structure to be successful, two things need to be considered: the passivation process to activate the structure and the quality of the CdTe/CMT interface.

The quality of the CdTe/CMT interface is a critical component for the function of ER structures. The addition of another thin film into the photovoltaic structure produces an additional interface that can be problematic for collection of charge carriers. Charge-carrier recombination at this interface can cause the V_{OC} to decrease, thus negating the positive effects of the ER structure [26]. Interfaces between heterogeneous materials can often lead to formation of defects that pin the Fermi level and allow charge recombination. This is especially true if the interface includes distinct grain boundaries or other structural defects. Therefore, a continuous interface between CdTe and CMT is preferred to reduce the interface recombination. The quality of CMT film deposition onto CdS/CdTe is an important step in the process to make sure the interface is clean. One benefit of using the CMT alloy

as the ER layer on CdTe thin films is the very low lattice mismatch [51] between the two semiconductors, which should lead to better quality interfaces.

The optimum passivation treatments for CdTe and $Cd_{1-x}Mg_xTe$ thin films differ significantly in both residual gas composition and passivation material. Simple CdS/CdTe structures benefit from having oxygen gas present during CdTe growth and vapor $CdCl_2$ passivation treatment, where the presence of oxygen increases CdS/CdTe intermixing [88] and likely reduces donor V_{Te} states [89] leading to higher CdTe doping. In contrast, $Cd_{1-x}Mg_xTe$ thin films degrade when oxygen is present during $CdCl_2$ or $CdCl_2/MgCl_2$ vapor passivation treatments [72, 74] because Mg has high affinity towards oxygen. Therefore, a reduction in oxygen during CMT film growth and during passivation is necessary. The dissimilar passivation treatments make it difficult to develop a single passivation process to optimize performance of the ER structure.

One possible way around this problem is to perform a two-step passivation treatment during processing of the CdS/CdTe/CMT structure. First, an oxygen rich $CdCl_2$ passivation would be performed on the CdS/CdTe structure, while a second oxygen free passivation would follow CMT growth. One important question of this sequence is the effect of CMT deposition on the $CdCl_2$-treated CdS/CdTe cell, as the CMT deposition temperature can negatively affect the performance of the underlying cell and CMT film quality. In this work, we take an in-depth look at the first step of this process sequence, i.e. CMT deposition on $CdCl_2$-treated CdS/CdTe structures. Our focus is on the material properties of the deposited CMT film, the quality of the CdTe/CMT interface, and how the CMT deposition process may affect the underlying cells. We present results of CMT film growth, interface quality, and cell performance of preliminary ER structures at various CMT deposition temperatures.

4.3 Experimental Details

The starting structures, soda-lime glass/SnO_x:F/CdS/CdTe, were grown and $CdCl_2$ treated using the Advanced Research and Deposition System (ARDS) at Colorado State Univer-

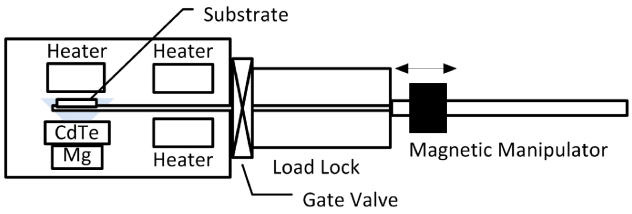

Figure 4.1: Side-view schematic of the Deposition Research Chamber used for deposition of $Cd_{1-x}Mg_xTe$ thin films.

sity. The ARDS, described previously [81, 82], is an in-line cluster tool that deposits CdS and CdTe thin films using a close-space sublimation (CSS) process on TCO-coated glass substrates and performs the necessary $CdCl_2$ and Cu treatments. For this study, typical 120nm CdS/1.75μm CdTe film stacks were made and $CdCl_2$ treated using the CSU standard process [82].

Deposition of CMT films has been demonstrated by several techniques, including sputtering [69, 72] and co-evaporation [74, 76, 87]. During our development process, we have replicated both sputtering and co-evaporation [79] with good success. We have also developed a novel co-sublimation process that allows fast and repeatable deposition of CMT thin films [90]. The co-sublimation method uses sublimated vapor from CdTe and Mg sources and mixes them prior to condensation on the substrate. The technique produces repeatable and easily tunable CMT alloy thin films [90]. In this study, CMT films were grown on treated CdS/CdTe samples using this co-sublimation method in the Deposition Research Chamber (Fig. 4.1). CMT films of about 130 to 150 nm thickness were deposited onto $CdCl_2$-treated CdS/CdTe structures at substrate temperatures ranging from 400 to 480 °C. After deposition, the films were analyzed using SEM, EDS, XRD, and SWLI techniques. Some films were also studied using cross-sectional TEM and EBSD. Small area devices of the structures were made by painting the films with conductive Carbon and Nickel acrylic paint and selectively delineating the cell area.

Films were imaged using a JEOL JSM-6500F field emission Scanning Electron Microscope (SEM) fitted with Energy Dispersive X-ray Spectroscopy (EDS) for composition analysis.

Glancing Angle X-Ray Diffraction (GAXRD) was performed with a Bruker D-8 Discover diffractometer utilizing Cu K_α radiation ($\lambda = 1.5418\mathring{A}$) at 2° incidence. Surface roughness of the deposited films was characterized using a Scanning White Light Interferometry (SWLI) using a Zygo NV7300 interferometer utilizing a 100X magnification objective and 2.0X nominal zoom. Transmission Electron Microscopy (TEM) was used to investigate the detailed microstructure of the cells. TEM samples were prepared by Focused Ion Beam (FIB) milling using a dual beam FEI Nova 600 Nanolab. A standard in-situ lift out method was used to prepare cross-sectional samples through the coating into the glass substrate. A platinum over-layer was deposited to define the surface of the samples and homogenize the final thinning of the samples. The TEM bright-field images with corresponding EDS chemical distribution maps were carried out in a FEI Tecnai F20 operating at 200 kV in STEM mode, equipped with an Oxford Instruments X-Max 80 mm^2 windowless Silicon Drift Detector (SDD) Energy-Dispersive Spectrometer (EDS). TEM bright-field images were obtained using a JEOL JEM 2000FX operating at 200 kV. The dual beam was also equipped with a Hikari Electron Backscatter Diffraction (EBSD) camera. EBSD maps were collected using a high current (nominally 20 nA) at 30 kV. The resolution of EBSD can be improved from tens of nanometers to around 5 nm if an electron transparent film is produced and positioned at 20° to the horizontal [91, 92]. Kikuchi patterns can be produced and collected from transmitted electrons from the underside of the sample; this Transmission Electron Backscatter Diffraction (T-EBSD) setup is shown in Fig. 4.2. This increases the spatial resolution of EBSD which is advantageous for this study due to the small grain sizes and structural defects. Performance of the cells was studied with a simulated 1.5AM light spectrum made by ABET Technologies 10500 Solar Simulator and a Keithley 2420 3A Sourcemeter.

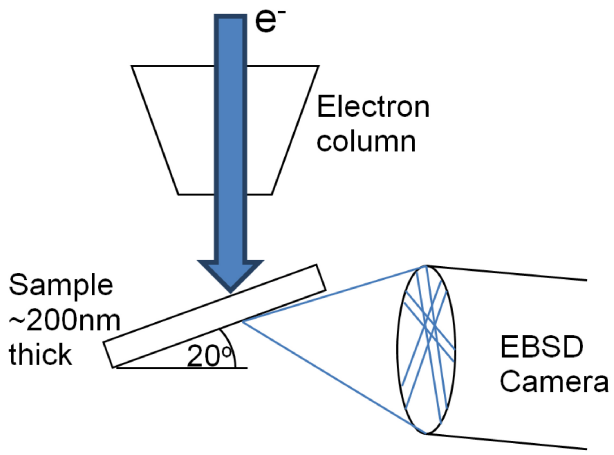

Figure 4.2: Schematic of Transmission Electron Backscatter Diffraction (T-EBSD) setup. Illustration courtesy of A. Abbas.

4.4 Results

4.4.1 Uniformity of CMT Growth

Figure 4.3 shows the SEM images of CMT films deposited on treated CdS/CdTe structures at various substrate temperatures. High temperature (460°C and 480°C) deposition of CMT (Figs. 4.3c and 4.3d) shows a crystal structure similar to CdTe films deposited using our typical CSS process [82], which is also performed around 480°C substrate temperature. Both the CMT film shown in Figs. 4.3c and 4.3d and our typical polycrystalline CdTe show grain size of about 1 μm and a coalesced film structure [93]. At colder substrate temperatures (400°C), the CMT appears to deposit with non-uniform coverage (Fig. 4.3a). The images show the surface grains of the CMT are separated and not coalesced. Surface grains have varying grain sizes, with nanometer sized grains seen in-between larger grains. It is suspected that non-uniform CMT coverage may be the start of columnar grain growth associated with low temperature deposition of thin films [94]. A lack of surface mobility of the deposited atoms and fast condensation on the surface leads to columnar grain formation with substantial space in-between the grains [94]. As the temperature is raised from

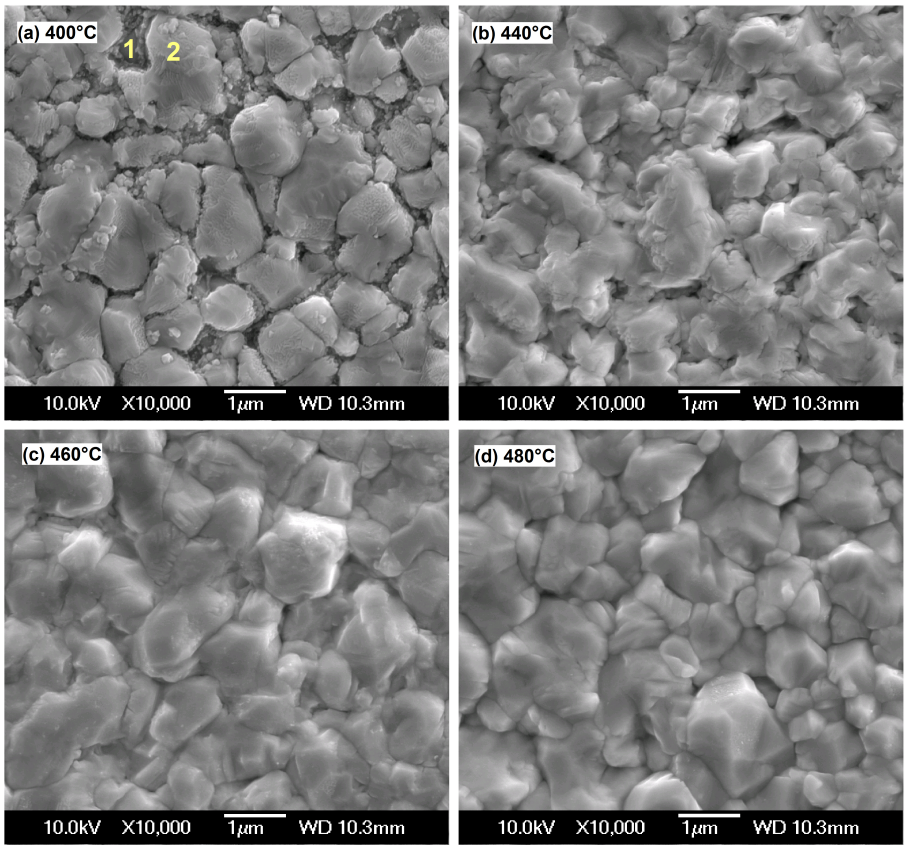

Figure 4.3: SEM images of 150 nm CMT films deposited onto $CdCl_2$-treated CdS/CdTe polycrystalline films at various substrate temperatures: (a) 400°C, (b) 440°C, (c) 460°C, and (d) 480°C.

400°C to 440°C, the smaller grains become larger and begin to coalesce to the large grains (Fig. 4.3b). At 440°C substrate temperature, CMT growth may be in transition from columnar (Fig. 4.3a) to uniform growth (Fig. 4.3c, 4.3d). As the substrate temperature increases further to 460 and 480°C (Fig. 4.3c, 4.3d), the CMT coverage becomes uniform and the films become coalescent.

The uniformity of coverage was studied with EDS. For CMT films deposited at higher substrate temperatures, where the coverage appears to be uniform, EDS shows a spatially uniform signal of Mg composition. For lower temperature deposition, EDS shows a significant decrease in Mg content in-between the large CMT grains. Figure 4.4 shows the EDS signals at two points of a CMT film grown at 400°C substrate temperature onto $CdCl_2$-treated

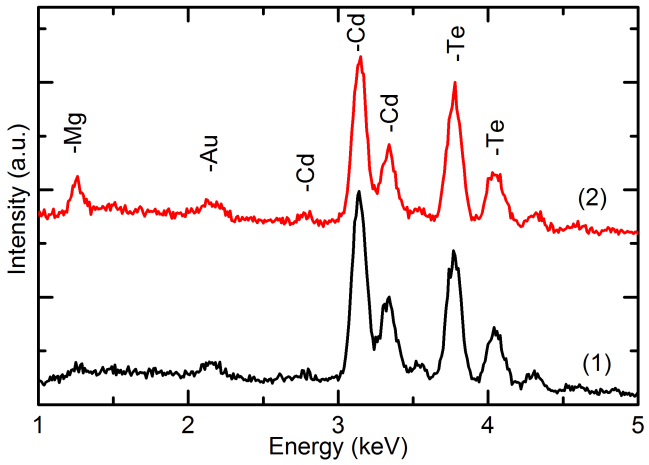

Figure 4.4: EDS point spectra at locations labeled in Fig. 4.3(a). Characteristic x-ray peaks are labeled.

CdS/CdTe. The location of these two points is marked in Fig. 4.3a. Position 1 is measured at the trough in-between larger grains. The EDS spectrum shows negligible Mg signal, indicating little to no Mg is present. Position 2, which is located at the top of the grain, shows a strong Mg signal indicating higher Mg content and thicker CMT at this location. Atomic concentration analysis of the EDS spectra estimates the composition of all films to be $Cd_{0.89}Mg_{0.11}Te$. The EDS measured value of composition, however, underestimates the true composition. The discrepancy occurs because the measured EDS volume is deeper than the CMT film thickness. A Monte Carlo calculation shows an electron beam penetration at a 10 kV acceleration voltage, which was used for SEM and EDS measurement, to be about 400 nm deep, which is significantly larger than the approximately 150 nm thick CMT film. Lowering the accelerating voltage below 10 kV, and therefore reducing the measured volume, is possible but reduces or eliminates the higher energy signals from Cd and Te atoms and makes atomic concentration calculations more inaccurate than they already are on rough surfaces.

Additional EDS mapping was done in cross-section on ultrathin samples prepped for TEM analysis. The thin samples allow better spatial resolution than a thick sample or a cleaved cross section. Figure 4.5 shows cross-sectional electron images of two CdS/CdTe/CMT

Table 4.1: Mean surface roughness of CdS/CdTe/CMT structures at various substrate temperatures during CMT deposition. Roughness measured by SWLI.

Temperature (°C)	Surface Roughness (nm)
400	79.5 ± 2.5
440	109.8 ± 1.9
460	68.3 ± 0.9
480	63.1 ± 0.1

structures, where the CMT was deposited at 400°C (Fig. 4.5a) or 470°C (Fig. 4.5b) substrate temperatures. Insets in Fig. 4.5 show EDS chemical maps of Mg, which identifies the CMT layer at the back of the device. Low temperature deposition (Fig. 4.5a) shows a very non-uniform CMT film, with varying thickness of Mg content and indication of gaps in the CMT film. As the deposition temperature increases (Fig. 4.5b), the EDS Mg signal becomes smooth and complete, indicating a uniform CMT film thickness. This correlates to the planar SEM images shown in Fig. 4.3 and further indicates non-uniformity of CMT coverage when it is grown at low substrate temperatures.

The surface roughness of the deposited CMT films was studied using SWLI. Table 4.1 shows the average surface roughness as a function of substrate deposition temperature during CMT film growth. As the substrate temperature increases, the film roughness first increases from the highly disoriented films grown at 400°C (Fig. 4.3a) to 440°C (Fig. 4.3b), where the film is still poorly coalesced. As the substrate temperatures increase further, the films become coalesced (Figs. 4.3c and 4.3d) and the roughness decreases because the gaps in-between grains are closed up. The high-temperature roughness is similar to that of 2 μm CdTe films produced by CSS [93], indicating the CMT film coverage is likely uniform. The underlying CdTe roughness is assumed to be nominally the same from sample to sample.

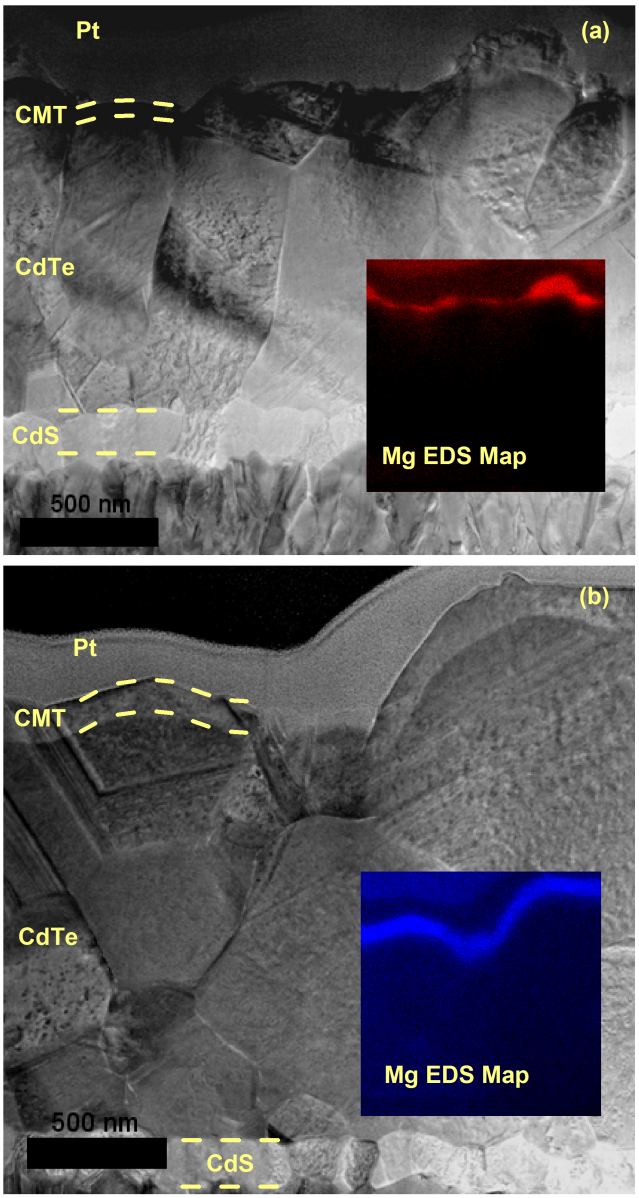

Figure 4.5: Electron image and corresponding EDS map of CdS/CdTe/CMT structures with CMT deposited at (a) 400°C and (b) 470°C. Imaging courtesy of A. Abbas.

4.4.2 Structural Analysis

GAXRD was performed on samples from Fig. 4.3. The GAXRD spectra, shown in Fig. 4.6, were collected at an incidence of 2 degrees. The data were first smoothed using the Savitzky-

Golay method, the background was subtracted using the Sommerveld approximation, and Cu $K_{\alpha 2}$ data were stripped using the Rachinger method. Normalized spectra (Fig. 4.6) show the films have the cubic zinc blende structure associated with CdTe and CMT films. The location of the peaks does not change with deposition temperature, indicating a similar lattice constant between the films. Since the CMT alloy also has the zinc blende structure with a similar lattice constant to CdTe, which only moves a little when the film is alloyed [90], the measured peaks are of both the base CdTe film and the 150 nm thick CMT film. Furthermore, at this incidence, the incoming X-rays penetrate about 1 μm into the film, and thus the majority of the signal is from the CdTe film and not the 150 nm CMT over layer. As deposition temperature increases, the (220) peak increases in intensity relative to other peaks. This change is small and likely a natural variation of the process. No additional diffraction peaks are seen in the spectra, indicating no other significant material phases are present in the film structure at the measured depth, such as Cd or Mg metal.

TEM and EBSD were performed on CdS/CdTe/CMT structures where the CMT film was deposited at 400°C and 470°C substrate temperatures. Figure 4.7 shows the TEM and EBSD images of the device cross sections with the individual films labeled. A clear interface between the TCO, CdS, and CdTe is seen in the images. The interface between CMT and CdTe is harder to distinguish due to the conformal growth of CMT on the CdTe layer. The CMT layer appears lighter in the TEM images due to lower atomic weight of Mg atoms compared to Cd. The CMT film seems thicker for the lower deposition temperature sample (Fig. 4.7a) than for higher temperature (Fig. 4.7b). In both cases, CMT films appear to be conformal to the underlying CdTe grains, show similar grain boundaries, and show some continuation of microstructural defects such as twins and stacking faults. Coverage appears to be uniform in both temperature cases, but only a small region of the structure is shown. Gaps and non-uniformity of CMT films, similar to those shown in Fig. 4.5, were seen with the 400°C sample in other regions during the TEM analysis. EBSD measurements (Figs. 4.7c and 4.7d) of the film structure show the orientation of the grains. It is important to note here, EBSD in Fig. 4.7c was measured at a slightly different location from Fig. 4.7a, while

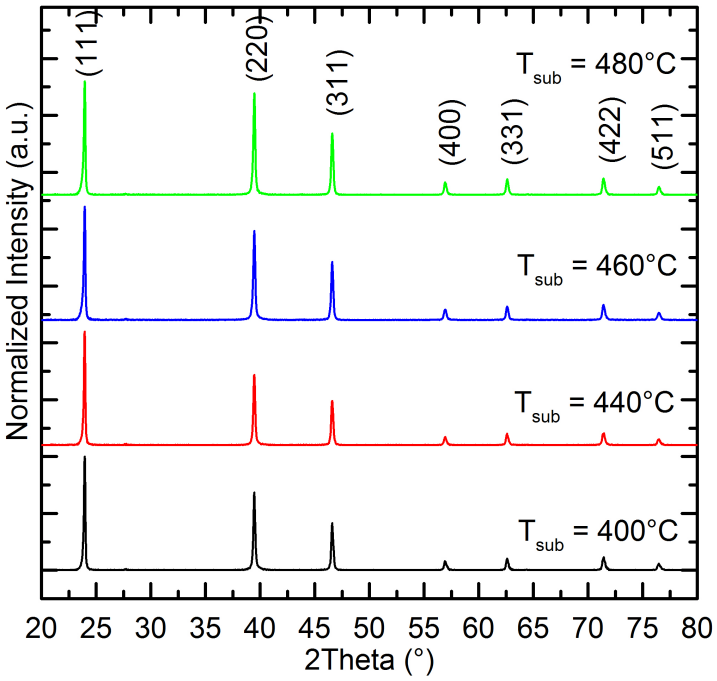

Figure 4.6: GAXRD spectra of CdS/CdTe/CMT structures at various CMT deposition substrate temperatures. Zinc blende peaks are labeled with their Miller indices.

Figs. 4.7b and 4.7d are relatively close to the same position. The EBSD coloring of each grain indicates areas of similar orientation in the polycrystalline CdTe and CMT films. Despite the added CMT film, a clear CdTe/CMT interface cannot be seen in the EBSD. At both deposition temperatures, the CMT grains appear to have the same grain orientation as the underlying CdTe. This indicates the CMT growth is epitaxial on CdTe at both low and high deposition temperatures used in this study.

Evidence of epitaxial growth is also seen in some of our previously developed samples, where CMT film was deposited by co-evaporation at 400°C to make the CdS/CdTe/CMT structure [79]. Although the growth rate is slower, co-evaporation deposition is qualitatively identical to co-sublimation deposition. Figure 4.8 shows an STEM image of the CdTe and CMT interface and high-resolution TEM images of both layers. The CdTe/CMT interface is clean and the CMT layer appears to take on the underlying microstructure of the CdTe

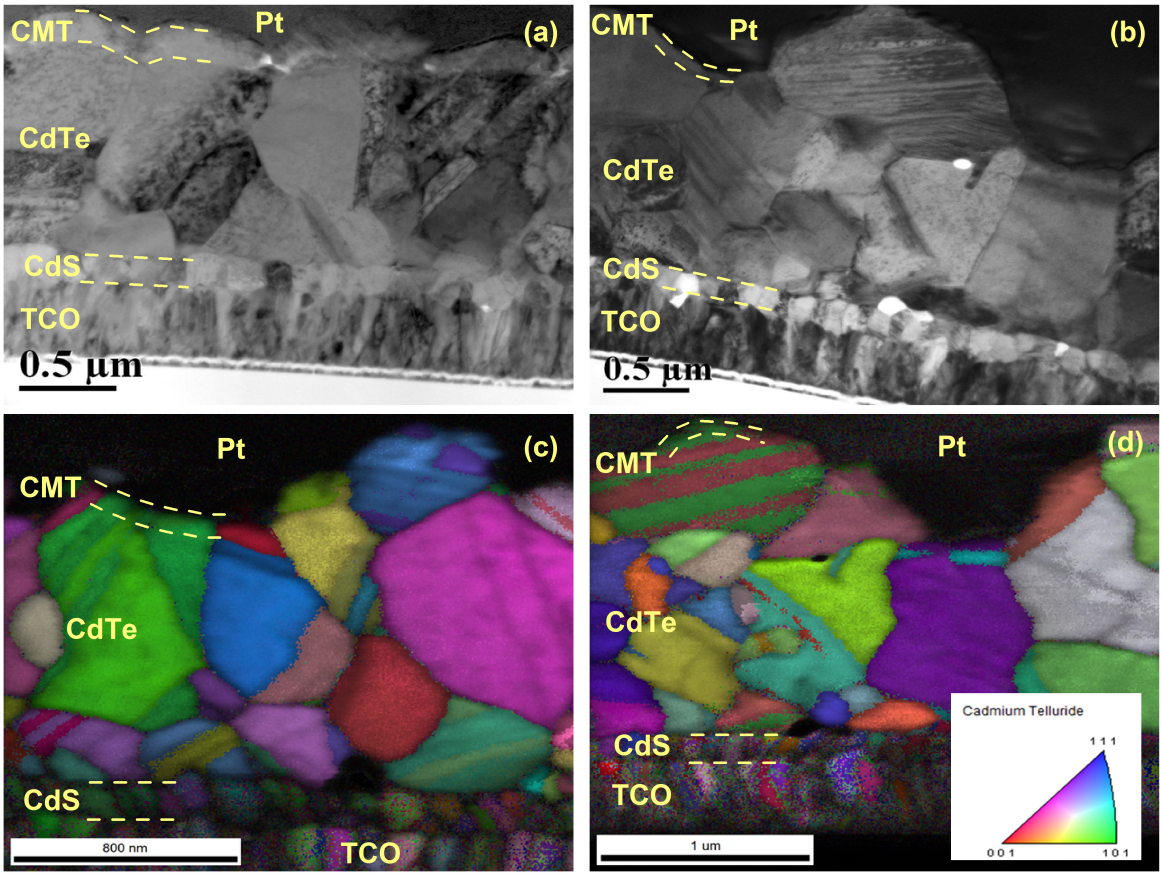

Figure 4.7: Cross-sectional TEM images (top) and EBSD images (bottom) of CdS/CdTe/CMT structures with CMT grown at (a, c) 400°C and (b, d) 470°C. Imaging courtesy of A. Abbas.

film, including the grain boundary between the two films. HRTEM images shows that both films are cubic and have a similar orientation, indicating epitaxial CMT growth.

To further confirm the epitaxial growth of CMT on CdTe, 800 nm CMT film was deposited onto 1 μm thick CdTe and analyzed with TEM and EBSD (Fig. 4.9). In this case, CMT was deposited at a substrate temperature of 480°C using the co-sublimation method [90]. From the TEM image, (Fig. 4.9top), the CdTe/CMT interface can be clearly seen and it appears to be distinct and the transition from CdTe to CMT is abrupt. Figure 4.9top shows the CMT film has the same grain boundaries as the underlying CdTe. Furthermore, the stacking faults, dislocations, and twin boundaries of the CdTe grains are continued in the

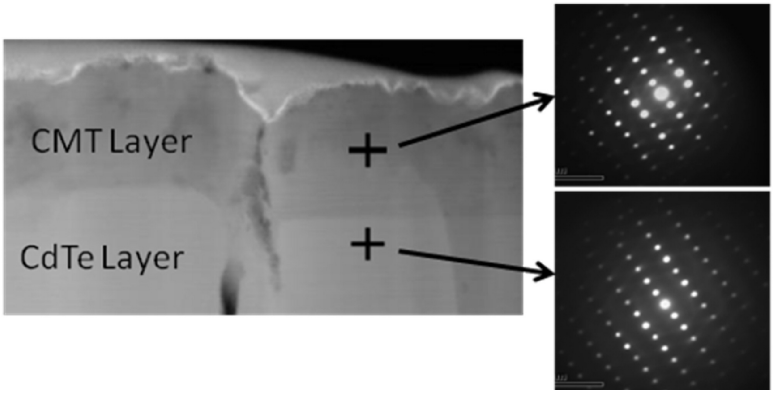

Figure 4.8: STEM images of CMT and CdTe layers showing similar lattice orientation and lattice constant. The CMT layer was deposited on CdTe at 400°C. Imaging courtesy of A. Abbas.

CMT grains. EBSD (Fig. 4.9bottom) shows that the CMT grains have the same orientation as the CdTe grains underneath, further indicating that growth is grain-level epitaxial.

4.4.3 Device Performance

Small area devices (approximately 1 cm^2) were made on the CdS/CdTe/CMT structures to test the J-V performance. The effect of the CMT film on device performance, however, needs to be separated from the effect of the thermal treatment the underlying structures go through during CMT deposition. This effect was studied by taking the $CdCl_2$-treated CdS/CdTe structures through an identical heating profile used for CMT deposition and finished with Cu and C/Ni back electrodes to make devices. The effect of reheat temperature on J-V performance is shown in Fig. 4.10. Low temperature reheats (400°C) has almost identical performance to the no reheat baseline. Once reheat temperature reaches 460°C, the cells begin to lose V_{OC}, FF, and J_{SC}, leading to lower efficiency. At the higher temperature, the excess heat is starting to degrade the activated CdTe device. This temperature also coincides with an improvement in CMT film coalescence as seen in Fig. 4.3, indicating the processes may be linked. J-V curves of CdS/CdTe/CMT devices, which were finished with Cu back contacts and C/Ni electrodes, are also shown in Fig. 4.10. It is important to note

here, without the Cu treatment, the cells would show very high resistance and show minimal photo-generated current. At low temperature, 400°C, the CMT film does not change the cell dramatically, where only a slight reduction in efficiency is seen. Once the deposition temperature increases, the cells begin to lose V_{OC}, J_{SC}, and FF. Although all parameters are lower, the 440°C cell has relatively good series resistance, as indicated by the curves slope at $J = 0$ mA/cm^2. At higher deposition temperatures (460 and 480°C), the slope decreases and the cells demonstrate behavior associated with a barrier in the structure. As seen from Fig. 4.3, this transition to barrier formation (from 440 to 460°C) occurs when the coverage of the CMT film transitions to complete uniformity.

4.5 Discussion

Structural characterization and imaging of CdS/CdTe/CMT ER structures shows grain-level epitaxial growth of $Cd_{1-x}Mg_xTe$ on polycrystalline CdTe thin films. Irrespective of substrate temperature during deposition, the CMT films demonstrate the same grain orientation as the underlying CdTe and a continuation of structural defects from CdTe into the CMT layer. This is an important advancement towards producing higher efficiency ER devices. Since CMT films are epitaxial on CdTe, the potential for electronic defect states at the CdTe/CMT interface is significantly reduced, indicating the quality of this interface is likely sufficient to produce good ER devices. Despite non-uniform coverage at low temperatures, the CMT film growth is epitaxial at both low and high temperatures, suggesting another mechanism is responsible for poor uniformity of the CMT film at low temperatures. Surface contamination of the CdTe film may be one possible source of poor CMT growth at low temperature. For example, the presence of residual $CdCl_2$ or oxychlorides [95], such as $Cd_3Cl_2O_2$, on the surface of treated CdTe films could impede uniform growth of the CMT film. Heating the substrate for CMT deposition to 460°C and above may thermally clean the CdTe surface, thus leading to uniform CMT films. At lower deposition temperatures (400°C), residual $CdCl_2$ or $Cd_3Cl_2O_2$ compounds are not sublimated off and could inhibit

formation of the CMT layer, thus leading to non-uniform coverage.

The J-V results (Fig. 4.10) provide interesting information about the ER devices and the CMT process. First, the underlying CdS/CdTe cells begin to lose efficiency as the CMT deposition temperature increases. The process for this efficiency loss is not completely understood, but likely stems from induced recrystallization of CdTe, or possible re-sublimation of Cl compounds formed during the passivation treatment. Secondly, J-V of higher temperature CdS/CdTe/CMT structures (Fig. 4.10) show a barrier behavior in the solar cell. It is apparent that this barrier behavior is associated with the CMT film because a similar trend is not seen in the reheat only samples. One source of the added barrier could be a high valence-band offset between CdTe and CMT. The higher band gap of the $Cd_{1-x}Mg_xTe$ alloy produces both a conduction-band offset (CBO) and a valence-band offset (VBO) with CdTe. The CBO is desired for the ER structure, as it leads to lower back-surface recombination and hence increases V_{OC} [11,26,50]. The VBO, however, can become problematic to current conduction if it is sufficiently large. A back surface VBO can impede injection of holes from the semiconductor into the back metal when the cells are operating in the power quadrant (i.e. at forward voltage and under light illumination). The ratio of band gap change attributed to VBO and CBO between CdTe and CMT has been estimated to be 35% VBO, 65% CBO [55]. Therefore, if the $Cd_{1-x}Mg_xTe$ band gap is high enough, the VBO may become high enough to impede current flow. The deposited CMT films in Fig. 4.10 devices had an $E_g \approx 1.86$ eV, which would make an approximately 0.13 eV VBO. Additional studies are under way to directly measure this value and whether it is significant enough to cause the barrier behavior in the cells. The VBO between CMT and CdTe may be one of several contributions to a hole barrier at the back of the device. Poor doping of the CMT film and a Schottky back barrier due to the CMT/metal interface could also contribute to the total barrier effect. The back barrier to holes can be reduced by increasing the doping density of the CMT films, which could be accomplished with passivation treatment. The barrier behavior does not appear at lower deposition temperatures, leading to better device performance. It is likely that the coverage of the CMT film on the CdTe has an impact on the cumulative performance of the

device. When the coverage is complete, the cells demonstrate the barrier behavior. However, if the coverage is incomplete (as is the case with lower temperature depositions), the gaps in the CMT film could form conduction paths that minimize the effects of the CMT film locally, thus reducing their cumulative effect on the whole cell.

Despite the non-uniformity, epitaxial growth of CMT on CdTe at a wide range of substrate temperatures provides added flexibility to the deposition process and could be useful in optimizing the manufacturing of ER devices. For example, improvement of CMT coverage at lower temperatures could be possible with better cleaning and or etching of the treated CdTe surface. Additionally, a second Cl-based passivation treatment will likely be necessary to improve the ER device performance. A passivation treatment after CMT growth will improve doping of the added CMT film and can reactivate the underlying CdTe if it degrades during CMT deposition temperature.

4.6 Conclusions

$Cd_{1-x}Mg_xTe$ thin films were deposited onto $CdCl_2$-treated CdS/CdTe structures at different substrate temperatures ranging from 400°C to 480°C. At low temperature, the coverage of CMT films is non-uniform. As the substrate temperature increases, the deposited CMT film becomes uniform and show similar microstructure to the underlying polycrystalline CdTe. Despite these differences, both low and high temperature growth conditions produce grain-level epitaxial growth of CMT on polycrystalline CdTe, where CMT grains take on the same orientation, grain boundaries, and structural defects as the underlying CdTe grains. Preliminary J-V results indicate the degradation of the underlying CdS/CdTe cell at CMT deposition temperatures above 450°C. Furthermore, cells with uniform CMT film coverage show an electronic barrier in the device, which is associated with either a large valance band offset between CdTe and CMT or a low doping of as-deposited CMT films. A secondary, optimized passivation treatment will be necessary to improve ER device performance by improving doping of the CMT film and reactivating the underlying CdS/CdTe cell.

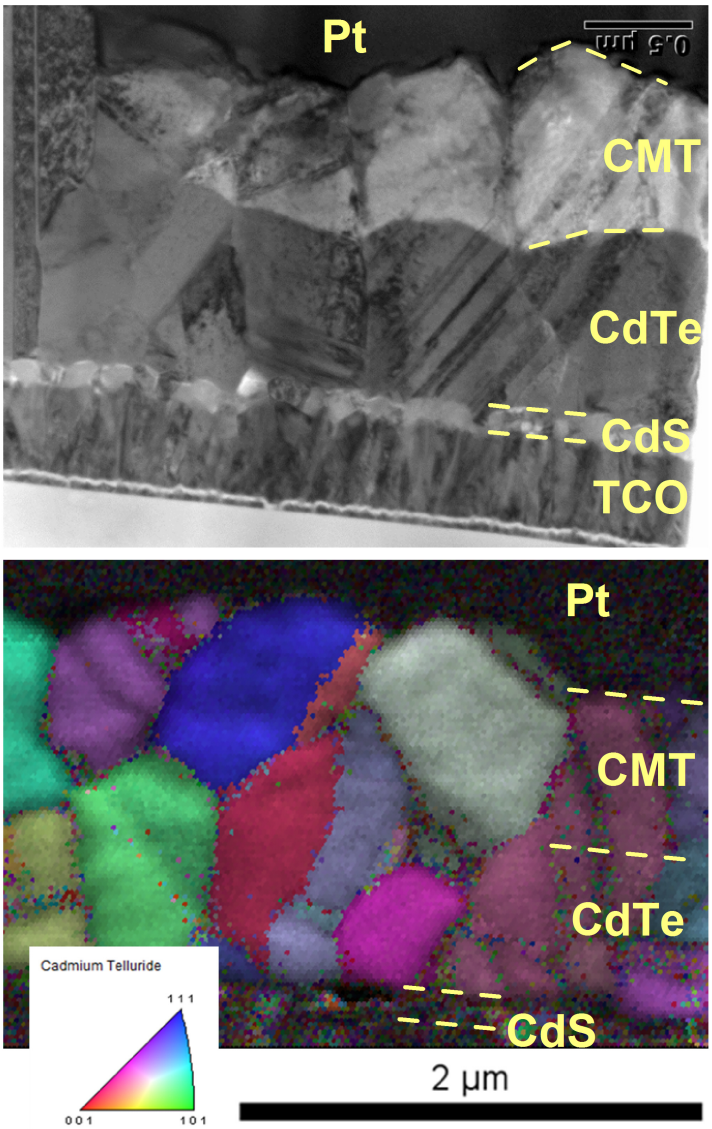

Figure 4.9: TEM image (top) and EBSD map (bottom) of a CdS/1 μm CdTe/ 0.8 μm CMT structure. CMT was deposited at 480°C. Imaging courtesy of A. Abbas.

Sample (Temp)	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Eff (%)
Baseline	781	21.2	65	10.8
Reheat (400°C)	775	21.3	67	11.0
Reheat (460°C)	678	19.8	68	7.6
CMT(400°C)	779	20.0	66	10.3
CMT(440°C)	695	15.1	48	5.0
CMT(460°C)	661	16.1	38	4.0
CMT(480°C)	616	13.0	32	2.5

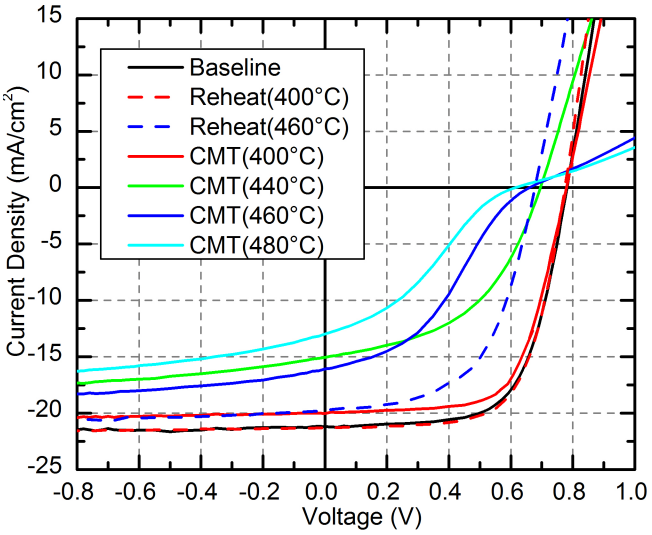

Figure 4.10: J-V curves and parameters of various treated CdS/1.75 μm CdTe cells: baseline, reheated to simulate CMT deposition, and with a 150 nm CMT film ($E_g \approx 1.85$ eV). Temperatures in parenthesis indicate substrate temperature during reheat or CMT deposition. All cells were treated with Cu and finished with C/Ni back electrodes.

Chapter 5

Passivation Treatment Effects on CdMgTe Thin Films[1]

[1]Below is a description of contributors and their involvement to the work presented in this chapter:

P.S. Kobyakov: For this study, Mr. Kobyakov helped make the samples, prepared the samples for material analysis, performed SEM, EDS, GAXRD, and SWLI characterization, analyzed data, and interpreted the results. Additionally, he prepared the figures, wrote and edited the manuscript, and submitted the work to the conference.

A. Abbas: Mr. Abbas performed the TEM, EDS, and EBSD material characterization, analyzed the data, and interpreted the results.

D.E. Swanson: Mr. Swanson helped with sample preparation, interpreting results, and editing of the manuscript.

J.M. Raguse: Mr. Raguse was involved with preparation of the studied samples, and helped interpret the results.

J. Drayton: Dr. Drayton helped with sample preparation, result interpretation, and editing of the manuscript.

J.M. Walls: Prof. Walls provided guidance to the material characterization portion of the study and contributed to interpretation of the results.

J.R. Sites: Prof. Sites provided guidance on sample development and material characterization. He also contributed to interpretation of the result and editing of the manuscript.

5.1 Overview

Polycrystalline CMT thin films could be used to improve CdS/CdTe solar cell efficiency. For example, CMT could be the top absorber in tandem cells or an electron reflector layer in single junction cells. Passivation of CMT films is an important step in development of either of these structures. In this chapter, material properties of CMT films before and after passivation treatment are presented. First, various band gap CMT films and CdS/CMT structures underwent $CdCl_2$-passivation treatment typically used for CdTe cells. After this treatment, the optical band gap of the films shifted to that of CdTe and thicker oxides were found on the rear surface, suggesting Mg loss and oxide formation due to treatment. TEM and EDS measurements showed Mg reduction at CMT grain boundaries. Possible use of $MgCl_2$ in addition to $CdCl_2$ was investigated as a solution to CMT band gap degradation. Preliminary results of $MgCl_2/CdCl_2$ treatment show less band gap degradation when residual oxygen is reduced during treatment. Additional studies on this passivation method are proposed.

5.2 Introduction

Thin films of the ternary alloy $Cd_{1-x}Mg_xTe$ (CMT) have potential to improve the efficiency of CdS/CdTe solar cells. First, a higher band gap absorber film, such as $Cd_{1-x}Mg_xTe$, can be used as a top cell in tandem devices [67, 72, 74]. In the second method, CMT thin films can be used as an electron reflector film in CdS/CdTe devices to improve open-circuit voltage [11, 50]. To make these structures successful, polycrystalline CMT films need to be treated to electronically activate the film. Treatment of CMT films has been performed with vapor heat treatment utilizing either $CdCl_2$ sources [72, 74, 76] or $CdCl_2/MgCl_2$ mixtures [83, 96]. The residual gas during heat treatment has been shown to be important

W.S. Sampath: Prof. Sampath provided guidance on sample development and material characterization. He also helped to interpret the results and edit the manuscript.

for the stability of CMT films. The presence of oxygen, either from using dry air or oxygen flow, during treatment has been shown to reduce the CMT band gap [72, 74], likely due to formation of MgO and CdTe phases in the CMT film [74, 76]. The band gap reduction after Cl treatment is also accompanied with significant material changes, including possible recrystallization, lattice constant relaxation, and resistivity changes [74]. To date, CdS/CMT cells have been generated with typical Cu/Au or ZnTe:Cu back contacts. With passivation and Cu optimization, CdS/CMT cells have reached efficiencies above 9.5% [76]. Despite these efficiencies, the effect of Cl treatment parameters on CMT material properties is not fully understood. In this work, we investigate the material changes associated with passivation treatment of our co-sublimation deposited CMT films, CdS/CMT devices, and CdS/CdTe/CMT ER structures utilizing our typical $CdCl_2$ treatment. We also show preliminary results and propose additional work to investigate $MgCl_2$ as a source material for treatment of CMT films.

5.3 Experimental Details

The CMT films were grown on either soda lime glass (SLG) or on commercially available TEC10 samples (SLG/SnO_x:F) coated with approximately 120 nm of CSS deposited CdS. CMT films were grown using the previously described co-sublimation method [83,90]. CMT films were grown at 460-500°C substrate temperature in 20-60 mTorr of Argon gas at a growth rate of approximately 500 nm/min.

Initially, chlorine treatment was performed using our standard method for passivation of our CdS/CdTe cells, which has been used to make CdS/CdTe cells with NREL verified efficiencies above 15% [82]. In this method, a layer of $CdCl_2$ is deposited on the film stack using a CSS process and then annealed at 400°C for about 3 minutes under 40 mTorr of nitrogen vacuum. After annealing, the film is removed from the vacuum chamber and excess $CdCl_2$ is rinsed with de-ionized water. Material properties before and after the treatment were studied using optical measurements, SEM, EDS, TEM, and GAXRD techniques. Resistivity

of the films was measured using a two probe method.

A different passivation treatment was also explored for TEC10/CdS/CMT structures. This treatment is a vapor process performed in a glass bell jar utilizing a bank of IR lamps to heat the vapor source material and substrate via graphite crucibles and a top heating plate, respectively [97]. Figure 5.1 shows a schematic of the bell jar passivation tool. The source material in this study was a 50/50 mix by weight of $CdCl_2$ and $MgCl_2$ anhydrous beads. Before heat is applied, the chamber is purged by a vacuum pump and filled with 400 Torr of residual gas. Ultra high purity Argon and 2% Oxygen in Argon were used to study the effect of oxygen on films property changes. Treatment was performed at 400°C for 5 minutes.

The films were imaged using a JEOL JSM-6500F field emission Scanning Electron Microscope (SEM) outfitted with Energy Dispersive X-ray Spectroscopy (EDS) for composition analysis. Glancing Angle X-Ray Diffraction (GAXRD) was performed with a Bruker D-8 Discover utilizing Cu K_α radiation ($\lambda = 1.5418\mathring{A}$) at a 2° incidence. The TEM bright-field images with corresponding EDS chemical distribution maps were carried out in a FEI Tecnai F20 operating at 200 kV in STEM mode, equipped with an Oxford Instruments X-Max 80 mm^2 windowless Silicon Drift Detector (SDD) Energy-Dispersive Spectrometer (EDS). Some TEC10/CdS/CMT structures were made into small area devices by vapor treatment with Cu, painting the films with conductive Carbon and Nickel acrylic paint, and selectively delineating the cell area. Performance of the cells was studied with a simulated 1.5AM light spectrum made by ABET Technologies 10500 Solar Simulator and a Keithley 2420 3A Sourcemeter. To measure resistivity, two small regions of the films were coated with our typical C/Ni contacts and a current-voltage (I-V) measurement was taken between them. Resistivity is then calculated from the slope of the I-V curve, film thickness, and the distance between the points.

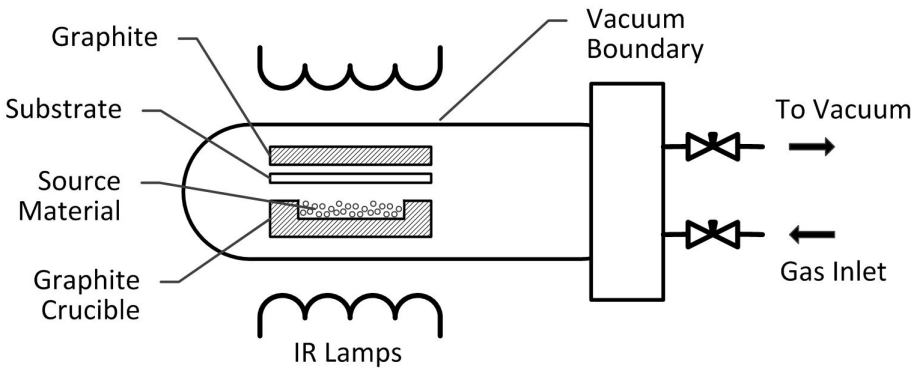

Figure 5.1: Schematic of Bell Jar for vapor Cl-based treatment of thin film structures.

5.4 Results

5.4.1 $CdCl_2$ Effects on CdS/CMT

Figure 5.2top shows transmission changes of CdS/1.7 μm CMT films before and after standard $CdCl_2$ treatment for various band gap CMT films. The band gaps of CMT films reduce towards CdTe band gap (∼830 nm), indicating possible Mg loss or CdTe phase formation. Similarly, reflection measurements (Fig. 5.2 bottom) show a shift towards CdTe band gap. Evidence of CMT still being present in the films after the treatment is indicated by the low wavelength transmission and the fringe patterns in reflection. This suggests not all of the film was converted to CdTe.

Figure 5.3 shows the SEM images of the high band gap CMT film (curves A and A' from Fig. 5.2top) before and after $CdCl_2$ treatment. The before treatment CMT film shows distinct grains with sharp edges and smooth faces. After passivation treatment, the film forms small nodules on the surface of the grain and grain boundaries and grain edges become rounded. Grain size does not appear to change with the treatment, suggesting the film likely did not recrystallize.

Possible Mg loss was evaluated using EDS measurements. Table 5.1 shows EDS measured composition in the films, including Mg, Cd, Te, and Cl atomic concentrations. The treatment

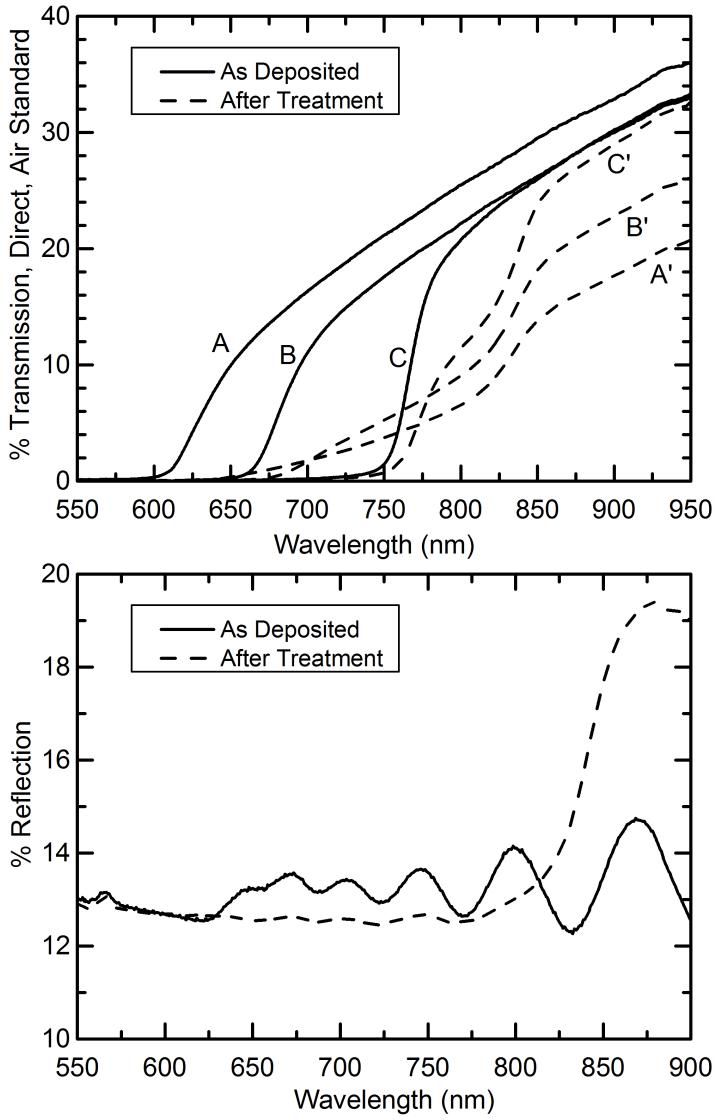

Figure 5.2: Transmission (top) and reflection (bottom) of CdS/CMT structures before and after $CdCl_2$ treatment.

clearly reduces the Mg content of the film and reduces the calculated alloy composition of the CMT film. Although the reduction is relatively small, it can have significant impact on film and device properties. Additionally, some chlorine has been added to the film and shows up in the EDS measurements.

GAXRD spectra were collected on CdS/CMT films to investigate possible recrystallization of the CMT film due to the treatment. Figure 5.4 shows the GAXRD spectra collected at an incidence of 2°, which is enough to avoid measuring the underlying CdS and SnO_x:F

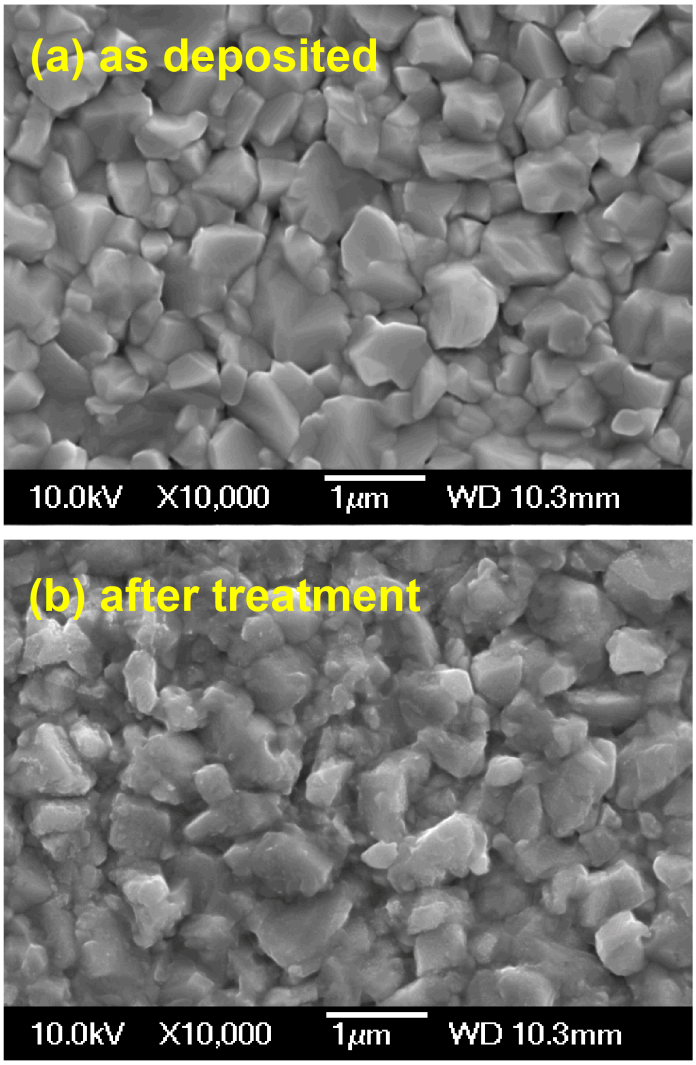

Figure 5.3: SEM images of CMT films before and after $CdCl_2$ treatment.

Table 5.1: EDS measured atomic concentrations (%) and calculated X value of $Cd_{1-x}Mg_xTe$ films.

	Before Treatment	After Treatment
Mg	14.22 ±0.15	11.84 ±0.15
Cd	34.11 ±0.31	37.46 ±0.32
Te	51.67 ±0.42	48.24 ±0.42
Cl	0 ±0.00	2.47 ±0.15
X=Mg/(Cd+Mg)	0.2942 ±0.003	0.2463 ±0.003

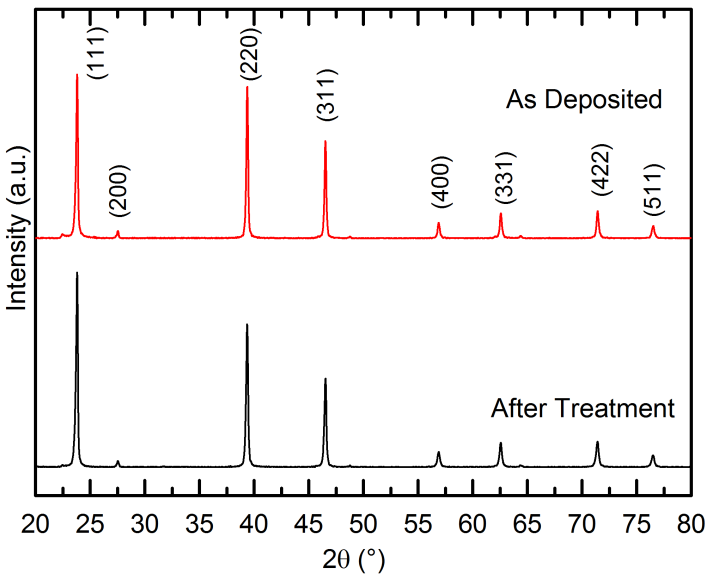

Figure 5.4: GAXRD spectra collected at 2° incidence of as deposited and after treatment CdS/CMT films. Peaks are labeled with their zinc blende Miller indices.

films underneath the 1.7 μm thick CMT. In both cases, the CMT film shows a zinc blende structure (Miller indices are labeled in Fig. 5.4). Only a small change in peak intensity of the (220) peaks is seen between the two spectra, indicating a minor change in the film orientation. Furthermore, the peaks do not shift to indicate a change in the lattice parameter due to the treatment. This data suggest that recrystallization has not occurred due to the treatment.

To investigate the possible nature of the CMT conversion to CdTe, XPS depth profiling was used to characterize the back surface of "as deposited" and "after treatment" CMT films. Fig. 5.5 shows the primary XPS spectra of Mg, O, Cd, and Te as a function of sputter time. For as-deposited CMT, the Te3d5 spectra show two peaks at the back surface. The peak centered at 572.5 eV is associated with CdTe. The peak centered at 576 eV is associated with Te based oxides, such as TeO_2 or $CdTeO_3$ [98]. After treatment, the CMT film does not show a significant signal from the Te atom, indicating the surface is dominated by other elements. Furthermore, the Te oxide peak is small, yet the film shows a significant amount of

oxygen is present deep into the films, indicating another oxide species has formed on the film surface. As the films are sputtered, Cd, Te, and Mg peaks become steady in size and location, while the oxygen peaks change dramatically. In both films, the O1s peaks demonstrate a double-peak shape associated with the presence of multiple oxygenated species. Resolving these double peaks for specie and bonding identification has proved difficult due to the wide spectrum and possible overlap of peak locations reported in literature [98]. Despite these limitations, additional information about bonding can be found from the Auger response during XPS measurements. Fig. 5.6 shows Mg KLL Auger spectra collected during sputter depth profiling. Mg KLL spectra of both films show a double peak shape associated with two different Mg species. The lower kinetic energy peak, centered on 1181 eV, is typically associated with MgO-like species [98]. At the rear surface, this peak is evident in both films, but is significantly more dominant for the after treatment sample. These "MgO" peaks decrease and are eventually eliminated during the sputtering process. The elimination of the "MgO" peak coincides with elimination of the O1s peak, indicating the signals are likely from the same material specie. The higher kinetic energy Mg KLL peak, centered on 1183 eV, is associated with Mg metal or possibly a "MgTe"-like species [98]. At the film surface (0 min), this "MgTe" peak is clearly evident in the as-deposited CMT sample but is not found in the after-treatment sample. The low "MgTe" signal at the rear surface after treatment coincides with the low Te3d5 signal (Fig. 5.5bottom), further suggesting the lack of MgTe bonding at the surface. As the films are sputtered, "MgO" peaks are eliminated and "MgTe" peaks become prevalent and steady through the bulk of the film.

Collectively, XPS and Auger data suggest the presence of oxides on the back surface for both before and after treatment CMT films. Oxide thickness, however, differs between the two samples. The O1s and "MgO"-like Mg KLL peaks were eliminated after 4 minutes of sputtering in as-deposited CMT, while after treatment CMT required more than 10 minutes of sputtering to eliminate these peaks, indicating a thicker oxide layer has formed during treatment. Formation of thicker oxides, may be correlated to CMT conversion to CdTe seen with optical studies.

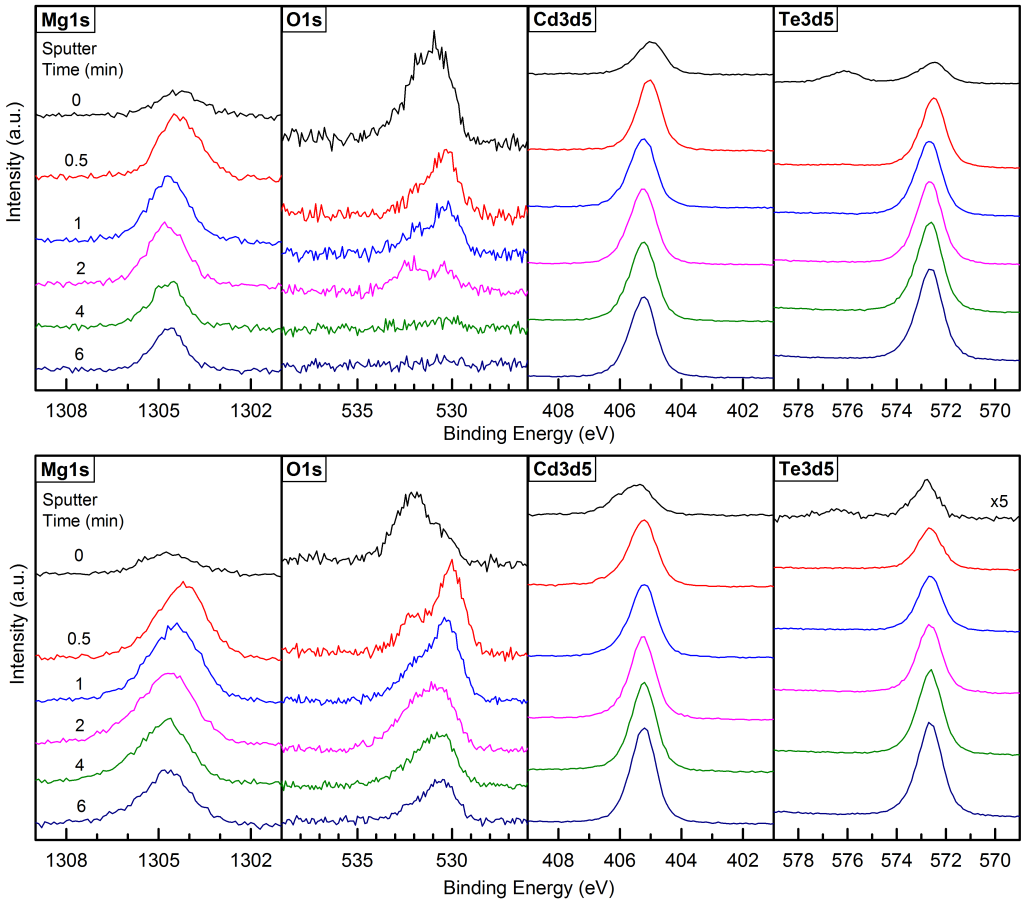

Figure 5.5: XPS spectra of as deposited (top) and after treatment (bottom) CdS/CdMgTe films sputtered for various times.

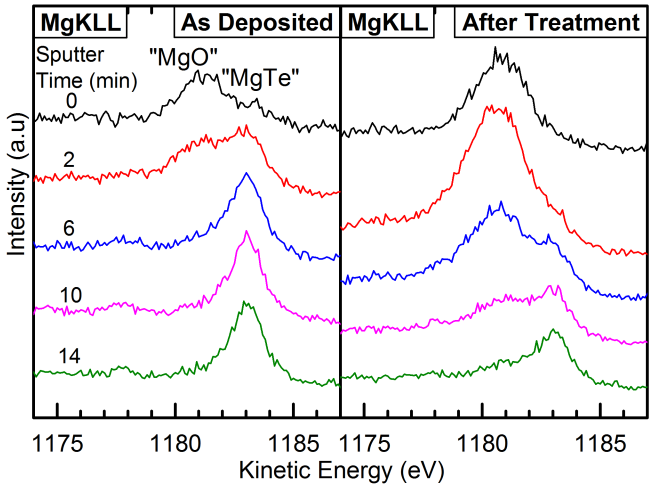

Figure 5.6: Mg KLL spectra of CMT films before and after $CdCl_2$ treatment.

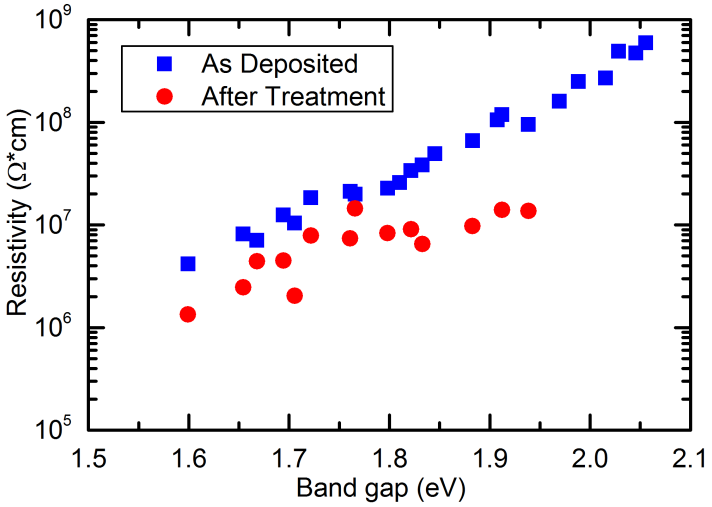

Figure 5.7: Resistivity of CMT films deposited on soda-lime glass before and after $CdCl_2$ treatment.

Resistivity of SLG/1.7 μm CMT films was measured at room temperature using a two point probe method. Fig. 5.7 shows the resistivity of before and after treatment as a function of CMT band gap. Resistivity of after treatment films was plotted against their as-deposited band gaps. Some after-treatment resistivity measurements were omitted due to film adhesion problems. From Fig. 5.7, resistivity of as-deposited CMT increases with the band gap. If the mobility is assumed to be constant for all films, the addition of Mg to CdTe appears to reduce the carrier concentration in the film. Since CdTe films are highly compensated (i.e. large numbers of N_A and N_D defects are present), it is likely the presence of excess anions during deposition increases the density of donors, such as Cd_i or Cd_{Te} [10], thus reducing total carrier density ($N_A - N_D$) and making the p-type films more resistive. $CdCl_2$ treatment of the CMT films reduces the measured resistivity and likely improves the carrier density. Passivation treatment of CdTe is known to increase acceptor density N_A by creating A-centers from the V_{Cd} and Cl_{Te} states [10]. Reduction of Mg in CMT can lead to V_{Cd} formation and therefore higher N_A and carrier density and lower resistivity.

5.4.2 Effect of $CdCl_2$ Treatment on CdS/CdTe/CMT Structures

The standard $CdCl_2$ solid-film treatment was also applied to TEC10/120 nm CdS/$\sim$1.75μm CdTe/$\sim$150 nm $Cd_{1-x}Mg_xTe$ film structures. Material properties of the treated films are presented here. Electronic characterization of devices with this structure are presented in Section 6.3.1 of this manuscript.

To analyze material changes induced during $CdCl_2$ treatment, the films were characterized with cross-sectional TEM and EDS. Figure 5.8 shows the electronic images and EDS elemental response maps of before and after treatment samples. Before treatment (Fig. 5.8top) the CMT film shows uniform coverage and a distinct Mg signal. Sulfur from the CdS layers also shows a distinct layer. Furthermore, no oxygen or sulfur signals are seen from the bulk CdTe and CMT films. In the after treatment sample (Fig. 5.8bottom), CdTe and CMT films shows significant changes due to the chlorine treatment. First, the electron of the film stack shows significant voids in the CdTe film. These voids correspond to high signals of chlorine in the film structure and are associated with accumulation of $CdCl_2$ at the CdS/CdTe interface and along the grain boundaries of the polycrystalline film. Identification of Cl at the grain boundaries in the bulk of the film is not uncommon and has been demonstrated by several groups [99, 100]. However, $CdCl_2$ accumulation at the CdS/CdTe interface is attributed to an overly aggressive passivation treatment. From the sulfur elemental map, it appears sulfur has diffused into the CdTe along the grain boundaries and to the $CdCl_2$ accumulation sites. Treatment of CdS/CdTe structures often results in intermixing at the CdS/CdTe interface [10] and is the likely cause of S signal in the CdTe sample. Additionally, a distinct oxygen signal is present at the back surface. It is likely the oxygen is from a MgO film formed at the rear surface, as was discussed in Section 5.4.1. The Mg signals from the CMT layer become less uniform across the measured sample area. Several spots of a decreased Mg signal are seen and appear to coincide with grain boundaries of the CMT and CdTe films. In bulk CdTe, faint Mg signals are also seen from the $CdCl_2$ accumulation sites at the CdS/CdTe interface, indicating Mg may have migrated to this area during treatment.

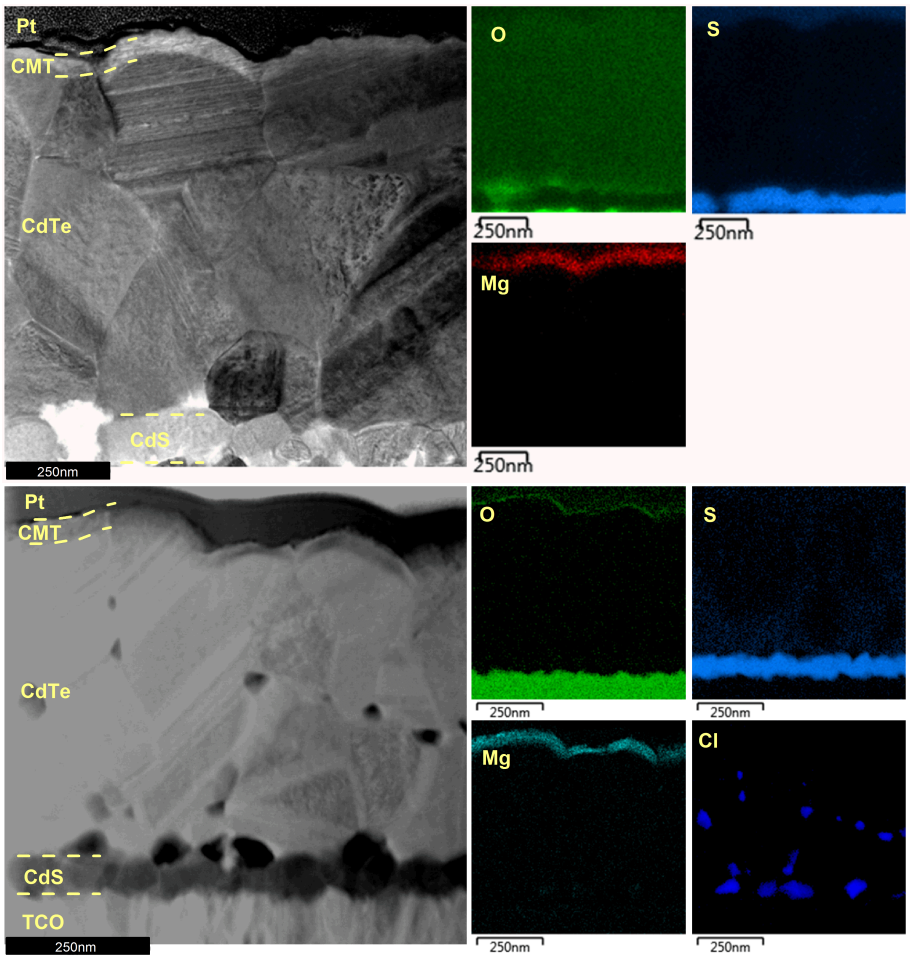

Figure 5.8: Electron images and elemental maps for CdS/CdTe/CMT structure before (top) and after (bottom) standard $CdCl_2$ treatment. Imaging courtesy of A. Abbas.

High Angle Annular Dark Field (HAADF) TEM imaging was performed on the CdTe and CMT grain boundaries to investigate the Mg loss. In HAADF, materials with heavier atomic weights look brighter due to added electron scattering; conversely, lighter compositions appear darker. Figure 5.9 the CdTe/CMT interface and grain boundary before and after the $CdCl_2$ treatment. Before treatment (Fig. 5.9a), the CMT film shows a distinct elemental interface with a CdTe and a continued grain boundary. This is in agreements with results shown in Chapter 4, where it was shown that CMT films grow epitaxially on CdTe and retain the microstructure of the underlying CdTe grains. By HAADF, the CMT film

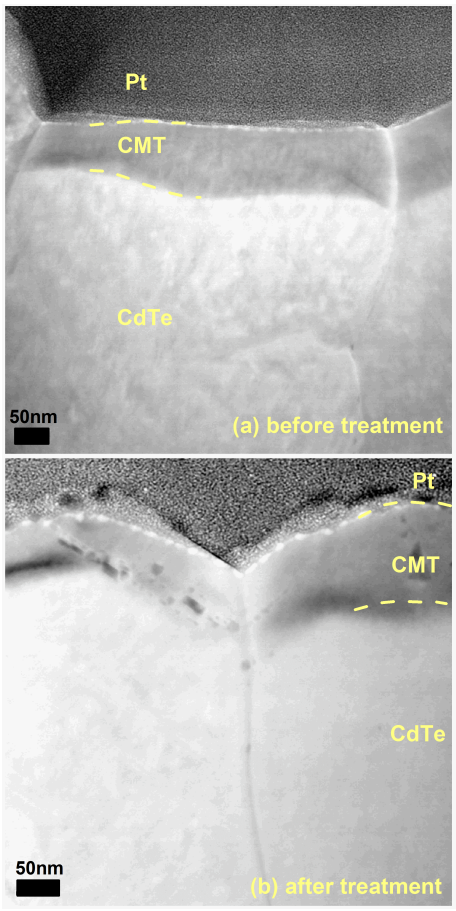

Figure 5.9: HAADF TEM images of CdTe/CMT junction and grain boundary before (a) and after (b) treatment. Imaging courtesy of A. Abbas.

appears to be uniform in composition before treatment. After $CdCl_2$ treatment, HAADF (Fig. 5.9b) shows a brighter signal from the CMT film near the grain boundary. This indicates the composition has changed towards heavier elements at the CMT grain boundary. It is likely, Mg atoms have diffused out of the CMT film during the passivation treatment, thus producing a heavier CdTe phase at this grain boundary.

5.4.3 $MgCl_2/CdCl_2$ Vapor Treatment of CMT Films

TEC10/CdS/$Cd_{1-x}Mg_xTe$ structures were treated with vapor $MgCl_2/CdCl_2$ in either pure Argon or 2% O_2 in Argon using the bell jar passivation tool. Figure 5.10 shows the direct transmission of these films before and after treatment. As oxygen is added to the treatment

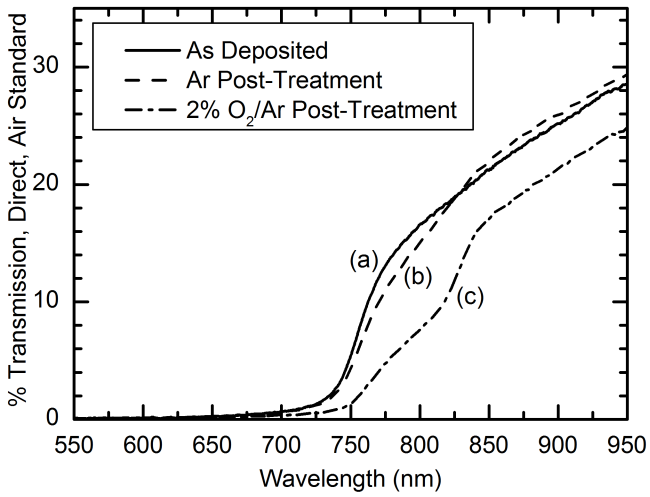

Figure 5.10: Direct transmission (air standard) of $CdS/Cd_{1-x}Mg_xTe$ structures: (a) as deposited and treated in (b) argon and (c) 2% O_2 in argon.

gas, the band gap of the as-deposited CMT film is reduced towards one of CdTe (around 830 nm). Without oxygen in the residual gas, the band gap of the CMT films is maintained, with only a small reduction in transmission. Figure 5.11 shows SEM images of the films, indicating a significant change in microstructure due to the presence of oxygen. The as-deposited film (Fig. 5.11a) has grain structure similar to typical CSS deposited CdTe, demonstrating sharp grain boundaries and smooth grain faces. After passivation in argon (Fig. 5.11b), the film shows small nodule formation on the surface of the grains, but not significant changes in the grain size or roughness. Treatment with oxygen (Fig. 5.11c) shows almost complete microstructure and morphology change. In this case, the grain faces are no longer smooth and grain boundaries are poorly defined. It is likely the film has recrystallized with treatment in oxygen. This microstructure also results in poor adhesion between the CMT and the underlying CdS, which has been problematic for making CdS/CMT devices. Adhesion issues, however, are not resolved with eliminating oxygen and therefore are not a product of recrystallization alone. Higher band gap CMT films tend to delaminate more frequently and at lower temperature than lower band gap CMT films. It is likely the chlorine treatment causes significant material changes at the interface that cause the delamination. The cause of delamination will be studied in more detail in future work.

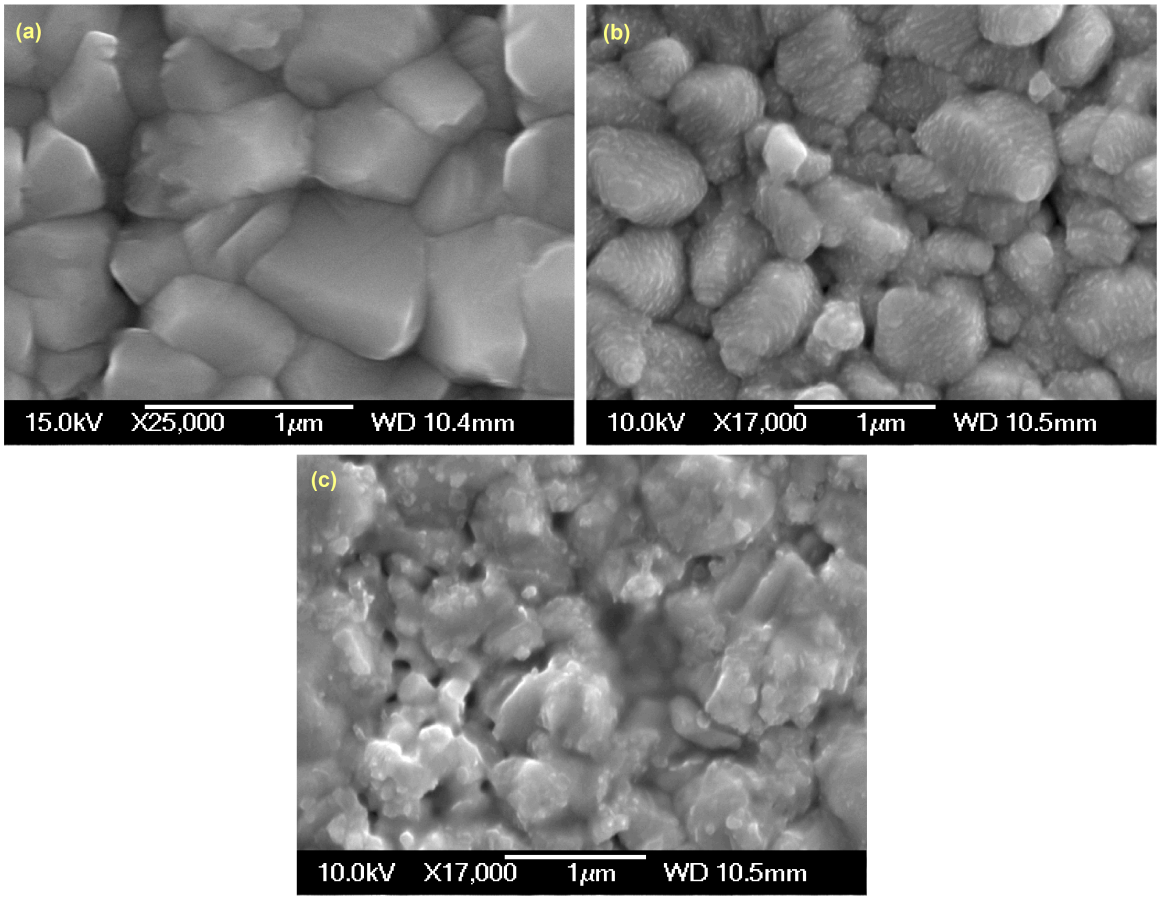

Figure 5.11: SEM images of $Cd_{1-x}Mg_xTe$ films (a) as deposited, and treated in (b) argon and (c) 2% O2 in argon.

Despite the adhesion problems, several CdS/CMT devices were made to evaluate the chlorine treatment and back contact processes. Figure 5.12 shows the Current Density - Voltage (J-V) curve of one of the best performing CdS/CMT devices. This device was a TEC10/150 nm CdS/1 μm CMT (E_g = 1.58 eV) structure. After CMT deposition, the stack was treated using $MgCl_2/CdCl_2$ vapor for 8 minutes at 410°C in 400 Torr of argon. The cell was finished with our standard Cu back contact and Carbon/Nickel back electrode processes [82, 83]. The J-V curve shows a device with acceptable series resistance, but poor open-circuit voltage and shunt resistance. Further optimization of the passivation treatment and improvements to the adhesion issues seen with CdS/CMT structures should improve performance of such devices. A carrier density, i.e. N_A-N_D, versus depletion width profile

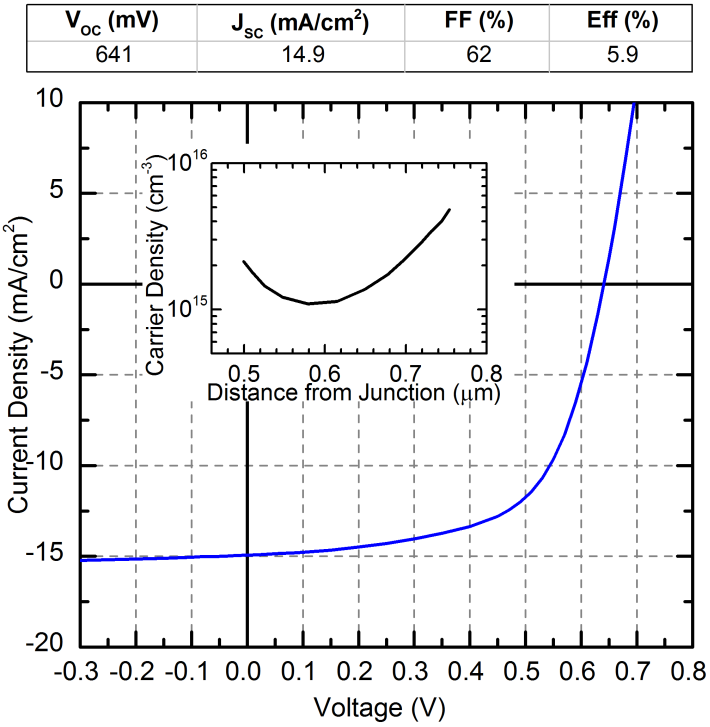

Figure 5.12: J-V curve of a CdS/$Cd_{1-x}Mg_xTe$ device at AM1.5 illumination. Inset is doping density derived from C-V measurements. Characterization courtesy of J. Drayton.

of the device is shown in Figure 5.12inset. This measurement is derived from Capacitance-Voltage (C-V) measurements. The doping profile indicates a bulk doping of the CMT film to be near 10^{15} cm^{-3}. Although this value is likely larger than the true doping, in part due to the thinness of the CMT absorber [101], the C-V measurement indicates that a *p*-type doping of similar magnitude to CdTe is achievable in CMT films with $MgCl_2/CdCl_2$ passivation and Cu treatment.

5.5 Discussion

The results show clear trends and material changes in the CMT films due to passivation treatment. Typical $CdCl_2$ treatment of the CMT films shows a distinct reduction of CMT band gap towards CdTe. This reduction occurs on both thick CMT films deposited on CdS

and on thin CMT films deposited on CdTe. In both cases, a MgO layer is formed on the back surface. Furthermore, cross-sectional TEM/EDS and HAADF images show that Mg is pulled out of CMT films near the grain boundaries, where $CdCl_2$ travels towards the junction. The data suggests the optical band gap reduction is likely due to Mg loss from the CMT films.

The chemical nature of this Mg conversion was investigated analytically. Table 5.2 shows several possible chemical reactions that could lead to reduction of MgTe bonding in the CMT films and their calculated Gibbs free energies. A negative Gibbs free energy means the reaction is favorable towards to the right side. In the first reaction, reaction (a), the presence of $CdCl_2$ around MgTe leads to production of CdTe and $MgCl_2$ species. This favorable reaction is likely the primary reason for CMT band gap loss. Once $MgCl_2$ is formed, it can travel down the grain boundary or is washed off during rinsing typically done after treatment.

The formation of MgO can be described by reactions (b), (c), and (d). In reaction (b), the role of O_2 gas is investigated. In the presence of MgTe and $CdCl_2$, diatomic oxygen can break apart and react with Mg atoms from the CMT film. The formation of MgO, CdTe, and Cl_2 species is highly favorable and is the primary degradation mechanism when oxygen is added to the residual gas during treatment. In addition to O_2, the presence of H_2O vapor in the chamber can cause MgO formation. Reactions (c) and (d) in Table 5.2 investigate the role of water vapor in forming MgO. Reaction (c), which is unfavorable, shows the formation of MgO, CdTe, Cl_2, and H_2. Reaction (d) changes the by-products to HCl and now the reaction become favorable since HCl gas is more stable than Cl_2 and H_2 species. Reaction (e) explores the effect of HCl on the MgTe bonds. HCl gas has been used for treatment of CdTe thin-films as a replacement for $CdCl_2$ [102, 103]. In the presence of MgTe, HCl gas breaks down and forms $MgCl_2$ and H_2Te. This favorable reaction may further point to reduction of Mg in the CMT film.

The impact of O_2 and H_2O on CMT films has been shown both experimentally and through analytical examination of the chemical reactions. It is evident, reduction of both O_2 and H_2O is needed during processing to reduce the possibility of forming MgO layers and

Table 5.2: Possible chemical reactions and their respective Gibbs free energies at 400°C. Negative value of ΔG implies the reaction is favorable. Energies are calculated from referenced values found in Ref. [104]

Label	Reaction	ΔG (kJ/mol)
(a)	$MgTe + CdCl_2 \longrightarrow CdTe + MgCl_2$	-139.0
(b)	$MgTe + \frac{1}{2}O_2 + CdCl_2 \longrightarrow MgO + CdTe + Cl_2$	-274.7
(c)	$MgTe + H_2O + CdCl_2 \longrightarrow MgO + CdTe + H_2 + Cl_2$	74.5
(d)	$MgTe + H_2O + CdCl_2 \longrightarrow MgO + CdTe + 2\,HCl$	-123.7
(e)	$MgTe + 2\,HCl \longrightarrow MgCl_2 + H_2Te$	-124.8

reducing Mg content of the CMT film.

The addition of $MgCl_2$ to $CdCl_2$ as a treatment source has been shown experimentally to reduce band gap reduction (see Fig. 5.10). The role of $MgCl_2$ vapor during treatment is believed to reduce the reaction kinetics of reactions (a) and (d) in Table 5.2 and therefore reduce the rate of Mg loss. Preliminary evidence suggests this can be successful in both passivating the CMT and CdTe films [97] and reducing the Mg loss from CMT films. Future work should focus optimization of the $MgCl_2/CdCl_2$ ratio during treatment to get the most passivation without losing Mg from the CMT film.

5.6 Conclusions

Several CdS/CMT and CdS/CdTe/CMT structures were treated with $CdCl_2/MgCl_2$ and $CdCl_2$ passivation treatment. Standard $CdCl_2$ treatment was shown to reduce the band gap of CMT by pulling Mg atoms out of the CMT film and replacing it with Cd. The excess Mg then forms either MgO, if O_2 or H_2O are present in the chamber, or $MgCl_2$. On CdS/CdTe/CMT structures, it is likely the formed $MgCl_2$ species diffused down the grain boundary with $CdCl_2$. Preliminary results show a a smaller band gap degradation after

passivation with a mixture of $MgCl_2/CdCl_2$ source materials. It is likely the excess $MgCl_2$ vapor reduces the reaction of MgTe with $CdCl_2$ and formation of CdTe and $MgCl_2$ during treatment. Additional work to optimize the $CdCl_2/MgCl_2$ passivation treatment is suggested for future development.

Chapter 6

Development of CdS/CdTe/CMT Electron Reflector Solar Cells[1]

[1]This chapter presents experimental results of various CdS/CdTe/$Cd_{1-x}Mg_xTe$ electron reflector structures and discusses their operation. Additionally, ER device performance was investigated with extensive device simulation to explain features found in experimental data.

Parts of this chapter have been submitted for a conference presentation as:
D.E. Swanson, R. Gesithardt, P.S. Kobyakov, J. Raguse, J. Drayton, K. Barth, J.R. Sites, and W.S. Sampath, "Reduction of Carrier Recombination by Addition of a $Cd_{1-x}Mg_xTe$ Electron Reflector Film," submitted to *40th IEEE Photovoltaic Specialists Conference*, February, 2014.

Below is a description of contributors and their involvement to the work presented in this chapter:

P.S. Kobyakov: For this study, Mr. Kobyakov helped make samples, analyzed data, and interpreted the results. Additionally, he performed the presented device modelings, prepared figures, and wrote and edited the manuscript.

D.E. Swanson: Mr. Swanson helped with sample preparation and result interpretation. Samples presented in Section 6.3.2 were prepared and characterized by Mr. Swanson.

J.M. Raguse: Mr. Raguse was involved with sample preparation and helped interpret the results. He is responsible for collecting the TRPL data.

K.N. Zaunbrecher: Mrs. Zaunbrecher helped with TRPL data collection.

H. Moutinho: Dr. Moutinho of the National Renewable Energy Laboratory performed all aspects of the EBIC measurements, including sample preparation, data collection, and analysis.

6.1 Introduction

During development of CdS/CdTe/CMT electron reflector devices, more than 100 different structures were made with varying process parameters. Some portions of the samples were converted to small-area devices (SADs) for performance while other portions were used for material characterization. Due to the large number of SADs generated during development, only the most relevant results are shown in this manuscript. For example, during development, a large effort was spent on optimizing the Cu process for CdS/CdTe/CMT structures for low temperature CMT deposition. If the reader is interested to learn about this portion of ER structure development, they are invited to explore Ref. [83], where the methods and results of Cu optimization are presented in detail. Additionally, other development research thrusts proved to be unsuccessful in generating useful data. For example, a collaborative effort to directly measure the valence-band and conduction-band offsets was found to be unsuccessful by two different approaches. First, measurement of the VBO and CBO were attempted with Ultra-violet Photoelectron Spectroscopy (UPS) and Inverse Photoelectron Spectroscopy (IPES), respectively. Although measurements were made, the data proved to be poor due to oxide contamination of the CMT surfaces and concrete conclusions about the band structure at the CdTe/CMT interface could not be reached. Similarly, Scanning Kelvin Probe Microscopy (SKPM) was attempted on cross-sectional SADs, but was unsuccessful due to difficult sample preparation and lack of resources.

Despite the aforementioned measurement setbacks, other device and electro-optical characterizations of ER structures showed useful results. These include J-V measurements of

J. Drayton: Dr. Drayton helped with sample preparation and interpretation of results.

J.R. Sites: Prof. Sites provided guidance on sample development, device modeling, and contributed to interpretation of the result.

W.S. Sampath: Prof. Sampath provided guidance on the sample development and device modeling. He also helped to interpret the results.

SADs as well as Time-Resolved Photoluminescence (TRPL) and Electron-Beam Induced Current (EBIC) measurements of the CdS/CdTe/CMT structures. In addition to direct measurements, device modeling can be used to explain the functionality of experimental devices, such as exploration of performance limiting conditions in the ER device. Specifically, device modeling, in conjunction with device and electro-optical characterization, can be used to investigate device behavior associated with an increasing CBO, increasing VBO, varying CMT band gap, and increasing recombination at the CdTe/CMT interface. This chapter provides important experimental results and uses device modeling to improve the functional understanding of experimental ER devices.

6.2 Experimental Details

The CdS/CdTe/CMT experimental devices were prepared using methods previously described in this manuscript. First, CdS/CdTe structures and treated were grown on TEC10 (soda-lime glass/SnO_x:F) substrates using the Advanced Research and Development System (see Appendix A.4.2 for more details) with the previously described process conditions [82]. Approximately 130 to 150 nm thick CMT films were deposited onto the CdS/CdTe structures at approximately 470°C using the co-sublimation process described in detail in Chapters 3 and 4. After CMT deposition, the structures were returned to the ARDS for another standard $CdCl_2$ treatment (details in Chapter 5) and Cu back contact processing. Finally, SADs were fabricated by painting C/Ni back electrodes and selectively delineating the cell area. Additional, sample specific process conditions are provided in the Results section of this chapter.

Current Density-Voltage (J-V) characteristics of SADs were measured with a simulated 1.5AM light spectrum made by ABET Technologies 10500 Solar Simulator and a Keithley 2420 3A Sourcemeter. Time-resolved Photoluminescence (TRPL) was performed on a CdS/CdTe/CMT structures without a back contact on both the glass side and back film side. Figure 6.1 shows a schematic of this setup. In this study, a pulsed laser at 760 nm

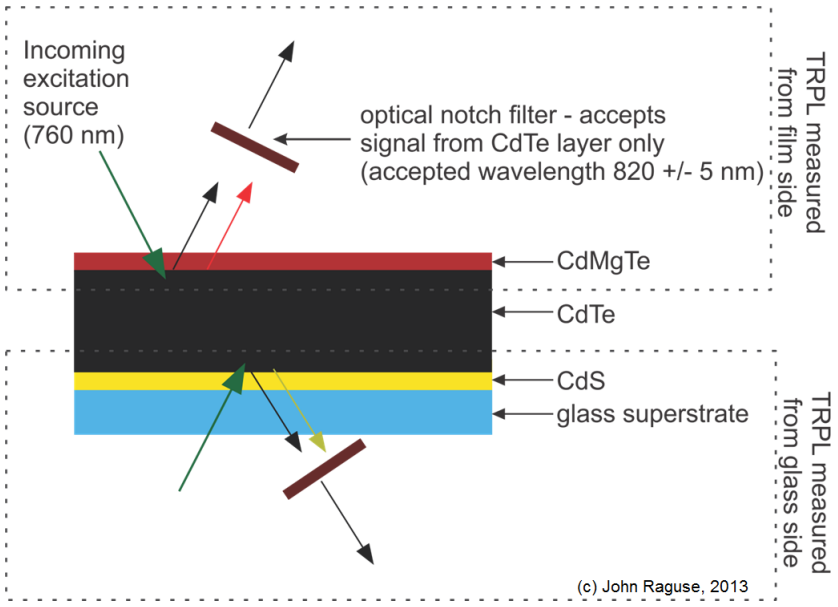

Figure 6.1: TRPL setup for film side and glass side measurements of CdS/CdTe and CdS/CdTe/CMT structures. Illustration courtesy of John Raguse.

was used as the excitation source at a pulse rate of about 1 MHz and a pulse width of 3 ps. The laser spot size was about 1 mm in diameter and ran at about 2 mW power. PL was measured in counts with respect to time by passing the PL signal through a long pass filter to a photomultiplier tube accepting 820±5 nm. This data provides the time-resolved photoluminescence decay after excitation of charge carriers and is an estimate of carrier lifetime in the device.

EBIC signals were on an FEI Nova 630 FEG SEM using a Hikari EBSD system from EDAX. The signals were measured with Matalect EBIC system with an induced signal monitor model ISM-6Aa. The measurements were performed on ion-milled cross sections of CdS/CdTe and CdS/CdTe/CMT devices at a 3 kV electron beam acceleration voltage.

Modeling was performed using the publicly available AFORS-HET version 2.2 software [105]. A background on this modeling software and model specific details are provided in Appendix B. In this work, the modeling was used to vary the CBO, VBO, CMT band gap, and recombination velocity at the CdTe/CMT interface to identify general J-V trends associated with these parameters.

6.3 Experimental Results

6.3.1 Standard Thickness J-V Results

The effect of the CMT electron reflector film on performance of standard thickness CdS/CdTe devices was investigated in detail. Approximately 130 to 150nm thick CMT films with band gaps ranging from 1.6 to 1.95 eV were deposited on $CdCl_2$-treated 120nm CdS/$\sim$ 1.7μm CdTe structures at 470°C and subsequently re-treated with $CdCl_2$ at standard conditions. Some, but not all, devices underwent further Cu back-contact treatment before the typical C/Ni back electrodes were applied. J-V performance of these devices is shown Fig. 6.2, which shows the light (top) and dark (bottom) J-V curves of these devices with (left) and without (right) the Cu treatment. Several important device characteristics are found in this data. First, the addition of higher Mg content CMT films shows a distinct movement of the dark curve towards higher and higher turn-on voltage. This indicates a larger barrier to forward electron flow is present in the devices. A clear barrier behavior, indicated by the kink of the J-V curve in the top right plot of Fig. 6.2, is seen with devices without Cu. As the band gap of the CMT film increases, the barrier increases indicating the two parameters are linked. The addition of Cu appears to reduce the barrier when the band gap is low and improves the FF of the devices. At higher CMT band gaps, however, Cu does not improve the barrier behavior.

Temperature dependant J-V response of some cells were studied to investigate the CMT-induced barrier. Fig. 6.3 shows the J-V-T of a baseline CdS/$\sim$1.7μm CdTe/Cu device and two $CdCl_2$-treated CdS/$\sim$1.7μm CdTe/$\sim$140nm CMT ($E_g \approx 1.7$ eV) ER devices with and without the Cu treatment. As is typical for baseline cells (Fig. 6.3a), decreasing cell temperatures increases the V_{OC} and apparent series resistance, R_s. Higher R_s could indicate a temperature dependent back contact barrier. As temperature decreases, additional electrical potential is needed to allow charge carriers to cross over the back surface barrier. In ER devices without Cu (Fig. 6.3b), the barrier associated with the CMT layer is evident, but

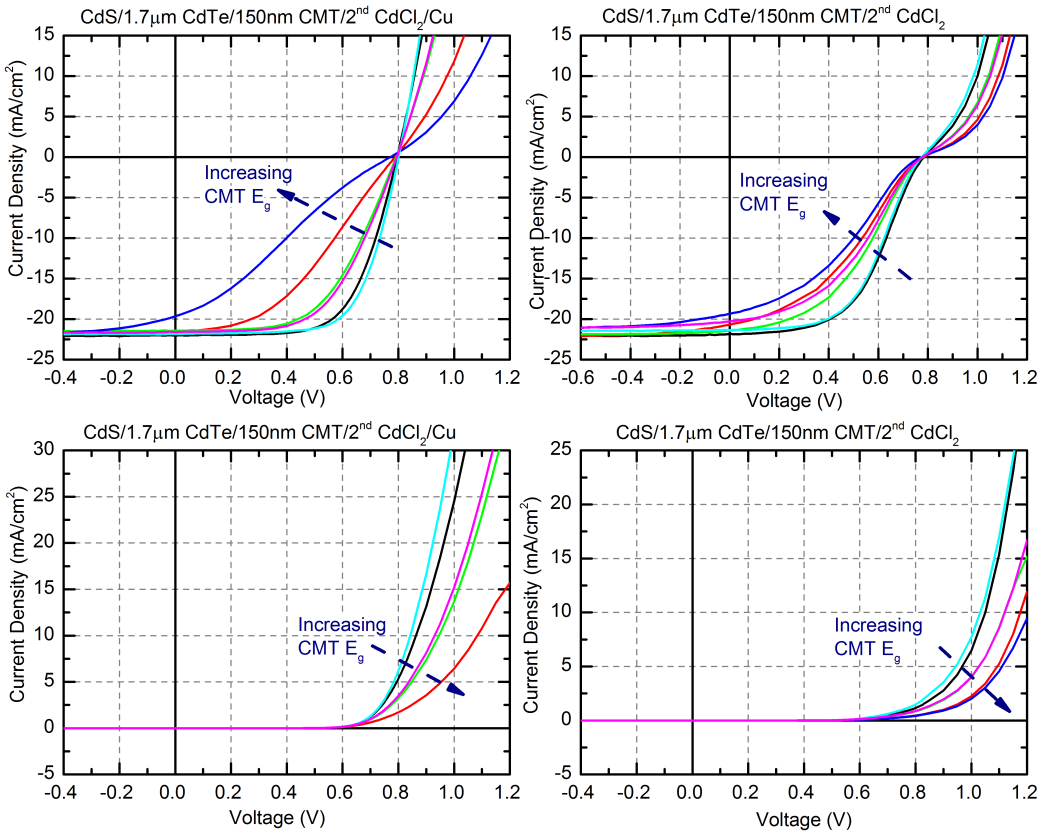

Figure 6.2: Light and dark J-V curves of experimental CdS/CdTe/CMT ER devices with and without Cu treatment.

does not appear to change with temperature indicating it is not temperature dependent. With the addition of Cu to the ER devices (Fig. 6.3c), the barrier is reduced and eliminated at high temperature. At low cell temperatures, the barrier re-appears and shows a larger cross-over between light and dark curves. Fig. 6.3d shows the $V_{OC} - T$ relationship of the three cells and the line fit parameters of each data set. ER devices have higher V_{OC} than the baseline at room temperature, but a lower extrapolated voltage at 0K. This might indicate that an additional recombination mechanism exists in ER devices that leads to poor built-in potential.

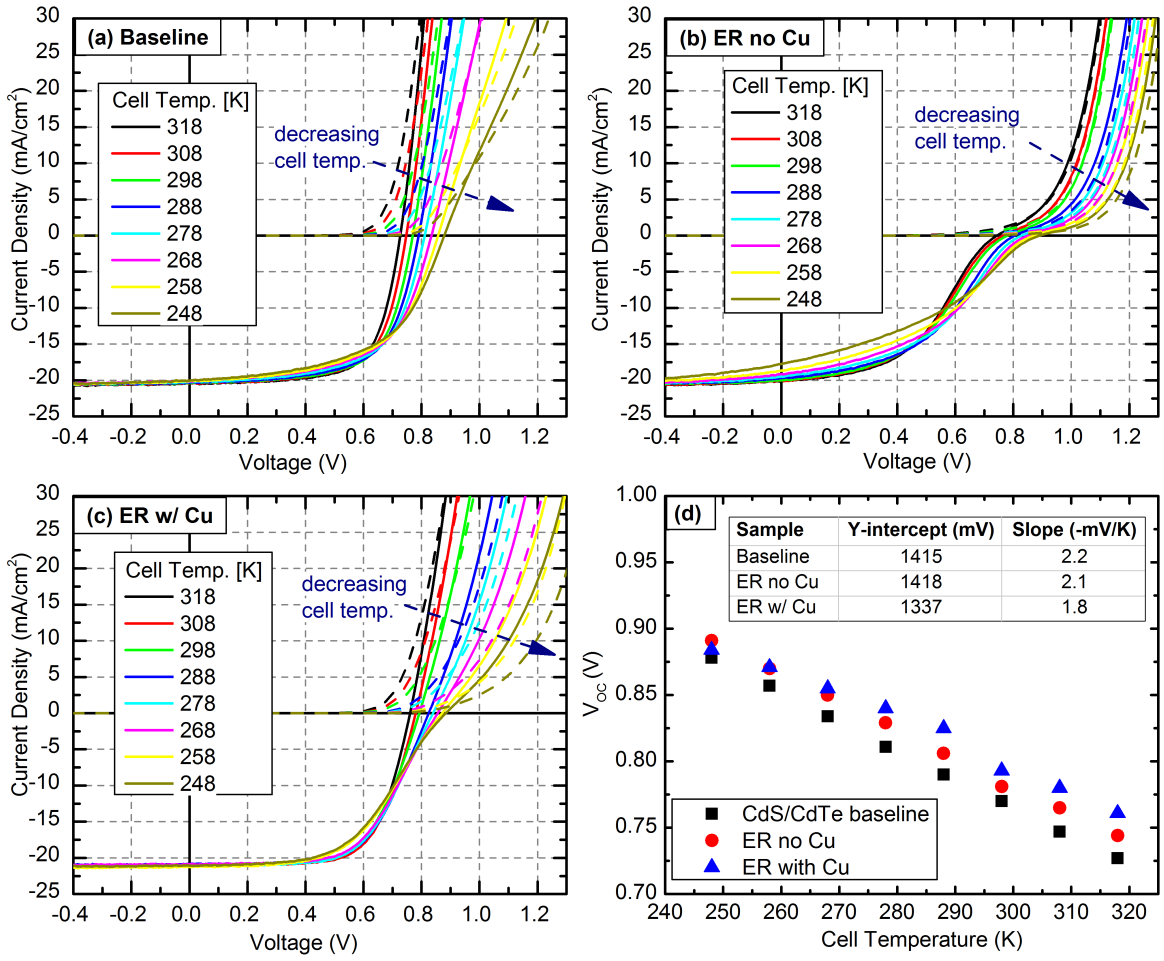

Figure 6.3: Light (solid) and dark (dashed) J-V-T curves of (a) CdS/CdTe/$CdCl_2$/Cu baseline and two $CdCl_2$-treated CdS/CdTe/CMT ER devices before (b) and after (c) Cu treatment. The $V_{OC} - T$ relationship (d) and linear fit parameters (d-inset) are shown for all three devices. CMT films ($E_g \approx 1.7$ eV, ~140 nm) were deposited on treated CdS/1.7μm CdTe cells at 470°C.

6.3.2 Thinning CdTe J-V Results

At standard thickness, the addition of a CMT electron reflector film does not significantly improve V_{OC} of CdS/CdTe devices. The standard CdTe thickness of 1.7μm, however, may be too thick to get the optimal effect of the ER structure. Thinning of CdTe was investigated

in order to see the effect of CdTe thickness on device performance. Figure 6.4 shows the J-V parameters of CdS/CdTe and CdS/CdTe/CMT ER devices at various CdTe thickness. One very interesting result from this study is the effect of the CMT layer on the V_{OC} of very thin CdS/CdTe devices. The voltage of standard CdS/CdTe devices reduces when CdTe becomes thinner. This is associated with higher back-surface recombination when the CdTe/back electrode interface approaches the CdS/CdTe junction. The presence of a CMT electron reflector layer, however, makes devices with consistent V_{OC}. The higher V_{OC} is attributed to a reduction in back-surface recombination. This indicates the ER film is working and helping thinner devices improve voltage. As expected, the J_{SC} of both baseline and ER devices is reduced when the CdTe is thinned due to a smaller absorber. Since CdTe is very absorbent, the ER layer does little to improve the total collected current. The fill factor of these devices shows another interesting trend. At thick CdTe, the FF is relatively good for CdS/CdTe but low for the ER device due to the aforementioned barrier behavior. When the CdTe is thinned, CdS/CdTe experience a reduction in FF, again likely due to increased back-surface recombination. ER devices, however, show an improved FF with thinner CdTe absorbers due to elimination of the barrier behavior in the J-V curve.

6.3.3 TRPL and EBIC Results

Figure 6.5 shows TRPL measurements of various baseline and ER devices. In Fig. 6.5a and b, the TRPL signals were taken from the film side of the structure before and after the Cu process. The CMT band gap in the ER devices is noted in the legend. The addition of CMT film shows a markable improvement in the carrier lifetime especially when the band gap is relatively high. Charge carrier lifetimes appear to be better without the Cu treatment, indicating Cu may not be a good dopant for CMT films. Glass side TRPL (Fig. 6.5c) also shows a markable increase in carrier lifetime due to the presence of the CMT electron reflector film. This result is consistent with MBE grown CdTe films, where a CMT cap can significantly improve the carrier lifetime [106] in the CdTe. Additionally, this indicates the CdTe/CMT interface is likely relatively free of recombination defects since lifetime at the

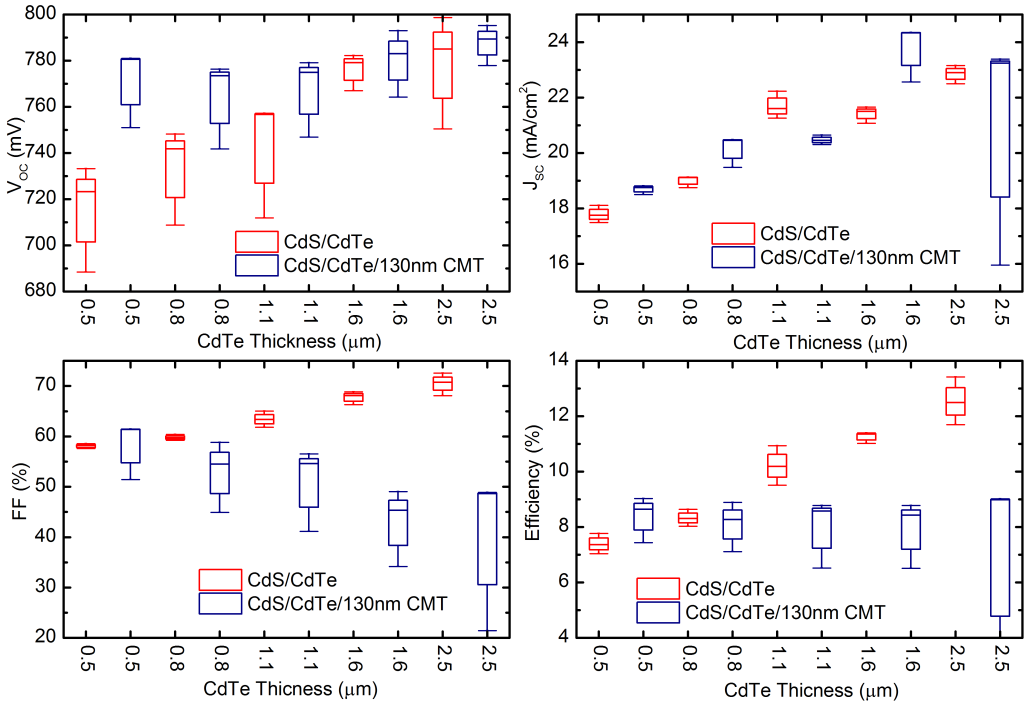

Figure 6.4: J-V Parameters of CdS/CdTe (red) and CdS/CdTe/130nm CMT (blue) devices at various CdTe thickness. CMT was deposited on untreated CdS/CdTe structures at 470°C and includes band gaps between 1.65 and 1.85 eV. All devices were subsequently $CdCl_2$ treated and finished with Cu back contacts per standard procedures. Experimental data courtesy of Drew Swanson.

back of CdTe is significantly better than that of the free CdTe surface.

Ion-milled cross sections of a CdS/CdTe baseline and a CdS/CdTe/CMT electron reflector device were analyzed with EBIC by Helio Moutinho at the National Renewable Energy Laboratory in Golden, CO. Both devices had undergone the standard Cu treatment. EBIC of the baseline cell (Fig. 6.6top) shows distinct signal changes from grain to grain. Through the thickness, the EBIC signal drops off right after the device junction is is passed. The decay is associated with carrier diffusion towards the built-in electric field. This indicates the electric field is relatively thin in the CdS/CdTe structure (about 0.7μm thick). With the addition of the CMT ER film (Fig. 6.6bottom), EBIC collection properties of the device change. First, grain to grain variation in signal is significantly reduced. Through the film

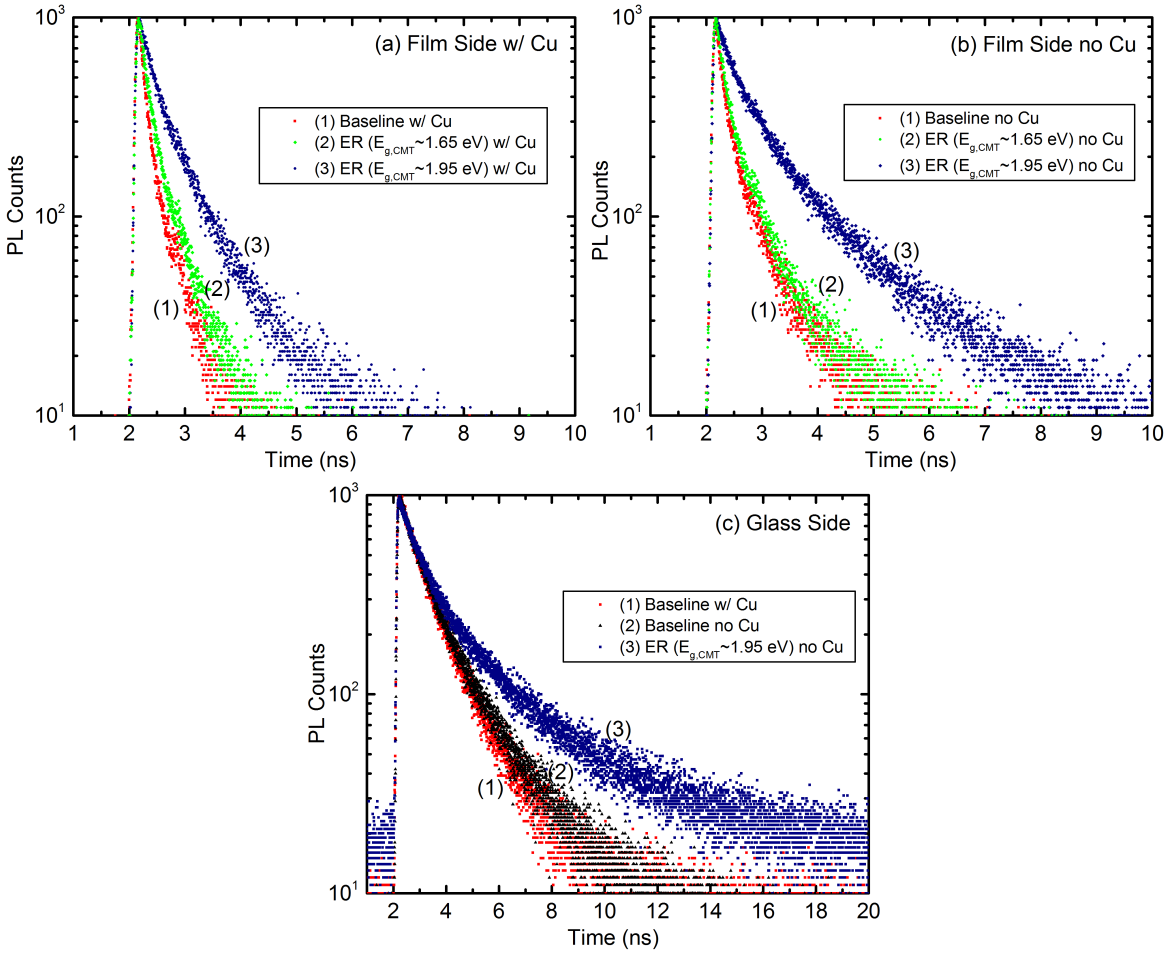

Figure 6.5: TRPL of various CdS/1.7μm CdTe baseline devices and CdS/1.7μm CdTe/140nm CMT ER structures measured from film side (a, b) and glass side (c). All CMT films deposited on treated CdS/CdTe films at 470°C. All devices were subsequently $CdCl_2$-treated. CMT band gaps and Cu back contact treatment are noted. Measurement data courtesy of John Raguse and Katherine Zaunbrecher.

thickness, the EBIC signal stays more uniform, and drops off sharply when it reaches the back surface. This may indicate a wider electric field or longer diffusion length in ER devices. Due to different collection settings, quantitatively comparing the EBIC signals (i.e. the brightness) is not possible with this data set.

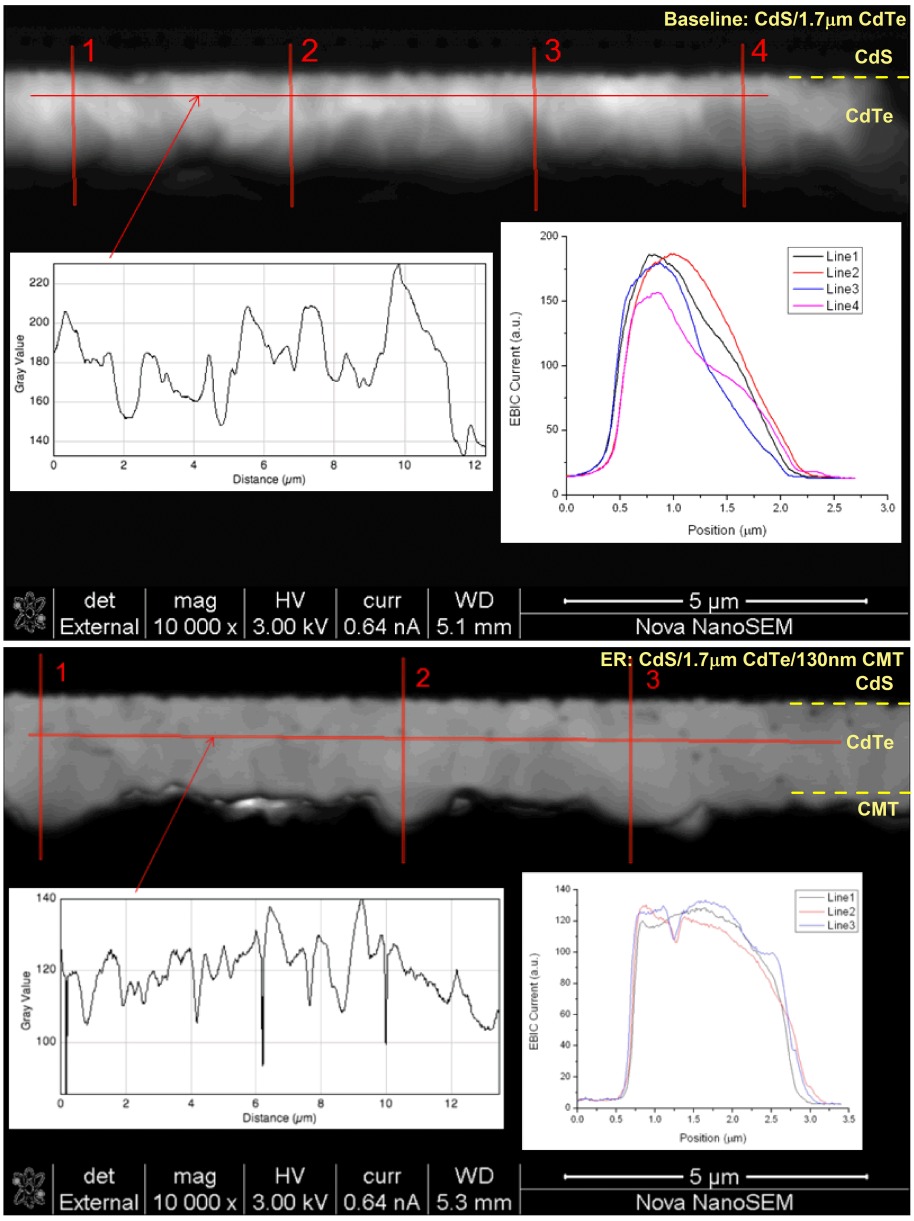

Figure 6.6: EBIC and intensity line profiles of a baseline CdS/1.7μm CdTe device (top) and a CdS/1.7μm CdTe/140nm CMT (1.95 eV) device (bottom). CMT film deposited on treated CdS/CdTe films at 470°C. Both devices had typical $CdCl_2$ and Cu back contact treatment. EBIC intensity between images is collected with different parameters and should not be compared directly. Measurement data courtesy of Helio Moutinho.

6.4 Discussion of Experimental Results

Evaluation the experimental data reveals a few consistent themes that need to be addressed in future development of electron reflector structures utilizing the $Cd_{1-x}Mg_xTe$ alloy. First, TRPL data and EBIC data suggests the device have longer charge-carriers lifetime when the CMT ER film is present. This suggests that the CdTe/CMT interface is relatively free of defects and is an improvement over the free CdTe surface. Due to higher lifetimes, a longer diffusion length may be present in the bulk CdTe film with the ER layer. EBIC data shows a consistently deeper collection of carrier in the device, which may be due to a wider electric field or a product of larger diffusion lengths, both of which should improve the performance of the devices.

Secondly, performance data shows that when the CdTe is thick, the added CMT film creates a barrier problem thus significantly reducing the FF with only minimal improvement to the V_{OC}. Conversely, when the CdTe is thin, the CMT film improves device voltage by likely restricting the back-surface recombination that leads to device voltage and barrier problems affecting the FF are also reduced. With thicker devices, the CMT film should also reduce back-surface recombination, but this effect might minimal due to the low diffusion lengths and carrier lifetimes in CdS/CdTe devices. This suggests that the CMT film provides a conduction-band barrier that reduces charge carrier recombination but an additional barrier is present that causes a reduction of current at voltages near V_{OC}. The source of this barrier needs further investigation.

Despite unsuccessful direct measurements of the band structure in CdS/CdTe/CMT electron reflector structures, very little work has been done to investigate band features and how they may affect the device performance. For instance, a better understanding of CdTe/CMT interface recombination, valence-band offset (VBO), and conduction-band offset (CBO) on device performance is needed. One-dimensional device modeling can be used to investigate these device parameters to see what factors correlate to experimental results and trends found in the J-V curves. These factors are evaluated in the next section of this manuscript.

6.5 Modeling of Electron Reflector Device Features

AFORS-HET device modeling software was used to analyze J-V trends of CdS/CdTe/CMT electron reflector structures which arise from recombination at the CdTe/CMT interface, VBO, CBO, and the CBO/VBO ratio. Additionally, modeling was used to understand the role of changing CdTe thickness on device properties. Specific model parameters are provided in individual sections below and Appendix B of this manuscript.

6.5.1 The CdTe/CMT Interface

Initial models of the CdS/CdTe/CMT interface explored recombination at the CdTe/CMT interface. This was accomplished by adding donor defects at the interface to generate a specific recombination velocity, S_i. Per Equation B.7, S_i was varied from 10^3 to 10^7 cm/s by changing the mid-gap donor defect density, N_t, from 10^5 to 10^9cm^{-3}. Other model parameters are shown in Table B.2.

Figure 6.7 shows the light and dark J-V curves of modeled CdS/2μm CdTe/200nm CMT electron reflector devices with varying recombination velocity at the CdTe/CMT interface. As interface recombination velocity increases, a kink in the power quadrant begins to form and reduces the V_{OC} and FF of the electron reflector devices. This occurs because minority charge carriers (electrons in the conduction band) are no longer reflected by the CBO, but are now recombining at the CdTe/CMT interface. The kink forms in the power quadrant and moves up until it reaches forward current. Once the recombination velocity reaches 10^7 cm/s, which is on the order of thermal velocity of electrons at room temperature, all improvements due to the ER layer are undone. It is important to note, Fig. 6.7 shows this kink formation trend at an optimum position for CBO and VBO and CMT band gap of all the tested models. The demonstrated trend, however, holds for most other combinations of CBO, VBO, and CMT E_g. The kink formation associated with recombination at the CdTe/CMT interface is unlike the trends seen in experimental results, suggesting the interface is not a significant problem in experimental devices.

6.5.2 The Conduction-Band Offset

To see the effect of the conduction band offset was studied by varying it from 0.1 eV to 0.3 eV for the CdS/CdTe/CMT devices. Again, general model parameters are shown in Table B.2. Figure 6.8 shows the effect of increasing CBO on a relatively optimum device with regards to the other parameters, i.e. low VBO (0.05 eV), good doping of CMT film ($p = 10^{13}$ cm^{-3}), and low interface recombination ($S_i = 10^3$ cm/s). As the CBO increases, the V_{OC} increases substantially over the no ER layer baseline. This is consistent with previous models (see Chapter 2). The jump in V_{OC} decreases between 0.2 eV and 0.3 eV CBO, indicating an electron reflector of 0.2 eV is sufficient to achieve large gain in V_{OC}. The addition of a CBO also moves the dark curves to higher turn-on voltages. This dark shift is similar to those seen in dark curves of experimental results (see Fig. 6.2) and suggests a CBO is also present in experimental work.

6.5.3 The Valence-Band Offset

The effect of the valence-band offset (VBO) was investigated at many model conditions and shows a distinct effect at various conditions. Figure 6.9 shows the effect of increasing VBO on an optimum device with high CBO (0.3 eV), good CMT doping ($p = 10^{13}$ cm^{-3}), and low interface recombination ($S_i = 10^3$ cm/s). As the VBO is increased from 0.05 eV to 0.10 eV, the FF changes slightly but there are no significant changes to V_{OC} or the shape of the J-V curves. At 0.15 eV, a large effect on FF starts to develop. At VBO above 0.15 eV, a large barrier-like behavior is formed due to the VBO offset, which not only reduces the FF but also slightly reduces the V_{OC}. This barrier behavior is similar the trend seen experimentally and suggests the VBO maybe a leading cause of poor fill factors in experimental devices. In experiments, however, the absolute values of voltage are not this high, suggesting the CBO is likely smaller than modeled here or other voltage loss mechanisms are present.

It is clear that the VBO offset causes the barrier effect. It is likely the VBO impedes hole transport from the valence-band of CdTe through the CMT to the back metal, thus reduc-

S_i (cm/s)	N_t (cm^{-2})	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Eff. (%)
10^3	10^5	1069	24.8	78.0	20.6
10^4	10^6	1067	24.8	77.5	20.5
10^5	10^7	1052	24.8	72.6	18.9
10^6	10^8	951	24.8	69.5	16.4
10^7	10^9	811	24.8	80.0	16.1

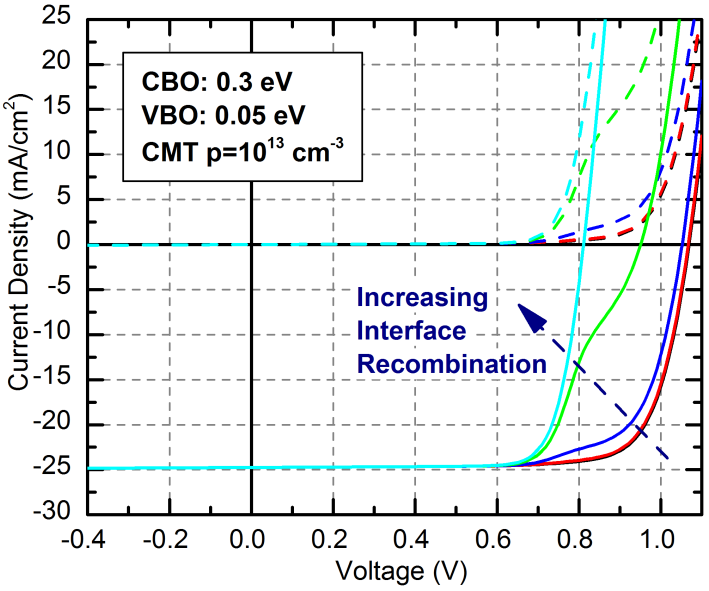

Figure 6.7: Light (solid) and dark (dashed) J-V curves of modeled CdS/2μm CdTe/200nm CMT structures with varying CdTe/CMT interface recombination. Specific model parameters are noted. General model setup and parameters are provided in Appendix B.2.2.

ing current at higher voltages. To confirm this mechanism, a closer look at charge carrier concentration and recombination rate can be done with numerical models. Specifically, the six device structures from Fig. 6.9 were analyzed at a forward bias of 0.9 volts to see the impact the VBO. The selection of 0.9 V allows to see the effect of current limiting effects for high VBO devices and also see good current behavior of low VBO devices. Figure 6.10 shows the charge carrier concentration for holes and electrons and the recombination rate through the CdTe film up to the CdTe/CMT interface. When the VBO in the devices is low, holes drifting towards back-surface are able to overcome the VBO and escape. Due to this current, hole and electron charge carrier concentrations are relatively low in the bulk CdTe film. A low charge carrier concentration implies the charge carriers are collected almost as

CBO (eV)	$E_{g,CMT}$ (eV)	CBO/VBO	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Eff. (%)
-	Baseline	-	829	24.8	82	16.7
0.1	1.65	67/33	936	24.8	82	19.0
0.2	1.75	80/20	1039	24.8	79	20.4
0.3	1.85	86/14	1069	24.8	78	20.6

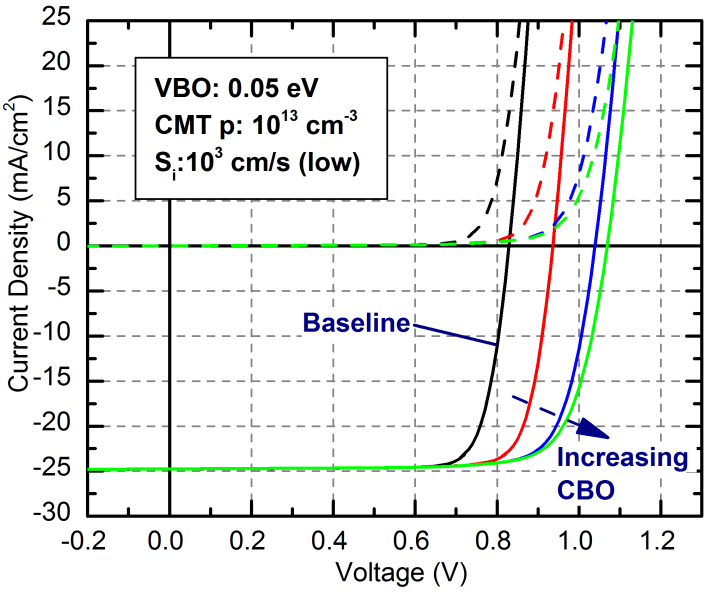

Figure 6.8: Light (solid) and dark (dashed) J-V curves of modeled CdS/2μm CdTe/200nm CMT ER structures with varying conduction-band offset. Specific model parameters are noted. General model setup and parameters are provided in Appendix B.2.2.

fast as they are generated, leading to high current conditions. Low VBO also demonstrates low recombination rates, meaning very few charge carriers are not collected. As the VBO increases, holes can no longer cross over the VBO and begin to pile up towards the CdTe/CMT interface. The high concentration of holes there leads to higher charge carrier concentrations through the bulk of the film and leads to higher recombination rates. Instead of being collected, charge carriers (electrons at the front of CdTe and holes at the back of CdTe) are recombining. Effectively, a high VBO quantum confines the holes at in the CdTe and causes significantly higher bulk and interface recombination rates. Although not shown here, at bias voltages near short-circuit current, electric fields in the device are strong and charge carriers are able to overcome the VBO and be collected, leading to much lower recombination rates and thus high currents. At forward bias, however, the electric field strength decreases

VBO (eV)	$E_{g,CMT}$ (eV)	CBO/VBO	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Eff. (%)
0.05	1.85	86/14	1,069	24.8	78.0	20.6
0.10	1.90	75/25	1,069	24.8	75.6	20.0
0.15	1.95	67/33	1,066	24.8	68.6	18.1
0.20	2.00	60/40	1,054	24.8	58.7	15.3
0.25	2.05	55/45	1,016	24.7	43.6	11.0
0.30	2.10	50/50	948	17.5	20.2	3.3

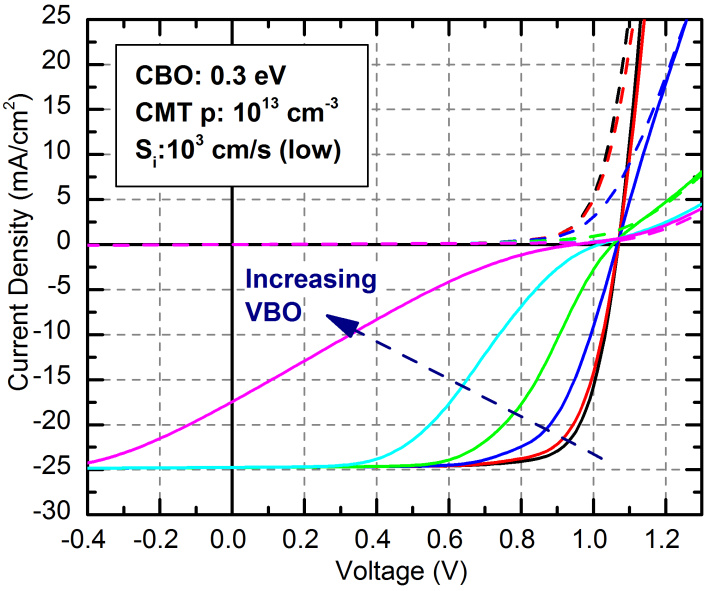

Figure 6.9: Light (solid) and dark (dashed) J-V curves of modeled CdS/2μm CdTe/200nm CMT electron reflector structures with varying valence-band offset. Specific model parameters are noted. General model setup and parameters are provided in Appendix B.2.2.

and thermionic transport of charge carriers dominates the charge carrier transport. Thus, higher barriers (VBO) to holes at the back surface produce less transport over the barrier and higher recombination, leading to poor current.

6.5.4 The CBO/VBO Ratio

As has been demonstrated so far, CBO and VBO in the ER structure can be varied independently to induce the positive and negative effects of the electron reflector layer. During experimentation however, the VBO and CBO cannot be varied independently, only the CMT band gap, which includes the CBO and VBO (i.e. $E_{g,CMT} = E_{g,CdTe} + CBO +$

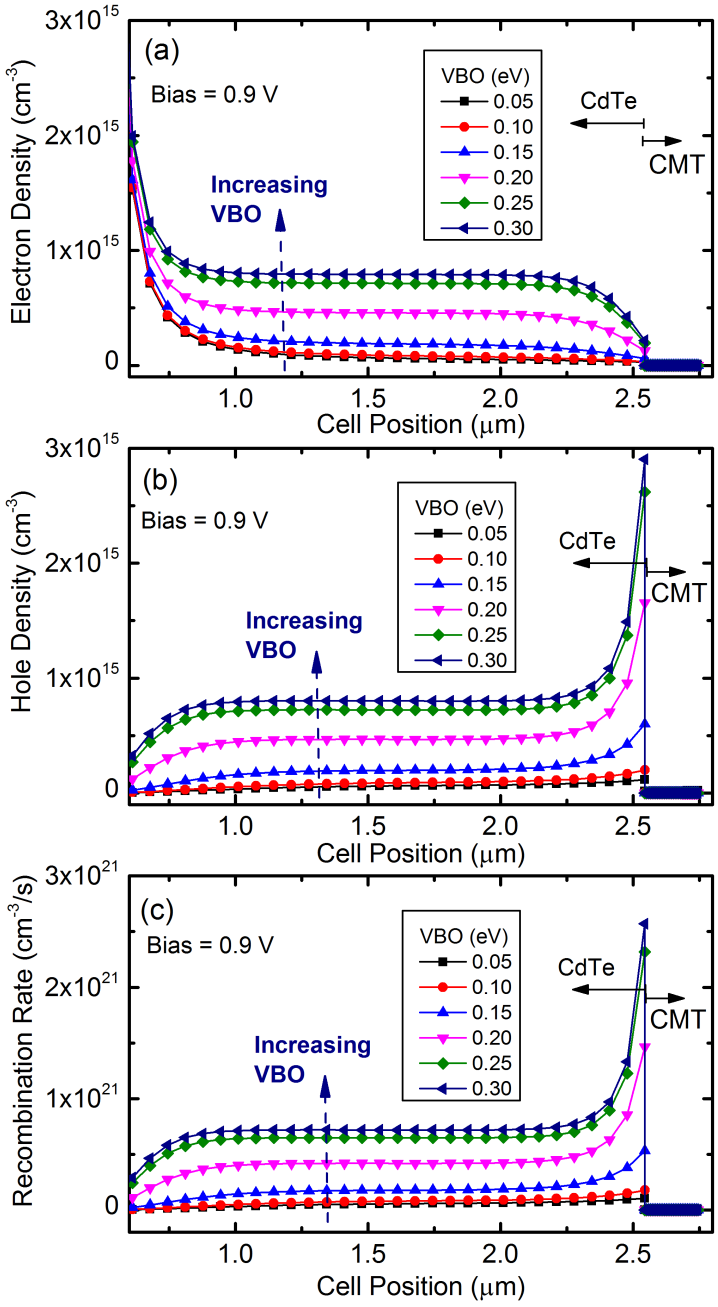

Figure 6.10: Electron (a) and hole (b) charge carrier concentrations and recombination rate (c) of modeled CdS/2μm CdTe/200nm CMT electron reflector structures with varying VBO. Light bias and voltage bias of 0.9 V was applied. Specific model parameters are the same as in Fig. 6.9. General model setup and parameters are provided in Appendix B.2.2.

VBO), can be varied. Furthermore, the ratio of CBO to VBO is poorly understood. As discussed in Section 2.2.2, the ratio is also poorly defined in literature. Direct measurements of the VBO have also been unsuccessful due to high rate of oxidation by the CMT films. Modeling of the ER structure was used to investigate the possible CBO/VBO ratio and its role in generating the V_{OC} increase and the barrier effect. Figure 6.11 shows three J-V plots of modeled CdS/CdTe/CMT devices with varying CMT band gap and CBO/VBO ratio.

The left portion of Fig. 6.11 shows a relatively good CBO/VBO ratio of 60/40. In this case, as the CMT band gap is increased, V_{OC} increases with little effect on FF. When the band gap reaches 1.8 eV, however, the VBO reaches 0.12 eV and a barrier starts to form. Increasing the band gap further produces devices with good V_{OC} but poor FF.

The middle graph of Fig. 6.11 shows the J-V curves of devices with CBO/VBO ratio set at 50/50. Again, as the band gap is increased, a smaller increase in V_{OC} is evident. Once the VBO reaches a value of 0.15 eV and above, a barrier starts to form, replicating the experimental results. V_{OC} values in these devices is around 980 mV, which is about 100 mV less than devices with high CBO and low VBO (see Fig. 6.9), indicating some V_{OC} gain may not be realized due to barrier formation at lower CMT band gap.

The right plot in Fig. 6.11 shows the J-V curves at an extremely poor CBO/VBO ratio of 30/70. As the band gap is increased, very little voltage gain is found, likely due to much lower CBO. The onset of the barrier behavior appears to initiate at higher values of VBO than in other models. In this case, the barrier forms between 0.21 eV and 0.28 eV VBO. This suggests the impact of VBO may be related to the value of CBO. When the barrier does form, it seems to form a kink in the power quadrant of the J-V curve and still produces high forward current past V_{OC}. This J-V behavior is significantly different from both experimental and other modeled results, indicating experimental CBO/VBO ratios are likely not close to 30/70.

Comparing the J-V trends of the CBO/VBO ratio models presented here to the J-V trends of experimental data (Fig. 6.2), it is likely the effective CBO/VBO ratio in experimental devices is close to a 50/50 ratio. The onset of the barrier occurs at similar band gaps

CBO (eV)	VBO (eV)	Eg (eV)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff. (%)
0.06	0.04	1.60	895	24.8	82.1	18.2
0.12	0.08	1.70	956	24.8	81.3	19.2
0.18	0.12	1.80	1,012	24.8	76.8	19.2
0.24	0.16	1.90	1,044	24.8	68.0	17.6
0.27	0.18	1.95	1,051	24.8	63.1	16.4
0.30	0.20	2.00	1,054	24.8	58.7	15.3
0.36	0.24	2.10	1,042	24.7	47.1	12.1

CBO (eV)	VBO (eV)	Eg (eV)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff. (%)
0.10	0.10	1.7	931	24.8	81.0	18.7
0.15	0.15	1.8	967	24.8	74.8	17.9
0.20	0.20	1.9	982	24.8	62.9	15.3
0.25	0.25	2.0	981	24.7	45.2	11.0
0.30	0.30	2.1	948	17.5	20.2	3.3

CBO (eV)	VBO (eV)	Eg (eV)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff. (%)
0.03	0.07	1.6	866	24.8	81.8	17.5
0.06	0.14	1.7	878	24.8	79.6	17.3
0.09	0.21	1.8	868	24.8	68.2	14.7
0.12	0.28	1.9	838	24.5	30.4	6.2
0.15	0.35	2.0	779	2.9	22.2	0.5

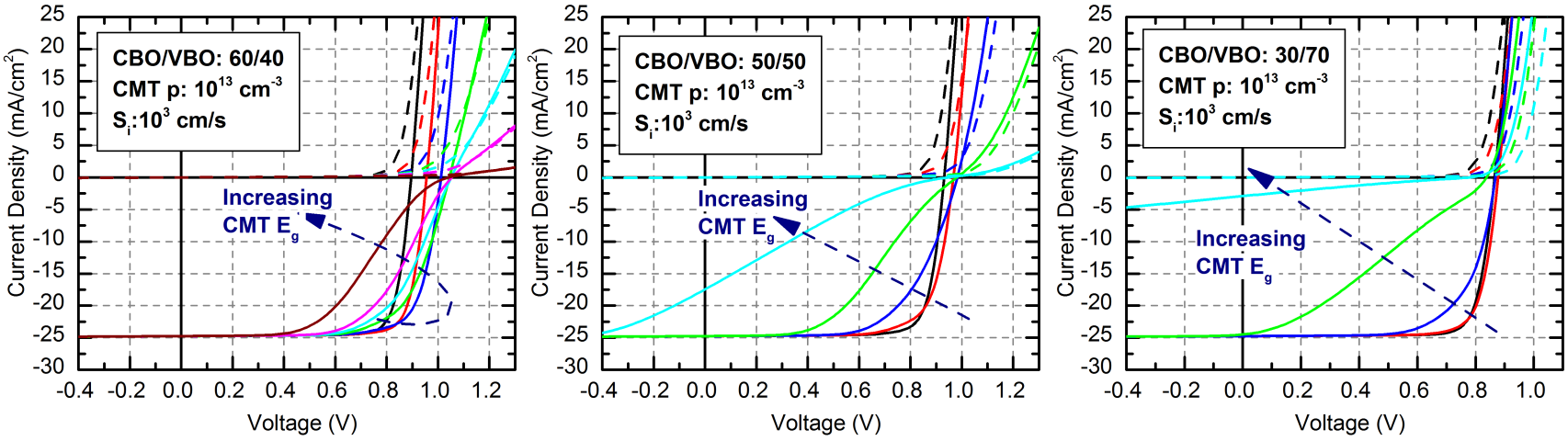

Figure 6.11: Light (solid) and dark (dashed) J-V curves of modeled CdS/2μm CdTe/200nm CMT electron reflector structures with varying CBO/VBO ratio and CMT band gap. Specific model parameters are noted. General model setup and parameters are provided in Appendix B.2.2.

and proceeds with similar patterns as seen in experimentation. Despite the similar trends, V_{OC} is higher in the models than in experiments. This is attributed to additional voltage loss mechanism that exist in experimental samples and to generous parameters used in the computational models for the baseline cell.

6.5.5 Modeling Thinning CdTe/CMT Structures

In an effort to understand the role of thinning CdTe on the function of ER devices, modeling was used to see if the parameter behavior shown in Fig. 6.4 can be replicated. The computational model was set up with varying CMT band gap, no CdTe/CMT interface recombination, and a 50/50 CBO/VBO ratio. CdTe thickness was varied from 1.75μm to 0.5μm. General model parameters are shown in Table B.3. The baseline parameters of CdTe and CMT doping and carrier lifetimes were changed to better represent physical conditions in a CdS/CdTe solar cell. Figure 6.12 parameter results of these models and should be directly compared to Fig. 6.4.

Experimental data showed that the CMT ER layer helps maintain device V_{OC} as the CdTe is thinned. This is attributed to reduction of back-surface recombination due to a conduction-band barrier (CBO) provided by higher band gap CMT films. Modeling results for V_{OC} (Fig. 6.12top-left) show a similar pattern. Without the added CMT layer, V_{OC} reduces as the CdTe is thinned. The addition of the CMT film not only increases the V_{OC} for thicker CdTe devices, but allows the voltage to be maintained at thinner devices. In the models, this trend starts at 1.6 eV band gap and continues up to 1.7 eV. At CMT band gaps of 1.8eV and higher, the models even show an improvement to V_{OC} as the CdTe is thinned. This may be due to improved electric field at the junction when the device is thinned.

Both experiment and models show identical behavior in the short-circuit current. As the main absorber (CdTe) is thinned, current is reduced due to smaller absorption region for the incoming light.

In experiments, as CdTe was thinned, FF was reduced in standard devices but increased in ER devices. Modeling results (Fig. 6.12bottom-left), however, show a small increase in

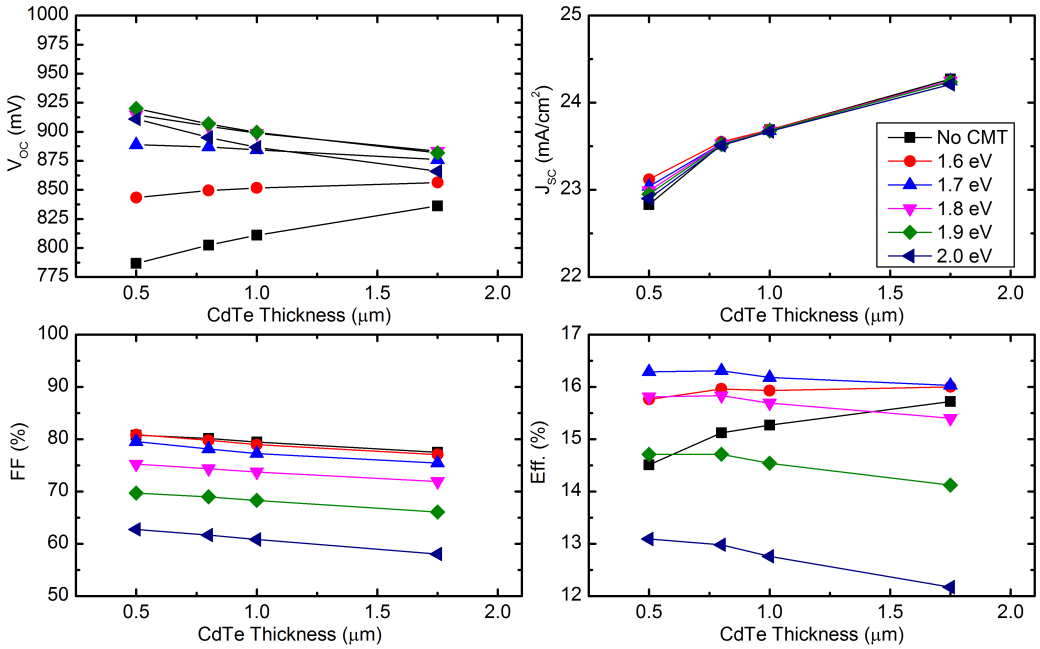

Figure 6.12: J-V parameters of modeled CdS/CdTe/130nm CMT electron reflector structures with varying CdTe thickness and CMT band gap. The CBO/VBO ratio was held at 50/50. Specific model parameters and model setup are provided in Appendix B.2.3.

FF with thinning of CdTe in both "No CMT" and "CMT" devices. This suggests that either the back-surface recombination or the back-contact barrier is higher in experimental devices than in the models. Decreasing the work function of the back metal (i.e. increasing the back barrier) can be used to investigate this further in future work. Increasing the band gap of the CMT film shows a bulk reduction of FF, which is attributed to the VBO barrier issues described earlier. Both experiment and model results show an improvement to FF when the CdTe is thinned, suggesting the barrier effect is reduced when the ER film is within the depletion region in CdTe. Absolute values of FF and smaller FF improvements produced by computational models suggests another FF loss mechanism may be present in experimental work.

6.6 Discussion of Modeling Results

Modeling of CdS/CdTe/CMT ER devices has demonstrated multiple J-V behaviors that improve the understanding of experimental results. First, modeling of recombination velocity at the CdTe/CMT interface shows a kink formation in the J-V curve that is not seen in experimental results, suggesting the CdTe/CMT interface in experimental devices is relatively good. This is consistent with TRPL measurements of the CdTe/CMT interface, which show an improvement in carrier lifetime. Due to the low lattice mismatch between CMT and CdTe (see Chapter 2) and confirmed polycrystalline epitaxy of CMT on CdTe (see Chapter 4), it is likely this interface has low density of electronic defects.

Modeling the effect of CBO (conduction-band barrier to electrons) and VBO (valence-band barrier to holes) on device parameters shows significant results correlated to experimentally seen trends. First, the addition of a CBO demonstrates positive improvements in device V_{OC}, as is expected, and no significant impact on FF. Increasing CBO in ER devices shifts the dark J-V curves to higher turn-on voltages, which is consistent with experimentally observed data. This implies that in experimental ER devices, a CBO is present in the band structure and is seen during dark measurements of the solar cell. Increasing the VBO in modeled device structures showed an increase in barrier behavior in the J-V curve. Additional analysis of the charge-carrier concentrations and recombination rate reveals that poor current at high forward bias is associated with poor hole current over the VBO. Due to a high VBO, holes are unable to reach the back contact, creating a large concentration of holes in the bulk CdTe and thus higher recombination rate. This suggests the VBO may be a significant source of barrier behavior seen in experimental samples.

Analysis of the CBO/VBO ratio, which is assumed to be constant with CMT band gap, further shows the barrier behavior is associated with the presence of both CBO and VBO in the band diagram. If the CMT film had very low CBO and very high VBO (e.g. a 30/70 CBO/VBO ratio), several J-V curve trends seen experimental would not be present. These include, a shift of the dark J-V to higher turn-on voltage, a roll-over of of the curves in

forward current, and small cross-over of light and dark J-V curves. Qualitative assessment of J-V trends produced by modeling suggest the effective CBO/VBO ratio in experimental device is close to 50/50. Additional modeling and direct measurements of the VBO and CBO in experimental device would be useful to confirm this interpretation.

Modeling used to replicate the thinning CdTe experiments showed very similar trends for V_{OC} and FF to the experimental results. The addition of a CMT based ER layer not only improves the device V_{OC}, but also maintains the V_{OC} as the CdTe is thinned. Slight improvements in FF are also evident in modeling results, suggesting thinner CdTe may reduce the impact of the VBO present in the band structure. Despite similar results, models showed lower improvements and higher absolute values of the V_{OC} and FF implying either the models need additional refinement to replicate physical behavior and that other V_{OC} and FF loss mechanism likely exist in experimental cells. For example, the confirmed presence of oxide layers at the back surface of CMT films (see Chapter 5) may have additional impact on FF and V_{OC} that is not captured in the models.

6.7 Summary

Experimental results of CdS/CdTe/CMT electron reflector devices showed a formation of a large barrier with increased CMT band gap, leading to small increases in V_{OC} but significant losses in FF. Device modeling and additional electro-optical characterization was used to investigate the source of this barrier behavior. Modeling data and TRPL results suggest the CdTe/CMT interface is not a likely source of this barrier behavior. In fact, TRPL showed an improvement in carrier lifetime due to the addition of the CMT film. Modeling of the CBO and VBO parameters in the band structure revealed that a substantial CBO is present in experimental devices. This was also confirmed by modeling and experimentation of ER devices with thinner CdTe absorbers, which showed lower back-surface recombination due to the ER layer. The presence of the CBO is a positive sign and indicates the CMT film does act as an electron reflector. However, modeling showed the barrier behavior likely stems

from the addition of a VBO to the device band structure. The VBO impedes hole current at the back surface, resulting in higher bulk recombination and current loss at voltages near V_{OC}. Furthermore, the models suggest the CBO/VBO ratio is likely close to 50/50 and other FF and V_{OC} loss mechanisms may be present in experimental devices. For these reasons, the estimated efficiency gains expected with ER structures have yet to be realized.

Chapter 7

Summary

7.1 Summary of Presented Work

The development of CdS/CdTe/$Cd_{1-x}Mg_xTe$ electron reflector structures has undergone a sequential development. First, a novel co-sublimation method for deposition of $Cd_{1-x}Mg_xTe$ thin films was developed. After significant process optimization and improvement, co-sublimation of CMT thin films was not only consistent but also demonstrated superb production rates, allowing many samples to be produced in a short amount of time.

At low substrate temperatures, CMT films deposited non-uniformly on CdTe, creating inconsistent CMT film thickness and sometimes gaps in the film coverage. At higher substrate temperatures, CMT deposited uniformly on CdTe with even thickness. Additional analysis of the CMT films and the CdTe/CMT interface showed that regardless of deposition temperature, in the range of 400 to 480°C, CMT grains grow epitaxially on the underlying CdTe films. The deposited CMT films retain the same grain orientation, structural defects, and grain boundaries as the polycrystalline CdTe directly beneath it. Additionally, the CdTe/CMT interface was found to be relatively abrupt in composition but uniform in grain structure.

Although it was shown that Cl-based treatment is useful in improving doping properties of the CMT film, a significant band gap reduction problem was discovered. Material analysis of films revealed the band gap loss was due to Mg loss from the CMT film and formation of Mg-based oxides on the film surface. Furthermore, Mg reduction was evident at the grain boundaries where $CdCl_2$ typically enters the CdTe film. The degree of band gap reduction was found to be affected by O_2 residual gas during treatment and can be mitigated with addition of $MgCl_2$ to the treatment source material and reduction of O_2 and H_2O

partial pressure during treatment. Additional process optimization is suggested for future development.

In Chapter 6, results of CdS/CdTe/CMT electron reflector devices are presented and analyzed with numerical modeling. Experiments show the addition of a CMT film improves carrier lifetime as measured by TRPL and increases carrier collection width as measured by EBIC. This indicates the CdTe/CMT interface has low concentrations of electronic defects. The presence of the desired conduction-band barrier (CBO) is found due to higher dark turn-on voltage of ER devices with increasing CMT band gap and due to higher V_{OC} when the CdTe absorber is thinned. Increasing CMT band gap, however, also significantly reduces the FF of the devices by introducing a barrier. Device modeling was used to investigate the source of this barrier, which is attributed to the presence of a valence-band barrier to holes (VBO). The VBO reduces hole current from the CdTe to the back electrode at forward bias near V_{OC}, and this causes a higher recombination rate in the bulk CdTe absorber. Additionally, modeling data suggest the effective CBO/VBO ratio is on the order of 50/50 in experimental devices, which produces lower V_{OC} gains and FF issues.

7.2 Suggested Future Work

Significant progress has been made to implement CMT films as an electron reflector layer in CdS/CdTe solar cells. Despite the progress, however, improvements to V_{OC} have been minimal. Furthermore, degradation in FF is seen with the addition of CMT electron reflector films. Additional processing and device structure improvements can be used to solve the aforementioned performance problems. For example, FF degradation, which maybe associated with a high valence-band barrier at the CdTe/CMT interface, can be mitigated by improving doping of the CMT film. By increasing doping of p-type CMT to 10^{16} cm^{-3} or above, FF issues can be mitigated. This can be accomplished with, for example As or N doping of CMT layers with various processing methods, such as reactive sputtering, plasma enhanced sublimation, or Metal-Organic Chemical Vapor Deposition (MOCVD).

Nitrogen doping of tellurium-based II-VI compounds, such as CdTe, MgTe, and ZnTe, up to 10^{16} cm^{-3} and above has been demonstrated by molecular beam epitaxy (MBE) [107] and could be investigated for polycrystalline deposition processes.

Some FF and V_{OC} losses may arise due to oxide formation and Mg-loss mechanism that occur during passivation treatment. Improved processing and different structures could be used to resolve these issues. For example, passivation process parameters can reduce the Mg-loss and oxide formation. Lower O_2 and H_2O partial pressures and use of $MgCl_2$ during treatment has been shown to reduce Mg-loss (see Chapter 5). ER devices with this process have not yet been optimized. Additional process optimization could improve the FF and V_{OC} of electron reflector devices. Finally, a CdTe-based capping layer on the deposited CMT film can be used to reduce oxide formation. This is already in practice in MBE-grown CdTe/CMT structures [106] and helps with oxide layer reduction.

If the above suggestions do not work to improve ER devices performance, a different material could be used for the ER layer to reduce the VBO. For example, alloying CdTe with Zn or Mn also increases their band gap. Investigation of these alloys may be useful in making a successful electron reflector structure in CdS/CdTe solar cells. For example, $Cd_{1-x}Zn_xTe$ alloys do not form a VBO with CdTe (see Chapter 2), thus the barrier problems seen with CdS/CdTe/CMT devices could be reduced. Processing of these other alloys, however, present other challenges that will need to be addressed.

Regardless of the method chosen, CdS/CdTe devices implementing an electron reflector have significant capability to improve device efficiency and reduce costs over standard CdS/CdTe devices.

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Appendix A

Background[1]

A.1 Solar Cell Operation

Photovoltaic (PV) devices are made from semiconductor materials, which have the capacity to absorb photon energy of light and deliver a part of that energy to electrical current charge carriers (i.e. holes and electrons). Semiconductor materials are usually doped for preferential electrical properties, such as density of charge carriers. PV devices are able to preferentially conduct electrical current by utilizing a semiconductor diode, which is able to separate generated charge carriers and force travel through an external electrical path, thus supplying electricity.

A.1.1 Semiconductor Physics

All materials have distinct electron energy bands that define their electronic properties. The valence band of the material is defined as the highest electron energy band which contains electrons. The electron energy level where electrons can move freely through the material is defined as the conduction band. Ideally, the gap between the valence-band maximum (VBM) and the conduction-band minimum (CBM) excludes any possible energy states where electrons can exist, and therefore called the forbidden gap. The nature of this forbidden gap is an important characteristic in all materials. If the gap is small or non-existent (i.e. the VBM and CBM overlap), the material acts as an electrical conductor, such as most metals. If this gap is extremely large then electrons from the VBM need extremely high energies to be promoted to the CBM for electrical conduction, which makes the material an electrical insulator. If the gap is not too large and electrons can be promoted

[1]Portions of this chapter have been published previously in the MSME Thesis of the author [93].

to the CBM through energy inputs such as heat or light absorption, the material is dubbed a semiconductor. Semiconductors are very useful materials in electronics and the backbone of modern electronic technology. In semiconductors, the energy it takes to promote an electron from VBM to CBM is defined as the band gap of the material and is given by:

$$E_g = E_C - E_V \tag{A.1}$$

where E_C is the energy of CBM and E_V is the energy of the VBM. Due to the relatively small values of E_g in semiconductors, electrons from the VBM can be promoted to the CBM through the absorption of minimal heat by the material. At a ground state (i.e. when the material is at absolute zero temperature, 0 K), only electrons will exist in the valence-band and the conduction-band will only have holes (states where an electron can exist). When the temperature rises, some energy is absorbed by a few electrons and they are promoted to the conduction band, leaving behind holes in the valence band. The probability of occupation is defined by the Fermi-Dirac distribution and is a function of temperature. The energy level where this probability is equal to 50% is defined as the Fermi energy of the material, E_F, and provides insight on the electronic properties of the semiconductor. For example, in intrinsic semiconductors at thermal equilibrium and without external excitation, the 50% probability falls near the halfway point between E_C and E_V. It is possible to calculate the charge-carriers density (electrons, n, in conduction band or holes, p, in the valence band) for the material using:

$$n = N_C e^{[-(E_C - E_F)/kT]} \tag{A.2}$$

$$p = N_V e^{[-(E_F - E_V)/kT]} \tag{A.3}$$

where N_C and N_V are effective density of states in the conduction band and valence band respectively, k is the Boltzmann constant (1.38×10^{-23} J/K), and T is the absolute temperature in Kelvin. In intrinsic semiconductors, electrons in the valence band equal to holes in the conduction band and therefore $n = p$.

Carrier densities of semiconductors can be tuned by applying extrinsic doping to the material that create states within the band gap with very small ionization energies. Depending on the state of the dopant, they can either add electrons (donors) or holes (acceptors) to the system. A semiconductor with a large donor density, N_D, is considered n-type and has electrons as the majority and holes as the minority carriers. A large acceptor density, N_A, makes p-type semiconductors with holes as the majority and electrons as the minority charge carriers. N_D states are close to the conduction band while N_A states are close to the valence band. Charge carrier concentrations are typically assumed to be equal to donor or acceptor concentrations, i.e. $n \approx N_D$ for n-type and $p \approx N_A$ for p-type semiconductors. Due to the changing carrier densities, a new position for the Fermi energy may be found using:

$$E_F - E_V = kTln\left(N_V/N_A\right) \tag{A.4}$$

for p-type semiconductors, and

$$E_C - E_F = kTln\left(N_C/N_D\right) \tag{A.5}$$

for n-type semiconductors. The Fermi energy shifts closer to the valence band for p-type and closer to the conduction band for n-type semiconductors.

In addition to thermal input, other external sources, such as light or applied electric field, can promote electrons from the valence band to the conduction band. The absorbance of light for this promotion is the primary functioning mechanism of a photovoltaic semiconductor. When light is absorbed, an electron in the valence band jumps to the conduction band, making an electron-hole pair. The electron and hole can move separately either by diffusion or due to an electric field present. The electron-hole pair can be annihilated by the demotion of the electron in the conduction band back to the hole in the valence band. This recombination process is an important aspect of semiconductor materials and devices. Recombination can occur in several ways: (a) radiative recombination produces emitted light usually equal in energy to the electron transition, (b) non-radiative recombination, where the released energy is in the form of a phonon in the material, and (c) Shockley-Read-Hall (SRH) recombination

where the electron travels through a mid-gap state caused by defects or impurities. The time it takes between generation and recombination of the electron-hole pair is the carrier lifetime of the semiconductor.

A.1.2 Solar Cell Device Physics

The diode, also referred to as the $p-n$ junction, is created when a $p-$type material (doped to have holes as majority carriers) and an $n-$type material (doped to have electrons as majority carriers) are joined in electrical contact. Before contact is made, it is evident that the $p-$type material has more holes than the $n-$type material and that the n-type material has more electrons than the $p-$type material. After contact is made, gradient in respective concentrations causes electrons from the $n-$side to diffuse into the $p-$side and holes from the $p-$side to diffuse into the $n-$side until equilibrium is reached. When electrons from the $n-$region are annihilated by holes, a positive charge in the material is left. Similarly, when holes in the $p-$type region are filled with electrons, a negative charge in that region develops. These two regions of charge are collectively called the space charge region (SPR), or depletion region. Figure A.1 depicts a typical cross section of a $p-n$ junction solar cell; the SPR is located between $-X_N$ and X_P and the $p-n$ junction located at 0. The creation of the SPR produces an intrinsic electric field, ξ, which is responsible for the built-in front to back potential difference of the device, V_{bi}. This field maintains equilibrium by imparting forces on the charge carriers, disallowing any further recombination. In typical solar cell structures the photo-generation absorber layer is usually the $p-$type material, while the $n-$type materials is called the window layer, since its function is to pass photons through to the absorber layer.

There are two types of $p-n$ junctions, a heterojunction and a homojunction. A homojunction is made from the same material but sections of it are differently doped to be $n-$type or $p-$type. A heterojunction is made up of two different materials that have different doping characteristics.

Homojunctions have significant advantages. Since the same materials are used for the

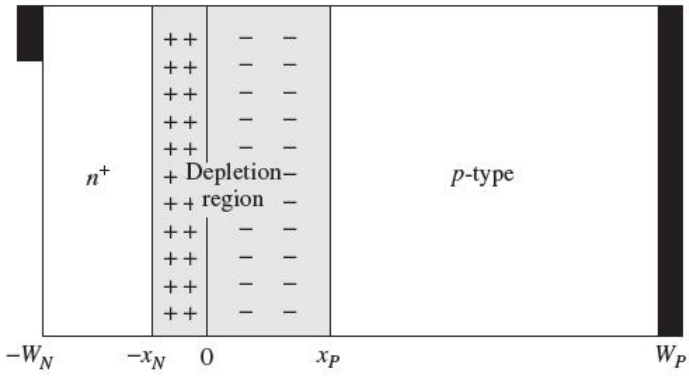

Figure A.1: Simple solar cell structure. Figure reproduced from Ref. [108].

$n-$type and $p-$type layer, the energy bands of the two layers match, thus resulting in an easier band diagram calculation. In Figure A.2, the band diagram can be easily interpreted to provide useful information, such as the built in voltage, V_{bi}, given by the following formula:

$$qV_{bi} = E_{Fn} - E_{Fp} \tag{A.6}$$

where q is the charge of one electron (1.6×10^{-16} Coulombs) and E_{Fn} and E_{Fp} are quasi-Fermi-level energies for electrons and holes respectively. Homojunctions avoid the formation of efficiency reducing barriers and spikes at the junction, thus introducing potential for improved performance. Since an absorber material is used as the window layer (typically the $n-$type material), the photon losses in this region must be considered and the thickness minimized. Thin window layers in homojunctions still provide non-trivial photon losses as well as the possibility of current losses due to surface recombination.

Heterojunctions, on the other hand, use different materials for the absorber and window layer, thus allowing flexibility in choosing appropriate materials. Typically, a material with higher band gap is desired for the window layer to allow more photons for absorption by the photo-generation layer. Although photon loss is minimized, the variation in band energies presents other problems, such as energy barriers (represented by spikes in Figure A.3) and interface states, making it harder to calculate band bending and predict performance. Additionally, intermediate compositions, lattice mismatch, and phase differences add to the

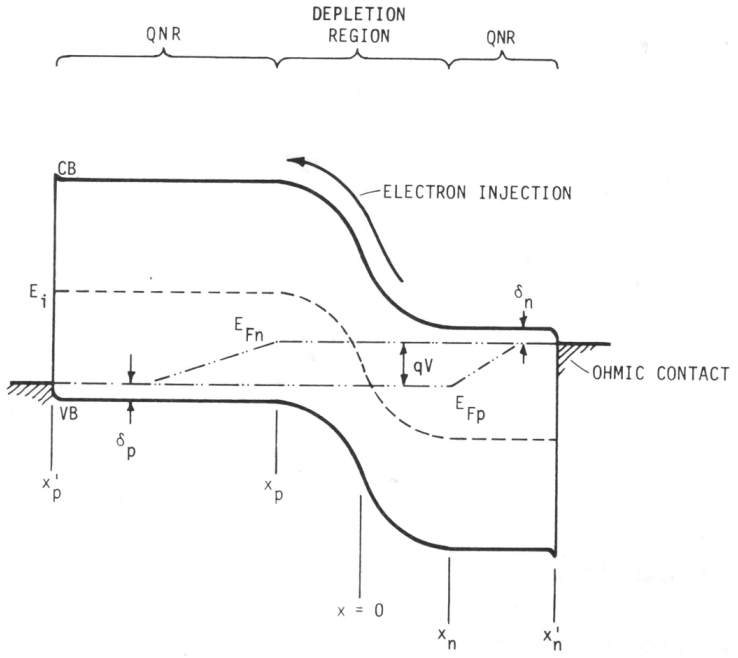

Figure A.2: Typical band diagram of a homojunction solar cell device. Figure reproduced from Ref. [109].

complexity of these junctions. Some mathematical models aim at predicting the behavior of the device (e.g. the Anderson model for heterojunctions [109]), but even these are not sufficient for complex junctions, such as CdS/CdTe.

A.1.3 Solar Cell Electrical Operation

When the junction is under light irradiation, photons with energy larger than the band gap, E_g, are absorbed and electron-hole pairs are created. The minority carriers in the material (i.e. electrons in the p-type material) are pushed through the $p-n$ junction, while majority carriers, holes, are pushed away from the junction towards the back contact. This separation of charge carriers leads to their accumulation at the electrodes immediately adjacent to the two semiconductor materials (e.g. at W_P and $-W_N$ in Figure A.1). If an electrical pathway was provided between these two surfaces, each pair of charge opposite charge carriers (i.e. one hole and one electron) would allow an electron charge, q ($1.6 \times$

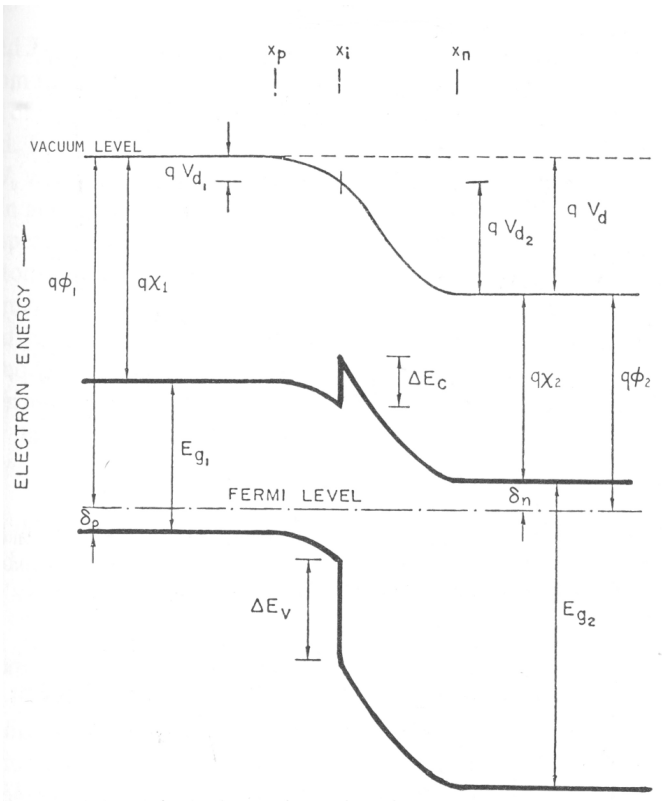

Figure A.3: Typical band diagram of a heterojunction solar cell device. Figure reproduced from Ref. [109].

10^{-16} Coulombs), to pass through the circuit. At continuous illumination, this resistance-free circuit would see constant flow of charge, which is referred to as the short circuit current, I_{SC}. Although current is an important characteristic of a solar cell, current density, J, is the usual parameter used to describe produced photocurrent. Current density is measured in mA/cm^2 and is defined by the following relation:

$$I = J * A \tag{A.7}$$

where A is the illuminated area of the cell.

Now let's assume that this circuit was not present but we still have constant illumination, the photo-generated charge carriers would accumulate at the electrodes until a new equilibrium is reached. A new electric field, ξ', is established, opposite to the intrinsic electric field. The new state also leads to a different potential difference between the electrodes,

namely the open circuit voltage, V_{OC}. V_{OC} can be derived from the two electric fields by the following equation:

$$V_{OC} = \int_{-W}^{W} (\xi' - \xi)\, \mathrm{d}x \tag{A.8}$$

It is important to note that the electric fields are dependant, among other parameters, on the electrical characteristics of chosen materials and charge carrier mobility. After evaluation of this integral, it is possible to see the various sources attributing to photovoltaic action [25], although this derivation is beyond the scope of this work.

Although J_{SC} and V_{OC} of a photovoltaic device are important characteristics, a solar cell is not designed to operate at these conditions. At V_{OC}, no current is produced thus resulting in no produced power, which is given by the following formula:

$$P = J * V \tag{A.9}$$

where P is the power density, typically in W/cm^2. At J_{SC}, V_{OC} is zero and thus $P = 0$. If the load on the device can be varied, measurements will produce a current density versus voltage ($J-V$) graph, as seen in Figure A.4, for both illuminated (light) and non-illuminated (dark) conditions. V_{OC} and J_{SC} are seen at the light plot's intersections with the x and y axes, respectively. Also on Figure A.4, a produced power density versus voltage plot is shown by the dashed line. The maximum power density of the device is given by P_{max}, located at corresponding current density, J_{max}, and voltage, V_{max}. Several cell characteristics can be derived from the produced plots. First, efficiency can be found by comparing maximum power density to the power density of the illuminating light:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{J_{max} * V_{max}}{P_s} \tag{A.10}$$

where P_S is the light irradiation. Internationally standardized testing has set this figure to 100 mW/cm^2 with a AM1.5 light spectrum. Specifics on standardized light irradiation testing are discussed further in Section A.2.3 of this manuscript.

Another important cell characteristic found from a $J - V$ curve is the fill factor, FF, of the solar cell. This is thought of as the "squareness" of the curve and is given by the

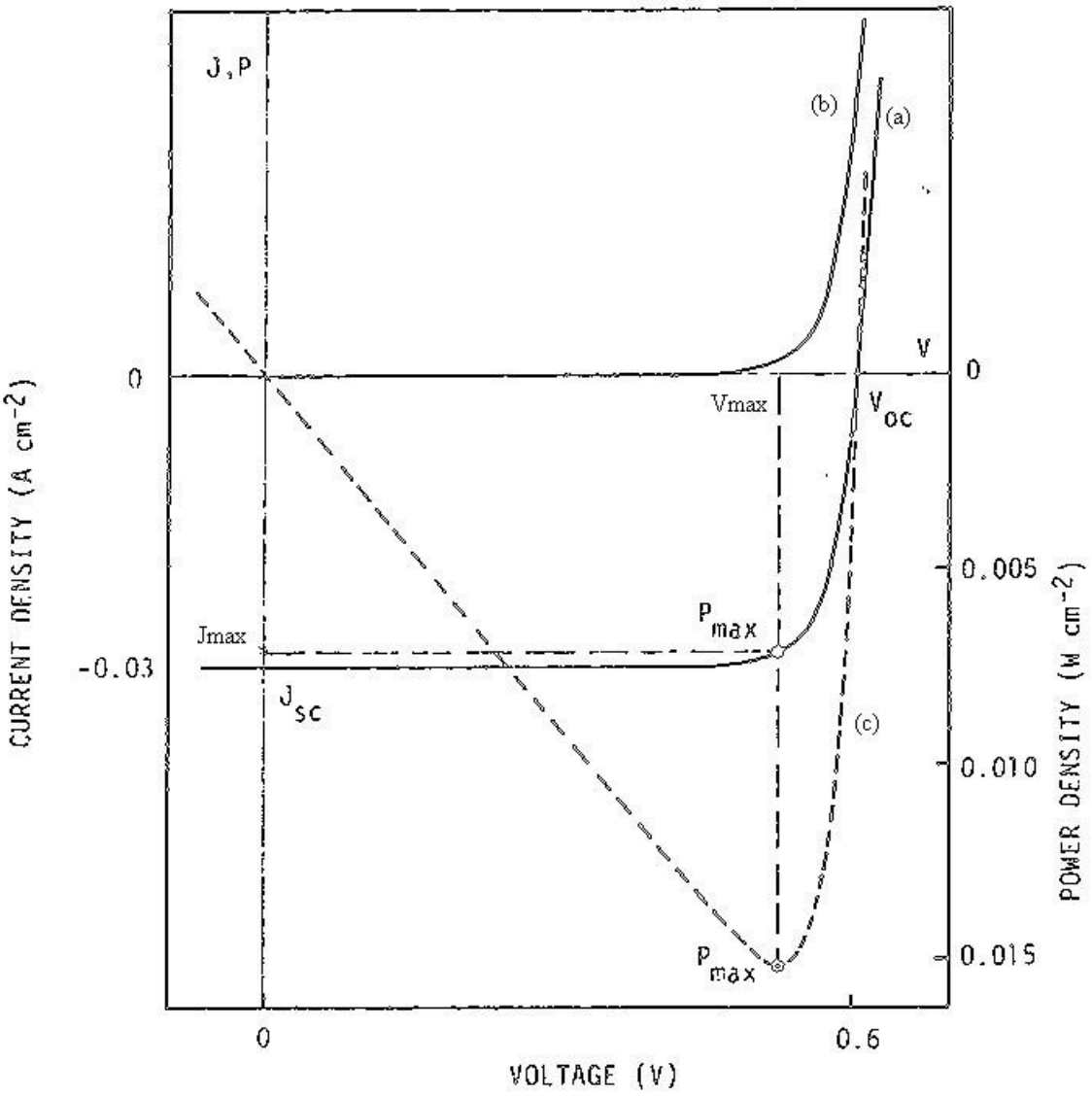

Figure A.4: Typical (a) light and (b) dark J-V curves and (c) corresponding power density. Figure reproduced from Ref. [109].

following relationship:

$$FF = \frac{J_{max} * V_{max}}{J_{SC} * V_{OC}}. \tag{A.11}$$

Fill factor is important because it can provide important insight into performance characteristics of the solar cell and lead to appropriate improvement path if such action is needed during production. Equations A.10 and A.11 can be combined to yield a new expression for

efficiency:

$$\eta = \frac{FF * J_{SC} * V_{OC}}{P_s}. \tag{A.12}$$

From Equation A.12 it is evident that efficiency of a solar cell can be improved by increasing any one of FF, V_{OC}, or J_{SC} independently of the others.

A.2 Device Characterization

There are numerous ways to characterize the performance of a solar cell. A first order measurement is to measure the current density versus applied voltage, which was described in Sec. A.1.2. This generates the power curve and determines the efficiency of the device. However, further electrical analysis, such as Capacitance-Voltage and Quantum Efficiency can used to understand device properties. This section describes these techniques in further detail.

A.2.1 Current Density-Voltage (J-V)

The power generated by a solar cell is measured using an AM1.5 spectrum simulated using various lamps. The AM1.5 spectrum is the representation of the sun spectrum that reaches the surface of Earth. The spectrum comes from the emission of radiation from the sun. The sun's surface temperature is 5762 K and its radiation can be modeled as isotropic black-body radiation at that temperature. Some of this radiation will be lost on its way to Earth. Additionally, not all of the radiation will penetrate through the earth's atmosphere. The spectrum that reaches just above Earth's atmosphere is referred to as air mass zero, AM0, and has an intensity of 1,353 W/m^2. The spectrum that reaches the surface of the earth is called air mass 1.5, or AM1.5, and has a normalized intensity of 1,000 W/m^2 [108]. AM1.5 is normalized because it can change significantly with the angle of penetration within the atmosphere. Black body, AM0, and AM1.5g spectra are presented in Fig. A.5. AM1.5g indicates a global spectrum: one that includes a diffusion component, and is the typical spectrum used in analysis and oftentimes simply called AM1.5. A direct spectrum, one

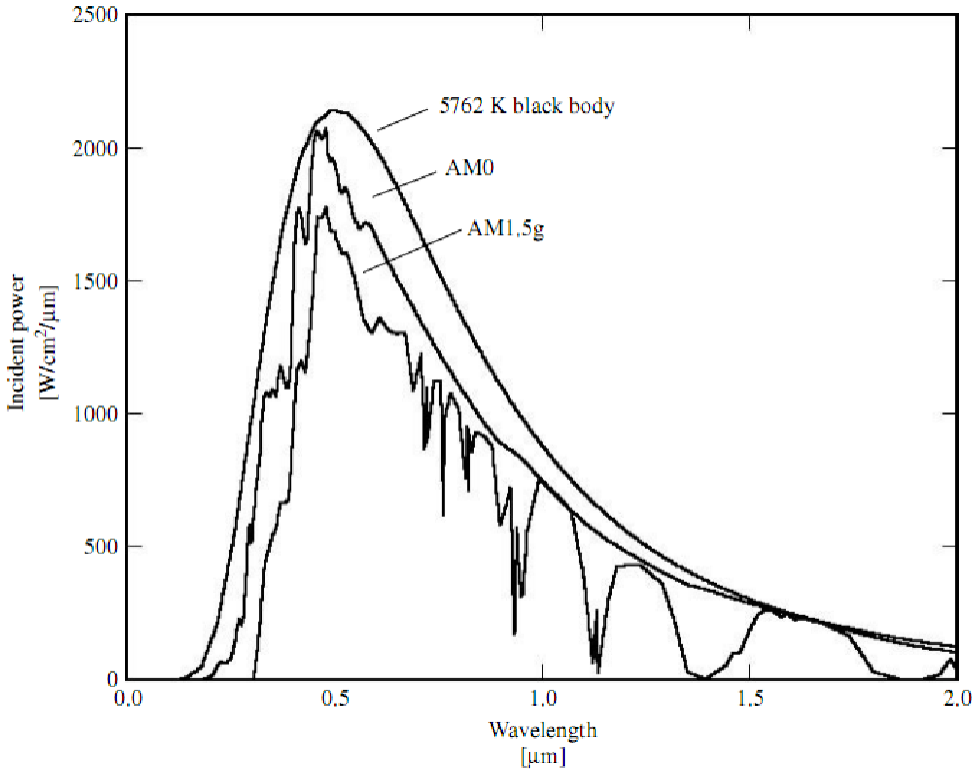

Figure A.5: Radiation spectra of a black body at 5762 K, AM0, and AM1.5g. Figure reproduced from Ref. [108].

without the diffusion component, is called AM1.5d.

J-V testing equipment is designed to simulate the AM1.5 spectrum while maintaining the correct intensity of 1,000 W/m^2 (100 mW/cm^2). This is done through use of a wide variety of lamps and through calibration. Calibration of the J-V test equipment in these tests was done by using a standard solar cell that has been previously tested and confirmed by NREL. Additionally, testing is done at roughly standard operating conditions (25°C), as temperature has a significant impact of voltage performance of the device. Current and voltage data collection was automated using LabVIEW software. Tests are performed by sweeping voltage bias across the device and measuring the output current using a Keithley Sourcemeter. Dark J-V tests are performed without light illumination.

A.2.2 Capacitance-Voltage (C-V)

Capacitance-Voltage (C-V) measurements are one type of admittance spectroscopy aimed at measuring the cell's depletion width and carrier densities. The C-V technique measures the AC response of $p-n$ junctions and uses that response to interpret the carrier density profile of the solar cell. The carrier concentration is given by the following equation:

$$N_p = \frac{C^3}{q\varepsilon}\left(\frac{dV}{dC}\right) \tag{A.13}$$

where N_p is the measured carrier density, C is the measured capacitance per unit area, q is the elementary electric charge, ε is the material permittivity, and V is the applied voltage. Typically, measured carrier density can be plotted against the distance from junction, W, via:

$$W\left(V\right) = \frac{\varepsilon}{C\left(V\right)} \tag{A.14}$$

These measurements can be useful for understanding of the properties of the solar cell. However, significant care must be taken in interpreting the results, as the capacitance will be influenced significantly by the back contact, deep levels, and absorber thickness of the cell structure and typically overestimates the carrier concentration of the material [101]. Nonetheless, qualitative comparisons of C-V profiles of two similar devices may be useful in optimizing the device structure.

A.2.3 Quantum Efficiency (QE)

Quantum efficiency (QE) measurements measure the spectral current response of the solar cell. It is a simple measurement, where a solar cell's photocurrent is measured for each wavelength of incident light. The quantum efficiency for each wavelength is the ratio of output current to input photon flux. A QE of unity indicates all incoming photons yield a collected charge carrier at that particular wavelength. QE, coupled with transmission and reflection data of the solar cell, can easily quantify photon losses in a device. A typical photon accounting plot, with included QE, for a CdS/CdTe solar cell is shown in Figure A.6 [110].

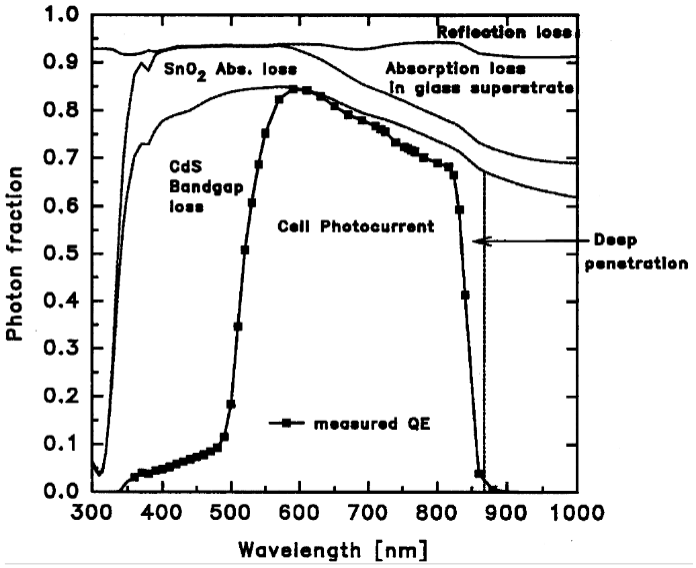

Figure A.6: A typical QE plot of a CdTe solar cell. Figure reproduced from Ref. [110].

Some interesting features are seen in the plot. CdS absorption losses are seen in the short wavelength onset of the QE at around 500 nm, which is the CdS band gap of approximate 2.5 eV. The CdTe band gap is seen in the long wavelength edge of the QE plot (around 850 nm). Other optical losses are also shown, for example reflection and absorption losses associated with the glass, TCO absorption, and deep penetration losses in the CdTe.

Without outside biases, QE measurements are done at short-circuit current conditions. However, applying a bias can be useful in seeing the spectral photocurrent of the cell at different conditions. For example, applying a white light bias puts the cell close to open-circuit voltage where the depletion width is narrow. Applying DC bias can also produce interesting results. For example, a small reverse bias, which extends the depletion width, can provide insight on the quality of the back contact of device in some thin-film solar cells.

A.3 Material Characterization

Several material analysis methods are used to characterize the microstructural features and chemical composition of the deposited thin films. Techniques used in the studies pre-

sented in this manuscript include X-ray Diffraction (XRD), Scanning Electron Microscopy (SEM), Energy Dispersion X-Ray Spectroscopy (EDS), and X-ray Photoelectron Spectroscopy (XPS). Additional electro-optical characterization was done using Time-Resolved Photoluminescence (TRPL) and Electron Beam-Induced Current (EBIC) measurements. This section explains the principles and details of using these techniques. Equipment descriptions are also presented.

A.3.1 X-ray Diffraction (XRD)

XRD measures the amount of radiation striking (incident beam) an object is reflected or absorbed (diffraction spectrum). This is called Bragg diffraction and is shown in Figure A.7. Diffraction of the X-rays follows Bragg's law represented by the following equation:

$$n\lambda = 2d\sin\theta \tag{A.15}$$

where n is an integer indicating multiple wavelengths, λ is the wavelength, d is the lattice spacing, and θ is the scattering angle. Analysis of XRD spectra can yield information on the crystal structure of the material. The diffraction pattern can be analyzed two ways. First, the spectrum can identify properties of a crystalline material through appropriate calculations. Initially the lattice spacing in cubic crystals can be found using the following formula:

$$d_{hkl} = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \tag{A.16}$$

where a is the lattice parameter and h, k, and l are Miller indices. Equations A.15 and A.16 can be combined to give the following relationship:

$$\sin^2\theta = \frac{\lambda^2}{4a^2}\left(h^2 + k^2 + l^2\right) \tag{A.17}$$

from which the Miller indices can be easily calculated. Conversely, the spectrum can be compared to previously calculated spectra to a calculated confidence level, degree of fit. This method utilizes computer software to fit the diffraction patterns and calculate the

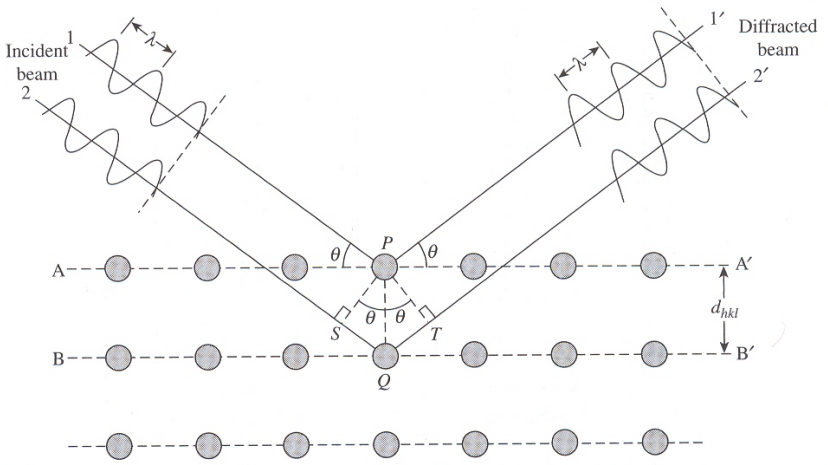

Figure A.7: Bragg diffraction by crystal planes. Figure reproduced from Ref. [111].

material characteristics. This method is the more popular due to its ease of use and large amounts of standardized data readily available for comparison.

The Central Instrumentation Facility (CIF) at Colorado State University maintains two XRD machines that were equally used in analysis. First is SCINTAG X2, utilizing a Peltier detector and Cu Kα radiation ($\lambda = 1.5418\mathring{A}$). This machine is able to analyze both powder and thin film samples. XRD peaks were fitted using Split Pearson 7 function, while unit cell parameters where calculated using TREOR 90 auto indexing software. The second XRD machine is a Bruker D-8 Discover, which also utilizes Cu Kα radiation. This machine is specific to thin films and is able to perform glancing angle and high resolution scans of the films. Sometimes, analysis of these diffraction patterns was done using XRD EVA, Topas, and Jade 5 software.

Using XRD techniques and peak fitting software several material properties were determined. First the crystal structure was found using the peak fitting software. Orientation of the thin films was analyzed using peak/sum ratios of the diffraction peaks as well as the Harris method. Additionally, unit cell parameters were calculated. These were found using both software driven calculations and through the use of the Nelson-Riley method. The Nelson-Riley method and the Harris analysis are described further in Chapter 4. Finally, Crystal

Maker software was used to verify molecular diagrams of the CdTe and CdS compounds and to evaluate the diffraction patterns.

A.3.2 Scanning Electron Microscopy (SEM)

SEM uses an electron incident beam to image the sample in the nanometer scale. A diagram of a typical SEM system is seen in Figure A.8. In this tool, a high energy electron beam passes through a condenser lens, which focuses the beam, and a probe lens, which focuses the beam into a fine probe and determines the resolution. The beam is scanned over the sample, similar to a television raster. Scattered electrons or secondary electrons are then collected to make an image. The image produced is a useful tool in seeing microstructural features of the deposited thin films. SEM equipment is also able to effectively measure distances on the images. This tool is useful in measuring layer thickness and grain size. SEM characterization was performed on a JOEL JSM-6500F, a field emission system with the In-Lens Thermal Fluid Emission Electron Gun.

A.3.3 Energy Dispersion X-ray Spectroscopy (EDS)

EDS measures characteristic X-rays from the process shown in Figure A.9. The incident excitation beam is made up of electrons. For this reason, EDS is mainly used with SEM equipment, where an electron beam is readily available. As the SEM electron beam hits atoms of the sample, secondary electrons are released from the inner electron shells of the atoms, leaving behind vacancies or holes. Electrons from outer shells drop into the vacant spot, thus dropping in energy level and releasing X-ray radiation. An EDS system collects this X-ray radiation, determines the energy level of the radiation, and analyzes the collected data. Specifically, EDS is used to identify elements of a particular sample. Coupled with the SEM, it is able to develop elemental mapping on SEM images, a useful tool in understanding multilayered thin film samples.

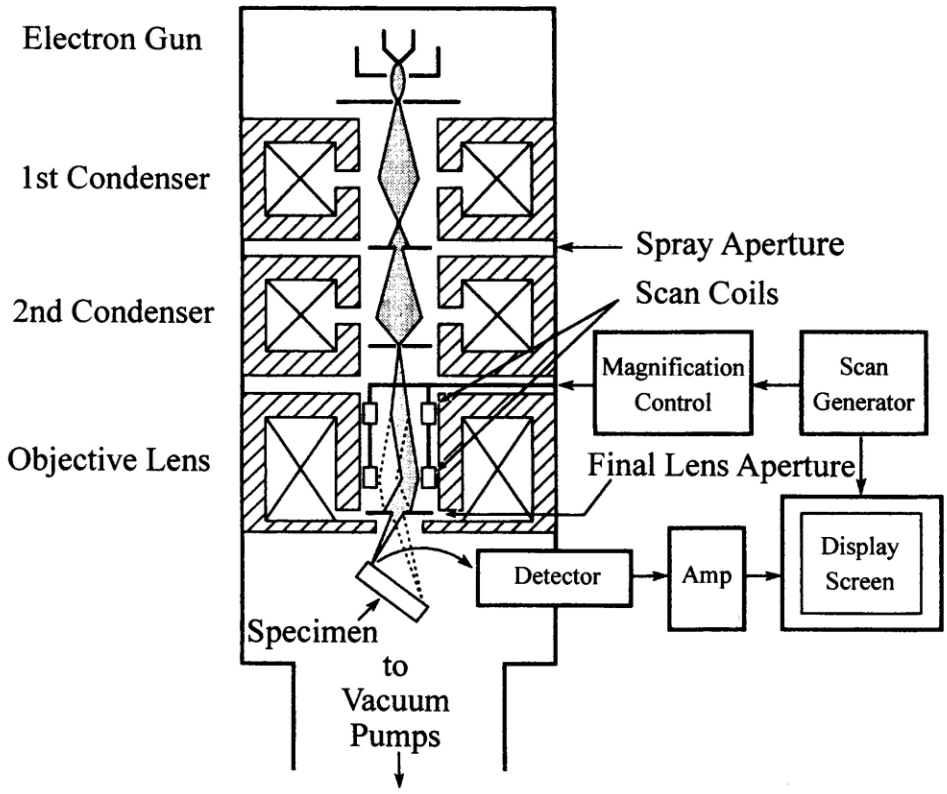

Figure A.8: Schematic of a typical Scanning Electron Microscope (SEM). Figure reproduced from Ref. [111].

A.3.4 X-ray Photoelectron Spectroscopy (XPS)

X-ray Photoelectron Spectroscopy (XPS) is another powerful tool in thin film characterization. In XPS, monochromatic X-ray radiation bombards the surface of the thin film, causing the release of electrons from various shells of the atoms (the ejected orbital electrons in Figure A.9). These electrons, which have a distinctive energy level based on their origin and the energy of probing X-ray beam, are collected and analyzed. Analysis, which compares the collected spectra against known data, can identify individual elements present in the thin film and types of bonding present in complex materials. Auger Electron Spectroscopy (AES) can also be performed with XPS equipment, giving it flexibility and improved accuracy in identifying elemental composition. In AES, the Auger electrons are produced from the absorption of emitted photons (characteristic X-rays) from the same electron relaxation process

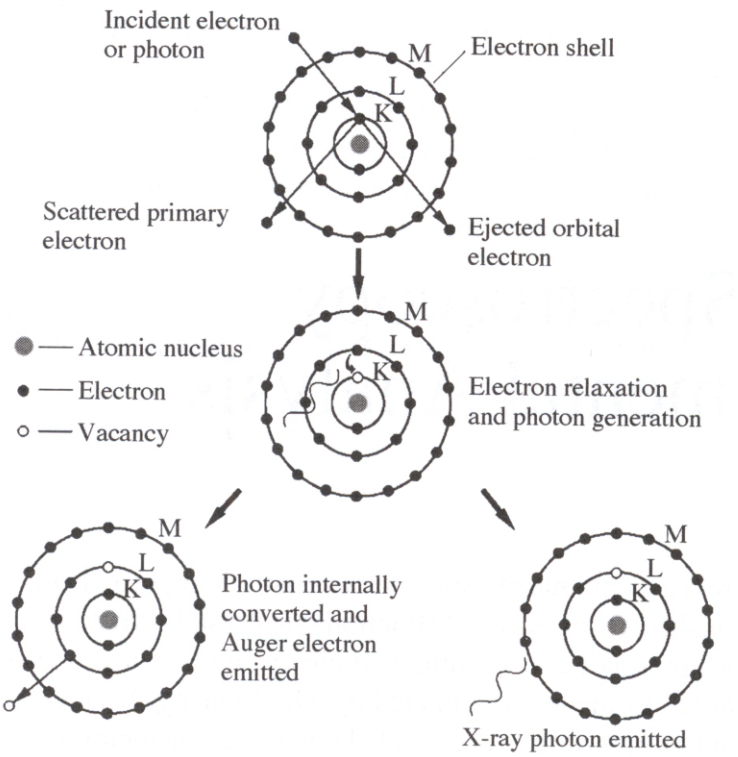

Figure A.9: Schematic of characteristic X-ray photon or Auger electron generation process. Figure reproduced from Ref. [111].

described earlier (Figure A.9). Additionally, XPS equipment can be equipped with ion (e.g. Ar^+) sputtering capabilities, where ions sputter away layers of the thin films in-between XPS analysis. This method allows depth profiling over sputtering cycles, yielding similar results to Secondary Ion Mass Spectrometry (SIMS) spectra.

A.3.5 Time-Resolved Photoluminescence (TRPL)

When light hits a photovoltaic cell, light of energy above the band gap of the material is absorbed by promoting an electron from the valence band to the conduction band, creating an electron-hole pair. If the charge carrier (electron) is not collected by the external circuit, it recombines with a hole in the valence band. Some of this recombination is radiative, releasing a photon equal to the energy of the recombination transition. By measuring this luminescence, many important parameters of the semiconductor material and PV device can

be made. Time-resolved Photoluminescence (TRPL) measures the decay of this luminescence with respect to time in order to characterize the carrier lifetime of the semiconductor material. The measurement is done by pulsing a laser on the semiconductor film or device and measuring the PL signal after the laser is turned off. Due to the fast nature of the decay, precise equipment is needed to characterize the PL decay time. TRPL measurements in this manuscript were performed at the National Renewable Energy Laboratory in Golden, CO.

A.3.6 Electron Beam-Induced Current (EBIC)

Electron Beam-Induced Current (EBIC) measurements are useful for showing the electrically active areas of PV devices. The measurement works by putting the functioning PV device in an SEM and bombarding the semiconductor surface (typically in cross-section) with an electron beam. The electron beam populates the conduction band of the semiconductor and travel through the device based on the present electric field or by diffusion. If the electron reaches the electrode of the cell, it can be collected by an ammeter and correlated to the electron beam position. This imaging of current collection provides important information on the depletion width of the solar cell and conduction paths through the thickness of the film. Changing the acceleration voltage of the electron beam and the injection current allows to investigate depth and injection related parameters of the solar cell. EBIC measurements in this manuscript were performed at the National Renewable Energy Laboratory in Golden, CO.

A.4 CdS/CdTe Devices

A.4.1 The CdS/CdTe Device Structure

The heterojunction in CdTe thin film cells is created at the interface of an $n-$type CdS layer and a $p-$type CdTe layer. Surrounding these layers, electrical contacts and a mechanical support are needed to produce a functioning cell. Cells can be grown in two config-

urations: a "superstrate", which is grown in the direction of sunlight traveling in the cell (i.e. deposition is done on transparent glass) and a "substrate", which is grown opposite the direction of irradiance (i.e. deposition on back contact or support). The superstrate configuration is the prevalent structure for high efficiency cells, and will be the focus of this manuscript. In this configuration, a glass substrate, which acts as the mechanical support, transmits light to a transparent conductive oxide (TCO) layer, the front electrode. CdS is deposited on the TCO, followed by CdTe, and application of a back contact. Post-deposition chlorine treatments and advancements in low-resistance back contact formation were found to be integral steps in improving cell performances [10]. Growth of these layers can be achieved using several deposition methods, such as closed space sublimation (CSS), evaporation, chemical vapor deposition (CVD), physical vapor deposition (PVD), chemical bath deposition (CBD), radio frequency sputtering (RFS) to name a few. Since processing methods strongly correlate to device performance and cost, their selection and execution is vital in effective large scale production.

The selection of an appropriate substrate material is very important in superstrate configurations. The substrate provides a mechanical support for the cell, thus a strong structural material is needed. In superstrate configurations, the substrate also needs to be transparent, as absorption of photon energy will lead to losses in cell performance. Processing temperature must also be considered during substrate material selection, as many deposition processes are performed at moderately high temperatures. For these reason, glass is usually used as the substrate. Glass provides a strong mechanical support for the cell, has minimal light absorption, is inexpensive, and can withstand high processing temperatures, unlike a clear polymer for example. Common types of glass used are soda lime glass and borosilicate glass. The former is less expensive while the latter can withstand higher processing temperatures.

The front electrical contact is achieved through a transparent conducting oxide (TCO). Conductivity, measured in sheet resistance, is typically around 10Ω/square. Tin oxide, SnO_2, is the most common TCO used. To reduce electrical resistance SnO_2 is often doped with indium, SnO_2:In, or fluorine, SnO_2:F. Other TCO materials include tin doped indium oxide,

In_2O_3:Sn (referred to as indium-tin oxide, ITO) and cadmium stannate, Cd_2SnO_4. Several other TCOs are in various stages of development for application in CdTe solar cell structures. Deposition methods, cost, microstructure, and optical characteristics play a crucial role in selecting a TCO. Tin oxide is the cheapest TCO available, its processing methods (e.g. sputtering) can be used in high throughput processing, and its microstructure is favorable for subsequent deposition of critical CdS layers. Electro-optical characteristics of other TCOs, however, are better than that of SnO_2, making them better options for high efficiency cells. Some cells also utilize a high resistance transparent oxide (HRT) layer, located between the TCO and CdS layer [10]. For this layer, $ZnSnO_x$ has been used and has shown to reduce local shunt paths or excessive forward current and to improve the junction quality [112].

A polycrystalline CdS layer is deposited and provides an $n-$type window layer for the $p-n$ junction, where it is coupled with a $p-$type absorbing CdTe layer. As a window layer, CdS has a wide band gap energy level of 2.42 eV at room temperature, giving it transparency to wavelengths of about 510 nm and above. Thin CdS layers can also be transparent to energy levels below 510 nm, where there is insufficient CdS material to absorb all the energy. Thus, a reduction in thickness is important for improving photocurrent to the CdTe layer. During processing, however, uniform coverage and subsequent intermixing between the CdTe and CdS layers impose a limit on CdS thinness [10]. Intermixing of CdTe and CdS layers during deposition and post treatments can lower the CdS band gap, leading to less transmission. This effect has been addressed through two primary methods of fabrication. The first method is the use of HRT layers [112, 113], which help consume CdS layer during processing and increase the band gap. The second method is to utilize $CdCl_2$ treatment prior to, rather than post, CdTe deposition [113], which recrystallizes the CdS layer and reduces intermixing problems.

The polycrystalline CdTe absorber layer is a $p-$type material, with a band gap energy of 1.45 eV. This band gap energy makes CdTe the best match to the solar spectrum and attributes to highest theoretical efficiencies of any currently used photovoltaic device. Due to lower carrier concentration in CdTe as compared to CdS, the majority of the depletion region

resides in CdTe layer and in this region the majority of the carrier generation occurs. Typical thickness of the CdTe layer ranges from 2 to 10 μm, depending on the processing methods and desired device structure. The majority of photocurrent generation, however, happens within the first 2 μm of the layer thickness, and above 6 μm little gain for photocurrent can be realized and losses from resistance are expected. Thus, the optimum value for CdTe layer thickness is between 2 and 6 μm [19]. Since CdTe exhibits amphoteric semiconductive behavior, it is possible to easily dope CdTe n and $p-$type [10]. In $n-$type CdS and $p-$type CdTe solar cells, proper carrier concentration and electrical conductivity is achieved though post deposition annealing treatments and doping.

Post deposition annealing treatments have found an important role in CdTe cell manufacturing. Exposure to chlorine-containing species, oxygen, and heat has proved to be critical for cell performance [10]. This processing step is generally referred to as "$CdCl_2$ treatment", or more generally "Cl treatment". Deposition of thin $CdCl_2$ films and subsequent annealing in air or oxygen environments is a common treatment method. Precipitation of $CdCl_2$ thin film can be achieved through dipping cells in $CdCl_2$-based solutions and subsequent drying to form precipitates or through closed space sublimation (CSS) of $CdCl_2$ and subsequent annealing. Other treatment methods include exposure to $CdCl_2$ vapor, to HCl or Cl_2 gas, or to Cl^- ions suspended in solutions used for CdTe growth in chemical bath deposition (CBD) [10]. Depending on prior thermochemical history of the CdTe and CdS layers, the $CdCl_2$ treatment induces benefiting changes on the CdTe cells. First, the treatment can recrystallize the CdTe polycrystalline layer to yield changes in material structure and grain size. Changes in grain sizes are dependent on grain sizes prior to post treatment. Grains tend to grow in size if the starting grain sizes are in the submicron range [10], which are common in low temperature deposition methods. Larger grain sizes and a columnar morphology are desirable for improving cell performance by reducing recombination at the grain boundaries and cell resistance [114]. Cl treatment with oxygen is also responsible for improved electrical improvements, such as decreases in sheet resistance of the CdTe layer [10]. In general the Cl and O treatments are responsible for passivating the deep acceptor states associated with

Cd vacancies by filling Te vacancies with Cl and thus producing a shallower acceptor state with the complex $V_{Cd} + Cl_{Te^-}$ [10]. These shallower acceptor states, i.e. holes, improve the charge carrier concentration of the CdTe layer while eliminating deep electrical traps associated with Cd vacancies.

The back contact, the rear electrode, provides an electrical path to the $p-$type CdTe layer. Formation of an ohmic back contact to CdTe is difficult due to the high work function of CdTe. Ideally, a metal with a higher work function than CdTe is needed, as majority carriers will be traveling from CdTe to the back contact. Since most metals do not have a high work function, holes moving will encounter a significant barrier over which to pass. The height of this barrier, ϕ_{bi}, is given by the following formula:

$$\phi_{bi} = \phi_s - \phi_m \tag{A.18}$$

where ϕ_s and ϕ_m are the work functions of the semiconductor, i.e. CdTe, and the metal contact respectively. Since no suitable metal is available, another approach is needed. One useful method is to create $p+$ layer that has a lower work function then a contacting metal, thus attaining a quasi-ohmic contact. This can be done with Cu or Au. A common way to make this contact is to etch the CdTe layer then evaporate Cu or Au onto this tellurium rich surface to form $p+$ Cu_2Te or Au_2Te interlayer. Cu or Au can also be deposited via a graphite paste or spray, where the graphite also acts as the back contact, or through other processing methods, such as CSS [14, 115]. Subsequent annealing diffuses Cu or Au atoms into CdTe and creates Cu_2Te or Au_2Te interfaces. Cells created using these methods report the best conversion efficiencies [10,112,115]. It is also known that Cu, which is a fast diffuser through CdTe, has been found to cause cell degradation affecting cell stability [115]. One method to correct this is to find another back contact material. Deposition of Sb_2Te_3 buffer layer with a Mo back contact has been shown to provide long term stability with comparable efficiencies to Cu containing back contacts [116].

A schematic of the typical structure made at CSU is shown in Figure A.10.

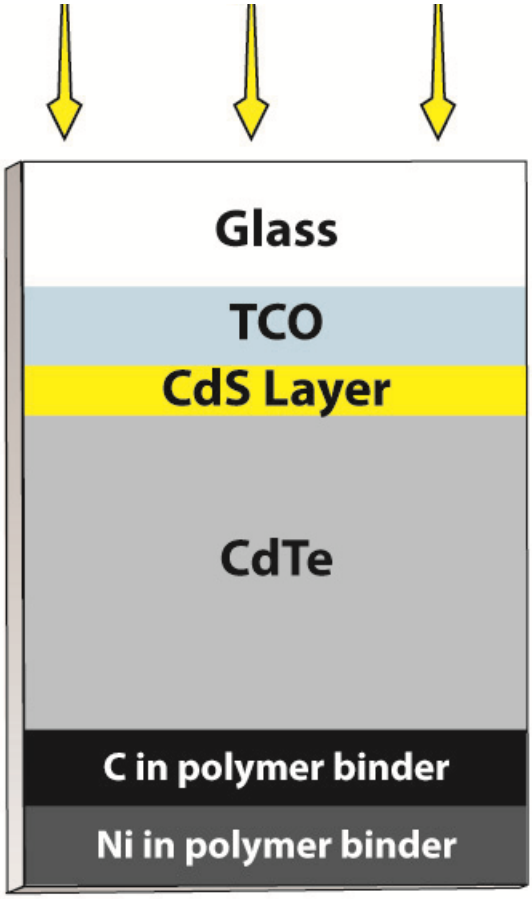

Figure A.10: Typical CdS/CdTe device structure made at CSU

A.4.2 Fabrication of CdS/CdTe Devices at CSU

The primary tool for the fabrication of CdS/CdTe solar cells at the Materials Engineering Laboratory (MEL) at Colorado State University is the Advanced Research and Development System (ARDS). A schematic of the ARDS tool is shown in Figure A.11. The ARDS is a linear cluster tool that is able to deposit the CdS window layer and the CdTe absorber by the heated pocket deposition (HPD) method developed at the MEL previously [14, 80]. The HPD deposition method is similar to close-space sublimation (CSS), but sublimated vapor is confined by a heated crucible to improve the vapor transport to the substrate and uniformity of the deposited thin film.

In addition to depositing CdS and CdTe films, the ARDS includes two stations to perform

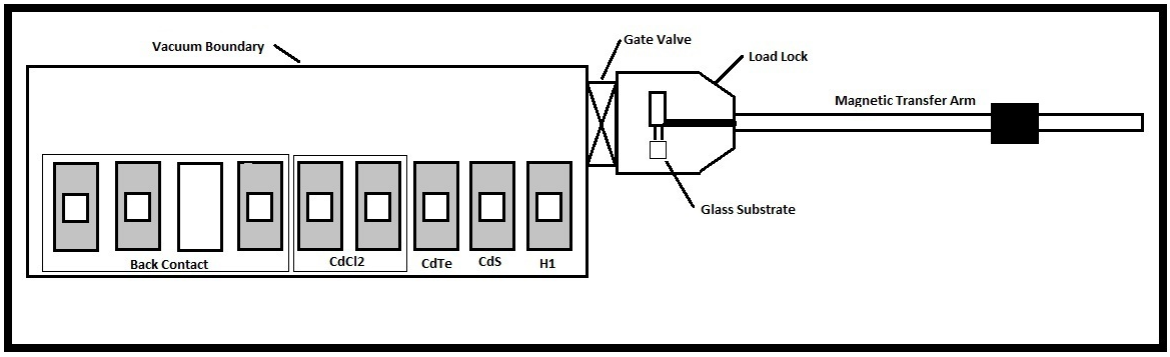

Figure A.11: Schematic of the Advanced Research and Development System (ARDS) at Colorado State University

the necessary $CdCl_2$ treatment for the solar cells. The treatment involved depositing a thin layer of $CdCl_2$ onto the CdTe film and annealing it to incorporate it into the film. The $CdCl_2$ film is deposited by CSS from a powder source.

The ARDS includes additional stations for Cu treatment for back contact formation. A small amount of Cu is deposited by sublimation from a $CuCl_2$ pellet. The films are then annealed to improve the Cu incorporation. This method allows for a small amount of Cu to be incorporated into the film. The low amount of Cu is beneficial for device stability [14].

These deposition and treatment processes are performed at 40 mTorr operating pressure of either N_2 or $2\%O_2$ in N_2. Base pressure in the ARDS is in the 10^{-6} range. The cluster design of the ARDS allows for quick sample generation and process optimization. Furthermore, the flexibility allows easy investigation into novel process sequences, substrates, and material structures. Baseline cells made on Pilkington TEC10 substrates can consistently reach 12.5% efficiency.

Appendix B

Modeling PV Devices

B.1 AFORS-HET Software

AFORS-HET (Automat FOR Simulation of HETero-structures) Version 2.2 [105] is a software package that performs one-dimensional numerical simulation of semiconductor devices. One-dimensional numerical simulation is not only useful but a necessary approach to modeling of photovoltaic devices. Operation of semiconductor devices can be described by coupled partial differential equations for which analytical solutions are generally not possible. One way around this problem is to transform them to non-linear algebraic equations and solve them numerically. AFORS-HET performs numerical calculations modeling of these equation through the bulk of the device. This is done by building a discrete set of gridpoints through the device structure and includes bulk points, interface points, and first and last interface points. For each type of point, the software solves different differential equations and boundary conditions until the calculation converges. This process repeats at each grid point at various settings (e.g. different external bias, etc.). The standard numerical model solves Poisson's equations and electron/hole equation of transport equations at each individual local grid point. Some of these equations are described in more detail below.

Poisson's equation is given by:

$$-\frac{d^2\phi}{dx^2} = \frac{q}{\varepsilon}\left(p + N_D - n - N_A + \sum_{defects} \rho_t\right) \tag{B.1}$$

where ϕ is the electron potential and ρ_t is the charge of defects (trap), which can be either donor-like (n_t) or acceptor-like (p_t).

Steady-state continuity equations are given by:

$$\frac{1}{q}\frac{dJ_p}{dx} = G_p - R_p \tag{B.2}$$

$$-\frac{1}{q}\frac{dJ_n}{dx} = G_n - R_n \tag{B.3}$$

where $G_{p/n}$ is the generation rate of holes/electrons from, for example, optical excitation in photovoltaic semiconductors. The generation rate is dependent on the absorption coefficient of the material at each wavelength and depth in the film, x. $R_{p/n}$ is the recombination rate for holes/electrons and depends on type of recombination, density of mid-gap trap states (for SRH recombination) and defect cross-sections. Continuity equations account for variations in charge carrier density in the devices.

Hole and electron current are given by:

$$J_p = q\mu_p pE - qD_p\frac{dp}{dx} \tag{B.4}$$

$$J_n = q\mu_n nE + qD_n\frac{dn}{dx} \tag{B.5}$$

where $\mu_{p/n}$ is the hole/electron mobility, $D_{p/n}$ is the hole/electron diffusivity. The currents are a sum of drift current (left term) and diffusion current (right term). Mobility and diffusivity are related by the Einstein relation:

$$D_{p/n} = \frac{kT}{q}\mu_{p/n} \tag{B.6}$$

.

Numerically, only the electric potential ϕ, electron density n, and hole density p are needed in the system to solve for other parameters. In AFORS-HET, the ϕ, n, and p are determined at each grid point by solving basic equations. After the model is initialized with appropriate boundary conditions, illumination, temperature, external bias, and other settings can be applied to solve for J-V performance and other device parameters.

SRH recombination velocity (cm/s) of a bulk film, an interface, or a free surface is given by:

$$S_{b/i/s} = N_{b/i/s}\sigma_{p/n}v_t \tag{B.7}$$

where $N_{b/i/s}$ is the bulk, interface, or surface defect density, $\sigma_{p/n}$ is the capture cross-section for holes/electrons, and v_t is thermal velocity of the charge carrier and is considered to be $v_t = 10^7$ cm/s at room temperature.

Carrier lifetime is given by:

$$\tau = \left(\sigma v_t N_{AG/DG}\right)^{-1} \tag{B.8}$$

where $N_{AG/DG}$ is the acceptor or donor mid-gap defect density in the bulk film, or at the surface or interface.

Using the equations above, a detailed AFORS-HET model of the CdS/CdTe PV structure can be built and used for analysis. Specific model parameters are described in the next section.

B.2 Model Parameters

B.2.1 Previous Models

Electron reflector device models presented in Chapter 2 were developed by K.J. Hsiao and are presented in detail in his Ph.D. Thesis [26]. This section is to provide some additional information about those models.

First, Dr. Hsiao made a baseline cell similar to the record efficiency cell at the time. Parameters for this baseline are shown in Table B.1 and are based on independent measurements or are reasonable assumptions. It was assumed donors and acceptors are completely ionized and thus $p = N_A$ and $n = N_D$ and the device had a 10% external optical reflection, 1 ns lifetime, and a 10^{13} carrier lifetime.

Based on the above model, a reasonable baseline cell ($J_{SC} = 24$ mA/cm^2, $V_{OC} = 830$ mV, $FF = 81$ %, $R_s = 1\Omega{\cdot}$cm^2, $G = 0.2$ mS/cm^2, and $\eta = 16\%$) was established. For electron reflector structures, Dr. Hsiao changed the last 200 nm of the absorber to an electron reflector film of higher band gap, establishing a CBO by changing the electron affinity, χ, by the change in band gap. All other parameters of the ER film were assumed to be identical

Table B.1: Parameters of the baseline cell used in previous modeling of ER structures. Index e/h represents electrons/holes, S surface recombination velocity, d thickness, $\varepsilon_0 = 8.8510^{-12}$ F/m electric constant, $N_{DG/AG}$ the donor-like/acceptor-like defect density, W_G the energy width of the Gaussian distribution for the defect states, τ carrier lifetime, and σ capture cross section. Table reproduced from Reference [26].

Contact Interface			
	Front		**Back**
Barrier Height (eV)	0.1 (E_C-E_F)		0.3 (E_F-E_V)
S_e (cm/s)	10^7		10^7
S_h (cm/s)	10^7		10^7
Semiconductor Layer			
	SnO_2 (TCO)	**CdS (n-type)**	**CdTe (p-type)**
d (nm)	500	45	1800
$\varepsilon/\varepsilon_0$	9	10	9.4
E_g (eV)	3.6	2.4	1.5
N_C (cm^{-3})	2.22×10^{18}	2.22×10^{18}	7.8×10^{17}
N_V (cm^{-3})	1.8×10^{19}	1.8×10^{19}	1.8×10^{19}
μ_e (cm^2/Vs)	100	100	320
μ_h (cm^2/Vs)	25	25	40
N_A, N_D (cm^{-3})	$N_D = 10^{17}$	$N_D = 1.1\times10^{18}$	$N_A = 10^{13}$
χ (eV)	4.5	4.5	4.4
Gaussian (Midgap) Defect States			
	SnO_2 (TCO)	**CdS (n-type)**	**CdTe (p-type)**
N_{DG}, N_{AG} (cm^{-3})	D: 10^{15}	A: 10^{18}	D: 9×10^{10}
W_G (eV)	0.1	0.1	0.1
σ_e (cm^2)	10^{-12}	10^{-17}	10^{-9}
σ_h (cm^2)	10^{-15}	10^{-14}	10^{-12}

to CdTe. Figure B.1 shows the band diagram of this model.

B.2.2 Model Set 1

Some of modeling results shown in Section 6.5 were modeled with the parameters listed here. At first, Dr. Hsiao's baseline model was reproduced and an additional electron reflector layer was added. Table B.2 shows the parameters for the TCO, CdS, CdTe, and CMT layers and the front and back contacts. Some modeling experimentation shown in

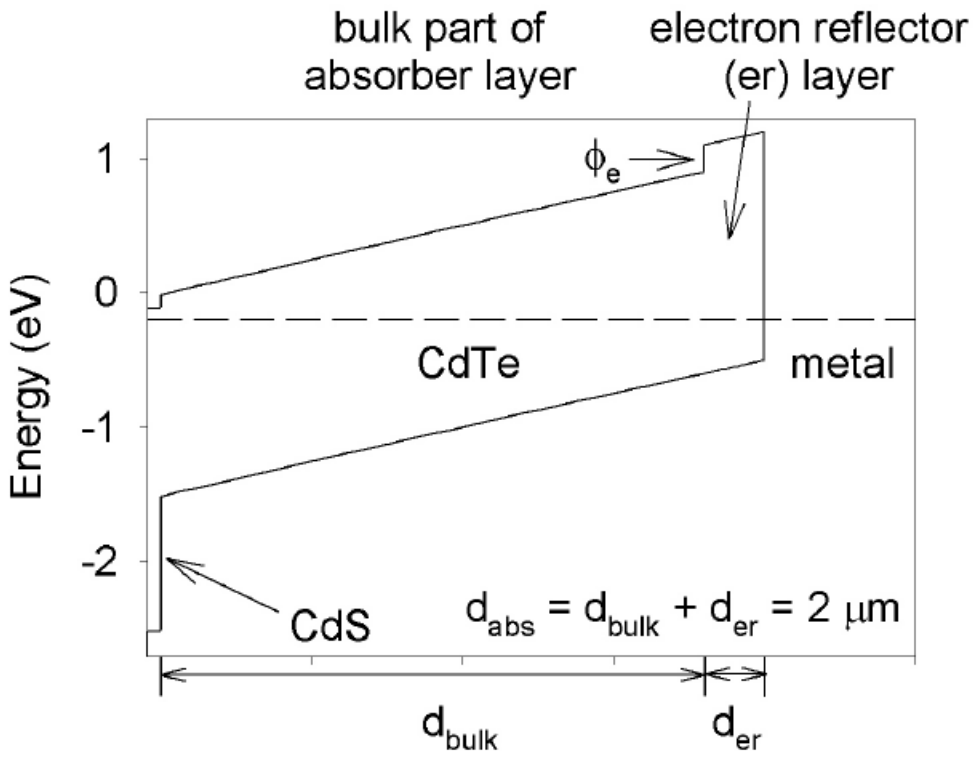

Figure B.1: Band diagram of the previous simulation model for CdS/CdTe/CMT electron reflector structure. Figure reproduced from Reference [26].

Section 6.5 included modeling recombination at the CdTe/CMT interface. Interface recombination was modeled by adding Gaussian mid-gap donor defects with the following parameters: $W_G = 0.15$eV, $\sigma_h = 10^{-12}$cm^2, and $\sigma_e = 10^{-9}$cm^2. Interface defect density was varied per Equation B.7 to obtain the desired recombination velocity.

B.2.3 Model Set 2

Thinning CdTe modeling shown in Section 6.5.5 was performed with the following model parameters. One may notice a change in CdTe and CMT parameters compared to previous model setups. These changes include a raising of the doping density N_A to 10^{14} cm^{-3} and setting $\tau_p = \tau_n = 10$ns. This new baseline is believed to be more in-line with physical measurements of doping density in CdTe solar cells and for carrier lifetimes.

Table B.2: Parameters used in modeling of standard thickness CdS/CdTe/CMT electron reflector cells. Index e/h represents electrons/holes, S surface recombination velocity, d thickness, $\varepsilon_0 = 8.8510^{-12}$ F/m electric constant, $N_{DG/AG}$ the donor-like/acceptor-like defect density, W_G the energy width of the Gaussian distribution for the defect states, τ carrier lifetime, and σ capture cross section.

Contact Interface				
	Front		**Back**	
Barrier Height (eV)	0.1 (E_C-E_F)		0.3 (E_F-E_V)	
S_e (cm/s)	10^7		10^7	
S_h (cm/s)	10^7		10^7	
Semiconductor Layer				
	SnO_x:F (TCO)	**CdS (n-type)**	**CdTe (p-type)**	**CMT (p-type)**
d (nm)	500	45	2,000	200
$\varepsilon/\varepsilon_0$	9	10	9.4	9.4
Eg (eV)	3.6	2.4	1.5	(varies)
N_C (cm^{-3})	$2.22x10^{18}$	$2.22x10^{18}$	$7.8x10^{17}$	$7.8x10^{17}$
N_V (cm^{-3})	$1.8x10^{19}$	$1.8x10^{19}$	$1.8x10^{19}$	$1.8x10^{19}$
μ_e (cm^2/Vs)	100	100	320	320
μ_h (cm^2/Vs)	25	25	40	40
N_A,N_D (cm^{-3})	$N_D = 10^{17}$	$N_D = 1.1x10^{18}$	$N_A = 10^{13}$	$N_A = 10^{13}$
χ (eV)	4.5	4.5	4.4	(varies)
Gaussian (Midgap) Defect States				
	SnO_x:F (TCO)	**CdS (n-type)**	**CdTe (p-type)**	**CMT (p-type)**
N_{DG}, N_{AG} (cm^{-3})	D: 10^{15}	D: 10^{18}	A: $9x10^{10}$	A: $9x10^{10}$
W_G (eV)	0.1	0.1	0.1	0.1
σ_e (cm^2)	10^{-12}	10^{-17}	10^{-9}	10^{-9}
σ_h (cm^2)	10^{-15}	10^{-14}	10^{-12}	10^{-12}

Table B.3: Parameters used in modeling various CdTe thicknesses in CdS/CdTe/CMT electron reflector cells. Index e/h represents electrons/holes, S surface recombination velocity, d thickness, $\varepsilon_0 = 8.8510^{-12}$ F/m electric constant, $N_{DG/AG}$ the donor-like/acceptor-like defect density, W_G the energy width of the Gaussian distribution for the defect states, τ carrier lifetime, and σ capture cross section.

Contact Interface				
	Front		**Back**	
Barrier Height (eV)	0.1 (E_C-E_F)		0.3 (E_F-E_V)	
S_e (cm/s)	10^7		10^7	
S_h (cm/s)	10^7		10^7	
Semiconductor Layer				
	SnO_x:F (TCO)	**CdS (n-type)**	**CdTe (p-type)**	**CMT (p-type)**
d (nm)	500	45	(varies)	130
$\varepsilon/\varepsilon_0$	9	10	9.4	9.4
Eg (eV)	3.6	2.4	1.5	(varies)
N_C (cm^{-3})	$2.22x10^{18}$	$2.22x10^{18}$	$7.8x10^{17}$	$7.8x10^{17}$
N_V (cm^{-3})	$1.8x10^{19}$	$1.8x10^{19}$	$1.8x10^{19}$	$1.8x10^{19}$
μ_e (cm^2/Vs)	100	100	320	320
μ_h (cm^2/Vs)	25	25	40	40
N_A,N_D (cm^{-3})	$N_D = 10^{17}$	$N_D = 1.1x10^{18}$	$N_A = 10^{14}$	$N_A = 10^{14}$
χ (eV)	4.5	4.5	4.4	(varies)
Gaussian (Midgap) Defect States				
	SnO_x:F (TCO)	**CdS (n-type)**	**CdTe (p-type)**	**CMT (p-type)**
N_{DG}, N_{AG} (cm^{-3})	D: 10^{15}	D: 10^{18}	A: 10^{10}	A: 10^{10}
W_G (eV)	0.1	0.1	0.1	0.1
σ_e (cm^2)	10^{-12}	10^{-17}	10^{-9}	10^{-9}
σ_h (cm^2)	10^{-15}	10^{-14}	10^{-9}	10^{-9}