A Clustered Yield Model for SMT Boards and MCM's

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Abstract—**This paper describes a clustered yield model for complex surface mount technology (SMT) assemblies and multichip modules (MCM's). Based on yield modeling techniques that have been proven in the manufacturing of integrated circuits (IC's), this model uses the negative binomial distribution of defects to calculate board yield after test. Manufacturing data validates that this model accurately predicts the clustering of defects and the yield predictions are significantly better than traditional binomial models.**

Index Terms—**Yields, SMT, MCM, board, clustered.**

I. Motivation

SURFACE mount technology assembly yield modeling is an important part of design for manufacturing (DFM) and of design for test (DFT) of electronic products. If the yield can be estimated accurately, the manufacturing cost, the capacity of the manufacturing line, the procurement of material, and the on-time-delivery of the product can be properly managed. On the other hand, if yield predictions are off, the effects will be felt in the manufacturing process and also in the profit margin of the product. An accurate yield model is particularly needed when the product is in the design stage, when trade-offs in DFM and testability can still be made.

Current board yield models are based on a binomial distribution of defects [1]. This approach predicts the yield well for assemblies which are not very complex. However, for complex SMT boards, namely boards for which the average number of defects is greater than 1, the binomial model will underestimate the yield since there is significant clustering of defects in a SMT production line.

II. Description of the Model

This model was developed on the premise that defects on complex SMT boards are clustered. This premise was validated by examining data from production boards at Hewlett-Packard (HP). Predictions of yield based on binomial distribution of defects were underestimating the yield by as much as 10 times.

There has been much work done on modeling of clustered phenomena. Rogers described how the negative binomial distribution can be used to model clustering of retail stores in a given town [2]. Stapper and many others have used the negative binomial distribution to predict yield of large integrated circuits [3], [4]. However, these methods are not directly applicable to SMT assemblies since the fault spectrum of an SMT board is not easily modeled in terms of defect density.

A. Fault Spectrum

An accurate characterization of the fault spectrum is the first step in SMT yield modeling. The fault spectrum is used to estimate the average number of defects per board. For released processes and for components that are already part of inventory, this is a matter of characterizing current products to obtain the failure data. For new assembly processes, custom ASIC and new parts, failure rate goals need to be set and proper plans put in place to ensure that they will be met.

The fault spectrum can be broken into two major parts: the assembly faults caused by the SMT manufacturing process (such as solder opens, solder shorts, misloads, cracked, etc.), and functional faults, which include single component performance faults and multiple component interaction faults. Component performance faults are usually test escapes from the component test. The fault spectrum for the board is derived by estimating the assembly faults on a per solder joint basis and functional faults on a per component basis.

The assembly fault probability model and functional probability model are based on a binomial distribution of defects. Consider a series on n independent trials, each resulting in either a fault or no fault, with fp being the fault probability in any trial. Further assume that fp remains constant from trial to trial. Then defining X as the random variable of the number of faults in n trials, the probability of k faults in n trials has a binomial distribution given by

$$P[X = k;\, n,\, fp] = \frac{n!}{k!(n-k)!}\, fp^k (1 - fp)^{n-k}.$$

In yield modeling, we are interested in the probability of at least one fault, which is one minus the probability of zero faults. To obtain the probability of zero faults in n trials, we set k to zero in the above equation and obtain

$$P[X = 0;] = (1 - fp)^n.$$

Then the probability of at least one fault, Pf, in n trials with fault probability fp is

$$Pf = 1 - (1 - fp)^n.$$

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In practice, it is not easy to obtain the fault probability fp for every component and every type of solder joint. In order to apply this model in the real world of manufacturing, we need to estimate the fault probability fp by defining the average point estimate fault probability $AvgFP$,

$$AvgFP = \frac{NF}{NT}$$

where NF is the number of units that failed a certain test and NT is the total number that participated in that test. In the case of manufacturing data we approximate this average point estimate fault probability with data collected over the manufacturing life of components and solder joints. This data is usually kept in parts per million (PPM).

B. Average Number of Defects per Board

Once the fault spectrum is characterized, one can estimate the average number of defects per board. However, the test coverage has to be included if one is interested in yield after test. The average number of defects per board is analogous to the average number of defects in IC yield calculations.

C. Test Effectiveness

Test effectiveness is defined as the actual detection of faults by the given coverage. As with the fault spectrum, test coverage is estimated for both assembly and functional faults for each test step. Type I errors are modeled by introducing a no trouble found (NTF) defect rate. Type II errors are modeled by derating the estimated coverage by an experimental factor.

D. Clustering Factor

In order to model yield using the negative binomial distribution of defects, a clustering factor has to be estimated. One would expect the clustering factor to remain constant for a given SMT process, as long as the boards have similar complexity. The estimation of the clustering factor needs to be performed experimentally and will vary for different SMT processes.

E. What is Clustered?

In evaluating the manufacturing process of complex SMT assemblies, one determines that not all defects are clustered. Solder defects tend to be clustered, especially for finer pitch components. Functional defects can be adequately modeled with the binomial distribution. Non-solder assembly defects, such as cracked, misloads, reversed polarity, and wrong value component, also can be adequately modeled with the binomial distribution. The overall yield is then obtained by multiplying the clustered and the nonclustered yield.

III. Mathematical Basis for the Model

In order to make the model manageable, the board is divided into categories according to different components. The model calculates the average number of defects by component category. To obtain the overall average number of defects per board, the defects from each component category are summed together. Calculations are done separately for functional faults, clustered assembly defects, and nonclustered assembly defects. The overall yield is the product of the individual yields

$$Y = Ycl * Yncl * Yfct$$

where Y is the overall yield after test, Ycl is the yield from clustered defects, $Yncl$ is the yield from nonclustered defects, and $Yfct$ is the yield from functional defects.

A. Defect Rates

Defect rates are a function of the assembly process and of the individual components [5], [6]. The following defect rates are characterized for a given SMT process and component:

- per joint solder defect rate for each type of joint,
- per component functional defect rate,
- per component assembly workmanship defect rate,
- per component test no-trouble-found defect rate.

The binomial distribution is used to compute the incoming probability of at least one defect per component for solder defects [1]

$$PDs = 1 - [1 - DRjt]^{Njt}$$

where PDs is the probability of at least 1 solder defect, Njt is the number of joints in the component, and $DRjt$ is the solder joint defect rate.

B. Average Number of Defects per Board

The average number of defects per board found after test for each type of yield is computed as follows [1]:

$$D = \sum N * PD * TE$$

where the sum is over all categories, D is the average number of defects per board, N is the number of components per category, PD is the incoming prob of defects, and TE is the test effectiveness per category.

C. Nonclustered Yield

For functional defects and nonsolder assembly defects the binomial distribution of defects was assumed. To calculate the probability of catching x defects, the Poisson approximation of the binomial distribution provides sufficient accuracy because the sample size is large and the defect rate is small for most cases that will be encountered. The Poisson approximation calculates the probability of a test catching x defects per board. Setting λ equal to D, the average number of defects found per board, we have [1]

$$Pd[x, D] = \frac{D^x e^{-D}}{x!}.$$

The nonclustered yield is then obtained when the test catches 0 defects ($x = 0$ in the above formula).

TABLE I
BOARD COMPLEXITY

Board #	# Solder joints	Complexity
1	4239	A
2	6832	A
3	11490	A
4	6202	B

TABLE II
DEFECT DISTRIBUTION PER BOARD

#boards with 0 defects	1000
#boards with 1 defects	300
#boards with 2 defects	150
"	
#boards with >16 defects	2

D. Clustered Yield

The modeling of clustered yield is the innovative aspect of this model. Solder defects make up the majority of SMT defects, and their behavior is very clustered.

In the original research for this model the approach was to look at clustering for each type of solder joint and also clustering in a batch of boards. However, once the data was examined it became clear that the it was sufficient to model clustering for all solder joint types on a per board basis. This simplifies the model significantly, since only one clustering factor needs to be determined.

The solder defects are modeled using the negative binomial distribution given as [3]

$$\text{YIELD} = \left[1 + \frac{\lambda}{a}\right]^{-a}.$$

In IC yield modeling, the average number of defects λ is calculated as the product of the process defect density and the chip area.

SMT processes do not have a defect density number since an assembly is made up of various components with different pitches and different solder joint defect rate. In fact the solderability of a 20 mil SMT part with 250 pins is very different from a 2-pin resistor or a through hole connector. However, an analogous average number of defects per board can be obtained as described in Section IV.B above giving

$$Ycl = \left[1 + \frac{D}{a}\right]^{-a}.$$

IV. MODEL VALIDATION

This model was validated using data from 4 different high volume complex SMT boards at HP. Table I shows the boards used in validation.

In Table I boards with complexity A have through-hole, SMT 50 mil, SMT 25 mil, and SMT 20 mil components; boards with complexity B are like A except that they have no SMT 20 mil components.

A. Alpha Estimation

The value of alpha was estimated based on the distribution of defects per board. Table II shows an example of a board with its distribution of solder defects.

If we let λ be the mean and σ the standard deviation of the data in Table II, the value of alpha can be estimated by [3]

$$a = \frac{\lambda^2}{\sigma^2 - \lambda}.$$

TABLE III
YIELD MODEL RESULTS

Board #	Actual Yield	Binomial Yield	Clustered Yield
1	***a***	50.05% of ***a***	98.03% of ***a***
2	***b***	44.24% of ***b***	105.26% of ***b***
3	***c***	9.68% of ***c***	98.03% of ***c***
4	***d***	31.84% of ***d***	64.93% of ***d***

In investigating 4 boards from HP's manufacturing line, Boards 1 and 3 (Table I) were used to estimate the clustering factor. It was found that an average α range of 0.35–0.45 should be used for the given process.

B. Yield Calculation

The model was used to predict yield for all 4 boards. In the following results variables are used in place of actual yields since we are interested in reporting model accuracy not data from a given SMT process. Table III gives the yield modeling results. Actual yield is the measured yield in the manufacturing line for a 4 month period. Binomial yield is the yield calculated by assuming Poisson distribution for all defects [1]. Clustered yield is the yield calculated with the model described in this paper. In Table III, 105.26% of ***b***, means the value of the actual yield ***b***, plus 5.26% of the value ***b***.

The values for the clustered model above were obtained with $\alpha = 0.4$. In the range 0.35–0.45, all yields except board 4 are predicted correctly by the clustered model.

Boards 1, 2, and 3 span the typical yield spectrum for the SMT process used because of their difference in number of solder joints. However, they are similar in complexity and density. It is very encouraging that the clustering was predictable across this variety of yields. Board 3 is the largest board, with the largest average number of defects per board. As one would expect, the binomial model significantly underestimates the yield, where the clustered model excels.

Board 4 is less dense and less complex than the other 3, thus its defect rates were lower and the clustering factor smaller. Although in practice one would need to scale defect rates and clustering factor based on complexity, it is encouraging that the cluster modeled predicted a yield two times closer to the actual yield than the binomial model.

V. CONCLUSION

This paper described a clustered model to predict yield of complex SMT boards. The major goal of this work was to develop a yield model which will better predict yield of new designs so that as new products are developed the

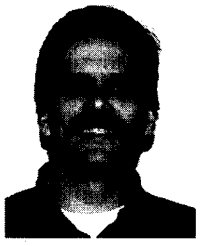
manufacturing ramp can be properly managed. The model uses the negative binomial distribution to predict the clustering of solder defects and Poisson distribution to model functional defects and nonsoldered assembly defects The average number of defects per board is obtained from defect rate goals and the test effectiveness used.

Validation of the model with data from the HP manufacturing line shows that the clustering effect is properly modeled and the yield predictions are excellent for a varied yield spectrum of boards of similar solder joint mix. The model is clearly superior to the binomial models currently used.

The cluster parameter will vary for different SMT processes. The characterization of the defect rates is also a necessary step which requires great discipline and process control. If the SMT assemblies are not very complex, binomial modeling will be sufficient, but for the highly complex boards with average number of defects greater than 1 clustering is going to be a dominant factor in yield predictions.

REFERENCES

[1] M. V. Tegethoff *et al.*, "Board test DFT model for computer products," in *Proc. Inte. Test Conf.*, 1992, pp. 367–371.
[2] A. Rogers, *Statistical Analysis of Spatial Dispersion.* London, UK; Pion Limited, 1974.
[3] J. A. Cunningham, "The use and evaluation of yield models in integrated circuits manufacturing," *IEEE Trans. Semiconduct. Manufact.*, vol. 3, no. 2, pp. 60–71, May 1990.
[4] C. H. Stapper *et al.*, "Integrated circuit yield statistics," *Proc. IEEE*, vol. 71, no. 4, pp. 453–470, Apr. 1983.
[5] G. Nobel and J. Gleason, "Tolerance issues in SMT assembly," in *Proc. Surface Mount Int.*, 1991, pp. 266–273.
[6] E. O. Schlotzhauer and R. J. Balzer, "Real-world board test effectiveness: What does it mean when the board passes?" in *Proc. Int. Test Conf.*, 1987, pp. 792–797.



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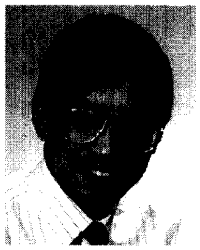

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