DISSERTATION

GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS IN CHIP SCALE PACKAGING: EVALUATION OF PERFORMANCE IN RADIO FREQUENCY POWER AMPLIFIERS AND THERMOMECHANICAL RELIABILITY CHARACTERIZATION

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ABSTRACT

GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS IN CHIP SCALE PACKAGING: EVALUATION OF PERFORMANCE IN RADIO FREQUENCY POWER AMPLIFIERS AND THERMOMECHANICAL RELIABILITY CHARACTERIZATION

Wide bandgap semiconductors such as Gallium Nitride (GaN) have many advantages over their Si counterparts, such as a higher energy bandgap, critical electric field, and saturated electron drift velocity. These parameters translate into devices which operate at higher frequency, voltage, and efficiency than comparable Si devices, and have been utilized in varying degrees for power amplification purposes at >1 MHz for years. Previously, these devices required costly substrates such as sapphire (Al_2O_3), limiting applications to little more than aerospace and military. Furthermore, the typical breakdown voltage ratings of these parts have historically been below ~200 V, with many targeted as replacements for 50 V Si LDMOS as used in cellular infrastructure and industrial, scientific, and medical (ISM) applications between 1 MHz and 1 GHz. Fortunately within the past five years, devices have become commercially available with attractive key specifications: GaN on Si subtrates, with breakdown voltages of over 600 V, realized in cost effective chip scale packages, and with inherently low parasitic capacitances and inductances.

In this work, two types of inexpensive commercially available AlGaN/GaN high electron mobility transistors (HEMTs) in chip scale packages are evaluated in a set of three interconnected experiments. The first explores the feasibility of creating a radio frequency power amplifier for use in the ISM bands of 2 MHz and 13.56 MHz, at power levels of up to 1 kW, using a Class E topology. Experiments confirm that a DC to RF efficiency of 94% is easily achievable using these

devices. The second group of experiments considers both the steady state and transient thermal characterization of the HEMTs when installed in a typical industrial application. It is shown that both types of devices have acceptable steady state thermal resistance performance; approximately 5.27 °C/W and 0.93 °C/W are achievable for the source pad (bottom) cooled and top thermal pad cooled device types, respectively. Transient thermal behavior was found to exceed industry recommended maximum dT/dt by over 80x for the bottom cooled devices; a factor of 20x was noted with the top cooled devices. Extrapolations using the lumped capacitance method for transient conduction support even higher initial channel dT/dt rates. Although this rate of change decays to recommended levels within one second, it was hypothesized that the accumulated mechanical strain on the HEMTs would cause early life failures if left uncontrolled. The third set of experiments uses the thermal data to design a set of experiments with the goal of quantifying the cycles to failure under power cycling. It is confirmed that to achieve a high number of thermal cycles to failure as required in high reliability industrial systems, the devices under test require significant thermal parameter derating to levels on the order of 50%.

ACKNOWLEDGEMENTS

If the heavens were all parchment, and the trees of the forest all pens, and every human being were a scribe, it would still be impossible to record all that I have learned from my teachers.

– Yochanan ben Zakkai, c. 75

The author wishes to acknowledge the individuals and groups who assisted him in producing this work.

I would like to recognize my parents, James and Janice, who instilled in me at a very early age the importance of an inquisitive nature and a good education. For this, I owe an eternal debt of gratitude.

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Finally I would also like to acknowledge the support of Advanced Energy Industries for providing a research oriented and challenging workplace at which works such as this can be conceived and developed. I have been fortunate to have the support of mentors both pragmatic and pedagogic, who have pushed me to achieve, and my level of appreciation for their enthusiasm on my behalf is high.

DEDICATION

My advice to you is get married: if you find a good wife you will be happy; if not, you will become a philosopher. – Socrates, c. 405 B.C.

Anyone who has undertaken a degree program while employed, with a working spouse and young children, knows that family support is paramount. To this end, first and foremost, I dedicate this work to my wife Cheryl. Her patience and support were instrumental in a great many ways. My daughter Maya and son Maxwell have provided numerous well-needed breaks, whether it be to watch birds, construct a Lego vehicle, listen to Bob Marley, or go sledding. It is my hope that seeing me work hard, over a protracted duration, overcoming obstacles and being repeatedly humbled in the process for something I wanted, motivates you to persevere and succeed in your own endeavors. Never take your eyes off the prize!

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CHAPTER 1 - INTRODUCTION

1.1 Technological background

Research on the topic of wide bandgap semiconductors is not a recent phenomenon. Scientists and engineers looking to exploit the benefits available have been eagerly pursuing GaAs, SiC, and GaN for power conversion for decades, and the rationale is simple: the basic material properties favorable as compared to those of Si. For reference, Table 1.1 illustrates the key parameters. Compared to Si, GaN offers an improvement in all measures. The bandgap, defined as the difference between the top of the valence band and bottom of the conduction band, is a region in which no electron states can exist, and what makes a material insulating, conducting, or semiconducting. When used as a semiconductor, the bandgap partially defines the breakdown voltage and the maximum operating temperature. Electron mobility is the speed at which an electron moves through a material and influences the ON-state resistance of a device. The electric field at which electrons break through a semiconductor is the critical field, which determines the breakdown voltage and leakage current in a transistor, MOSFET, or HEMT. The saturated carrier velocity is a measure of the speed which a particle attains as it traverses a material. Above this point, further increases in the applied electric field produce no additional carrier velocity. Finally, the thermal conductivity can be defined as the quantity of heat transmitted through a material due to a temperature gradient. This parameter strongly determines the amount of heat which can be removed from an active device and the resultant power density which is practical in an application.

Table 1.1 - Comparison of semiconductor material properties.

	Bandgap (eV)	Electron Mobility (cm^2/Vsec)	Critical Field (10^5 V/cm)	Saturated Electron Drift Velocity (10^7 cm/sec)	Thermal Conductivity (W/cmK)
Si	1.1	1450	2	1.1	1.5
SiC	3.26	900	30	2	4.9
GaAs	1.4	8500	4	2	0.5
GaN	**3.2**	2000	**30**	**2.5**	2

As illustrated in Figure 1.1, using a figure of merit (*Breakdown Voltage x* $R_{DS,ON}$), the performance limits of GaN are enhanced by on the order of 3.5 orders of magnitude. Si superjunction devices, which are alternately stacked layers of heavily doped n- and p-type layers, are notably absent in this plot; their figure of merit performance is roughly halfway between the material limit of Si and SiC. The net result is devices which are physically smaller, have lower ON-state resistance, and higher breakdown voltages.

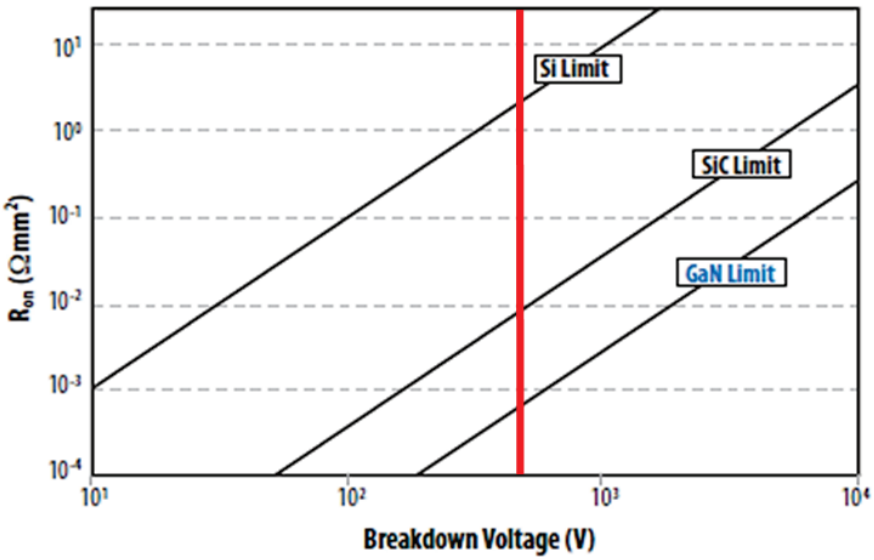


Figure 1.1 - Material performance limits of Si, SiC, and GaN, from [1].

A typical AlGaN/GaN on Si HEMT is shown in Figure 1.2. The spontaneous formation of a two-dimensional electron gas (2DEG) at the AlGaN/GaN interface is a critical phenomenon in the operational performance of the device. The interfacial confinement of electrons forms a sheet charge, which is caused by spontaneous and piezoelectric polarizations of the GaN channel and the AlGaN barrier. This causes high sheet carrier concentrations and strong confinement at this interface [2]–[5]. The presence of the 2DEG yields a very high carrier concentration (~ 2 x 10^{13} cm^{-2}) and hence mobility (~ 3 x 10^{3} $cm^2/V{\cdot}s$ at 25 °C, with approximately $T^{-1.8}$ temperature dependence) resulting in lower $R_{DS,ON}$ and extended maximum operational frequency in AlGaN/GaN HEMTs [6]–[10].

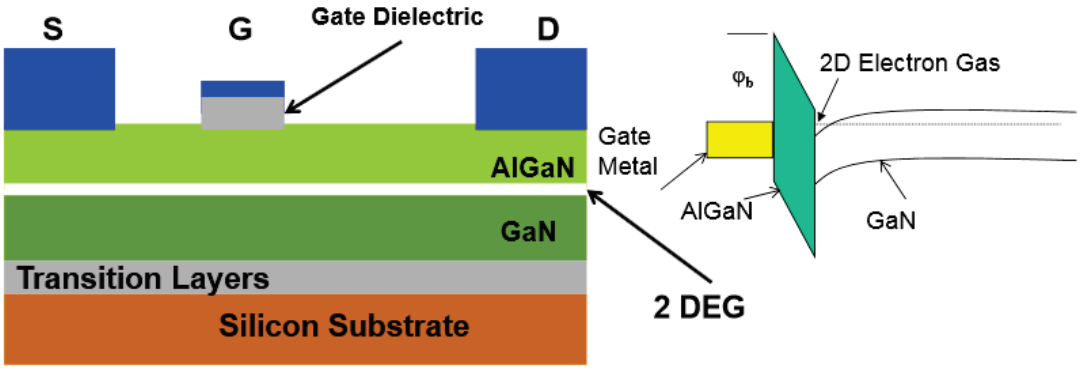


Figure 1.2 - Typical structure of an AlGaN/GaN HEMT, from [11].

Regarding the structure of available GaN HEMTs, performance requirements have previously required costly substrates such as sapphire (Al_2O_3), limiting the applications to little more than aerospace and military. Although associated costs have been lowered through the use of novel techniques such as the heat exchanger method for sapphire growth [12], there are complications in processing which manifest as bowing and cracking of the substrate [13]. Cost

improvements continue to be realized through the use of Si substrates, even when considering use of the non-standard (111) plane [14].

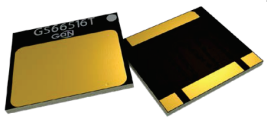
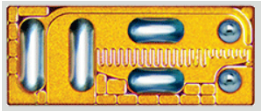
The infrastructure of the semiconductor manufacturing industry has been set up for inexpensive and rapid development of Si devices; the overwhelming majority of devices and integrated circuits available today are based on Si for this reason. Nonetheless, the interest in wide bandgap materials has continued and within the past decade, SiC and GaN in particular have been designed into products and applications ranging from milliwatt radio frequency transmitters to megawatt renewable energy inverters, from integrated lighting solutions to grid-tied power storage [15]–[25].

1.2 Description of research

GaN has been utilized in varying degrees for power amplification purposes at > 1 MHz for years. However, commercially available parts which are used to this end are relatively expensive, restricting use to applications where cost is not a primary driving factor. Additionally, the specified voltage standoff ratings of these devices historically been below ~ 200 V. The target replacement of these HEMTs has been ruggedized 50 V Si LDMOS as used in cellular infrastructure and industrial, scientific, and medical (ISM) applications between 1 MHz and 1 GHz. Examples of Si parts are the BLF and MRF series, as produced by Freescale Semiconductor, and the ST Microelectronics SD series [26], [27]. A higher DC bus voltage is desirable, as the DC subsystem feeding the power amplifier can be realized in a physically smaller form factor while being less expensive. GaN HEMTs with a blocking voltage on the order of 600 V have recently become available off the shelf from multiple suppliers, including Panasonic, International Rectifier, Transphorm, and GaN Systems, some of which are illustrated in Table 1.2. These devices have

improved electrical characteristics when compared to their Si counterparts. Most high voltage HEMTs are packaged in industry standard form factors such as the TO-247 but for high frequency operation, a low inductance package such as a chip scale package variant are preferred. Engineers looking to exploit the benefits of wide bandgap semiconductor devices, particularly the III-V group including GaN, have many more options than existed just five years ago. Commercial off the shelf (COTS) devices capable of switching anywhere from watts to kilowatts are available with improved static (lower $R_{DS,ON}$) and dynamic (lower C_{ISS}) parameters than their silicon counterparts. These benefits enable applications to be more energy and volumetrically efficient.

Table 1.2 - Example of GaN devices available.

				
Size	Medium	Small	Very small	Medium
Form factor	TO-220 / TO-247	Chip Scale Package	Chip Scale Package	Standard RF flanged package
Target application	DC-DC conversion	DC-DC conversion RF amplification up to 100 MHz	DC-DC conversion RF amplification up to few GHz	RF amplification up to 10's of GHz
Replaces	Si FETs IGBTs	Si FETs	Si FETS GaAs FETs	GaAs FETs
$R_{DS,ON}$ (mΩ)	150	27	100	2,000
Q_G (nC)	6	5	0.4	1
Cost	Medium	Low-medium	Low	High

Naturally with any new technology there are open questions to be addressed. GaN HEMTs have had historical reliability challenges. These problems have been attributed to inherent device characteristics and design constraints [28]–[46], high voltage stress [47]–[50], and those specific

to RF operation [51]–[55]. The degradation physics have also been documented by some authors [56]–[67]. Many have been characterized and remedied in modern devices, and the manufacturers have extensive knowledge regarding how to mitigate the risk of early life device failure. But many COTS devices are using CSP or other surface mount packaging styles, which lowers cost and realizes further improvements for high speed switching and high frequency amplification due to very low inductances. Again, the CSP / SMD trend is not without unanswered questions and design tradeoffs; the device physics reliability challenges are being surpassed by more traditional back end of line (BEOL) packaging reliability concerns, involving solder joint fatigue, power dissipation density, and thermal strain related failures. Fortunately, the associated failure modes have been understood for decades with Si devices.

1.3 Organization of dissertation

This dissertation explores these topics specifically as they relate to AlGaN/GaN on Si HEMTs in chip scale packaging. Chapter 2 presents the concept, design, and experimental results of using these devices in radio frequency power amplifiers using a Class E topology. ISM frequencies of 2 MHz and 13.56 MHz are considered, at power levels of up to 1 kW. In Chapter 3, the two types of devices are installed in typical systems and evaluated in the transient and steady state thermal domains. Chapter 4 presents the results of a set of experiments which quantify the cycles to failure under power cycling. Finally, Chapter 5 summarizes the current work and speculates on potential future work on this topic.

CHAPTER 2 – DESIGN AND VERIFICATION OF RADIO FREQUENCY POWER AMPLIFIERS

2.1 Basic RF Power Amplifier Topologies

An initial consideration for the design of an RF power amplifier is the topology, or more specifically, the mode of operation of the active device(s). Naturally there are tradeoffs involved in the selection of one class versus another, so the designer must balance parameters such as design complexity, efficiency, and physical size, some of which are mutually exclusive. A summary of basic design considerations when choosing an operating mode are shown in Table 2.1.

A topology for illustrating Class A, B, and C is shown in Figure 2.1. The most linear and low distortion amplifier is achieved through Class A, where the active device acts as an ideal voltage-controlled current source. The device conducts over the entire range of the input signal cycle and hence there is always dissipation due to the bias current, even when there is no input signal. Amplifiers biased for B operation also operate the active device as a current source, but the bias is arranged to shut off the output device half of every cycle. Class C amplifiers are unique in the sense that while the active device is operated as a current source, a resonant circuit is needed to ensure a sinusoidal load current. The bias in this configuration is such that the device conducts less than half of every cycle. Therefore, the input signal consists of a pulse train. While amplifiers using Class A, B, or C are generally simpler to design, there are two key drawbacks. The first disadvantage is that the output amplitude is limited to $V_{DC}/2$, where V_{DC} is the drain supply voltage. Secondly, the only way to improve efficiency is to control current. Current source amplifiers require a large ON state current to deliver power, which due to device biasing remains large even in the OFF state.

Table 2.1 – Summary of Amplifier Operating Mode Considerations.

Class	**Linear operation?**	**Active device mode**	**Number of devices**	**Output network complexity**	**Efficiency**	**Size**	**Cost**
A	Yes	Current source	1	None	50%	Large	Very high
B	Yes	Current source	2	None	78.5%	Moderate	High
C	No	Current source	1	Low	90%	Moderate	Moderate
D	No	Switch	2	Low	100%	Small	Low
E	No	Switch	1	Moderate	100%	Small	Low
F	No	Switch	1	High	100%	Small	Low

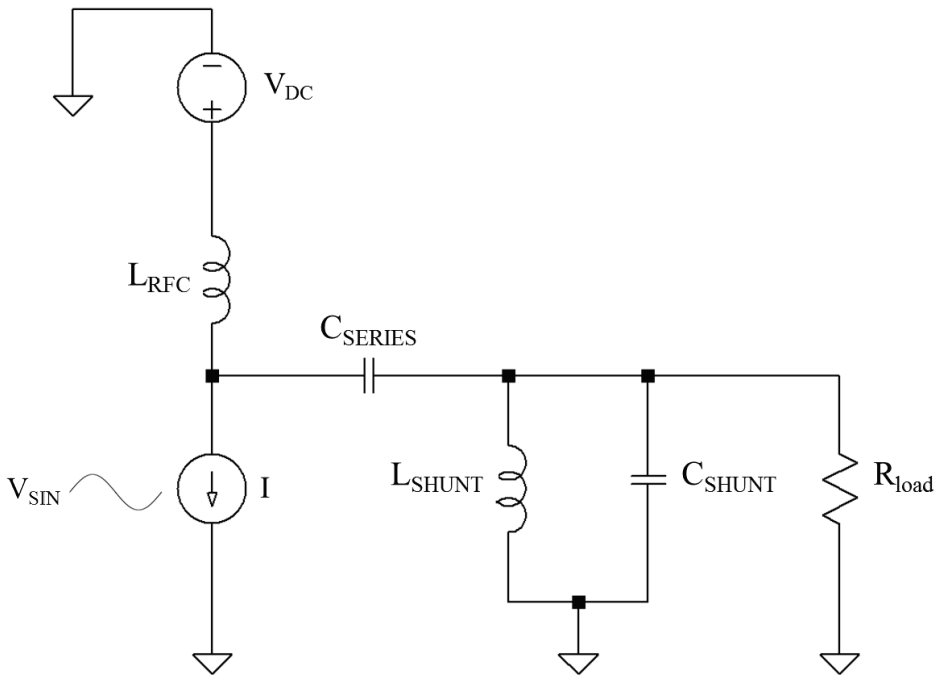


Figure 2.1 – Basic topology for Class A, B, and C amplifiers.

The other classes shown in Table 2.1 are inherently nonlinear. In Classes D, E, and F, the active device(s) are operated as ON/OFF switches. In the ideal cases, the efficiency is 100%, as a perfect switch in the ON state would both conduct all current with no voltage across it and in the OFF state would have the full drain voltage across it but with zero current flowing. Class D amplifiers utilize two devices stacked in series between the supply voltage and ground, and can be configured as current-mode or voltage-mode, the latter of which is illustrated in Figure 2.2. The input is configured to switch only one device ON at a time, which can be achieved through transformers, complementary n- and p-type devices, and specialized gate drive ICs for example.

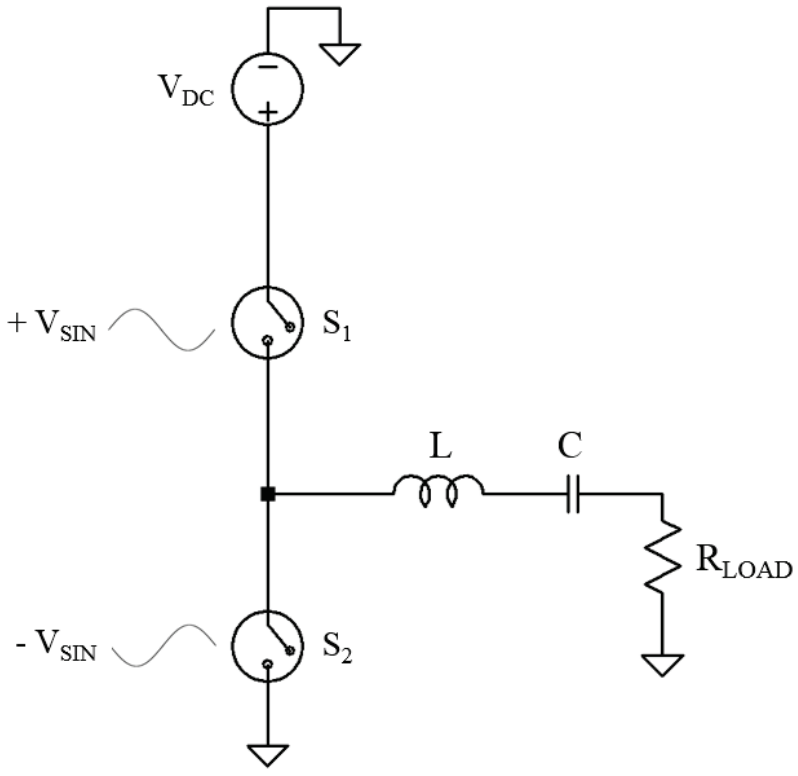


Figure 2.2 – Basic topology for Class D amplifiers.

Class E amplifiers most commonly utilize a single ground referenced active device, as shown in Figure 2.3. The Class E topology uses a tuned passive network to shape the switch voltage such that it has both zero value and slope at turn on, reducing switch losses. The Class F topology, presented in Figure 2.4, incorporates harmonic peaking to closer approximate a square wave switching signal, at the expense of a more complicated load network. This is achieved through tuning even harmonics to short circuits and allowing odd harmonics into the voltage waveform. In practice, it can be difficult to control more than 7th harmonic.

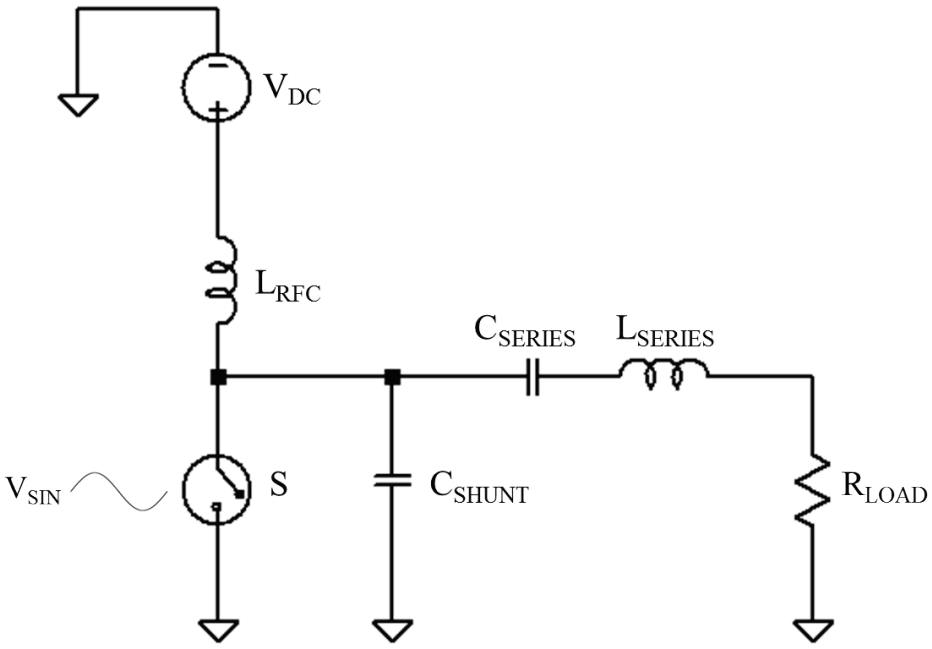


Figure 2.3 – Basic topology for Class E amplifiers.

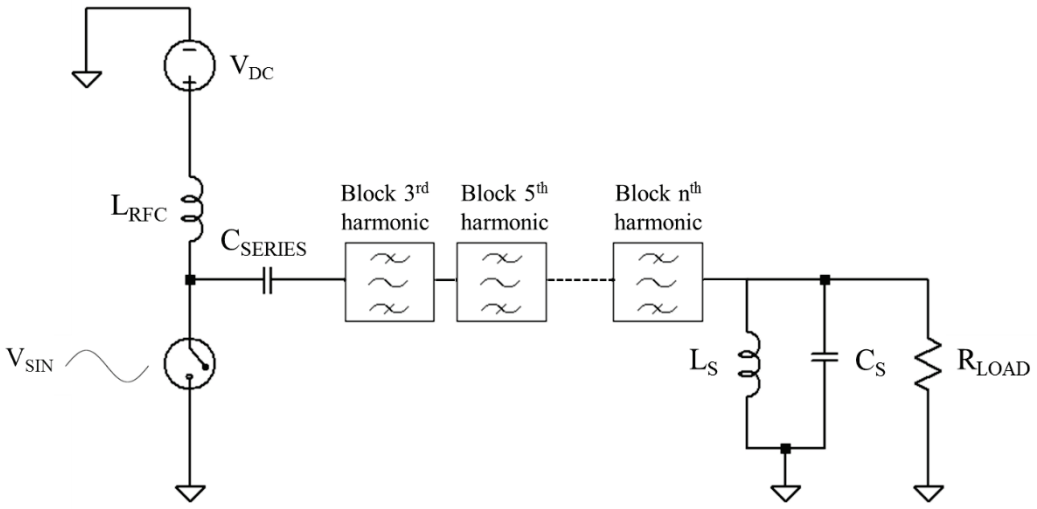


Figure 2.4 – Basic topology for Class F amplifiers.

2.2 Efficiency of Switched Power Supplies and Power Amplifiers

High efficiency is especially relevant with battery powered systems, but for broadcast and industrial RF power systems, poor efficiency results in costly heatsinking strategies, larger physical size, and higher electrical utility costs. Increased efficiency for a given amplifier power output also increases reliability, as device junction temperatures are lower, resulting in higher mean times to failure (MTTF) for temperature accelerated failure mechanisms.

The active device loss mechanisms in a switch mode power supply or switching amplifier decrease the overall efficiency of the system and are comprised of static and dynamic losses, which are summed:

$$P_{loss} = P_{conduction} + P_{switching} + \left(P_{body}\ \mathbf{OR}\ P_{Schottky}\right) \tag{2.1}$$

where

$$P_{conduction} = I_D{}^2 R_{DS,ON} D \tag{2.2}$$

$$P_{switching} = \left(\frac{1}{2} V_{DS} I_D\right)(t_{ON} + t_{OFF}) f_{SW} + \left(\frac{1}{2} C_{OSS} V_{DS}^2 f_{SW}\right) \tag{2.3}$$

$$P_{body} = Q_{RR} V_{DS} f_{SW} \tag{2.4}$$

$$P_{Schottky} = \left(\frac{1}{2} C_{Schottky} V_{DS}^2 f_{SW}\right) \tag{2.5}$$

and $R_{DS,ON}$ is the *ON* resistance of the device, D is the converter duty cycle, t_{ON} and t_{OFF} are the durations of the switch *ON* and *OFF* transition times, f_{SW} is the switching frequency, C_{OSS} is the switching device output capacitance, Q_{RR} is the reverse recovery charge of the body diode (for the case of no external Schottky diode), and $C_{Schottky}$ is the capacitance of an external Schottky diode (if utilized). The body diode and Schottky terms are only relevant for inverter and rectifier cases, and are illustrated here for completeness. There are two noteworthy observations: (1) switching and diode losses are directly proportional to switching frequency and (2) reducing the switch transition time produces a reduction in switching losses.

The three parameters of interest which are characteristic of the device being utilized are $R_{DS,ON}$, $C_{OSS,}$ and t_{RR}. $R_{DS,ON}$ is largely a function of the device die size; a physically larger die has higher resistance due to the increased amount of semiconductor material. For Si MOSFETs, $R_{DS,ON}$ is also a nonlinear function of the die temperature and can be estimated by [68]

$$R_{DS,ON}(T) = R_{DS,ON}(25\ ^\circ C)\left(\frac{T}{300}\right)^{2.3} \tag{2.6}$$

Switching losses in a transistor, MOSFET, or HEMT are partially dependent on the device capacitances. A larger capacitance requires more time to charge, resulting in longer switch

transition times and power dissipation. Through parasitics, the gate-drain capacitance (C_{GD}) negatively affects the switching speed in a nonlinear way, and is dependent on voltage; the related charge and voltage relationship is referred to as the Miller effect. Although it is dependent on the exact devices, at higher frequencies, C_{OSS} becomes the predominant loss mechanism. It is therefore beneficial for a switching amplifier to employ devices with the lowest possible C_{OSS}.

Silicon MOSFETs have a parasitic bipolar junction from the source to drain terminals referred to as the "body diode." Reverse drain current cannot be blocked because the body is connected to the source. This intrinsic diode generally switches much slower than the MOSFET. In a bridge topology, switching dead-time (both high- and low-side OFF) or fast recovery / Schottky diodes must be incorporated to prevent cross conduction and failure. The body diode contributes to losses in MOSFET switching amplifiers due to the reverse recovery current flowing through the body diode. A device which minimizes the body diode reverse recovery current also minimizes this loss mechanism.

These descriptions of device capacitances and parasitic bipolar junctions are relevant in the context of recently available GaN devices, specifically HEMTs with very low C_{OSS} (< 20 pF), low $R_{DS,ON}$ (< 0.1 mΩ), and by virtue the HEMT design itself, no Q_{RR} / t_{RR}. It follows that a highly efficient, high frequency switched amplifier could be devised utilizing such devices.

2.3 Details of Class E Design

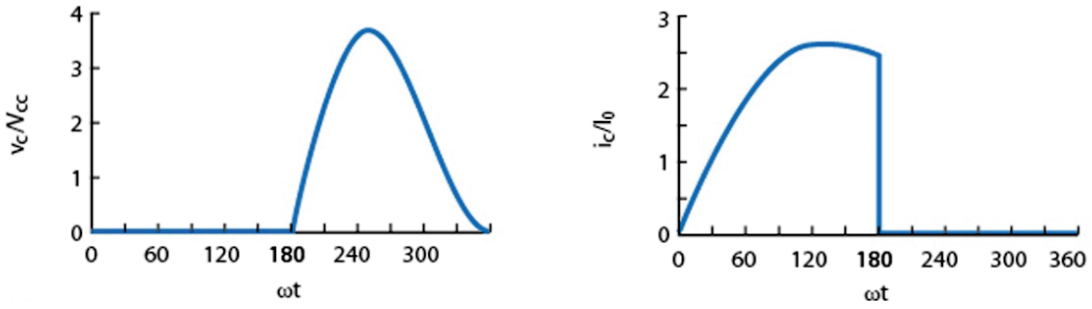
As previously mentioned, the well-known Class E topology [69] is illustrated in Figure 2.3. The switching device is ground referenced. The component C_{SHUNT} is an additional capacitance added between the drain and source terminals of the switching device to ensure that during device turn off, the drain to source voltage remains low. The resonant elements C_{SERIES} and L_{SERIES} comprise a tuned circuit which ideally provide zero voltage and zero current switching. L_{RFC} is a choke sized to deliver a sufficiently constant current source from the DC rail, V_{DC}; the exact value does not affect the power amplifier operation. Determining the resonant component values requires simultaneous mathematical conditions; the resultant parameters are

$$R_{LOAD} = \frac{(V_{DD} - V_{DS})^2}{P}\left(\frac{2}{\frac{\pi^2}{4}+1}\right) \tag{2.7}$$

$$C_{SHUNT} = 1/2\pi f\, R_{LOAD}\left(\frac{\pi^2}{4}+1\right)\left(\frac{\pi}{2}\right) \tag{2.8}$$

$$C_{SERIES} \approx \left(\frac{1}{(2\pi f)^2 L_{SERIES}}\right)\left(1+\frac{1.42}{Q_L-2.08}\right) = C_{SHUNT}\left(\frac{5.447}{Q_L}\right)\left(1+\frac{1.42}{Q_L-2.08}\right) \tag{2.9}$$

The derivations for 2.7 – 2.9 can be found in [69]. The quality factor Q_L of the tuned elements represents a tradeoff between low harmonic content delivered to the load, efficiency, and filter complexity. It is possible to ensure turn on/off conditions $V = 0$ and $dV/dt = 0$ across a ~ 1.6:1 frequency band with single tuned element values. The ideal drain voltage and current waveforms for the Class E operation are shown in Figure 2.5.



(a) (b)

Figure 2.5 - Illustrative (a) drain voltage and (b) drain current waveforms for Class E operation.

Lossless operation requires optimum conditions immediately preceding the switch-ON state, at the moment t=2π and the device is saturated, such that

$$v_{DS}(\omega t)|_{\omega t=2\pi} = 0 \tag{2.10}$$

and

$$\left.\frac{dv_{DS}(\omega t)}{d\omega t}\right|_{\omega t=2\pi} = 0. \tag{2.11}$$

The current through the switch can be expressed as

$$i(\omega t) = I_{R_{LOAD}}[\sin(\omega t + \varphi) - \sin(\varphi)] \tag{2.12}$$

where ω is the angular frequency and φ is the initial phase shift. The voltage across the switch is then written as

$$v(\omega t) = \frac{1}{\omega C_{SHUNT}} \int_{\pi}^{\omega t} i_{C_{SHUNT}} d\omega t \tag{2.13}$$

In a Class E amplifier, applying 2.12 and 2.13, the phase angle φ can be calculated as

$$\varphi = tan^{-1}\left(-\frac{2}{\pi}\right) = -32.482°. \tag{2.14}$$

The equations can be manipulated through trigonometric identities and some algebra to produce

$$I_{DC} = 0.577\frac{V_{DD}}{R_{LOAD}} \tag{2.15}$$

and

$$V_{D,peak} = -2\pi\varphi V_{DD} = 3.562V_{DD} \tag{2.16}$$

both of which are useful in determining steady state operating parameters and aiding in device selection.

The details of the output filter type and design are generally permissive, although minimizing intermodulation distortion requires a maximally flat response. This is achieved through correctly choosing the low-pass filter parameters in line with those for a Butterworth type network, calculated by

$$L = 0.7\frac{R_{load}}{\pi f_c} \tag{2.17}$$

and

$$C = \frac{1}{2.8\pi f_c R_{load}} \tag{2.18}$$

where f_c is the cutoff frequency [70].

The GS66504B and GS66516T from GaN Systems, as used in this work, are both rated at 650 V drain to source voltage [71], [72, p. 66]. The GS66504B is specified at 15 A continuous drain current, with the GS66516T at 60 A. The inherent properties of the AlGaN/GaN on Si construction yield devices with low input capacitance (C_{ISS} = 130 pF for GS66504B and 525 pF for GS66156T) and low on-state resistance ($R_{DS,ON}$ = 110 mΩ for GS66504B and 27 mΩ for GS66516T). The device packaging has also been designed with very low internal inductances. These traits enable a switching amplifier with dynamic losses which are favorably low compared with their traditional Si based counterparts, as noted by other authors in the Class E topology [73], [74] and the Φ_2 topology [75], [76] amongst others.

2.4 Gate Drive Design for 2 MHz Power Amplifier

The first power amplifier for consideration was designed around the GS66504B. 2 MHz was chosen as the operating frequency due to its common use in industrial applications, specifically semiconductor processing. Based on simple calculations, it was also found that a 2 MHz amplifier could be constructed without resorting to complicated gate drive techniques. A gate drive IC was utilized, specifically the IXYS / Clare IXD609. A simplified block diagram of this part is shown in Figure 2.6. Relevant specifications include 9 A peak source / sink drive current, a wide operating range of 4.5 V to 35 V, and matched rise and fall times of approximately 10 ns. The leaded SOIC8 package was chosen to enable manual rework and modifications as necessary.

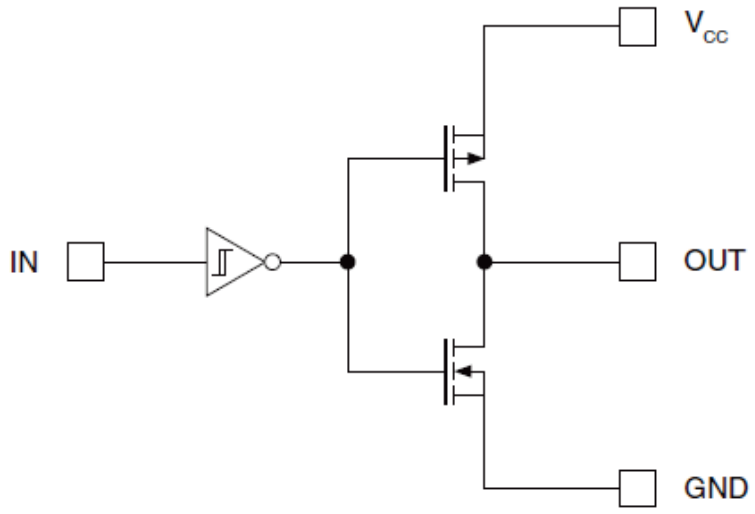


Figure 2.6 – Topology of gate drive IC for 2 MHz power amplifier.

2.5 Simulated Performance for 2 MHz Power Amplifier

The freeware SPICE program LTspice was used to approximate the circuit behavior in the time domain [77]. The device model provided by the HEMT supplier was used without alteration, although other published results show that these models may require additional scrutiny [78]. The circuit as simulated is shown in Figure 2.7 and the passive component values are annotated in Table 2.2. A nominal Q_L value of 5 was used for the entirety of this work. Note that four HEMTs and their associated gate drive resistors were implemented in parallel to reduce the current stress per device. The results indicate a very high theoretical power added efficiency (PAE) of 98.6%, with a total of 14 W dissipated across the four HEMTs.

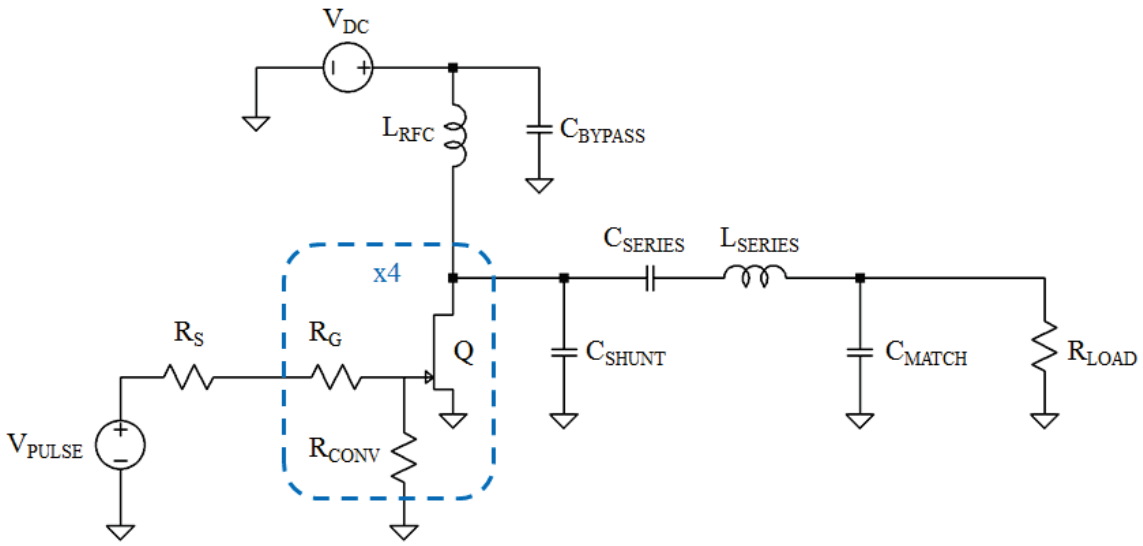


Figure 2.7 – 2 MHz power amplifier circuit as simulated.

Table 2.2 - Passive component values used in the prototype amplifier.

Name	Value
R_G	2 Ω
C_{SHUNT}	1,307 pF
C_{SERIES}	1,844 pF
L_{SERIES}	6.3 µH
C_{MATCH}	2,760 pF

Figures 2.8 and 2.9 illustrate the relevant waveforms. The ringing at device turn off as observed in the drain current trace is due to the very low $R_{DS,ON}$ of the HEMTs. The 170 VDC bus produces a maximum drain to source potential of 610 V, which is within the rated maximum.

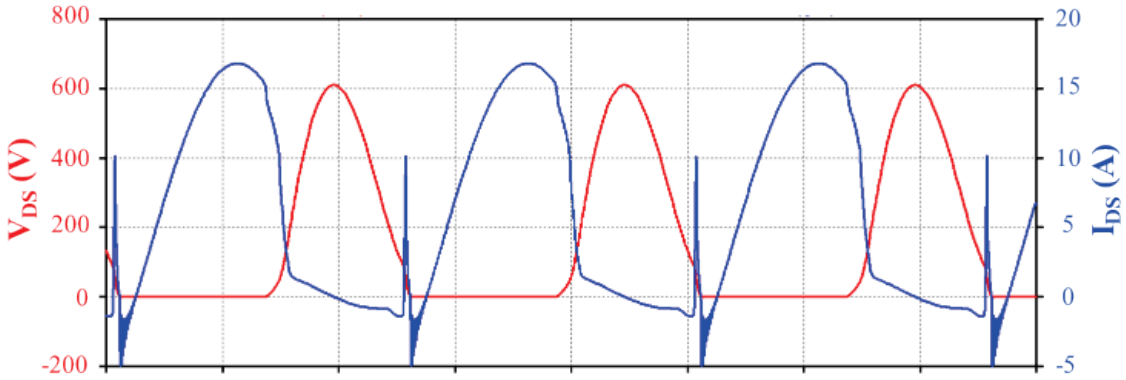


Figure 2.8 - Simulated 2 MHz drain voltage and current waveforms.

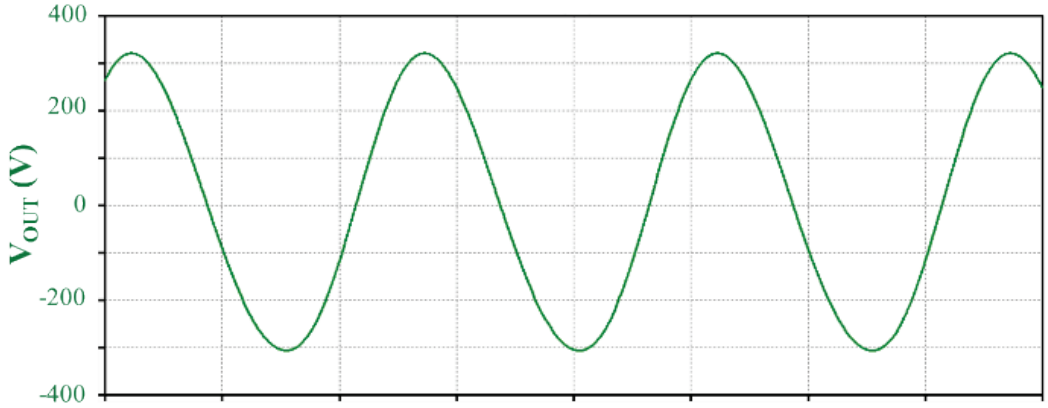


Figure 2.9 - Simulated 2 MHz output voltage waveform.

2.6 Experimental Verification of 2 MHz Power Amplifier

The amplifier was constructed on a 90-mil thick FR4 PCB using 2-oz copper traces to maximize heat spreading. The amplifier was affixed to a water cooled heat sink which was maintained at approximately 18 °C for the duration of the measurements, and a fan provided airflow. The output was connected to a water cooled RF load. An annotated photograph of the amplifier is shown in Figure 2.10.

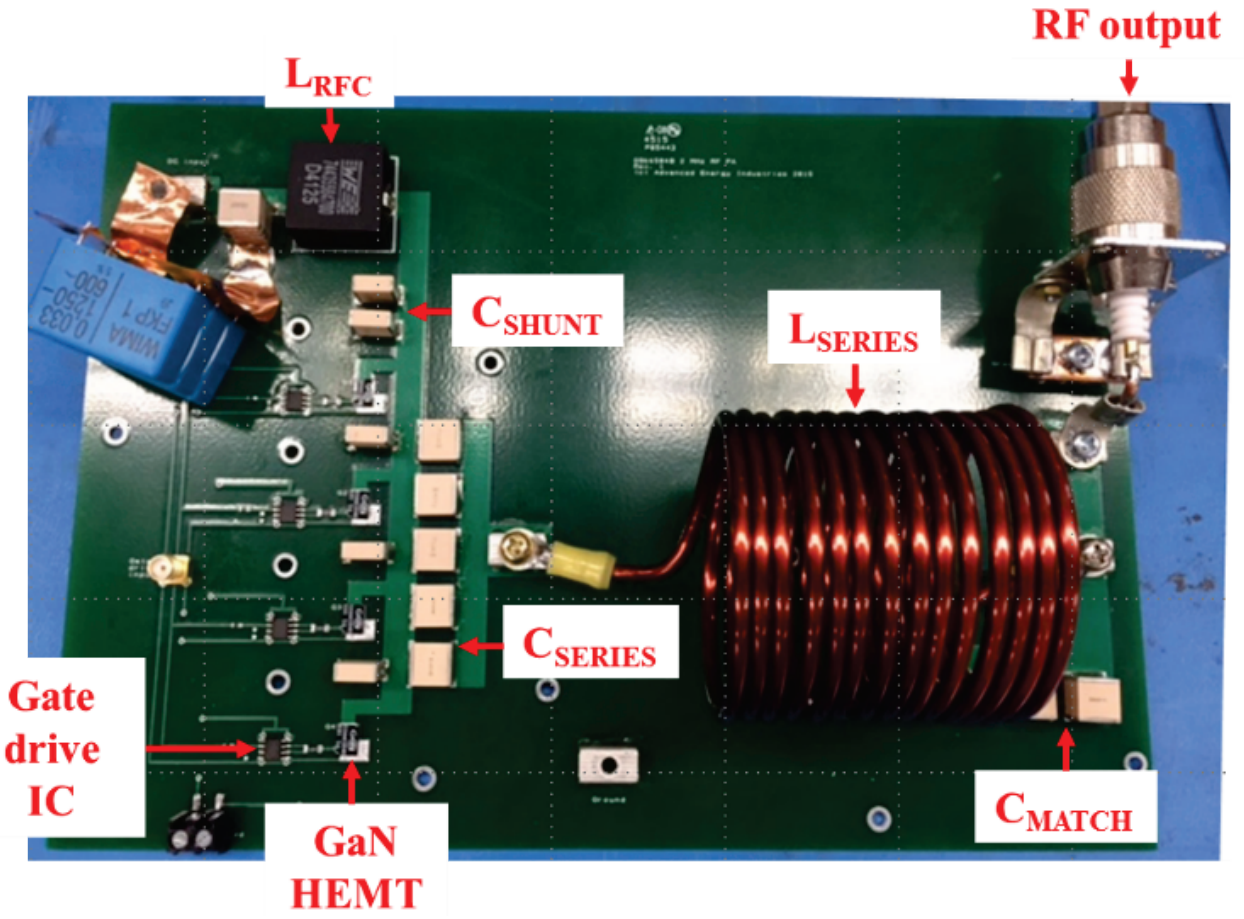


Figure 2.10 – 2 MHz prototype amplifier as tested.

Figures 2.11 and 2.12 show the drain and output voltage waveforms, respectively. The maximum drain voltage is 643 V and the shape exhibits well controlled Class E behavior. A Bird 4021 RF power sensor and 4421 power meter measured the output power delivered as 1,009 W. This value accounts for a 0.4% loss in a six foot length of RG-393 coaxial cable. Figure 2.13 shows the attenuation of RG-393 for reference.

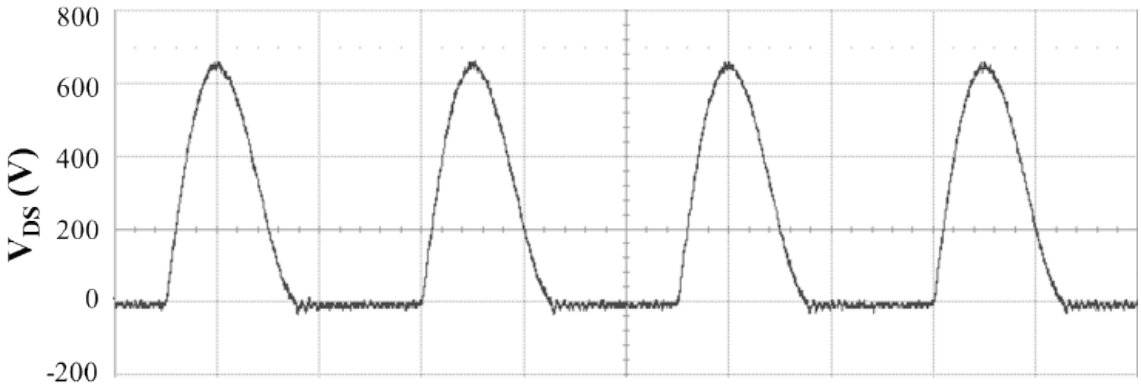


Figure 2.11 - Measured 2 MHz PA drain voltage waveform.

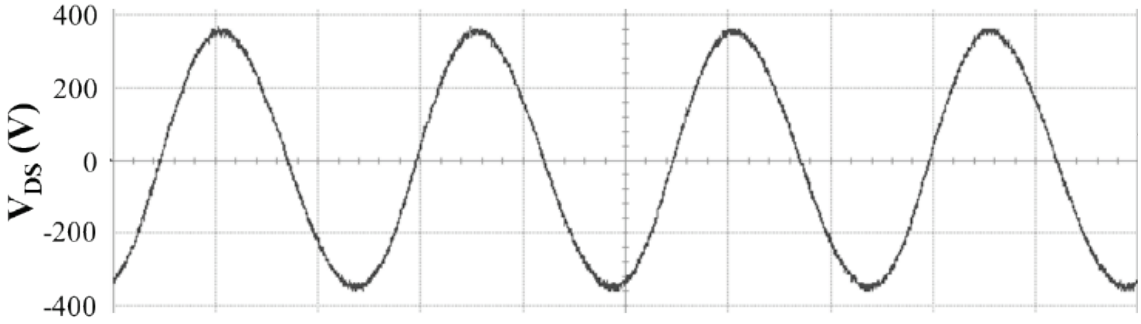


Figure 2.12 - Measured 2 MHz PA output voltage waveform.

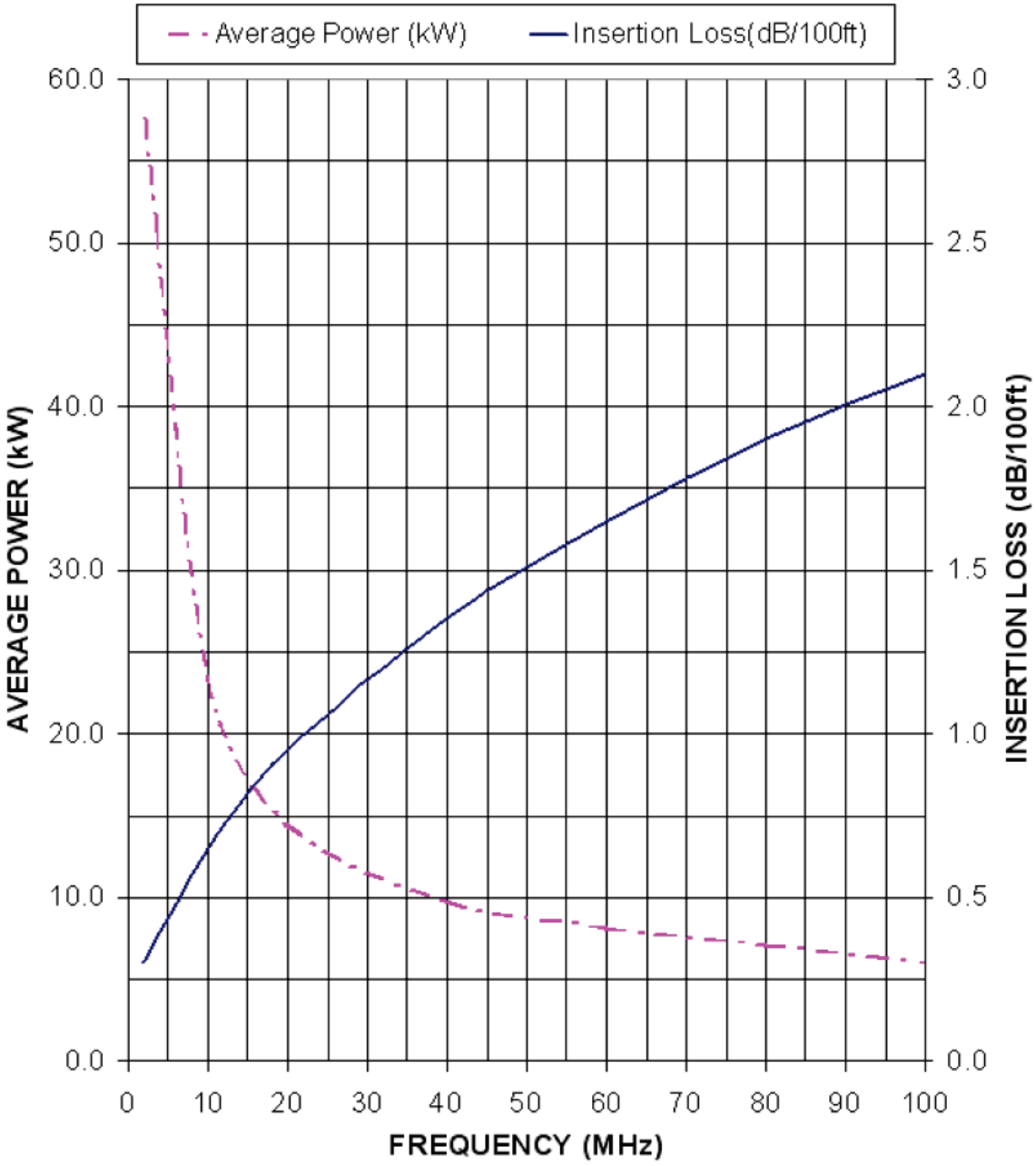


Figure 2.13 – Attenuation of RG-393 cable, from [79].

Input voltage was measured with a Keithley 2000-2 multimeter. To determine the input current, a 2 mA/V calibrated shunt was wired in series with the power amplifier drain and the DC voltage across the shunt measured with an Agilent 34401A multimeter. The positive and negative leads of both the supply and measurement cables were tightly twisted and routed as far from each other as was practical. RF suppression on the measurement cables were provided by multiple clamp-on ferrites. At 1,009 W RF output power, the input power was measured at 1,073 W.

The resultant power added efficiency (PAE) of 94% is noticeably lower than the simulated value of 98.6%. There are a few obvious sources of the discrepancy. Firstly, PCB parasitics were not modeled in the LTspice simulations, and some losses of this type are inevitable. Secondly, it should be noted that very little effort was spent tuning the amplifier resonant elements or the matching elements to increase efficiency. A detailed frequency domain analysis of these parameters would likely yield further efficiency improvements. Finally, the simulated amplifier did not account for RF choke dissipation, yielding higher efficiency figures. Nevertheless, a 94% PAE remains high compared to similar amplifiers based on silicon active devices.

Figure 2.14 is an infrared image of the amplifier when operated at 1 kW output power. The RF choke operates at an elevated temperature for two reasons: (1) its value was oversized to ensure operating stability, and (2) the ferrite core was not specifically designed for low loss at high frequencies. Nonetheless, the maximum surface temperature of approximately 74 °C is acceptable. Three of the four HEMTs have surface temperatures of 27 °C; the remaining device is at 39 °C. This discrepancy was later found to be related to a gate drive IC defect. The form factor of the HEMTs is a passivated die and as a result, the channel temperatures are easily estimated by adding approximately 5 °C to the maximum surface temperature. It is apparent that the devices are well

within their thermal operating range and could likely be operated with a well-designed forced air heat sink in place of chilled water cooling.

Figure 2.14 - Infrared thermal measurement of amplifier at 1 kW output.

2.7 Gate Drive Design for 13.56 MHz Power Amplifier

The GS66504B was used as the active device in a power amplifier with a 13.56 MHz center frequency, a popular ISM frequency for plasma processing equipment. The ON/OFF switching times for a ~ 74 ns cycle are ideally no greater than 5 ns, unachievable with the IXYS / Clare IXD609 gate drive IC as utilized in the 2 MHz design. Instead the gate drive was designed around an alternate IC – the LM5114 from Texas Instruments. An internal block diagram of the part is shown in Figure 2.15. The pertinent specifications include a 7.6 A sink and 1.3 A source current capability, rise and fall times of 5 ns, and a leadless package for low parasitics. The part is also

specifically designed to drive enhancement mode GaN HEMTs and has separate positive and negative outputs to allow for independent rise and fall control times through the use of unequal additional gate drive resistors. Application notes and reference designs from GaN Systems indicate that the inclusion of a low dropout regulator (LDO) at the input of the LM5114 improves stability. The Micrel MIC5225 was chosen for this function [80]. This part requires minimal external parts while providing a typical 0.25% load regulation. The LDO functionality also adds a level of device protection for unintentional gate drive loss. A functional block diagram of this part is shown in Figure 2.16.

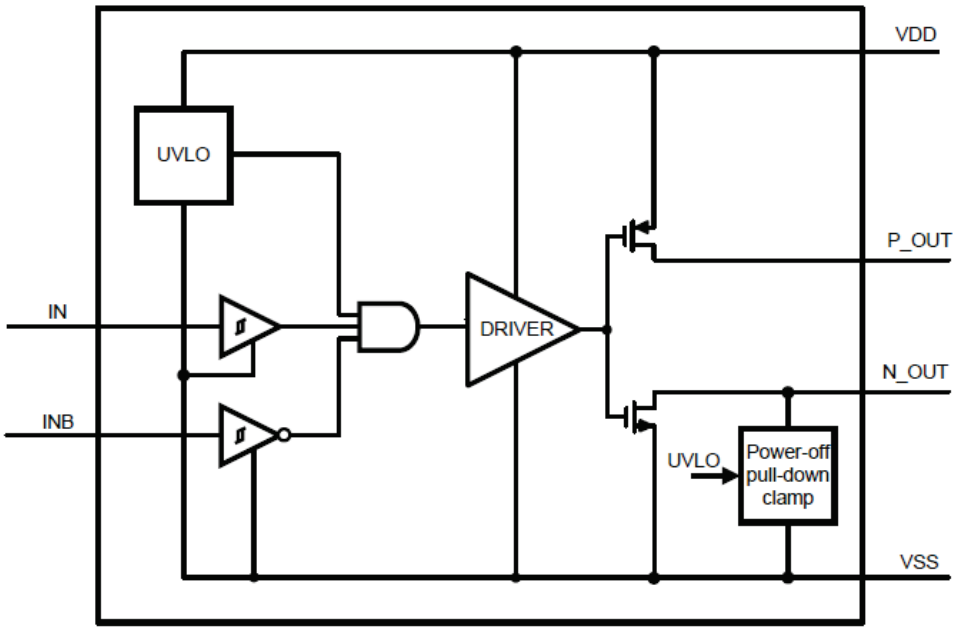


Figure 2.15 – Functional block diagram of gate drive IC used in 13.56 MHz power amplifier.

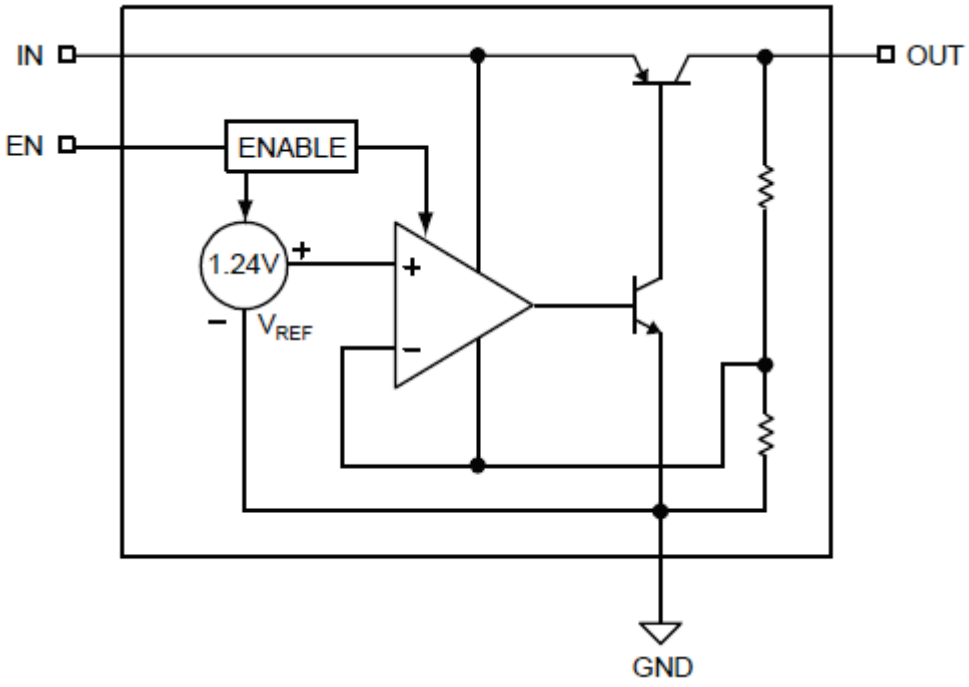


Figure 2.16 – Functional block diagram of LDO used in 13.56 MHz amplifier.

2.8 Simulated Performance for 13.56 MHz Power Amplifier

LTspice was used for simulation of time domain behavior and a cursory frequency domain analysis with the Fast Fourier Transform (FFT) functionality. The HEMT device model was unchanged. The schematic simulated is shown in Figure 2.17, while the final passive component values are tabulated in Table 2.3. It was found through multiple iterations that a reduction in the DC rail value from ~ 170 VDC enabled progressively higher total efficiency. For the simulations, a DC input voltage of 130 VDC was used. As with the 2 MHz amplifier, R_S is the source impedance of the pulse generator. C_{BYPASS} is a high frequency decoupling capacitor comprised of a large aluminum electrolytic and a polypropylene film and aluminum foil capacitor. R_{CONV} aids the simulator in achieving convergence of the standard Newton-Raphson algorithm immediately following the initial startup.

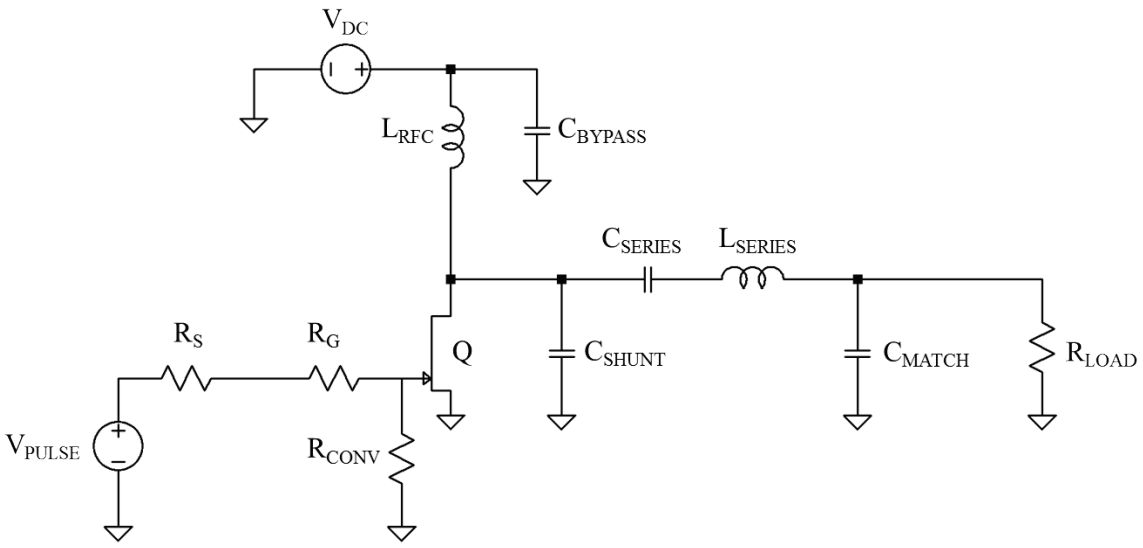


Figure 2.17 – 13.56 MHz power amplifier circuit as simulated.

Table 2.3 - Passive component values used in the prototype amplifier.

Name	**Value**
R_G	2 Ω
C_{SHUNT}	53 pF
C_{SERIES}	109 pF
L_{SERIES}	1.985 µH
C_{MATCH}	201 pF

The simulated drain voltage and current is shown in Figure 2.18. The reduction of the supply voltage has kept the peak drain voltage at approximately 460 V. The drain current has a peak value of 6.5 A, with an RMS value of 3.7 A. Both the drain voltage and current are comfortably within the manufacturer specifications and indeed have margin for higher power

operation. The drain voltage displays well controlled Class E behavior. The simulation indicates however that there is an oscillation in the drain current, most likely due to the low ON resistance and input capacitance of the GaN HEMT. This observation was explored using the FFT functionality, which is illustrated in Figure 2.19. There are significant peaks in the drain current at harmonics of 13.56 MHz, and many of them are ~ 30 dB lower in relative magnitude than the fundamental. Although the individual harmonics are low in magnitude, the combination of all harmonics is noticeable in the Figure 2.18 drain current waveform.

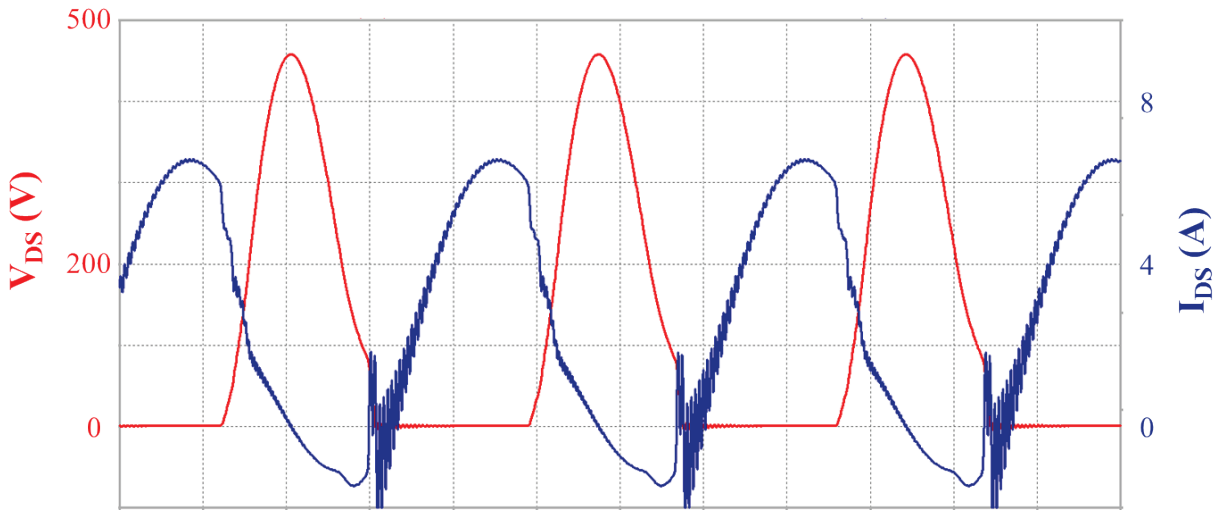


Figure 2.18 - Simulated 13.56 MHz drain voltage and current waveforms.

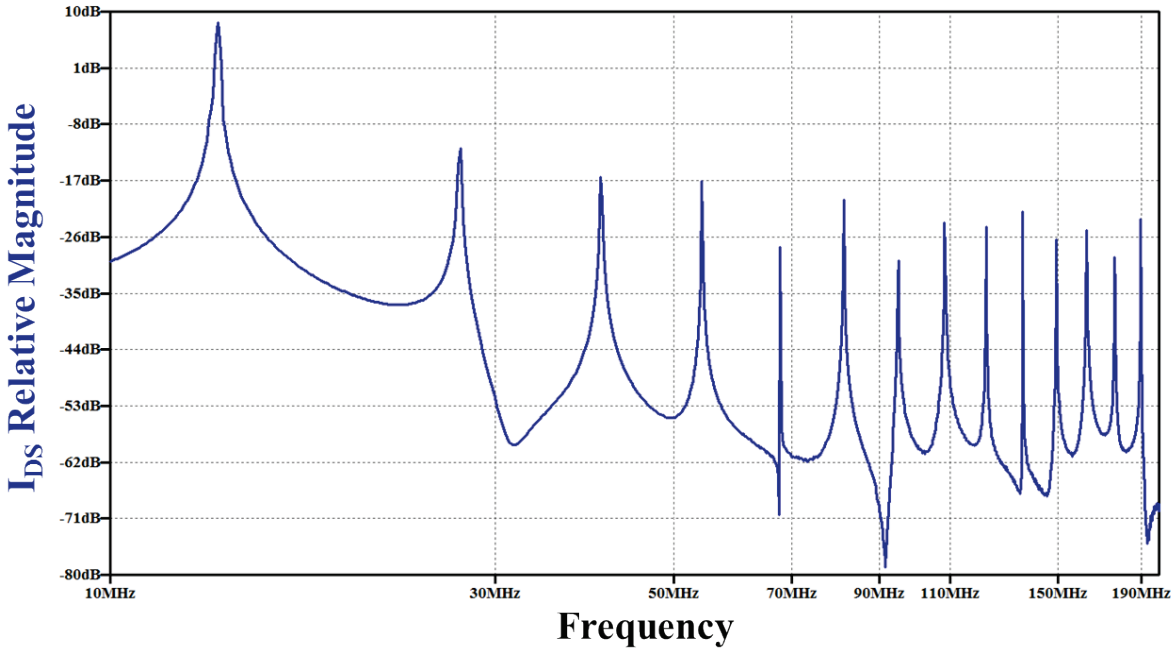


Figure 2.19 – FFT of simulated 13.56 MHz drain current waveform.

The simulated output voltage is presented in Figure 2.20. The sinusoid has a peak value of 180 VAC, with an RMS value of 120.7 VAC. The results calculate a PAE of 96.8%, with 9.8 W dissipated in the GaN HEMT.

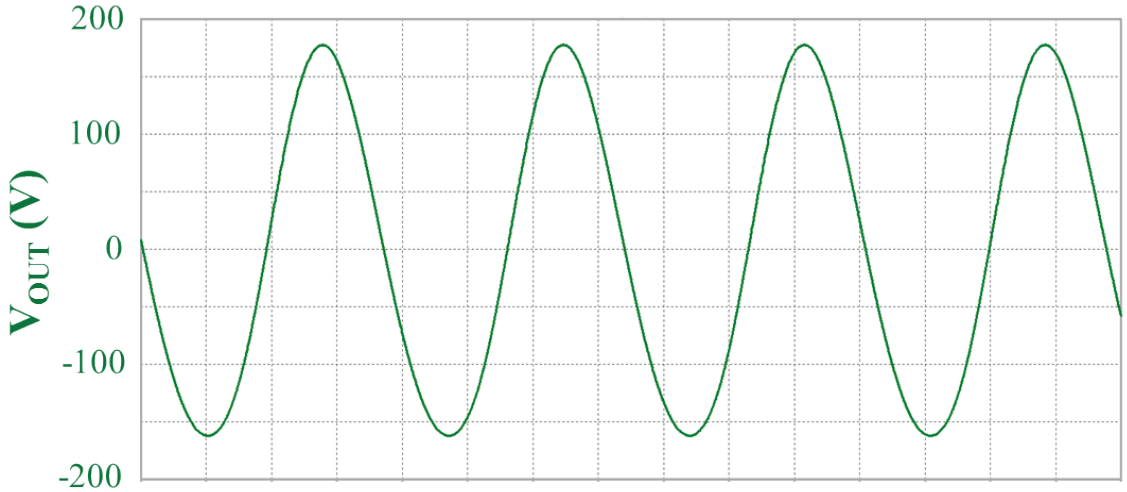


Figure 2.20 – Simulated 13.56 MHz output voltage waveform.

2.9 Experimental Verification of 13.56 MHz Power Amplifier

The 13.56 MHz amplifier utilized 90-mil thick FR4 PCB with 2-oz copper traces. The PCBA layout was scrutinized to minimize parasitics and ground loops, as evidenced by the proximity of the gate drive IC and resistors to the HEMT. A partial view of the layout is provided in Figure 2.21.

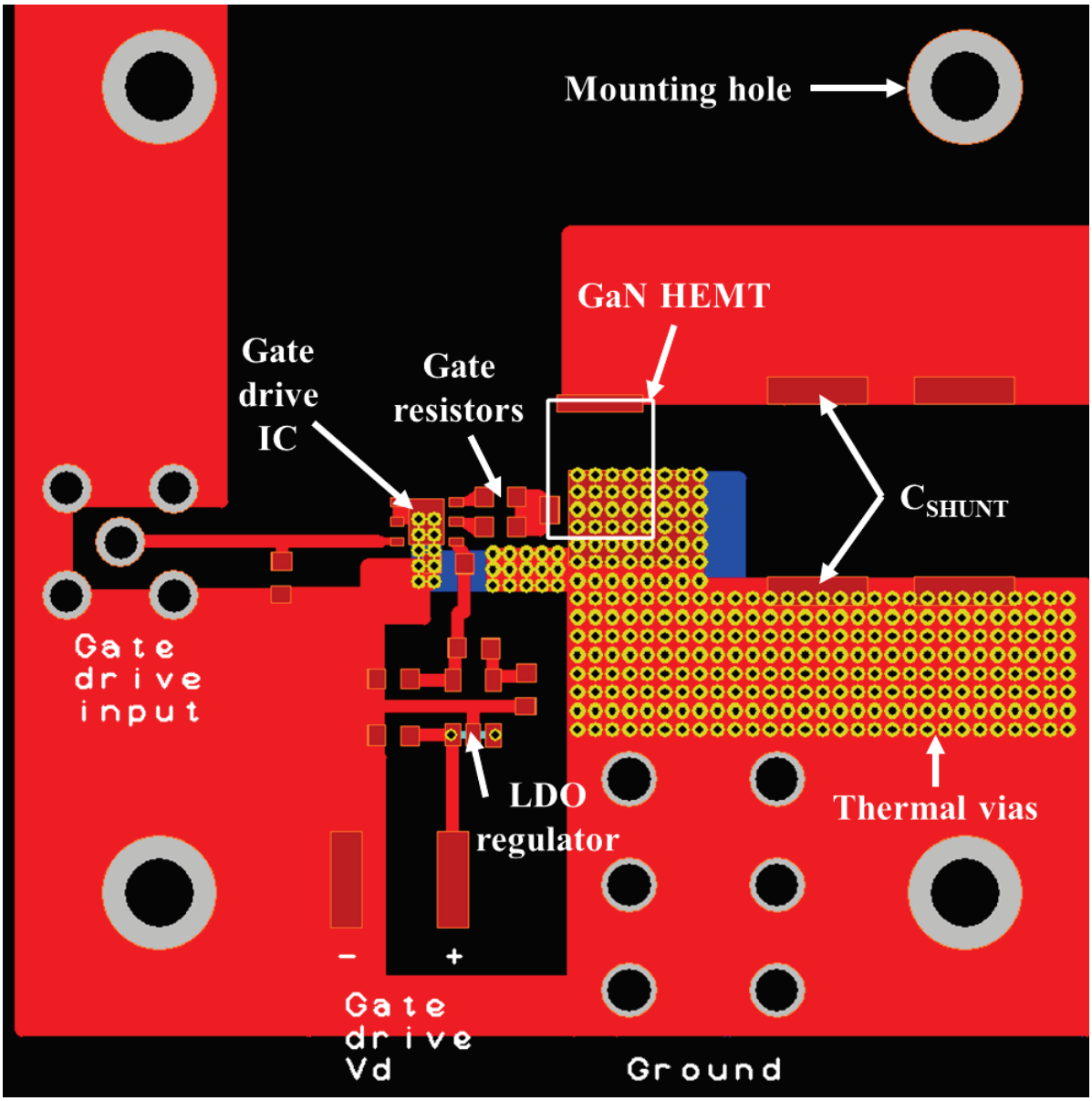


Figure 2.21 – Partial view of 13.56 MHz power amplifier PCBA layout.

Similar to the 2 MHz verification, the 13.56 MHz amplifier was mounted to a water cooled heat sink controlled to approximately 18 °C, while a fan provided supplementary airflow. The output was connected to a water cooled RF load. An annotated photograph of the amplifier is shown in Figure 2.22.

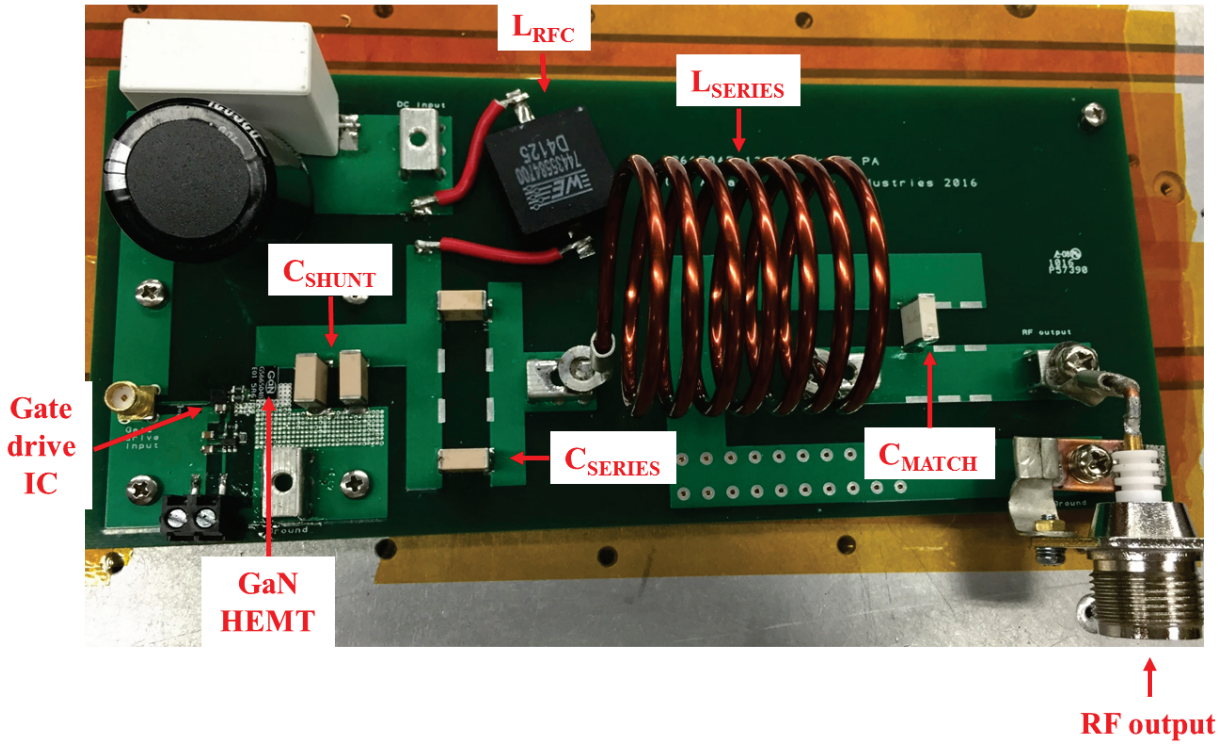


Figure 2.22 – 13.56 MHz prototype amplifier as tested.

The drain and output voltage waveforms are represented in Figures 2.23 and 2.24, respectively. The maximum drain voltage is 415 V. A proprietary 13.56 MHz RF power sensor with an accuracy of less than +/- 1% measured the power output as 236 W [81], [82]. This value accounts for a 0.9% loss in a six foot length of 6 ft RG-393 coaxial cable. Similar methods as those described for the 2 MHz amplifier were used to measure the input voltage and current. At 236 W RF output power, the input power was measured at 254 W, indicating a total of 18 W dissipation.

Although not verified, it is likely that ~ 13 W were dissipated in the HEMT while the remaining 5 W is distributed across the passive parts, particularly the RF choke, series capacitor, and series coil. The PAE is calculated at 93%, lower than modeled but nonetheless higher than traditional Si implementations. An additional explanation for the lower than modeled efficiency could be the presence of harmonics in the drain waveform, as predicted by LTspice. Provisions for measuring drain current were not made in the PCBA layout, and the output filter removes these harmonics from the output waveform.

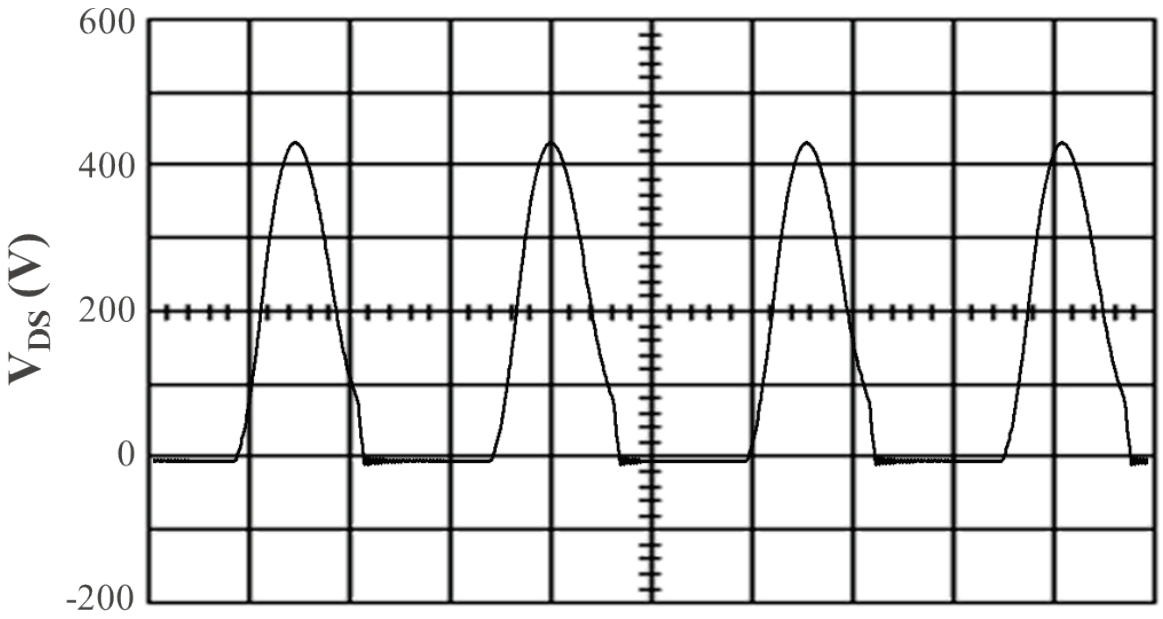


Figure 2.23 – Measured 13.56 MHz PA drain voltage waveform.

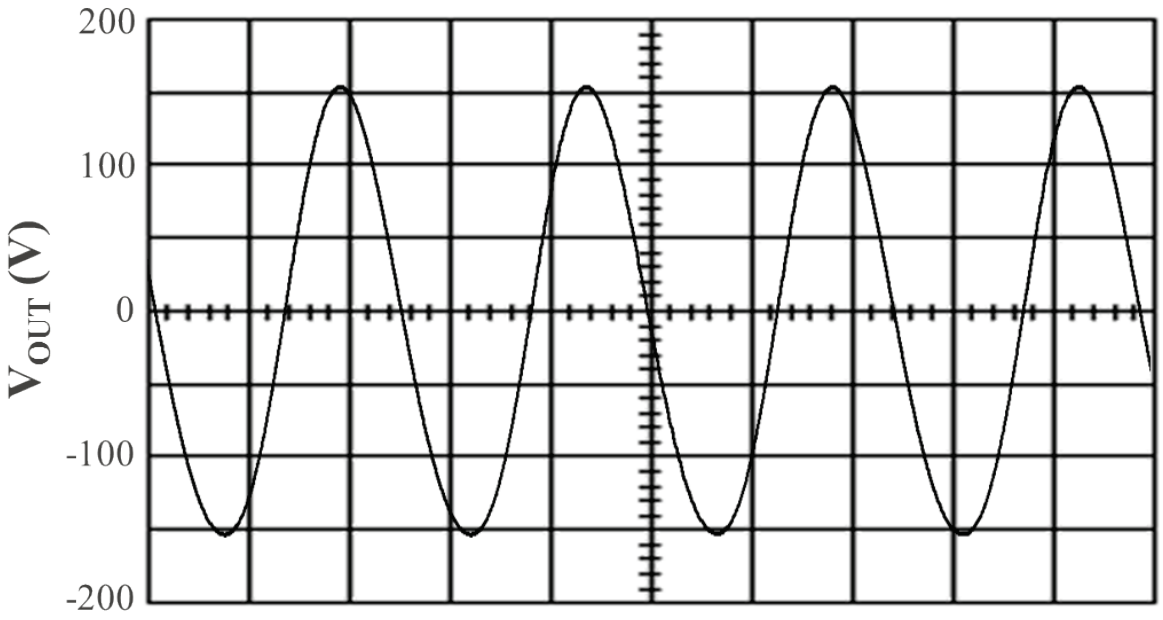


Figure 2.24 – Measured 13.56 MHz PA drain voltage waveform.

2.10 Summary

The absence of loss mechanisms due to reverse recovery charge, low input capacitance and ON state resistance, and a chip scale package which minimizes parasitics hypothetically create a device which is well suited to switch mode operation at frequencies in the tens of MHz. The work in this chapter demonstrates that this theory is valid. Considering the constraints of widely documented amplifier topologies, a pair of Class E RF power amplifiers were conceived, designed, simulated, and experimentally verified using the GS66054B GaN HEMT from GaN Systems.

The 2 MHz amplifier utilized four devices well below their datasheet voltage, current, and temperature ratings to achieve an RF power output of 1,009 W with a PAE of 94%. Infrared thermography also demonstrates the fundamental efficiency of the GaN HEMTs, as the estimated channel temperatures were lower than 40 °C.

The 13.56 MHz amplifier was demonstrated to generate 236 W of RF power with a single HEMT, with a PAE of 93%. In this implementation, the device is operated at lower voltages, but at higher current. Again the demonstrated efficiency is less than the modeled value, but simulations indicate that oscillations may be at least partially responsible.

Many variants of this work could be explored further. The implementation of the same or similar GaN HEMTs in Class D amplifiers for compact higher power amplifiers, especially at lower frequencies where the gate drive timing is less challenging to achieve, would be a reasonable extension. Class F topologies may also prove to be relevant particularly at frequencies higher than those evaluated here, but with correspondingly lower output power.

CHAPTER 3 – TRANSIENT AND STEADY STATE THERMAL PERFORMANCE

3.1 Introduction

The importance of thermal management in power electronics cannot be overstated. With the exception of extremely low temperature environments, elevated temperatures degrade both performance and reliability. Regardless of the failure modes involved, it is always necessary for an engineer to be cognizant of the many aspects of thermal control required. Steady state thermal parameters are generally straightforward and can be recorded using equipment such as thermocouples, infrared images, or fiber optic devices. Depending on the parts in question and the thermal system design, transient thermal parameters may be not only significantly more challenging to capture but also more complex in determining if additional actions are required and how to implement them.

This chapter expands on this topic specifically as it relates to commercially available CSP GaN HEMTs. The chip scale packaging has appealing benefits, including low cost and small physical size. But the minimalist form factor is directly responsible for a select set of drawbacks. The lack of integrated thermal management pushes the burden of heat removal onto the additional components comprising the thermal system. As a point of reference, Table 3.1 illustrates a sample of common semiconductor packages and their respective methods for thermal management. All of the other packages incorporate some method of thermal management; the large IGBT and ISOTOP have direct copper bond (DCB) baseplates which act as heat spreaders. The Xeon microprocessor die is attached to a heat spreader, as can be seen in Figure 3.1 [83]. As illustrated in Figure 3.2, the VHF MOSFET uses a highly engineered thermal stackup with BeO, a Cu/Mo/Cu composite, a brass body, and a copper baseplate to match the coefficient of thermal expansion

(CTE) of the Si die to the heat sink [84]. The chip scale packaged GaN HEMTs, however, have an active area encapsulated in a high temperature FR4 sandwich which has gate, drain, and source connections on the bottom side [85]. When a CSP part is attached to a circuit board, there are no heat spreading or CTE matching materials, so steady state and transient thermal stresses must be controlled through other methods. The experimental regimens in this chapter were designed to quantify how CSP GaN HEMTs perform thermally in a typical system including a PCB and a heat sink.

Table 3.1 – Sample of semiconductor packages and thermal management strategies.

	Device	**Thermal dissipation density**	**Thermal management**	**Package cost**
	Intel Xeon	0.06 W/mm^2	• Integrated heat spreader • Numerous pins for direct heatsinking	Medium
	High power IGBT	0.2 W/mm^2	• DCB plate • Large active area: package size	High
	SOT-227 (ISOTOP)	0.6 W/mm^2	• DCB plate • Bond wires	Medium
	GaN Systems HEMT	0.6 W/mm^2	• Cooled through source pad • Die in FR4 stack	Low
	Industrial VHF	2 W/mm^2	• Cu/BeO/Mo stack for CTE match	High

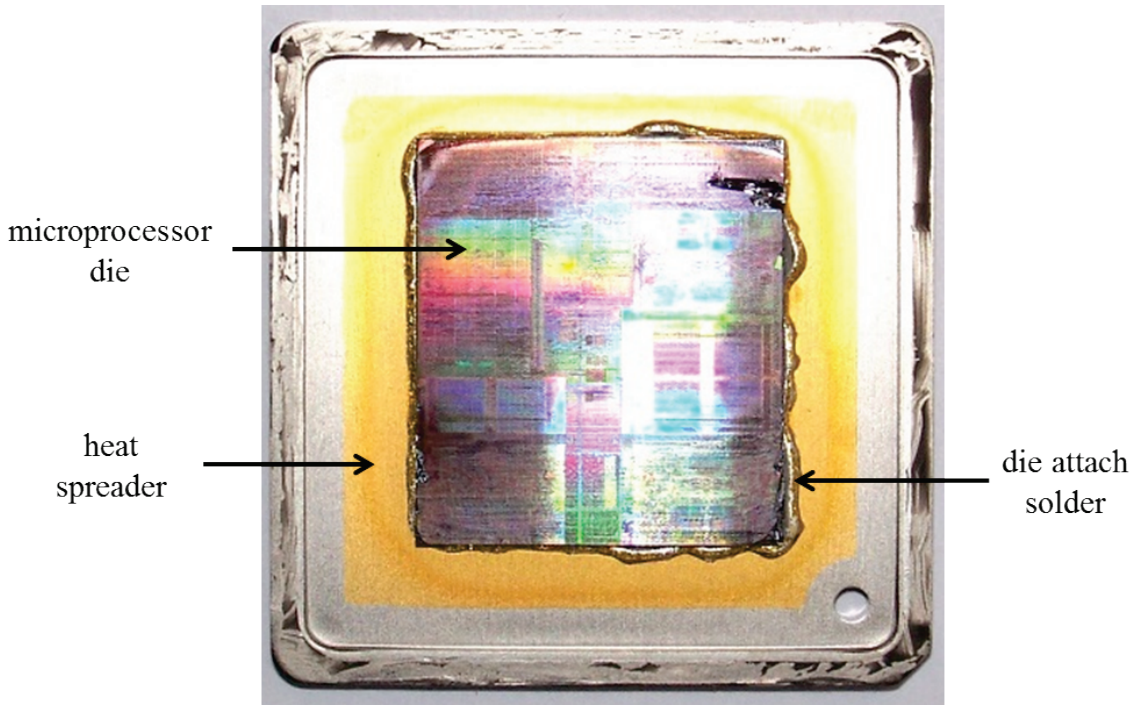


Figure 3.1 – Intel Xeon microprocessor die on heat spreader, from [83].

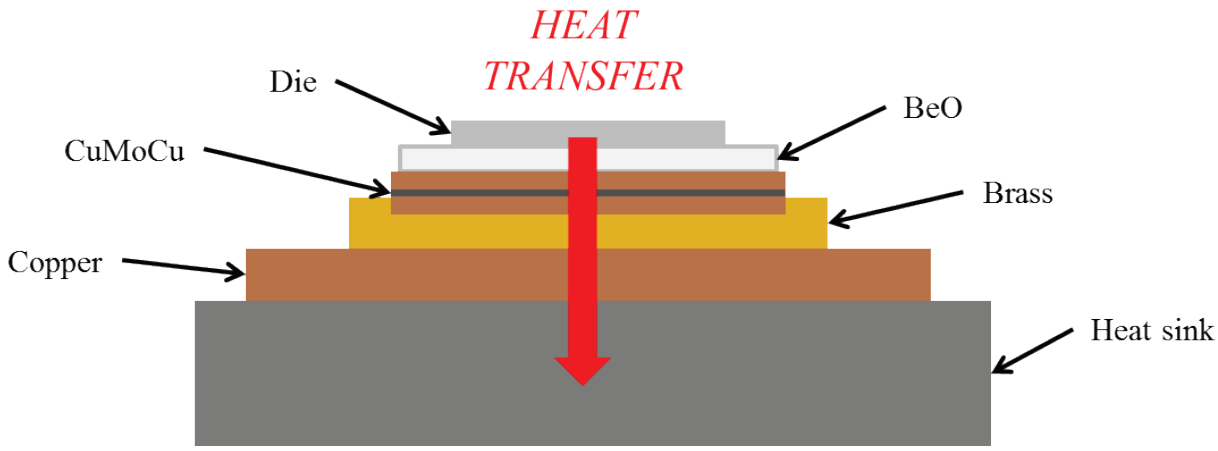


Figure 3.2 – Thermal management scheme for industrial VHF MOSFET, from [84].

3.1 Experimental Design for Thermal Characterization

Two types of GaN HEMTs were chosen for experimentation, both of which are manufactured by GaN Systems. As implemented in the 2 MHz and 13.56 MHz amplifiers, the GS66504B is a device which is cooled primarily through the bottom side source pad [71, p. 66504]. Another device type is embodied in the GS66516T which has a top-side thermal pad for higher power dissipation [72]. Although two variants were ultimately required, a simple four-up PCBA fixture was designed to accommodate the parts under test, while providing gate drive and drain current measurement functionality. The PCBA fixtures for GS66504B and GS66516T are illustrated in Figures 3.3 and 3.4, respectively. The PCBA for the GS66504B was designed using the manufacturer recommended thermal via layout, which enlarges the source pad further than the extent of the package outline, as illustrated in Figure 3.3a. A gap pad (Bergquist 5000S) was used to provide z-axis compensation of mechanical variation between the PCBA and heatsink with good thermal performance; a 20-mil resultant thickness has a thermal resistance of 0.15 °C·in^2/W [86]. As can be seen in Figure 3.3b, the PCBAs were attached with fasteners to a water cooled heatsink maintained at 15 ± 1 °C. The PCBA fixture used for the GS66516T is identical in functionality but the top-side thermal pad on the device requires the HEMT to be affixed to the bottom side of the PCBA, enabling direct cooling to the heatsink. Referring to Figure 3.4, subfigure (a) shows the gap pad with a cutout to accommodate the HEMT. The total z-axis thickness of the device and solder joint is very close to the 20-mil gap pad thickness, to within 2 mils. A sheet of pyrolytic graphite (Panasonic PGS) was then placed over the gap pad and device, as shown in Figure 3.4b. This material functions as a heat spreader in the x-y direction, as the specified thermal conductivity in the x-y plane is a very high 1,950 W/m·K for a 10 μm thickness [87]. Figure 3.4c shows the PCBA detail, including a circular hole which is used for IR imaging of the device underside.

Similar to the PCBA for the GS66504B, the fixture used to test the GS66516T is attached to the heatsink with fasteners.

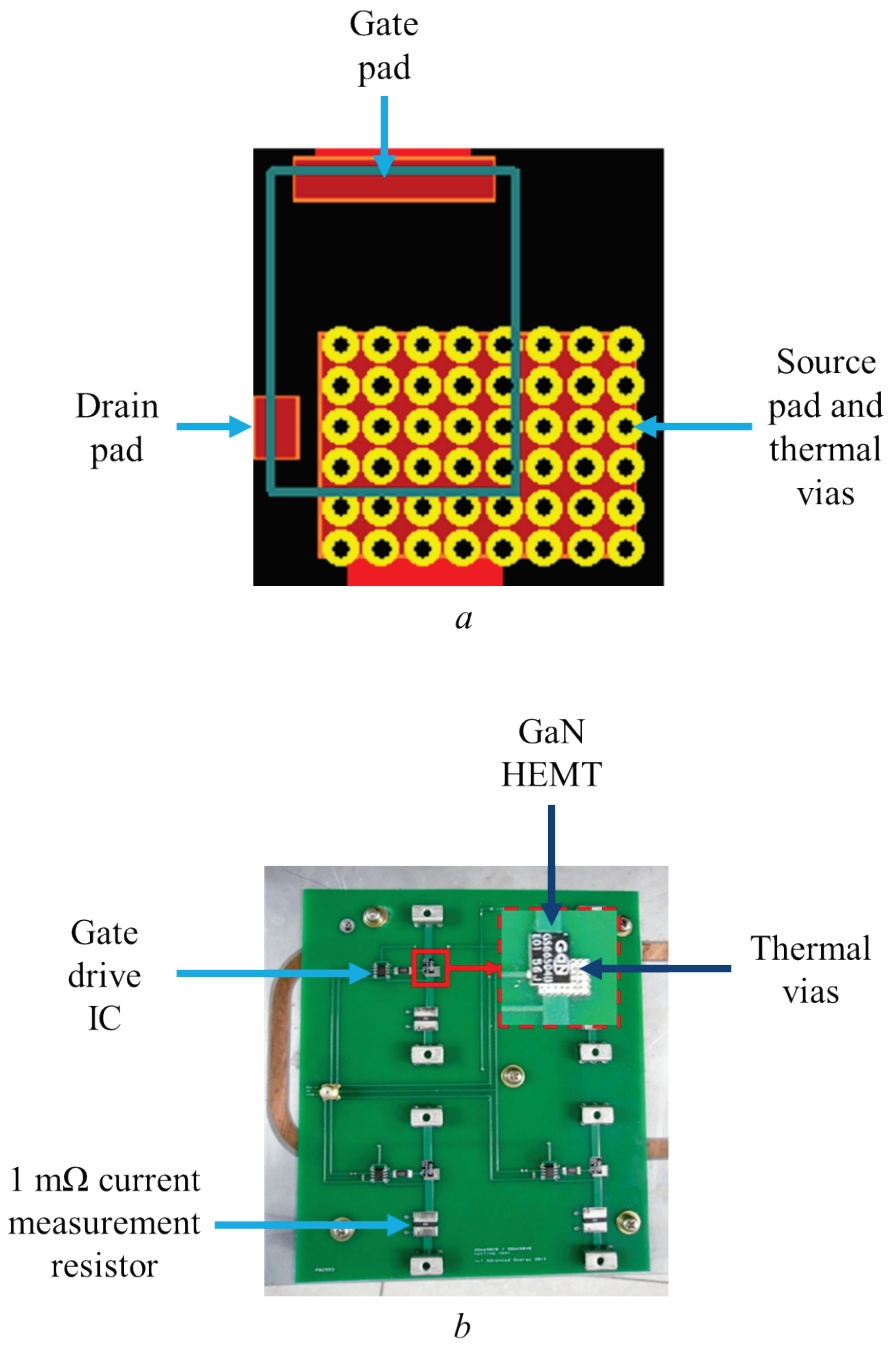


Figure 3.3 - Test fixture for bottom-cooled HEMTs.

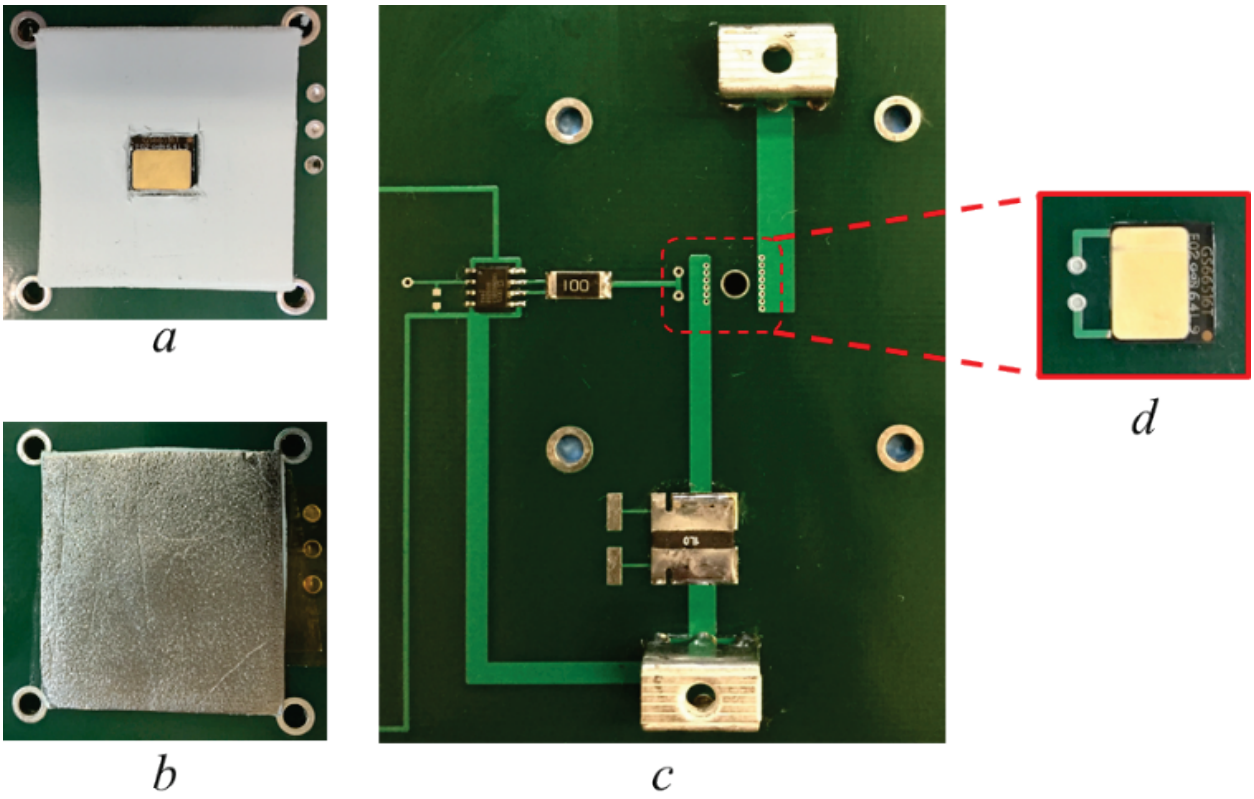


Figure 3.4 - Test fixture for top-cooled HEMTs: (a) with gap pad, (b) including graphite heat spreader, (c) top view of fixture, and (d) inverted device mounted under fixture.

3.2 Steady State Thermal Results

The first step in the experimental plan was to characterize the two types of devices under steady state conditions. For clarification, 'steady state' in this context refers to a state in which, after application of power, the device under test reached a temperature which did not further increase for a duration of five seconds. A high resolution infrared camera (FLIR Systems SC5000) and associated data capture software were used [88], [89].

The results for the GS66504B are shown in Figures 3.5 and 3.6; results for the GS66516T are shown in Figures 3.7 and 3.8. The thermal performance measured in °C/W is reflective of the entire thermal system comprising the device, thermal interface, and heatsink, so the results are

only valid for a specific embodiment. The GS66504B dissipated 18.8 W when operated at a channel temperature of 132 °C, using the +5 °C approximation. Data for the absolute maximum channel temperature is not available, but linear extrapolation would estimate a power of 23 W associated with operation at 150 °C. The calculated thermal resistance varied from 4.68 °C/W at lower temperatures to 5.27 °C/W at the upper end of the temperature range, evidence of nonlinear behavior, which was verified by repeating the experiment but not explored further. Nonetheless, the maximum temperatures reflected in the measurements are favourable considering the physical size of devices involved.

Power [W]	dT [°C]	°C/W
8.0	37	4.68
10.2	49	4.80
13.5	68	5.04
16.7	88	5.27
18.8	99	5.27

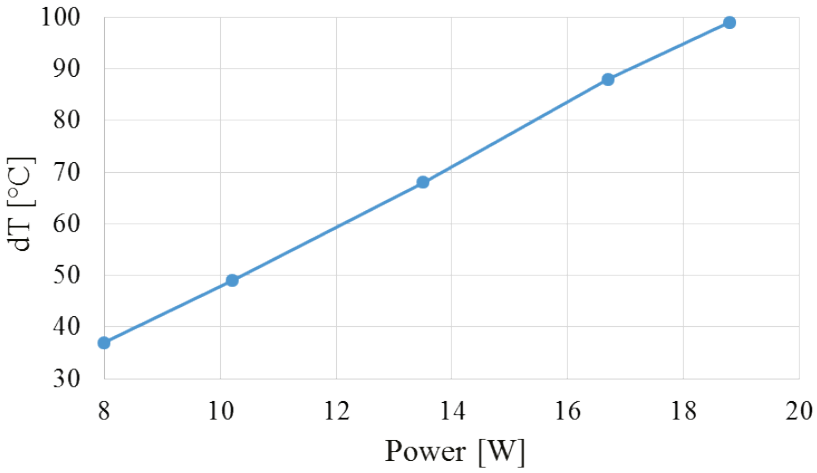


Figure 3.5 - Steady state thermal performance of GS66504B.

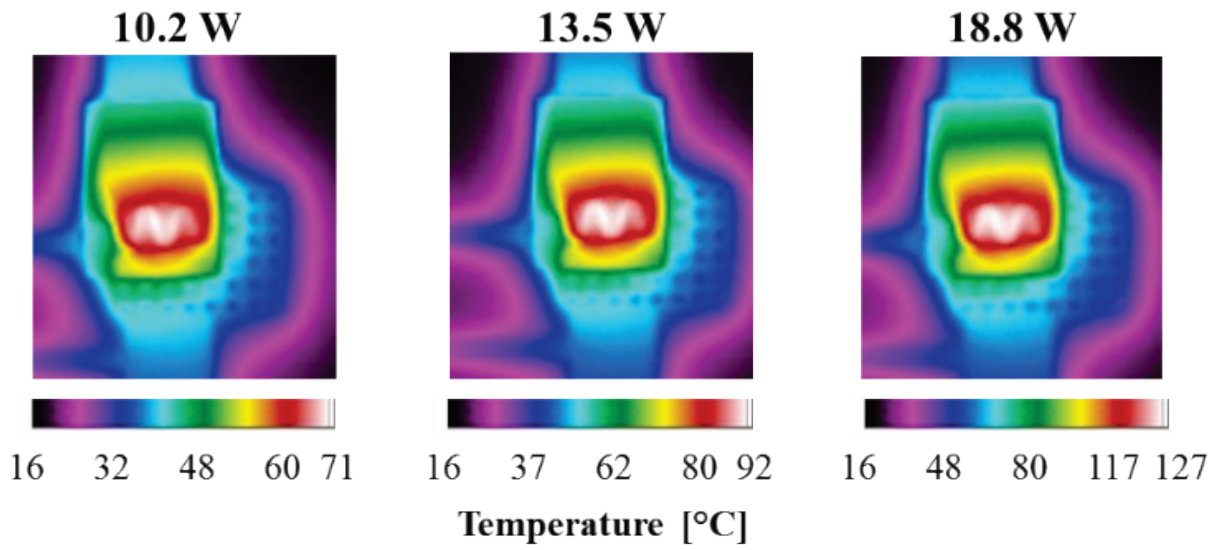


Figure 3.6 - Steady state temperature profiles of GS66504B.

Referring to Figures 3.7 and 3.8, the GS66516T and associated thermal system were capable of dissipating 110 W at 150 °C, for a thermal resistance of ~ 1.2 °C/W. This is in line with other high performance surface mount compatible packages such as the DirectFET [90] and LFPAK [91]. For reference, a carefully designed SOT-227 can easily achieve a thermal resistance of 0.2 °C/W and high power RF packages can be as low as 0.1°C/W [92].

Power [W]	dT [°C]	°C/ W
27	25	0.93
55	60	1.09
74	87	1.18
103	125	1.21

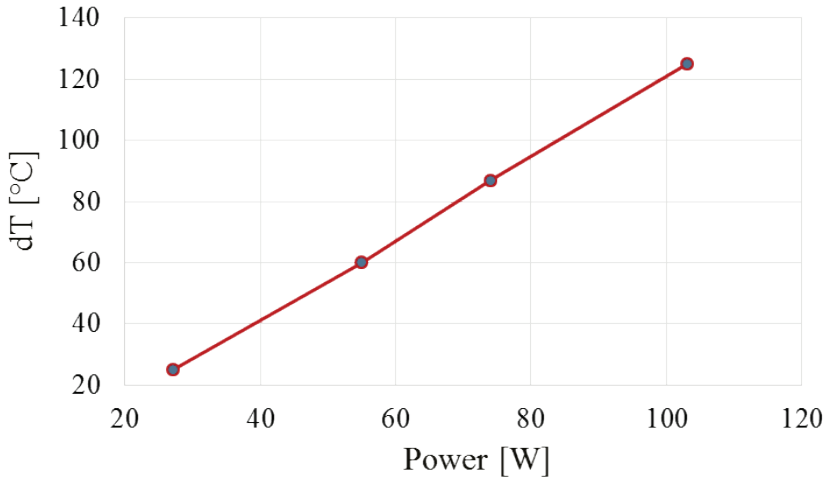


Figure 3.7 - Steady state thermal performance of GS66516T.

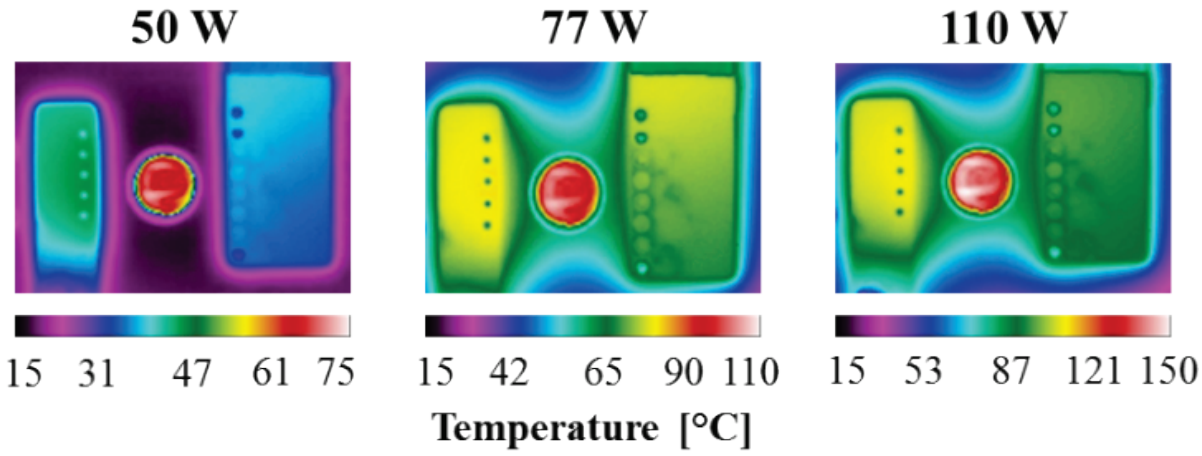


Figure 3.8 - Steady state temperature profiles of GS66516T.

3.3 Measured Transient Thermal Results

Regarding the time dependent thermal behaviour of the devices under test, a separate set of measurements was gathered using the same experimental setup as for the steady state measurements. The power supply used for this set of experiments is a 7 V / 300 A switchmode model from Xantrex [93]. A secondary experiment was conducted which verified that if given sufficient time between events, the power supply was capable of meeting the voltage, current, and power setpoints requested within approximately 70 ms. The rail voltage was held constant and at a time $t = 0$, the gate drive signal was enabled to turn the HEMT to its ON state, mostly unencumbered by power supply lag. The horizontal dashed red line shown in Figures 3.9 and 3.10 the maximum temperature change rate specified by JEDEC JESD22-A106, an industry reference point for comparison [94]. Looking at the data for the GS65504B in Figure 3.9, the device reaches a temperature plateau after approximately 2.5 seconds of 70 °C. This is well within the maximum channel temperature specifications of the HEMT, which is 150 °C. The thermal rate of change exceeds the standard, initially by a factor of > 20x, but settles to a level below this threshold after approximately 0.4 seconds. A similar test at higher power dissipation shows that the dT/dt factor is initially exceeded by a factor approaching 80x and settles below the reference level after about 0.8 seconds.

Similar results are presented for the GS66516T in Figure 3.10. The factor by which the device exceeds the JESD22-A106 standard for dT/dt is lower, but will still clearly drive early life failure modes if power cycled extensively.

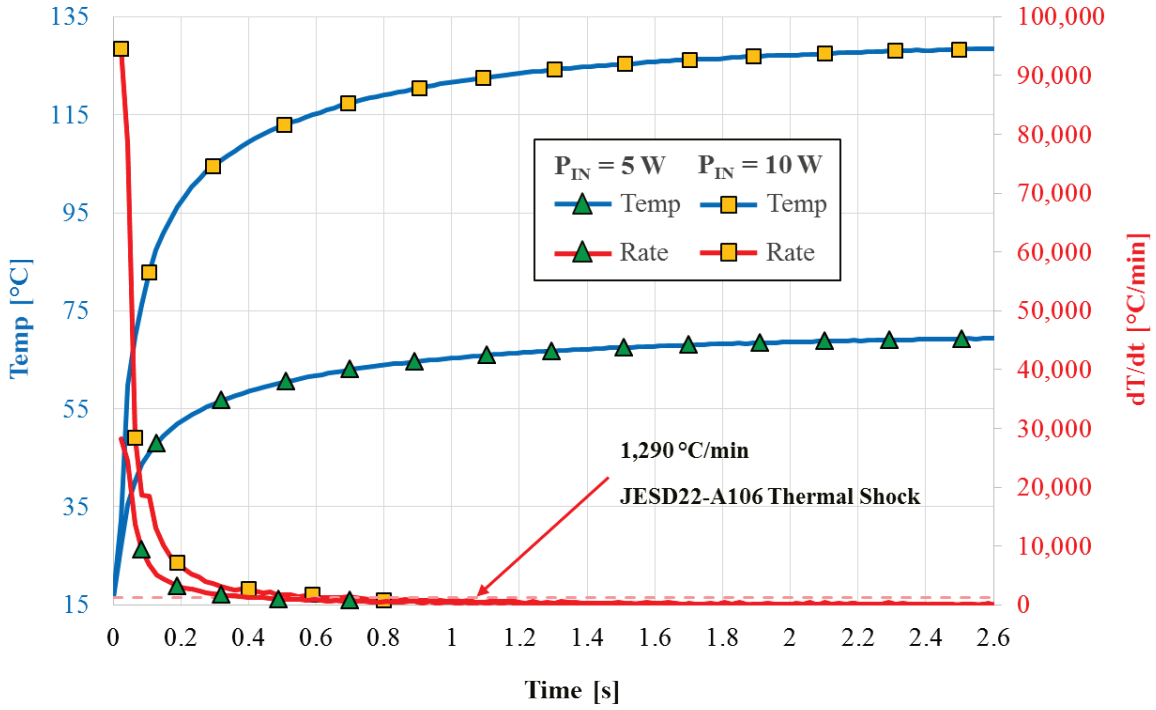


Figure 3.9 - Transient thermal behaviour for GS66504B.

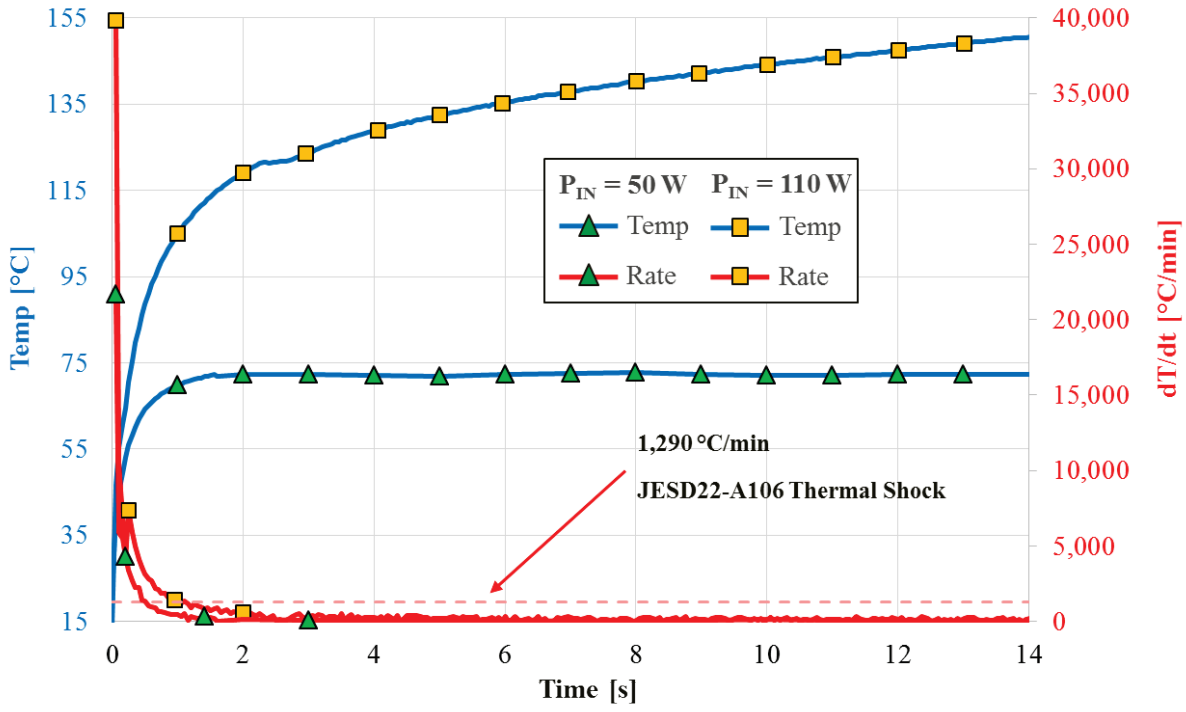


Figure 3.10 - Transient thermal behaviour for GS66516T.

3.4 Extrapolated Transient Thermal Calculations

The measured transient thermal data was obtained through IR imaging of the HEMT surface. Guidance from the device manufacturer indicates that the actual channel temperature will be very close to the measurable value with this method, but for transient analysis, the passivating layer has the effect of delaying the measured response. A straightforward method was used to estimate the actual channel temperature following power application [95]–[98]. Figure 3.11 shows the basic schematic of a lumped capacitance method for estimating the thermal time constant. Like its analog in electrical circuits, this quantity expresses the time in which an exponentially decaying quantity reaches 1/e times its original value and hence provides an estimation in the transient domain of how quickly a system or parts of a system change temperature. At a hypothetical time $t = 0$, the switch is closed, and the dissipated power flows from the source into the bodies which comprise the system. Each body is represented as a parallel RC circuit with a different time constant. As only one interface is unquantified, there is only one RC time constant to calculate. Power eventually flows into the heat sink, which for the purposes of this work is constrained only by its heat transfer coefficient, assumed to be constant over the temperatures of interest.

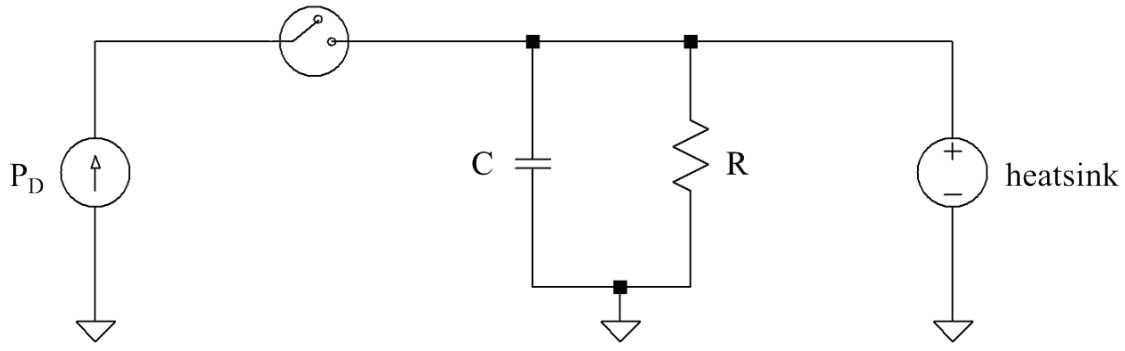


Figure 3.11 – Schematic of lumped capacitance method for transient thermal analysis.

The process for estimating the thermal time constant begins with

$$C(T) = \frac{\delta Q}{dT} \tag{3.1}$$

where C = heat capacity, δQ = heat path function. If the heat path function is sufficiently small, an assumption made here,

$$C = \frac{Q}{\Delta T} \tag{3.2}$$

where Q = heat. The heat capacity represents the capacitive element in Figure 3.11. The heat flux must be considered next, such that

$$\vec{q} = -\lambda \vec{\nabla} T \tag{3.3}$$

where $\vec{q}$ = heat flux, λ = thermal conductivity, $\vec{\nabla} T$ = temperature gradient. For the one-dimensional approximation where all heat is flowing from the source to the sink,

$$q = \frac{H}{A} \tag{3.4}$$

where H = heat per second through the surface and A = surface area

$$H = -\lambda A \frac{dT}{dx} \tag{3.5}$$

where λ = thermal conductivity and dx = distance of heat travel. The resistive element of the thermal time constant is then calculated as

$$R = \frac{dx}{\lambda A} \tag{3.6}$$

Ideally, the type and thickness of the passivation layer would be available but this information is proprietary to the manufacturer. It is known that the HEMT uses a thin deposit of material, and based on the construction of the remainder of the device, it is estimated to be 2 to 5 mils of high temperature FR4 material, the parameters for which are readily available [99], [100]. The following values were used for the thermal time constant approximation: λ = 0.4 W/m·K; dx = 5 mils; A = 6.8 mm^2; specific heat = 1.3 J/g·K; and density = 1.92 g/cm^3. Using the method described, the thermal time constant is calculated as 101 ms.

This value was iteratively back calculated into the measured data to determine by how much the passivation layer retarded the response. The results for the GS66504B are presented in Figure 3.12. Although not verified, the overshoot is likely a function of the simplified model or discrepancy in the material properties. Nonetheless, with reasonable assumption, the channel temperature of the HEMT is likely reaching steady state much faster than measured, perhaps as quickly as 200 ms.

The results for the GS66516T are shown in Figure 3.13. Although the material assumptions are the same, the extrapolated estimate appears to be realistic. Compared to the result for the GS66505B, there is relatively low overshoot and the shape of the extrapolated curve is simply time shifted to the left on the abscissa. As precise accuracy was not the intention, the estimate supports the likelihood that the channel temperature on this HEMT is rising at a higher rate than the measured values. Therefore the actual dT/dt values at the core of the package are surpassing the industry recommendations by a larger margin than it is possible to measure with IR thermography.

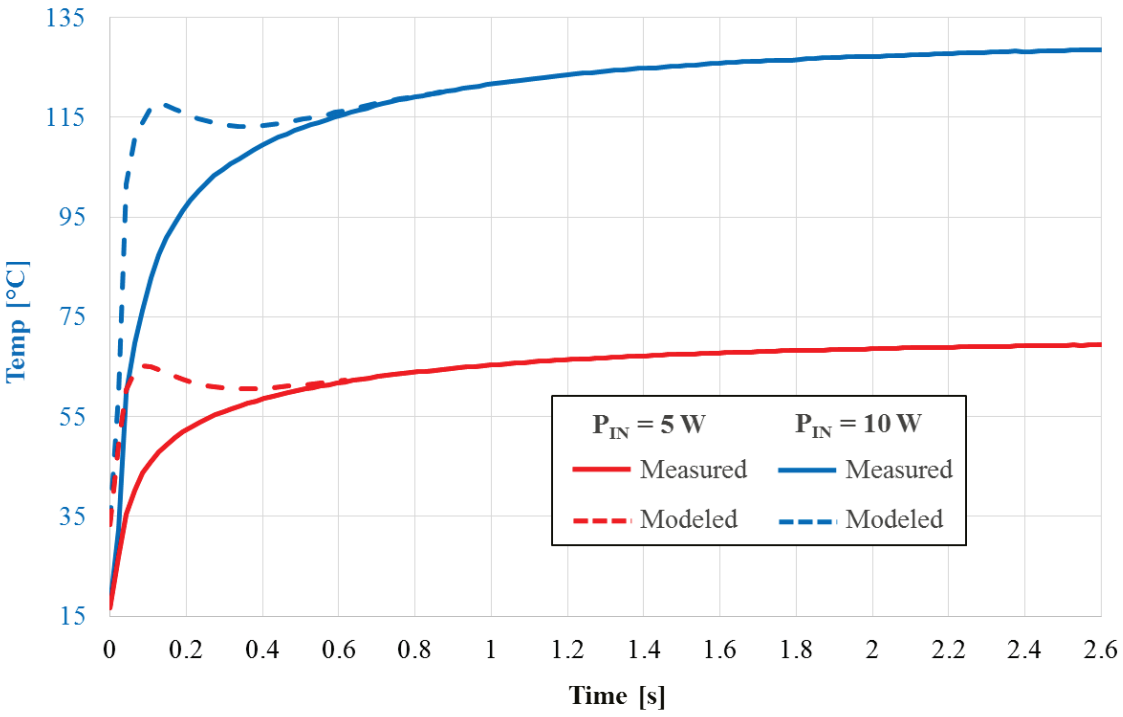


Figure 3.12 – Extrapolated transient thermal behaviour for GS66504B.

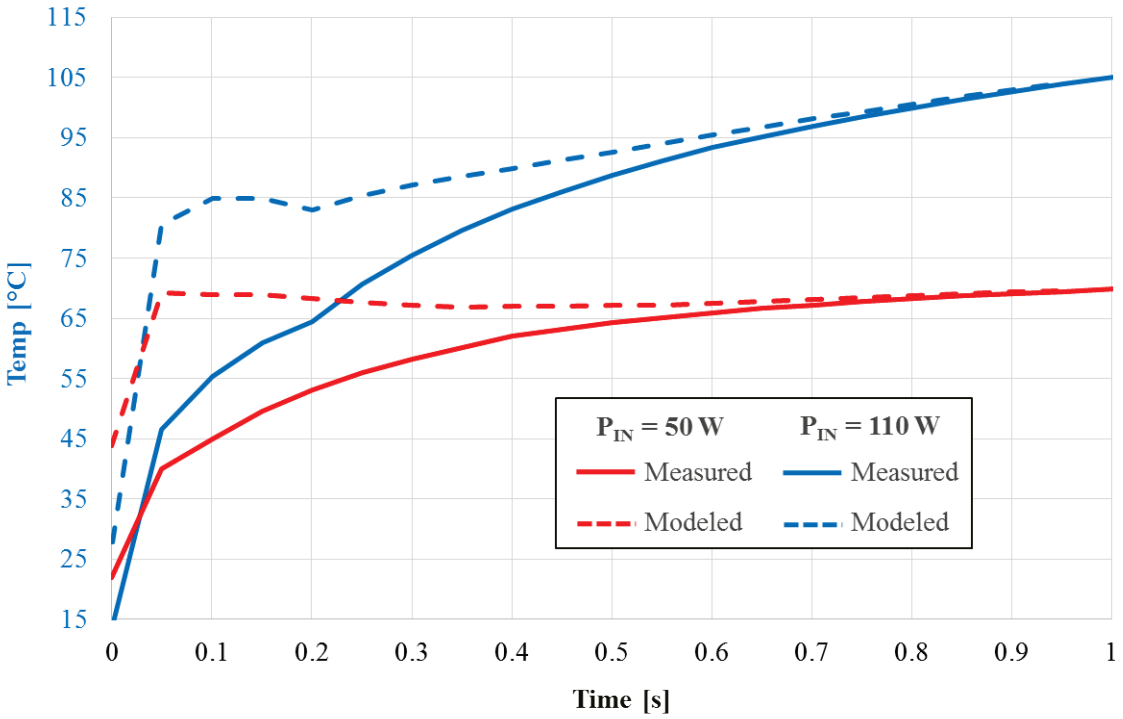


Figure 3.13 – Extrapolated transient thermal behaviour for GS66516T.

3.5 Summary

To quantify the steady state and transient thermal behaviour for the CSP GaN HEMTs, a set of experiments was designed and conducted. It was shown that even when the devices are operated well within their steady state maximum junction temperatures, the measured transient thermal rate of change exceeds published guidelines by a factor of up to 80x for a short period of time. A first order approximation was used to calculate the temporal effect of the passivation layer. It is shown that for a 5 mil thick layer of high-T_g FR4, the thermal time constant is on the order of 100 ms. This value is then used to estimate the actual channel temperature with time, which is considerably compressed, further adding to concerns about premature device damage due to thermal excursions.

CHAPTER 4 – POWER CYCLING

4.1 Statistical Methods

The discipline of reliability engineering commonly uses a graphic referred to as the 'bathtub curve' to illustrate the change in failure rate of a complex part, assembly, or product with time, as shown in Figure 4.1. According to this theory, failures are initially dominated by manufacturing or quality problems. While highly problematic for both the producer and consumer, these failures are not generally considered to be inherent to the system. The intrinsic failure period is a duration of time in which the failure rate is nearly constant. Also called the 'useful life period,' failures during this time are randomly distributed in nature and are typically attributable to multiple root causes. The final segment is wearout, during which unavoidable failure mechanisms occur. Examples would be seizing of a bearing mechanism in a cooling fan or drying of a wet-type electrolytic capacitor.

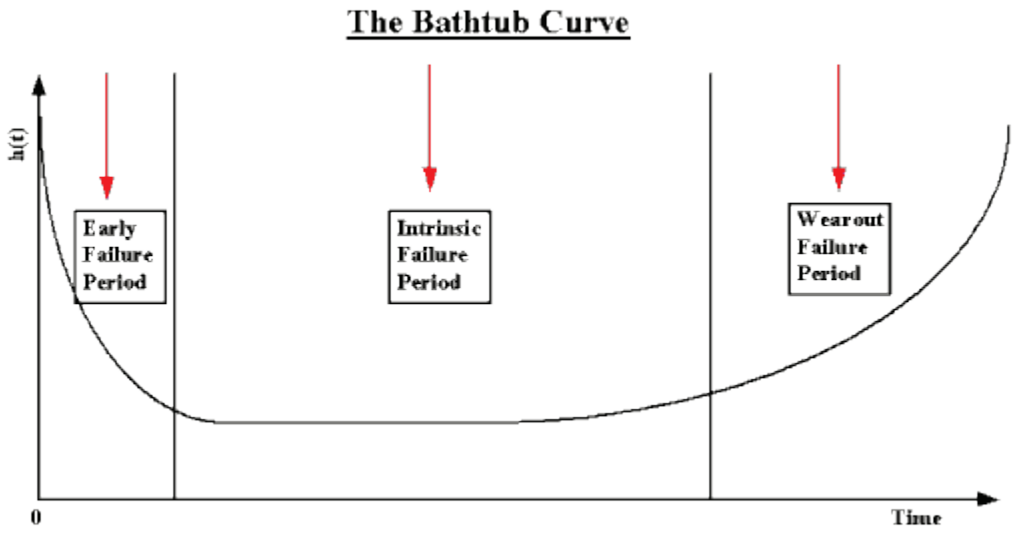


Figure 4.1 – Characteristic failure rate curve, i.e. 'bathtub curve.'

Many types of statistical distributions exist to quantify parameters associated with the phases of electronic product life. The lognormal distribution is often a good fit to early life failures, shown by

$$f(t) = \frac{1}{\sigma t\sqrt{2\pi}} e^{\left(\frac{-[\ln(t)-\mu]^2}{2\sigma^2}\right)} \tag{4.1}$$

where σ = standard deviation of the natural logarithms of the times-to-failure and , μ = mean of the natural logarithms of the times-to-failure [101].

The two-parameter exponential distribution fits the constant failure rate portion of the bathtub curve well, described by

$$f(t) = \lambda e^{-\lambda(t-\gamma)} \tag{4.2}$$

where λ = the failure rate and γ = the location parameter, which shifts the temporal portion of the distribution by a positive amount, effectively signifying that the specific failure mode will not occur prior to this time. During this phase, the instantaneous failure rate is simply

$$f(t) = \lambda e^{-\lambda t} \tag{4.3}$$

and the reliability is

$$R(t) = e^{-\lambda t} \tag{4.4}$$

For the exponential distribution only, a commonly used descriptor, the mean time to failure (MTTF) is conveniently calculated as $1/\lambda$. The normal distribution often sufficiently describes the wearout phase, and is expressed as

$$f(t) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{t-\mu}{\sigma}\right)^2} \tag{4.5}$$

where σ = standard deviation of the times-to-failure and , μ = mean of the normal times-to-failure.

However, the failure rate life cycle for many products can be described by the Weibull distribution, which employs a 'shape parameter,' typically denoted as β to encompass the logarithmic ($\beta < 1$), exponential ($\beta = 1$), and normal distributions ($\beta > 1$). The distribution is expressed as

$$f(t) = \frac{\beta}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{\beta-1} e^{-\left(\frac{t-\gamma}{\eta}\right)^{\beta}} \tag{4.6}$$

where η = the scale parameter, for which increasing values temporally elongate the distribution while decreasing the probability density function magnitude, as the area under the curve is constant. The instantaneous Weibull failure rate can be calculated by

$$\lambda(t) = \left(\frac{\beta}{t_{63}}\right)\left(\frac{t}{t_{63}}\right)^{\beta-1} \tag{4.7}$$

where t_{63} is the time at which $1 - \left({}^{1}/_{e}\right)$, or 63% of failures are expected to have occurred. In data sets which are relatively small, the method for parameter estimation are relevant. Of the available methods, the least squares, also known as rank regression is the most commonly used. However, the maximum likelihood estimation (MLE) technique is more applicable to the data in this work. MLE is a special case of maximum a posteriori estimation, which assumes a prior distribution and iterates to maximize the likelihood function. For a random variable x following a continuous probability distribution with the density function f depending on Θ, the likelihood function

$$\mathscr{L}(\Theta|x) = f_{\Theta}(x) \tag{4.8}$$

For l = average log-likelihood,

$$l = \frac{1}{n} ln\mathscr{L} \tag{4.9}$$

the maximum likelihood technique estimates Θ_0 by finding a value of Θ which maximizes $l(\Theta;x)$ [102]

$$l(\Theta|x) = \frac{1}{n}\sum_{i=1}^{n} \ln f(x_i|\,\Theta) \tag{4.10}$$

The statistical distributions and methods for parameter techniques described will be used for the remainder of this Chapter.

4.2 Failure Models and Experimental Design

Unlike standardized thermal shock testing protocols available from JEDEC and the United States military [94], [103], [104], power cycling is highly application dependent because it evaluates the device under test as part of a larger system. Published studies are available [105]–[107], some of which are specific to CSP failure modes [108]–[110]. In more traditional off-the-shelf power semiconductor packages such as TO-220, mechanical failure modes such as bond wire heel crack / liftoff and die attach solder fatigue become prevalent. However, these failure modes are not present in leadless packages like the BGA and chip scale package due to the lack of both bond wires and die attach methods. Furthermore, as illustrated in Figure 4.2, the standards are comparably benign when overlaid with a typical atomic layer deposition process used in the

semiconductor industry, commonly on the order of seconds per step [111]. When the power semiconductors used to generate power and ignite / sustain a plasma for these types of processes are subjected to 10^5 or 10^6 thermal cycles throughout a product lifetime, high cycle fatigue mechanisms become highly relevant.

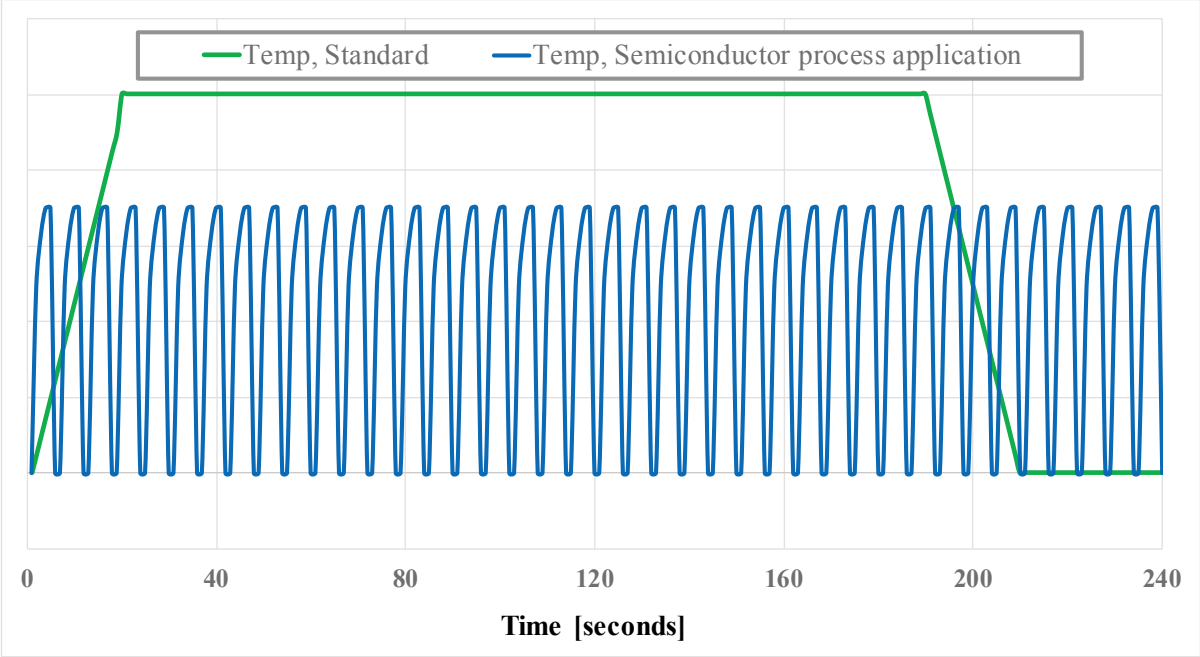


Figure 4.2 – Industry standard thermal cycling profile vs. modern ALD process.

Methods for accelerating failure modes are useful because they reduce the duration of experiments. Failures can be accelerated through increasing stressors, such as with increased temperature, voltage, current, humidity, and vibration. The Arrhenius equation is often used to model acceleration based solely on a temperature increase, such that

$$k = Ae^{-E_a/k_B T} \tag{4.11}$$

where k = rate constant, T = temperature, E_a = activation energy for the reaction, and k_B = Boltzmann constant. Acceleration due to thermomechanical fatigue is commonly expressed by the Norris-Landzberg equation, here noted in terms of an acceleration factor

$$AF = \left(\frac{f_{field}}{f_{test}}\right)^{-m} \left(\frac{\Delta T_{field}}{\Delta T_{test}}\right)^{-n} \left(e^{\frac{E_a}{k}\left(\frac{1}{T_{max,field}} - \frac{1}{T_{max,test}}\right)}\right) \tag{4.12}$$

where f = frequency of cycling, m and n = material constants (~ 0.33 and 1.9 for SnPb, respectively) [112]. The Coffin-Manson equation is an alternate method for estimating fatigue

$$Cycles\ to\ failure = A_0(\Delta T)^{-q} \tag{4.13}$$

where q is a material constant, experimentally determined values for which are summarized in Table 4.1 [113].

Table 4.1 – Empirically determined Coffin-Manson exponents for sample materials.

Material	**Exponent (q)**
Soft metals (solder, Al)	1-3
Hard metals / intermetallics	3-6
Brittle materials (dielectrics)	6-9

Also pertinent to this experimentation are models used for predicting solder fatigue. Many are available but the empirical model which has produced consistently repeatable results, especially for Pb-free solder joints is referred to as the Modified Engelmaier model [114]–[117].

The model is based on strain rate and accounts for cumulative damage and has three parts. The first is a solder strain range computation

$$\Delta \gamma = C \frac{L_D}{h_S} \Delta\alpha\Delta T \tag{4.14}$$

where γ is strain, L_D is half of the component length, h_S is the solder joint height, and $\Delta\alpha\Delta T$ is the differential thermal expansion between the component and the substrate. The second portion is a strain energy computation

$$\Delta W \cong \Delta \gamma\tau \tag{4.15}$$

where W is the strain energy density. The third part of the model is a solder fatigue equation

$$N_f = (0.0015 w_{acc})^{-1} \tag{4.16}$$

where N_f represents the cycles to failure and w_{acc} is the accumulated strain energy.

The acceleration and fatigue models are germane to the experiments conducted in this Chapter. Information gathered during thermal characterization was used to design a set of experiments with the goal of quantifying the cycles to failure under power cycling. Both the GS66504B and GS66516T were tested in thermal systems identical to those described in Chapter 3 for each device type.

4.3 Results for GS66504B

The GS66504B was tested at three stress levels: dT = 50 °C, 70 °C, and 110 °C. For the most extreme case of dT = 110 °C, failures occurred at less than 2k cycles, while the experiments run at dT = 70 °C yielded failures in the 400k cycle range. The final set of tests at dT = 50 °C was

suspended after no failures were observed at 2.4M cycles. A summary of the resultant data is illustrated in Figure 4.3. It is noteworthy that the difference between the dT = 50 °C and dT = 70 °C is approximately one order of magnitude in time to failure reduction, while between dT = 70 °C and dT = 110 °C represents two orders of magnitude. Both cases show approximately a 10x reduction in cycles to failure for a 10 °C increase in dT.

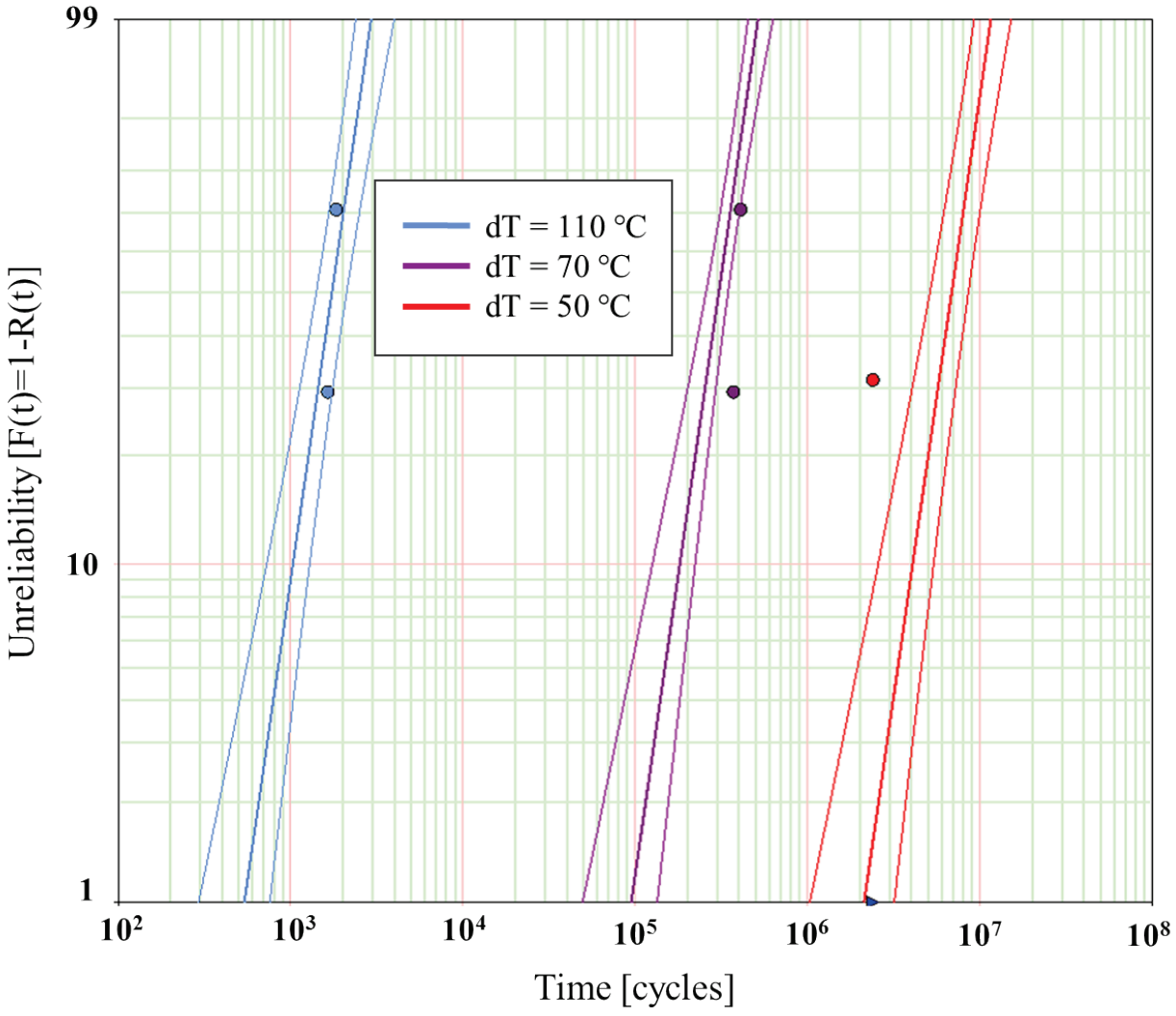


Figure 4.3 - Weibull distribution fit of dT vs. cycles across multiple use case stress levels for GS66504B.

Data plots for the dT = 50 °C case of the GS66504B are illustrated in Figures 4.4 and 4.5. The data was calculated using MLE, with the blue best fit line. The red lines are 80% upper and lower confidence bounds using the Fisher Matrix method.

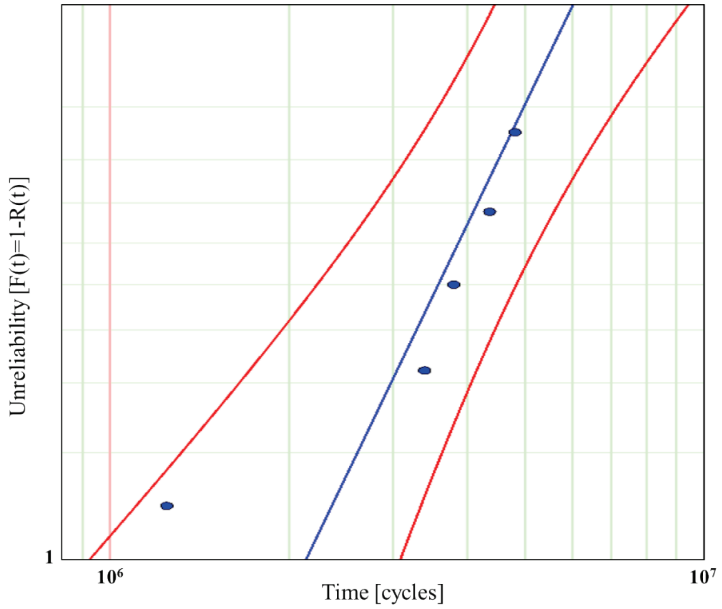


Figure 4.4 – Probability of failure for GS66504B cycling at dT = 50 °C.

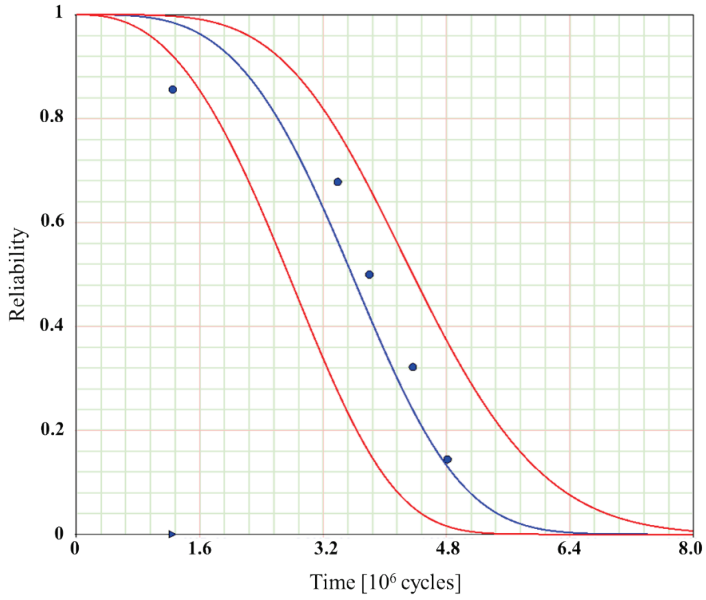


Figure 4.5 – Reliability for GS66504B cycling at dT = 50 °C.

Data plots for the dT = 70 °C case of the GS66504B is illustrated in Figures 4.6 and 4.7. The data was calculated using MLE, with the blue best fit line. The red lines are 80% upper and lower confidence bounds using the Fisher Matrix method.

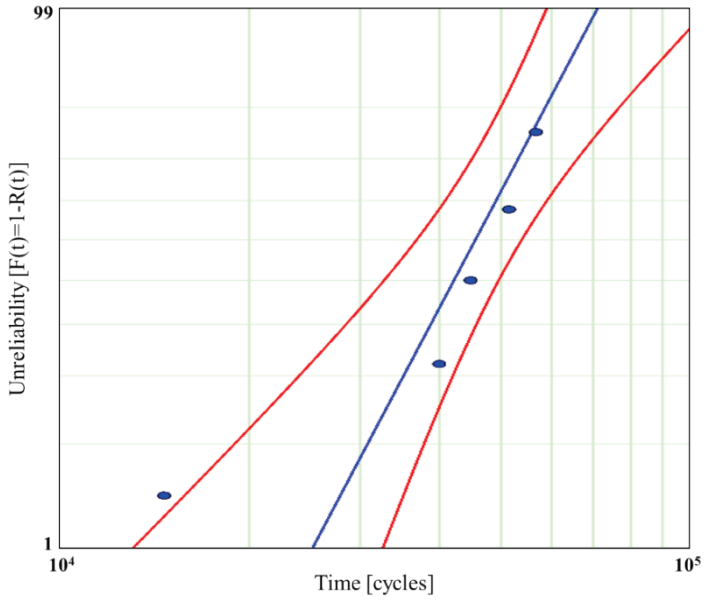


Figure 4.6 – Probability of failure for GS66504B cycling at dT = 70 °C.

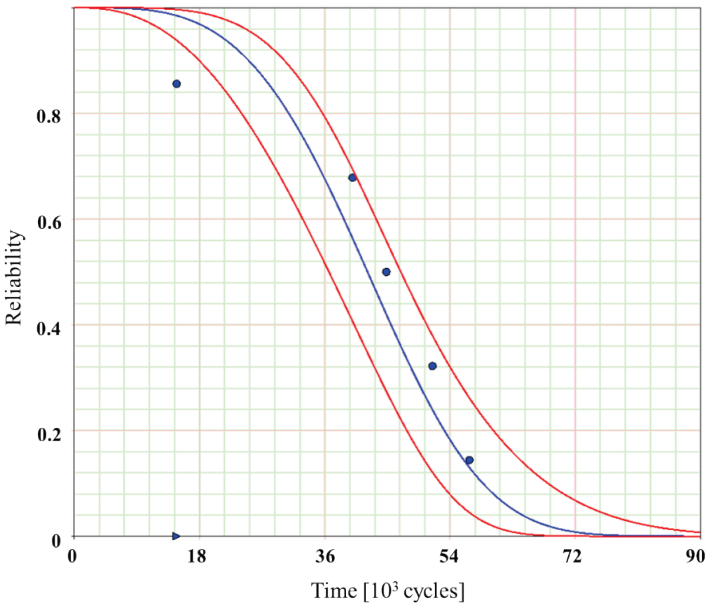


Figure 4.7 – Reliability for GS66504B cycling at dT = 70 °C.

Data plots for the dT = 110 °C case of the GS66504B is illustrated in Figures 4.8 and 4.9. The data was calculated using MLE, with the blue best fit line. The red lines are 80% upper and lower confidence bounds using the Fisher Matrix method.

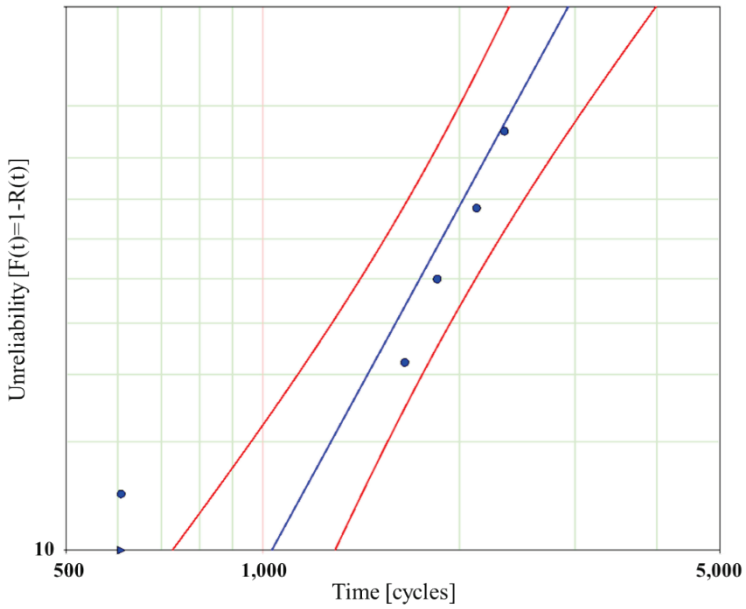


Figure 4.8 – Probability of failure for GS66504B cycling at dT = 110 °C.

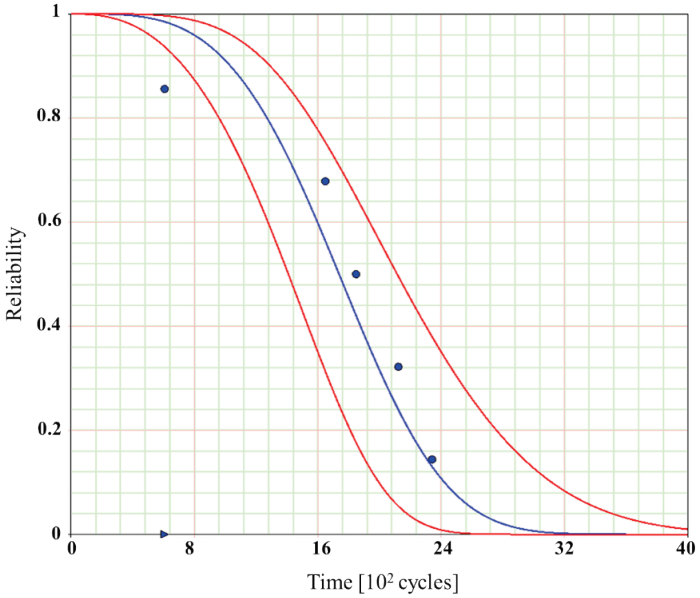


Figure 4.9 – Reliability for GS66504B cycling at dT = 110 °C.

Using the Norris Landzberg model for acceleration, the curve fit equation is

$$Cycles\ to\ failure = 1.05\ x\ 10^{16} * dT^{-5.62} \tag{4.17}$$

which is plotted as Figure 4.10, with red confidence bounds at 95%. The regression line fits a power law model very well, with an R-squared value of 0.9997. Referring back to Table 4.1, the coefficient of 5.62 is in line with mechanical strain or fatigue of a hard metal or intermetallic. Analysis using a Weibull distribution fit calculates a shape parameter (β) of 3.62 and an activation energy (E_a) for this failure mode of 1.63 eV. For reference, other early-life failure modes in semiconductors are those associated with assembly defects (0.5-0.7 eV) and contamination (~1.0 eV). The higher activation energy of the failure mode observed indicates that it has increased temperature dependence, highlighting the critical nature of dT.

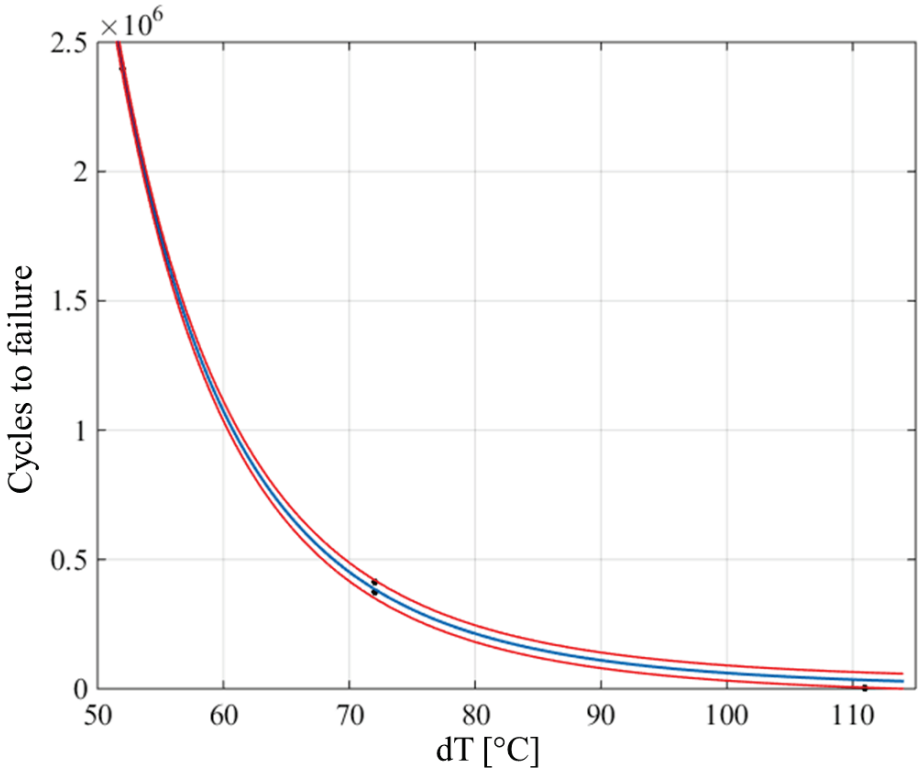


Figure 4.10 – Curve fit for GS66504B fatigue acceleration.

4.4 Results for GS66516T

Logistical constraints limited power cycling of the GS66516T to a single stress level of dT = 100 °C. The resultant time-to-failure data is shown in a two-parameter Weibull distribution fit in Figure 4.11. The β value is calculated as 3.34, with a characteristic life (η) of 11,696 cycles. The high β value is indicative of a wearout mechanism, whereas the relatively low η value suggests that power dissipation derating will be similarly critical for this package as for the GS66504B.

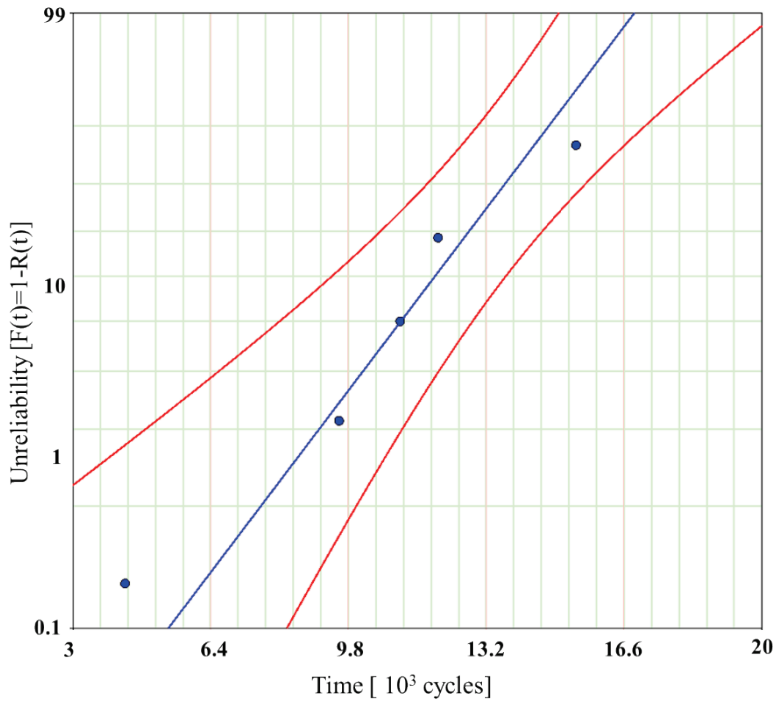


Figure 4.11 – Probability of failure for GS66516T cycling at dT = 100 °C.

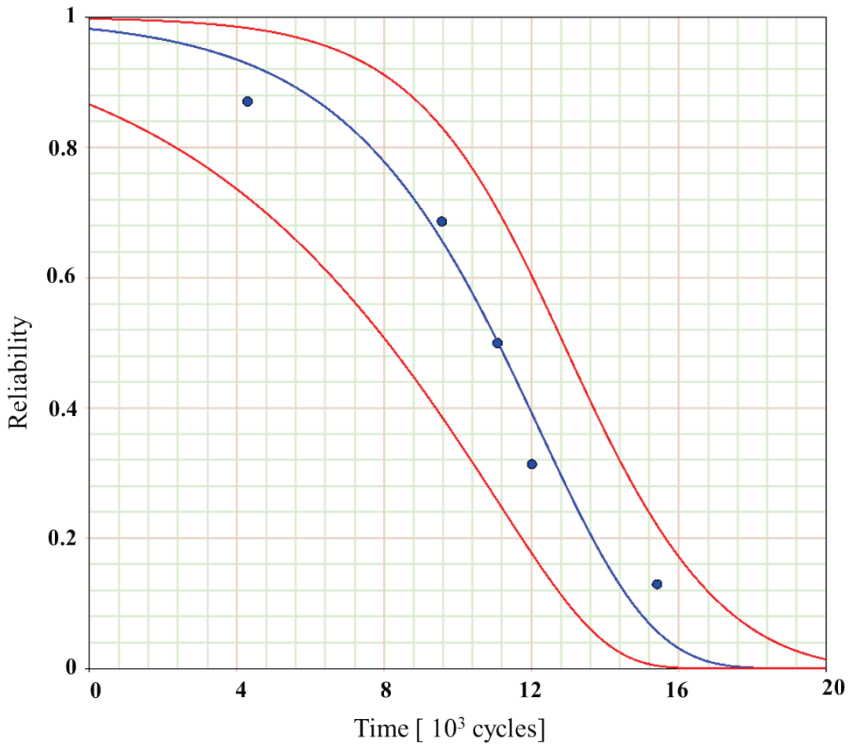


Figure 4.12 - Two-parameter Weibull distribution fit of cycles to failure vs. unreliability for GS66516T.

4.5 Summary

To quantify the thermal behaviour and power cycling times to failure for the most recent generation of COTS GaN HEMTs in CSP form factors, a set of experiments was designed and conducted. It was shown that even when the devices are operated well within their steady state maximum junction temperatures, the transient thermal rate of change is a major aggrevating factor in lowering the early life failure rate. Extrapolations predict that derating the power dissipated by a device by up to 50% may be required for long-term reliability (> 1M cycles to failure) in industrial applications.

CHAPTER 5 – CONCLUSIONS AND FUTURE WORK

The theory and results of three interlinked experiments on the topic of GaN HEMTs in chip scale packaging have been presented. The Class E radio frequency power amplifiers developed at 2 MHz and 13.56 MHz were able to produce over 1 kW at 94% efficiency. Results from thermal characterization of the HEMTs when installed in a typical system show that both types of devices have steady state thermal performance of between 0.93 °C/W and 5.27 °C/W. Transient thermal behavior as expressed in dT/dt exceeds standards by 20 to 80x. A final set of experiments demonstrates that to achieve reliability expected in industrial systems, the HEMTs evaluated require significant thermal parameter derating on the order of 50%.

Future efforts to expand on these topics could be in multiple areas. The RF amplifiers as presented may be characterized in more detail. A starting point would be load pull, which generally includes power output, efficiency, and gain as a function of load impedance presented. Power output as a function of VSWR is also an interesting and relevant measure, as well as a characterization of safe operating area over ranges of bus voltage, HEMT drain current, impedances, and ambient temperatures. The output filter topology and implementation has an appreciable effect on overall power amplifier performance; benefits to certain performance parameters would be realized using alternate filters. As mentioned previously, similar HEMTs from the same manufacturer have been shown to operate into the low VHF range, and a useful exploration into their feasibility as power amplifying devices at frequencies on the order of 100 MHz could be a natural progression. There are also commercially available devices from alternate suppliers such as Efficient Power Conversion (EPC) which could be evaluated in with similar methodologies.

The thermal tests which were conducted on the HEMTs could be extended through experimentation, first by devising additional systems in which to install and evaluate the devices. In this manner, universal thermal models would be developed for use in generalized systems. This may be more useful in the transient space, as the steady state parameters are relatively straightforward calculations. In addition, detailed simulations using FEA tools would be an improvement over the simple lumped capacitance method which was used in this work. Ideally this would involve modeling of the HEMT structure and materials, and use iterative verification with experimental data for statistical confidence.

The power cycling subtopic could be supplemented primarily with additional experimentation. Test cases with extended ΔT would assist in predictive model accuracy. Conducting the experiments for longer durations, including data points in the millions of cycles would be useful. Enhanced methods for monitoring progressive degradation and understanding the physics of failure behind each mechanism for degradation is desirable and would be recommended if possible.

Potential supplementary efforts would include direct comparisons between the GaN HEMTs evaluated and alternative technologies, the most obvious being SiC MOSFETs. Since the most recent SiC MOSFETs are intended for use at lower fundamental frequencies, such as < 500 kHz, the intended application and circuit topology would need to change from RF power amplifiers to DC-DC converters.

Regarding HEMT reliability, it is not clear to what degree the newest generation of devices is susceptible to cyclical strain and eventual fatigue due to the inverse piezoelectric effect. As mentioned previously, there have been recent efforts on this topic which focus on insertion of field

plates, minimizing initial strain through process control, and adding a high-k dielectric cap. Additional experiments designed specifically to target this failure mode would yield useful results.

Diverging from the chip scale packaged GaN HEMTs, additional work into the RF feasibility and device reliability could be undertaken for parts available in more traditional packaging, such as TO-247. Some manufacturers only make GaN HEMTs available in these packages, so studies in this manner have the potential to add to the body of knowledge through further isolation of package and device technology failure modes. Detailed parametric comparisons between specific implementations of AlGaN/GaN HEMT technology across manufacturers would also be fruitful to quantify how device design and process parameters effect results for a general technology.

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