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Through Silicon Via Field-Effect Transistor with Hafnia-based Ferroelectrics and the Doping of Silicon by Gallium Implantation Utilizing a Focused Ion Beam System

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Abstract

3-dimensional integration has become a standard to further increase the transistor density and to enhance the integrated functionality in microchips. Integrated circuits are stacked on top of each other and copper-filled through-silicon VIAs (TSVs) are the industry-accepted choice for their vertical electrical connection. The aim of this work is to functionalize the TSVs by implementing vertical field-effect transistors inside the via holes. The front and back sides of 200 ... 300 μm thin silicon wafers were doped to create the source/drain regions of n- and p-FETs. The TSVFETs showed very stable saturation currents and on/off current ratios of about 10^6 (n-TSVFET) and 10^3 (p-TSVFET) for a gate voltage magnitude of 4 V. The use of hafnium zirconium oxide on a thin SiO_2 interface layer as gate dielectric material in a p-TSVFET, enabled the implementation of a charge trapping memory inside the TSVs, showing a memory window of about 1 V. This allows the non-volatile storage of the transistor on/off state. In addition, the demonstration of the use of gallium as the source/drain dopant in planar p-FET test structures (ion implanted from a focused ion beam tool) paves the way for maskless doping and for a process flow with a low thermal budget. It was shown that ion implanted gallium can be activated and repaired at relatively low temperatures of 500 °C ... 700 °C.

Kurzfassung

Die 3-dimensionale Integration hat sich zur weiteren Erhöhung der Transistordichte und der integrierten Funktionalität in Mikrochips als ein Standard durchgesetzt. Integrierte Schaltkreise werden übereinander gestapelt und mit den industrieweit im Einsatz befindlichen Kupfer-gefüllten Silizium-Durchkontaktierungen (TSVs, Through-Silicon VIAs) vertikal elekrisch verbunden. Ziel dieser Arbeit ist die Funktionalisierung der TSVs durch die Implementierung von vertikalen Feldeffekttransistoren innerhalb der Durchgangslöcher. Die Vorder- und Rückseite von 200 ... 300 μm dünnen Silizium-Wafern wurden dotiert, um die Source/Drain Bereiche von n- und p-FETs zu erzeugen. Die TSVFETs zeigten sehr stabile Sättigungsströme und hohe ein/aus-Stromverhältnisse von etwa 10^6 (n-TSVFET) und 10^3 (p-TSVFET) für einen Gate-Spannungsbetrag von 4 V. Die Verwendung von Hafnium-Zirkonium-Oxid auf einer dünnen SiO_2-Grenzflächenschicht als Gate-Dielektrikum in einem p-TSVFET, ermöglichte die Implementierung eines Halbleiter-Ladungsfallenspeichers in den TSVs, der ein Speicherfenster von etwa 1 V aufwies. Dadurch wird die nicht-flüchtige Speicherung des ein/aus-Zustandes der TSVFETs möglich. Darüber hinaus ebnet die Demonstration des Einsatzes von Gallium für die Source/Drain-Dotierung von planaren p-FET-Teststrukturen (ionenimplantiert mit einem fokussierten Ionenstrahl) den Weg für maskenlose Dotierungen und Prozessketten mit geringem thermischen Budget. Gallium-Implantationen können bei relativ niedrigen Temperaturen von 500 °C ... 700 °C aktiviert und ausgeheilt werden.

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Zu allererst möchte ich meine Dankbarkeit gegenüber allen vom Lehrstuhl für Halbleitertechnik aussprechen. Die angenehme Arbeitsatmosphäre im gesamten Team hat immer dazu beigetragen, dass ich auch in stressigen Zeiten sehr gern zur Arbeit gegangen bin. Danke Leute, es war eine richtig tolle Zeit!

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List of Symbols

Symbol	Description
A	Area
C	Capacitance
C	Capacitance
C-V	Capacitance-voltage
C_{hf}	High frequency capacitance
C_i''	Specific insulator capacitance per area
C_{IF}	Interface layer capacitance
C_{ins}	Insulator capacitance
C_{ins}''	Specific insulator capacitance per area
C_{it}	Interface state capacitance
C_{it}''	Specific interface state capacitance per area
C_{lf}	Low frequency capacitance
C_{max}	Maximum capacitance
C_D	Semiconductor capacitance
C_i	Insulator capacitance
χ	Dielectric susceptibility
D	Displacement field
D	Diffusion coefficient
d	Contact distance
d	TSV diameter
d	Transistor distance
$D_{0,B}$	Preexponential factor for the boron diffusion coefficient
$D_{0,P}$	Preexponential factor for the phosphorus diffusion coefficient
D_0	Preexponential factor for the diffusion coefficient
$D_{Ga,Si}$	Diffusion coefficient of gallium in silicon
D_{Ga,SiO_2}	Diffusion coefficient of gallium in silicon dioxide
D_{it}	Interface state density
d_{TSV}	Diameter of the through silicon VIAs
ΔR_p	Standard deviation of projected range
ΔV	Voltage shift
E	Electric field
E	Ion Energy
E	Electric field
e	Euler's number
e	Elementary charge
E	Acceleration energy
$E_{A,B}$	Activation energy of boron
$E_{A,P}$	Activation energy of phosphorus
E_{vac}	Vacuum energy
E_c	Coercive field

Symbol	**Description**
E_C	Conduction band engery
E_F	Fermi energy
E_V	Valence band energy
ε_0	Vacuum permittivity
ε_r	Relative permittivity
$\varepsilon_{r,ins}$	Relative insulator permittivity
ε_{Si}	Permittivity of silicon
G	Conductance
g_m	Transconductance
h	Dopant layer thickness
I	Current
I-V	Current-voltage
$I_{D,off}$	Drain current in off state
$I_{D,on}$	Drain current in on state
I_{DS}	Drain-source current
I_{Ion}	Ion current
I_{off}	Diode current with reverse bias voltage
I_{off}	Transistor (drain) current in off state
I_{on}	Diode current with forward bias voltage
I_{on}	Transistor (drain) current in on state
I_D	Drain current
I_G	Gate current
I_S	Saturation current
J	Diffusion flux
J	Current density
J	Ion current density
J-V	Current density-voltage
J_{off}	Diode current density with reverse bias
J_{on}	Diode current density with forward bias
J_G	Gate Current Density
k_b	Boltzmann's Constant
L	Length of the transistor channel
L	Length of the resistor
L	Contact length
L_G	Gate length
L_T	Transfer length
m	Segregation coefficient
μ	Charge carrier mobility
μ_{FE}	Field-effect mobility
μ_n	Electron mobility
μ_p	Hole mobility
N	Particle concentration

Symbol	**Description**
N	Target atom density
n_{GOX}	Volumetric gate oxide defect density
N_0	Saturation concentration
N_A	Acceptor concentration
N_D	Ion Dose
N_D	Donator concentration
n_i	Intrinsic carrier concentration
N_P	Phosphorus concentration
P	Polarization
P-E	Polarization-electric field
P-V	Polarization-voltage
P_{sp}	Spontaneous polarization
P_r	Remanent polarization
Φ	Ion fluence or dose
ϕ_{bi}	Built-in potential
Φ_F	Fermi potential
Φ_{inv}	Inversion potential
Φ_{MS}	Metal semiconductor work function difference
Q	Pre-deposition
q	Charge
Q_{ins}	Insulator charge
Q_{it}	Interface trapped charge
Q_{ot}	Oxide trapped charge
Q_f	Fixed oxide charge
Q_m	Mobile charge
r	Potential distance from tip
R_{4pp}	Resistance obtained by 4pp measurement
R_{meas}	Resistance to be measured
R_{sh}	Sheet resistance
R_{tot}	Total resistance
R_C	Contact resistance
R_D	Drain resistance
R_p	Projected Range
R_S	Source resistance
R_W	Wire resistance
ρ	Electrical resistivity
ρ_c	Contact resistivity
$S_e\left(E\right)$	Cross-section of electronic stopping
$S_n\left(E\right)$	Cross-section of nuclear stopping
s_x	Tip distance
σ	Electrical conductivity
t	Diffusion time

Symbol	**Description**
t	Junction depth
t	Layer thickness
T	Temperature
t	Implantation time
T_{anneal}	Annealing temperature
t_{ins}	Insulator thickness
T_{max}	Maximum temperature
V	Voltage
V_{bi}	Built-in voltage
$V_{D,sat}$	Saturation voltage
V_{DD}	Drain-drain voltage
$V_{depolarize}$	Depolarization voltage
V_{DS}	Drain-source voltage
V_{ext}	External voltage
V_{FB}	Flatband Voltage
V_{GS}	Gate-source voltage
V_{SB}	Substrate bias voltage
V_{th}	Threshold voltage
V_C	Contact voltage
V_D	Drain voltage
V_F	Forward voltage
V_G	Gate voltage
V_R	Reverse voltage
V_T	Thermal voltage
W	Width of the transistor channel
W	Width of the resistor
W	Width of the barrier
W	Width of doped area
$W_{\chi,Si}$	Electron affinity of silicon
$W_{F,M}$	Metal work function
W_B	Barrier height
W_F	Work function
w_{scr}	Width of the space charge region
x	Diffusion length
x	Depth
x_j	Junction depth
Z	Contact width

List of Abbreviations

Abbreviation	Description
1T	One Transistor
1T-1C	One Transistor, One Capacitor
2D	Two Dimensional
2.5D	Two-point-five Dimensional
3D	Three Dimensional
4pp	Four point probes
AC	Alternating Current
ALD	Atomic Layer Deposition
ASE	Anisotropic Silicon Etcher
ASTM	American Society for Testing and Materials
B	Bulk / Substrate
B:μc-Si	Boron doped micro-crystalline silicon
BEOL	Back End Of Line
BHF	Buffered Hydrofluoric Acid
BL	Bit Line
CB	Conduction Band
chem.	Chemical
CMOS	Complementary Metal Oxide Semiconductors
CVD	Chemical Vapor Deposition
D	Drain
DC	Direct Current
dd	Deep depletion
DHE	Differential Hall Effect
DRAM	Dynamic Random-Access Memory
DRIE	Deep Reactive Ion Etching
ECD	Electro-Chemical Deposition
ECPR	(Ethylcyclopentadienyl)(Pyrrolyl)Ruthenium(II)
EDL	Electron Device Letters
EEPROM	Electrically Erasable Programmable Read-Only Memory
EOT	Equivalent Oxide Thickness
EPROM	Erasable Programmable Read-Only Memory
ERS	Erase
FD-SOI	Fully Depleted Silicon On Insulator
FE	Ferroelectric
FE Mobility	Field-Effect Mobility
FeFET	Ferroelectric Field-Effect Transistor
FEOL	Front End Of Line
FeRAM	Ferroelectric Random-Access Memory
FET	Field-Effect Transistor
FG	Floating Gate
FIB	Focused Ion Beam
FinFET	Fin Field-Effect Transistor
FOX	Field Oxide
G	Gate
GAA	Gate All-Around
HF	High Frequency
hf	High frequency
HKMG	High-k Metal Gate
HZO	Hafnium Zirconium Oxide
IC	Integrated Circuit
ICP	Inductively Coupled Plasma

Abbreviation	Description
IEEE	Institute of Electrical and Electronics Engineers
IF	Interface layer
IGFET	Insulated Gate Field-Effect Transistor
IHM	Institute for Semiconductors and Microsystems
IITC	International Interconnect Technology Conference
IS-TSVFET	Ion Sensitive Through Silicon VIA Field Effect Transistor
Kapton	Polyimide foil
LDD	Lightly Doped Drain
lf	Low frequency
Litho	Lithography
LOCOS	Local Oxidation of Silicon
LSS	Lindhard-Scharff-Schiott (Model)
MALab	Material Analysis Lab
MFIS	Metal-Ferroelectric-Insulator-Semiconductor
MFMIS	Metal-Ferroelectric-Metal-Insulator-Semiconductor
MHOS	Metal/HfO_2/Oxide/Silicon
MIM	Metal Insulator Metal
MIS	Metal Insulator Semiconductor
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MRAM	Magnetoresistive Random-Access Memory
MW	Memory Window
NAND	Not AND
NMOS	Metal Oxide Semiconductor using electron conduction
NMP	N-Methyl-2-pyrrolidone
PcRAM	Phase-change Random-Access Memory
PD-SOI	Partially Depleted Silicon On Insulator
PE-ALD	Plasma Enhanced Atomic Layer Deposition
PE-CVD	Plasma Enhanced Chemical Vapor Deposition
PL	Plate Line
PLD	Pulsed Laser Deposition
PMOS	Metal Oxide Semiconductor using hole conduction
PRG	Program
PVD	Physical Vapor Deposition
PZT	Lead Zirconium Titanate
qs	Quasi-static
RC delay	Resistance-Capacitance delay
ReRAM	Resistive Random-Access Memory
RF	Radio Frequency
RIE	Reactive Ion Etching
ROM	Read-Only Memory
RTA	Rapid Thermal Anneal
RTP	Rapid Thermal Processing
S	Source
S/D	Source/Drain
SALICIDE	Self-Aligned Silicide
SBT	Strontium Bismuth Tantalate
SCR	Space Charge Region
SCS	Semiconductor Characterization System
SEM	Scanning Electron Microscopy
sim	Simulated
SIMS	Secondary Ion Mass Spectrometry
SISC	Semiconductor Interface Specialists Conference

Abbreviation	**Description**
SMU	Source Measure Unit
SOD	Spin-On Dopants
SOI	Silicon On Insulator
SONOS	Silicon/Oxide/Nitride/Oxide/Silicon
SRAM	Static Random-Access Memory
SRIM	The Stopping and Range of Ions in Matter (Software)
SRP	Spreading Resistance Profiling
STI	Shallow Trench Isolation
T1	Transistor 1
T2	Transistor 2
TCAD	Technology Computer Aided Design
th.	Thermal
TLM	Transmission Line Method
TMA	Tri-Methyl Aluminium
TMB	Trimethylborane
TEMAHf	Tetrakis(EthylMethylamido)Hafnium(IV)
TEMAZr	Tetrakis(Ethylmethylamido)Zirconium(IV)
TSC	Through Silicon Capacitor
TSV	Through Silicon Vertical Interconnect Access
TSVFeFET	Through Silicon VIA Ferroelectric Field Effect Transistor
TSVFET	Through Silicon VIA Field Effect Transistor
UPS	Ultraviolet Photoelectron Spectroscopy
VB	Valence Band
VIA	Vertical Interconnect Access
WL	Word Line
XPS	X-Ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction
ZyALD	Zirconium precursor for Atomic Layer Depositions from Air Liquide
RD	LTspice parameter for the drain resistance
RS	LTspice parameter for the source resistance
TOX	LTspice parameter for the gate oxide thickness
TPG	LTspice parameter for the gate type
U0	LTspice parameter for the charge carrier mobility
VTO	LTspice parameter for the threshold voltage

1 Introduction

Today's society is accustomed to permanent accessibility, digitalized instant messaging and access to knowledge at all times. Mobile devices such as smartphones, tablets and smart watches play a very important role in this respect – 7.5 billion smartphones have been sold in the last 5 years alone [1]. The integrated ICs (Integrated Circuits) used in these devices are highly performant and offer various functionalities. This includes a central processing unit (CPU), memory for data processing and storage and chips for wireless connectivity and for the global positioning system satellites (GPS). Furthermore, Micro-Electro-Mechanical Systems (MEMS) such as accelerometers, gyroscopes, pressure sensors and image sensors (digital camera) give these hand-held devices their multifunctional character [2].

Since mobile devices should be operational for at least one working day, a correspondingly large battery is required, taking up most of the space behind the display. Only a small portion is left to implement all the functions mentioned before. One way to overcome this, is to put many features into one chip – the CPU chip often includes a graphics processing unit (GPU) and wireless connectivity functionality, as seen in Qualcomm's Snapdragon [3], Apple's A-Series [4] and HiSilicon's Kirin processors [5]. Additionally, chips are stacked on top of each other, as commonly done with DRAM (Dynamic Random-Access Memory) and the central processing unit. Through silicon VIAs (TSVs, VIA – Vertical Interconnect Access) are used as vertical copper-filled connections, providing short links that bring increased chip–to–chip performance and a higher integration density, while reducing the overall energy consumption [6], [7].

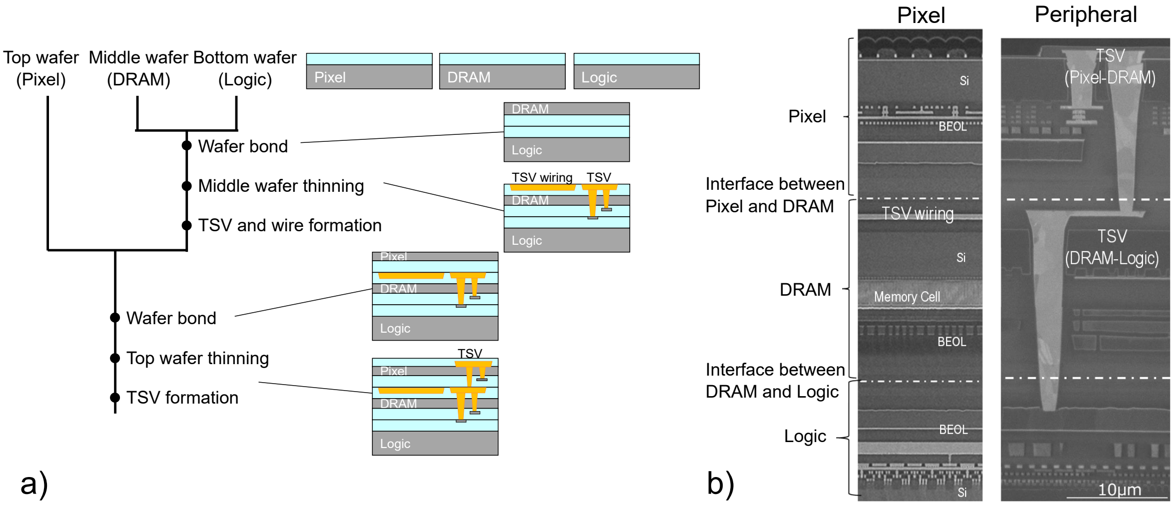


Fig. 1.1: Sony 3-layer image sensor with TSV technology a) Process flow for the chip stacking b) Cross sections of the stacked chips, reconstructed from [8]

This trend of a heterogeneous integration with various features in one IC or the stacking of chips is called the "More than Moore" path and TSVs play an important role. A prominent example for this kind of 3-dimensional chip integration is an image sensor, introduced by Sony in 2017 [8]. It is comprised of a stack of three different ICs. The pixel layer (collecting light) is placed on top of DRAM memory (temporary pixel information storage) and a logic chip (data processing). All three were fabricated separately and later stacked on top of each other and connected by TSVs, as it is depicted in Fig. 1.1. The interposed DRAM increases the output speed of the pixel information and enables super slow motion videos with 960 frames per second, while still saving lateral space due to the stacking.

In contrary, the miniaturization of structure sizes (*down-scaling* of widths, lengths and thicknesses), is known under the expression "More Moore" [9]. This path of developments is named after Gordon E. Moore, who formulated an empirical law in 1965, stating the doubling of the number of integrated components (e.g. transistors) in an IC every year. Since structural scaling is reaching its limits and the performance is not necessarily improved anymore [10], the stacking of integrated circuits could be one way to keep Moore's Law effectively alive and to further raise the volumetric transistor density by placing it in the third dimension.

The major objective of this work is the functionalization of the through silicon VIAs. Invented as an electrical connection, further applications should be made possible for the TSVs. The integration of through silicon capacitors (TSCs, see Fig. 1.2) has already been discussed for the use in power delivery systems to limit voltage peaks and ensure current integrity [11]. The use of the TSVs as optical waveguides by filling them with transparent polymers (depicted in Fig. 1.3) is also a current topic of research [12].

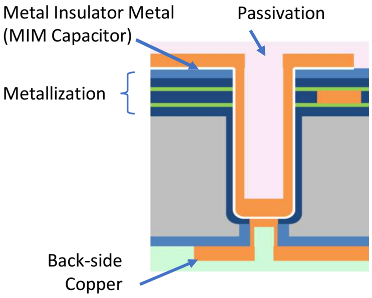


Fig. 1.2: The realization of a through silicon capacitor, from [11]

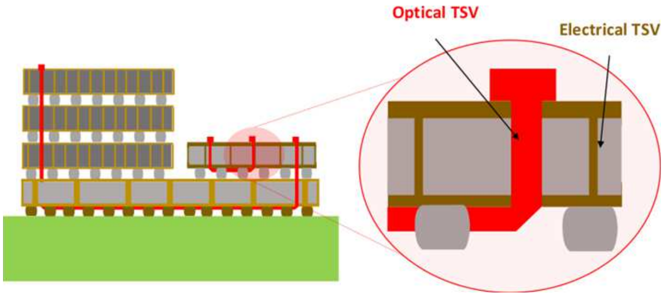


Fig. 1.3: Schematics of TSVs filled with an optically transparent polymer, from [12]

The integration of a field-effect transistor inside the through silicon VIAs (***TSVFET***) is one main goal of this thesis. It makes the VIA switchable and offers the possibility for new applications. As one example, the TSVFET could be used to easily activate or deactivate stacked ICs (partially or completely) by controlling their connection to the power supply. The implementation of the FET as a trapping or ferroelectric switching memory should also be demonstrated, which would allow the non-volatile programing of the state of conduction (on/off), holding it without the constant application of a (gate) voltage.

In order to achieve these goals, processes of microelectronics manufacturing must be used for the integration of the new devices. The fabrication should be simple, cheap and realizable in the cleanroom of the IHM (Institut für Halbleiter- und Mikrosystemtechnik, engl. Institute for Semiconductors and Microsystems) at TU Dresden. The implementation of a MOSFET (Metal Oxide Semiconductor FET) in a TSV requires specific doping structures. A significant part of this dissertation therefore covers the doping of silicon from spin-on or pre-deposited films and the corresponding drive-in process. A novelty investigated and applied here is the gallium doping by the implantation from a FIB (Focused Ion Beam) system. In summary, this work should give detailed insights on the processing of the transistors and the discussion of the resulting electrical performance.

This dissertation is organized as follows:

In chapter 2, first the basic working principles of field-effect transistors and their technological advancements are described. This is followed by an overview of semiconductor memories with a focus on ferroelectric materials. Furthermore, the 3-dimensional integration by the use of through silicon VIAs is reviewed. The chapter is closed with a basic discussion of the doping of silicon – including thermal diffusion and ion implantation.

The electrical characterization methods used in this work are introduced in chapter 3. This includes four-point probes measurements, contact resistivity measurements (use of transmission line method – TLM – structures), the determination of doping concentration profiles (differential hall effect – DHE – method) and capacitance–voltage measurements and their interpretation. Basic transistor measurements of the output and transfer characteristics and their interpretation are also part of the chapter.

Chapter 4 is dedicated to describe the idea of the TSV field-effect transistor. Planar transistor structures, used as a test vehicle to investigate different dielectrics, metals and dopings are also discussed.

In chapter 5.1, first the doping by thermal diffusion from thin films (Phosphorus n-doping with spin-on dopants and Boron p-doping from micro-crystalline silicon) is investigated as a prerequisite for the manufacturing of active devices. Then, the manufacturing of n- and p-TSVFET is discussed in detail and the electrical characterization of the devices and simulations in LTspice, TCAD and Ginestra$^{\text{TM}}$ are presented.
In 5.2, ferroelectric p-MOS field-effect transistors are investigated on planar test structures and this knowledge is transferred to the TSVFET structure to build a memory device inside the through silicon VIAs.
In 5.3, the use of gallium for the doping of silicon is studied. Implantations from a FIB system are discussed as an alternative low-temperature integration flow. Moreover, the co-integration of TSVFETs and copper-filled TSVs is proposed.

Finally, chapter 6 summarizes the results and presents an outlook for a continuation of this work.

2 Fundamentals

2.1 Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

A MOSFET (Metal Oxide Semiconductor Field Effect Transistor) consists of two heavily doped regions and a moderately doped well (or substrate) in between (see Fig. 2.1). The highly doped regions are called source and drain (S/D) and the area in between is the channel area. A dielectric material is needed for such an insulated gate FET (IGFET) which insulates the gate contact above the channel (originally SiO_2). The distance between source und drain is the channel length L and the width W is defined by the lateral dimensions of the highly doped regions. For CMOS (Complementary Metal Oxide Semiconductors), both n- and p-MOSFETs are needed and are made of $n^{(+)}$ S/D doping with a p well and $p^{(+)}$ S/D doping with an n well, respectively. In the conductive state, n-MOSFETs use electron conduction, whereas p-MOSFETs use hole conduction.

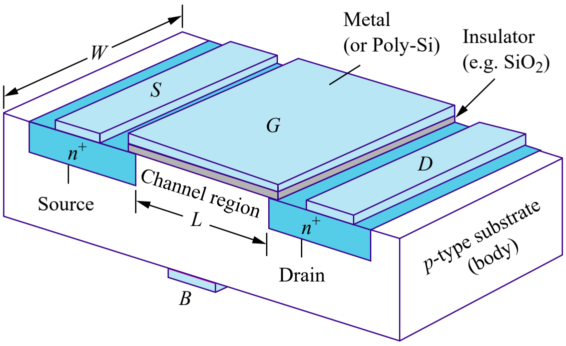


Fig. 2.1: Structure of an n-MOSFET, from [13]

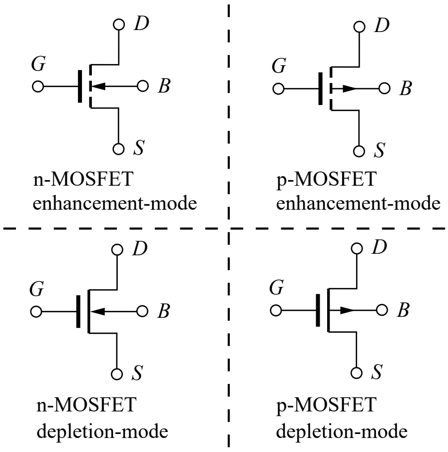


Fig. 2.2: IEEE Standard MOS transistor circuit symbols, from [13]

The circuit symbols of enhancement (normally off) and depletion (normally on) mode n- and p-MOSFETs are shown in Fig. 2.2. The MOSFET is a voltage controlled device. There are 4 terminals – source, drain, gate and bulk (the well or body or substrate). The voltage applied to the bulk terminal determines the potential in deeper regions of the semiconductor and has an influence on the threshold voltage of the device. Source and drain form pn junctions with the well region, which involves the corresponding space charge regions. Ideally, there is no current flowing, when a drain-source voltage V_{DS} is applied to an enhancement type FET. However, the channel becomes conductive when a sufficiently high gate-source voltage V_{GS} (or short V_G) is applied – with a positive polarity for an n-channel and negative polarity for a p-channel – and a vertical electrical field is present. This capacitive modification of the channel conductance is caused by the so-called field effect.

The Field Effect

The gate dielectric forms a MOS capacitor above the channel region with the gate contact and the well as electrodes. When V_G is applied at the gate, the amount of charge at the gate is compensated in the channel. Depending on the voltage, the state of accumulation, depletion and inversion can be achieved.

For an n-MOS transistor (p-doped body), positive majority charge carriers (holes) are attracted and pulled towards the *Si–Insulator* interface for negative gate voltages $V_G < 0$ – this state is called *accumulation*. There is no conduction between source and drain, since the pn junctions between the p- and n^+-regions block the current.
A *depletion* of the majority charge carriers occurs for small positive gate voltages. The positively charged holes are pushed away from the interface and immovable negatively charged doping ions remain. For higher gate voltages, the depletion layer reaches deeper into the substrate and includes more ions that compensate the charges on the gate electrode.
A further increase of the gate voltage V_G leads to a charge injection of electrons from the source and drain areas. This characteristic value is called the threshold voltage V_{th}. These mobile minority charge carriers form a conducting channel along the *Si–Insulator* interface. In this state of strong *inversion*, a conducting channel connects source and drain. The application of a drain–source–voltage V_{DS} leads to a current across that low-ohmic path.

2.1.1 Historical Development – Technological Advancements

Gordon E. Moore stated a prediction in 1965, known as Moore's Law [9]. One part concerns the device density of integrated circuits, that is expected to double every year for the next 10 years ("number of components per integrated function"). It was later revised and still holds up to this day, describing a doubling rate of every 18-24 months [14]. This miniaturization is characterized by down-scaling of transistor nodes and the use of new technologies and materials.

One of the main reasons to make transistors smaller is the reduction of manufacturing costs. A higher number of ICs (Integrated Circuits) fabricated on a wafer (batch processing) means lower expenses per IC. Additionally, the device performance increases when its key dimensions are scaled, which are the channel length L, width W and the insulator thickness. This way, the channel resistance stays the same but gate capacitance is reduced, which leads to lower RC delay and faster switching speeds [15]. This changed about 10 years ago – the reduction of the device dimensions does not necessarily result in performance improvements (higher switching frequencies) anymore, since the interconnect RC delay plays a more significant role and is not scaling with downsizing (it is rather increasing) [10].

The introduction of self-aligning processes played a significant role in down-scaling. Replacing the Al metal gate with poly-Si enabled a self-aligned gate process by implantation, reducing "Miller capacitances" by eliminating the gate-source/drain overlap [16]. The isolation of adjacent transistors, initially done by LOCOS (Local Oxidation of Silicon) [17], was replaced by the less area-consuming STI (Shallow Trench Isolation) [18]. The use of spacer technologies lead to lightly doped drain (LDD, reduction of device degradation due to hot electrons) [19], SALICIDE (Self-Aligned Silicide) [20] and self-aligned contacts (higher contact yield) [21]. Further improvements were developed to reduce short-channel effects such as junction leakage (higher doping levels, retrograde wells, "halo" doping [22]) or velocity saturation (strained silicon by an additional SiGe layer [23]). Fig. 2.3 summarizes several of these advancements.

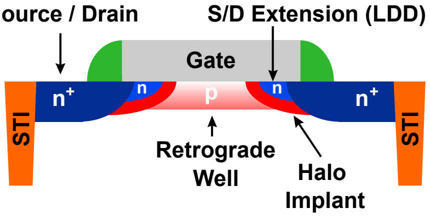


Fig. 2.3: MOSFET advancements, from [24] (modified)

Transistors on SOI (Silicon On Insulator) wafers especially reduce the parasitic capacitance in the channel region and lower junction leakage currents can be achieved due to the isolation from the bulk Si. After partially depleted SOI devices (PD-SOI), fully depleted SOI (FD-SOI) transistors are now used in a high number of products [25]. In the case of FD-SOI, the Si device layer is very thin and holds a very low amount of mobile charges (often intrinsic / undoped). The off current is extremely low and a lower amount of charge is needed on the gate to switch the transistor on – this approach is mostly used for ultra-low power applications [26].

The gate insulation layer was originally made of SiO_2 (gate oxide), later silicon oxynitride (SiON) was chosen for a thickness <3 nm to increase the dielectric permittivity of the gate insulator and to eliminate boron penetration from p^+ Si gates [27]. When Intel reached its 65 nm manufacturing node, the gate oxide thickness could not be further reduced due to high gate leakage because of direct tunneling through the insulator (compare Fig. 2.4). By using high-k dielectric materials, the physical thickness of the insulator could be increased or kept at a sufficiently high value without a reduction of the capacitance. For the 45 nm node, SiON was replaced by a hafnium-based material with an EOT (equivalent oxide thickness, $EOT = (k_{SiO_2}/k_{high-k}) \cdot t_{high-k}$) of 1.0 nm, reducing gate leakage by a factor of >25 x [28]. Metal gate electrodes had to be reintroduced to eliminate the problems of carrier depletion within the poly-Si gate and mobility degradation effects due to phonons coming from dipole vibrations in the high-k [29]. However, an SiO_2 interface (IF) layer is still necessary (often chemically grown) underneath the high-k dielectric for various reasons. It acts as nucleation layer for the atomic layer deposition (ALD) of HfO_2 [30], [31] and offers a channel interface of high quality and high reliability [32].

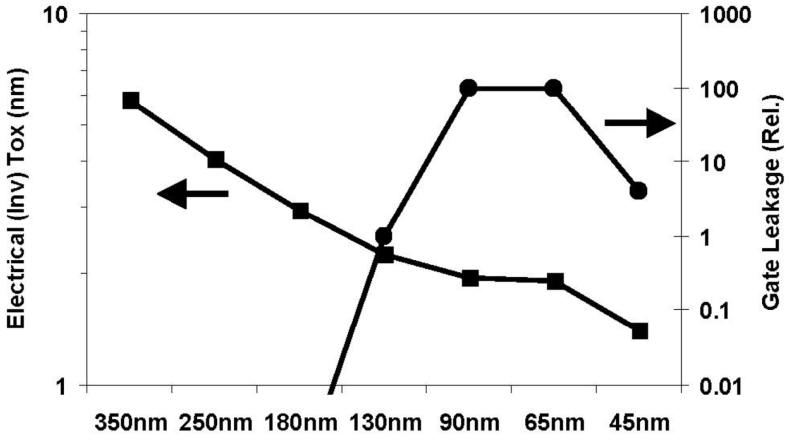


Fig. 2.4: Intel scaling trend for the gate oxide thickness Tox, from [28]

Atomic layer deposition offers an extremely good step coverage and a precise control over the deposited film thickness in the range of an atomic mono layer [35], [36]. Thus, ALD processes became an enabler for the coating of features of extremely small size and 3-dimensional structures, relying on the repeated use of saturating reactions of two or more separately provided precursors [33], [34].

For a better electrical control over the channel, structural changes were made. Multi-gate transistors such as state-of-the-art “FinFETs” have a tri-gate structure, surrounding the channel not only from one but from three sides [37], [38], which is reducing S/D leakage. Further developments will most probably bring gate all-around transistors (GAA) in the form of Si “nanosheets” [39], [40].

As explained, the introduction of HfO_2 as the gate dielectric material was a very important step to keep Moore’s Law and down-scaling alive. The transition to high-k gate dielectrics also brought the possibility of an easy functionalization of these extremely scaled devices by replacing the high-k with different materials, such as charge-trapping stacks or non-linear dielectrics like ferroelectrics. This will be further discussed in chapter 2.1.2.

Placement of this Work

In this work, some of the newest technological advancements were used to realize totally new concepts for the integration of field-effect transistors. Dimensional down-scaling (meaning gate length L and width W) of transistors was not the goal. Instead, this work implements new functionality by structural changes and the application of new materials. A completely new FET structure inside through-silicon VIAs (TSVs) was implemented (see especially chapters 4.1 and 5.1.2 and 5.2.2), converting metal-filled plugs into switchable connections (TSV basics described in chapter 2.2). This 3D vertical FET could only be fabricated by the use of ALD processes for depositions in these high aspect ratio structures. Furthermore, functionalzied high-k (ferroelectic hafnium-zirconium-oxide) metal gate (TiN) transistors (HKMG) with an SiO_2 interface layer were investigated in terms of ferroelectric switching endurance on p-FET devices with large gate lengths (several tens of μm). Additionally, the demonstration of source/drain doping by the implantation of gallium from a focused ion beam tool is a new approach and extends the range of materials used for the integration in FETs. It could basically allow the creation of doped structures by mask-less direct writing.

2.1.2 Field-Effect Transistors in Semiconductor Memories

The storage and preservation of information has always been of high importance in human history. The focus shifted from written information transmission on clay tablets or later on paper to purely digital platforms. The data to be processed, have to be temporarily or permanently stored for the use in systems with information processing units. For the use in CMOS devices, data are stored as “words” composed of a binary state of logical “1” and “0”.

Field-effect transistors have been used in various semiconductor memories of different type and function. In **ROM** (Read-Only Memory), the programming is done by design and the (non-changeable) information is stored in the IC. This can be done by field oxide programming (thick or thin SiO_2 over the active area), implantation (additional channel doping for normally on transistors) or programming by contact hole etching. **SRAM** (Static Random-Access Memory) cells in CMOS are usually made of six FETs – four n-MOS and two p-MOS transistors – and the information is directly stored in two cross-coupled inverters. The information is lost when the electrical power is switched off, therfore *volatile*. SRAM offers very fast read and write, but the cells are very large (150 F^2, where F is the minimum manufacturing feature size) [41]. Another type of volatile memory is **DRAM** (Dynamic Random-Access Memory). The information is stored in a capacitor (charge storage), that is connected to a transistor. This architecture is called *1T–1C*. A periodic refresh is needed, since a silicon FET provides a low barrier height of 1.1 eV (band gap) and the charge cannot be held for long. The size of the DRAM cells is much smaller compared to SRAM (6 F^2 with open bit line architecture), but the operation is slower, due its dynamic nature [41].

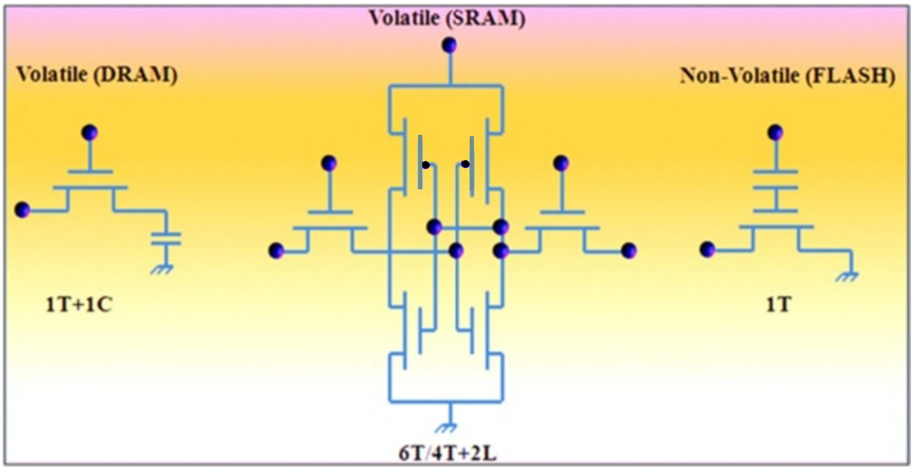


Fig. 2.5: Circuitry structures of DRAM, SRAM and Flash memory, from [42] (modified)

The non-volatile semiconductor memories can be divided in classical and emerging memories. Classical non-volatile flash memories use a floating gate (FG) or rely on charge trapping layers (SONOS – Silicon/Oxide/Nitride/Oxide/Silicon) – their basic gate stacks are depicted in Fig. 2.6. Floating gates have now been used for more than 30 years and were already introduced in *EPROM* (Erasable Programmable Read-Only Memory) and *EEPROM* (Electrically Erasable Programmable Read-Only Memory) memories [43]. Both approaches are still used in fabrication [44], but its integration simplicity gave rise to bandgap engineered SONOS stacks with additional blocking layers for retention improvements [45], [46]. Due to its commonly used NAND (Not AND) architecture (use of "pages" as smallest entity and the series connection of memory cells) the transition to layered 3D flash ("V-NAND") with a rising layer count and a very high cell density was a relatively straight forward advancement [47], [48].

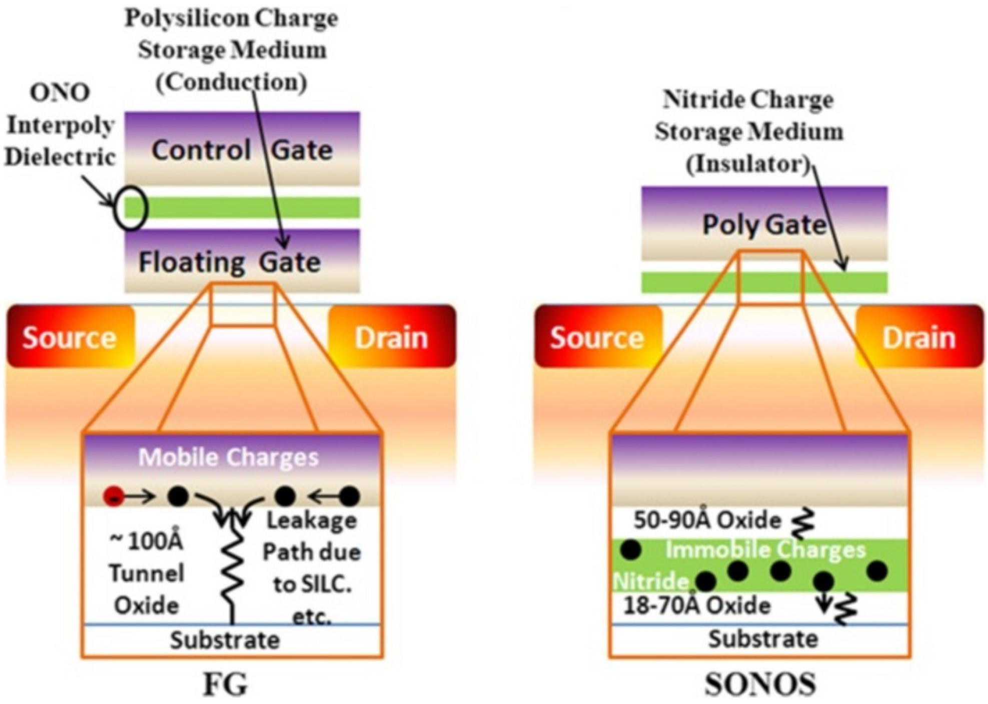


Fig. 2.6: Floating gate and charge trapping SONOS FETs, from [42]

HfO_2, the high-k dielectric gate material commonly used in state-of-the-art MOSFETs, has also been investigated as a trapping material. An MHOS (metal–HfO_2–SiO_2–Si) stack shows charge trapping, thus shifting the threshold voltage depending on the amount of trapped charges. When the interface oxide layer is thick enough to prevent instant de-trapping (e.g. 3 ... 4 nm [49]), the charge can be stored and the gate stack can be used in a memory device [50], [51].

Emerging memories include MRAM (Magnetoresistive RAM), PcRAM (Phase-change RAM), ReRAM (Resistive RAM) and FeRAM (Ferroelectric RAM) [41], [52], [53]. All those non-volatile memories are based on different switching effects and usually require materials which are incompatible with standard CMOS technology. Since ferroelectric materials have been used and investigated in this work, these will be discussed in more detail.

Ferroelectric Memories

Two distinct states are needed to store the logic states "0" and "1" in a material used in a memory device. Ferroelectric materials show a non-linear polarization-voltage behavior. An external electric field can be used to modify the spontaneous polarization. The electric displacement field D describes the response of a dielectric material in the presence of an electric field E and can be expressed as:

$$D = \varepsilon_0 E + P \tag{2.1.1}$$

where ε_0 is the vacuum permittivity and P the dielectric polarization. P is usually linearly dependent on the applied E field, but in ferroelectric materials, a non-linear history-dependent polarization can be observed. A typical polarization-voltage curve is depicted in Fig. 2.7. Additionally, a spontaneous polarization P_{sp} has to be added to the linear part:

$$P = \varepsilon_0 \chi E + P_{sp} \tag{2.1.2}$$

The combination of equations 2.1.1 and 2.1.2, leads to:

$$D = \varepsilon_0 \left(1 + \chi\right) E + P_{sp} = \varepsilon_0 \varepsilon_r E + P_{sp} \tag{2.1.3}$$

where where χ is the dielectric susceptibility and ε_r the relative dielectric permittivity.

Traditional perovskite materials, such as strontium bismuth tantalate (SBT) or lead zirconium titanate (PZT), suffer from H_2 damage and diffusion problems and need to be encapsulated. These materials and associated electrode systems have been extensively optimized to achieve compatibility in CMOS integration, specifically concerning reliability and processability using small thermal budgets [54]. The discovery of a ferroelectric phase in doped hafnium oxide by Böscke et al. [55] brought full CMOS compatibility, scalability and stability. The common understanding is, that the doping (typical dopants are Si, Al, Gd and others [54]) stabilizes an orthorhombic phase after annealing at an elevated temperature (see Fig. 2.8). From X-ray diffraction (XRD) measurements, this non-centrosymmetric phase is responsible for the ferrelectric properties. A tetragonal phase is responsible for anti-ferroelectric behavior (pinched P-E hysteresis) – cubic and monoclinic phases are associated with paraelectric P-V characteristics [56].

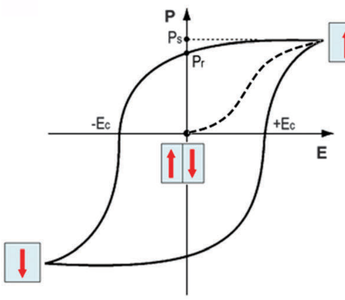


Fig. 2.7: Polarization hysteresis (P-E or P-V with $E = \frac{V}{thickness}$), P_s is the saturation polarization, P_r the remanent polarization and E_c the coercive field, from [57]

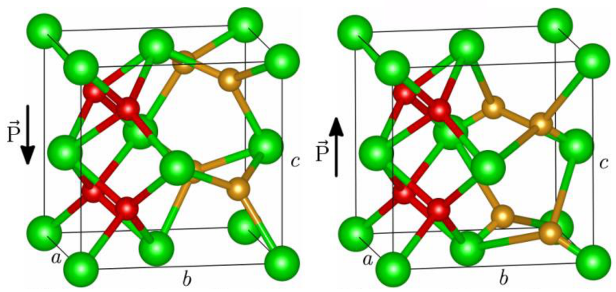


Fig. 2.8: Simulated stabilized unit cell of the ferroelectric orthorhombic phase in hafnia – hafnium atoms are green, oxygen atoms are indicated in red and golden, indicating the two polarization states, from [56]

Doping is done in the range of a few atomic percent. For the use of Si as the dopant, paraelectric behavior is observed up to $3\,\mathrm{at}-\%$, up to $4.4\,\mathrm{at}-\%$ the material is ferroelectric and for a further increase in the doping concentration, an anti-ferroelectric behavior can be observed. Due to these low doping concentrations, slight fluctuations due to manufacturing process deviations could already lead to unexpected film properties. Ferroelecticity was also shown in hafnium-zirconium-oxide (HZO), which is comprised of the same lattice structure as doped hafnia. A 1:1 composition ($Hf_{0.5}Zr_{0.5}O_2$) is known to show a high remanent polarization, small variations are not as crucial as for doped HfO_2 [58], [59]. Due to its process robustness, HZO was used in this work to build ferroelectric FETs (FeFETs). The FeFET is also called the 1T (one transistor) memory architecture and it will be described in the following, together with the 1T-1C (one transistor, one capacitor) setup.

FeRAM (1T-1C)

The concept of the FeRAM is a DRAM-like construction with one field-effect transistor and a ferroelectric capacitor (Fig. 2.9). The FE (ferroelectric) material in the capacitor makes it non-volatile and eliminates the periodic refresh that is needed in DRAM. The cell can be programed and read out by the application of a voltage to the plate line (PL). During the read-out the capacitor is biased in one direction (positive voltage for "Reading" in Fig. 2.10) and the current charges the bit line (BL), when the word line (WL) actives the transistor. Depending on the initial polarization of the ferroelectric, the current is high for a 1 or low if a 0 was written. The read-out is destructive and the state has to be subsequently written back, since the capacitor will be set to a certain polarization state, depending on the voltage polarity. The down-scaling of FeRAM memories leads to smaller cell sizes and less amount of charge stored in the capacitor. Therefore, a high remanent polarization is needed to achieve a stable read operation.

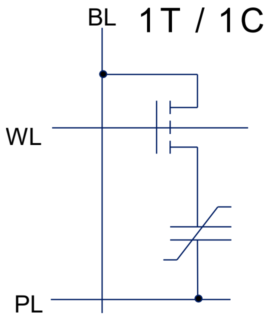


Fig. 2.9: Schematic layouts of the FeRAM cell, from [60]

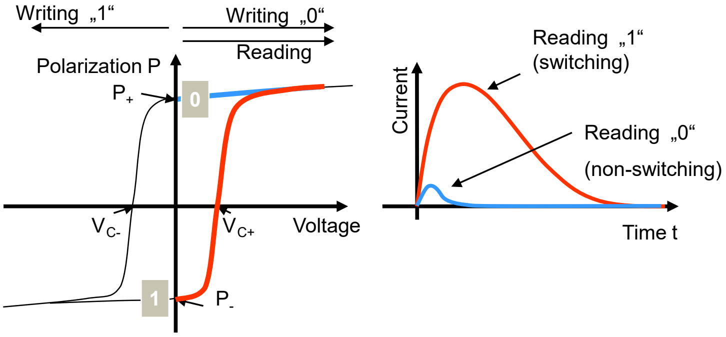


Fig. 2.10: Read-out of FeRAM depending on the previous polarization state, from [60], modified

FeFET (1T)

The integration of a ferroelectric material into the gate stack of a field-effect transistor makes it a FerroFET (FeFET) and represents a very small non-volatile memory cell. The read-out is non-destructive and the amount of charge needed for a stable operation is much lower than for the capacitor type. The transfer curve of the FeFET ($I_D\left(V_G\right)$) can be shifted (ΔV) by switching the polarization of the ferroelectric layer while applying a positive or negative gate voltage V_G. The voltage shift is also called memory window (MW) and depends on the coercive field E_c and the FE layer thickness. The drain current I_D (V_D connected to the bit line) at a certain gate voltage V_G

(connected to the word line) depends on the the polarization state of the ferroelectric and directly holds the binary information.

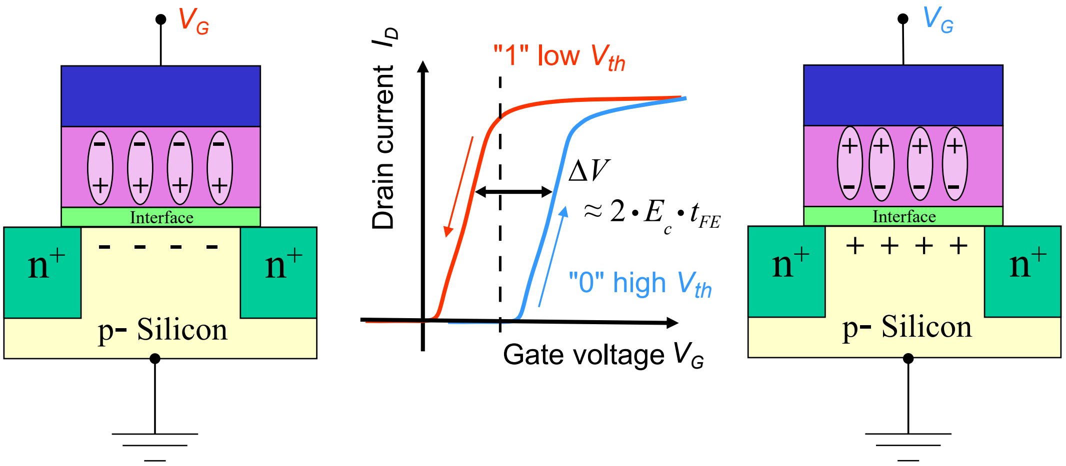


Fig. 2.11: Threshold voltage shift due to the polarization in the FE layer of a FeFET with interface oxide layer, from [60], modified

Similar to HKMG FETs, a thin interfacial oxide layer has to be implemented between the Si and the FE. It should be kept as thin as possible, since it causes a depolarization field, as depicted in Fig. 2.12. When no voltage is applied at the gate, the total voltage across the dielectric stack has to be zero. Since a polarization is present in the FE layer, an opposing voltage must drop across the low-k interface layer, depolarizing the FE. The *retention* time of the written state is mainly influenced by this.

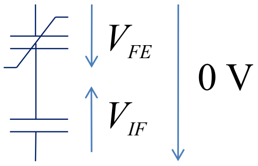


Fig. 2.12: Description of the depolarization field – voltage drop across the low-k interface oxide layer, from [60]

Further reliability aspects include the so-called imprint effect and fatigue. So-called *imprint* is usually occurring when the ferroelectric is continuously biased and stressed in one direction. The P-V curve (hysteresis) is shifted into one direction due to pronounced charge trapping and the coercive fields $\pm E_c$ are getting asymmetric. *Fatique* describes the reduction of the remanent polarization P_r after repeated cycling stress, when more and more of the ferroelectric domains cannot be switched anymore. This degradation mainly determines the lifetime of the memory cell.

2.2 3D Integration and the Use of TSVs (Through Silicon VIAs)

As already mentioned in chapter 2.1.1, down-scaling and the miniaturization of transistors is one way to put more devices in an IC to reduce manufacturing costs while increasing the performance at the same time. This path is called “More Moore” and relies on new materials and manufacturing technologies. Another direction is “More than Moore”, aiming for a heterogeneous integration, combining more functionality in one chip (e.g. Logic, memory, analog, RF/HF, photonics, biochips, ...). The use of various mature and thoroughly developed fabrication nodes adds manufacturing capacity and also enables cost reductions due to very high chip yield for these nodes.

Chip stacking has the potential to further drive both of these paths. Coming from a 2-dimensional approach, so-called 2.5D and 3D integration came into focus. The 2.5-dimensional way uses interposers to enable a close side-by-side arrangement of different ICs without traditional wire-bonds. So-called TSVs (short for TSVIA, Through Silicon Vertical Interconnect Access) are used as (short) vertical connections to the PCB (Printed Circuit Board). Real 3-dimensional chip stacking makes use of on-chip TSVs. Either individual dies are stacked on top of each other (possibly fabricated by the use of different manufacturing nodes) or monolithic single-chip approaches are used [61], [62]. This is summarized in Fig. 2.13 – the 2.5D and 3D integration offer shorter interconnects, resulting in reduced delays, lower power consumption and an increased overall performance.

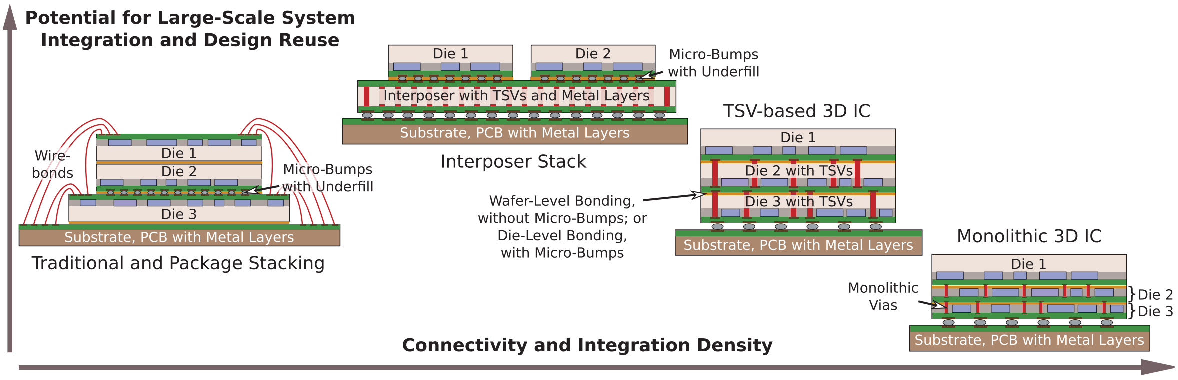


Fig. 2.13: Traditional 2D integration with wire-bond connections, 2.5D using an interposer and off-chip TSVs and real 3D stacking, from [61]

As widely accepted, on-chip through-silicon VIAs can be fabricated in three different ways [63]. For the *VIA-first* approach, the TSVs are etched and filled with a conductive material before the subsequent steps. This prohibits the possibility to utilize

Cu, because it will diffuse into the silicon when high temperatures are applied during transistor manufacturing (FEOL (front end of line), up to 1000 °C and above). Poly-Si or W could be used instead. The subsequent BEOL (back end of line) process steps involve Cu and are performed at lower temperatures (400 °C and below), before the substrate is thinned down to the TSV depth. For *VIA-middle*, the transistors are made first, then follows the TSV preparation, followed by the BEOL metallization and wafer thinning. This way, the TSVs can be filled with Cu, providing superior electrical properties. The *VIA-last* method starts with the complete device fabrication (FEOL and BEOL), before the wafer is thinned down. Only then, the TSVs are etched and filled. By processing the TSVs from the backside, the device layer can also be contacted – without perforating the entire stack of device and metal layers, as it is shown in Fig. 2.14.

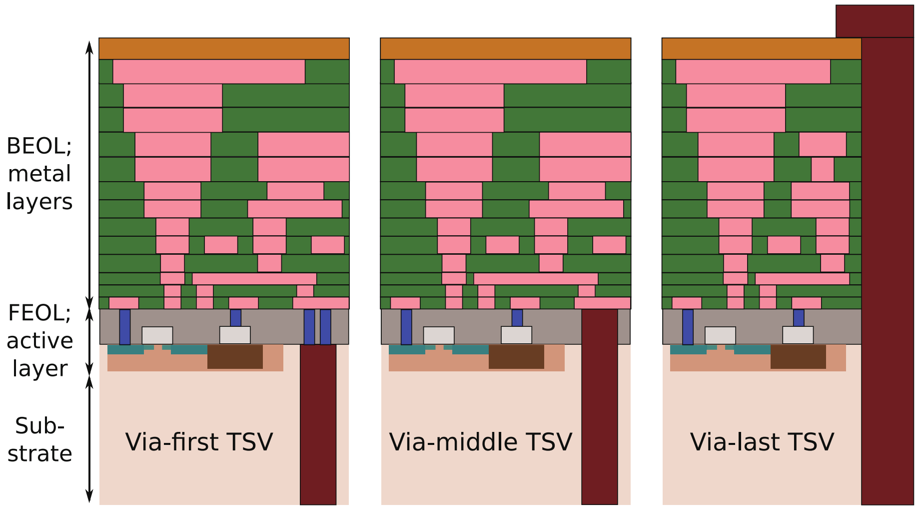


Fig. 2.14: Integration of TSVs – VIA-first, VIA-middle and VIA-last approach, from [61], derived from [63]

	VIA etching	VIA isolation	Barrier/seed deposition	Litho	VIA filling
VIA-first	⊕	⊕ thOx ⊙ Other	⊙ (barrier changes at high T)	⊕	⊕ Poly-Si ⊙ W ⊖ Cu
VIA-middle	⊕	⊙ thOx ⊙ Other	⊕	⊕	⊕ Poly-Si ⊕ W ⊕ Cu
VIA-last	⊕	⊙ thOx ⊙ Other	⊕	⊙ back side alignment	⊙ Poly-Si ⊕ W ⊕ Cu

Tab. 2.1: Comparison of VIA-first, -middle, -last, from [64]

Advantages and disadvantages for each TSV implementation are summarized in Tab. 2.1, where $\oplus$ is a suitable process, $\odot$ means limited feasibility and $\ominus$ is not feasible.

The fabrication of a Cu-based Si interposer for 2.5D integration is shown in Fig. 2.15 and should be briefly discussed here. The authors used a thin wafer ($200\,\mu$m), bypassing a thinning step. TSV etching was done through a Bosch DRIE (deep reactive ion etching) process [65]. The authors described, that the insulator was formed by wet thermal oxidation of the Si – the thermal budget during the TSV processing is comparable to the VIA-first approach. When Cu is used, a barrier is always needed to prevent diffusion. Since Cu was electrochemically deposited, a seed layer with a reasonably low resistance had to be applied at the whole TSV surface. A thermal ALD process of Ru was used in this case – thermal atomic layer deposition ensures an excellent step coverage, which is needed for TSVs of high aspect ratio (up to 20:1 described, hole diameter down to $10\,\mu$m). The front side and back side were structured to create U-shaped metal connections and pads for SnAg or PbSn solder bumps.

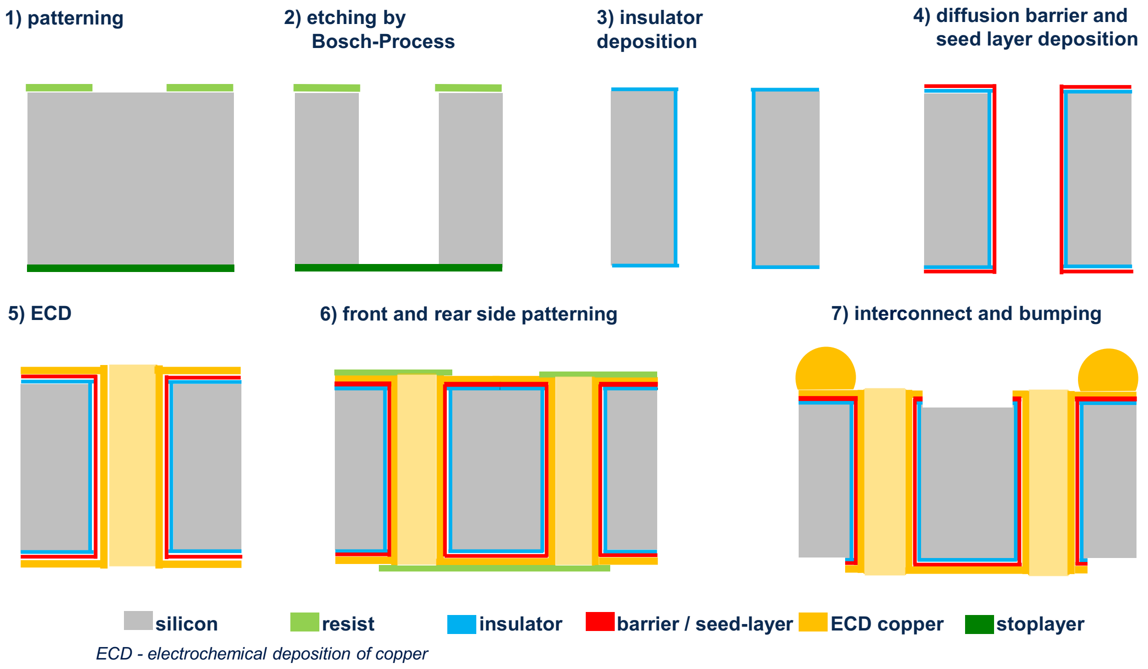


Fig. 2.15: Typical process flow for the fabrication of a Cu-based Si interposer, from [66]

Parts of this process flow served as inspiration for the integration of field-effect transistors in the interposer – as described in the chapters 4 and 5. High temperature FEOL processes are possible, enabling the first realization of an active TSVFET inside these through silicon VIAs.

2.3 Doping of Silicon

Doping is the controlled substitution of atoms in a semiconductor lattice. This changes the resistivity and enables the conversion of the conduction type from p (hole) to n (electron) or vice versa. For the doping of silicon, elements from the third and fifth main group of the periodic table are used. For p-doping, boron (B) is mostly used – aluminum (Al) and gallium (Ga) are also a possibility. The n-doping is commonly done by phosphorus (P) or arsenic (As), antimony (Sb) is also used.

Doping of silicon shifts the Fermi level towards the edge of the valence band (VB) or conduction band (CB). While it is located right in the center of the band gap for intrinsic material, the Fermi level is closer to the VB for p-doping and closer to the CB for n-doping. The creation of a pn junction inside a single crystal of semiconductor material forms the elemental building block for integrated circuits. When an external voltage is applied, it is blocking the current for a reverse bias and is passing it through in forward bias mode. Various devices such as diodes, transistors, light-emitting diodes, solar cells and complex ICs are made up of pn junctions.

The most common processes used for doping are thermal diffusion and ion implantation. Doping can also be done during the semiconductor material generation – e.g. by the addition of dopants to the molten material for Czochralski crystal growth [67] or by the introduction of dopant-containing precursors during layer growth (CVD [68], [69], epitaxial growth [70], PLD [71], ...).

2.3.1 Doping by Thermal Diffusion

The doping profiles after a thermal diffusion of dopants in silicon can be derived from Fick's 1st and 2nd law with the use of certain boundary conditions [72], [73].

$$J = -D\frac{\partial N}{\partial x} \qquad \text{Fick's 1st law} \tag{2.3.1}$$

$$\frac{\partial N}{\partial t} = -\frac{\partial J}{\partial x} \qquad \text{Fick's 2nd law} \tag{2.3.2}$$

J is the diffusion flux, N the particle concentration, D the diffusion coefficient as proportionality factor, t the diffusion time and x the diffusion length. The diffusion equation follows as a combination of Fick's laws:

$$\frac{\partial N}{\partial t} = D\frac{\partial^2 N}{\partial x^2} \tag{2.3.3}$$

Two cases can be defined for infinite and limited diffusion sources. Fig. 2.16 shows the initial situations for each form.

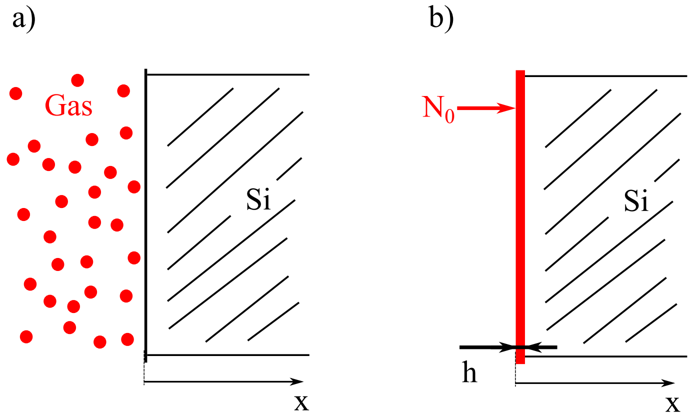


Fig. 2.16: Doping from a) infinite and b) limited source

For an infinite source, the following boundary conditions apply:

- $N\left(x > 0, t = 0\right) = 0$, at time 0 there are no dopant atoms in the silicon
- $N\left(x = 0, t > 0\right) = N_0$, at a time $t > 0$ the surface absorbs $x = 0$ dopant atoms until the saturation concentration is reached, because there are always far more particles provided than can be taken up

Applied to the diffusion equation, the result is a dopant distribution that follows a conjugated error function (erfc function):

$$N\left(x,t\right)=N_0\cdot\operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right)\tag{2.3.4}$$

For diffusion from a limited doping supply, e.g. from a pre-deposited film with a very thin layer thickness and low dopant concentration N_0, different boundary conditions are assumed:

- $N\left(0<x<h,t=0\right)=N_0$, at time 0 all dopant atoms are located in the precoating layer
- $N\left(x>h,t=0\right)=0$, at time 0 there are no dopant atoms in the silicon
- furthermore $\left[\frac{\partial N(x,t)}{\partial t}\right]_{x<0}=0$, i.e. diffusion outside the wafer is prevented

Inserted into the diffusion equation, these conditions lead to a Gaussian function:

$$N\left(x,t\right)=\frac{Q}{\sqrt{\pi Dt}}\cdot\exp\left[-\left(\frac{x}{2\sqrt{Dt}}\right)^2\right]=N_0\left(t\right)\cdot\exp\left[-\left(\frac{x}{2\sqrt{Dt}}\right)^2\right]\tag{2.3.5}$$

Q is the pre-deposition $Q=N_0\cdot h$, with h as the thickness of the layer. $N_0\left(t\right)$ is not constant and depends on the diffusion time t.

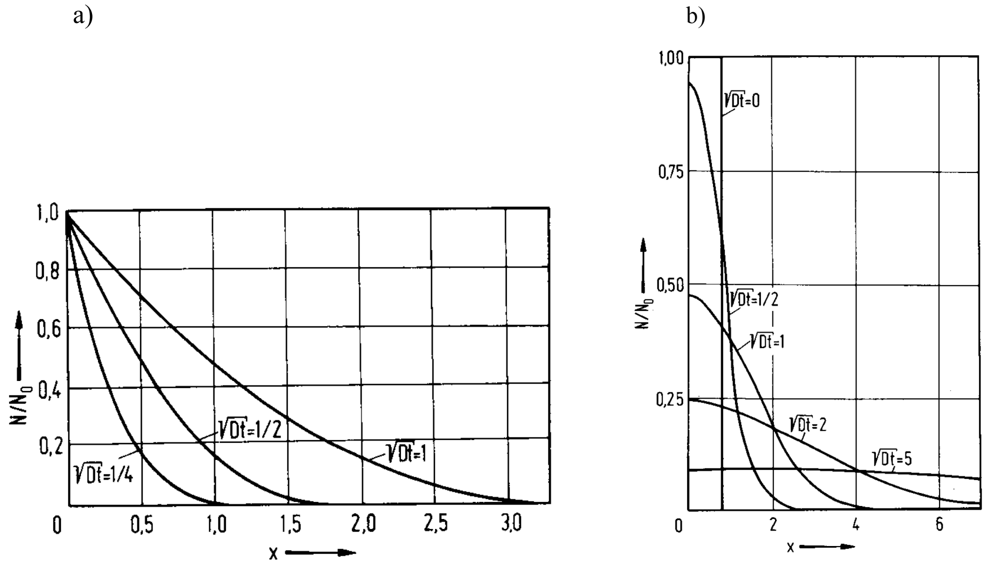


Fig. 2.17: Normalized doping profiles from a) infinite and b) limited supply for different diffusion parameter $\sqrt{Dt}$, from [72]

It should be noted, that during the thermal treatment, dopants diffuse not only in vertical but also in lateral direction. When defined areas should be doped through a structured hard mask (e.g. SiO_2 [74]), the lateral diffusion underneath the mask is about $0.8\cdot x_j$ (where x_j is the junction depth) [75].

2.3.2 Doping by Ion Implantation

For ion implantations, the dopant atoms are ionized, separated into masses, accelerated in an electric field and then shot at the substrate. The majority of the ions penetrate into the substrate. It has some advantages over thermal diffusion. The temperature can usually be kept lower, the subsequent annealing step is defining the thermal load. Photo resist can be used as the masking material and minimal lateral doping can be expected (minimal thermal diffusion in lateral direction during the activation). Ion implantation offers a very precise control over the dose (concentration) and the maximum of the concentration is located inside the silicon (can lead to better device performance, lower diode off-currents).

The so-called LSS model (named after J. Lindhard, M. Scharff and H.E. Schiott) describes the interaction of ions with the bombarded material during the implantation [76]. Mainly, the projected range R_p and its standard deviation ΔR_p are considered. Relevant retardation mechanisms are inelastic scattering with the electrons in the atomic shells (electronic stopping) and elastic scattering with the nuclei (nuclear stopping, coulombic scattering) [77]. Elastic scattering with the electrons and inelastic scattering with the nuclei have less influence. For lighter ions and higher kinetic energy, electron stopping dominates, for heavy ions and lower kinetic energy it is nuclear stopping. The energy loss per distance traveled can be expressed by equation 2.3.6, where $S_n(E)$ and $S_e(E)$ are the cross-sections of nuclear and electron retardation and N is the target atom density. $S_e(E)$ is approximately proportional to $E^{1/2}$. Integration leads to the the projected ion range (equation 2.3.7):

$$-\frac{dE}{dx} = N\left(S_n(E) + S_e(E)\right) \tag{2.3.6}$$

$$R_p = \frac{1}{N}\int_0^{E_0} \frac{1}{S_n(E) + S_e(E)} dE \tag{2.3.7}$$

The concentration profile of doping atoms follows a Gaussian distribution [78]:

$$N(x) = \frac{N_D}{\sqrt{2\pi}\Delta R_p} e^{-\frac{(x-R_p)^2}{(2\Delta R_p)^2}} \tag{2.3.8}$$

where N_D is the ion dose [1/cm^2] and x is the depth.

However, experimental data does not show a Gaussian distribution. A detailed comparison of model and experiment shows that a so-called Pearson distribution fits much better, as it includes a certain skewness (γ) and peakedness (kurtosis β). As an example, boron (B) and phosphorous (P) implantations into germanium (Ge) are shown in Fig. 2.18. Fits of Gaussian and Person curves are indicated.

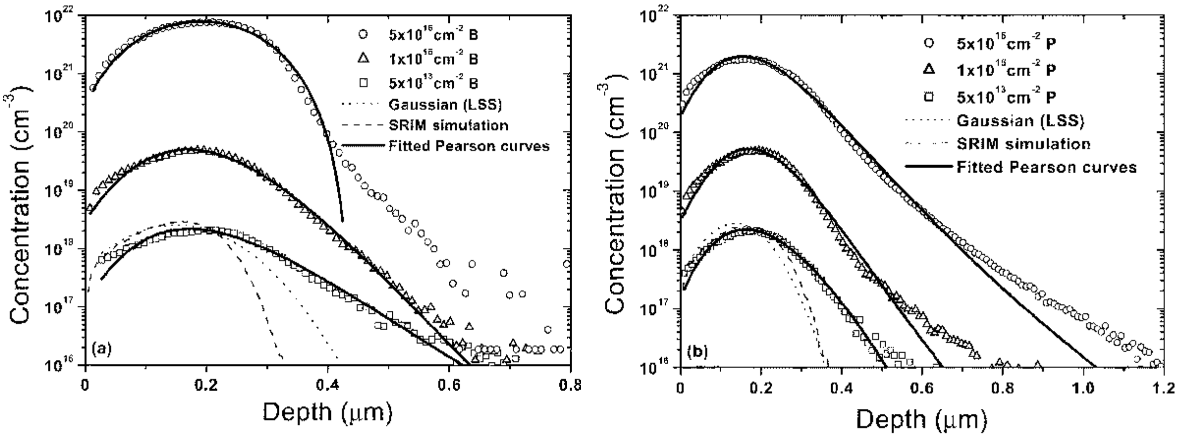


Fig. 2.18: SIMS measurements and simulations of boron (60 keV) and phosphorus (170 keV) implantations into germanium, from [79]

As already mentioned, the LSS model is only a first order approximation. It describes only interactions with amorphous material without taking the lattice structure into account. *Channeling* appears in low Miller index directions, the probability for a collision is very low – this leads to a deeper penetration than described by LSS. Channeling can be reduced by tilting of the crystalline material or the implantation through a scatter film (e.g. SiO_2). Further effects are *sputtering* during the implantation that shifts the concentration maximum into deeper regions, impact *damage* of the crystal lattice and an *amorphization* for high implantation doses.

After implantation, damage recovery has to be done and the doping atoms have to be activated, since they are positioned at interstitial sites and are not incorporated in the target lattice. A thermal treatment is necessary at high temperatures for a short period of time (RTA, Rapid Thermal Anneal).

3 Electrical Characterization

3.1 Resistivity Measurements

3.1.1 Resistance Determination by Four-Point Probes Measurement

The characterization of doped regions and thin layers is carried out in numerous forms by means of electrical resistance measurements. In the following, the four-point-probe measurement will be briefly presented. In addition, the sheet resistance is introduced and the relationship to the resistivity is explained.

Four-Point Probes Method

In many cases a four-point measurement is used for resistance measurements. The advantage over a two-point measurement is that both – the contact resistance and the resistance of the measuring circuit – are eliminated. The measurement results are therefore easier to interpret. Fig. 3.1 shows the measurement arrangements for both cases.

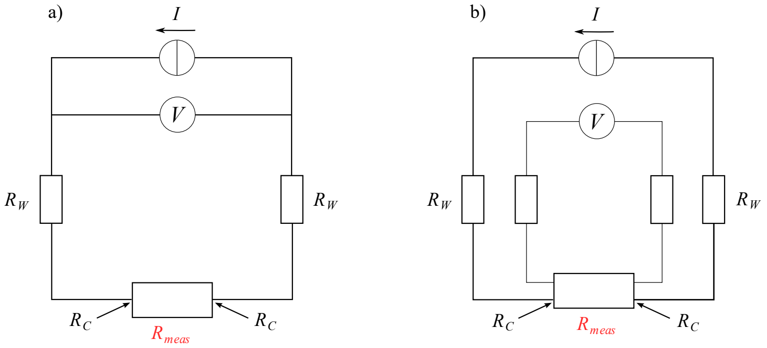


Fig. 3.1: Schematic representation of a) two-point measurement and b) four-point measurement, from [80]

The measured total resistance R_{tot} is composed as follows for a two-point measurement:

$$R_{tot} = \frac{V}{I} = 2 \cdot R_W + 2 \cdot R_C + R_{meas} \tag{3.1.1}$$

R_W indicates the resistance of the measuring circuit, R_C the contact resistance and R_{meas} the resistance to be measured. It can be seen that it is not possible to determine the exact resistance R_{meas} with this structure. The remedy is the four-point probes measurement. A current I is driven through the resistor and the voltage V is measured with two further probes. The resistance can be determined by linear regression of the recorded V-I characteristic. The paths to the voltmeter also contain R_W and R_C, but the flowing current is very small due to the high input resistance of the volt meter ($\geq 10^{12}\ \Omega$). The voltage drop is therefore negligibly small, so that R_{meas} can be determined very precisely.

Typical four-point measurements are performed with probes arranged in a row. A known current is driven through the two outer tips and the voltage drop is measured over the two inner. This makes it possible to determine the resistivity of an electrically conductive sample or layer. According to [80], the field under the tips follows the equation

$$E = J \cdot \rho = \frac{dV}{dr} \tag{3.1.2}$$

where J is the current density, ρ is the resistivity of the measured layer, and dV/dr describes the voltage drop as the distance from the tips increases. The current density can be replaced by

$$J = \frac{I}{A} = \frac{I}{2\pi r^2} \tag{3.1.3}$$

A is the area under the contact, the current flows through. The voltage V at a point $\mathbf{P}$ with a distance r from the tip then results as follows:

$$\int_0^V dV = -\frac{I\rho}{2\pi} \cdot \int_0^r \frac{dr}{r^2} \Rightarrow V = \frac{I\rho}{2\pi r} \tag{3.1.4}$$

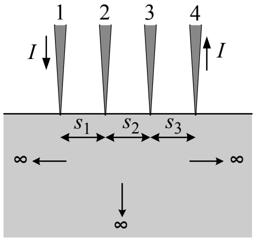


Fig. 3.2: Four-point measurement with probes in a row and with constant distance, from [80]

Equation 3.1.4 applies to each of the four probes. For a voltage measurement between the middle probes 2 and 3 (see Fig. 3.2) with tip distances of s_x can be written as:

$$V = \frac{I\rho}{2\pi}\left(\frac{1}{s_1} - \frac{1}{s_2 + s_3} - \frac{1}{s_1 + s_2} + \frac{1}{s_3}\right) \tag{3.1.5}$$

If a constant probe distance of $s = s_1 = s_2 = s_3$ is used, the relationship for the resistivity is as simple as:

$$\rho = 2\pi s \frac{V}{I} F \tag{3.1.6}$$

The correction factor $F = F_1 \cdot F_2 \cdot F_3$ is introduced to include a correction for the relationship between tip distance and sample thickness (F_1). In addition, the lateral expansion of the sample is F_2 and the position of the measuring point relative to the edge of the sample is F_3. For measurements in the middle of the sample, the lateral extent and the distance to the edge are so large that F_2 and F_3 can be set to 1. If the tip distance is large compared to the sample thickness, the correction factor is simplified to $F_1 = F = \frac{t/s}{2ln(2)}$. Where t is the thickness of the measured layer. After inserting F into equation 3.1.6 you get

$$\rho = \frac{\pi}{ln(2)} \cdot t \cdot \frac{V}{I} \tag{3.1.7}$$

Sheet Resistance

Thin (doped) layers can also be characterized by their sheet resistance R_{sh}, which results as follows:

$$R_{sh} = \frac{\rho}{t} = \frac{\pi}{ln(2)} \cdot \frac{V}{I} \tag{3.1.8}$$

The sheet resistance is a parameter that only depends on the layer thickness t and the material properties, but not on the lateral dimensions. A resistor consisting of this material with the length L and width W is calculated according to $R = R_{sh} \cdot (L/W)$. R_{sh} has the unit $\frac{\Omega}{\square}$ (pronounced: Ohm per “square”) and can be understood as a measure for the average resistivity over the sample thickness. When doped areas are produced by diffusion, unevenly doped areas are the result. In this case, the layer resistance can be seen as the depth integral (0 to t) over all doped atoms - independent of their spatial distribution in this depth section.

$$R_{sh} = \frac{1}{\int_0^t \left[1/\rho\left(x\right)\right] dx} = \frac{1}{\int_0^t \sigma\left(x\right) dx} = \frac{1}{q\int_0^t \left[n\left(x\right)\mu_n\left(x\right) + p\left(x\right)\mu_p\left(x\right)\right] dx} \tag{3.1.9}$$

3.1.2 Contact Resistivity

The contact resistance between metallization and doped areas has a significant influence on the achievable saturation current of a MOSFET. A high electrical resistance between source and drain regions and the metallization connected to the outside leads to low drain currents. In this chapter, the metal-semiconductor contact is described and a method for determining the contact resistivity is explained.

Metal-Semiconductor Contacts

There are basically two types of metal-semiconductor contacts. Schottky contacts with junction behavior and contacts with ohmic behavior. Exemplarly, the case for n-doped regions is explained here. When an n-doped semiconductor is brought into contact with a metal of higher work function (e.g. aluminum), electrons migrate from the semiconductor into the metal, because the Fermi levels of both materials align to each other (thermodynamic equilibrium) [81]. A positive space charge region is created in the semiconductor, which is compensated by the accumulation of electrons in the metal. The opposing field prevents further electron migration into the metal. The resulting potential difference is called contact voltage V_C. The vacuum level does not change abruptly at the interface between the metal and semiconductor, which leads to band bending in the semiconductor (see Fig. 3.3).

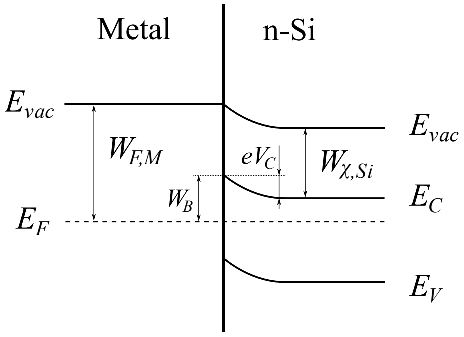


Fig. 3.3: Band bending at an interface between n-Si and a metal of higher work function

For such a junction, reverse or forward polarity can occur. When a negative voltage V_R (reverse polarity) is applied, electrons are removed from the the semiconductor at the junction. In addition, the Fermi level in the metal is shifted upwards by the value $e \cdot V_R$, which increases the band deflection. This increases the so-called Schottky barrier W_B and prevents an electron flow from the metal into the n-doped semiconductor. With a forward bias, the Fermi level in the semiconductor is raised by $e \cdot V_F$, which reduces the band bending and allows electrons to flow into the metal. The current increases exponentially with increasing voltage and follows the equation

$$I = I_S \cdot \left(e^{\frac{V_F}{V_T}} - 1 \right) \tag{3.1.10}$$

where I_S is the saturation current, V_F is the applied forward voltage, and V_T is the thermal voltage.

The diode behavior of such a Schottky contact is not desirable in integrated circuits. A metal-semiconductor contact independent of polarity with approximately ohmic behavior and low electrical resistance is wanted. This goal is achieved by a high $n^{(+)}$ doping (or in the case of a p-MOSFET high $p^{(+)}$ doping) of the semiconductor. Although there is no particularly low Schottky barrier, it becomes very thin, as shown in Fig. 3.4.

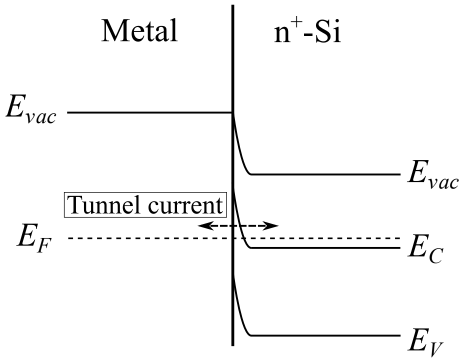


Fig. 3.4: Thin Schottky barrier for n^+ doping

A measure of the width of the barrier is the width of the space charge region. It depends, among other things, on the substrate doping N_D and can be calculated with the following equation:

$$w_{scr} = \sqrt{\frac{2 \cdot \varepsilon_0 \varepsilon_{Si} \cdot V_C}{e \cdot N_D}} \tag{3.1.11}$$

For doping concentrations around 10^{19} cm^{-3}, w_{scr} reaches low values of a few nanometers. In addition to passing the barrier by thermal activation, electrons can also tunnel through the barrier with these dimensions and tunnel currents by far exceed the thermal emission currents [81]. This process is also known as field emission. The tunnel probability and thus also the contact resistance depend essentially on the width of the Schottky barrier. Contact resistance is exponentially dependent on the root of the inverse dopant concentration ($R_C \sim \exp\left(\sqrt{\frac{1}{N_D}}\right)$).

Contact resistance measurement

According to [80] the contact resistance can be determined, with so-called TLM structures (Transmission Line Method). These are regularly arranged metal contacts with the same contact area. Fig. 3.5 shows the arrangement.

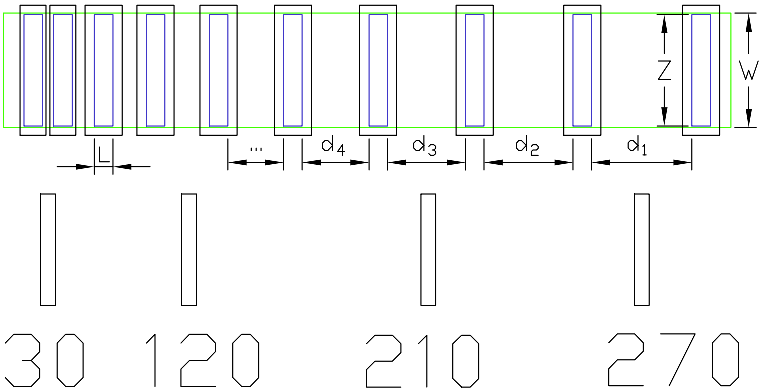


Fig. 3.5: TLM structure for the determination of contact resistance (green are doped areas, blue are contact holes, black indicates the metallization)

Since the contact resistance to the S/D areas is of interest, the contacts are aligned to the doped silicon. The current flow under the contacts is shown in Fig. 3.6. When flowing from the semiconductor into the metal, the current experiences both, the contact resistivity ρ_c and the layer resistance of the semiconductor R_{sh}.

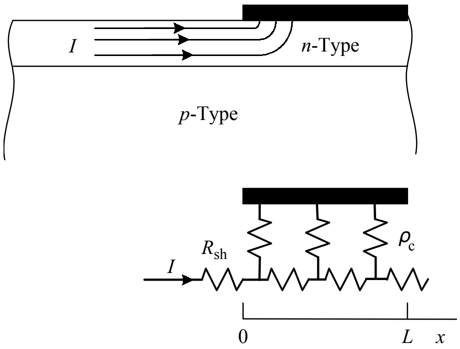


Fig. 3.6: Current flow and resistances under the TLM contacts, from [80]

Under the contact, the potential applied to the metal drops almost exponentially. The distance at which a drop to $1/e$ times the applied voltage can be observed is called the transfer length L_T. The potential curve can be determined according to [82] and [83] as follows.

$$V(x) = \frac{I\sqrt{R_{sh} \cdot \rho_c}}{Z} \cdot \frac{cosh\left[(L-x)/L_T\right]}{sinh\left(L/L_T\right)} \tag{3.1.12}$$

In this equation ρ_c is the contact resistivity, all other values can be taken from Fig. 3.5 or 3.6. The transfer length can also be described as the distance over which the current is transferred from the metal to the semiconductor, as shown schematically in Fig. 3.6. For good contacts this length is in the range of $1\,\mu$m. Since the contacts of the TLM structures used in this work are designed much larger than that ($L = 50\,\mu$m), only parts of the entire area contributes to the transition. From equation 3.1.12 the following equation for the contact resistance R_C can be concluded for $x = 0$ (at the contact edge):

$$R_C = \frac{V\,(x=0)}{I} = \frac{\sqrt{R_{sh}\cdot\rho_c}}{Z}\cdot coth\left(\frac{L}{L_T}\right) = \frac{\rho_c}{L_T\cdot Z}\cdot coth\left(\frac{L}{L_T}\right) \tag{3.1.13}$$

When the individual resistances between the designed contacts are determined and these values are drawn over the contact distance d, the double contact resistance $2\cdot R_C$ can be read as intersection with the ordinate axis. This extrapolation to a distance of $d = 0$ allows the elimination of the semiconductor resistance and thus the extraction of the contact resistance R_C. The transfer length L_T can be read for $R = 0$ at the intersection with the abscissa. From the slope of the curve, the sheet resistance R_{sh} can also be deduced. Fig. 3.7 summarizes this.

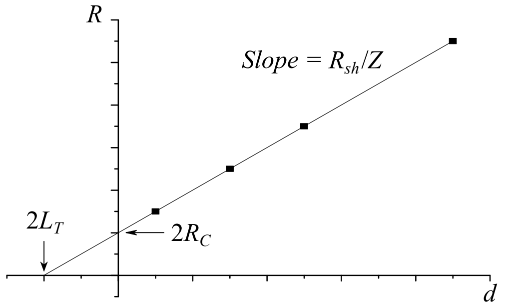


Fig. 3.7: Resistances R measured at the TLM structure over the contact distance d

With this knowledge, the contact resistivity follows from equation 3.1.13:

$$\rho_c = \frac{R_C\cdot L_T\cdot Z}{coth\left(\frac{L}{L_T}\right)} \tag{3.1.14}$$

The length Z of the contact should ideally be identical with the width of the doped area W below. Otherwise there will be a current flow around the contact, which leads to a falsification of the measured value, since such a simple geometry can no longer be assumed. For process reasons, however, the contact length Z was chosen to be $8\,\mu$m smaller than the width W of the doped area ($4\,\mu$m on each side). The contact should be located exclusively above the highly doped area, otherwise the measurement result will be influenced by the current flow over the Si substrate. Further influences which stand in the way of an exact determination of the contact resistivity ρ_c:

- The determination of L_T as intersection with the abscissa is not very precise, which can lead to erroneous calculations.
- An unknown change of the sheet resistance below the contacts compared to the doped silicon between the contacts; the determination is made under the assumption of a constant sheet resistance under and between the contacts. However, a large change is expected mainly for alloyed or silicide contacts which were not used in this case.
- Process variations such as slight underetching during the contact hole generation (especially when wet etched) or variations in initial sheet resistance; the measurement of multiple TLM structures per sample and averaging reduces this error.

3.1.3 Doping Concentration

Multiple techniques are available to obtain the impurity profile of doped silicon. SRP (Spreading Resistance Profiling) requires angled polishing as sample preparation (beveling) and very precise positioning of the electrical measurement system [84]. For SIMS measurements (Secondary Ion Mass Spectrometry), the associated tool has to be available. A focused primary ion beam is used for sputtering of the sample surface and a detector is collecting and analyzing ejected secondary ions. SIMS is very sensitive and not only electrically active doping ions are detected – this can lead to believe in doping concentrations that are slightly too high [85].

In this work, the choice was made for the DHE (Differential Hall Effect) method [86]. It will be described in more detail here – repetitive etching and 4-point-probes measurements are needed, as shown in Fig. 5.1 from chapter 5.1.1 and in Fig. 3.8.

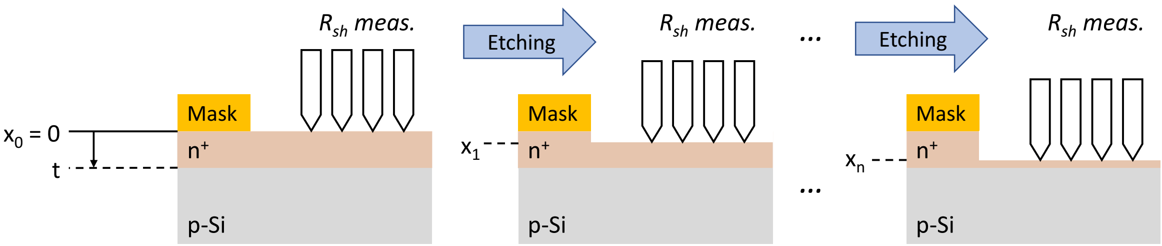


Fig. 3.8: Illustration of the steps for the DHE method – measurement of R_{sh} and thin layer removal by Si etching

The current flow (4pp measurement) is confined by the pn-junction, therefore only electrically active charge carriers of the measured layer contribute to the conductivity. The resulting sheet resistance R_{sh} over depth x curves need to be further processed. The following formula describes the value for doped layers with a thickness of t.

$$R_{sh} = \frac{1}{q \int_x^t \left[n(x)\, \mu_n(x) + p(x)\, \mu_p(x) \right] dx} \tag{3.1.15}$$

Here, x is the distance from the original Si surface (depth) and t is the junction depth. The sheet resistance at the Si surface is represented by the measurement result for $x = 0$.

The doping concentration is assumed to be constant in lateral direction (at a constant depth) – to eliminate measurement errors due to doping inhomogeneity, the 4pp measurements should be always performed at the same position on the sample. By inverting the R_{sh} profile and differentiation, a profile of the conductivity can be calculated.

$$\frac{d\left[1/R_{sh}\left(x\right)\right]}{dx} = -q\left[n\left(x\right)\mu_n\left(x\right) + p\left(x\right)\mu_p\left(x\right)\right] = -\sigma\left(x\right) \tag{3.1.16}$$

With $\rho(x) = 1/\sigma(x)$, the resistivity can be calculated from equation 3.1.16 as follows:

$$\rho\left(x\right) = \frac{-1}{d\left[1/R_{sh}\left(x\right)\right]/dx} = \frac{R_{sh}^2\left(x\right)}{dR_{sh}\left(x\right)/dx} = \frac{R_{sh}\left(x\right)}{d\left[ln\left(R_{sh}\left(x\right)\right)\right]/dx} \tag{3.1.17}$$

In this work, a polynomic trendline was applied to the $1/R_{sh}$ curve in a spread sheet program such as Microsoft Excel. To obtain the function of the resistivity curve $\rho(x)$, the derivative was calculated from this extracted formula. Another way was to use the “derivative” function in MATLAB software. These mathematic approaches are discussed in more detail in [87].

From the ASTM standard (American Society for Testing and Materials) F723-99 [88], the conversion between resistivity and doping concentration for boron doped silicon is given by:

$$N_B = \frac{1.33\cdot 10^{16}}{\rho} + \frac{1.082\cdot 10^{17}}{\rho\left[1+\left(54.56\rho\right)^{1.105}\right]}\left[cm^{-3}\right] \tag{3.1.18}$$

$$\rho = \frac{1.305\cdot 10^{16}}{N_B} + \frac{1.133\cdot 10^{17}}{N_B\left[1+\left(2.58\cdot 10^{-19}N_B\right)^{-0.737}\right]}\left[\Omega cm\right] \tag{3.1.19}$$

For phosphorous doped silicon it is:

$$N_P = \frac{6.242\cdot 10^{18}10^Z}{\rho}\left[cm^{-3}\right], \quad \text{with} \quad Z = \frac{A_0 + A_1x + A_2x^2 + A_3x^3}{1 + B_1x + B_2x^2 + B_3x^3} \tag{3.1.20}$$

$$\rho = \frac{6.242\cdot 10^{18}10^Z}{N_P}\left[\Omega cm\right], \quad \text{with} \quad Z = \frac{C_0 + C_1y + C_2y^2 + C_3y^3}{1 + D_1y + D_2y^2 + D_3y^3} \tag{3.1.21}$$

Where for the phosphorous density $x = log_{10}(\rho)$, $A_0 = -3.1083$, $A_1 = -3.2626$, $A_2 = -1.2196$, $A_3 = -0.13923$, $B_1 = 1.0265$, $B_2 = 0.38755$, $B_3 = 0.041833$ and for the resistivity $y = log_{10}(N_P) - 16$, $C_0 = -3.0769$, $C_1 = 2.2108$, $C_2 = -0.62272$, $C_3 = 0.057501$, $D_1 = -0.68157$, $D_2 = 0.19833$, $D_3 = -0.018376$.

Alternatively, the conversion can also be carried out using tabular values. In appendix A.1, a diagram with ρ over N_P and N_B is shown for 23 °C [88]. Several scientific web pages offer online calculators, covering these calculations [89], [90], [91]. Exemplarily, Fig. 3.9 depicts the inverse sheet resistance curve for a phosphorous diffusion from the SOD P-8545 from Honeywell used in this work on a p-doped Si Wafer (60 min, 1000 °C). The calculated resistivity and obtained dopant density profile are also shown.

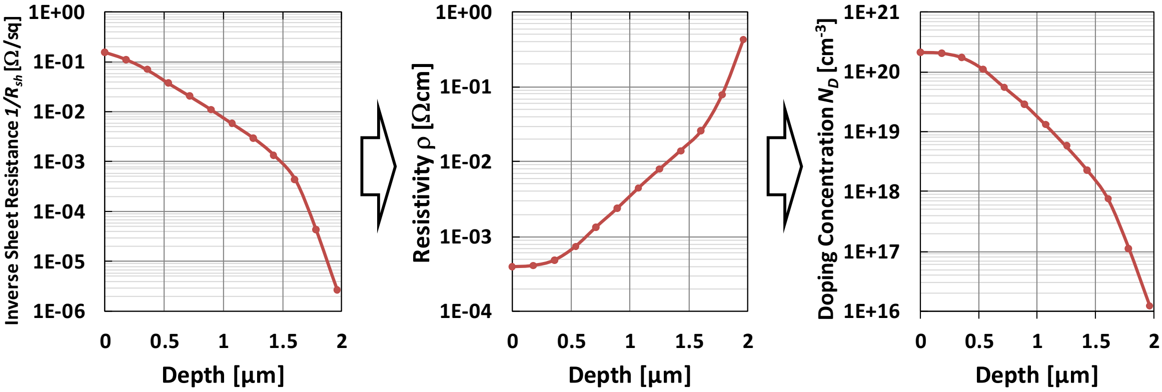


Fig. 3.9: Result of a diffusion from the Honeywell spin-on dopant solution P-8545 for 60 min at 1000 °C – calculated $1/R_{sh}$ from the measurement of R_{sh}, calculated ρ and N_P

3.2 C-V Measurements

3.2.1 Fundamentals of MIS C-V Measurements

Capacitance-Voltage (C-V) measurements of MIS (Metal-Insulator-Semiconductor) capacitors are done by applying a sweeping voltage at the metal or gate contact. The semiconductor undergoes accumulation, depletion and inversion – or the other way around, depending on the polarity and magnitude of the applied voltage. It can be done by a quasi-static / low frequency (qs, lf) method or with a high frequency (hf) measurement tool.

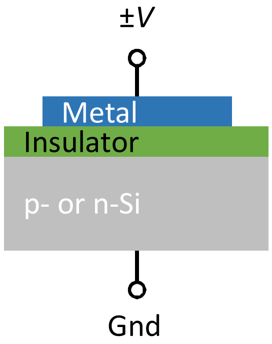


Fig. 3.10: MIS structure as it can be used for C-V measurements

Qausi-static (qs-) / Low Frequency (lf-)C-V

For quasi-static C-V measurements, the displacement current is measured as a function of time to determine the capacitance value. Insulating materials showing high leakage cannot be measured, because this leakage current would be added to the displacement current, leading to wrong capacitance values.

An ideal curve of a quasi-static C-V measurement of a MIS capacitor with p-Si body is shown in Fig. 3.11. When the semiconductor of the MIS stack is in accumulation or the inversion condition, the measured capacitance value is the capacitance of the oxide alone. The capacitance minimum is measured, when the semiconductor is in depletion mode. In this case, a series of capacitances – the oxide and the maximally depleted space charge region of the semiconductor are contributing [92].

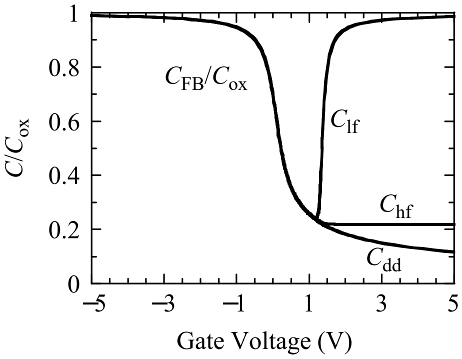


Fig. 3.11: C-V curves for lf and hf measurements for a MIS capacitor with p-Si and depiction of deep depletion (dd)

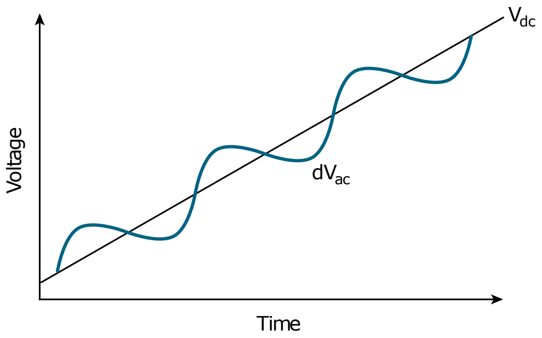


Fig. 3.12: AC and DC signals applied for the hf C-V sweep, from [93]

High Frequency (hf-)C-V

In the case of a high-frequency (hf) C-V measurement, the capacitance measured for accumulation and depletion is expected to be (nearly) the same as the quasi-static measurement. If the frequency of the biasing signal is high enough, the capacitance value measured for the inversion condition is different from the quasi-static C-V as a consequence of the non-equilibrium behavior of the inversion layer.

The inversion layer is formed by the minority carriers generated in the depletion region and these carriers are moved to the semiconductor–insulator interface by the applied electric field on the metal electrode [92]. In equilibrium, the minority carriers (inversion layer) have enough time to respond to the change in the applied electric field. Due to the slow carrier generation–recombination process in the semiconductor, the response of these carriers is too slow to follow the change of the electric field for the hf case. Therefore, the inversion layer appears fixed with respect to the AC signal component of the biasing voltage. The ideal curve of an hf-C-V measurement is depicted in Fig 3.11. For hf-C-V measurements, the capacitance value for the inversion condition is referred to as the minimum capacitance.

The measurement is performed by applying two simultaneous voltage signals – an AC signal is “wobbling” around a DC sweep, as shown in Fig. 3.12. The AC magnitude usually ranges between 30 ... 100 mV.

When the DC sweep is too fast while applying a high AC frequency, the semiconductor goes into deep depletion (dd) and the measured capacitance gets smaller than the minimum at equilibrium. When going from depletion into inversion too fast, the generation of the minority carriers can not keep up and the depletion layer increases beyond its maximum, further reducing the total capacitance (Fig 3.11).

3.2.2 Interpretation of C-V Measurements

C-V measurements can be used to gain various knowledge about MOS capacitors and MOSFETs. A few analyses used in this work are explained in the following chapter.

Permittivity

The deposition of thin dielectric films results in layers with certain electrical characteristics, including the permittivity, leakage current, breakdown voltage and others. They depend on the deposition type (CVD, PVD, ALD, ...) and multiple process parameters. In order to determine the permittivity, a C-V measurement can be used.
When the semiconductor is in accumulation, a layer of mobile majority carriers can easily compensate the charge on the metal electrode. The capacitance measured in accumulation is the maximum value C_{max} and represents the capacitance of the insulator C_{ins} alone. Since the area A of the metal electrode should be known, the permittivity of the insulator ε_{ins} (or effective permittivity of a stack of insulating materials) can be calculated after rearrangement of equation 3.2.1, where C is the measured capacitance, ε_0 is the vacuum permittivity and t is the thickness of the insulator.

$$C_{max} = C_{ins} = \varepsilon_0 \cdot \varepsilon_{ins} \cdot \frac{A}{t} \tag{3.2.1}$$

Flatband Voltage

The gate voltage at which the band bending in the silicon substrate disappears, is called the flat band voltage V_{FB}. It separates the accumulation regime from the depletion regime. For thin dielectrics and moderate doping of the substrate, V_{FB} is very close to the inflection point of the C-V curve [94].
For non-linear dielectric materials such as the ferroelectric Hafnium-Zirconium-Oxide used in this work, the flatband voltage shifts due to the polarization of dipoles in the material. The result is a hysteresis of the C-V curve, dependent on the direction of the voltage sweep. When the capacitance is measured over the gate of a ferroelectric FET, the voltage distance of the curves corresponds to the memory window (V_{th} shift) of the transistor.
Mobile charges drifting through the insulator or charging and discharging of traps in the dielectric material can also cause hysteresis effects, leading to unstable device characteristics.

Oxide and Channel Interface Defects

Since the determination of the oxide charge density is very important for the function of field effect transistors, possible oxide and interfacial defects are explained here.

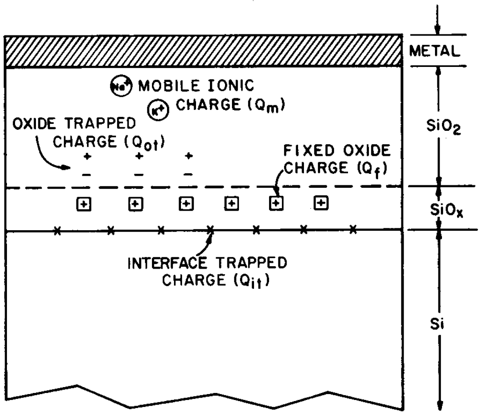


Fig. 3.13: Charges in thermally grown oxide, from [92]

Fig. 3.13 shows the various oxide charges, which include the following [92], [95]:

Q_{it} (interface trapped charges) are charges present at the SiO_2–Si interface. A disturbed lattice symmetry at the interface allows states for crystal electrons. Localized electron states in the band gap of the silicon are introduced, which act as traps for electrons and holes. Q_f (fixed oxide charges) are fixed positive charges in the oxide near the interface. Incompletely oxidized silicon atoms, which do not form complete tetrahedral SiO_4 groups do not form a sufficient number of covalent bonds and thus act as a positive charge. A forming gas anneal (H_2 in N_2) at 400 ... 450 °C can be used to reduce both, positive interfacial charges in the oxide (Q_f) and electron traps (Q_{it}) from 10^{12} ... 10^{15} charges/cm^2 to uncritical values of 10^9 ... 10^{10} cm^{-2}.
Two types of charges are also present in the volume of SiO_2. Highly mobile alkali metal ions Q_m (mobile charges) get incorporated during the oxidation and can move freely in the oxide at higher temperatures. These are mainly Li^+, Na^+ and K^+, which lead to unstable threshold voltage shifts. A counteraction for the reduction of these charges would be the addition of HCl during the gate oxidation. Chlorine is very reactive and ensures the removal of these ions. Q_{ot} (oxide trapped charges) are caused by exposure to radiation. These are open Si-O bonds which act as traps for charges. They can occur during plasma processing. Ions can be implanted and have a damaging effect or the UV radiation generates mobile charge carrier pairs. In addition, these impurities can be formed by so-called “hot carriers”, injected during the operation of the transistor. Also alpha radiation can be cited as one of the causes of Q_{ot}.

In the following, the quantification of interfacial charge (Q_{it}) and the interfacial state density (D_{it}) will be explained in more detail. The influence on the C-V curves is depicted in Fig. 3.14. Since traps can be charged and discharged, they reduce the surface potential. This leads to the effect known as strech-out for both, hf and lf curves. A difference between the hf and lf curves appears in the minimum capacitance measured. In the case of the low-frequency curve, the minimum capacitance is higher, because the traps can follow the potential change well and thus act like a parallel surface capacitance C_{it} (Fig. 3.15). The high-frequency curve shows a lower minimum capacitance, since the traps can no longer follow the alternating field and therefore, the capacity C_{it} plays no role.

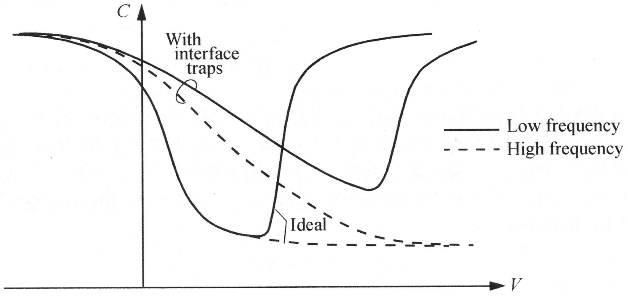


Fig. 3.14: Influence of interfacial defects on C-V characteristics, from [92]

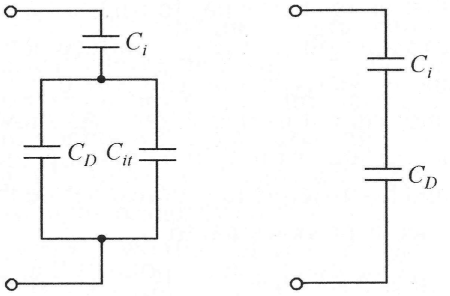


Fig. 3.15: Equivalent circuit for lf and hf C-V, from [92]

The difference in the total capacitance between the lf and hf curve can be determined as [92]:

$$C_{lf} = \frac{C_i\,(C_D + C_{it})}{C_i + C_D + C_{it}} \tag{3.2.2}$$

$$C_{hf} = \frac{C_i C_D}{C_i + C_D} \tag{3.2.3}$$

C_i is the capacity of the oxide and C_D the capacity of the charge distribution in the semiconductor. The capacitance of the interfacial states C_{it} follows as:

$$C_{it} = \left(\frac{1}{C_{lf}} - \frac{1}{C_i}\right)^{-1} - \left(\frac{1}{C_{hf}} - \frac{1}{C_i}\right)^{-1} \tag{3.2.4}$$

The density of interfacial states is:

$$D_{it} = \frac{C''_{it}}{e^2} \tag{3.2.5}$$

where e is the elementary charge and C''_{it} is the specific capacitance per area.

By measuring the hf (about 10 kHz and higher) and lf curves, the interfacial density can be obtained. Usually, values as low as $2 \cdot 10^{10}$ $\mathrm{cm^{-2}eV^{-1}}$ can be achieved for dry thermally grown SiO_2 layers after a forming gas anneal [96]. A high number of interface traps can lead to high gate leakage [97]. Especially the gate oxide of the TSV transistor introduced in chapter 5.1.2 is expected to have a high number of interface states. The channel was etched using a Bosch process (alternation of plasma etching and passivation layer deposition) and should be holding much more defects than oxides on polished wafer surfaces.

3.3 Transistor Measurements

3.3.1 Output Characteristics (I_D-V_D)

MOSFET current equation

An equation for the drain current of MOSFETs can be derived from the vertical and horizontal field progressions (derived from V_G and V_D) in the channel region, the gate capacitance, the charge distribution along the channel and the carrier velocity in the channel [98]. Taking the threshold voltage V_{th} into account, the relationship for the drain current I_D, named after Chih-Tang Sah, follows:

$$I_D = \frac{\mu \varepsilon_0 \varepsilon_{r,ins}}{t_{ins}} \cdot \frac{W}{L} \left\{ (V_G - V_{th}) \cdot V_D - \frac{1}{2} V_D^2 \right\} \tag{3.3.1}$$

where ε_0 is the dielectric constant (vacuum permittivity), $\varepsilon_{r,ins}$ is the relative permittivity of the gate insulator, μ is the mobility of the charge carriers and t_{ins} is the thickness of the gate insulator. W and L are channel width and channel length.

Working Modes of MOSFETs

From the equation of Sah (3.3.1), different working modes of the field effect transistor can be defined. The corresponding output characteristic field is shown in Fig. 3.16.

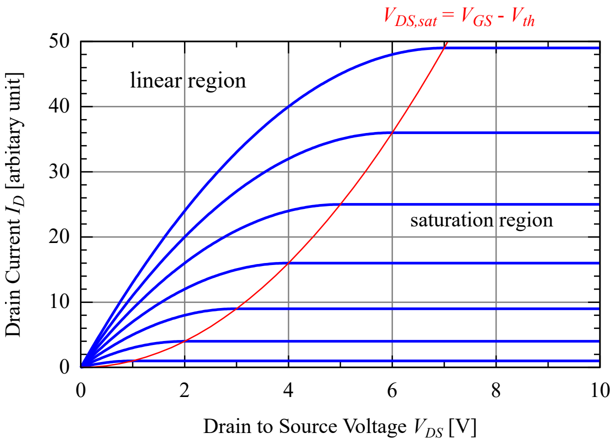


Fig. 3.16: Output characteristics of a n-MOSFET, assimilated from [99]

At each point in the channel, the surface potential consists of a vertical ($V_G - V_{th}$) and a horizontal (V_D) portion. In the *linear region*, the drain current I_D is correctly

described by the equation of Sah. In this case, the drain voltage V_D is lower than the so-called saturation voltage $V_D < V_{DS,sat}$. The drain current follows an almost linear characteristic for small V_D and behaves like an ohmic resistance with the conductance $G = 2 \cdot \mu \cdot C''_{ins} \cdot \frac{W}{L} \cdot (V_G - V_{th})$ [81].
In the *saturation region* V_D is so large that it comes to the so-called "pinch-off" of the channel. This can be observed, when $V_D \geq V_G - V_{th}$ is fulfilled. The voltage drop across the inversion channel remains constant at the value $V_{D,sat}$, that is reached at pinch-off. With a further increase of V_D, the additional voltage drops across the reversed pn-junction between drain and channel. The electrons still reach the drain area, however an increase of the drain current is not observed. I_D reaches a characteristic saturation value $I_{D,sat}$, which can be calculated by inserting the "pinch-off" condition in equation 3.3.1 as follows:

$$I_{D,sat} = \frac{\mu \varepsilon_0 \varepsilon_{r,ins}}{2 \cdot t_{ins}} \cdot \frac{W}{L} \left(V_G - V_{th}\right)^2 \qquad (3.3.2)$$

The *cutoff region* is characterized by a missing inversion channel. The gate voltage V_G is lower than the threshold voltage and only the sub-threshold off current and leakage currents are flowing ($I_D \approx 0$).

From these output characteristics, the $I_{D,on}/I_{D,off}$ ratio can be extracted. The saturation currents for the intended operation voltage (e.g. $V_D = V_{DD}$) are extracted at a gate voltage of $V_G = V_{DD}$ (on) and $V_G = 0$ (off). The ratio is a measure for how well the on and off state are distinguishable.

3.3.2 Transfer Characteristics (I_D-V_G)

The transfer characteristics describe the switching behavior of the transistor. It can be seen as a “cut” through the output curves at a fixed drain voltage. Usually, V_D is set to a value in the linear region.

The intersection of the tangent through the reversal point of the transfer curve with the voltage axis can be used to determine the *threshold voltage* V_{th}. From the equation of Sah (equation 3.3.1), $V_{th} = V_{G,I_D=0} - V_D/2$ follows for $I_D = 0$. As shown in equation 3.3.3, the threshold voltage depends on the insulator thickness t_{ins}, the relative permittivity of the insulator material $\varepsilon_{r,ins}$, the substrate doping concentration N_A or

N_D, the fermi potential Φ_F (dependent on N_A or N_D), the work function of the gate contact (expressed as the work function difference between metal and semiconductor Φ_{MS}) and insulator charges Q_{ins}. A substrate bias voltage V_{SB} has an influence as well.

$$V_{th} = \gamma\sqrt{V_{SB} + 2\Phi_F} + 2\Phi_F + \Phi_{MS} - \frac{Q_{ins} \cdot t_{ins}}{\varepsilon_0 \varepsilon_{r,ins}} \qquad \text{with} \quad \gamma = \frac{t_{ins}\sqrt{2e \cdot N_A \cdot \varepsilon_0 \varepsilon_{r,Si}}}{\varepsilon_0 \varepsilon_{r,ins}} \tag{3.3.3}$$

The *charge carrier mobility* (field effect mobility), can be calculated from the transfer curve. For the calculation of the field effect mobility μ_{FE}, the transconductance g_m can be used [100].

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_{DS}=const.} = \frac{W}{L}\frac{\varepsilon_0 \varepsilon_{r,ins}}{t_{ins}} \cdot \mu_{FE} \cdot V_D \tag{3.3.4}$$

Rearranged, it gives the following:

$$\mu_{FE} = \frac{\partial I_D}{\partial V_G} \cdot \frac{L}{W} \cdot \frac{t_{ins}}{\varepsilon_0 \varepsilon_{r,ins}} \cdot \frac{1}{V_D} \tag{3.3.5}$$

$\frac{\partial I_D}{\partial V_G}$ can be determined from the slope of the transfer curve. Fig. 3.17 shows the measured transfer characteristic for the TSV transistor, characterized in chapter 5.1.2. In addition, the field effect mobility μ_{FE} is plotted.

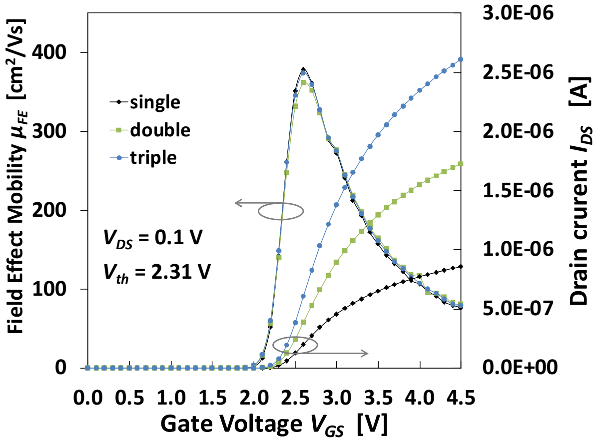


Fig. 3.17: Transfer curves and calculated field-effect mobility for single, double and triple structures of n-TSVFETs with 200 μm gate length and a TSV diameter of 20 μm

For higher gate voltages, the mobility usually decreases and the transfer curve saturates. In [100], three different scattering processes in the channel region are named as the cause. First, phonon scattering caused by lattice oscillations. For very low temperatures this influence becomes extremely small, for room temperature or for heated transistors, this kind of scattering contributes to the mobility saturation. Coulomb interactions also play a role. Charge centers such as electron traps at the Si-SiO$_2$ interface or ionized impurities in the channel contribute to this. In addition, the mobility is reduced by surface roughness at the Si-SiO$_2$ interface. This type of scattering is particularly effective at high gate voltages, since there is a dependence on the distance of the charge carriers from the surface. The TSV transistor introduced in this thesis is especially affected by this.

The *sub-threshold slope* is a measure for how fast the transition between the off and on state is passed and how much power is dissipated during that event. When the current I_D is plotted on a logarithmic axis, the sub-threshold swing can be extracted as voltage increase per decade of drain current increase. The reciprocal value is the sub-threshold slope – the ultimate value at room temperature is 60 mV/dec [101], [102]. So-called “negative-capacitance” FETs recently published, promise even lower sub-threshold swings $< 60\,\mathrm{mV/dec}$ [101], [103], [104]. A large number of traps will increase the sub-threshold slope – the TSV transistor from chapter 5.1.2 has a relatively defect-rich channel and is showing values of about 125 mV/dec.

Dielectric gate materials with a ferroelectric behavior or gate stacks that show severe charge trapping, shift the whole transfer curve of the transistor. This V_{th} shift represents the so-called *memory window* (MW) of the device.

4 TSV Transistor

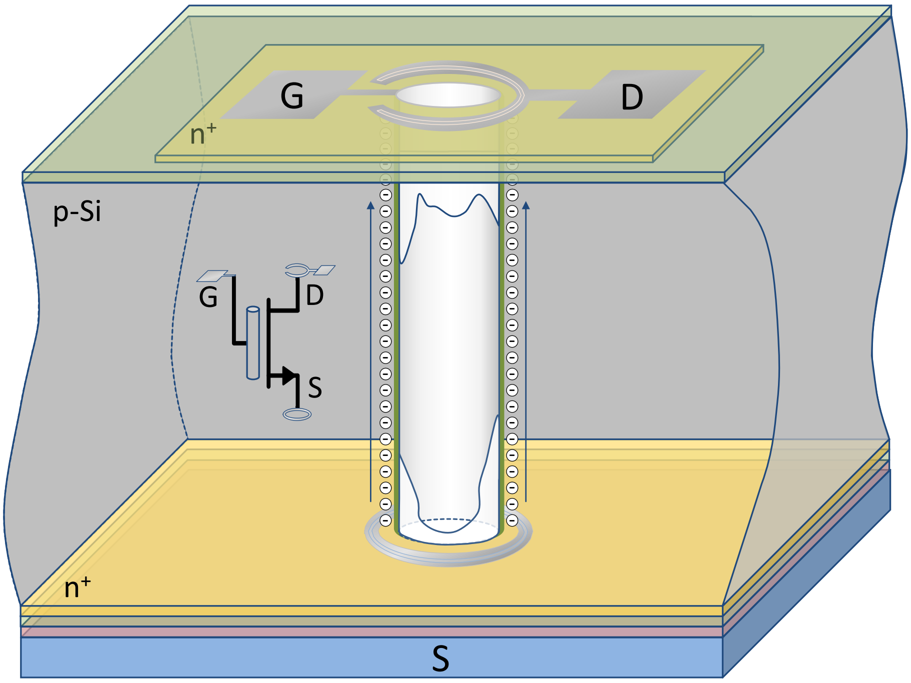


Fig. 4.1: Schematic of the TSV transistor described in the following chapters

4.1 Idea and Motivation

3D integration is a bypass to the upcoming limitations in the so-called “More Moore” path and has therefore become very important. As explained in chapter 2.2, chips are getting stacked on top of each other and connected by the use of through silicon VIAs. This increases the integrated functionality and further enhances the integration density. So far, the industry is using these vertical connections as metal lines by filling them with copper in combination with the necessary electrical isolation layer and Cu diffusion barriers. In addition, there is a trend towards optical interconnects, providing higher bandwidth connections. By filling the TSVs with optically transparent polymers such as SU-8 or OrmoCore^{TM}, vertical optical 3D chip connections are made possible [105], [106], [107], [108].

The functionalization of these TSVs can be taken one step further – the use of the TSVs can be extended by integrating passive and active devices. Through silicon capacitors (TSCs) have been shown before [11] for the use in power delivery networks, limiting voltage peaks and ensuring power integrity. Switchable devices would further increase the range of use for these connections. Building MOSFETs into the TSVs is an elegant way to enable smart interposers. Source and drain would be located at the front- and backside of the substrate and the channel would be formed along the inner surface of the hole, being covered with the gate that reaches through the TSV (see Fig. 4.1).

A similar concept stems from International Business Machines Corporation (IBM), who filed a patent in 2014. It describes the design and manufacturing of a FET with a similar concept [109]. However, such structures were not implemented before – a TSVFET was realized for the first time in the context of this work. This applies to electrical data of these devices as well as to a detailed presentation of the fabrication steps.

New fields of applications would be enabled by such a device.

- Rudimentary logic in the upper metallization layers of integrated circuits could be implemented. Activating / deactivating of stacked chips or parts of these could be done by the connection and the use of these long-channel TSVFETs could contribute to decrease the overall power consumption – a low off-current would be a preferred characteristic for this application.
- Electro-optical TSVs are possible as a combination, since the hole of the TSVFET could be left hollow, since the space is not needed for a Cu filling. Instead, light could be guided through it.
- An implementation as an ion sensitive IS-TSVFET, where the surrounding vertical channel confines a small volume of liquid.
- Chip layout camouflaging could be another possible application. Introducing security in the back end of line (BEOL) is a promising way of keeping the intellectual property of the chip designers safe. Switchable / programmable VIAs – as an alternative to dummy VIAs – could further impede reverse engineering [110], [111], [112].

4.2 Design and Layout of the TSV Transistor

4.2.1 Design of the TSV Transistor Structures

Due to the process experience at the IHM (Institut für Halbleiter- und Mikrosystemtechnik, engl. Institute for Semiconductors and Microsystems) of TU Dresden, the diameter of the transistor TSVs was either 20 or 40 μm [66]. TSV-nFETs were built on p-doped wafers with a thickness of 200 μm and for the p-TSVFETs 300 μm thick n-doped wafers were used. This difference arose due to the availability of wafers with a doping that had to fit as channel concentration for field effect transistors (concentrations in the range of $1 \cdot 10^{15}$ ... $1 \cdot 10^{16}$ cm^{-3} give reasonable threshold voltages V_{th}). Therefore the aspect ratios of the etched TSVs ranged between 5:1 and 15:1. Since thinning down by grinding and lapping was not possible at the IHM cleanroom facilities of TU Dresden, the transistors needed to be processed on wafers with the smallest available and handable thickness.

The TSVFETs have been implemented as single, double and triple structures. Two and three transistors were wired in a parallel way in the design to further increase the W/L ratio and to achieve higher output currents. Accordingly, different channel width to length ratios existed and can be found in Table 4.1.

TSV diameter d	$W = \pi \cdot d$	L (n-FET)	W/L (n-FET)	L (p-FET)	W/L (p-FET)
20 μm	62.8 μm	200 μm	0.31	300 μm	0.21
40 μm (2x 20)	125.7 μm	200 μm	0.63	300 μm	0.42
60 μm (3x 20)	188.5 μm	200 μm	0.94	300 μm	0.63
40 μm	125.7 μm	200 μm	0.63	300 μm	0.42
80 μm (2x 40)	251.3 μm	200 μm	1.26	300 μm	0.84
120 μm (3x 40)	377.0 μm	200 μm	1.88	300 μm	1.26

Tab. 4.1: W/L ratios for the n- and p-TSVFETs

Fig. 4.2 shows the structures as a top view in a photograph taken with an optical microscope. The gate contact reaches into the hole to cover the surface of the TSV hole that forms the channel of the FET. The contact holes (drain contact) were designed to surround nearly the entire TSV hole, in order to realize a large contact area and to keep contact resistances low. The structures at the backside of the wafer mirror the exact same layout with a source contact and the gate overlapping the edges of the holes.

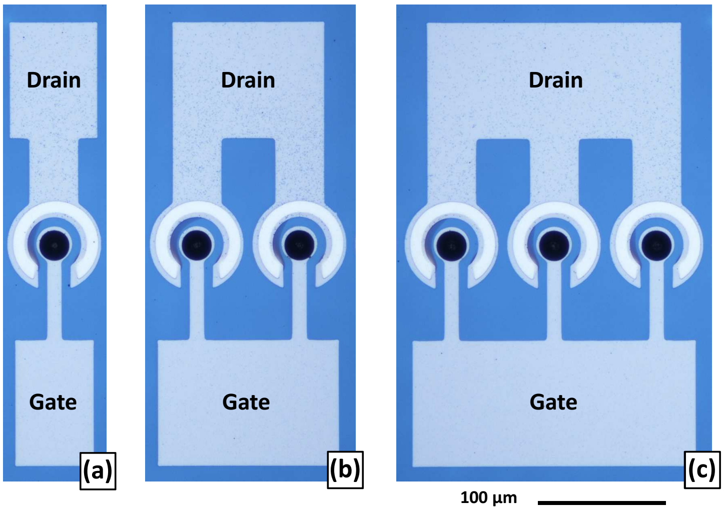


Fig. 4.2: Microscope photographs of the single (a), double (b) and triple (c) structures of the TSVFET

A depiction of the mask design can be found in the appendix A.2. It also holds electrical test structures for contact resistance measurements, MIS capacitors and others. The manufacturing of the TSV transistor and variations in the process flow are discussed in chapter **5 – Variations in the Integration Scheme of the TSV Transistor**.

4.2.2 Test Structures for Planar FETs

In order to develop the working process flows for different kinds of (TSV-) transistors, conventional planar structures have been used for n- and p-FETs. Since the setup is relatively easy and the fabrication can be done with high transistor yield, these were used as test vehicle for different gate dielectrics, metals and doping. The W/L ratio was kept constant at 3/1 in the design, gate lengths ranged from 150 ... 10 μm. Additionally, test structures for sheet resistance measurements of doped areas and metals, TLM structures for contact resistivity measurements, diodes and MIS capacitors have been included in the design.

Usually, 4 inch wafers with a moderately high p- or n-doping (1...10 Ωcm) were applied for n-FETs and p-FETs, respectively. This substrate doping predetermined the carrier concentration in the channel area of the fabricated transistors, thus making a simple four mask process possible.

- The first mask was used to achieve source and drain doping by diffusion through oxide windows (phosphorous or boron diffusion) or resist windows (gallium implantation).
- The second mask was designed to structure a field oxide (FOX) for the active area definition.
- The third mask contains the shapes to etch contact holes into the gate dielectric.
- The fourth mask was used to structure the metal layer that forms the gate as well as the source and drain contact lines.

The process flow differs – several material combinations and deposition techniques have been tested. The general integration flow, mentioning the different material and process possibilities, is shown in Fig. 4.3.

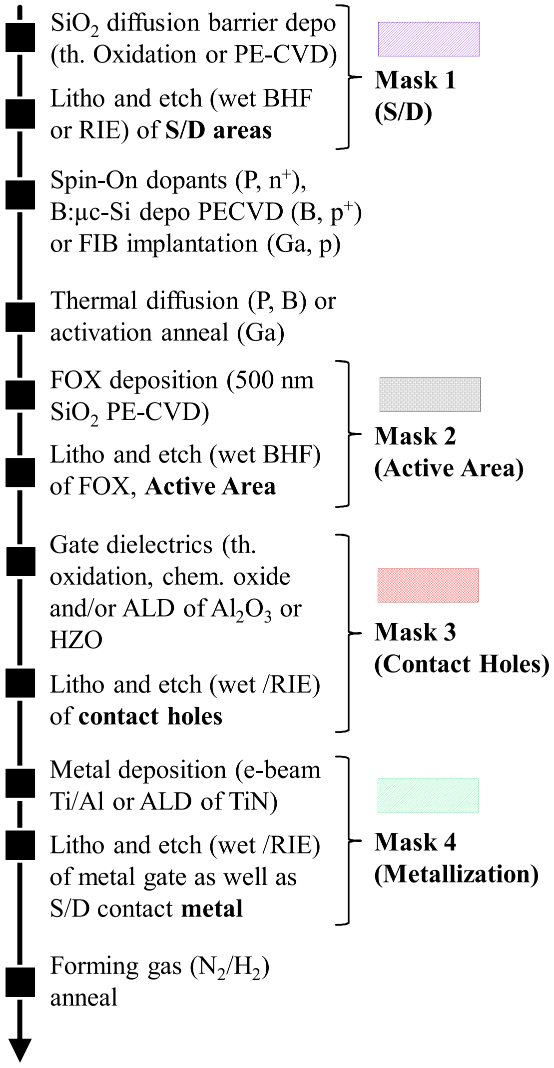


Fig. 4.3: Typical process flow for planar FETs

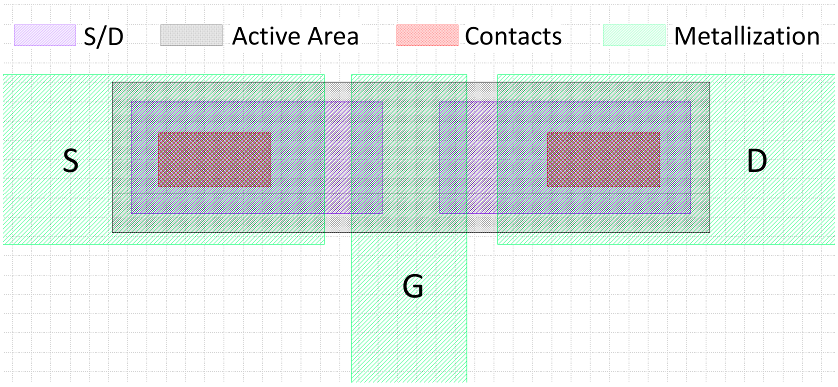


Fig. 4.4: Mask set for planar FETs, $L_G = 15\,\mu$m is shown

The mask structures needed for the manufacturing of the transistor can be seen in Fig. 4.4, an overview of the whole mask design is shown in the appendix A.3. It was used for structures investigated in chapter 5.2.1 (ferroelectric FETs) and 5.3.2 (S/D doped by implanted Ga).

5 Variations in the Integration Scheme of the TSV Transistor

The following chapter first addresses the manufacturing of n- and p-TSVFETs doped from thin films in chapter 5.1. Ferroelectric transistors (FeFET) are discussed in chapter 5.2. Finally, doping by implantation of gallium from a focused ion beam (FIB) tool was investigated and is described in chpater 5.3.

5.1 Doping by Diffusion from Thin Films

In this work, the source and drain regions were mostly doped from thin layers providing the dopants.

As a precoating before performing a drive-in anneal, for n-FETs, spin-on dopants (phosphorous) were applied as dopant source, while for p-FETs, highly doped microcrystalline silicon (boron) was deposited using a PE-CVD process at 140 MHz.

Detailed knowledge about the doping concentration profiles resulting from corresponding process parameter variations such as diffusion temperature and time is essential for the manufacturing of transistors. In the following chapter 5.1.1, these doping profiles were obtained by the use of the DHE (Differential Hall Effect) method [86].

Chapter 5.1.2 describes the detailed manufacturing of the TSV transistor using doping by diffusion from thin films.The TSVFET is electrically characterized and some specifics of this new kind of transistor structure are discussed.

5.1.1 Determination of Doping Profiles

Silicon doping was one of the process steps that needed to be introduced to the facilities at the IHM of TU Dresden, in order to be able to fabricate active devices such as field-effect transistors. The correct knowledge about doping concentration profiles and junction depths help to design the possible geometries and performance of the resulting transistors. As described in chapter 3.1.3, DHE is a method that takes only electrically active doping ions into account. An anisotropic silicon etcher (STS ASE) was used for repetitive thin layer removal, needed for DHE. Fig. 5.1 illustrates the processing and measurements that were done to obtain the dopoing concentration.

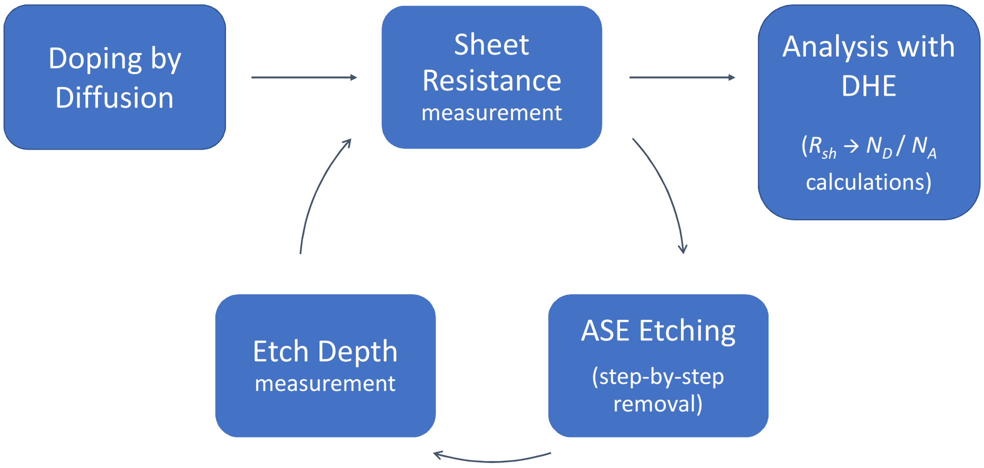


Fig. 5.1: Doping profile determination by thin layer removal and repetitive resistance measurements

The phosphorous doping supply for n-doping was the spin-on dopant solution P-8545 from Honeywell Inc. spun on at a maximum speed of 4000 rpm to achieve a thickness of 100 nm after drying at 250 °C for 10 min. As substrate, a p-doped Si wafer ($5 \cdot 10^{15}\ \mathrm{cm}^{-3}$) of 525 μm thickness was used.

Boron doping was done from a micro-crystalline layer of highly boron doped Si. A 125 nm thick layer was deposited by a PE-CVD process [68]. Trimethylborane (TMB) was used in the process as the source of boron. The process parameters for this deposition can be found in Tab. 5.1. The substrate was an n-doped Si wafer with a thickness of 525 μm and phosphorous concentration of about $1 \cdot 10^{15}\ \mathrm{cm}^{-3}$.

Power	Pressure	Time	TMB	SiH_4	H_2	Temp.	Plasma Frequency
44 W	0.2 mbar	15 min	0.038 sccm	1.5 sccm	198 sccm	200 °C	140 MHz

Tab. 5.1: Process parameters for the highly boron-doped μc-Si deposition

The diffusion processes were done at various temperatures and for different times. The variations are summarized in Tab. 5.2.

	n-doping (SOD P-8545) and p-doping (B:μc-Si)				
	900 °C	950 °C	1000 °C	1050 °C	1100 °C
30 min	n / p	n	n / p	n	n / p
60 min	n / p	–	n / p	–	n / p
120 min	n / p	–	n / p	–	n / p

Tab. 5.2: Phosphorous doping from the SOD P-8545 from Honeywell Inc. and boron doping from highly doped μc-Si

Fig. 5.2 exemplarily shows the furnace processes for 30 min phosphorous diffusions at different temperatures. Since the furnace has to be heated up with the door closed, the samples are thermally treated during ramping and diffusion takes place for temperatures lower than T_{max} as well. Thus, the ramp-up and -down times were kept constant as much as possible.

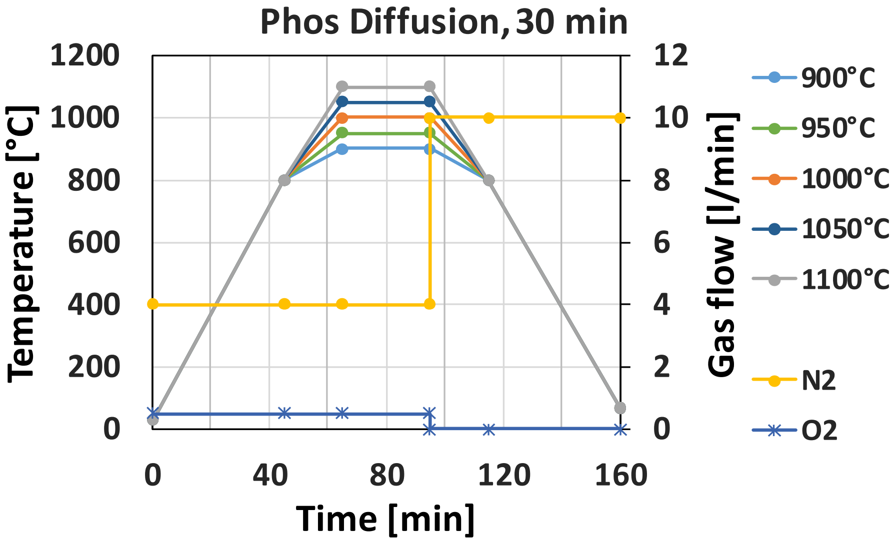


Fig. 5.2: Diffusion processes for phosphorous, 30 min holding time at T_{max}

After the diffusion process, the SOD was removed by BHF wet etching – the μc-Si layer was left on top. Subsequently, 4-point-probes measurements were done alternating with etching as described in Fig. 5.1.

A recipe for the Si layer etching needed to be developed. A low etching rate in the range of <100 nm/min was required and a very smooth Si surface after etching (low roughness), good reproducibility and no polymer residuals from the process were required at the same time. Since the resistance of the doped Si is measured by a 4pp measurement, residuals of any kind (masking material, polymer, native oxide, ...) would increase the contact resistance and lead to measurement errors. The process was developed by J. Lijian during his diploma thesis work [87]. The chosen parameters were as follows:

Process Name	SF_6 [sccm]	C_4F_8 [sccm]	p [mbar]	P_{ICP} [W]	P_{HF} [W]	Etch Rate [nm/min]
Simold9	20	85	13	800	15	40
Simold10	15	85	13	800	15	24

Tab. 5.3: Process parameters for the repetitive Si etching

A masking material was needed to create a masked step to measure the thickness of the removed Si. This allows the determination of the measurement position (depth) in the concentration profile. Several candidates have been tested.

Aluminium – deposited by e-beam evaporation – was structured by lithography and wet etching. Its use lead to micro masking effects due to sputtering and reposition during the Si etching. Photo resist itself was consumed and thinned down during the etching step, which lead to an ambiguous depth measurement.

The choice fell on Kapton^{TM} tape (adhesive polyimide foil) which is highly resistant against the etchant and stable at high temperatures of 200 ... 400 °C [113]. The doped samples were partly covered by the tape. After the etching, the tape was manually removed and the etch depth was measured with a Veeco Dektak Profiler 8 (7.5 Å 1σ repeatability). The etching processes were performed at a duration of 1 ... 4 min, depending on the position in the doping profile and if “Simold9” (rate 40 nm/min) or “Simold10” (rate 24 nm/min) was used.

The conversion of the R_{sh} measurements to doping concentration profiles was done as described in chapter 3.1.3. The resistivity ρ was calculated by a differentiation of the inverted R_{sh} curve and tabular values were used to derive the doping concentration from the resistivity. The resulting profiles for the phosphorous doping are summarized in Fig. 5.3 ... 5.6. A summary of the boron doping results is shown in Fig. 5.7.

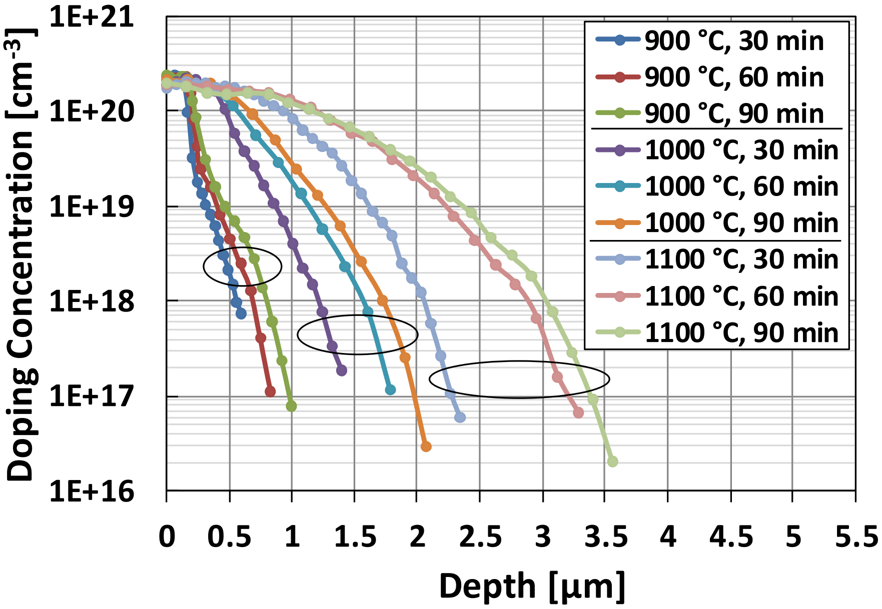


Fig. 5.3: Phosphorous doping – summary for 900 °C, 1000 °C and 1100 °C

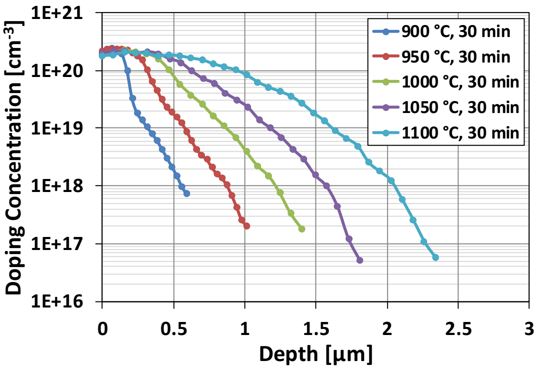


Fig. 5.4: Phosphorous doping for 30 min at different temperatures

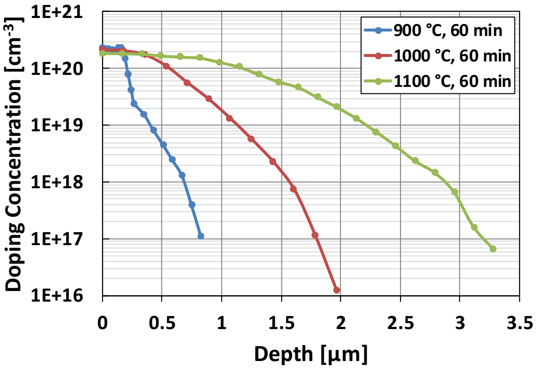


Fig. 5.5: Phosphorous doping for 60 min at different temperatures

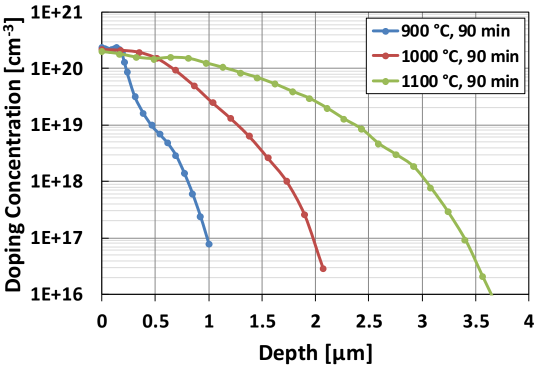


Fig. 5.6: Phosphorous doping for 90 min at different temperatures

For the phosphorous doping, the saturation concentration was reached for all cases. Since a low oxygen flow of 0.5 l/min was used in the diffusion process (see 5.2), a thin oxide was growing during the high temperature treatment. The pile-up of the concentration would be expected due to the segregation coefficient $m > 1$. Since the saturation concentration was already reached and more dopants do not further decrease the resistance, the 4pp measurements of the DHE method do not capture this. The concentration reaches a maxiumum of about $2 \cdot 10^{20}$ cm^{-3} in all cases and the dopants are then "pushed" deeper into the silicon by the growing SiO_2, thus this maximum concentration is also reaching into deeper regions. The SOD layer with a thickness of 100 nm seems to act as an infinite doping supply for the tested process conditions (up to 1100 °C for 90 min).

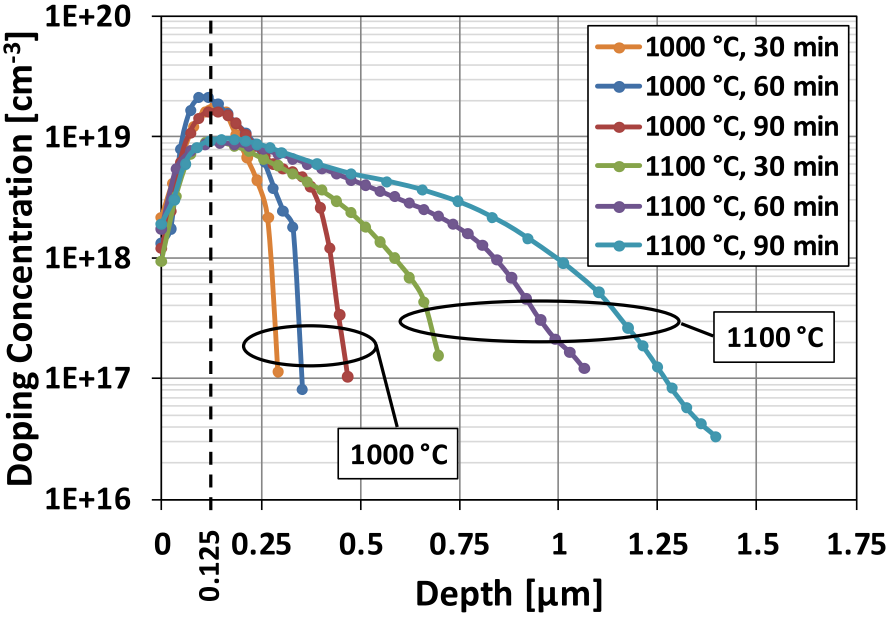


Fig. 5.7: Boron doping – summary for 1000 °C and 1100 °C

From literature it is known, that boron shows a much lower diffusivity in silicon than phosphorous ($D_{0,B} = 0.76\,\mathrm{cm^2/s}$ and $D_{0,P} = 3.85\,\mathrm{cm^2/s}$), while the values of the activation energies are nearly the same ($E_{A,B} = 3.46\,\mathrm{eV}$ and $E_{A,P} = 3.66\,\mathrm{eV}$) [114]. Thus, the diffusion length for B in Si is much lower compared to P in Si for the same process conditions. The junctions for 900 °C were very shallow, leading to very high resistances, making the use of the DHE method impossible. Consequently, only doping profiles for the diffusions at 1000 °C and 1100 °C are shown in Fig. 5.7.

The dashed line at a depth of 125 nm indicates the initial μc-Si layer, which was not etched back after diffusion. The lower doping concentration in that upper part originates from the grain boundaries in the μc-Si, resulting in higher resistivity for the same amount of charge carriers. The DHE method is not valid for that layer.

Two different maximum values are clearly visible with $2 \cdot 10^{19}$ cm^{-3} for the 1000 °C and $9 \cdot 10^{18}$ cm^{-3} for the 1100 °C diffusions. They can be attributed to two different μc-Si PE-CVD depositions and give a good hint on process stability. The boron content in the B:μc-Si layer slightly varies for individual depositions. For the fabrication of transistors, this layer was usually removed by a sacrificial oxidation (wet, 1000 °C, 40 min). This always leads to further diffusion and therefore a reduction of the surface concentration – in addition to the pile-down at the growing Si–SiO$_2$ interface.

The DHE method has been verified by SIMS measurements, done at the material analysis lab (MALab) of GLOBALFOUNDRIES Dresden. Two samples with shorter and two with longer diffusion lengths were chosen for comparison (see Tab. 5.4).

Doping	Process parameters
n (SOD)	900 °C, 30 min
n (SOD)	1100 °C, 60 min
p (μ-Si)	1000 °C, 30 min
p (μ-Si)	1100 °C, 60 min

Tab. 5.4: Diffusion parameters for the comparison of DHE and SIMS

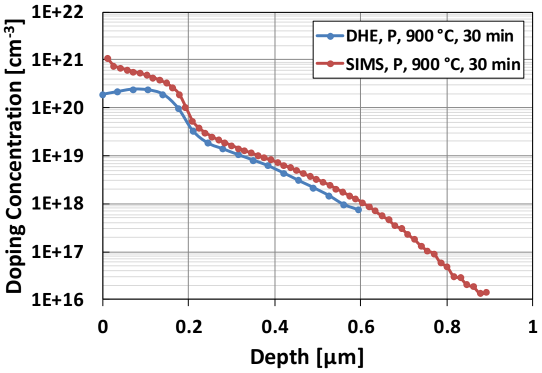


Fig. 5.8: Comparison of DHE and SIMS measurements for phosphorous doping (900 °C for 30 min)

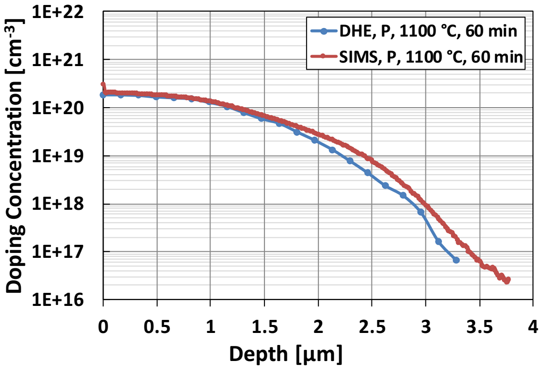


Fig. 5.9: Comparison of DHE and SIMS measurements for phosphorous doping (1100 °C for 60 min)

The SIMS results for the phosphorous doping are in good agreement with the DHE outcomes. SIMS detects all dopants (substituted as well as interstitial) and DHE takes only electrically active ones (4pp measurement) into account – that describes the slightly higher concentration obtained by SIMS, depicting the pile-up effect. Furthermore, the SIMS curves show phosphorous ions at lower concentrations, demonstrating its higher sensitivity and the limitation of measurements of high resistances.

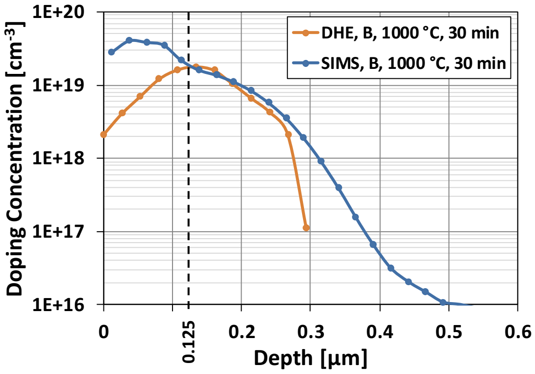


Fig. 5.10: Comparison of DHE and SIMS measurements for boron doping (1000 °C for 30 min)

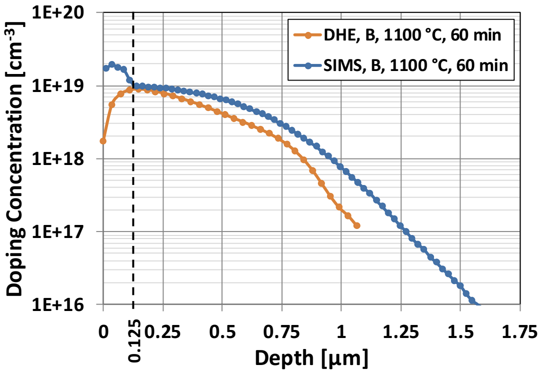


Fig. 5.11: Comparison of DHE and SIMS measurements for phosphorous doping (1100 °C for 60 min)

For the boron doping, DHE and SIMS show large differences in the upper area, where μc-Si is covering the single crystalline n-Si wafer material. The large content of grain boundaries in the μc-Si causes a higher resistivity – the conversion from ρ to N_A by the use of tabular values for sc-Si is therefore giving misleading values. Dopant gettering of the grain boundaries in multi-crystalline Si is a known phenomenon [115], [116] and contributes to the resistivity increase as well. Therefore, SIMS reveals higher dopant concentrations in the μc-Si layer. For 1000 °C and 30 min, the diffusion length is relatively short, which increases the error for the DHE method due to the very high resistivity.

However, in general, the results from the DHE method could be confirmed by the SIMS measurements.

Equations 2.3.4 (erfc profile – diffusion from infinite source) and 2.3.5 (gaussian profile – diffusion from limited dopant supply) described in chapter 2.3.1 were derived under the assumption of a constant diffusion coefficient. This only applies for a carrier concentration lower than the intrinsic concentration n_i at the corresponding diffusion temperature (e.g. $n_i \approx 5 \cdot 10^{18}\text{cm}^{-3}$ for 1000 °C [117]). The doping concentration exceeds n_i for all diffusions, thus it is called "extrinsic" and the calculation of the profiles gets more complicated. The rising electrical field, that is introduced by the charge of the dopant atoms, drives the dopants in addition to the concentration difference [118].

There is a practical use for the results presented here (knowledge will be used for the fabrication of active devices), but the mathematical adaption to the theory of thermal diffusion was not the focus of this work.

5.1.2 n- and p-TSVFETs Manufactured by the Use of the Diffusion Technique

Parts of the following chapter 5.1.2 were published in IEEE Electron Device Letters (EDL) [119] (mentioned on the cover of the Oct. 2018 issue), at the IEEE International Interconnect Technology Conference 2019 (IITC) [120] (invited as best student contribution) and as a poster at the IEEE Semiconductor Interface Specialists Conference 2018 (SISC) [121].

The manufacturing of the TSVFETs is discussed first. In the second part, the devices are electrically characterized and in the third part, simulations done in LTspice, TCAD (Technology Computer Aided Design) from Synopsis and in Ginestra^{TM} from MDLSoft Inc. are presented.

Device Fabrication

The process flow for the fabrication of the TSV transistor is shown in Fig. 5.12. The figures represent the manufacturing of n-TSVFETs. For p-TSVFETs the processing sequence is identical, only the doping type is inverted. A p-doped Si (100) wafer of 200 μm thickness with a boron concentration of about $5 \cdot 10^{15}$ cm^{-3} was used as substrate for the n-TSVFETs. The p-TSVFETs were fabricated on n-doped Si (100) wafers of 300 μm thickness with a phosphorous concentration of about $1 \cdot 10^{15}$ cm^{-3}. The difference in wafer thickness had no technical reasons and founded only on the availability of suitable substrates. The doping concentration needed to be in a range, were single digit threshold voltages could be expected. This ensured the possibility to meet sufficient material property requirements such as dielectric breakdown voltages.
A first lithographically structured resist mask (AZ5214E, 2 μm thickness) was used to etch 1 μm deep alignment crosses into the silicon substrate placed right along a vertical symmetry line. Etching was done by reactive ion etching (RIE) with SF_6. The whole design was aligned along this line, allowing the same masks to be used for the front and back side of the wafers.
The diffusion barrier for the subsequent doping was formed by a 500 nm SiO_2 layer, deposited by a silane PE-CVD process at 340 °C using SiH_4 and N_2O. The second lithographic mask was used to structure this SiO_2 by wet chemical etching with buffered HF (BHF). These oxide windows define the drain areas at the front side of the substrate and therefore the active area. The n$^+$ doping for n-TSVFETs was done by thermal

diffusion from the SOD P-8545 (phosphorous; Honeywell) at 1000 °C for 60 min. The resulting junction depth was 2 μm with a surface concentration of about $2 \cdot 10^{20}$ cm^{-3} (see chapter 5.1.1). The p^{+} doping (for a p-TSVFET) was done from a 125 nm thick layer of highly boron-doped micro-crystalline silicon (B:μc-Si) at 1000 °C for 60 min [68]. Fig. 5.12a summarizes these steps. After the diffusion process, a sacrificial thermal wet oxide (1000 °C, 40 min) was grown. The junction depth resulting from these two high temperature steps was ≈0.5 μm and a surface concentration of about $5 \cdot 10^{18}$ cm^{-3} was achieved (see also chapter 5.1.1). Both, the SOD layer (n-doping) or the oxidized B:μc-Si layer (p-doping) were then removed by wet etching with BHF.

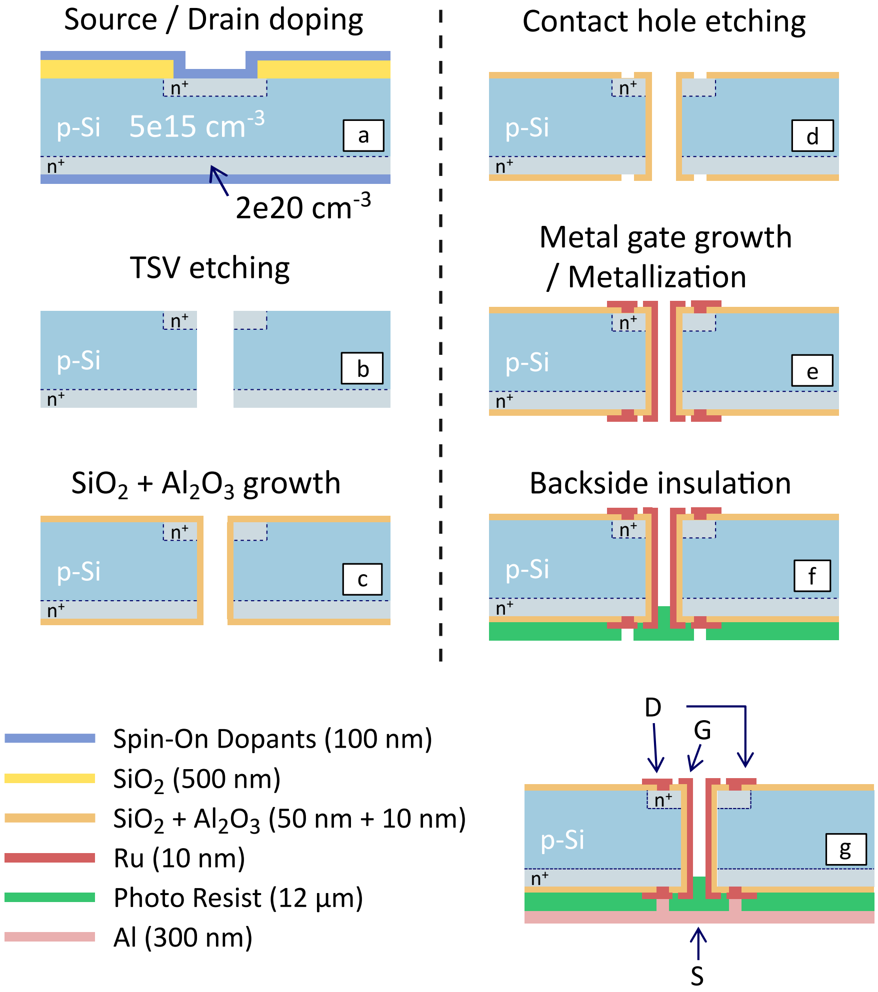


Fig. 5.12: Process sequence for the manufacturing of the n-TSVFETs

As shown in Fig. 5.12b, the TSVs were etched in the next step. A third lithographic mask was used with thick photo resist without any hard mask (n-TSVFET: 12 μm of AZ4562, 200 μm etch depth / p-TSVFET: 15 μm of AZ9260, 300 μm etch depth). A Bosch process was used for TSV etching – a procedure with alternating processes of etching (SF_6) and polymer passivation layer deposition (C_4F_8) [122]. So-called "notching" is a known problem when insulating materials are used as etch stop layers. Due to the ion bombardment of the stop layer, it gets positively charged and further incoming ionized etching species are deflected towards the sidewalls. This results in a larger opening at the bottom of the hole (back side of the wafer) but can be prevented by the use of a conducting etch stop layer [66]. 50 nm Al was deposited on the back side of the wafer by electron beam evaporation before TSV etching. The Al layer was afterwards removed by wet etching with a mixture of phosphoric and acetic acids. Since the surface of the TSV hole will later serve as the channel of the device, smooth wall surfaces are highly desirable. Therefore, several cleaning steps followed the etching process. A wet cleaning process with N-Methyl-2-pyrrolidone (NMP) was done for 30 min at 55 °C to remove polymer residuals. This ensures a successful subsequent sacrificial wet oxidation process (1000 °C, 60 min) serving to smoothing the inside of the TSV [66]. The resulting oxide layer was then removed by a BHF procedure, supported by an ultrasonic treatment to guarantee the transport of fresh etchant inside the hole and reactants out of it. This wet oxidation process drives the dopants deeper into the bulk silicon. The n^+ (phosphorous dopants) junction depth shifts to about 2.2 μm and as a result of the pile-up at the Si–SiO_2 interface, the surface concentration remains very high. The p^+ junction depth extends to about 0.6 μm and the surface concentration is expected to decrease due to the pile-down during silicon oxidation.

As illustrated in Fig. 5.12c, the gate dielectric material was grown next. The best results (low leakage currents, high $I_{D,on}/I_{D,off}$ ratio, saturation of the output curves) was achieved with a relatively thick thermally grown SiO_2 of 50 nm thickness (dry O_2 process at 1000 °C) and a 10 nm thick Al_2O_3 layer on top (thermal ALD, TMA and H_2O as precursors, at 300 °C [123].

In the following step, contact holes were etched into the gate dielectric material. SiO_2 and Al_2O_3 can both be wet etched in one single step by the use of BHF. Both sides of the wafer were structured with a third lithographic mask, realizing access to drain at the front side and source at the back side of the wafer (Fig. 5.12d). The shape of the contact holes resembles three quarters of a circle to surround as much of the hole as possible, thus creating a large contact area and to reduce contact resistance (see also chapter 4.2.1).

For the metallization in Fig. 5.12e, thALD was employed as well [66], [124], [125]. Nominally 10 nm Ru was grown by the use of ECPR and H_2O as precursors at 250 °C. Since Ru does not form closed layers on top of SiO_2 but does form closed layers on Al_2O_3, the described stack of Al_2O_3 on top of a thermally grown SiO_2 was used as the gate dielectric. The metallization was patterned by a fourth mask, forming the metal gate as well as the contact metal for source and drain. Ru was etched by reactive ion etching (RIE) using an O_2 plasma process. This was followed by a forming gas anneal at 400 °C for 45 min.

An insulating material (in this case 12 μm AZ4562 photo resist) was spun on the wafer back side, preventing an electrical short connection between gate and source. The third mask (contact holes) was used again, as depicted in Fig. 5.12f. Photo resist was chosen, because it was easy to apply by a spin-on process and due to the high viscosity of AZ4562 it was bridging the holes, thus reliably insulating gate and source. Long-term stability in the presence of an electric field remains an open question. CVD grown or sputtered SiO_2 or an ALD grown insulator such as Al_2O_3 would be favorable in terms of electrical stability. A safe insulation will especially be possible after filling the TSVs using Cu ECD and therefore providing a planar surface, spanning the edges of the hole with the subsequently deposited insulator.

Finally, a layer of 300 nm Al was deposited on the back side by electron beam evaporation. Fig. 5.12g shows the completely prepared TSV transistor with its accessibility of source from the back (by the chuck of a measurement setup) – drain and gate can be contacted from the front side. In Fig. 5.13, SEM (Scanning Electron Microscopy) images of the TSVFET are shwon.

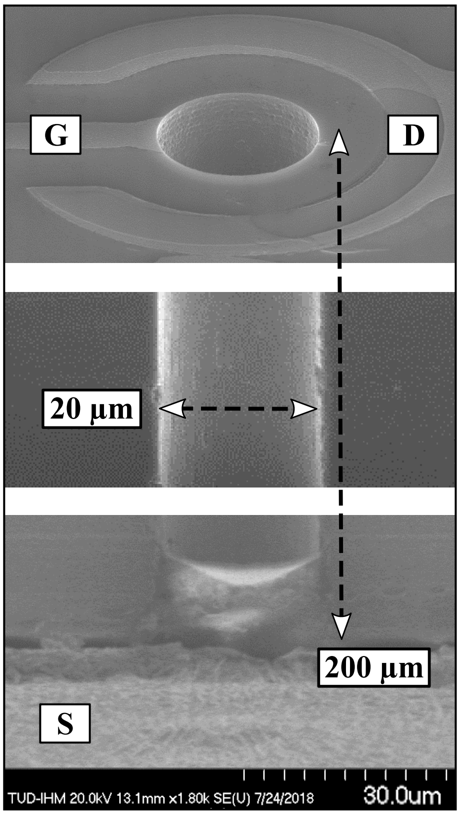


Fig. 5.13: SEM images of the upper, middle and lower part of the TSVFET

Electrical Device Characterization

The TSVFETs were electrically characterized with a Keithley 4200 Semiconductor Characterization System (SCS). Output (I_D over V_D) and transfer curves (I_D over V_G) were measured in DC mode.

Transfer Curve (I_D-V_G) Measurements

A threshold voltage of 2.31 V was obtained, as it is shown in Fig. 5.14 for n-TSVFETs with single, double and triple structures (gate length $L_G = 200\,\mu$m, hole diameter $d_{TSV} = 20\,\mu$m). The work function (W_F) value of 5.6 eV of Ru was determined by UPS (ultraviolet photoelectron spectroscopy) measurements [126]. Its high value leads to a relatively high V_{th} and is in good agreement with calculations for the present stack of gate dielectrics and channel doping. The possibility to decrease this high V_{th} will be shown later in the modeling section.

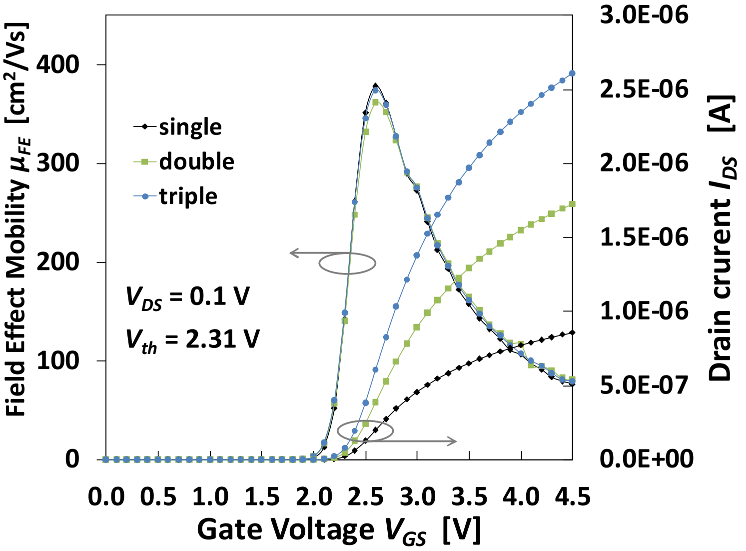


Fig. 5.14: Transfer curves and calculated field-effect mobility for single, double and triple structures of n-TSVFETs with 200 μm gate length and a TSV diameter of 20 μm, gate stack: 10 nm Al_2O_3 on 50 nm SiO_2

For the p-TSVFETs, n-doped substrates with a higher thickness of about 300 μm were used. The TSV etching process was not optimized for an aspect ratio of 15:1, which lead to stress and cracks in the photo resist and no working transistors (very high gate leakage) with a TSV diameter of 20 μm. The side walls of these holes were found to be significantly rougher than for 200 μm thick p-doped wafers. However, the p-TSVFET devices with a hole diameter of $d_{TSV} = 40\,\mu$m and a gate length of $L_G = 320\,\mu$m (the total thickness variation (TTV) of the n-doped wafers was ±20 μm) exhibited good transistor behavior. They showed a threshold voltage of -1.5 V, as depicted in Fig. 5.15.

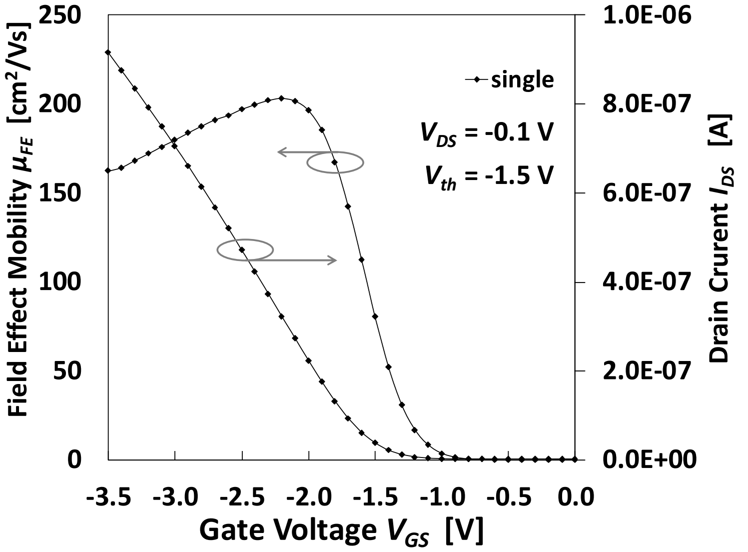


Fig. 5.15: Transfer curve and calculated field-effect mobility for a single p-TSVFETs with 320 μm gate length and a TSV diameter of 40 μm, gate stack: 10 nm Al_2O_3 on 50 nm SiO_2

The channel surface is far from being perfectly smooth, although the inside of the TSVs was cleaned by wet processes and smoothed by a sacrificial oxidation. The treatment reduced defects, but remaining irregularities lead to fixed oxide charges, interface-state charges and localized charges due to ionized impurities in the thermally grown gate oxide. These charges act as scattering centers and lead to a rather low steepness of the transfer curves [100]. For the n-TSVFETs, the corresponding field effect mobility could be found to be about 378 cm^2/Vs and for the p-TSVFETs it was 203 cm^2/Vs. As expected, μ_{FE} is lower for the p-FETs, since hole mobility is lower compared to electron mobility [127]. A sub-threshold slope of 125 mV/dec could be found for the n-TSVFETs, which is rather high. This "slow" switching can be explained with the high amount of charge traps to be charged and discharged, which is even more pronounced for the p-TSVFETs with 370 mV/dec.

Output Curve (I_D-V_D) Measurements

The output curves of the n-TSVFETs show a very stable saturation up to at least $V_{DS} = 5$ V. To prevent an electrical breakdown across the insulating photo resist at the backside of the transistor, higher voltages have not been applied. The $I_{D,on}/I_{D,off}$ ratios shows very high values above 10^6 – an excellent switching behavior. The contacts are not completely ohmic, a Schottky-like part can be seen for Ru on n$^+$-Si in Fig. 5.16 (especially visible in comparison to LTspice simulations in Fig. 5.24). The TLM structures were used to determine the contact resistivity – it was measured to be $6 \ldots 9 \cdot 10^{-3}$ Ωcm^2, which is several orders higher than for typical contact metals such as Ni, Ti, Co or others [128], [129]. A stack of TaN/Ru resulted in clear Schottky-like contacts (see also [119]) and should preferably not be used – TaN is a common choice as Cu diffusion barrier for TSV hole filling [130], [131], [132].

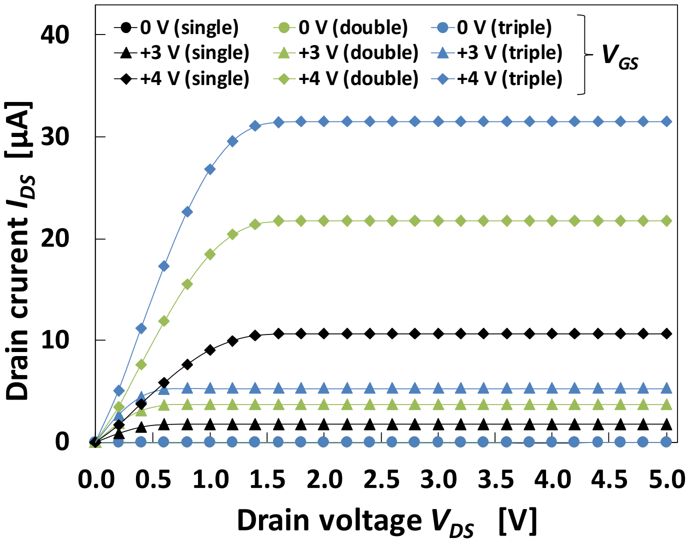


Fig. 5.16: Output curves for single, double and triple structures of n-TSVFETs with 200 μm gate length and a TSV diameter of 20 μm, gate stack: 10 nm Al_2O_3 on 50 nm SiO_2

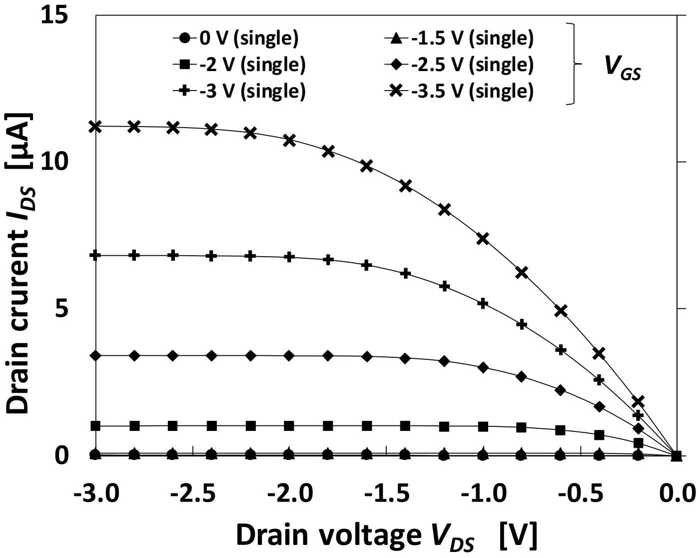


Fig. 5.17: Output curves for a single p-TSVFETs structure with 320 μm gate length and a TSV diameter of 40 μm, gate stack: 10 nm Al_2O_3 on 50 nm SiO_2

The output curves of the p-TSVFETs are very stable in saturation. A good (ohmic) contact could be found for Ru on the p$^+$-Si, as shown in Fig. 5.17. The contact resistivity extracted from TLM structures was found to be $5 \cdot 10^{-3}\ \Omega\text{cm}^2$, which was in the lower range of the values for the n-TSVFETs. The switching is characterized by an $I_{D,on}/I_{D,off}$ ratio of 10^3.

Calculation of the Density of Gate Interface States and Gate Leakage

As mentioned before, the channel is not perfectly smooth and holds many sites for trapped charges. Low-frequency (lf) and high-frequency (hf) C-V measurements on the gate were done in order to obtain the density of interface traps resulting from the processing of the TSV holes. A quasi-static (low-frequency) C-V measurement could not be performed (high gate leakage lead to ambiguous measurements), C-V measurements with 10 kHz and 1 kHz have been compared instead. D_{it} was calculated by equations 5.1.1 and 5.1.2, already discussed in chapter 3.2.2.

$$C_{it} = \left(\frac{1}{C_{lf}} - \frac{1}{C_i}\right)^{-1} - \left(\frac{1}{C_{hf}} - \frac{1}{C_i}\right)^{-1} \tag{5.1.1}$$

$$D_{it} = \frac{C''_{it}}{e^2} \tag{5.1.2}$$

The C-V sweeps were done on the gate – bulk (the substrate), source and drain were connected to ground. The gate dielectric stack was prepared in various ways. Thinner SiO_2 layers with a thickness of 1.6 nm (native oxide), 2 nm (piranha oxide, chemically treated for 10 min, H_2SO_4:H_2O_2, ≈3:1, starting at 110 °C, then cooling down) and 4.5 nm (thermally grown) were each covered with Al_2O_3. The case discussed in the device characteristics part (50 nm thermally grown SiO_2 and 10 nm Al_2O_3) was investigated as well.

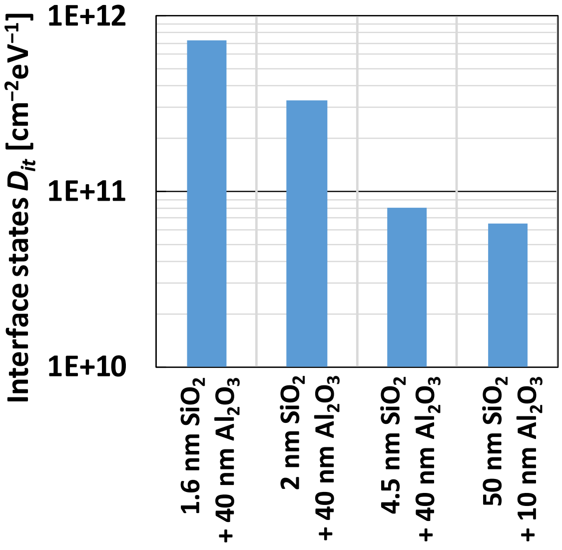


Fig. 5.18: Calculated interface states for different gate stacks for n-TSVFETs with a diameter of 20 μm and a gate length of 200 μm

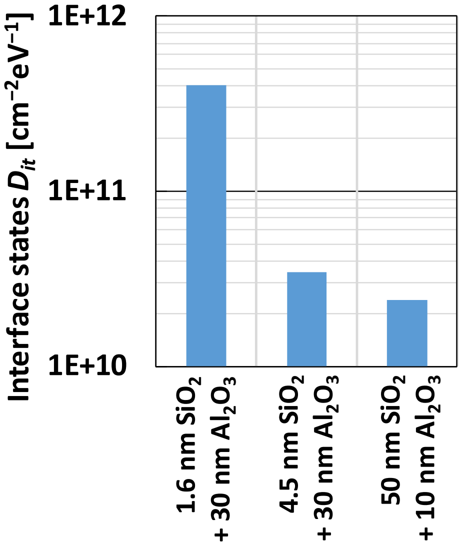


Fig. 5.19: Calculated interface states for different gate stacks for p-TSVFETs with a diameter of 40 μm and a gate length of 300 μm

As shown in Fig. 5.18 and Fig. 5.19, the density of interface traps shows reasonably low values (higher 10^{10} cm^{-2}eV^{-1} range for the thicker SiO_2 layers), which is expected for good Si–SiO_2 interfaces after forming gas (H_2 in N_2) anneals [96] or when small amounts of gaseous HCl are added to the dry-oxygen-gas stream [133]. Since the lf-C-V measurements were replaced by ones at 1 kHz, the real values are expected to be higher, since more charges would be able to follow the field and more traps would be charged at even lower frequencies. Despite that, the trend meets the expectation of lower densities for thicker oxide layers. The oxide layer growth is consuming defect sites (rough surface) remaining from the Bosch etching process by smoothing the etched surface.

Although the C-V curves appear as expected (accumulation, depletion and inversion were clearly visible), the transistors with the thin SiO_2 interface layers (1.6 nm native oxide, 2 nm chemical oxide (piranha, n-FET only) and 4.5 nm thermally grown) resulted in a very low transistor yield. This applies for n-TSVFETs as well as for p-TSVFETs. Exemplariliy, output and transfer curves of an n-TSVFET with a 2 nm piranha oxide interface layer and 40 nm Al_2O_3 are shown in Fig. 5.20 and 5.21. The threshold voltage is expected to be 1.7 V, but is shifted to a much higher value of $V_{th} = 3.3$ V, indicating a high total amount of negative charge ($\approx 10^{13}$ cm^{-2} coming from traps at the interface, inside the SiO_2 and from charge in the high-k layer).

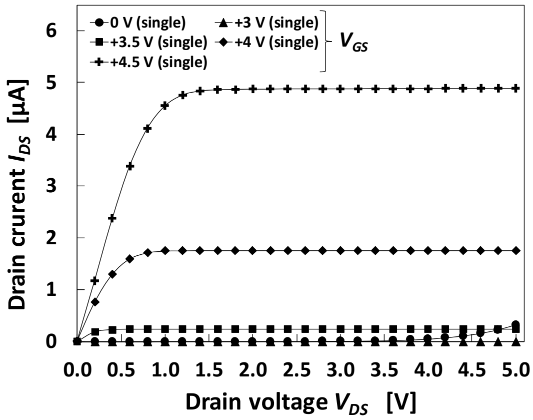


Fig. 5.20: Transfer curves of a single n-TSVFETs with 2 nm piranha oxide and 40 nm Al_2O_3 in the gate stack

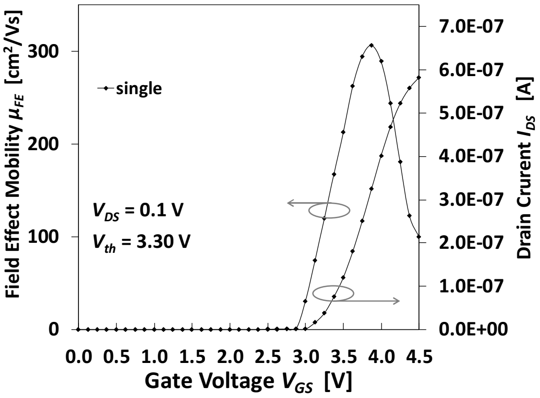


Fig. 5.21: Transfer curve of a single n-TSVFETs with 2 nm piranha oxide and 40 nm Al_2O_3 in the gate stack

Most of the transistors with a thin interface layer were showing non-saturating output curves with no sign of amplification by the application of gate voltages V_G. Thus, the gate currents were measured (Fig. 5.22 and Fig. 5.23).

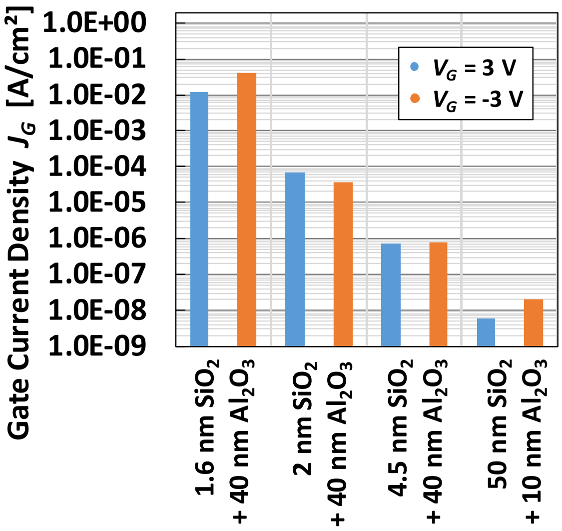


Fig. 5.22: Gate current density for n-TSVFETs with a diameter of 20 μm and a gate length of 200 μm for different gate stacks

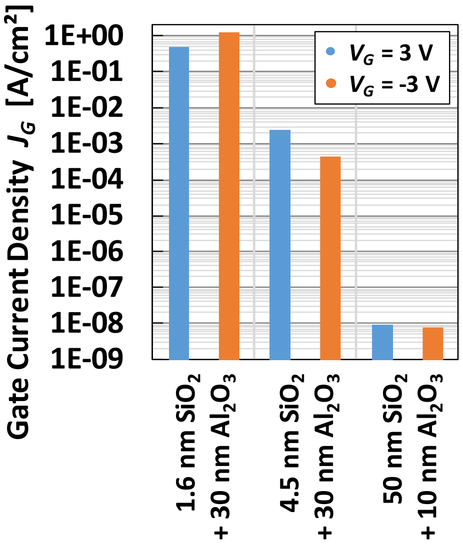


Fig. 5.23: Gate current density for p-TSVFETs with a diameter of 40 μm and a gate length of 300 μm for different gate stacks

As expected, the gate leakage is very low for the thickest SiO_2 layer. For the case of 4.5 nm thermally grown SiO_2 with 40 nm Al_2O_3, the gate current is two orders of magnitude higher than for the conventional planar p-FeFETs discussed in chapter 5.2 – even though, it was manufactured using the same processes and a similar dielectric stack (4.5 nm thermally grown SiO_2 with hafnium-zirconium-oxide). This can be accounted to a much higher defect density for the TSVFETs compared to the channel region of the FeFETs (polished Si wafer surface) [97]. The transistors with very thin interface oxide layers show very high gate leakage, explaining the non-existent amplification in most cases.

Simulations in LTspice (n-TSVFET)

Simulations in LTspice [134] were done with an NMOS model (level 3) for a single n-TSVFET. The following parameters were used:

.model NMOS(LEVEL=3 L=200u W=63u VTO=2.31 TOX=55n TPG=0 U0=378)

For all the other parameters, the default values were left unchanged. The channel length **L** (200 μm) and channel width **W** (63 μm, circumference of the TSV holes with 20 μm diameter) were set according to the dimensions of the transistor. **TPG**=0 stands for a metal gate, the threshold voltage **VTO** was set to a fixed value of 2.31 V. A gate stack of 50 nm SiO_2 ($\varepsilon = 3.9$) and 10 nm Al_2O_3 ($\varepsilon = 8$) was used in the simulation. For the gate oxide thickness **TOX**, an equivalent oxide thickness (EOT) of 55 nm was calculated. The mobility **U0** was set to the maximum field-effect mobility of 378 cm^2/Vs, calculated from the measured I_D-V_G curves.

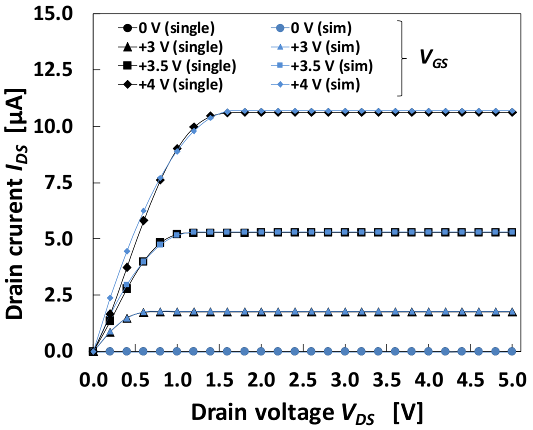


Fig. 5.24: Output curves (measured vs. simulated in LTspice) for a single n-TSVFETs with 200 μm gate length and a TSV diameter of 20 μm

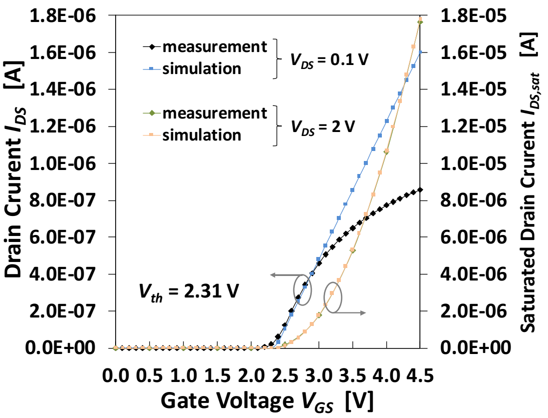


Fig. 5.25: Transfer curves (measured vs. simulated in LTspice) for a single n-TSVFETs with 200 μm gate length and a TSV diameter of 20 μm

The model fits very well for the output curves, as it can be seen in Fig. 5.24. A slight difference was found for lower $V_{DS} < 0.5\,\mathrm{V}$. The measured drain currents are slightly lower than the simulated ones, indicating Schottky-like contacts. The transfer curve (Fig. 5.25), that was measured and simulated for a low drain voltage of $V_{DS} = 0.1\,\mathrm{V}$, confirms this deviation and differs quite significantly from the measurement for higher gate voltages. This can be attributed to the non-ohmic contacts, as well as to channel roughness that is not considered in the simulation. Raising the drain voltage to $V_{DS} = 2\,\mathrm{V}$ (transistor in saturation), the improved agreement can be seen in the transfer curve as well.

In general, the n-TSVFETs resemble the basic electrical characteristics of conventional planar devices with the same geometrical dimensions. It should be noted, that only the DC case was investigated. The high frequency characteristics are expected to be inferior compared to planar devices – especially the gate overlap with source and drain cannot be prevented and is given by design, leading to high miller capacities. Even if the TSV holes would only be plugged and the gate contact is not pulled out of the hole onto the substrate surface (across the n^+ region), the overlap to source and drain would not be eliminated completely. Therefore, rather low switching speeds – compared to transistors with a self-aligned gate – must be expected.

Simulations in Ginestra^{TM} (n-TSVFET)

The commercially available multi-scale platform Ginestra^{TM} [135], [136] was additionally used to identify material combinations that could lead to better device behavior. The multiscale model describing the device operations is comprised of two main parts consistently connected. It is the device geometry and material modifications (left side in Fig. 5.26) and the charge transport (right side in in Fig. 5.26). This is crucial to model device aging and reliability phenomena as well as for an accurate assessment of interfacial defects and its impact on device performance. Since manufacturing is very time-consuming, a modeling approach can help to understand the key properties to be changed and could be used as a future tool to improve the TSV transistor characteristics.

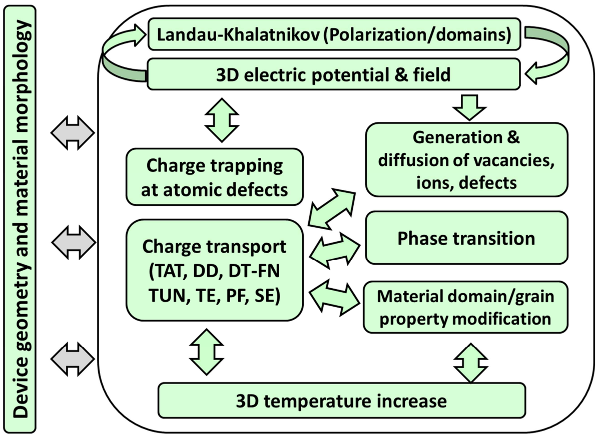


Fig. 5.26: Flow chart and schematic illustration of the multiscale modelling platform presented Ginestra^{TM} used for the simulation

A device structure equivalent was defined (see Fig. 5.27), resembling the gate stack of 50 nm thermally grown SiO_2, 10 nm Al_2O_3 and 10 nm Ru. The transfer curve I_D-V_G of a single n-TSVFET was simulated, as depicted in Fig. 5.28. The simulation is in good agreement with the experiment, successfully capturing the device physics and geometry. The volumetric defect density in the gate oxide stack was set to $n_{GOX} = 5 \cdot 10^{19}$ cm^{-3}, representing an area defect density in the SiO_2 of $N = 5 \cdot 10^{12}$ Defects/cm^2 at a distance of $d \leq 1$ nm to the Si–SiO_2 interface.

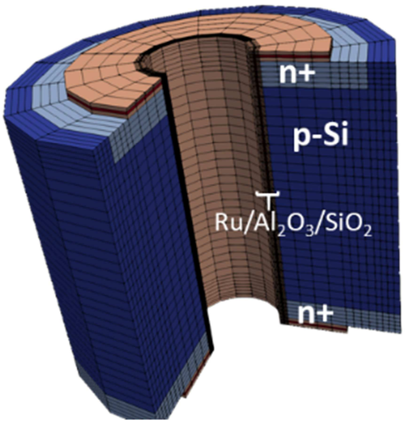


Fig. 5.27: Device geometry structure with the mesh

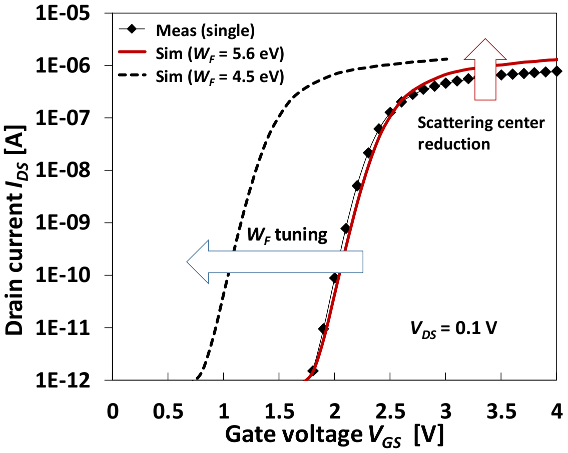


Fig. 5.28: Transfer curve I_D-V_G, simulated with Ginestra^{TM}

By replacing the Ru gate with TiN (which is typically used for state of the art high-k metal gate n-FETs [137], [138], [139], [140]), the possibility to decrease the threshold voltage could be shown by changing the work function W_F from 5.6 eV to 4.5 eV. A lower threshold voltage means higher output currents for the same operation voltages and therefore faster and more power-efficient switching.

The use of TiN leads to a higher CMOS manufacturing compatibility and would have been the obvious choice for this work as well. Though, there was no availability of a feasible process for the TiN deposition. As experimentally checked, PE-ALD was not an option, since the precursor excitation did not completely reach into holes of high aspect ratio. Due to collisions with the TSV side walls in the upper parts of the holes, no material could be deposited in deeper regions. However it was shown that thermal ALD of TiN is possible with suitable precursors [141], [142], [143] leading to a conformal deposition of high aspect-ratio structures.

Transistor-Transistor Interference – TCAD Simulations of n-TSVFETs

An obvious difference to planar transistors is the non-existent electrical isolation between neighboring devices. Therefore, the minimal distance of two TSVFETs with zero interference is of great interest. The vertical channel arrangement causes horizontal field expansion underneath the gate towards adjacent transistor channels. The width of the space charge region (SCR) underneath the gate dielectric for such MIS structures can be calculated by equations 5.1.3 and 5.1.4:

$$\Phi_{inv} = \frac{2k_bT}{e} \cdot ln\left(\frac{N_A}{n_i}\right) \tag{5.1.3}$$

$$w_{scr} = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0\Phi_{inv}}{eN_A}} \tag{5.1.4}$$

From a technological point of view, it is controlled by the doping concentration of the substrate material (N_A). With $N_A = 5 \cdot 10^{15}$ cm^{-3}, the inversion potential is $\Phi_{inv} = 0.33\,\mathrm{V}$ and with $\varepsilon_{Si} = 11.9$, the width of the space charge region is $w_{scr} = 416\,\mathrm{nm}$ wide. For $N_A = 1 \cdot 10^{15}$ cm^{-3} it is significantly wider, $w_{scr} = 869\,\mathrm{nm}$ in this case. Since the influence of the gate voltage on the potential curve under the gate is confined to these calculated values, no transistor–transistor disturbance would be expected for distances >1 ... 2 μm, originating from the SCR underneath the gate.

Technology Computer Aided Design (TCAD) simulations in Synopsis [144] have been performed in order to examine this relation. Since real 3D structures are not available in Synopsis, the structure in Fig. 5.29 has been used instead. Two planar transistors facing each other at the front and back side of a p-doped ($5 \cdot 10^{15}$ cm^{-3}) silicon substrate should represent two adjacent n-TSVFETs, rotated for a vertical setup in the figure. One obvious difference is the direction of the source and drain doping concentration decrease. The simulation allows only horizontal diffusions – the fabricated TSVFETs show a vertical drop in doping concentration. The distance d between the two transistors is indicated (2 μm in the depicted case). The junction depths ($N_D = N_A$) were set to 500 nm for a distance $d = 2\,\mu$m and to 50 nm for lower distances.

Transfer curves have been simulated for single n-TSVFETs with a gate dielectric stack of 10 nm Al_2O_3 on top of 50 nm SiO_2. The gate metal was Ru and the threshold voltage was set to 2.31 V (see the measured transfer curve in Fig. 5.14). Since the channel roughness and contact resistance could not be taken into account in the simulations, the transfer curves are not saturating as much as in reality. As a consequence, the simulated drain current values do not mirror the measurements. Nevertheless, the simulations exhibit the influence between neighboring transistors (caused by electrical fields) with a sufficient validity.

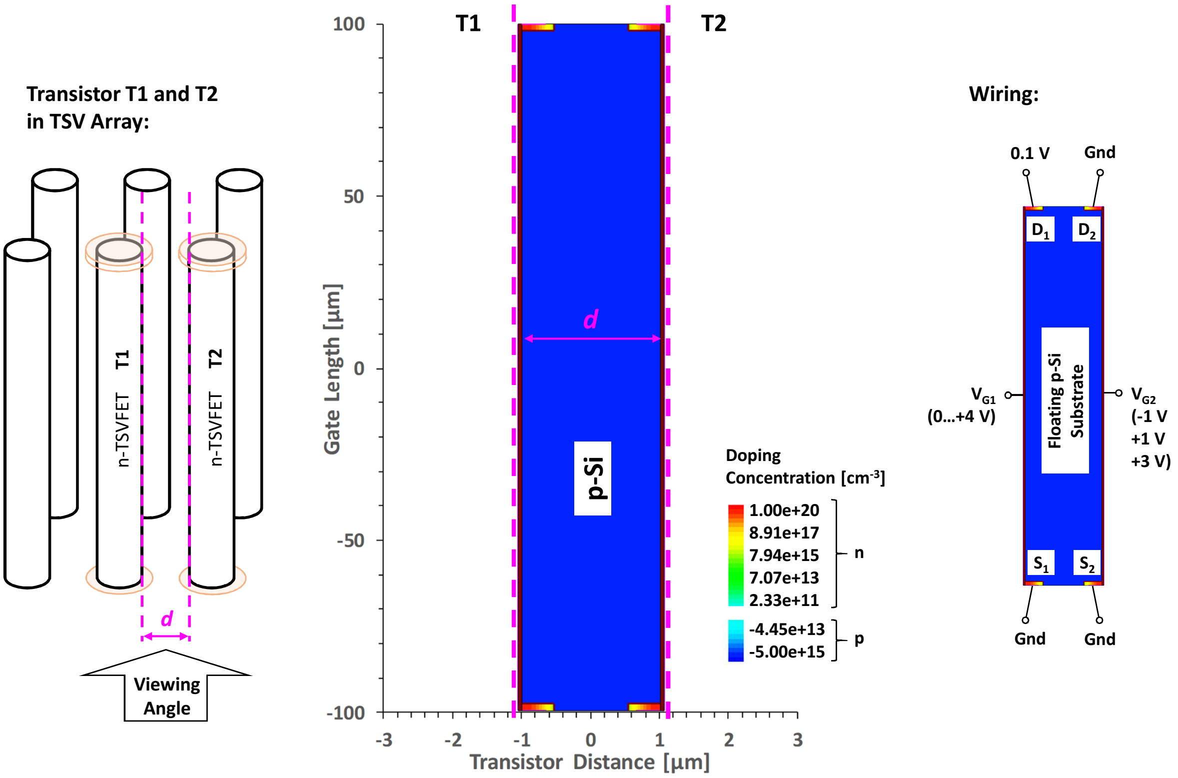


Fig. 5.29: Explanation of the simulated test structure, two adjacent n-TSVFETs with a distance of 2 μm and depiction of the wiring of sources and drains

The distance d was varied between 0.15 ... 2 μm. The drain voltage of T1 (left transistor 1) was fixed at $V_{D,1} = 0.1\,\text{V}$, source was at ground level. Drain and source of T2 (right transistor 2) were both connected to ground as well. The voltage $V_{G,2}$ at the gate of T2 was set to fixed values of -1 , +1 and 3 V. The transfer curves were generated for $V_{G,1}$ varying between 0 ... 4 V

Fig 5.30 depicts the influence of $V_{G,2}$ on the transfer curve of T1 for a separation of $d = 2\,\mu$m. Transistor T1 is not influenced by the gate voltage of T2 – the transfer curves look nearly identical. The drain currents of transistor T2 are very low, as it was expected due to its grounded source and drain junctions.

For $V_{G,2} = 3\,\text{V}$, an inversion layer is created underneath the gate of T2. The drain current of T2 raises by one order of magnitude from 10^{-13} A to 10^{-12} A. The direction of $I_{D,2}$ is out of the junction (negative sign), the electrons can only flow into the drain of T1.

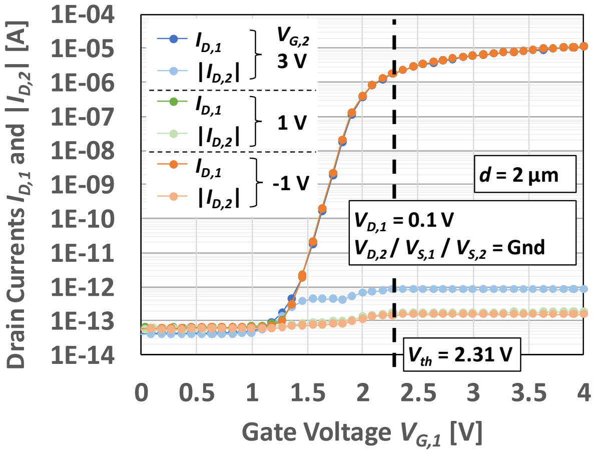


Fig. 5.30: Transfer curve of T1 ($I_{D,1}$ over $V_{G,1}$) and $|I_{D,2}|$ of T2 for a fixed transistor distance of $d = 2\,\mu$m

The electrostatic potentials for $V_{G,1} = V_{G,2} = 3\,$V are show in Fig. 5.31a. The maximum of 2.1 V originates from the work function difference of Si and the gate metal Ru, which is about 0.9 V. The slightly negative potential of the floating substrate can be explained with the p-doping, shifting the Fermi level down and the conduction band up – the potential is getting negative.

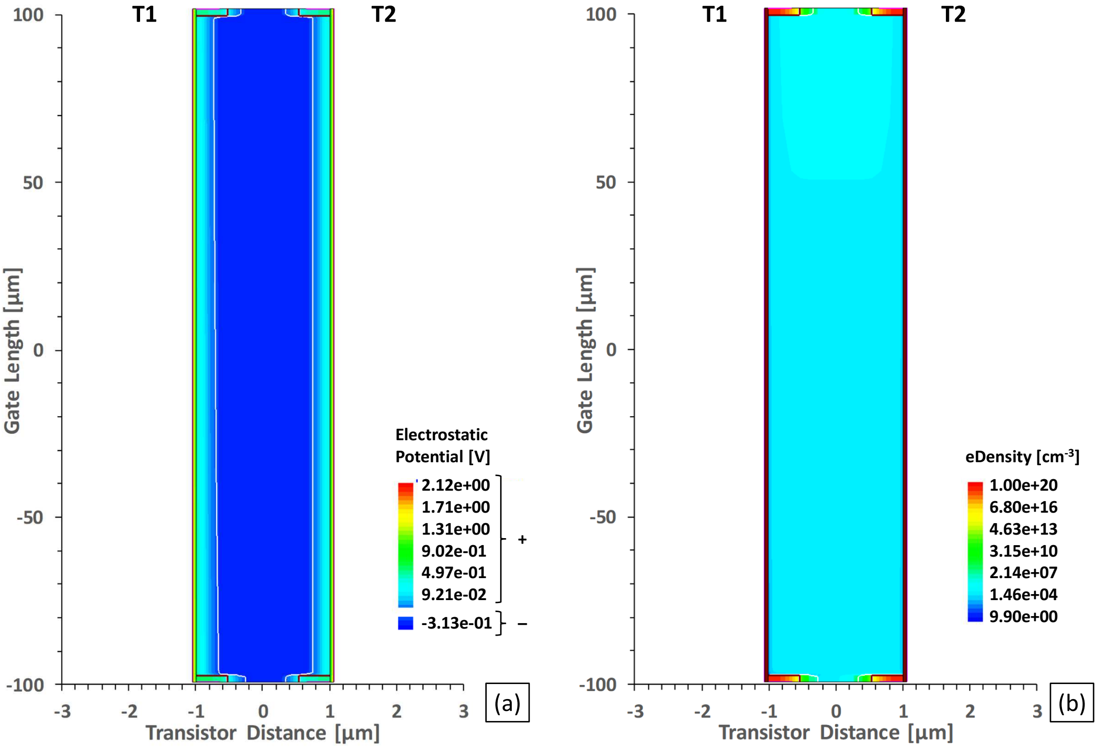


Fig. 5.31: (a) Potential ($V_{G,1} = V_{G,2} = 3\,$V) and (b) electron density ($V_{G,1} = V_{G,2} = 0\,$V) for a distance of $d = 2\,\mu$m

The space charge regions underneath the gates are not influencing each other, the electron density shown in Fig. 5.31b is rather constant for the bulk substrate and in between the source and drain regions of T1 and T2. In the space charge region surrounding the S/D regions, holes are depleted and therefore the electron concentration increases to satisfy $n \cdot p = n_i^2$. A raised electron concentration is clearly visible in the horizontal direction ($\approx 10^{10}$ cm^{-3}) – due to the size ratio it is not pronounced vertically in the depiction.

A constant gate voltage of $V_{G,1} = 3\,\text{V}$ was applied at T1, turning it on. Fig. 5.32 and Fig. 5.33 show the drain currents of T1 and T2.
The drain current $I_{D,1}$ of T1 is nearly identical for distances of 1.5 ... 2 μm. For a distance of $d = 0.7\,\mu$m it increases by approx. 1 μA or 18.5 % of the initial value. Simultaneously, the drain current of T2 goes up to a value of about 1 μA, providing the additional current flowing into the drain of T1.

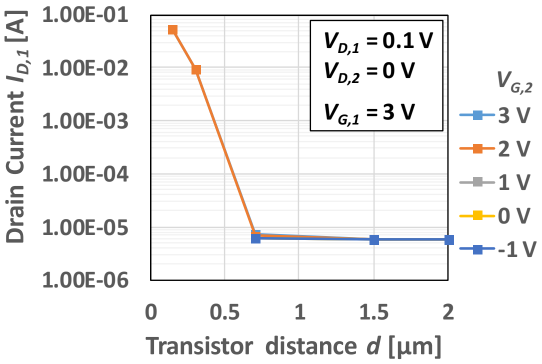


Fig. 5.32: Drain current of T1 for various transistor distances

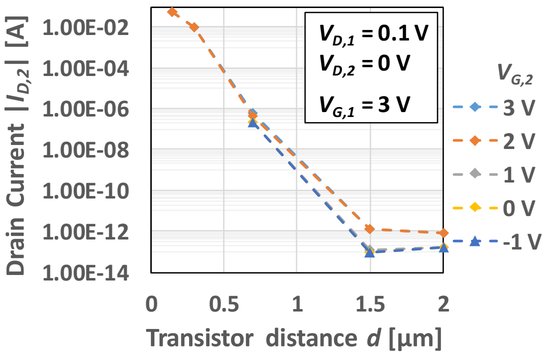


Fig. 5.33: Magnitude of the drain current of T2 for various transistor distances

The potential for $V_{G,1} = V_{G,2} = 3\,\text{V}$ and a separation distance of 0.7 μm is still very close to 0 (floating body), as depicted in Fig. 5.34a. As shown in Fig. 5.34b, the space charge regions underneath the source and drain regions ($\approx 3.5 \cdot 10^{10}$ electrons/cm^{-3}) are merging and start to form a short connection for $d = 0.7\,\mu$m. For the shorter distances (0.3 μm and 0.15 μm), the current from T2 to T1 raises to 10 ... 100 mA due to even higher electron densities between the S/D regions of the transistors.

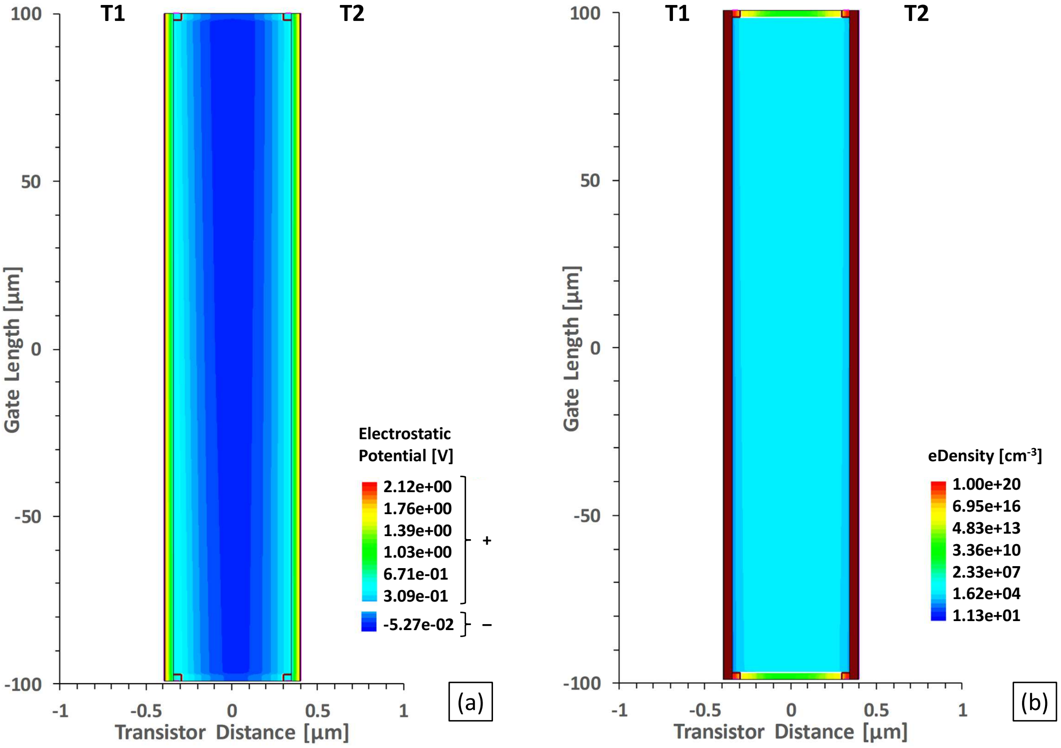


Fig. 5.34: (a) Potential ($V_{G,1} = V_{G,2} = 3\,\mathrm{V}$) and (b) electron density ($V_{G,1} = V_{G,2} = 0\,\mathrm{V}$) for a distance of $d = 0.7\,\mu\mathrm{m}$

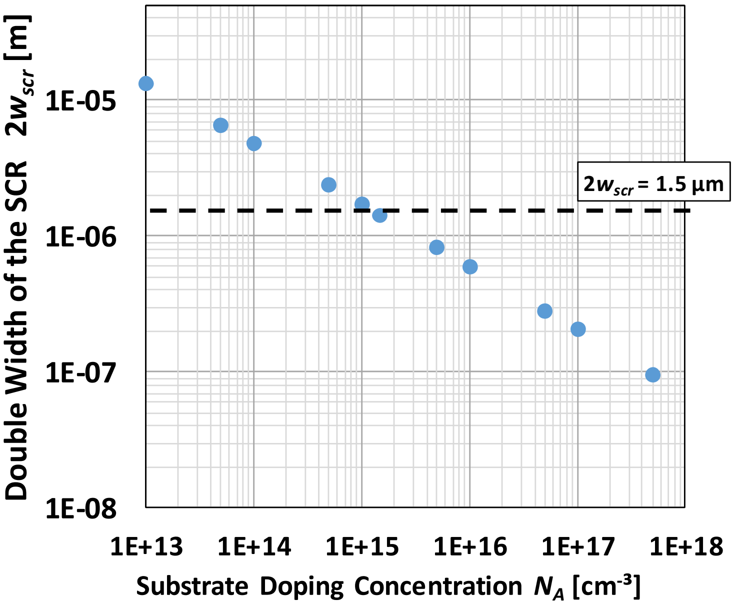


Fig. 5.35: Calculated double width of the space charge region ($2 \cdot w_{scr}$) underneath a MIS stack (e.g. transistor gate) to evaluate the needed TSV transistor distance for no transistor–transistor–disturbance

In summary, a distance of $d = 1.5\,\mu\mathrm{m}$ is sufficiently high for a substrate doping concentration of $5 \cdot 10^{15}\ \mathrm{cm}^{-3}$ and gate voltages up to 3 V. As already discussed, the width of the space charge region underneath the gate is controlled by the doping concentration of the substrate and can be calculated by equation 5.1.4. As shown in Fig. 5.35, the doping should not be lower than $1.5 \cdot 10^{15}$ cm^{-3} for a transistor distance of 1.5 μm, otherwise the SCRs of neighboring transistors ($2 \cdot w_{scr}$) would influence each other. The space charge region for substrates with very low doping concentrations in the range of 10^{14} cm^{-3} and below reaches several μm deep, requiring higher transistor distances. The minimal distance between the TSVFETs was designed to be 63 μm in this work, hence no transistor to transistor–to–transistor effect had to be expected and was not seen in the measurements.

An isolation between adjacent devices should be introduced to prevent a short connection of source and drain regions. Oxide filled trenches, e.g. STI (shallow trench isolation) or a recessed LOCOS (Local Oxidation of Silicon) isolation that reaches deep enough, could be used for that.

Comparison of the n-TSVFETs to Cu filled TSVs

The TSVFET replaces an electrical connection through an interposer in terms of functionality but not in terms of its electrical parameters. As electromigration experiments unveiled, Cu TSVs (filled by ECD) with an aspect ratio of 7.5 ($L = 15\,\mu$m length, $d = 2\,\mu$m hole diameter), endured currents of 180 mA for more than 100 h at a temperature of 270 °C [145]. Typical currents are in the mA range and single TSV connections should have resistances well below 1 Ω [146].

The resistances in the linear region of the I_D-V_D curves (differential resistance / small signal resistance) were extracted for several gate voltages and can be found in Tab. 5.5. Measurement data from the n-TSVFETs with 20 μm hole diameter and 200 μm gate length was evaluated. The gate stack was 10 nm Al_2O_3 on top of 50 nm SiO_2 with Ru as gate metal.

	n-TSVFET Resistance (linear regime)		
	Single	Double	Triple
$V_G = 1\,\text{V}$	$> 10^{11}\ \Omega$	$> 10^{11}\ \Omega$	$> 10^{11}\ \Omega$
$V_G = 2\,\text{V}$	2.2 GΩ	377 MΩ	338 MΩ
$V_G = 2.5\,\text{V}$	1.2 MΩ	521 kΩ	383 kΩ
$V_G = 3\,\text{V}$	268 kΩ	130 kΩ	90 kΩ
$V_G = 3.5\,\text{V}$	150 kΩ	73 kΩ	51 kΩ
$V_G = 4\,\text{V}$	110 kΩ	53 kΩ	36 kΩ

Tab. 5.5: n-TSVFET Resistance (linear region) for various gate voltages V_G

These resistances are very high and not even close to plain electrical connections made of Cu filled TSVs ($k\Omega$ well above V_{th} and $M\Omega$ ... $G\Omega$ below V_{th}). For $V_G = 4\,\text{V}$, the saturation currents are 10.6 μA (single), 21.8 μA (double) and 31.5 μA (triple), respectively. Characteristically, higher drain voltages V_D are not leading to higher drain currents for field-effect transistors – the additional voltage drops across the reverse-biased pn junction formed by drain region (n) and body (p).

One way to greatly increase these low drain currents is to change the geometry of the transistor. Shorter channels (and therefore higher W/L ratios), will result in proportionally higher output (drain) currents for the same gate material and unchanged operating voltages. One concept could be a recessed TSV hole, as it is shown in Fig. 5.36.

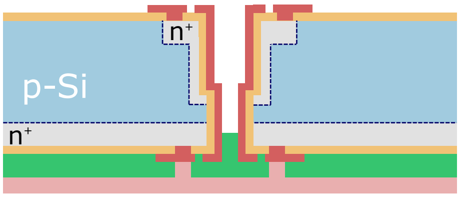


Fig. 5.36: n-TSVFET with recessed holes to create a shorter channel length L, resulting in higher drain currents

The manufacturing would start with the etching of blind holes from the front side, not completely perforating the substrate. The use of the phosphorous SOD enables doping at the bottom of the TSV holes and on the side walls, as the solution can fill up the blind holes. The substrates can then be punched through by etching of holes with a smaller diameter from the back side. All subsequent fabrication steps can be carried out in the same way as described in Fig. 5.12 above.

5.2 Ferroelectric Hafnium-Zirconium-Oxide (HZO) in the Gate Stack

Ferroelectric (FE) memories like FRAM and especially ferroelectric field effect transistors (FeFETs) are experiencing a renaissance with the discovery of ferroelectric properties [55] in hafnium and zirconium oxide. Fully CMOS compatible and scalable materials enabled the integration of a large number of ferroelectric gate devices spanning from ultra-scaled memory [147] and low-power logic devices [101] to devices dedicated to neuromorphic computing [148], [149] and devices for logic in memory [150]. So far, only n-FeFETs have been reported and discussed. However, to enable the full ferroelectric hierarchy [151] both p- and n-type devices should be available. In addition, independently of the application, all FeFETs suffer from the large field drop over the low-k interface (IF) layer which not only increases the power consumption required for the logic state (polarization) reversal but also decreases the lifetime and limits the endurance of these devices to about 10^5 program/erase (PRG/ERS) cycles [136], [152], [153]. In the follwing chapter 5.2.1, a p-FeFET with a large memory window (MW) is shown for the first time. Moreover, different integration schemes are investigated comprising structures with and without internal gate resulting in metal-FE-insulator-Si (MFIS) and metal-FE-metal-insulator-Si (MFMIS) devices.

The following chapter 5.2.1 is organized as follows: First, the integration scheme and fabrication flow is discussed. This is followed by a discussion about the impact of the IF and its thickness on the memory characteristics. In the last part the possible reduction of the interface layer field and operation voltage (drop over low-k IF layer) by using an internal gate approach and area factor scaling to tune the ratio between the ferroelectric and IF component of the voltage divider is discussed.

Most of these results were presented at the IEEE Device Research Conference 2019 (DRC) [154].

5.2.1 Planar ferroelectric p-MOSFETs Doped by Thermal Diffusion

Device Fabrication

An n-doped Si (100) wafer of 525 μm thickness with a phosphorus concentration of about $1 \cdot 10^{15}$ cm^{-3} was used as substrate. SiO_2 was grown thermally with a thickness of 100 nm as diffusion barrier for the following p^+ doping through oxide windows. The SiO_2 was structured with a first mask and wet chemical etching using a 5% buffered HF (BHF) solution. Source and drain doping was done by thermal diffusion from a 100 nm layer of boron doped microcrystalline silicon (B:μc-Si) at 1000 °C for 60 min. The B:μc-Si was deposited using plasma-enhanced chemical vapor deposition (PE-CVD) at a high frequency of 140 MHz. The source of boron was Trimethylborane (TMB), added to the silane process (see also chapter 5.1.1) [68]. After diffusion, a sacrificial thermal wet oxide (1000 °C, 40 min) with a thickness of about 275 μm was grown. This SiO_2 layer, including the diffusion mask, was then removed by BHF. The junction depth resulting from these two high temperature steps was 0.6 μm and a surface concentration of about $5 \cdot 10^{18}$cm^{-3} was achieved. The field oxide layer was subsequently deposited by a silane PE-CVD process to form 500 nm of SiO_2. It was structured by a second lithographic mask and BHF. Fig. 5.37a summarizes these steps.

Three different IFs were tested. The 1.6 nm thick native oxide, a chemically grown oxide of 2 nm thickness (piranha treatment for 10 min, H_2SO_4:$H_2O_2 \approx$ 3:1, starting at 110 °C, then cooling down) or 4 nm SiO_2 grown by dry thermal oxidation. The IF layer is depicted in Fig. 5.37b.

Devices with and without internal gate were fabricated. As internal gate, TiN was grown by PE-ALD (plasma enhanced ALD, capacitively coupled) with a thickness of 2 nm. $TiCl_4$ and $N_2/H_2/Ar$ were used as precursors at 250 °C. Fig. 5.37(int1) shows the deposited internal gate, Fig. 5.37(int2) its structuring.

The ferroelectric layer in the gate stack was Hafnium-Zirconium-Oxide (HZO), grown by thermal ALD. TEMAHf (tetrakis(ethylMethylamido)hafnium(IV)) and TEMAZr (tetrakis(ethylmethylamido)zirconium(IV)) were used with water as co-reactant at 250 °C. Using super-cycles of – TEMAHf, Ar purge, H_2O, Ar purge, TEMAZr, Ar purge, H_2O, Ar purge – lead to $Hf_{0.5}Zr_{0.5}O_2$. This composition is known to have a high remanent polarization (P_r) [59].

A third mask was used to structure contact holes. The HZO was etched by reactive ion etching (RIE) using NF_3 and Ar. Fig. 5.37c summarizes the gate dielectric deposition and etching steps.

As metallization layer, 20 nm thick TiN was used and deposited with the same process as the internal gate (PE-ALD). An RTP (rapid thermal processing) anneal followed for the HZO to form a FE phase [59]. A temperature of 600 °C / 650 °C for 20 s or 1000 °C for 1 s was applied. The TiN was then structured by a fourth lithographic mask and was again etched by RIE using NF_3 and Ar. As shown in Fig. 5.37d, TiN was used as the gate metal and as the source and drain contact material.

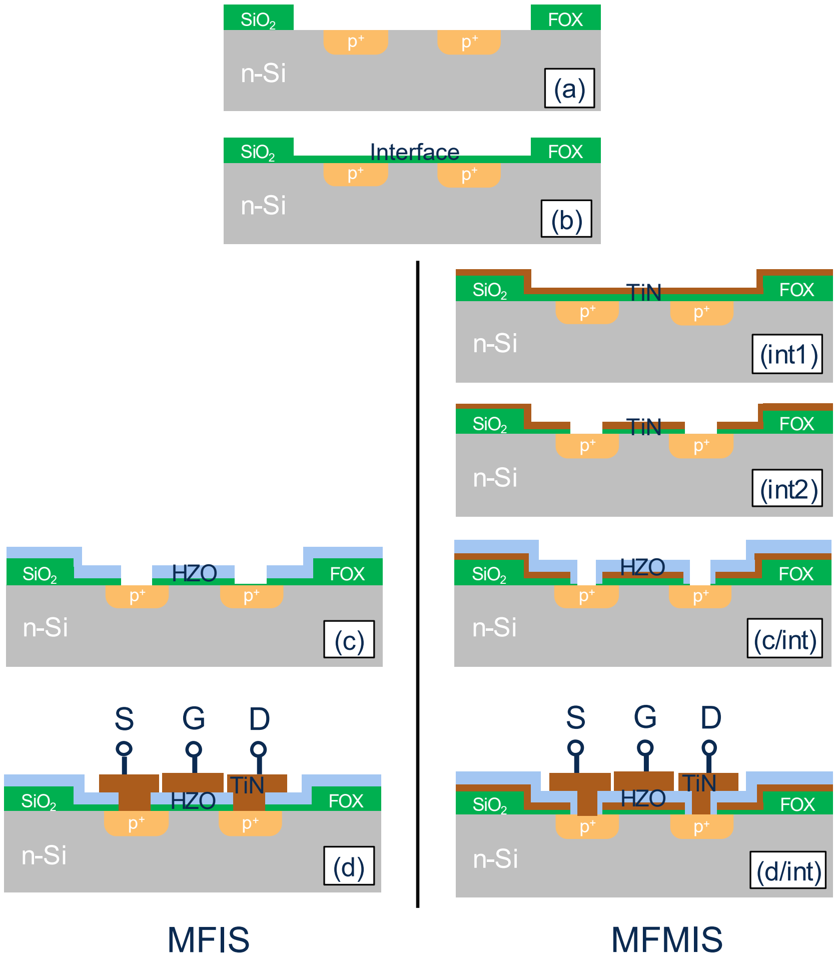


Fig. 5.37: Integration flow of the device without and with internal gate

The mask set from chapter 4.2.2 was used to fabricate these p-FeFETs. The transistors had gate lengths ranging from 10 ... 150 μm. A width to length ratio of 3 was kept constant in the design. Fig. 5.38 shows the transistor structure on the samples.

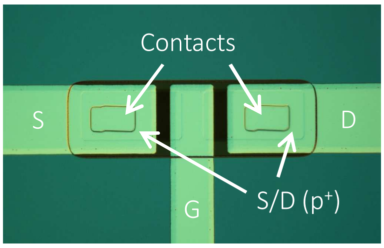


Fig. 5.38: The design of the transistors (top view microscope photograph)

Material Properties and Device Characteristics

As shown in Fig. 5.39 ... 5.41, the FE properties of the devices were investigated. The devices exhibited very clean, leakage-free polarization-voltage (P-V) curves showing a slight voltage bias. The biasing can be explained with the asymmetry of the TiN work function and Si substrate. Well saturated P-V characteristics with a P_r of $17.5\,\mu\text{C/cm}^2$ and wake-up-free [156] field cycling was observed. The P_r endurance is shown in Fig. 5.40. Beside the MFIS transistors, processed MFMIS capacitor test-structures exhibited similar P_r values and well saturated characteristics (Fig. 5.41).

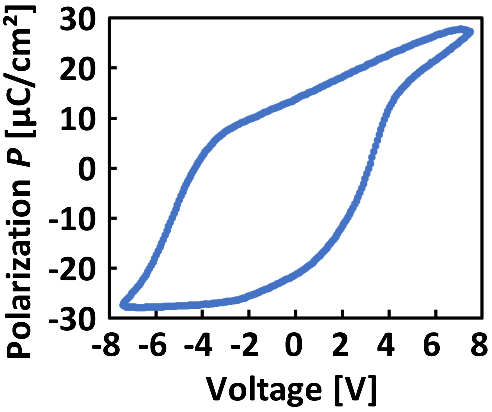
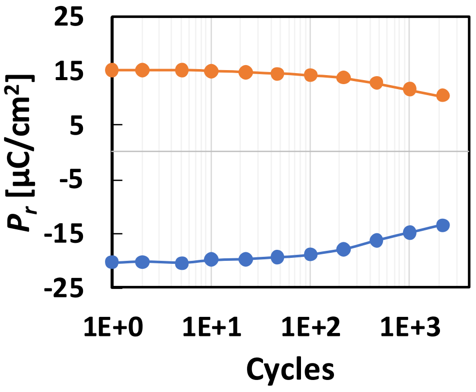


Fig. 5.39: Saturated P-V curve



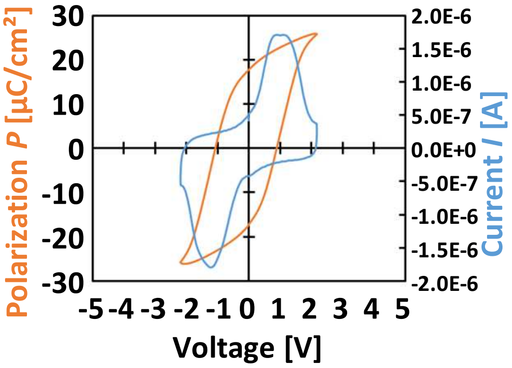


Fig. 5.40: P_r-endurance of the p-FeFET

Fig. 5.41: P-V characteristics of the MFMIS structure

Large test structures resulted in very good transistor behavior, as it can be seen in Fig. 5.42. Different from what is depicted here, most of the transistors showed a schottky-like behavior. This can be attributed to a relatively high contact resistivity of about $2 \cdot 10^{-2}\ \Omega\text{cm}^2$ between the TiN metal and p-doped Si. The value was obtained from a TLM (transmission line method) test structure, described in chapter 3.1.2. This is four to five orders higher than for very good contacts found in the literature [128], [129]. A fifth mask – to separate the gate metal from the S/D contact metallization – should be introduced to eliminate this problem. However, very low gate leakage could be measured (Fig. 5.45). The process conditions can be found in Tab. 5.6. As expected, an increase of the IF thickness (required for internal gate isolation) resulted in leakage reduction whereas the increase of the annealing temperature yielded in higher leakage. I_D-V_G measurements unveiled a memory window (MW) >2 V (a record of >80 % of the theoretical MW) with a slight shift due to charge trapping (Fig. 5.43). The subthreshold slope is different for the PRG and ERS state. It is very probable, that the high gate overlap with source and drain (no self-aligned processes used) leads to this. Between gate and the highly doped p^+ source / drain regions, the potential curve looks different than between the gate and the n-doped channel region. Fig. 5.44 shows the hysteresis of a C-V sweep on the gate between -6 ... 6 V at a frequency of 100 kHz with 0.1 V voltage level. The measurement confirms the broad memory window of >2 V.

Process	A	B	C	D	E	F
d_{IF} [nm]	1.6	2	4	4	4	4
d_{HZO} [nm]	15	15	16	16	24	24
Anneal	600 °C 20 s	600 °C 20 s	1000 °C 1 s	650 °C 20 s	1000 °C 1 s	650 °C 20 s

Tab. 5.6: Process conditions A-E with interface layer thickness d_{IF}, HZO thickness d_{HZO} and annealing conditions *Anneal*

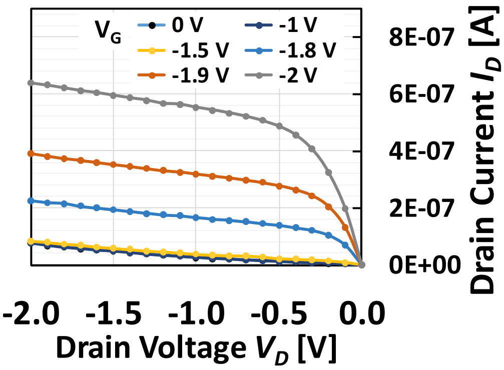


Fig. 5.42: I_D-V_D characteristics of the static readout of the cell after PRG

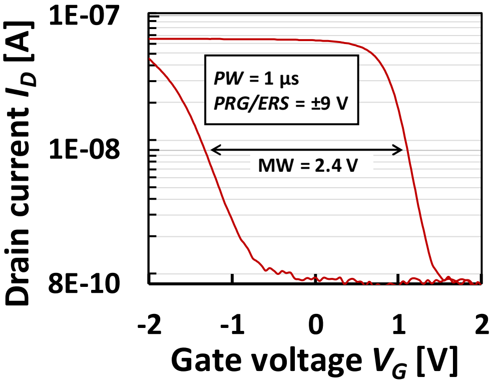


Fig. 5.43: I_D-V_G shift due to programing and erasing and the corresponding $MW = 2.4\,\mathrm{V}$

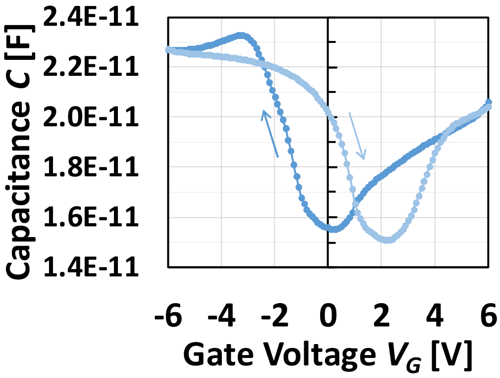


Fig. 5.44: C-V sweep with the $MW = 2.4\,\mathrm{V}$

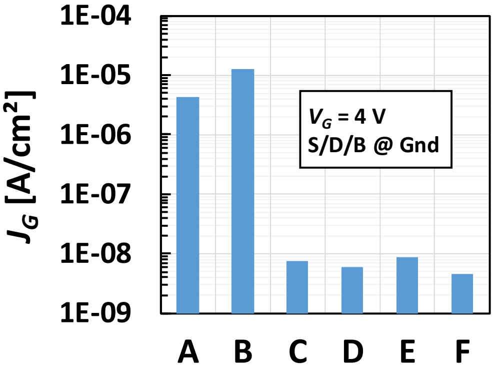


Fig. 5.45: Gate current density J_G measured at $V_G = 4\,\mathrm{V}$ for processes A - E

Memory Properties

The memory properties of these p-FeFETs have also been investigated. Only devices processed with lower thermal budged and an IF thickness below 4 nm showed a ferroelectric memory window. The others resulted in a negative MW due to trapping and depolarization originating from the thick interface layer (Fig. 5.46) [152]. The endurance of the memory window is shown in Fig. 5.47 for a native oxide interface layer. As it can be seen in Fig. 5.48, the MW and retention of the devices with native oxide is significantly higher compared to the devices having a chemically grown interface oxide. The same can be seen when comparing the P_r evolution during cycling, where the thicker interface layer (chemically grown) shows stronger relaxation (Fig. 5.49).

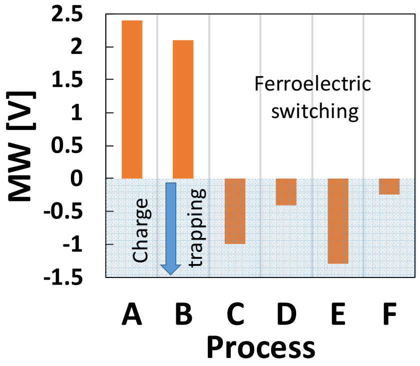


Fig. 5.46: MW as function of the process condition

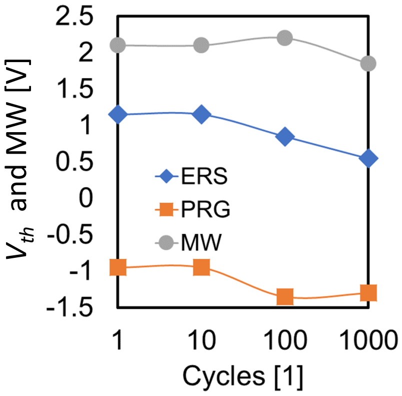


Fig. 5.47: Threshold voltage V_{th} and MW endurance of the p-FeFET

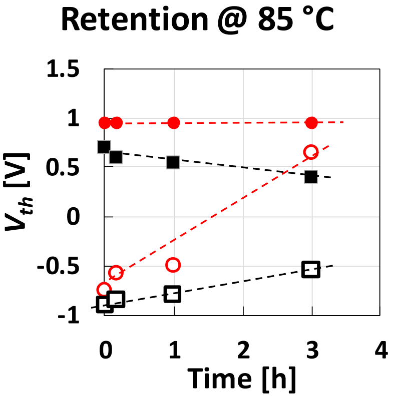


Fig. 5.48: p-FeFET memory window retention at 85 °C with native oxide (black) and chemically grown IF (red)

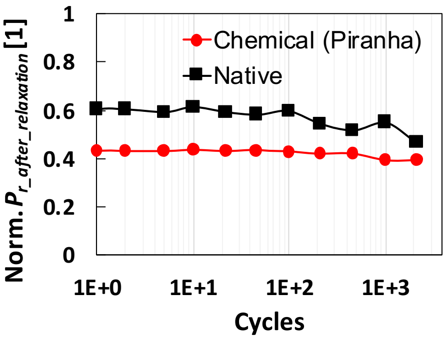


Fig. 5.49: P_r-evolution with cycling for transistor test structures

The majority of the devices with internal gate showed strong leakage. There was a general problem with the internal gate isolation against source and drain – the IF layer was too thin and shows high leakage, ultimately bridging the channel. Thus, these transistors could not be evaluated with statistical significance and had to be deliberately omitted. A simulation study was carried out instead. Modeling was done using the commercially available multi-scale simulation tool Ginestra$^{\mathrm{TM}}$ [135], already proven in assessing FE devices [136], [157].

Simulated Gate Stack Engineering

As aforementioned, the IF and FE-HZO are forming a voltage divider. Area factor (area of internal vs. area of control gate) tuning [158] via an internal gate can be deployed to modify the voltage distribution across the voltage divider (same effect as changing the k-value of the SiO_2 IF), thus reducing the field loss and stress over the critical interfacial layer. Fig. 5.50 shows possible gate stacks, originating from different manufacturing approaches.

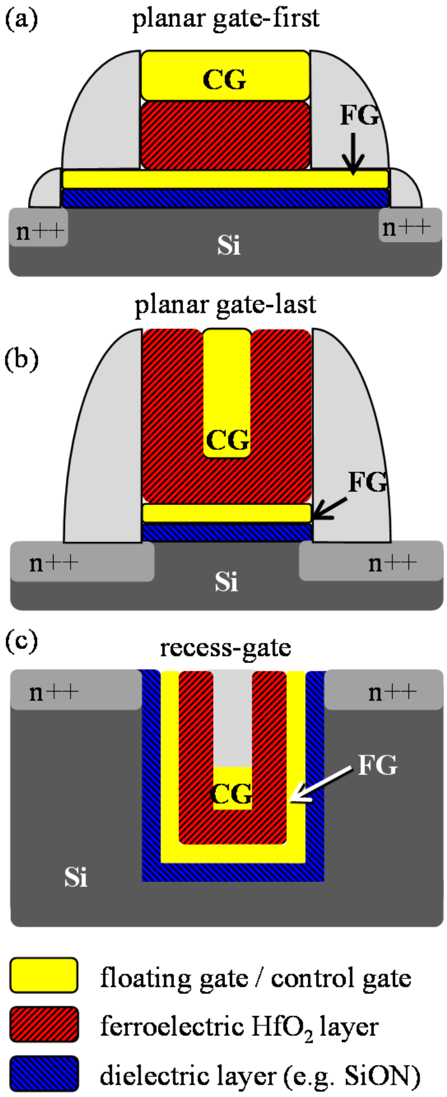


Fig. 5.50: Area factor tuning: (a) lithographically sized – gate first, (b) intrinsic size reduction of the gate plug in replacement gate – gate last or (c) gate contact sized in a recess gate; FG is the internal floating gate, CG is the control gate; taken from [158]

The impact of area factor tuning on the MW – when polarization is fully saturated – is negligible for the case of an 1.6 nm thick IF below the internal floating gate (Fig. 5.51). However, to saturate P_r, voltages above 8 V are required, which would result in instantaneous breakdown of the IF of the device. Therefore, a realistic operation voltage of 5.6 V was used for modeling. The possible decrease of the operation voltage was estimated as well as the electric field over the IF (Fig. 5.52) depending on the area factor while preserving the MW. An area ratio of 5, which could be realized in a recessed gate integration scheme, reduces the programming voltage by more than 40 % to 3.2 V and below (Fig. 5.52). This approach is very promising for reducing the degradation of the IF and achieving low power devices with enhanced endurance.

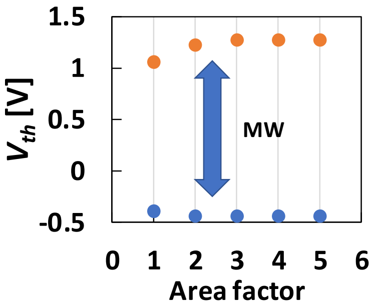


Fig. 5.51: Simulated MW of the FeFET depending on the area factor. An IF layer of 1.6 nm below the floating electrode was assumed

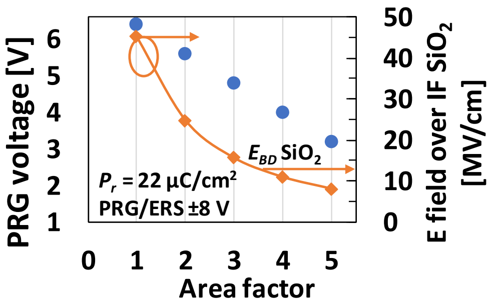


Fig. 5.52: PRG voltage and electric field over the SiO_2 interface layer as a function of the the area factor

Summary

The influence of different low-k interface layer thicknesses on the endurance and storage behavior of p-FeFET have been investigated. The first p-FeFET with an excellent MW of more than 2 V, low leakage and a very high $I_{D,on}/I_{D,off}$ ratio could be shown. An integration scheme with floating gate and the tuning of the area factor of the FeFET was proposed to reduce the degradation of the low-k IF. The proposed gate stack engineering of the voltage divider enables lower programming voltages and a reduction of the field over the interface layer by a factor of 3. An increase in the cycling endurance is therefore expected.

The knowledge gained from these planar structures was used in chapter 5.2.2 to integrate HZO in the p-TSVFETs introduced in chpater 5.1.2.

5.2.2 p-TSVFETs with Hafnium-Zirconium-Oxide Metal Gate

The integration of HZO in the TSVFET structure described in chapters 4.2.1 and 5.1.2 should take the functionalization of through silicon VIAs one step further and make the realization as a memory device possible. The connection of stacked chips would not only be switchable, the on/off state (connected or disconnected) would also be stored when the voltage supply is turned off.

The fabrication of the p-TSVFET as a ferroelectric transistor (p-TSVFeFET) followed the description in Fig. 5.12. Silicon substrates of 300 μm thickness with a phosphorous doping concentration of $1 \cdot 10^{15}$ cm^{-3} were used – the same as for the p-TSVFETs. Compared to the p-TSVFETs, the gate stack of the p-TSVFeFETs comprises of a thin low-k interface layer (1.6 nm native oxide, 2 nm chemically grown "piranha" oxide or 4 nm thermally grown SiO_2) and 15 nm of hafnium-zirconium-oxide (HZO), grown by thermal ALD (compare to chapter 5.2.1 and [154]), instead of SiO_2 and Al_2O_3. Here, "ZyALD" from Air Liquide was used as the zirconium precursor and TEMAHf was again used as the hafnium supply – the deposition was carried out at 300 °C with ozone (O_3) as oxygen source. The contact holes were etched by RIE with Ar and NF_3. Given the depth of the junction of 0.6 μm, an expected overetch of 10 ... 20 nm does not represent an issue, hence an electrical short to the substrate is highly unlikely. After the deposition of the metal gate (thermal ALD of Ru) and structured (O_2 plasma etching), the HZO was annealed at 600 °C for 20 s to form its ferroelectric phase. Fig. 5.53 shows the completed structure of the p-TSVFeFET.

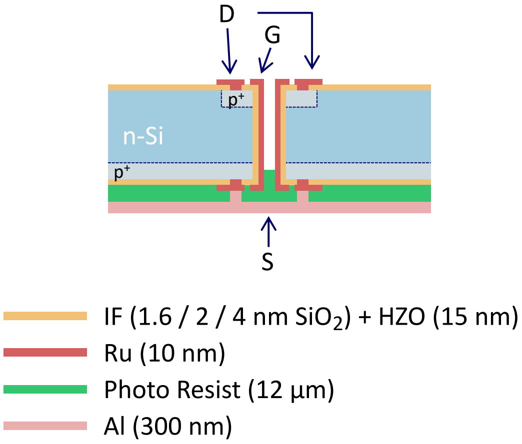


Fig. 5.53: Structure of the p-TSVFeFET

One significant difference to the planar p-FeFETs discussed in chapter 5.2 is the material of the gate metal – Ru was used instead of TiN (widely investigated with ferroelectrics). Namely, the columnar nature of the TiN grains and the layer stress is required for the stabilization of the ferroelectric phase and the growth of columnar grains within the HZO during the RTP anneal. Therefore, a reduced P_r is expected, as it has already been shown for RuOx [159].

HZO Material Properties

The basic material properties of the Hafnium-Zirconium-Oxide were investigated on MFM capacities with TiN electrodes. Wake-up free and well saturated P-E curves could be measured, as shown in Fig. 5.54. An HZO layer of 15 nm thickness was annealed 600 °C for 20 s – analog to the transistor fabrication. The A stable remanent polarization of about 17 μC/cm^2 could be observed for up to 10000 field cycles. More cycling lead to stress-induced leakage enhancement of the ferroelectric, which is superimposed with polarization [160]. The polarization curves lose their saturating shape and P_r rises in positive and negative direction (Fig. 5.55). Pulsed PUND measurements (Positive-Up Negative-Down) would help to decouple the dielectric (displacement and leakage current) and ferroelectric (polarization) contributions [161].

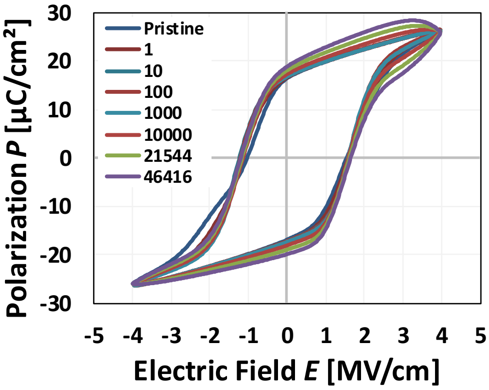


Fig. 5.54: Saturated P-E curve for the MFM capacitor with TiN electrodes

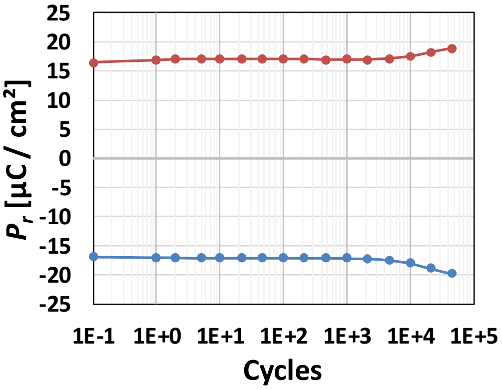


Fig. 5.55: P_r-endurance for the HZO in the MFM capacitor with TiN electrodes

p-TSVFeFET Device Characteristics

Similar to the investigations of planar p-FeFETs (see chapter 5.2.1 for details), the process conditions were chosen for the TSVFET devices and are summarized in Tab. 5.7. The transistors with the thermally grown SiO_2 interface (thickness 4 nm) show good switching behavior with an $I_{D,on}/I_{D,off}$ ratio of 10^3, as it can be seen in Fig. 5.56.

The contact is schottky-like, which can be explained with the high contact resistivity of Ru on the p$^{(+)}$-doped source and drain regions for this case – $\rho_c = 7 \cdot 10^{-3}\ \Omega\text{cm}^2$. In contrast to the p-TSVFETs in chapter 5.1.2, the contact resistance was higher due to slight process variations in the PE-CVD B:μc-Si film used as dopant supply. As expected, transistors processed under the conditions "III" ($d_{IF} = 4\,\text{nm}$) experience charge trapping. The transfer curve is shifted towards higher voltages for (positive) programming voltages – electron trapping leads to higher V_{th} for p-FETs. Furthermore, the thick interface layer causes a high depolarization field ($V_{depolarize} = \frac{Q}{C_{IF}} = \frac{Q \cdot d_{IF}}{\varepsilon \cdot A}$, thick IF), which destabilizes the ferroelectric dipoles and reduces the ferroelectric MW. As indicated in Fig. 5.57, a memory window of up to 0.8 V could be achieved. This was confirmed by C-V measurements between ±5 ... ±7 V at a frequency of 100 kHz with 0.1 V voltage level on the wafer surface (MFIS capacitor of Ru/HZO+IF/n-Si, see Fig. 5.58) and on the gate of a transistor with 300 μm gate length and a TSV diameter of 40 μm (Fig. 5.59).

Process	I	II	III
d_{IF} [nm]	1.6	2	4
d_{HZO} [nm]	15	15	15
Anneal	600 °C, 20 s	600 °C, 20 s	600 °C, 20 s

Tab. 5.7: Process conditions I-III with interface layer thickness d_{IF}, HZO thickness d_{HZO} and annealing conditions *Anneal*

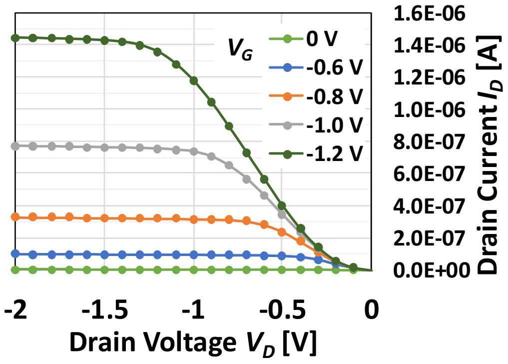


Fig. 5.56: I_D-V_D curves of the static readout of the p-TSVFET (process conditions III) with 300 μm gate length and a TSV diameter of 40 μm after PRG of $V_G = +4\,\text{V}$

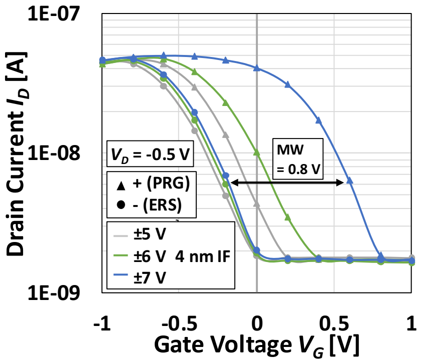


Fig. 5.57: I_D-V_G shift due to programming and erasing (process conditions III), 300 μm gate length and a TSV diameter of 40 μm

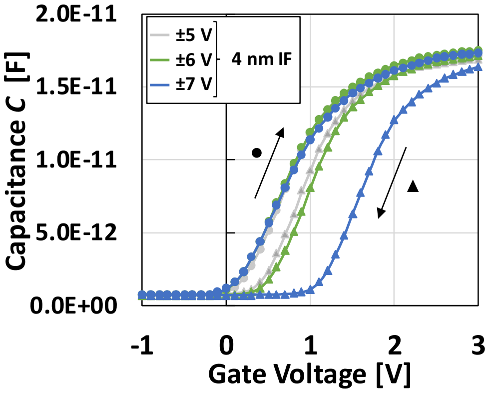


Fig. 5.58: *C*-*V* sweeps on MFIS capacitors on the wafer surface (process conditions III)

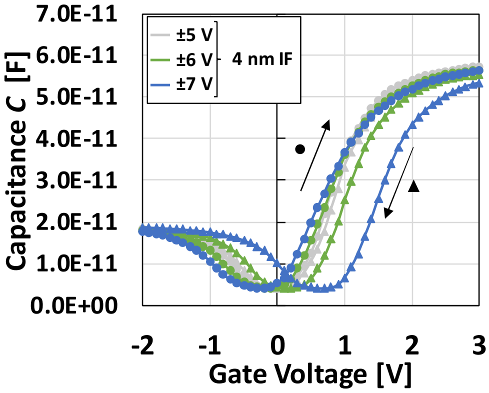


Fig. 5.59: *C*-*V* sweeps on the transistor gate with 300 μm gate length and a TSV diameter of 40 μm (process conditions III)

The observations from chapter 5.2.1 – ferroelectric switching can be seen for the thinner interface layers only – were confirmed on these TSVFET samples. MFIS capacitors on the polished wafer surface show exactly this behavior for 1.6 nm (native oxide) and 2 nm (chemically grown SiO_2 by piranha treatment) interface layers. The *C*-*V* sweeps (100 kHz, 0.1 V voltage level) depicted in Fig. 5.60 unveil a counter-clockwise hysteresis, indicating a V_{FB} shift due to ferroelectric polarization switching. The memory window was 2 V for sweeps between -6 ... 6 V for the stack with a native oxide interface layer. Switching could also be observed on the gate of the transistors, but charge trapping was superimposing and dominating the ferro effect (Fig. 5.61). As indicated, there is a capacitance boost (overshoot) between 1.5 V ... 2.5 V, which should be accounted to ferroelectric switching, since the change in polarization raises the current. The transistor channel (TSV hole surface) is very rough and offers a high number of defect sites promoting charge trapping.

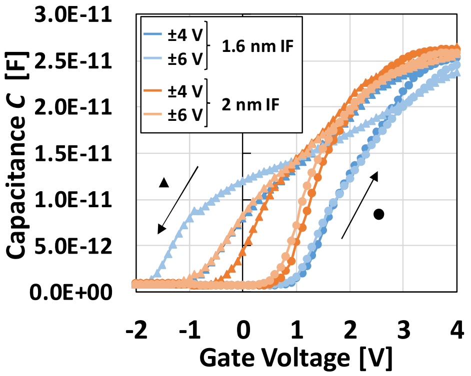


Fig. 5.60: *C*-*V* sweeps on MFIS capacitors on the wafer surface (process conditions I and II)

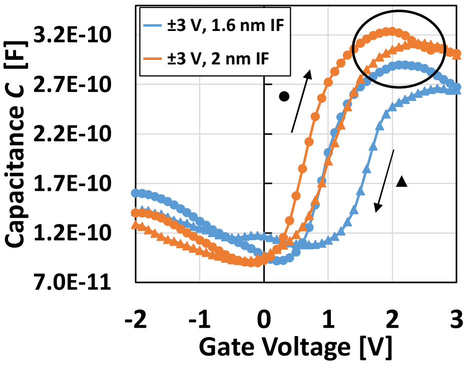


Fig. 5.61: *C*-*V* sweeps on the transistor gate with 300 μm gate length and a TSV diameter of 40 μm (process conditions I and II)

The memory window (MW) as a function of the process condition is summarized in Fig. 5.62. As shown in Fig. 5.63, this leads to very high gate leakage – numerous electrons can easily flood the layer interfaces and HZO, ultimately remaining there. The interface state densities (calculated from C-V measurements) are shown in Fig. 5.64 – they are in the same range as the n- and p-TSVFETs from chapter 5.1.2.

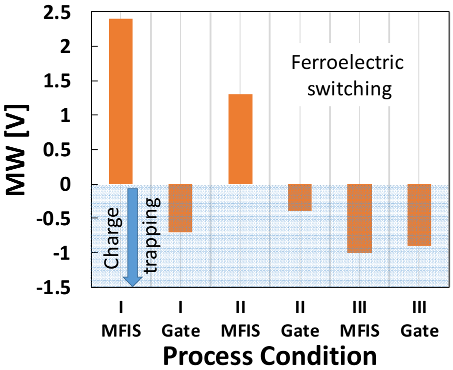
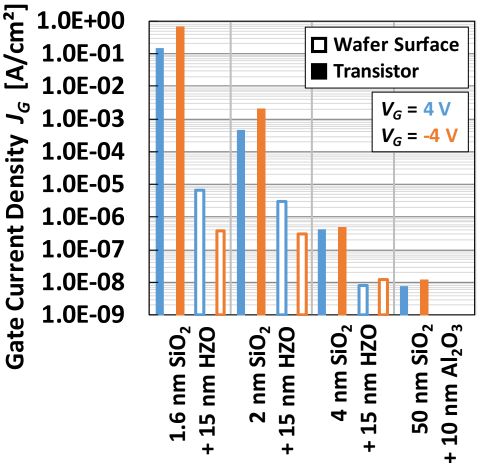


Fig. 5.62: Memory window as function of the process condition – from C-V measurements on the MFIS capacitor (polished wafer surface) and on the gate in the TSV hole



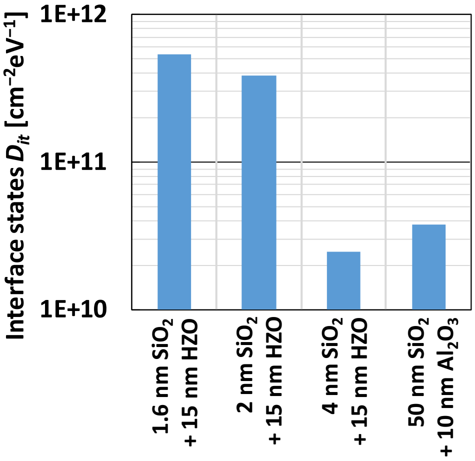


Fig. 5.63: Gate current density for MFIS capacitors on the polished wafer surface and for p-TSVFETs with different gate stacks, 300 μm gate length and a TSV diameter of 40 μm (p-TSVFET with 10 nm Al_2O_3 on 50 nm SiO_2 for comparison)

Fig. 5.64: Calculated interface state density for MFIS capacitors on the polished wafer surface and for p-TSVFETs with different gate stacks, 300 μm gate length and a TSV diameter of 40 μm (p-TSVFET with 10 nm Al_2O_3 on 50 nm SiO_2 for comparison)

Summary

In general, HZO was successfully integrated in the new TSV field-effect transistor. However, devices with the thinner low-k interface layers (1.6 nm and 2 nm) showed strong gate leakage and typical transistor curves could not be measured. Furthermore, this lead to the domination of charge trapping over ferroelectric switching, as found by C-V measurements. The most probable way to overcome these problems would be to first and foremost optimize the etching process for the through silicon VIAs, in order to get smoother sidewalls and therefore a transistor channel of higher quality. Moreover, the introduction of a TiN metal gate known for the promotion of the FE phase is recommended to obtain a better ferroelectric gate. TSVFeFETs with a thicker interface layer of 4 nm resulted in charge trapping devices with a memory window of about 1 V, as it has already been shown for planar p-FeFETs in chapter 5.2.1. These devices show low leakage and a good switching behavior. Even though the counter-clockwise hysteresis was not observed in the transfer characteristics of the device, such devices could be used as charge trapping memory. Still, the retention and endurance of such devices has to be investigated.

5.3 Doping by Ion Implantation of Gallium with a Focused Ion Beam (FIB) Tool

Gallium is a p-dopant (trivalent metal) in silicon and can therefore be used to modulate its electrical properties. Gallium is used as a dopant for long-wavelength infrared silicon detectors in the atmospheric window for wavelengths between 8 ... 14 μm [162]. For photovoltaic applications, Ga doping is gaining importance as replacement for boron-doped substrates, due to its long minority carrier lifetime with no degradation [163], [164].
Implantations of gallium into silicon have been studied before. The need of relatively low annealing temperatures of 400 ... 600 °C were demonstrated for Ga implantations with an acceleration energy of $E = 275\,\text{keV}$ and a maximum solubility of Ga in Si at 570 °C was found to be $4 \cdot 10^{19}$ cm^{-3} [165]. Focused ion beam (FIB) implantations of Ga into Si have also been investigated ($E = 50\,\text{keV}$) with anneals between 550 ... 700 °C. The critical dose for continuous amorphous layer formation was found at 8 ... $10 \cdot 10^{13}$ ions/cm^2 for low beam speeds. Shallow implants with a junction depth of about <100 nm and a maximum carrier concentration of $\approx 10^{20}$ cm^{-3} could be obtained by SIMS measurements after annealing at 700 °C [166].
The diffusion of Ga in Si has also been investigated. The diffusivity and maximum solubilities for higher temperatures (800 ... 1100 °C) are discussed in [167]. Resistivity over doping concentration plots can also be found – for large parts, the dependence is nearly the same as for boron doping [168].

In summary, the basic characterization of Ga as a dopand of Si can be found in literature. In this work, FIB (focused ion beam) implantations of Ga are used to fabricate active devices for the first time. High doping concentrations should be achievable, thus the fabrication of S/D regions for p-FETs or the manufacturing of Ga doped Si diodes should be possible. Due to the low projected range of Ga ions in Si (see also Tab. 5.8), implants with very small dimensions can be created. In general, direct maskless writing of individually designed doped structures is made possible by the use of the ion beam.

First, diodes were fabricated and electrically characterized in chapter 5.3.1. The implantation dose was varied as well as the annealing temperature. The gained knowledge was used in chapter 5.3.2 for the fabrication of field-effect transistors (p-FETs) with S/D regions, doped by implated Ga. In chapter 5.3.3 an integration flow for TSV transistors with Ga doped S/D regions is proposed, co-integrated with Cu-filled TSVs.

5.3.1 Ga doped Si Diodes

Ga ions were implanted into Si (n-doped, phosphorous, $1 \cdot 10^{15}$ cm^{-3}) by the use of a focused ion beam tool EXPEDIA 1985 from FEI. The ion current density was set to very low values, in order to reduce sputtering and structuring of the bombarded Si as much as possible.

The implantations were simulated with SRIM (THE STOPPING AND RANGE OF IONS IN MATTER) [169]. The FIB supported acceleration voltages between 3 ... 30 kV. Implantations for an energy of 10 and 30 keV were simulated and the following characteristic values were found (Tab. 5.8):

Ion Energy	R_p (Projected Range)	ΔR_p (Longitudinal Straggling)	Lateral Straggling
10 keV	12.5 nm	4.8 nm	3.6 nm
30 keV	29.6 nm	9.3 nm	7.2 nm

Tab. 5.8: Projected range and straggling of Ga implanted into Si

Since the projected range is very low, the tool was operated at its maximum acceleration voltage of 30 kV for the following experimental investigations. SIMS measurements of such implantations can be found in [170] – the depth profile of the relative atomic concentration of Ga in Si is shown in Fig. 5.65.

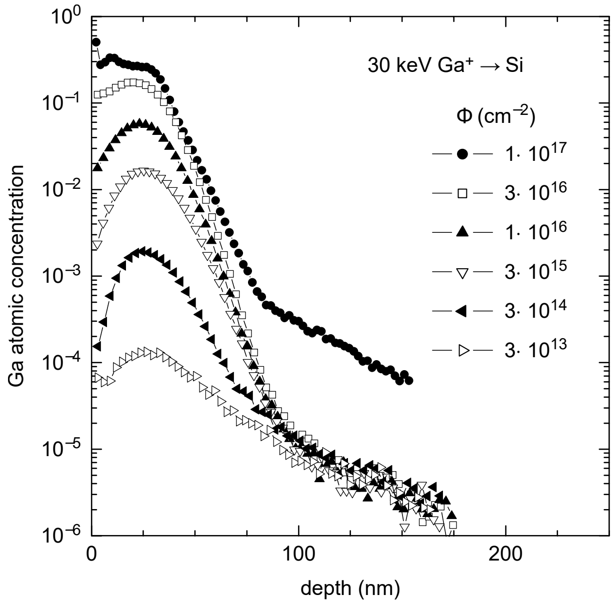


Fig. 5.65: Depth distributions for 30 keV Ga implantations in Si (SIMS), from [170]

An amorphization of the lattice structure always takes place during the implantation. Only substitutional impurities are "active" as dopants (providing free holes) and high activation enthalpies are usually required, in order to anneal defects by vacancy-mediated self-diffusion of Si (about 5 eV) [171]. It can be easier (using lower temperatures) to regrow the crystal from the amorphous layer via solid phase epitaxy (activation energy about 2.7 eV in Si, [172]) which was done in this work. As it can be seen from Tab. 5.11, the amorphization dose of single-crystal Si ($1 \cdot 10^{13}$ Ions/cm^2) was by far exceeded [166]. From the two annealing possibilities (**A** – implant above the critical dose and anneal at low temperature to regrow the material or **B** – implant below the critical dose and anneal at high temperature to remove the defects), **A** had been choosen here.

Diffusion of Gallium in Si and SiO$_2$

For Ga diffusion in Si an activation energy of $E_A = 3.31\,\text{eV}$ and pre-exponential factor of $D_0 = 8.21 \cdot 10^{-5}$ m^2/s could be extracted from the Arrhenius plot of the diffusion coefficient $D_{Ga,Si}$ over the reverse temperature $1000/T$ from [173]. This allows the calculation of the diffusion coefficient D and the diffusion length L_D for lower temperatures as they have been used in this work with the following equations Eq. 5.3.1 and Eq. 5.3.2. The same applies for Ga diffusion in SiO$_2$. From [174] an activation energy of $E_A = 4.17\,\text{eV}$ and $D_0 = 1.04 \cdot 10^{+1}$ m^2/s could be calculated. The diffusivity D_{Ga,SiO_2} was given for 1100 °C and 1250 °C in the publication and was used for the calculations.

$$D = D_0 \cdot e^{\left(-\frac{E_A}{k_B T}\right)} \tag{5.3.1}$$

$$L_D = \sqrt{2 \cdot D \cdot t} \tag{5.3.2}$$

Where k_B is Boltzmann's constant and t is the diffusion time.

The calculated values can be found in Tab. 5.9. The diffusion length of Ga in Si for low temperatures (between 400 ... 700 °C) and a short time of 15 min is negligibly low and does not exceed one nanometer. A similar picture can be drawn in SiO$_2$, where the diffusion length is just above two nanometers. Higher temperatures were not used for the activation of the dopants.

T [°C]	t [min]	$D_{Ga,Si}$ [m^2/s]	$L_{D,Ga,Si}$ [m]	D_{Ga,SiO_2} [m^2/s]	L_{D,Ga,SiO_2} [m]
400	15	1.44e-29	1.61e-13	6.61e-31	3.45e-14
450	15	7.40e-28	1.15e-12	9.49e-29	4.13e-13
500	15	2.29e-26	6.42e-12	7.17e-27	3.59e-12
550	15	4.67e-25	2.90e-11	3.20e-25	2.40e-11
600	15	6.74e-24	1.10e-10	9.25e-24	1.29e-10
650	15	7.28e-23	3.62e-10	1.86e-22	5.78e-10
700	15	6.16e-22	1.05e-9	2.74e-21	2.22e-9

Tab. 5.9: Diffusion coefficients D and diffuion lenghths L_D of Gallium in Si and SiO$_2$

Fabrication of Ga Doped Si Diodes

For the fabrication of diodes with the aforementioned FIB, different implantation doses were compared at different annealing temperatures. Seven samples were prepared and annealed between 400 ... 700 °C. A conventional furnace was used for that, the maximum temperature T_{max} was applied for 15 min. The process parameters are summarized in Tab. 5.10.

Sample	1	2	3	4	5	6	7
T_{max} [°C]	400	450	500	550	600	650	700
t [min]	15	15	15	15	15	15	15

Tab. 5.10: Annealing conditions for each diode sample

Each sample held seven diodes, the implantation parameters are shown in Tab. 5.11. An area of 410 x 340 μm^2 was scanned by the ion beam. Si was partially removed and also redeposited in the vicinity by sputtering effects.

Diode	A	B	C	D	E	F	G
I_{Ion} [pA]	8250	8250	8250	5900	5900	5900	900
t [min]	33	16	8	16	32	48	90
Φ [Ions/cm^2]	7.31e16	3.55e16	1.77e16	2.54e16	5.06e16	7.61e16	2.18e16

Tab. 5.11: Implantation parameters with ion current I_{Ion} and calculated dose Φ

The following process sequence was used for the fabrication of these diodes. A schematic is shown in Fig. 5.66.

a) Resist mask on n-Si wafer (phosphorous doped) with 800 x 800 μm^2 squares as open areas for orientation
b) Implantation of Gallium (square shapes, 410 x 340 μm^2) with the FIB
c) Resist removal and cleaning with acetone / isopropanol / DI water
d) Deposition of 300 nm SiO_2 (magnetron sputtering) to prevent contamination from furnace quartz tube
e) Annealing and activation in the furnace (15 min, 400 ... 700 °C)
f) Removal of the covering oxide by wet etching with BHF
    ⇒ 4-point-probes measurements
g) Ti (20 nm) and Al (300 nm) e-beam evaporation
h) Litho mask for Al/Ti dots (130 x 130 μm^2)
i) Etching with etchant containing H_2PO_4 (Al etcher) and HF (0.5 %) (Ti etcher)
j) SF_6 RIE etching of 500 nm Si with the metal dots as hard mask (remove residuals / "clean" the area between the contacts)
k) Al e-beam evaporation as back side metallization (500 nm)
l) Forming gas anneal (5 % H_2 in N_2, 400 °C, 30 min)
    ⇒ IV and CV measurements

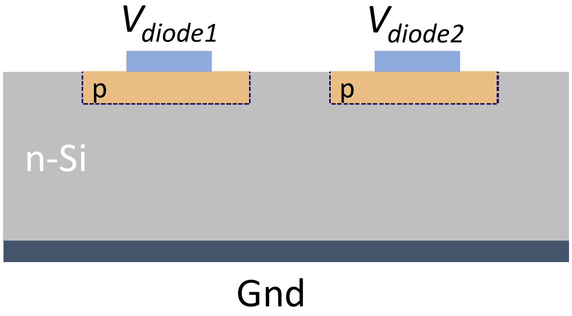


Fig. 5.66: Ga doped Si Diodes fabricated by the use of a FIB, light-blue is Ti/Al and dark blue is Al

4pp Resistance Measurements

A four point probe head was used to contact the doped Si directly in order to measure the resistance for all implanted areas on all samples. The distance of the measuring head from the edge of the measuring field was not a multiple of the needle distance (see Fig. 5.69), which is a prerequisite for accurate 4pp measurements. Since this was valid for all measured samples, it was acceptable for these comparative measurements. Two KEITHLEY Source Measure Units (SMU K236 and K237) were used and the current was swept between -0.5 ... 0.5 mA. Fig. 5.67 exemplarily shows a typical *I*-*V* curve for each sample. For annealing temperatures between 400 ... 550 °C, the curves follow a linear trend, whereas very high driving voltages were needed for samples annealed at higher temperatures. The same trend can be seen when all the resistance values are compared to each other (Fig. 5.68).

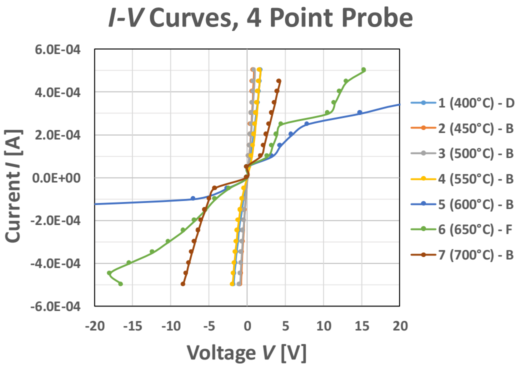


Fig. 5.67: *I*-*V* curves from the 4pp measurements of the doped regions after activation

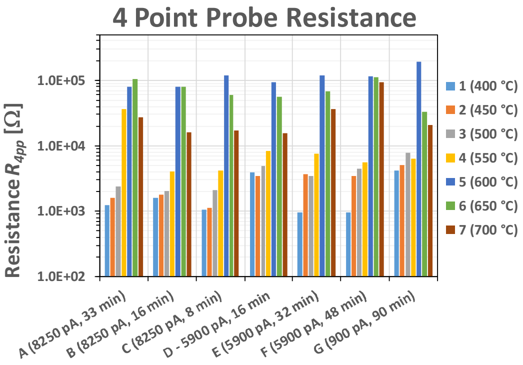


Fig. 5.68: Resistance R_{4pp} of the doped regions after activation

For annealing temperatures of 400 ... 550 °C and below, the resistance increases for increasing temperature. The values obtained were between $R_{4pp} = 1 \dots 8\,\mathrm{k\Omega}$. With equation 3.1.8, a sheet resistance between $R_{sh} = 4.5 \dots 36.3\,\mathrm{k\Omega}/\square$ and a resistivity in the range of $\rho = 0.02 \dots 0.13\,\Omega\mathrm{cm}$ were calculated (junction depth assumed to be $x_j \approx 35\,\mathrm{nm}$). The average doping concentration ranges between $N_A = 3 \cdot 10^{18} \dots 2 \cdot 10^{17}$ Ions/cm^3.

Above 550 °C, the measured resistance drastically rises by more than one order. Furthermore, scratches caused by the needles used to contact the Ga doped Si, were left on the surface of the samples. Fig. 5.69 shows an optical microscope image of this. Ga tends to form agglomerations at higher temperatures (due to its liquid state of matter between 29.8 ... 2400 °C [175]) as it can be seen in Fig. 5.70. These profiler measurements show agglomerations with a height of up to 300 nm.

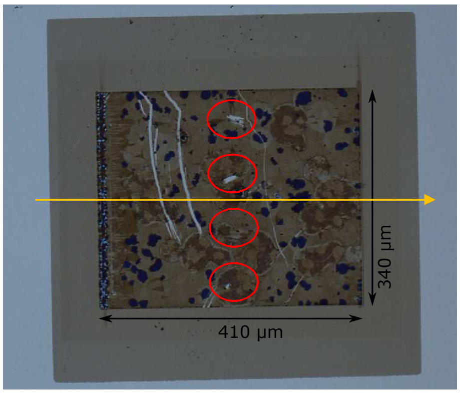


Fig. 5.69: $T_{anneal} = 650\,°C$, circled scratches from tips, arrow indicates profiler scan from Fig. 5.70

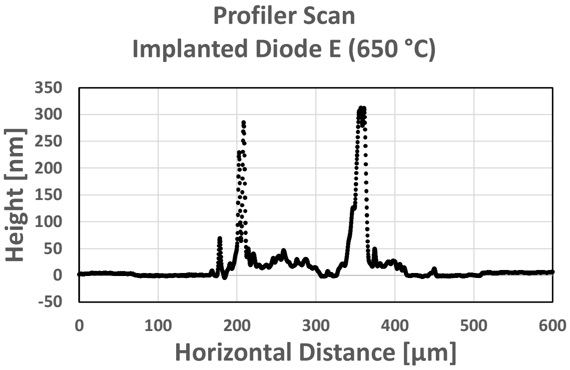


Fig. 5.70: DEKTAK Profiler Scan across the implanted area

Gallium is known to show fast diffusion in SiO_2 [173], [176]. A silicon dioxide layer was deposited on top of the implanted areas in order to prevent a contamination of the diodes, originating from the quartz tube of the furnace used for annealing and activation. Since the diffusion in SiO_2 is fast, an increased diffusion into the SiO_2 can be assumed for higher temperatures.

The oxide was deposited by an RF sputter process and it was therefore of lower density than thermally grown films. An indicator for that was a much higher etch rate in 5% BHF (600 nm/min for the PVD SiO_2 vs. 100 nm/min for thermally grown oxide). Higher diffusion coefficients for Ga are expected in these films compared to those mentioned in Tab. 5.9. A sputtered layer with many grain boundaries offers a surface with an irregular structure, leading to non-uniform diffusivity and explaining the spikes in the profiler measurements [177]. The temperature should not exceed 550 °C while covering it with this particular sputtered SiO_2 layer during the activation and anneal.

XPS measurements were performed of samples annealed at 400 °C and 650 °C, in order to check for pure Ga at the surface of the Si. The comparison did not show any difference in the Ga content. The Ga signal count was very low in general and close to the detection limit.

Diodes – I-V Measurements

Diode B (8250 pA, 16 min) was used to investigate the impact of the annealing temperature on the diode behaviour. For sample 1 (400 °C) diode D (5900 pA, 16 min) had to be chosen, due to bad adhesion of the top electrode (Ti/Al) on B. Most diodes on samples 6 and 7 (650 °C and 700 °C) did not show characteristic behavior. F (650 °C) and B (700 °C) were chosen because the data was fairly following typical diode curves. Tab. 5.12 summarizes this and shows some measurement results.

Sample	1 400 °C	2 450 °C	3 500 °C	4 550 °C	5 600 °C	6 650 °C	7 700 °C
Diode	D	B	B	B	B	F	B
J_{on} [A/cm^2] @ +1 V	1.6e+1	4.0e+0	5.7e−1	7.7e−1	7.8e−2	7.4e−3	4.0e−1
J_{off} [A/cm^2] @ -0.8 V	4.2e−6	5.3e−6	9.6e−6	2.7e−7	9.9e−8	2.6e−4	6.6e−4
I_{on}/I_{off}	3.8e+6	7.5e+5	5.9e+4	2.9e+6	7.9e+5	*2.7e+1*	*6.0e+2*
V_{th} [V]	0.68	0.59	0.53	0.68	0.61	*0.14*	*0.24*

Tab. 5.12: I_{on}/I_{off}-Ratio comparison and threshold voltage V_{th}

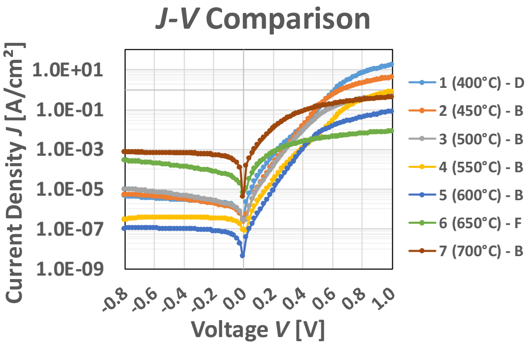


Fig. 5.71: J-V curves for differently annealed samples

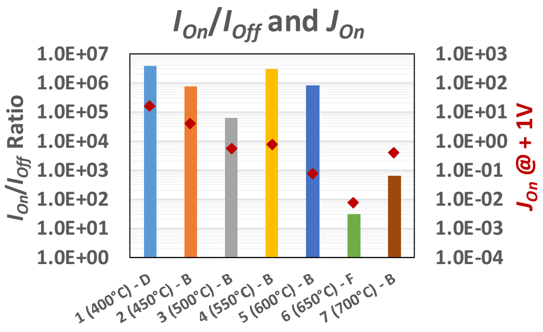


Fig. 5.72: I_{on}/I_{off} comparison for different T_{anneal}

The highest J_{on} could be measured for 400 °C, decreasing for higher annealing temperatures. Among other things, the doping concentration at the metal – semiconductor interface defines the contact resistance of these contacts (see chapter 3.1.2). Since Ga shows fast diffusion in SiO$_2$, a higher annealing temperature leads to a lower Ga concentration at the interface (Si – SiO$_2$), when the doped area is covered with SiO$_2$ during the activation anneal. A lower doping concentration at the metal – semiconduc-

tor interface would mean a higher contact resistance and therefore lower output current density J_{on} for the diode. The I_{on}/I_{off} ratios are reasonably high for diodes that were activated at temperatures of 600 °C and below ($5.9 \cdot 10^4$ ... $3.8 \cdot 10^6$). The highest values occur for 400 °C due to its high J_{on} and for 550 °C due to its low J_{off} value. This agrees with the 4pp resistance measurements of the Ga doped Si, which showed the lowest resistance for 400 °C, increasing with higher temperature. Lower contact resistances can be assumed for lower sheet resistance values (higher doping, higher amount of active dopants). The threshold voltage V_{th} is in the range of 0.55 ... 0.68 V for anneals up to 600 °C – close to the expected value of 0.7 V for Si diodes.
Higher annealing temperatures (650 °C and 700 °C) lead to diodes with very low threshold voltages (0.14 V and 0.24 V) and the curves differ from typical diode characteristics (low steepness and a very low I_{on}/I_{off} ratio).

Diodes – C-V Measurements

Capacitance-Voltage measurements were performed between -1.2 ... -0.1 V in 0.05 V steps at a frequency of 1 kHz with 0.1 V voltage level. $1/C^2$ was plotted over the applied voltage V and the built-in voltage V_{bi} or built-in potential ϕ_{bi} (see Fig. 5.74) could be extracted from the intersection with the voltage axis (see Fig. 5.73).

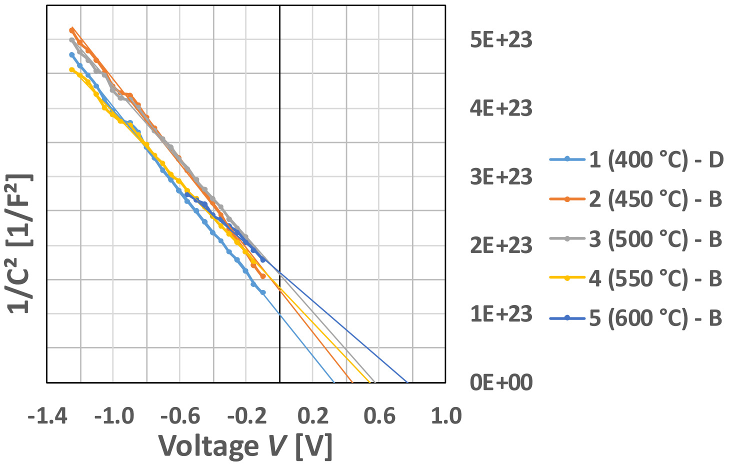


Fig. 5.73: $1/C^2$ calculated from C-V measurements, extrapolated to extract V_{bi}

The built-in voltage is present at the interface between two oppositely doped regions. It can be explained as the potential difference between the conduction band edges of p and n without any external voltage.

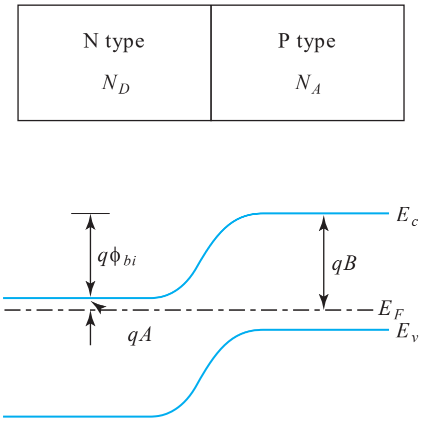


Fig. 5.74: Illustration of the built-in potential, from [178]

As it can be seen in Fig. 5.75, the built-in voltage was found to be between 0.33 ... 0.75 V and it increases for increasing anneling temperatures. For 650 °C and 700 °C, no reasonable C-V measurements could be performed.

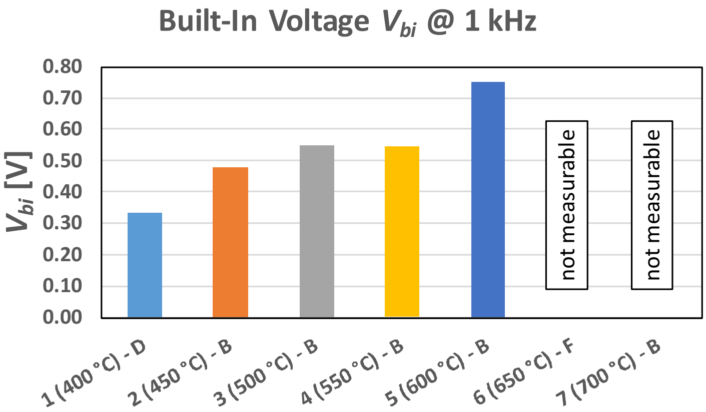


Fig. 5.75: Comparison of the built-in voltages

The effective doping concentration of the Ga doped p-regions can be calculated by:

$$V_{bi} = \frac{k_B T}{e} \cdot ln\left(\frac{N_A N_D}{{n_i}^2}\right) \tag{5.3.3}$$

k_B is Boltzmann's constant, T is the temperature of the diode, e is the elementary charge, N_A and N_D are the doping concentrations of the p and n doped regions and n_i the intrinsic carrier concentration of Si [179].

The doping concentrations in the Ga doped Si were calculated as $7.9 \cdot 10^{10}$ cm^{-3} for 400 °C (very low!) and up to $9.0 \cdot 10^{17}$ cm^{-3} for 600 °C – lower doping for the lower activation temperatures, higher doping for the anneals at higher temperatures.

This is in contrast to the other findings. The 4 point probes measurements showed the lowest resistance for $T_{anneal} = 400\,°\mathrm{C}$, indicating the highest doping concentration of the fabricated diode samples. This could be explained with the very high concentration ($\Phi \approx 10^{16}$ cm^{-2} can be considered as a very high implantation dose) and the metallic character of Ga located very close to the Si surface. It might act as an extension of the metallic contact on top of the Si, resulting in misleading doping concentration values. This assumption is supported by the characterization of the S/D diodes fabricated in chapter 5.3.2. These diodes experienced an even higher maximum annealing temperature of 700 °C for 60 min during the wet gate oxidation. Their I_{on}/I_{off} ratios of 10^7 ... 10^8 represent the highest values of any Ga doped diodes fabricated in this work (compare to: 10^6 for 400 °C measured here).

The resulting width of the depleted space charge region – caused by an external diode voltage V_{ext} – can be calculated by:

$$w_{scr} = \sqrt{\frac{2\varepsilon_0\varepsilon_{Si}\left(V_{bi} - V_{ext}\right)}{eN_D}} \tag{5.3.4}$$

Where ε_{Si} is the permittivity of Si [179].

The width of the space charge region ranges from 0.66 ... 0.99 μm ($V_{ext} = 0\,\mathrm{V}$), 1.32 ... 1.52 μm ($V_{ext} = -1\,\mathrm{V}$) and between 2.65 ... 2.75 μm for ($V_{ext} = -5\,\mathrm{V}$), respectively. These values are particularly interesting when Ga doped regions are used for the fabrication of field-effect transistors as described in chapter 5.3.2. When the width of the space charge region reaches a value close to the channel length, correct transistor behavior (switching) cannot be expected anymore.

It should be noted that the quantification of V_{bi} (and therefore N_A and w_{scr}) by the use of the $1/C^2$ method is strongly dependent on the C-V frequency. Keeping the measurement conditions constant revealed clear trends (e.g. higher V_{bi} for higher T_{anneal}) but the total values should be handled with caution. Nevertheless, it is a measurement that can be used to get a rough estimation and it also gives the right trend for process variations.

Since gallium shows such a high diffusion coefficient in SiO_2, the FIB tool could also be used to implant Ga into a thin layer of thermally grown silicon dioxide, which would then be used as a thin film dopant source. The thickness is precisely controllable and the thermal diffusion should be very uniformly due to the high quality of the thermally grown oxide. From SRIM simulations, the projected range of Ga ions implanted into SiO_2 was extracted as $R_p(30\,\mathrm{keV}) = 25.3\,\mathrm{nm}$ with $\Delta R_p(30\,\mathrm{keV}) = 7.5\,\mathrm{nm}$ and $R_p(10\,\mathrm{keV}) = 11.7\,\mathrm{nm}$ with $\Delta R_p(10\,\mathrm{keV}) = 3.9\,\mathrm{nm}$ for an acceleration voltage 30 kV and 10 kV, respectively. To prevent extensive out-diffusion into the furnace atmosphere during the diffusion and activation anneal, a silicon nitride layer (Si_3N_4) should be considered as capping layer [180].

5.3.2 Planar p-MOSFETs Doped by Ga Implantation

The following chapter first discusses the manufacturing of planar p-MOS field-effect transistors. The source and drain regions were doped by gallium that was implanted using the FEI Expedia 1985 FIB. In the second part, *I*-*V* and *C*-*V* measurements of the S/D diodes are discussed, similar to chapter 5.3.1. The third part describes the transistor characteristics and simulations in LTspice conclude the discussions.

Manufacturing

N-doped (phosphorous, $5 \cdot 10^{15}$ Ions/cm^3) wafers (100) with a thickness of 525 μm were used as a substrate. 1000 nm of SiO_2 was thermally grown at 1000 °C (H_2O oxidation). That step could be replaced by a PE-CVD deposition at much lower temperatures (e.g. silane process at 340 °C), when the themal budget does not allow such a high temperature step. This layer later acts as the field oxide of the transistor structure. The source and drain areas were opened in the oxide layer by structuring a first lithographic mask using 2 μm AZ5214E resist. The oxide was wet etched by buffered hydrofluoric acid (BHF) and the resist was left on the wafer as a mask for the subsequent implantation. Gallium was implanted using the FIB tool. A rectangular area, overlapping source and drain (see Fig. 5.77a) was scanned by the ion beam.

The mask set from chapter 4.2.2 was again used to build these transistors. The gate lengths were in the range of 10 ... 25 μm, larger structures have not been doped. The area of the implanted rectangular was between $1.6 \cdot 10^{-5}$ ... $3.6 \cdot 10^{-4}$ cm^2, resulting in a fluence ($\Phi = \frac{J}{e} \cdot t = \frac{I}{e \cdot A} \cdot t$) between 1.3 ... $6.5 \cdot 10^{16}$ Ions/cm^2. The resist was then removed and 500 nm of SiO_2 was deposited by a PE-CVD silane process at 340 °C. The oxide was intended as a barrier against out-diffusion and also protects the sample from being contaminated and contaminating the furnace tube, respectively. Since problems arose with RF sputtered films in chapter 5.3 (see spikes in Fig. 5.70), a PE-CVD process was used here. An activation anneal was done for 15 min at 600 °C (Fig. 5.77b shows the layer structure).

The CVD oxide was subsequently removed with BHF. Since underlying was the wet thermal SiO_2 that was initially grown, an etch stop on that layer was not possible. The 1000 nm thick layer got thinned down to 890 nm.

A second mask was used to define the active area by removing the remaining SiO_2 in the channel area and in a small section around source and drain. A gate dielectric was formed by a stack of SiO_2 and Al_2O_3. The oxide was again grown by wet thermal oxidation at a temperature of 700 °C for 60 min resulting in 8 nm within the active area. In order to prevent the unwanted doping of the channel region by out-diffusion during the temperature ramp-up, oxygen (as carrier gas through the bubbler) was flowing, ensuring the growth of an oxide film from the start. As a result, 8 nm of SiO_2 was grown on the channel. Fig. 5.77c summarizes these steps.

During the 60 min at 700 °C, a diffusion length of Ga into SiO_2 of about 4.4 nm can be expected (see chapter 5.3.1). Ga diffuses fast in SiO_2 and as it can be seen in Fig. 5.76d, the segreation coefficient is $m > 1$. It can be assumed that most of the Gallium, that was diffusing into the SiO_2 during the oxide growth, escapes into the furnace space and in consequence, the surface concentration is lowered.

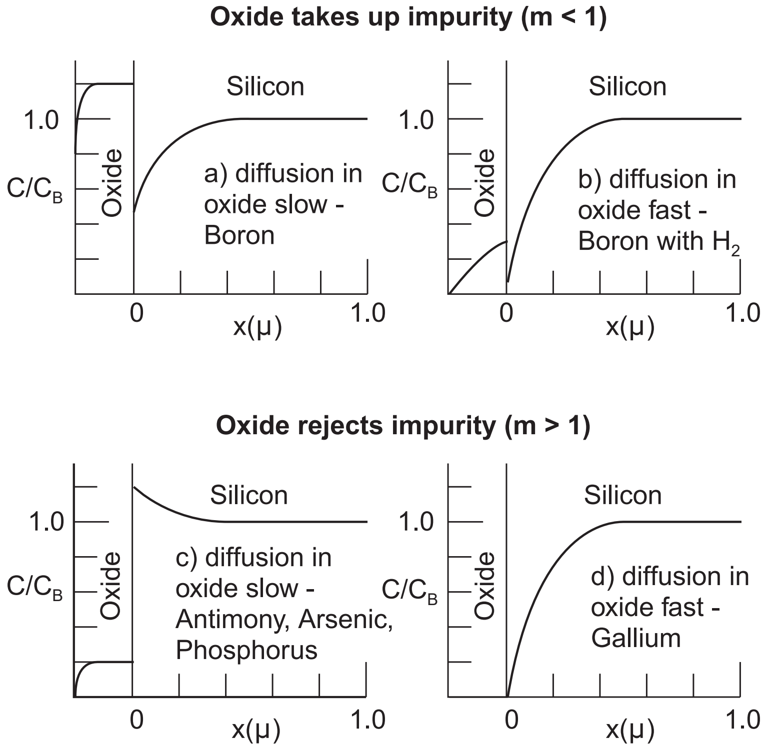


Fig. 5.76: Diffusion of different dopants during oxidation, from [173]

30 nm of Al_2O_3 was deposited on top of the SiO_2 by thermal ALD at 300 °C, with Tri-Methyl Aluminium (TMA) and H_2O as precursors. Contact holes were wet etched by the use of a third mask with BHF (Fig. 5.77d).

20 nm of Titanium and 300 nm of Aluminuim were deposited as gate metal and as source and drain contact metal. It was structured with a fourth lithographic mask and wet-etched by phosphoric acid (Al) and 0.5% HF (Ti). To ensure a good body contact, the backside of the wafer was covered with 500 nm of Al. A forming gas anneal was

then done at 400 °C (5% H_2 in N_2) for 45 min to reduce contact resistivity and to passivate oxide and interface defects. Fig. 5.77e shows the fabricated transistor structure.

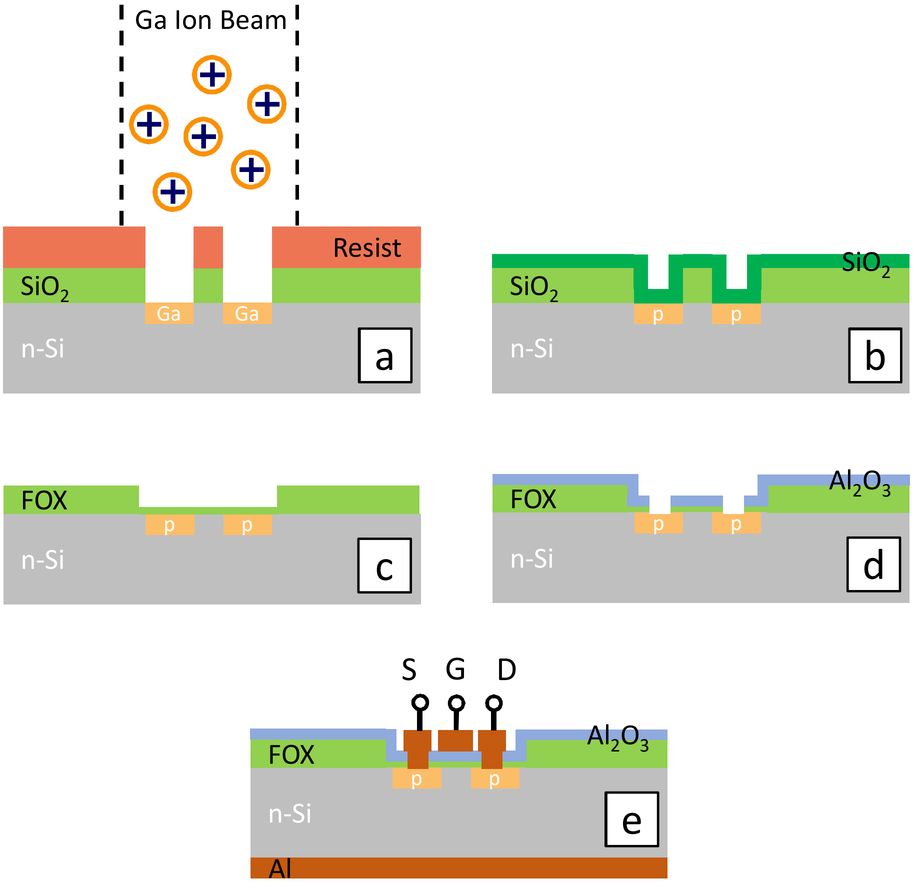


Fig. 5.77: Integration flow of the p-MOSFET fabrication using Ga implantation

Drain Diodes – I-V Measurements

The drain diodes of the transistors with a gate length of $L_G = 15\,\mu$m were characterized. The drain area was 29 μm x 65 μm. The p-region was contacted by the drain line (300 nm Al on top of 20 nm Ti, also running over the field oxide) and the n-doped subtrate was accessed by a chuck of a wafer prober from the backside. All diodes were annealed at a maximum temperature of 700 °C for 60 min (during the wet gate oxidation), similar diode characteristics are therefore expected. The variation in the ion fluence of the implantation is shown in Tab. 5.13.

Transistor	1	2	3	4	5
Ion Fluence Φ [Ions/cm^2]	1.28e+16	1.29e+16	2.33e+16	4.80e+16	6.51e+16

Tab. 5.13: Ion fluence / dose used for implantation

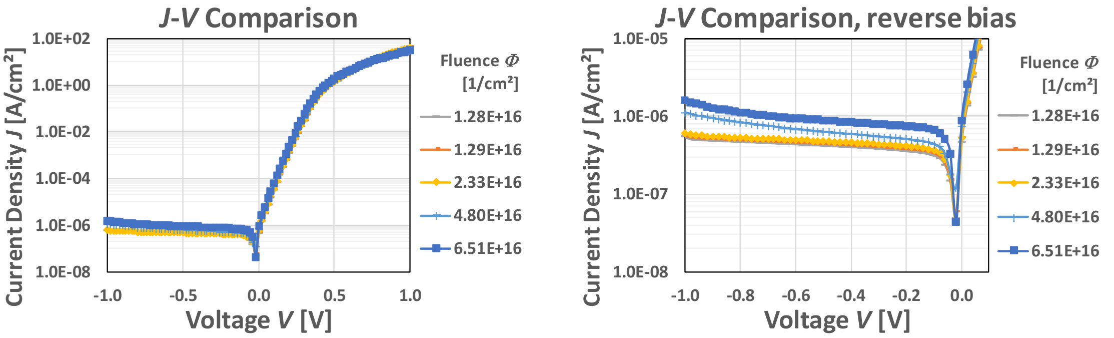


Fig. 5.78: J-V curves for the drain diodes **Fig. 5.79:** J-V comparison for reverse bias

A Keithley SMU K236 was used to perform I-V measurements of the diodes between -1 ... 1 V with 0.02 V steps. The calculated J-V curves look very similar for all implantations (Fig. 5.78). A difference can be seen in the off-current density (Fig. 5.79), but the on-current is nearly identical for all diodes. The higher the fluence, the higher is I_{off} and as a consequence the I_{on}/I_{off} ratio decreases as shown in Fig. 5.80. Since all diodes were annealed under the same conditions, the number of remaining crystal defects left should be higher for the higher fluences due to more ion bombardment, leading to higher off-currents [181].

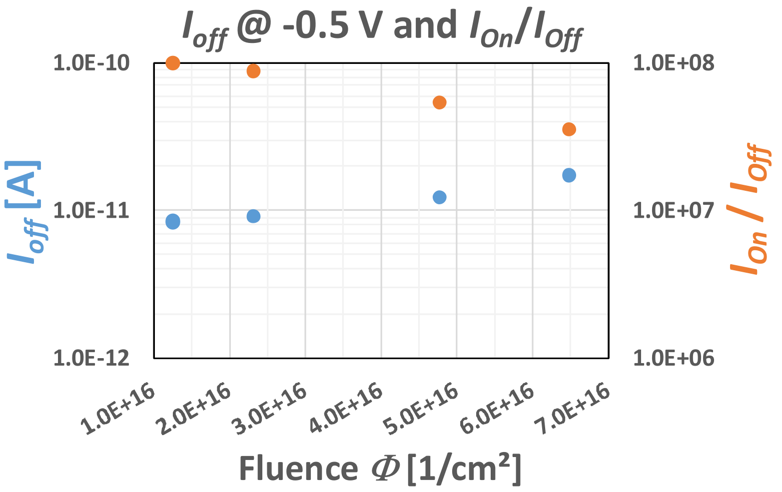


Fig. 5.80: I_{on}/I_{off} comparison for different implantation doses Φ

Drain Diodes – C-V Measurements

Capacitance voltage measurements were done at 1 kHz between -1.2 ... -0.1 V in 0.05 V steps, the voltage level was 0.1 V. The built-in voltage was extracted again by the use of the $1/C^2$ method.

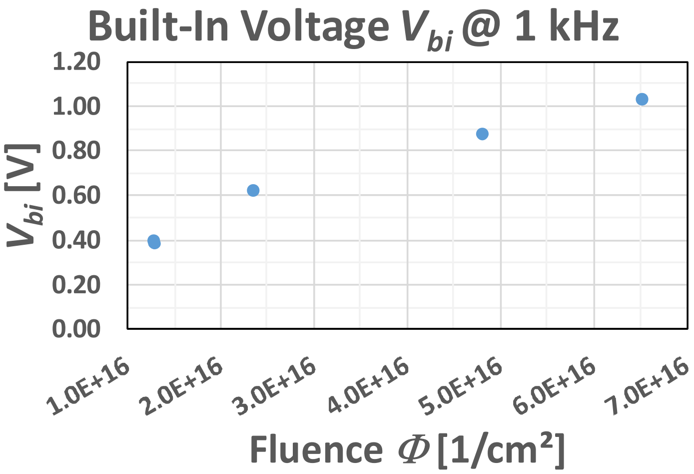


Fig. 5.81: V_{bi} for various implantation doses Φ

As it can be seen in Fig. 5.81, the higher the dose, the higher is the built-in voltage. This indicates a higher amount of activated doping atoms for more implanted gallium ions. N_A and the width of the space charge region w_{scr} (for different V_{ext}) for $N_D = 1 \cdot 10^{15}$ cm^{-3} were calculated by the use of euqations 5.3.3 and 5.3.4 and can be found in Tab. 5.14.

Ion Fluence [cm^{-2}]		1.28e+16	1.29e+16	2.33e+16	4.80e+16	6.51e+16
V_{bi} [V]		0.40	0.39	0.48	0.72	0.86
N_A [cm^{-3}]		2.4e11	1.6e11	1.7e15	2.8e19	9.2e21
w_{scr} [μm] @ V_{ext}	0 V	0.32	0.32	0.41	0.48	0.52
	-1 V	0.61	0.60	0.65	0.70	0.73
	-5 V	1.19	1.19	1.22	1.24	1.26
	-8 V	1.49	1.49	1.51	1.53	1.54

Tab. 5.14: V_{bi} and calculated N_A and w_{scr} for serveral applied voltages V_{ext}

The doping density values seem very low for the lower doses and very high for the higher implantation doses but the calculated values show a clear trend. As already mentioned in chapter 5.3.1 – the $1/C^2$ method strongly depends on the measurement frequency and the outcome should be seen as a rough estimation. Especially in this case, the V_{bi} extraction was error-prone. The drain contact metal line is also running over the field oxide, contributing to the measured capacitance value. It was subtracted to obtain the diodes capacitance only. Thickness variations of the FOX across the wafer are expected, since it was partially etched back by wet chemical etching.

Transistor Measurements

The output curves I_D-V_D and transfer curves I_D-V_G have been measured. A Keithley Semiconductor Characterization System 4200 was used for that in DC mode. All transistors (gate lengths ranging between 10 and 25 μm) showed the typical behavior. However, the transfer curves saturate quite fast, as shown in Fig. 5.82 for transistors with a gate length of $L_G = 15\,\mu$m.

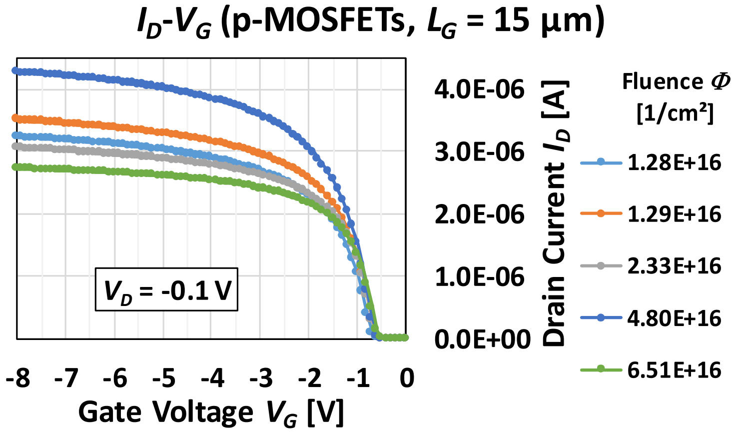


Fig. 5.82: Comparison of the transfer curves for different transistors with a gate length of 15 μm

The source and drain regions are very shallow with an approximate junction depth of 35 nm and a rather low doping concentration (10^{17} cm^{-3}). In addition, the gate is overlapping the source and drain regions and the negative gate voltage of up to -8 V ($V_{GS} = 0 \dots -8$ V) will attract many of the majorities (holes). The result is an increasing S/D resistance with increasing gate voltage V_G and consequently a saturating transfer curve ($I_D = f(V_G)$). The sub-threshold slope was found at reasonably low values of 73.2 ... 79.5 mV/dec. The $I_{D,on}/I_{D,off}$ ratios were found to be very high – $1 \cdot 10^6 \dots 1 \cdot 10^7$ for the lower fluences. Higher doses ($4.8 \cdot 10^{16}$ and $6.5 \cdot 10^{16}$ Ions/cm^2)

imply a higher degree of amorphization – the transistors showed very low $I_{D,on}/I_{D,off}$ of $3 \cdot 10^1$ and $1 \cdot 10^1$, respectively. The off-currents are higher for these devices which is in good agreement with the diode measurements of them (see Fig. 5.79).

L_{Gate}	15 μm				
Ion Fluence [cm^{-2}]	1.28e+16	1.29e+16	2.33e+16	4.80e+16	6.51e+16
$I_{D,on}$ [A]	-1.9e-4	-2.5e-4	-1.9e-4	-3.5e-4	-1.8e-4
$I_{D,off}$ [A]	-2.3e-11	-2.5e-11	-2.3e-11	*-1.2e-05*	*-1.4e-05*
$I_{D,on}/I_{D,off}$	8.4e+6	1.2e+7	8.3e+6	*2.9e+1*	*1.4e+1*
V_{th} [V]	-0.68	-0.61	-0.61	-0.62	-0.56

Tab. 5.15: $I_{D,on}/I_{D,off}$ ratio and threshold voltage V_{th} of different transistors

Tab. 5.15 shows the on/off-ratios and threshold voltages for transistors with a gate length of $L_G = 15\,\mu$m. Threshold voltage measurements (extrapolation of the ($I_D = f(V_G)$) curves to $I_D = 0$) reveal V_{th} to be between –0.56 ... -0.68 V. The output and transfer characteristics of the transistor with an implantation dose of $2.33 \cdot 10^{16}$ cm^{-2} is shown in Fig. 5.83 and Fig. 5.84.

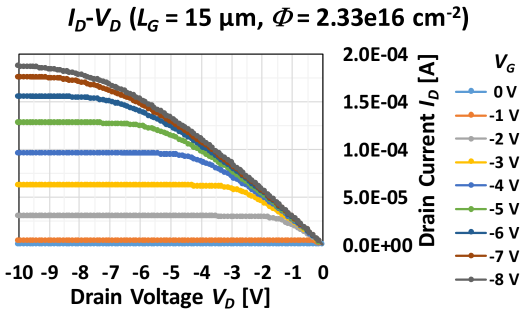


Fig. 5.83: Output curves I_D-V_D of the Ga doped transistor

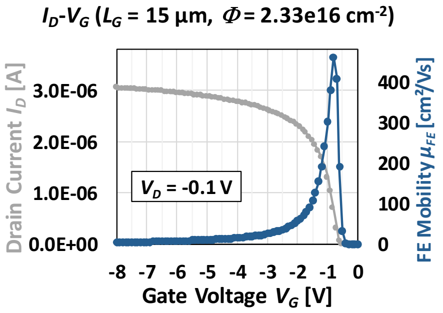


Fig. 5.84: Transfer curve I_D-V_G of the Ga doped transistor

Simulations in LTspice

Simulations in LTspice were performed using a PMOS model (level 3) for the transistor that had junctions, implanted with a dose of of $2.33 \cdot 10^{16}$ cm^{-2}. The following parameters were used:

PMOS(LEVEL=3 L=15u W=29u VTO=-0.61 TOX=22.6n TPG=0 RS=a RD=b)

All other parameters were kept at its default values. **L** is the channel length (15 μm), **W** is the channel width (29 μm), **VTO** is the threshold voltage (-0.61 V), **TPG=0** stands for a metal gate, **RS** and **RD** are the source and drain resistances that had to be varied in order to achieve a good fit between the simulation and the measurement. **TOX** is the gate oxide thickness for which an equivalent oxide thickness (EOT) of 22.6 nm was calculated. The SiO_2 was 8 nm thick ($\varepsilon_r = 3.9$) and on top of that, a layer of 30 nm Al_2O_3 ($\varepsilon_r = 8$) was deposited.
The source resistance R_S and drain resistance R_D had be drastically raised to the kΩ range to come close to a good fit for the simulation. However, it could be seen that **RS** and **RD** were not constant. The transistor behavior could be modeled by setting different R_S and R_D values for varying drain voltages V_D. This is shown in Fig. 5.85.

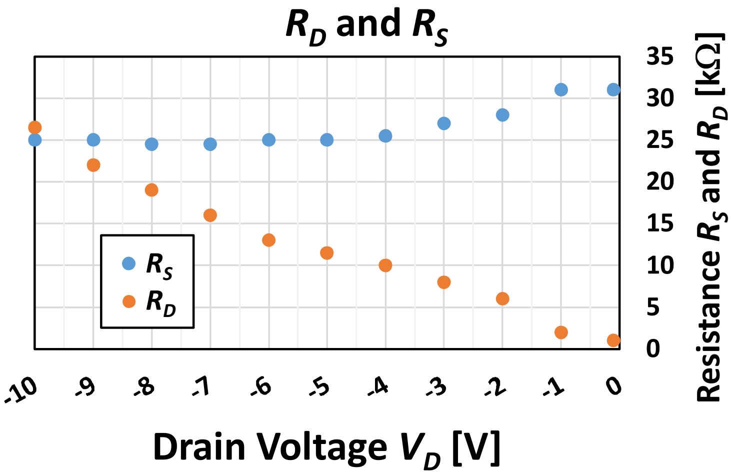


Fig. 5.85: **RD** and **RS** extracted from the simulation in LTspice

The smaller the magnitude of the drain voltage, the smaller is the resulting space charge region around the drain diode and the lower is its transition resistance to the channel. R_S is relatively stable, making up for a constantly high total resistance across the source to drain path. The assumption of high S/D resistances due to low doping concentration was confirmed by this. Feeding these transfer curves back to construct the output curves gives a good fit, as it can be seen in Fig. 5.86. The measured output curves are represented by the lines, the data points (crosses) visualize the simulated result.

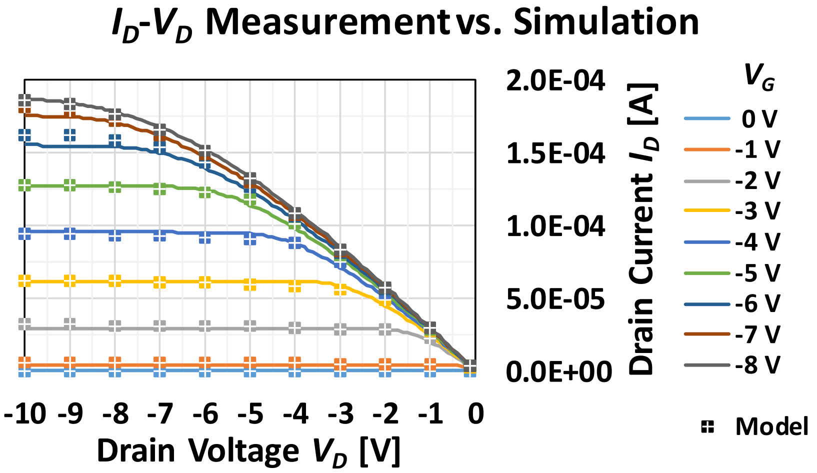


Fig. 5.86: Output characteristics – Simulation vs. measurement of the p-MOS transistor with $L_G = 15\,\mu$m and $\Phi = 2.33 \cdot 10^{16}$ 1/cm^2

For a 35 nm junction depth, the total resistance of about 32 kΩ (for $V_D = -0.1$ V) corresponds to a doping concentration of $7 \cdot 10^{17}$ cm^{-3} and a resistivity of 0.05 Ωcm, respectively. For this estimation, the distance between the contact holes and the channel was considered – two squares with an edge length of 29 μm on the source and on the drain side (see Fig. 5.87). This is in good agreement with the better diodes from chapter 5.3.1 that showed R_{4pp} values of about 1 kΩ, which translates to 0.02 Ωcm.

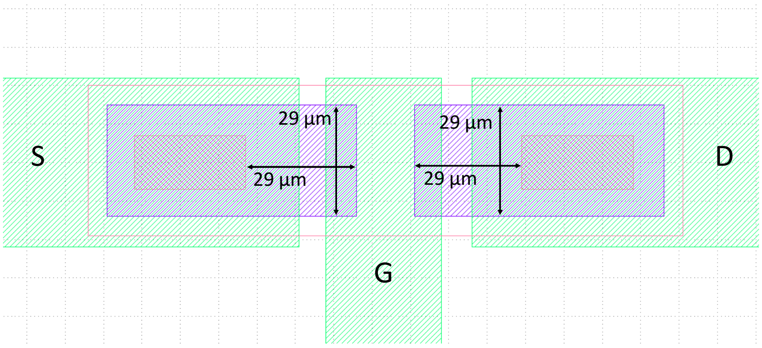


Fig. 5.87: Screenshot from the design of the transistor structure with a gate length of 15 μm

5.3.3 Proposal for a parallel integration of Cu TSVs and p-TSVFETs

The manufacturing of planar Ga doped devices was demonstrated in chapter 5.3.2. In this chapter, a process flow for p-TSVFETs with implanted Ga source and drain regions is proposed. The integration in such a way allows the co-fabrication of electrical interconnects and TSV transistors on the same interposer.

In chapter 5.3.2, a maximum temperature of 700 °C was used to grow the gate oxide after the junctions were formed. As shown in chapter 5.1.2, the channel of the TSVFET was smoothed by a sacrificial oxidation at 1000 °C. However, experiments have shown that Ga tends to agglomerate under very high temperatures, invalidating its function as a dopant. Therefore, it would be highly favorable to first etch, clean and smoothen (thermal oxidation + back etching) the TSV holes and only then implant the gallium. An integration of TSV interconnects (filled with Cu) and TSVFETs on the same interposer is a possibility. The isolation of the Cu TSVs could be formed in the same step by covering the interconnect TSVs with photo resist before etching back the sacrificial oxide (see Fig. 5.88-(1)).

Following this route, preventing side-wall doping would be the most important part during the implantation. The TSVs should first be filled with a sacrificial material, subsequently to its etching and smoothing. Otherwise, the S/D regions would reach uncontrollably deep or the p-FETs would even be depletion-type devices due to unintentional channel doping. Photo resist is a typical masking material for implantations and with the right viscosity, the filling of the TSVs should not be a problem. As shown in Fig. 5.88-(2), the area around the TSVFETs should be lithographically opened to allow the implantation. The dose to clear should only be reached on the wafer surfaces, in order to prevent the development of the resist inside the holes. A possible thin residual layer could be removed by a short O_2 plasma flash.

The implantation of gallium would follow with a dose, taken from chapter 5.3.2.

As depicted in Fig. 5.88-(3), a wet gate oxidation at 700 °C for 60 min could follow to form a thin interfacial oxide layer (8 nm SiO_2, compare to chapter 5.3.2), to activate the gallium and to anneal the amorphized Si at the same time. Subsequently, Al_2O_3 would be deposited by thermal ALD to increase the thickness of the dielectrics, allowing higher operation voltages without electrical breakdown and to assure a threshold voltage well beyond 0 V.

Contact hole structuring follows for the TSVFETs by wet etching. As it is illustrated in Fig. 5.88-(4), the holes in the photo resist mask, could directly be used as a lift-off

mask to implement a contact metal (such as Ni, Ti or Co) on the p-doped Si.
Thermal ALD processes could be used to deposit Ru/TaN/Ru as the metal gate stack (as published in [119]) and it would function as the seed layer for the ECD of Cu at the same time [183], [184] (Fig. 5.88-(5)). The underlying Al_2O_3 ensures a fast and reliable initial growth of the Ru, when ECPR and O_2 are used as the precursors.
TaN is introduced as diffusion barrier for Cu, that should be deposited electrochemically in the next step, as shown in Fig. 5.88-(6) [130], [131], [132]. Chemical mechanical polishing (CMP) would follow the Cu deposition, stopping on the Ru layer, as it was done in [182]. In the next step, the Ru/TaN/Ru stack would be structured by RIE, to cut the gate and to define the S/D metal lines of the TSVFETs. Around the interconnect TSVs, the metal would be completely removed to electrically separate them from each other. The Cu filling serves the vertical interconnects as the conductive material, but represents the gate contact of the p-TSVFETs.

The parallel intergration of TSVFETs and Cu interconnects on a Si interposer was not done yet. In this chapter, a possible process flow is proposed for the first time. Although designed specifically for Ga doping, it should not be limited to it. Boron or phosphorous doping could be done before the etching of the TSVs, staying closer to the integration schemes in chapters 5.1.2 and 5.2.2.

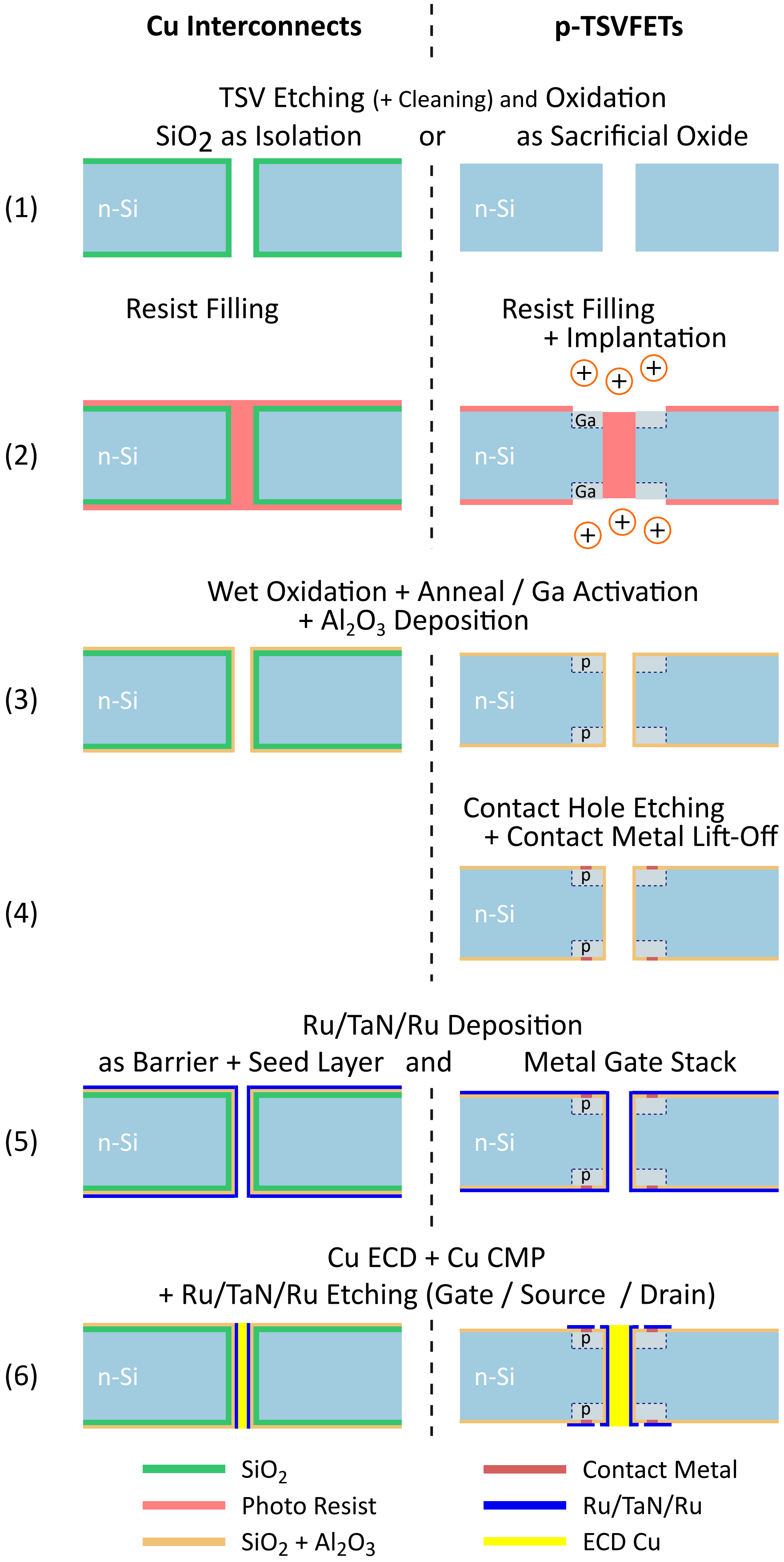


Fig. 5.88: Process sequence for the parallel manufacturing of p-TSVFETs with Ga implantations and Cu interconnects on one Si interposer

6 Summary and Outlook

The 3D integration of microchips and especially the use of through silicon VIAs (TSVs) is one way to overcome the upcoming limitations in down-scaling of the transistor device structures. It allows the integration of more functionality ("More than Moore") while keeping the chip footprint constant and makes a further increase of the volumetric transistor density ("More Moore") possible. This work was aiming for the functionalization of the TSVs, expanding their purpose of use from simple vertical electrical connections to actively switching devices. As summarized in the following, the **TSVFET** was implemented as n-MOS and p-MOS transistor and as a semiconductor memory device, using the charge trapping character of the gate stack.

As prerequisite knowledge, investigations on the doping by thermal diffusion from thin films were presented in chapter 5.1. The doping concentration profiles for phosphorous (from spin-on dopants) and boron (from thin highly boron-doped micro-crystalline Si layers) doping of silicon were obtained for numerous diffusion parameters (temperatures and times) as a precondition for the fabrication of active semiconductor devices. The integration and manufacturing of field-effect transistors inside through-silicon VIAs has been demonstrated and discussed in detail. n- and p-FETs could be implemented on substrates with the corresponding bulk doping. Fig. 6.1 shows a schematic of the TSV transistor (n-FET) and in Fig. 6.2 SEM images of the upper, middle and lower part of the realized n-TSVFET are depicted.

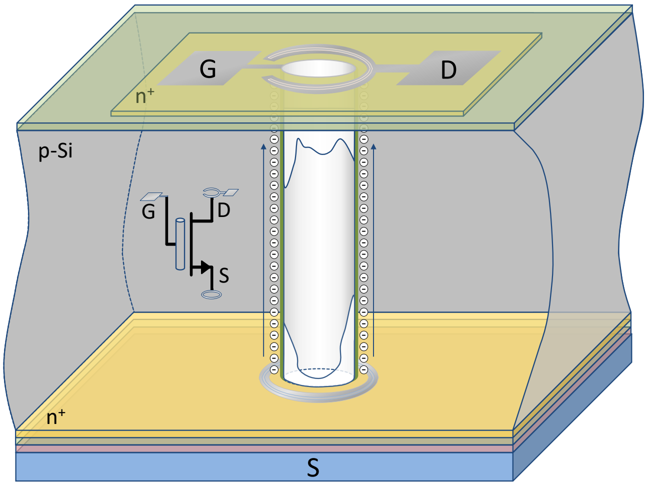


Fig. 6.1: Schematic of the TSV transistor

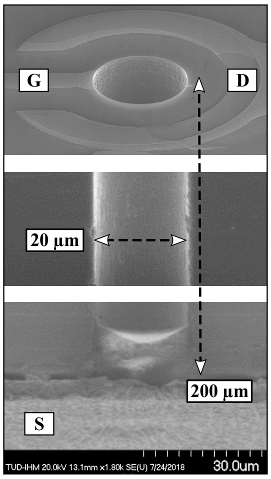


Fig. 6.2: SEM images of the upper, middle and lower part of an n-TSVFET realized in this work

Since the transistor channel of these devices is made up of an etched silicon surface created by deep reactive ion etching (Bosch process), it is accordingly defect-rich. The smoothness of the sidewalls strongly influences the electrical characteristics of the FETs. The well-optimized etching recipe for TSVs on p-Si wafers with a $200\,\mu$m thickness ($20\,\mu$m hole diameter) enables the manufacturing of n-TSVFETs with excellent switching behavior (high $I_{D,on}/I_{D,off}$ ratio of 10^6 for a gate voltage of 4 V) and a sub-threshold slope of 125 mV/dec. For p-TSVFETs (on n-Si wafers of $300\,\mu$m thickness) the channel surface holds higher amounts of charge traps that have to be charged and discharged during switching, leading to a relatively high sub-threshold slope of 370 mV/dec. Due to the lower mobility of holes compared to electrons and higher off-currents than for the n-FETs, the $I_{D,on}/I_{D,off}$ ratio of the p-FETs measured 10^3 for a gate voltage of $V_G = -4\,\mathrm{V}$.

Another main goal was the realization of ferroelectric transistors inside the TSVs and thus the functionalization as memory devices. Planar test structures of p-FeFETs were fabricated for the first time and showed a stable memory window of $> 2\,\mathrm{V}$ for more than 10^3 cycles, as discussed in chapter 5.2. The influence of the low-k interface layer thickness on the endurance and storage behavior has been investigated. Ferroelectric switching was observed for 15 nm of hafnium zirconium oxide (HZO) on thin SiO_2 interface layers (1.6 nm and 2 nm) but charge trapping dominated for interface oxides with a thickness of 4 nm. The thinner the interface oxide, the lower is the resulting depolarization field – consequently the higher was the data retention time. The transfer of this knowledge to the p-TSVFETs was also presented. For an interface layer thickness of 4 nm, charge trapping on the gate was confirmed and a one-transistor memory device with a memory window of about 1 V could be demonstrated inside the TSVs. Due to high gate leakage, charge trapping was dominating over the ferroelecric switching effect for the thinner interface oxides and a FE memory device could not be implemented.

In chapter 5.3, focused ion beam (FIB) implantation of gallium has been studied for the doping of Si. Diodes have been fabricated and characterized and the use of gallium for the source / drain doping of a planar p-FET was successfully demonstrated. Gallium implants can be annealed and activated at moderate temperatures of 500 ... 700 °C and could be proven as an alternative dopant for low thermal budgets. A proposal for the co-integration of TSVFETs and copper-filled TSVs on the same interposer was additionally given. In this context, gallium implantation was discussed as a possibility. Generally speaking, the demonstration of p-FETs doped by the use of a gallium FIB system, shows the feasibility of mask-less direct writing of doped structures in silicon.

Outlook

For the further optimization of the TSVFETs, a recessed gate approach (proposed in chapter 5.1.2) should be tested. Here the channel length of the fabricated transistors was given by the substrate thickness. A recess would enable an increased drain current due to a decreased channel length. The optimization of the etch depth uniformity across the wafer is expected to be the most challenging task, since it defines the transistor gate length and the output current is directly influenced by it.

The charge trapping devices, that were realized inside the TSVs (chapter 5.2.2) should be further characterized. Above all, cycling tests should be performed as well as temperature stress should be applied in order to obtain the endurance and data retention times.
Moreover, hafnium zirconium oxide should be used in the gate stack of the n-TSVFETs as well. Due to the higher mobility of electrons compared to holes, it promises higher drain currents and $I_{D,on}/I_{D,off}$ ratios. The much more optimized etching recipe for the p-doped wafers of 200 μm thickness compared the n-doped wafers of about 300 μm thickness, provides smoother sidewalls and the domination of the ferroelectric switching effect over charge trapping is much more likely.

Furthermore, gallium should be used for the doping of the source and drain regions of the TSVFET in order to demonstrate the usability of the suggested low-temperature process flow (maximum temperature 700 °C for anneal and gate oxidation, discussed in chapter 5.3.3). Especially when metals are involved, the thermal budget is very limited and low activation temperatures would be an enabler to fabricate active devices in the presence of a metallization.

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A Appendix

A.1 Resistivity and Dopant Density

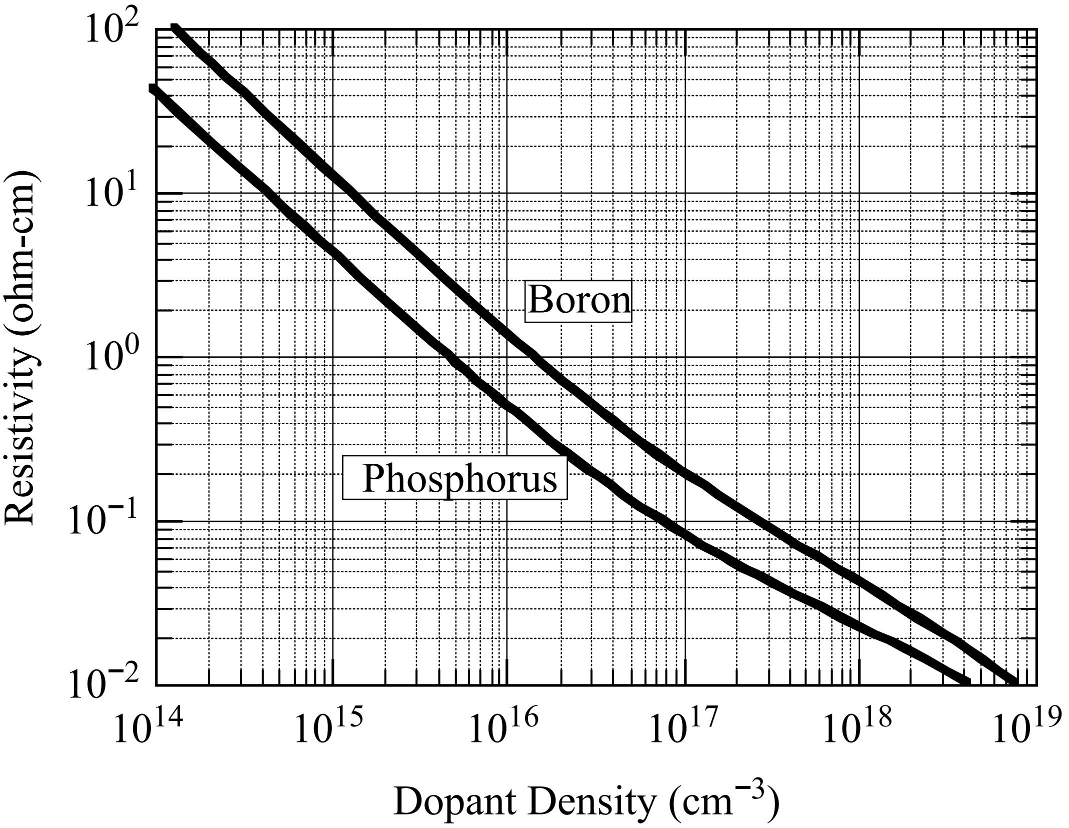

Fig. A.1: Resistivity over dopant density for n-type (phosphorus-doped) silicon at 23 °C, from the ASTM standard F723-99 [88]

A.2 Mask set for the TSVFET

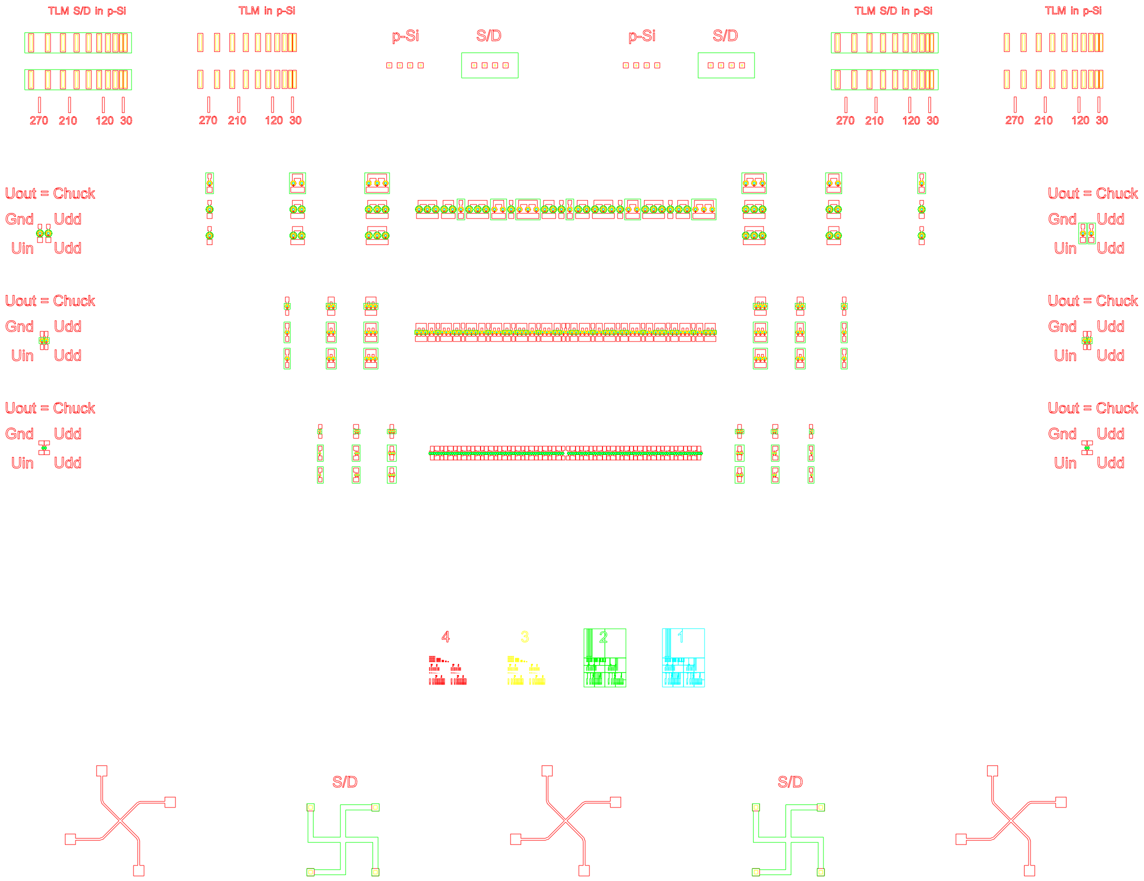

Fig. A.2: Overview of the mask set for the TSVFET; the entire block can be found four times on the mask, vertically arranged

A.3 Mask Design of the Planar Test Structures

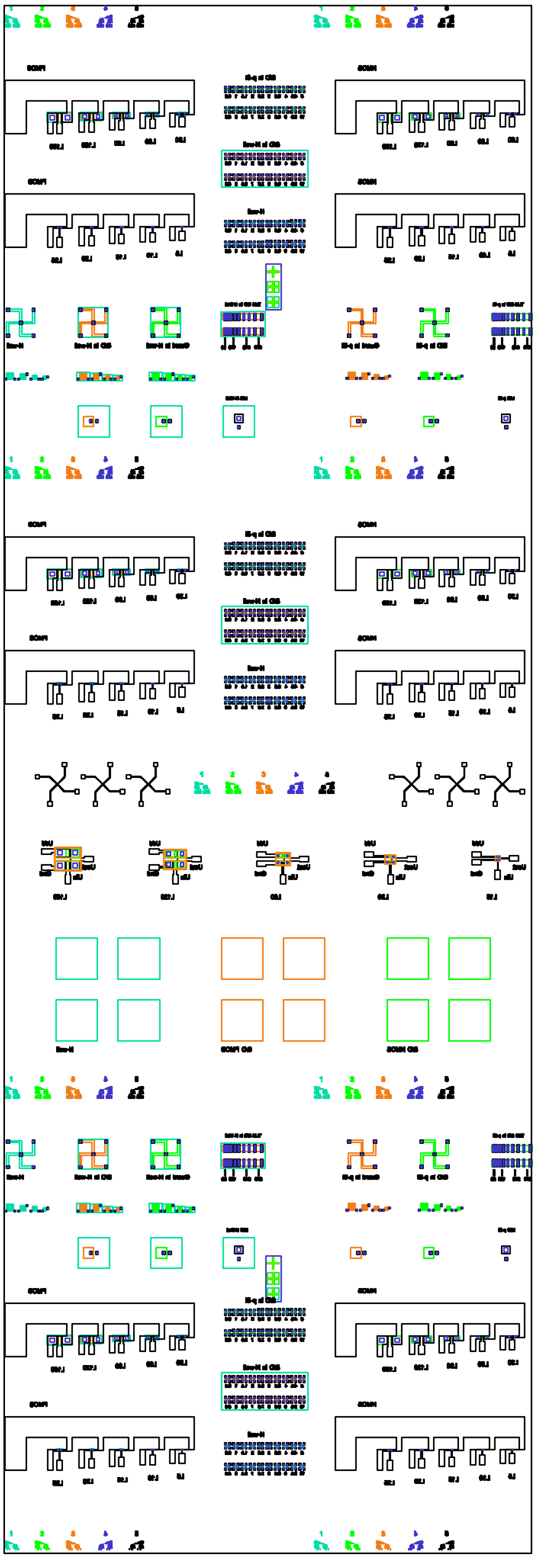

Fig. A.3: Overall view of the mask design (planar FETs), dimensions: 3 cm × 8 cm

Curriculum Vitae

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Date of Birth	March, 31st 1988
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Academic Career

Scientist / PhD Student Dec. 2013 – present	TU Dresden, Institute for Semiconductors and Microsystems: Research on the integration of novel field-effect transistors
Master studies (M. Sc.) Oct. 2011 – Nov. 2013	**Nanoelectronic Systems**, TU Dresden, Master thesis "Development of a Stable Process Flow for Field-Effect Transistors Manufactured by the Use of the Diffusion Technique"
Bachelor studies (B. Eng.) Sep. 2006 – Aug. 2011	**Microtechnology (Cooperative Program with Qimonda Dresden)**, UAS Zwickau, Bachelor thesis at GLOBALFOUNDRIES Dresden "Root Cause Investigations Regarding ESD Damage on Photomasks in a Wafer Fab using the E-Reticle^{TM}"

Teaching Experience

Tutor Oct. 2014 – Sep. 2017	**Basics of Electrical Engineering** and **Electrical and Magnetic Fields**, TU Dresden, Faculty of Electrical and Computer Engineering

Laboratory Course Advisor Apr. 2016 – Sep. 2019	**Semiconductor Technology: Photolithography**, TU Dresden, Chair for Semiconductor Technology

Miscellaneous

Student Employee Aug. 2010 – Mar. 2013	**GLOBALFOUNDRIES Dresden**, Dept. Lithography (Photomasks), ESD Root Cause Investigations, Defect Printability Studies, Reticle Requalifications
Internship Jul. – Sep. 2009	**X-FAB Dresden**, Dept. Lithography, Improvement and Optimization of a Polyimide Spin-Coating Process
Trainee Sep. 2008 – Jun. 2009	**Qimonda Dresden**, Dept. Lithography (Photomasks), Practical Part of the Integrated Degree Program
Support Operator Jun. – Aug. 2006	**Infineon Dresden**, Dept. Wafer Inspection, Optical Defect Measurements of Resist Structures on 8-inch Product Wafers

List of Scientific Publications

Conference Talks

1) F. Winkler, S. Killge, M. Pešić, and J. W. Bartha, "TSVFET – Vertical 3D Field-Effect Transistor," in *2019 IEEE International Interconnect Technology Conference (IITC)*, **2019**.
2) F. Winkler, M. Pešić, M. Hoffmann, T. Mikolajick, and J. W. Bartha, "Demonstration and Endurance Improvement of p-channel Hafnia-based Ferroelectric Field Effect Transistors," in *2019 77th Device Research Conference (DRC)*, **2019**.

Articles in Conference Proceedings as First Author

1) F. Winkler, S. Killge, M. Pešić, and J. W. Bartha, "TSVFET – Vertical 3D Field-Effect Transistor," in *2019 IEEE International Interconnect Technology Conference (IITC)*, IEEE, **2019**.
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2) F. Winkler, M. Pešić, M. Hoffmann, T. Mikolajick, and J. W. Bartha, "Demonstration and Endurance Improvement of p-channel Hafnia-based Ferroelectric Field Effect Transistors," in *2019 77th Device Research Conference (DRC)*, **2019**, 51.

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1) T. Henke, M. Knaut, M. Geidel, F. Winkler, M. Albert, and J. W. Bartha, “Atomic layer deposition of tantalum oxide thin films using the precursor tert-butylimido-tris-ethylmethylamido-tantalum and water: Process characteristics and film properties,” in *Thin Solid Films*, **2017**, 627, 94.
2) C. Strobel, C.A. Chavarin, B. Leszczynska, S. Leszczynski, F. Winkler, S. Killge, S. Völkel, K. Richter, A. Hiess, M. Knaut, J. Reif, M. Albert, Ch. Wenger, and J. W. Bartha, “Demonstration of a graphene-base heterojunction transistor with saturated output current,” in *Journal of Applied Physics*, **2019**, 125, 234501.
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