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pinMOS Memory:
A novel, diode-based organic memory device

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Abstract

A novel, non-volatile, organic capacitive memory device called p-i-n-metal-oxide-semiconductor (pinMOS) memory is demonstrated with multiple-bit storage that can be programmed and read out electrically and optically. The diode-based architecture simplifies the fabrication process, and makes further optimizations easy, and might even inspire new derived capacitive memory devices. Furthermore, this innovative pinMOS memory device features local charge up of an integrated capacitance rather than of an extra floating gate.

Before the device can perform as desired, the leakage current due to the lateral charge up of the doped layers outside the active area needs to be suppressed. Therefore, in this thesis, lateral charging effects in organic light-emitting diodes (OLEDs) are studied first. By comparing the results from differently structured devices, the presence of centimeter-scale lateral current flows in the n-doped and p-doped layers is shown, which results in undesirable capacitance increases and thus extra leakage currents. Such lateral charging can be controlled via structuring the doped layers, leading to extremely low steady-state leakage currents in the OLED (here 10^{-7} mA/cm^2 at -1 V). It is shown that these lateral currents can be utilized to extract the conductivity as well as the activation energy of each doped layer when modeled with an RC circuit model.

Secondly, pinMOS memory devices that are based on the diode with structured doped layers are investigated. The memory behavior, which is demonstrated as capacitance switching for electrical signals, and light emission for optical signals, can be tuned either by the applied voltage or ultraviolet light illumination, respectively. The working mechanism is explained by the existence of quasi steady-states as well as the width variation of space charge zones. The pinMOS memory shows excellent repeatability, an endurance of more than 10^4 write-read-erase-read cycles, and currently already over 24 h retention time. Furthermore, an early-stage investigation on emulating synaptic plasticity reveals the potential of pinMOS memory for applications in neuromorphic computing. Overall, the results indicate that pinMOS memory in principle is promising for a variety of future applications in both electronic and photonic circuits. A detailed understanding of this new concept of memory device, for which this thesis lays an important foundation, is necessary to proceed with further enhancements.

Zusammenfassung

Es wird ein neuartiges, organisches kapazitives Speicherelement demonstriert, das p-i-n-Metalloxid-Halbleiter (pinMOS) Speicher genannt wird und eine Mehrfachbitspeicherung besitzt, die elektrisch und optisch programmiert und ausgelesen werden kann. Die auf einer Diode basierende Architektur vereinfacht den Herstellungsprozess sowie die weitere Optimierung und könnte sogar Inspiration für neue kapazitive Speichermedien sein. Darüber hinaus basiert dieses innovative pinMOS Speicherelement auf der lokalen Aufladung einer integrierten Kapazität und nicht auf einem zusätzlichem "Floating Gate".

Bevor das Speicherelement wie gewünscht funktioniert, muss der Leckstrom, der durch die laterale Aufladung der dotierten Schichten außerhalb des aktiven Bereichs verursacht wird, unterdrückt werden. Deshalb werden in dieser Arbeit zuerst die lateralen Aufladungseffekte in organischen Leuchtdioden (OLEDs) untersucht. Beim Vergleich verschiedener Device-Strukturen wird die Existenz von lateralen Stromflüssen im Zentimeterbereich in den n- und p-dotierten Schichten gezeigt, was zu einer unerwünschten erhöhten Kapazität und folglich einem höheren Leckstrom führt. Diese laterale Aufladung kann durch die Strukturierung der dotierten Schichten kontrolliert werden, was zu extrem geringen Gleichgewichtsleckströmen in den OLEDs (10^{-7} mA/cm^2 bei -1 V) resultiert. Es wird auch gezeigt, dass die lateralen Ströme genutzt werden können um die spezifische Leitfähigkeit sowie die Aktivierungsenergie der einzelnen dotierten Schichten zu extrahieren, wenn diese mit einem RC-Modell modelliert werden.

Im zweiten Teil werden pinMOS Speicherelemente, die auf der Diode mit strukturierten dotierten Schichten basieren, untersucht. Das Speicherverhalten, dass durch Kapazitätsschaltung für elektrische Signale und als Lichtemission für optische Signale gezeigt wird, kann entweder durch die angelegte Spannung, beziehungsweise durch die Belichtung mit ultraviolettem Licht eingestellt werden. Die Wirkungsweise wird durch die Existenz quasistatischer Gleichgewichte sowie durch die Größenänderung der Raumladungszonen erklärt. Der pinMOS Speicher zeigt eine hervorragende Wiederholbarkeit, eine Beständigkeit über mehr als 10^4 Schreiben-Lesen-Löschen-Lesen Zyklen und aktuell schon eine Retentionszeit von über 24 h. Weiterhin offenbaren erste Versuche in der Nachahmung von Neuronaler Plastizität das Potenzial von pinMOS Speichern für Anwendungen im "Neuromorphic Computing". Insgesamt deuten die Ergebnisse an, dass pinMOS Speicher prinzipiell vielversprechend für eine Vielzahl von zukünftigen Anwendungen in elektronischen und photonischen Schaltkreisen ist. Ein tiefgreifendes Verständnis von diesem Konzept neuartiger Speicherelemente, für das diese Arbeit eine wichtige Grundlage bildet, ist notwendig, um weitere Verbesserungen zu entwickeln.

Contents

Chapter 1

Introduction

We are living in a more and more electronic world where electronics like computers and phones, accompanied by modern communication techniques like internet, occupy our daily life. Electronics based on inorganic materials, i.e., silicon, are the main body of commercial applications owing to their advanced fabrication techniques and remarkable device performance [1]. However, silicon-based devices cannot meet the emerging application requirements on flexibility and optical transparency, indicating that inorganic electronics are not appropriate candidates for the future tendency in foldable electronics or flexible electronics [2]. Furthermore, the expensive and energy-intensive fabrication process limits the further development of silicon-based devices. Therefore, organic electronics that involve semiconductors, dielectrics, electrolytes, ferroelectrics, and even biological organisms, have been intensely investigated in the last decade. Their potential to make ultra-lightweight, low-cost, large area, printable electronics promises several commercial applications including electronic papers, imagers, sensors, organic light-emitting diode (OLED) drivers, etc [3-8]. Some of them can already reach the real consumer market, especially OLED based color displays that widely used in TV, computer, phone with long lifetime and high efficiency. Other organic electronics like organic field-effect transistors (OFETs) and organic solar cells (OSCs) are on the way to commercialization, while more exotic devices such as organic memories and lasers are studied with high expectations.

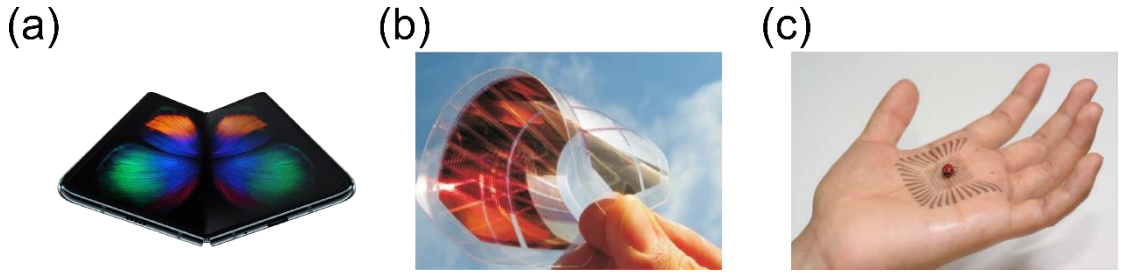


Figure 2.1.1: Photographs of (a) phone with foldable OLED display, (b) flexible OSCs, and (c) skin electronics based on stretchable transistor array. Pictures are taken from [9-11].

Among major devices now being investigated in this large and ever-growing field, the demand for organic memory devices, which are data storage devices, increases along with the advance of digital information technology. Three memory technologies dominate the market: silicon-based solid state dynamic random access memory (DRAM) and flash memory, and inorganic magnetic hard disk

drives [12], [13]. Emerging technologies such as resistive random access memory (ReRAM), single transistor-based memory comprising a floating gate layer as charge-storage (trapping/detrapping) layer, ferroelectric memory including ferroelectric random access memory (FeRAM) and ferroelectric field-effect transistor (FeFET), phase-change random access memory, electrochemical memory have been intensively studied and some of them are about to enter the market [14-18]. To take advantage of unique properties from organic electronics for extending the field of applications, a wide variety of organic materials or hybrid materials, including polymers, small molecules, hybrid perovskite, ferroelectric organic polymers, have been studied and utilized as hysteretic elements in integrated memory devices, especially in organic non-volatile memory (ONVM) devices [19], [20]. Despite the architectural difference, organic memory devices that are most widely studied are those holding information by using resistance-switching behavior, which can be modeled by employing memristive equations and are widely proposed to participate in artificial neural networks as artificial neuromorphic devices [21-23]. However, another type of memory devices, the memcapacitors or capacitive memory devices, have received less attention although it can also possess memory behavior via switchable capacitances and even superior in prospective applications (like artificial neural networks) with lower power consumption and free of steady-state crosstalk currents [24-26]. Furthermore, similar to the role of OLED in electronics, memory devices nowadays should not limit to electrical accessibility but have functionality though optical pathways such as storage and read out of information via light emission. Such kind of memory devices are referred to as optical storage devices.

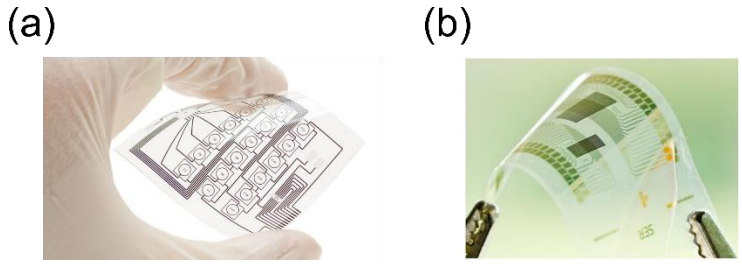


Figure 2.1.2: Photographs of (a) organic flash memory and (b) re-programmable non-volatile memory arrays produced on flexible substrates. Pictures are taken from [27], [28].

With the consideration of appropriate device architecture, storage capabilities, device down-scaling, optical switching and read-out property, as well as easy fabrication, a novel concept of diode-based, non-volatile, capacitive memory device is demonstrated in this thesis. In the beginning, a fundamental introduction of organic semiconductors is provided in Chapter 2 as a theoretical background for carbon-formed molecules as well as the related charge carrier motions. Based on this knowledge, concepts of organic junctions like Schottky junction, p-n junction, p-i-n junction and devices like MOS capacitor and OLED, are further discussed in Chapter 3. An overview of organic memory devices is then presented in Chapter 4 with a focus on organic resistive memory devices, organic transistor-based memory devices, and organic ferroelectric memory devices. Within Chapter 5, the basics of experimental techniques that have been used for device fabrication and characterization are described, along with an overview of materials used in this thesis.

In order to obtain a structure comprehension for further memory device optimization, the results part starts with Chapter 6 by investigating the centimeter-scale lateral charge flow in crossbar structure

with doped layers that are larger than the active area. Not limited to the memory devices studied in this thesis, organic devices commonly have crossbar structures where doped layers are applied (with larger occupied area than active area) in a sandwich layer architecture stacked between two electrodes. The high conductivity of doped layers facilitates the charge carrier transport and thus device performance in organic electronics, but sometimes introduces a rarely noticed side-effects of leakage current and extra capacitance increase at low frequency. The leakage currents are in general unwanted for electronics as they increase the device's power consumption, reduce the on-off or rectification ratio of transistors and diodes, and remove the information stored in memory device and thus ruin the basic memory function. Here, by studying the centimeter scale lateral charge flow in OLEDs, an easy and effective method is proposed to prevent the introducing of leakage current by structuring the doped layers. With the assistance of a newly developed RC circuit, the controlled capacitive charge up of the doped layers outside the active area can be used for extracting the information about the conductivity as well as the corresponding activation energy of the n-doped and p-doped layer, simultaneously. In this way, the doped layer quality can be easily checked after device fabrication. More importantly, the device layout, especially for the memory device, is proven to require have well-structured doped layers.

Further results and investigations regarding the proposed p-i-n-metal-oxide-semiconductor (pinMOS) memory are presented in Chapters 7 and 8. The pinMOS memory device is a memory device with multiple-bit storage that can be tuned and read out electrically or optically, i.e., it can be programmed by either voltage application via Zener tunneling or ultraviolet light illumination, and be read-out by either capacitance (electric signal) or light emission (optical signal). The pinMOS memory is based on an OLED with an integrated capacitor on which charges can be added or removed in fractions, revealing a very decent memory performance in terms of repeatability, cyclic endurance, and retention time. The working mechanisms, both under quasi and dynamic steady-state operation conditions, are proposed to get an essential understanding of this novel concept of device for further optimization or applications. Three advantages are pointed out for the pinMOS memory: easy to achieve multiple-bit storage and possibility for device downscaling; an easy fabrication process that is a straight-forward layer-by-layer deposition similar to OLED; the ability to be written and read out by light, which is attractive for future use in integrated electronic and photonic circuits.

As summarized in Chapter 8, the pinMOS memory and the basic understanding behind it might open the pathway for future applications not only in the general electrical memory system but also in the full-color visual system, optical-electrical-optical repeater systems, or capacitive neural networks.

Finally, a conclusion of the work is given in Chapter 9.

Chapter 2

Fundamentals of organic semiconductors

In this chapter, the basic physical properties of organic semiconductors are introduced from aromatic organic molecules to solids and related charge carrier behaviors. The hybridization of carbon atoms and the resulting stable molecules with partially delocalized electrons are shown in Sec. 2.1 by using examples of ethane and benzene. The transition from a single molecule to a solid state molecule is discussed with the consideration of interactions between molecules and the spin of electronic state. Furthermore, two different charge carrier transport models are overviewed in Sec. 2.2 with different applicable conditions. Besides charge transport in the semiconductor, the injection from electrode is also highlighted in Sec. 2.3 with aspects of contact interface, current limitations regarding the injection barrier, and injection mechanism models. The doping, which is important for improving both, the charge carrier mobility and injection efficiency, is demonstrated in Sec. 2.4. This chapter paves the fundamental way of understanding semiconductor devices.

2.1 Electronic states of a molecule

2.1.1 Atomic orbitals and molecular orbitals

Organic semiconductor materials are carbon-based materials with heteroatoms, therefore the discussion will start with the electronic structure of carbon atoms. A single carbon atom has six electrons in its ground state and atomic orbitals are referred to as s orbital and p orbital with angular momentum quantum number of 1 and 2, respectively. As illustrated in Fig. 2.1.1 (a), the s orbital is radially symmetric with a spherical charge distribution while the three p orbitals named after the plane in which they lie have a positive and a negative (the sign of the wavefunction) lobe with a "dumbbell" charge distribution [29]. The possibility of the electron being in either lobe in one p orbital is the same. When two atomic orbitals hybridize, molecular orbitals called σ-orbitals will be formed if it is head-on overlapping, otherwise π-orbitals will be formed if it is side-by-side overlapping (Fig. 2.1.1 (b)) [30].

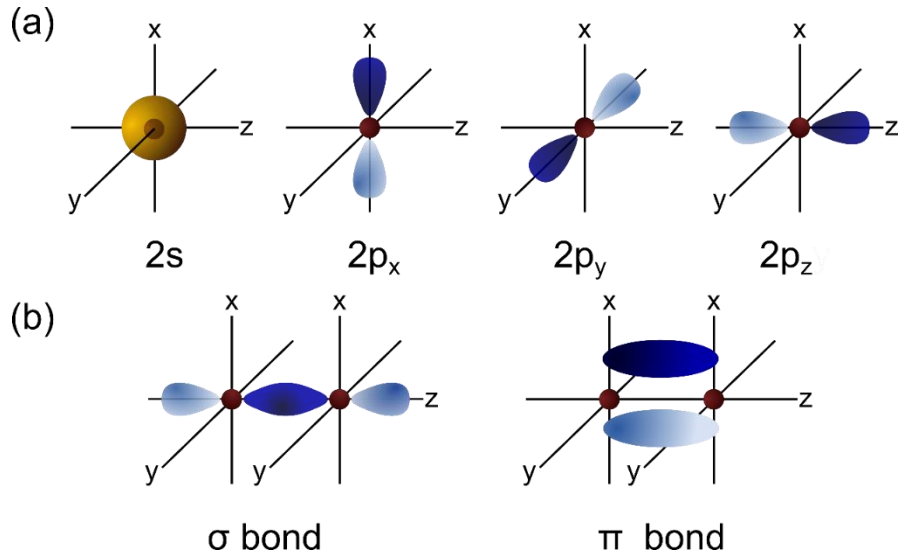


Figure 2.1.1: (a) The atomics and p orbitals. (b) The molecular σ and π orbitals.

A single carbon atom has six electrons in its ground state with the configuration of $1s^2 2s^2 2p^2$, i.e., two electrons in a 1s orbital, another two in a 2s orbital, and the remaining two in two out of the three 2p orbitals ($2p_x$, $2p_y$ or $2p_z$) as shown in Fig. 2.1.2 (a). When carbon is in its elementary atomic form of $1s^2 2s^2 2p_x^1 2p_y^1 2p_z^0$, only two covalent bonds are available to form in the singly occupied p orbitals. However, if one of the doubly occupied 2s electrons excited (or promoted) into the empty $2p_z$ orbital, four singly occupied orbitals enable four covalent bonds. As a result, new hybridized orbitals with more stable bonds, σ bond or π bond, are obtained by a linear combination of atomic orbitals between the 2s and 2p orbitals (Fig. 2.1.2 (b)).

As shown in Fig. 2.1.2, after the electron excitation, there are three possible hybridizations from the combinations of orbitals, sp, sp^2, and sp^3, named after the number of participating p orbitals. For the sp hybridization, a 2s orbital hybridized with one out of the three 2p orbitals, resulting in two sp-hybrid orbitals with a bond angle of 180° in a linear arrangement. In the case of sp^2 hybridization, two p orbitals (assume to be $2p_x$ and $2p_y$) are mixed with the 2s orbital, leading to three sp^2 orbitals distributed in the xy-plane with a bond angle of 120° in a trigonal arrangement. The unhybridized $2p_z$ orbital is orthogonal to xy-plane of the new sp^2 orbitals. When all of the three p orbitals participate, sp^3 hybridization with four equivalent hybridized orbitals can be obtained with a bond angle of 109.5° in a three-dimensional tetrahedral construction. The combination of different types of hybridization leads to different chemical bonds between carbon atoms. For example, the combination of two hydrogen atoms and two sp hybridized carbon atoms results in ethyne (CH≡CH), which has one σ-bond and four π-bonds between the two carbon atoms. However, a similar case between two sp^2 hybridized carbon atoms will lead to ethene (CH_2=CH_2) with only two π-bonds, and so on, two sp^3 hybridized carbon atoms yield the molecule ethane (CH_3-CH_3) with σ-bond only. Therefore, hybridization has large impact on the molecules and consequently determines the properties of the materials.

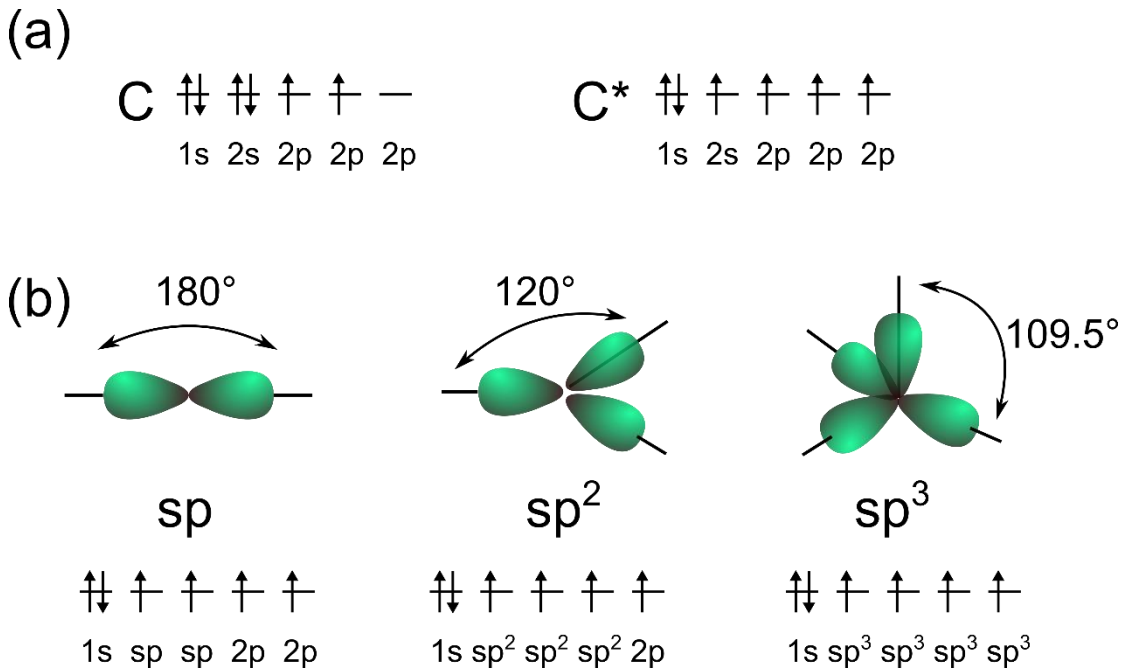


Figure 2.1.2: (a) The ground state and excitation state configurations of the carbon atom. (b) The sp, sp2, and sp3 hybridizations and the corresponding carbon configuration.

Among all types of hybridizations discussed above, sp^2 hybridizations as well as the bonds between the sp^2 hybrid orbitals are most important for organic semiconductors and thus will be further discussed in detail. The simplest case is ethene which has two threefold degenerate sp^2 orbitals in-plane and two $2p_z$ orbitals from the carbon atoms out-plane being perpendicular as shown schematically in Fig. 2.1.3 [31]. Since energy contributions from orbitals of different energy are small, we can simplify the stimulation of resulting molecular orbitals energy by only considering the mutual interaction of orbitals at equal or similar energy. Here, a covalent σ-bond is formed between two out of the six sp^2 orbitals along the internuclear axis, while σ-bonds are formed between the 1s orbitals that not shown here. Furthermore, π-bonds without rotational symmetry formed due to the interaction of the $2p_z$ orbitals. The bonding molecular orbital comes from the energetic splitting of two single orbital energy levels with different resonance interactions and leads to different attractive forces. For the 1s orbitals which are close to the core, the resulting bonding from σ orbital and anti-bonding from σ*-orbital has little splitting due to the negligible resonance interaction. However, since the principal quantum number of the carbon 1s orbital is one, it will be fully occupied by two electrons, leading to no participation in the covalent carbon-carbon band. For the sp^2 hybrid orbitals, due to a large amount of charge overlapping, they create a strong bonding σ and anti-bonding from σ* with a large resonance integral and thus a large energetic splitting. All three sp^2 hybrid orbitals from one carbon own one single electron for each orbital. Once they combine with the electron from either another sp^2 hybrid orbital in another carbon atom or the 1s orbital in the hydrogen atom, the new electron pair will fill the low-lying bonding σ and leave the high-lying anti-bonding σ* empty. Since the energetically lowest states will always be filled first, the low bonding states of the three σ orbitals will be filled right after the 1s orbitals. Finally for the p_z orbitals which are comparable far away from the nuclei, the interaction between them is weak, resulting in weak splitting between the bonding π and anti-bonding π*. Due to the smaller charge

overlapping π-bonds, in general, are much weaker than σ-bonds. As the third order of being filled by electrons, the bonding π orbital is the highest occupied molecular orbital (HOMO). The next higher orbital in ethene is the anti-bonding π* orbital, which is empty, referred as the lowest unoccupied molecular orbital (LUMO). The energy gap is then given by the energetic distance between the LUMO and the HOMO level as:

$$E_g = E_{LUMO} - E_{HOMO} \tag{2.1.1}$$

In organic semiconductors, electronic processes like charge injection from metal electrodes, light absorption, photon excitation, etc. decide the application of the materials. Because of the weaker splitting of π and π* orbitals, the moderate energy difference between the orbitals or relative to the typical electrode work functions enables various electronic processes. For example, the charge injection from electrodes is impossible due to the significant energy difference, and the optical transitions between the σ and σ* orbitals will be out of visible light range, requires much higher energy like UV light. Therefore, the energy levels of HOMO and LUMO are two important orbitals for organic semiconductor applications, and their energy levels need to be tuned for their applications.

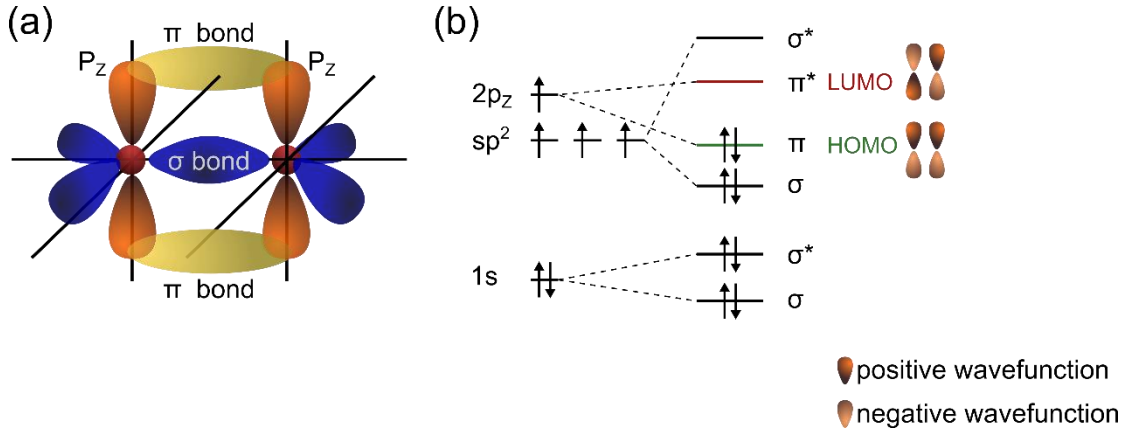


Figure 2.1.3: (a) Schematic of sp^2 hybridizations in ethene with σ and π orbitals. (b) Energy levels of the ethane.

Furthermore, electrons can delocalize in the HOMO and LUMO in a conjugated system with neighboring sp^2 hybrid orbitals sharing one π-bond, resulting delocalized π-system like benzene shown in Fig. 2.1.4 [32][33]. The electrons from the six p_z orbitals with π-system bonds in benzene are effectively delocalized over the conjugated system across the full benzene ring. Meanwhile, the six sp^2 hybrid orbitals are arranged in a planar hexagon with a larger network of carbon rings, forming σ bonds with either further carbon atoms or hydrogen atoms. Depending on the sign of six wavefunctions of the p_z orbitals, the symmetry or antisymmetric combinations will result in six molecular orbitals. Among these molecular orbitals, different numbers of nodes lead to different energy levels, which are presented by three bonding π_1, π_2, π_3 orbitals with lower energy and three anti-bonding π_4*, π_5*, π_6* orbitals with higher energy. The HOMO (π_2, π_3 orbitals) and LUMO (π_4*, π_5* orbitals) are illustrated in Fig. 2.1.4 (b).

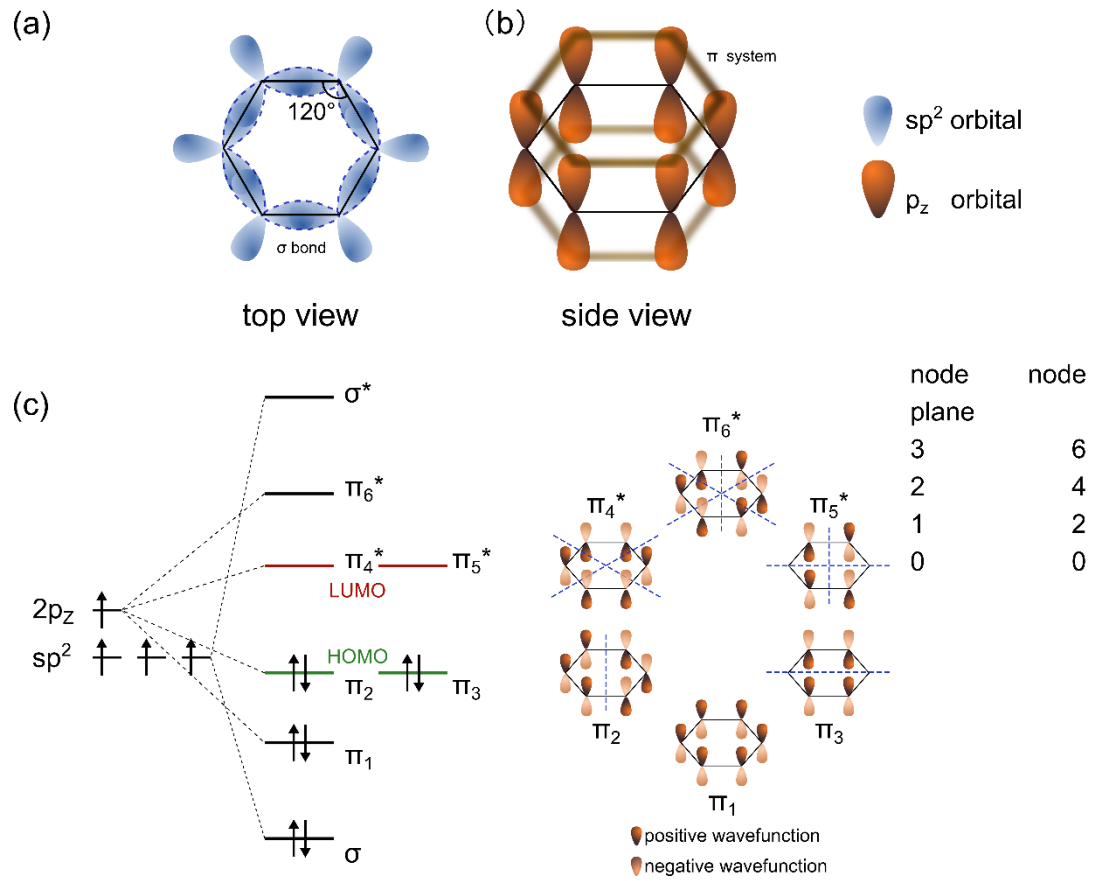


Figure 2.1.4: (a) Top view of sp^2 hybrid orbitals in a carbon ring configuration. (b) Side view of p_z orbitals and the delocalized ring-like π systems formed by π bonds at the above and bottom of p_z orbitals. (c) Energy levels of the benzene and graphical representation of the molecular orbitals with their node planes.

2.1.2 Solid states

In a solid state, atoms or molecules are held together by a attractive force (beside repulsive force) between them. The strong covalent bonds which are the common bonds between inorganic atoms, cannot exist in organic semiconductors since all electrons are already incorporated in bonding orbitals by hybridization so that molecules do not usually form any further covalent bonds. However, the charge distribution of organic molecules is not entirely rigid, implying that a temporary fluctuating dipole moment can be induced if there is a temporal fluctuation in the charge distribution in a molecule (e.g. a displacement of the delocalized π-system). This dipole will further induce a corresponding fluctuating dipole in the second molecule. The attractive force between the correlated dipoles is the van-der-Waals interaction, which will stabilize the dipoles and which forms the attractive force between them.

The van-der-Waals force strongly depends on the distance r between the molecules. When a temporary dipole moment p_1 is induced in one molecule, an associated electric field F will be formed by:

$$F \sim \frac{p_1}{r^3} \qquad (2.1.2)$$

while another fluctuating dipole in the second molecule will be induced by:

$$p_2 \sim \alpha \frac{p_1}{r^3} \tag{2.1.3}$$

where α is the polarizability of the second molecule which indicating the ability to induce dipole moments in charge distribution. Therefore, the potential energy associated with a van-der-Waals interaction is given by:

$$\mathrm{E} = -p_2 \cdot \mathrm{F} \sim -\alpha \frac{p_1^2}{r^6} \tag{2.1.4}$$

which decrease with the sixth power of the distance and it is part of the Lennard-Jones potential which describs the repulsive and attractive forces between two molecules [34]:

$$\mathrm{V(r)} = \mathrm{A}\frac{1}{r^{12}} - B\frac{1}{r^6} \tag{2.1.5}$$

where A and B are molecule specific coefficients. The nucleus will repel each other as they are all positively charged. The closer they get, the more repulsive the Coulomb interaction will be.

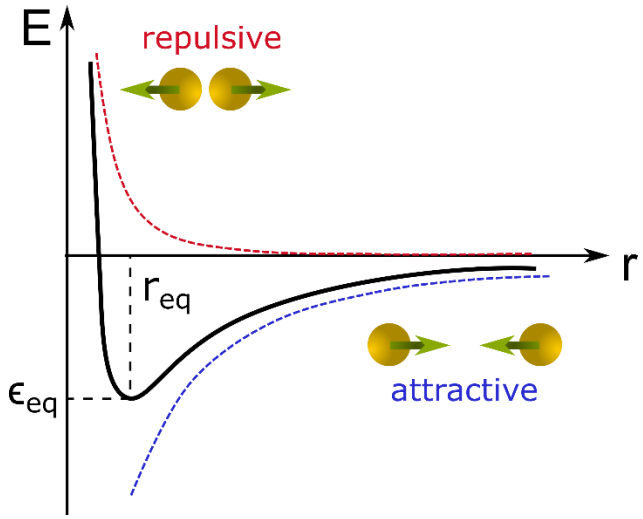


Figure 2.1.5: Schematic of Lennard-Jones potential, consisting of an attractive and a repulsive part.

As schematically shown n Fig. 2.1.5, with the increase of molecular distance r, the repulsive part decreases much faster than the attractive part and finally achieves an equilibrium state in a global energetic minimum. At the equilibrium state, the distance r_{eq} between two bounded molecules is defined when the net force is zero, and the depth of the potential presents the maximum binding energy ϵ_{eq} needed for breaking the bond. Since the typical binding energy is in the range of several 0.1 eV or smaller, similar to the thermal energy at room temperature (~0.25 eV), the bonds from the van-der-Waals force thus are really weak and can be broken thermally [35]. Furthermore, thermally induced energy fluctuations could already separate the two molecules if the k_BT (k_B is the Boltzmann's constant) is higher than binding energy ϵ_{eq}, resulting in a liquid or gaseous phase and thus a low melting point or sublimation temperature of the material.

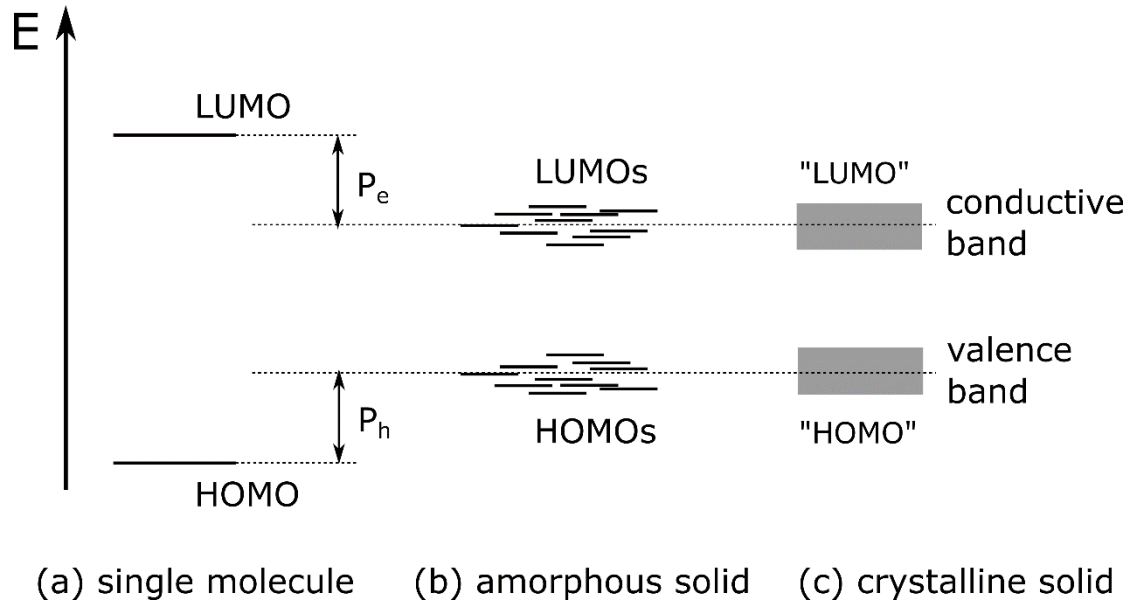


Figure 2.1.6: Comparison of the distribution of the energy levels HOMO (or valence band) and LUMO (or conductive band) in (a) a single molecule, (b) amorphous solid, and (c) crystalline solid.

Organic solids can be crystalline or amorphous. Due to the above discussed van-der-Waals forces between the organics molecules, most of them are not arranged perfectly in an amorphous solid. The molecule in the disorder solid state will polarize and redistributes charges with adjacent molecules for reaching an energetically favorable configuration. Therefore, the energy levels of the HOMO and LUMO in amorphous solid will shift due to the different interactions between neighboring molecules. As a consequence, the disorder arrangements of molecules from the local variations in polarization energy for electrons P_e and holes P_h will lead to a variety of different slight energy level shift as compared with a single molecule shown in Fig. 2.1.6 (b) [36].

In organic crystals, however, molecules have a regular arrangements, such as in anthracene or pentacene whose π-systems are mainly located above and underneath the molecular plane, resulting in close electron clouds and thus strong interaction. The regular arrangement of the molecules leads to the formation of electronic bands. Due to the polarization energy, the ionization potential decreases (by P_h) while the electron affinity is increased (by P_e), leaving a narrower bandgap in crystal as shown in Fig. 2.1.6 (c).

2.1.3 Singlet and triplet states

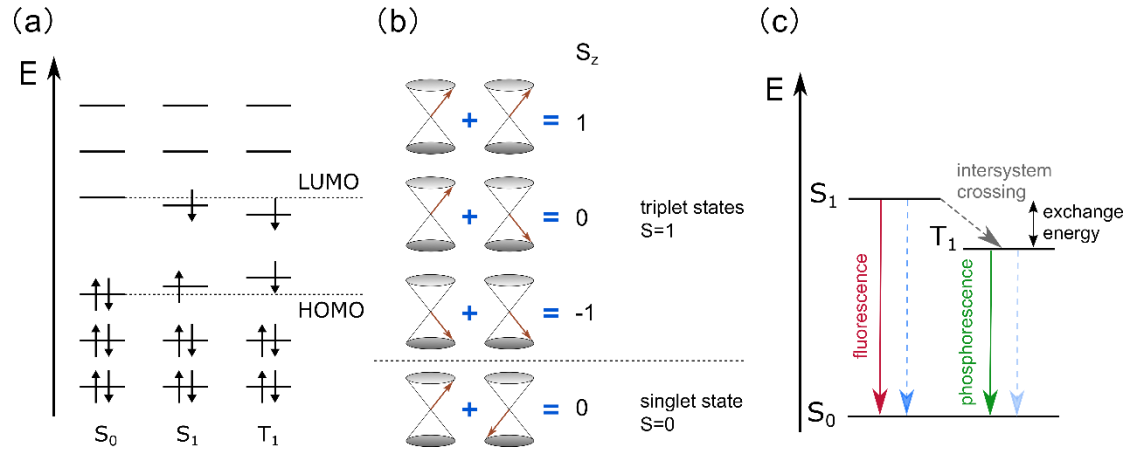


Figure 2.1.7: (a) Orbital configuration schematic of singlet and triplet states. (b) Vector diagram of four spin wavefunctions regarding the relative orientations of the two electron spins for the singlet and the triplet states. (c) State schematic of singlet and triplet states with radiative (fluorescence for singlet state and phosphorescence for triplet state) and non-radiative decays.

The spin of an electronic state of a molecule is given by the total spin of all electrons in all orbitals. As the Pauli exclusion principle states, it is impossible for two electrons in an atom to have the same four quantum numbers, which are the principal quantum number n, the Azimuthal quantum number ℓ, the magnetic quantum number m_ℓ, and the spin quantum number m_s. Therefore, the maximum two electrons that occupy the same orbital have to have opposite spin states, and are referred to as spin pairing. These paired electrons in filled orbitals contribute zero to the total spin and the state is singlet ground state (S_0). When there is an unpaired electron, a doublet state occurs that shows the splitting of spectral lines into a doublet. Further two unpaired electrons then result in triplet states. However, it is sufficient only to consider the concept of singlet and triplet states in this thesis since only these two states can be formed when one electron of the paired electrons is excited to a higher energy level [37]. In an excited state configuration, the unpaired electrons are usually one located in a π^* orbital and one in a π orbital. For the singlet excited state, the spin of electron in the π orbital is promoted in the same spin orientation as it was in the ground state, therefore being antiparallel to the remaining electron in the π orbital, adding up a total spin of zero. For the triplet excited state, the spin of electron in the π orbital has the same spin orientation (parallel) as the unpaired electron in the π^* orbital, resulting in a total spin of 1. As indicated in Fig. 2.1.7 (a), the excited states then can be referred to in energetic order as S_1, S_2 and so on for singlet excited state, or T_1, T_2, and so on for triplet excited state. The unpaired electrons in the excited state dominate the forming of a two-particle system, consisting of four eigenstates for description as illustrated in schematic in 2.1.7 (b). These eigenstates are listed in Tab. 2.1.1 [38]:

spin wavefunction	S	S_z
$\Psi_{spin,\ T+} = \alpha_1\alpha_2$	1	1
$\Psi_{spin,\ T0} = \frac{1}{\sqrt{2}}(\alpha_1\beta_2 + \beta_1\alpha_2)$	1	0
$\Psi_{spin,\ T-} = \beta_1\beta_2$	1	-1
$\Psi_{spin,\ S} = \frac{1}{\sqrt{2}}(\alpha_1\beta_2 - \beta_1\alpha_2)$	0	0

Table 2.1.1: The spin wavefunctions of the four eigenstates to the two-particle system with the yielding total spin and magnetic field in the z-direction.

Where the Ψ_{spin} is the spin wavefunction, and α or β denote the spin wavefunctions of the one-electron states with eigenvalues of s = 1/2, m_s = 1/2 or s = -1/2, m_s = -1/2, index 1 and 2 refer to electron 1 and 2, giving the eigenvalues S of total angular momentum to be 1, 0, and S_z of magnetic field in z-direction to be 1, 0, -1. The first three spin wavefunctions with a total spin of 1 are the arrangement for the triplet states, while the last spin wavefunction with a total spin of 0 refers to the singlet state. As shown in Fig. 2.1.7 (c), there is an exchange energy of several tenths of eV by which the energies between the first singlet (S_1) and triplet (T_1) state differ, and which scales exponentially with the overlap of the respective electron wavefunctions. Therefore, the more significantly HOMO and LUMO overlap, the larger the exchange energy will be. Due to the spin selection rule, the triplet state T_1 with lower energy level cannot be accessed by a direct electronic excitation from ground singlet state S_0 [39]. When the electron in the ground singlet state S_0 absorbs energy, it will excite to another singlet state S_1, and then follows several possible processes that occur between different states. If the excited state S_1 has a transition back to the S_0, it will have either radiative or non-radiative (quenching or relaxation) decay. The former case, referred to as fluorescence, will give off a photon which is invariably red-shifted, i.e., the wavelength is longer than the one that initially led to excitation. Nevertheless, the electron can also end up in the triplet excited state T_1 via intersystem crossing, subsequent either non-radiative relaxation or phosphorescence that electron drop back down to the S_0, accompanied by the emission of a photon.

2.2 Charge transport

2.2.1 Charge carrier mobility

Charge carriers will move once they are injected into the semiconductor and then driven by an electric field with a gradient in the electrostatic potential Φ. The contributions from drift and diffusion will sum up to a total current as:

$$j_{tot} = j_{drift} + j_{diffusion} \tag{2.2.1}$$

of which the drift current through the semiconductor can be given by the number *N* of charges *e* that flow per unit time *t* and unit area *A* as:

$$j_{drift} = \frac{eN}{At} = \frac{eN}{At}\frac{l}{l} = env_{drift} = en\mu F \tag{2.2.2}$$

where l is the unit length, n is the number density of charges, that is, the charge carrier contraction, and v_{drift} is the mean drift velocity that charges obtained from the electric field F. Therefore, the associated mobility of the charges can be gained from:

$$\overrightarrow{v_{drift}} = \mu\vec{F} \tag{2.2.3}$$

Under a gradient in the electrostatic potential, there is also a gradient in the charge carrier concentration that leads to an effective movement from the region with higher concentrations towards regions with a lower concentration. Therefore, the diffusion current can be gained by:

$$j_{diffusion} = -eD\frac{dn}{dx} = -\mathrm{eD}\nabla\mathrm{n} \tag{2.2.4}$$

where D is the diffusion coefficient. The final equation is the continuity equation (not shown), in which can be gained by using the Einstein relation between diffusivity D and mobility as:

$$eD = \mu k_B T \tag{2.2.5}$$

Based on the above discussion, the total current now can be sum up as:

$$j_{total} = en\mu\nabla\Phi - \mathrm{eD}\nabla\mathrm{n} \tag{2.2.6}$$

where the former part comes from the drift current and the latter part comes from the diffusion current. Which one dominates in the final current depends on the relative magnitude of the relevant gradients. In organic semiconductors, the charge concentration and its gradient are smaller (compared with that of inorganic semiconductors), and the current is thus usually dominated by drift. However, there are some exceptions like the condition of space charge limited current (SCLC).

2.2.2 Charge carrier transport

In the concept of orbital, the charge carrier transport is the process that an electron in the LUMO orbital transfer to the empty LUMO orbital, or a hole transfer between the HOMO orbitals equivalently. In order to have charge carrier transfer process, one necessary yet not sufficient condition is the electronic coupling among the sites in orbitals. At absolute zero temperature (T~0 K), an electron (or a hole) in a regularly ordered crystal will move coherently within a band of states. If the crystal is then in an electric field, the scattering process at the band edge drives the charge carrier to move at constant mobility. However, for a molecular with irregular structure, such perfect conditions will not be the case. Close to a certain temperature, lattice vibrations of phonons will lead to additional charge carrier scattering. If such scattering is weak compared with the overall electronic coupling between the adjacent molecules, the band transport model can be used for describing the charge transport, yielding an inverse temperature relation with charge carrier mobility. If the vibronic coupling of molecular becomes comparable to the electronic coupling at a high temperature, the charge carrier will scatter at each site which can be described by a hopping model with different temperature dependence of the charge carrier mobility [40].

Band transport As described above, band transport can be obtained in organic semiconductors that have a highly crystalline structure. In this case, the interaction energy is large than the energy

fluctuations from dynamic or static disorder, and charge carrier transport can be modeled by a band. The charge carriers are delocalized across the regularly arranged molecules that form a propagating Bloch wave which may be scattered by lattice vibrations [41]. As discussed above, compared to inorganic crystals where covalent interactions dominate, the electronic coupling is weak in organic molecular crystals. Furthermore, the bands of organic semiconductors will be narrow due to the van-der-Waals force between the molecules, leading the charge carriers behave as if having a larger effective mass m* which is determined by the electronic coupling. Therefore, the charge carrier mobility can be given by Drude model as:

$$\mu = \frac{e\tau}{m*} \tag{2.2.7}$$

where τ is the mean scattering time between collisions of the charge carriers. As the Eq. 2.2.7 indicates, a larger effective mass compared to the inorganic semiconductors results in a lower mobility, which can be easily understood by less efficient acceleration after a higher mass collisions with defects or phonons.

When band-like transport prevails, the scattering with defects, phonons, or electron-interactions will increase with the increase of temperature and results in lower mobility as the temperature dependence equation:

$$\mu \propto T^{-n}, \quad 0 < n < 3 \tag{2.2.8}$$

of which the ideal exponent n is 3/2 at room temperature. At low temperature (T<50 K) however, the relation will no longer be true since the mobility is saturated.

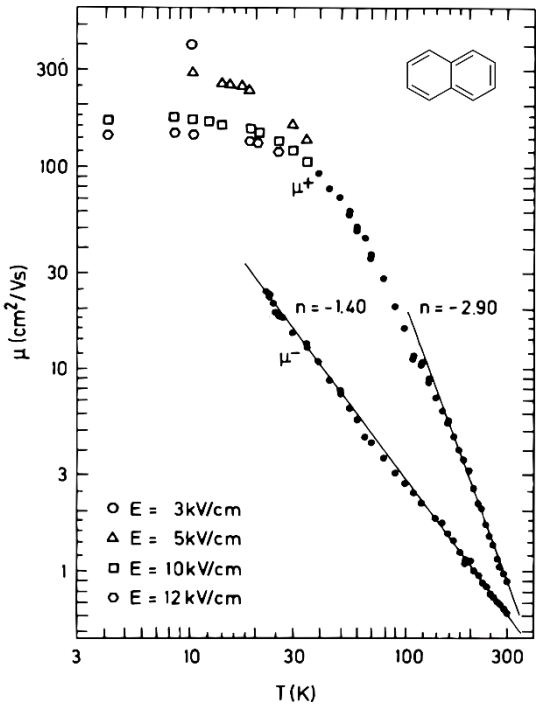


Figure 2.2.1: The temperature dependence of electron (n=2.90) and hole (n=1.40) mobilities in an ultrapure naphthalene with electric field applied parallel to the crystallographic *a* direction. (Figure is redrawn from [42])

An experimental example of proving the band-like transport in an organic molecular crystal was presented by Karl et. al by measuring the temperature dependence of charge carrier mobility in naphthalene crystal (Fig. 2.2.1) [42]. In a temperature range of 4 K to 300 K, both electron and hole mobilities were measured along the crystallographic *a* and *b* directions with different electric fields E. With the decrease in temperature, the mobility increases linearly in the double-logarithmic figure, revealing a temperature power-law with an n of 2.90 for hole transport and 1.40 for electron transport. When the temperature is below 30 K, the hole mobility reaches the saturation value and only shows the dependence on electric field.

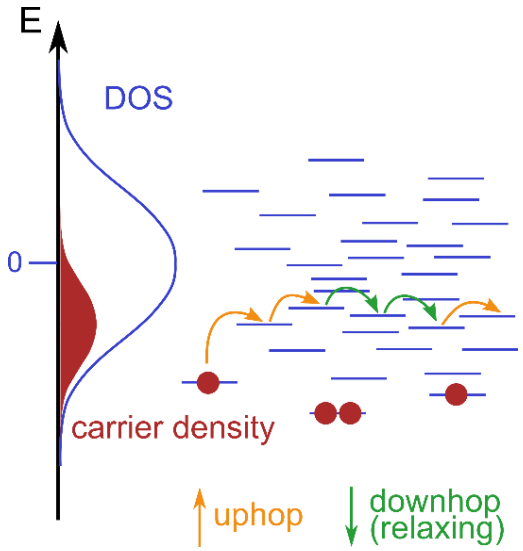


Figure 2.2.2: Schematic charge hopping transport in amorphous solids with a Gaussian DOS distribution. The orange arrows indicated the "uphop" where charge "jump" from low energy site to high energy site thermally, while the green arrows reveal the "downhop" where charge in the high energy site relaxes into the low energy site. The hopping process is only possible if the destination state is unoccupied.

Hopping transport In an amorphous organic semiconductor, regular arrangements of molecules no longer exist, and an energies spread, therefore, will come from dynamic or static disorder. If such energies are larger than the nearest neighbor interaction energy, the delocalized wavefunctions will be destroyed and thus band transport will not occur anymore. Herein, charge carriers are localized at individual states, i.e., the states in the HOMO and LUMO levels are distributed. The concept of incoherent hopping transport is applicable to this situation, as the carrier has to "hop" from its state (site *i*) into a nearby free state (site *j*) and then proceeds a sequence of non-coherent transfer. If the energy level of the destination site *j* is lower than the initial site *i*, the charge carrier can relax into the lower state site (green arrows in Fig. 2.2.2), which is preferred. Otherwise the carrier in the site *i* needs to be promoted with additional thermal energy in order to "jump" into site *j* which has higher energy (orange arrows in Fig. 2.2.2). This site to site carrier motion is a phonon-assisted tunneling mechanism, in which electrons tunneling through an energetic barrier involving lattice phonons whose energy facilitates the process [43][44]. The hopping rate (transition rate) ν_{ij} can be given by Miller-Abrahams rate as:

$$\nu_{ij} = \nu_0 \exp(-2\gamma r_{ij}) \begin{cases} \exp(-\frac{\Delta E_{ij}}{k_B T}) & \Delta Eij > 0 \text{ uphop} \\ 1 & \Delta Eij \leq 0 \text{ downhop} \end{cases} \quad (2.2.9)$$

where v_0 is the maximum hopping rate (attempt-to-escape frequency), and γ is the inverse localization radius that proportional to the transfer integral, ΔE_{ij} and r_{ij} are the energy and distance difference between the site *i* and *j* [45]. The transitions from lower energy site *i* to higher energy site *j* with energy difference $\Delta E_{ij} >> k_B T$ is unlikely, indicating that unlike the band transport, hopping transport at low temperature is either impossible or has small mobility. The mobility can be expressed with temperature dependence as:

$$\mu(T) = \mu_0 \cdot \exp(-\frac{T_0^2}{T^2}) \tag{2.2.10}$$

where μ_0 is the mobility with infinitely high temperature and T_0 is proportional to the width of the Gaussian DOS (density of states) [46]. For the hopping transport, the higher the temperature, the lower the mobility will be, which is opposite to the band transport.

When an external electric field is applied, the hopping transport is promoted since the electric field lowers the potential energy in the direction of the charge carrier drift. The probability of uphopping, where the carriers (electrons as the example) jump into energetically higher states, becomse higher since the electron gain additional energy of ca. $e|F|a$ (a is the mean distance of the molecule). Meanwhile, the number of "jumps" without the support from additional thermal energy is increased, indicating that the possible hopping sites increase. As a consequence, hopping mobility has field dependence as charges are transported more efficient with a higher electric field.

Furthermore, the charge carrier concentration also determines the mobility of hopping transport as partly indicated in Fig. 2.2.2. When the carrier concentration is low, meaning the numbers of electrons in the LUMO (or holes in the HOMO) is less, the charge transport will happen in the region where the energy of the states is low, and the density is small. Therefore, the spatial site distance r_{ij} as well as energetic difference ΔE_{ij} between two neighboring sites are large, resulting in a low hopping rate according to Eq. 2.2.9. When the carrier concentration is high, the low states are filled with charges preferentially, allowing the energetically higher free states to participate in the hopping transport. Following the Gaussian distribution, the transport energy is more close to the maximum value of DOS, leading to a smaller r_{ij} and ΔE_{ij} that increase the charge transport mobility.

It is worth to mention that although a one-dimensional schematic is shown for the hopping process, the three-dimensional space is the real model, where charge carriers can bypass the high energy sites by transporting through multiple low energy sites with larger total site distance.

2.3 Charge injection

2.3.1 Current limitation

Under the dark condition, the currents that flow through a device (i.e., through a optoelectronic device where a semiconductor is applied with metal contacts in various layouts like organic light-emitting diodes (OLEDs), organic solar cells (OSCs), organic field-effect transistors (OFETs), or organic non-volatile memories (ONVMs)) can be limited by either the efficiency of charge injection from the electrode, associated as injection limited current (ILC), or by the charge crowding, referred

to as space charge limited current (SCLC) [47-54]. In either case, the current density can be described by the drift current with the Eq. 2.2.2 discussed in Sec. 2.2.1.

Metal-semiconductor interface For maintaining a constant current flow in the device, charge carrier injection between the metal (electrode) and semiconductor is necessary and is limited by interrelated factors. If the current cannot meet SCLC conditions, which will be discussed later in this section, the current in the device is injection limited, i.e., the electrode cannot supply a sufficient number of charge carriers and the current is determined by these limited carriers. Otherwise the current will be limited as space charge limited current. Therefore, the ability of an electrode in sustaining SCLC conditions plays an important role in deciding the type of current limitations. Such ability, however, depends on both the injection barrier between the metal-semiconductor interface, and the charge carrier mobility of the organic semiconductor.

The simplified case for contact discussion is a metal-semiconductor-metal device shown in Fig. 2.3.1 (a) regardless of the band bending. The work function of both electrodes, Φ_{ano} for anode and Φ_{cat} for cathode, are gained by taking the Fermi energy with respect to the vacuum level E_{vac}. For ideal interfaces, the injection barrier for holes is given by the energy difference between the work function of the anode Φ_{ano} and the ionization potential E_{ip} of the semiconductor, while the electron injection barrier is the difference between the work function of the anode Φ_{cat} and electron affinity E_{ea} of the semiconductor. The built-in potential is then the difference between the two electrode work functions. Although there are some little correlations as well as different derivations, several theorems state that the ionization energy and electron affinity can be approximated as HOMO and LUMO energy, respectively [55]. The carrier injection can be improved or designed by semiconductor bandgap tuning, electrode selection. Furthermore, devices with different carrier types, like hole-only device (Fig. 2.3.1 (b)) or electron-only device (Fig. 2.3.1 (c)), can be fabricated by blocking one type of carriers injection [56]. The higher the mobility of charge carriers, the more crucial is the height of the injection barrier.

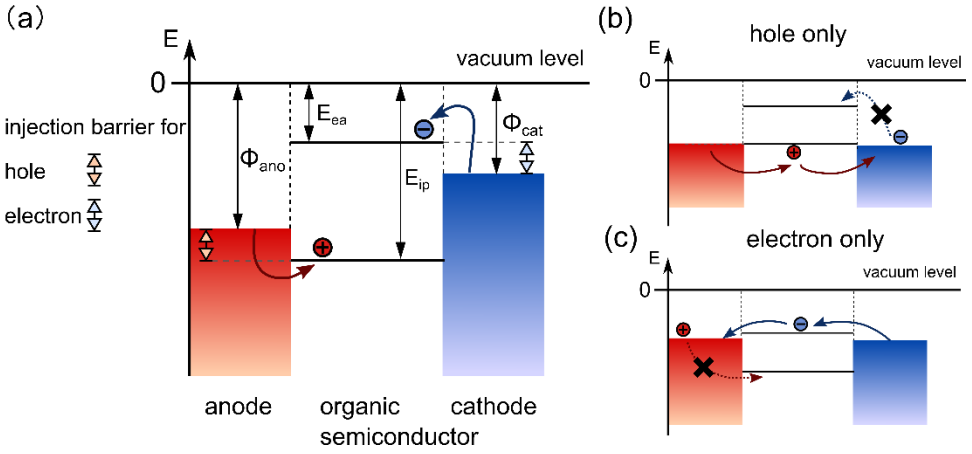


Figure 2.3.1: Energy diagram of the metal-semiconductor-metal device with (a) common alignment of energy levels, and (b) hole only transport or (c) electron only transport by tuning of electrode work function or semiconductor bandgap to prevent one type of carrier injection.

Injection limited current (ILC) When the injection barrier is large, the current flow is limited by the number of charges injected at the contact per time and per area. Here, the injection limited current

does not account for the subsequent carrier transport, and the associated injection rate for holes as an example can be given as:

$$\frac{dn_+}{dt} = G - k_{tr}n_+ - \gamma n_- n_+ \tag{2.3.1}$$

where G is the rate of hole injection per unit volume, and n_+, n_- are the hole and electron concentration, respectively. Also, γ is the rate constant for bimolecular recombination and k_{tr} is the rate constant for monomolecular decay which corresponds to the hole reciprocal transit time as $k_{tr} = 1/\tau_+$, of which further depends on the electric field F as:

$$\tau_+ = \frac{d}{\mu_+ F} \tag{2.3.2}$$

where d is the semiconductor thickness and μ_+ is the hole mobility. Here, the electric field is constant across the whole semiconductor as $\mathrm{F} = \mathrm{V}/\mathrm{d}$. Since only hole injection is considered in this case, i.e., the electron injection is comparable small, yielding that $k_{tr}n_+ \gg \gamma n_- n_+$, the hole concentration n_+ then can be calculated from the steady-state where $\mathrm{d}n_+/dt = 0$ to be $n_+ = G/k_{tr}$, which then, as mentioned above, can distort the drift current (Eq. 2.2.2) as:

$$\mathrm{j} = \mathrm{e}n_+\mu_+F = e\frac{G}{k_{tr}}F = e\frac{G}{\mu_+ F}d\mu_+F = eGd \tag{2.3.3}$$

The Gd yields the rate of hole injection per unit volume, referred to as g. Then the current can then be expressed as $\mathrm{j} = \mathrm{eg}$, which has dependence only on the injection rate. The injection limited current (ILC) can be extended to electron injection or injection from both electrodes following the same assumptions above, and the gained current has no relationship with either the electric field or temperature.

Space charge limited current (SCLC) When the injection barrier is small, meaning sufficient charge carriers injected from the electrode, the current will be limited by space charge region formed with unlimited injected carriers. Although the condition that the amount of injected charge is greater than the device's transport ability is conventionally associated with Ohmic contact, the current in SCLC case does not obey the predictions from Ohm's law that varies linearly with the electric field F. For a metal-semiconductor-metal architecture in which the semiconductor has a thickness d, capacitance per unit area C, and dielectric relative permittivity ε_r, the charge Q of this sandwich-type capacitor (consider the semiconductor as a dielectric layer) gained per unit area is $\mathrm{Q} = \mathrm{CV} = \varepsilon_0\varepsilon_r\frac{V}{d}$. Assuming that all gained charges will migrate from the injection electrode to the opposite electrode, the resulting current is $\mathrm{j} = \mathrm{Q}/\tau_{device}$ where τ_{device} is the time it takes the charges to travel through the device. Since the τ_{device} can be gained as $\tau_{device} = \frac{\mathrm{d}}{\mu\mathrm{F}} = \frac{d^2}{\mu V}$, yielding the current as $\mathrm{j} = \varepsilon_0\varepsilon_r\frac{\mu F^2}{d}$ which is clearly shows non-linear but quadratic relationship between the current and electric field. However, the current gained from this simplified calculation ignored the inhomogeneous of the electric field in the semiconductor (treated as dielectric layer), that is $\mathrm{F(x)} = \frac{3}{2}\frac{V}{d}\sqrt{\frac{x}{d}}$, and the corresponding charge concentration is $\mathrm{n(x)} = \frac{3\varepsilon_0\varepsilon_r V}{4ed^2}\sqrt{\frac{d}{x}}$ with an average value of

$n = \frac{3}{2}\varepsilon_0\varepsilon_r\frac{V}{ed^2}$ [29]. Therefore, a correction factor of *9/8* needs to be added according to the Mott-Gurney equation (Child's law) as [57]:

$$j = \frac{9}{8}\varepsilon_0\varepsilon_r\frac{\mu F^2}{d} = \frac{9}{8}\varepsilon_0\varepsilon_r\mu\frac{V^2}{d^3} \tag{2.3.4}$$

Herein, since both the charge carrier concentration (not proven here) as well as the electric field contribute with linear dependencies on the applied voltage, the overall linearity is destroyed. However, the linearity can reflect in the measurable linear current-voltage relation in the semiconductor characterizations.

Two current limitations described above set clear a limits to the injection ability, i.e., the metal-semiconductor contact has either negligible contact resistance or significant contact resistance. However, the contact resistance has an exponential voltage dependence in reality, indicating that with the decrease of the electric field, the reduction of contact resistance is much stronger than the reduction of semiconductor layer resistance. As a consequence, the same device has different injection limitations in different voltage regimes: at low voltage, an injection limited current (ILC) is present, whereas at high voltage, a space charge limited current (SCLC) dominates [58].

2.3.2 Charge injection mechanisms

The intrinsic conductivity of an undoped semiconductor is typically low, indicating that, in fact, the intrinsic semiconductor is an insulator. Unlike inorganic semiconductors, which have narrow bandgaps (e.g., crystalline silicon has bandgap value of 1.1 eV with an absorption edge of 1100 nm) and large relative dielectric constants (ε_r=11) to yield free electrons and holes with negligible Coulomb effects at room temperature, the bandgap of an intrinsic semiconductor is usually larger than 2 eV and the dielectric constant is as small as 3-4 [59]. Therefore, the excess charges generated by optical excitation have comparable large Coulomb attraction in between the hole and electron, resulting Coulomb-bound electron-hole pairs with non-negligible binding energy (normally 0.5-1.0 eV) instead of free charge carrier. Therefore, unless the semiconductor is doped (will be discussed in the following section), the free charge carriers have to be injected from electrodes [60]. To overcome the injection barrier mentioned above in Fig. 2.3.2, either tunneling or thermal activation is needed in principle.

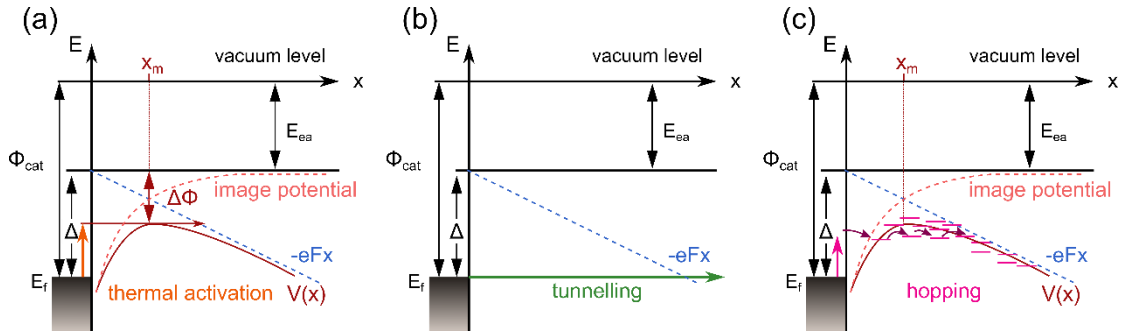


Figure 2.3.2: Schematic of electron injection from the electrode to the semiconductor via (a) Richardson-Schottky thermionic emission, (b) Fowler-Nordheim tunneling, i.e., filed emission, and (c) thermally activated

injection. Here, x is the distance from the electrode while the blue dash line (-eFx) donates potential energy due to the electric field F. Redraw from [29].

Richardson-Schottky thermionic injection Modeling the Schottky effect, or also known as field enhanced thermionic emission, by the Richardson equation gives the Richardson-Schottky thermionic injection, in which there is the image-force-induced lowering of the barrier potential for charge carrier injection in the presence of an external electric field. Considering electron injection, the potential barrier leaving for thermal excitation is the difference between the work function of cathode and electron affinity of semiconductor $\Delta = \emptyset_{cat} - E_{ea}$ as indicated in Fig. 2.3.2 (a) [61]. When an electron is at a distance *x* from the electrode, a positive image charge will then be induced on the electrode surface, creating attractive force (image force) toward the electrode. This image Coulomb force *K* is between the real electron at the distance *x* and its image charge at the distance -*x*, given by:

$$K = -\frac{e^2}{4\pi\varepsilon_0\varepsilon_r(2x)^2} = -\frac{e^2}{16\pi\varepsilon_0\varepsilon_r x^2} \tag{2.3.5}$$

and image potential Φ_{image} can be given as:

$$\emptyset_{image} = \int_{\infty}^{x} k dx = -\frac{e^2}{16\pi\varepsilon_0\varepsilon_r x} \tag{2.3.6}$$

shown as a light red dash line in Fig. 2.3.2 (a). When an external field F is applied, the true potential barrier which results from the superposition of the external and the image charge potential is smaller than the initial potential barrier, enabling the electrons being injected from the metal with sufficient thermal energy (Fig. 2.3.2 (a)). The total potential follows:

$$\mathrm{V(x)} = (\emptyset_{cat} - E_{ea}) + \emptyset_{image} - eFx \tag{2.3.7}$$

in which involves the potential barrier. By calculating the condition of $\mathrm{dV(x)/dx} = 0$, the minimum of the total potential can be gained at a certain distance $\mathrm{X_m}$ from the interface:

$$X_m = \sqrt{\frac{e}{16\pi\varepsilon_0\varepsilon_r F}} \tag{2.3.8}$$

at which distance the injection barrier is lowered maximum by ΔΦ:

$$\Delta\emptyset = \sqrt{\frac{eF}{4\pi\varepsilon_0\varepsilon_r}} = 2FX_m \tag{2.3.9}$$

And the injection current is predicted to be:

$$j_{RS} \propto T^2 \exp(-\frac{\Delta - \Delta\emptyset}{k_B T}) \tag{2.3.10}$$

with temperature dependence.

Herein, the inelastic scattering is ignored in the potential barrier for kicking out the possible recombination during the injection process, requiring a long intermolecular spacing and appropriate electric field (< 1 MV/cm) [62][63].

Fowler-Nordheim tunneling injection As mentioned before, the injection barrier between the electrode and semiconductor is identified with the work function of the metal. With the presence of a strong electric field (~1 MV/cm), electrons can tunnel from the Fermi level of the metal through a triangular barriers into the vacuum as a one-step tunneling process, also known as field emission (Fig. 2.3.2 (b)). Neglecting the Schottky effect, which will be introduced in the next chapter, Fowler and Nordheim predicted the injection current with the filed dependence as [64]:

$$j_{FN}(F) \cong F^2 \exp\left(-\frac{4\sqrt{2\mathrm{m} * \emptyset^3}}{3\hbar eF}\right) \tag{2.3.11}$$

where $\hbar$ is the reduced Planck constant. Such field emission is temperature-independent and yields a straight with a slope of proportional to Φ^3 when plotting $ln(j_{NF}/F^2)$ versus $1/F$. However, the Fowler-Nordheim equation ignores the image potential, which is then only applicable when the injection barrier is much higher than an image charge that the injection is into the vacuum, obviously not the case for intrinsic organic semiconductor. Furthermore, for getting rid of the inelastic scattering, electron in organic molecular semiconductor needs to tunnel the distance that is several times of the intermolecular spacing, making it impossible even for molecular crystals.

Thermally activated injection In a disordered organic semiconductor, the models of either Richardson-Schottky thermionic injection or Fowler-Nordheim tunneling injection have limited applicability since both of them are driven from a view to crystalline, inorganic semiconductors. Therefore, a model shown in Fig. 2.3.2 (c) is developed by considering the image charge at the electrode, the charge carrier hopping transport, and the energetic disorder in molecules comprehensively. As Gartstein and Conwell state, with an initial thermal activation, an electron at the Fermi level of the electrode can "jump" to the tail state of the density of states (DOS) distribution of transport sites of the organic semiconductor [65][59]. As long as there is a neighboring hopping site with lower energy, the injected carrier at the tail state cannot relax back to the initial site close to the metal, or recombines with its image charge in the electrode, but continue motions by hopping transport as discussed in Sec. 2.2.2.

2.4 Doping

To increase the number of free charge carriers as well as to improve the injection efficiency, introducing dopants that act as electron donors or acceptors in the organic semiconductor is a common way. By doing so, the conductivity of a semiconductor, which is the sum of hole (+) and electron (-) conductivity that comes from the product of respective charge carrier density and the mobility as $\sigma = n_+ e\mu_+ + n_- e\mu_-$, increases. Furthermore, the injection barrier is narrowed after doping, thus more charge carriers can be injected from the electrode and the injection current can be increased.

A simple doping mechanism is illustrated in Fig. 2.4.1 with simplified one-electron images. In the intrinsic organic semiconductor (matrix molecules) with filled HOMO and empty LUMO, it behaviors as the host which can either accept an electron or donate one, depends on the band energy levels of the dopant. For p-type doping, the LUMO level of p-dopants with high electron affinity is close to the HOMO of the host matrix molecules. Therefore, an electron from the filled HOMO of

the host can transfer to the empty LUMO of the dopant, creating a free hole in the host, increasing the hole density, and lowering the Fermi level towards the HOMO of the matrix molecules. The p-dopants in this case act as electron acceptors. Similar to the n-type doping with n-dopants that act as electron donors. Since the filled HOMO level of n-dopants is close to the empty LUMO of the matrix molecules, an electron can transfer to the LUMO of the host as a new free charge carrier in the organic semiconductor. The n-dopants are electron donors, leading to an increase of electron density and raising the Fermi level of the host toward its LUMO.

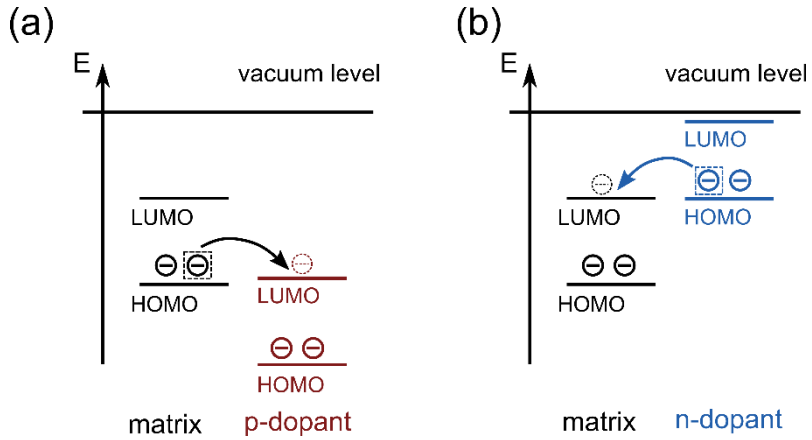


Figure 2.4.1: Schematic of the molecular orbital levels of organic molecules (matric) and dopants for (a) p-type doping and (b) n-type doping.

In this thesis, doping is achieved by co-evaporation of matrix molecules and dopant molecules at the same. The p-dopant is 2,2'-(perfluoronaphthalene-2,6-diylidene)dimalononitrile (F_6-TCNNQ) while the n-dopant is the alkali metal of Cs [66]. Both experimental and material details will be presented in Chapter 5.

Chapter 3

Organic junctions and devices

This chapter introduces the fundamental concepts of junction and related semiconductor devices in organic electronics, especially in organic light-emitting diode (OLED). Regarding the metal-semiconductor junction: a brief introduction of Ohmic contacts, ideal Schottky contacts, and Schottky contacts with surface states that result in Fermi level pinning is given in Sec. 3.1. Following that is a further investigation, in Sec. 3.2, about metal-oxide-semiconductor capacitor with three different operation conditions and corresponding different capacitance behaviors. Finally in Sec. 3.3, a discussion about p-n junctions, p-i-n junctions as well as OLEDs based on these two concepts is presented with their specific electrical properties.

3.1 Metal-semiconductor junction

As electrical metal-semiconductor junction is formed when the metal (electrode) makes contact with a semiconductor. Depending on the characteristics of the interface, the metal-semiconductor junction can behave either as an Ohmic contact or a Schottky junction barrier. Both of them have band bending near the interfacial energy levels, but in the opposite shifting directions [67]. For the Ohmic contact, with the injection of charges, the energy levels of the semiconductor molecules will shift to form space charge layer, which creates what is referred to as band bending. The Ohmic contact has strict requirements for the interface energy level (work function of the metal needs to be larger than the Fermi level of the p-type semiconductor, or smaller than the n-type semiconductor) that often requires doped organic semiconductors for organic systems. The Schottky junction is of importance, especially the accompanying barrier which is responsible for controlling the current as well as its capacitance behavior. Although a brief overview of the metal-semiconductor interface and the related different injection mechanisms has been given in Sec. 2.3, a more detailed discussion regarding the thermal equilibrium of Fermi levels and interface states will be held in this section.

3.1.1 Schottky junction

For the ideal Schottky junction without interface states and interface dipoles, the formation process can be illustrated as in Fig. 3.1.1 with an example of a metal with high work function Φ_m and an n-type semiconductor with conduction band energy E_C, valence band energy E_V, and Fermi energy E_F [68][69].

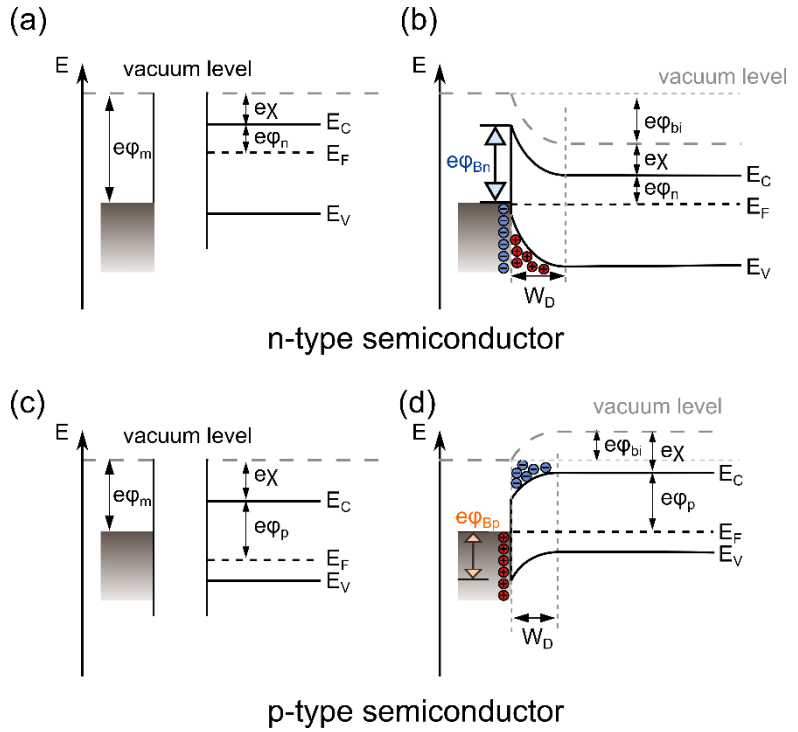


Figure 3.1.1: The formation of a Schottky junction with (a), (b) n-type semiconductor and (c), (d) p-type semiconductor. Partly redraw from [69].

Before the contact (Fig. 3.1.1 (a)), the metal has the work function $e\varphi_m$, while the semiconductor has the electron affinity of E_{ea} (= eχ), leaving the energy difference between E_c and Fermi level to be Δ_n (=$e\varphi_n$). The potential difference between the work function of the metal (φ_m) and the semiconductor ($\chi + \varphi_n$) is the contact potential. When the metal and the semiconductor are connected (Fig. 3.1.1 (b)), for example through an external wire connection, electrons will diffuse from the semiconductor into the metal until thermal equilibrium is established with the line up of both Fermi levels. Therefore, the Fermi level of the semiconductor is lowered by an amount equal the value of the contact potential. Since the metal then has excess electrons that are now missing in the semiconductor in the same amount, a positive charge region (holes) is formed at the interface in the semiconductor with a width of W_d, associated with a built-in field and a resulting built-in potential drop of φ_{bi}. This region is the depletion region which will be discussed later. As mentioned in Sec. 2.3.1, the barrier height is the difference between the work function of the metal and electron affinity of semiconductor, given by:

$$e\varphi_{Bn} = e(\varphi_m - \chi) \tag{3.1.1}$$

However, this simple expression normally cannot be realized experimentally due to the unavoidable interface states, dipoles, or image-force lowering introduced in Sec. 2.3.2. Furthermore, a similar but opposite charge region and band bending direction for Schottky junction with p-type semiconductor is simply shown in Fig. 3.1.1 (c) before contact and (d) with contact.

Depletion region When the Schottky junction is formed between the metal and the n-type semiconductor (as the example), the Fermi level of the semiconductor is far below the conduction band level due to the depletion region where there is lack of electrons (excess of equal positive charge). This difference will reduce with the distance from the junction until the n-type semiconductor returns back to charge-neutral condition with Δn (=eφn) as before contact was made.

The band change across the depletion region is the band bending for the Schottky junction. Since the energy relationship in the thermal equilibrium junction is defined, the width of depletion region W_d under an external applied voltage V can be gained by solving the Poisson equation [29][69]:

$$\frac{d^2\varphi}{dx^2} = -\frac{eN_d}{\varepsilon_0\varepsilon_r} \tag{3.1.2}$$

with the abrupt boundary condition (N_d is the charged impurities of donor), giving:

$$W_D = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{eN_d}(\varphi_{bi} - V - \frac{k_BT}{e})} \tag{3.1.3}$$

where the k_BT/e term arises from the majority-carrier contribution in addition to the impurity concentration N_D (here for the n-type semiconductor).

The space charge Q_{sc} per unit area of the semiconductor is:

$$Q_{sc} = eN_DW_D = \sqrt{2e\varepsilon_0\varepsilon_rN_D(\varphi_{bi} - V - \frac{k_BT}{e})} \tag{3.1.4}$$

and the capacitance of depletion region per unit area C_D can be written as:

$$\frac{1}{C_D^2} = (\frac{W_D}{\varepsilon_0\varepsilon_r})^2 = \frac{2(\varphi_{bi} - V - \frac{k_BT}{e})}{e\varepsilon_0\varepsilon_rN_D} \tag{3.1.5}$$

leading to a straight slope for extracting φ_{bi} and thus φ_{Bn} ($\varphi_{bi} = \varphi_{Bn} - \varphi_n$) by plotting $1/C_D^2$ versus voltage if N_D is constant throughout the depletion region.

Charge transport Although several injection mechanisms with different current models have been discussed in Sec. 2.3.2, the current conduction mechanism across a Schottky junction is generally governed by the thermionic emission model with image force, yielding [70]

$$\mathrm{j} = j_0(\exp\frac{\mathrm{eV}}{k_BT} - 1) \tag{3.1.6}$$

where j_0 is the saturation current.

3.1.2 Surface states

Surface states are electronic states at the atom layers closest to the surface of the semiconductor, resulting in different electron energy levels within the energy bandgap. If the surface states are considered in the Schottky junction and it is assumed that the atomic dimension interfacial layer between the metal and semiconductor is transparent to charges but can withstand potential across it, the energy band diagram of a Schottky junction can be illustrated as Fig. 3.1.2 with the n-type semiconductor as an example [69].

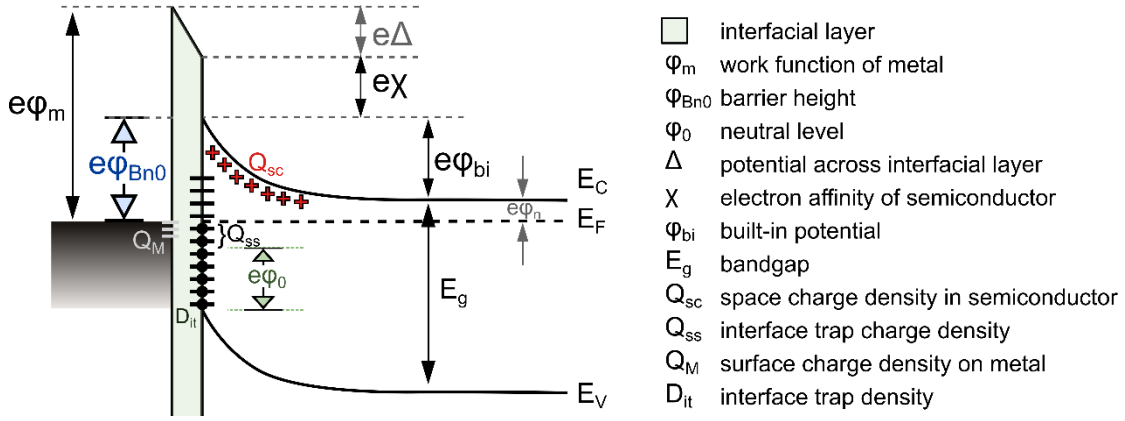


Figure 3.1.2: Energy band diagram of a Schottky junction of n-type semiconductor with surface states but without image force induced barrier lowering. Figure is redrawn from [69].

Neutral level The charge neutral level Φ_0 is a concept defined as an energy level above which the states are of acceptor-like trap states, i.e., the trap is charge-neutral when empty, and negatively charged when filled, and underneath which the states are of donor-like trap states, i.e., charge-neutral when filled, positively charged when empty. After the contact at the semiconductor surface, the neutral level may not coincide with the Fermi level at the semiconductor surface, leading to the interface trap charge. The position of the charge neutral level with respect to the bent valence band E_V is referred to as $e\varphi_0$. When the neutral level is lower than the Fermi level as shown in Fig. 3.1.2, the interface is negative charged, and the net charge of acceptor-like interface traps per unit area of the surface can be given by:

$$Q_{ss} = -eD_{it}(E_g - e\varphi_0 - e\varphi_{Bn0}) \tag{3.1.7}$$

where D_{it} is the constant interface trap density, E_g is the bandgap, and φ_{Bn0} is the new Schottky barrier. Due to the presence of the space charge Q_{sc} that forms in the depletion region of the semiconductor at thermal equilibrium (see Eq. 3.1.4), the total equivalent surface charge at the semiconductor surface is the sum up of both Q_{ss} and Q_{sc}, associated with an equal but opposite charge Q_M at the metal surface.

Fermi level pinning When the interface trap density D_{it} is large, the Schottky barrier height is independent of the metal work function, and totally decided by the surface properties of the semiconductor as:

$$e\varphi_{Bn0} = E_g - e\varphi_0 \tag{3.1.8}$$

so that the Fermi level of the semiconductor is pinned at the interface by the surface states value of eφ0. This is called Fermi level pinning effect [71]. The intensity of the pinning effect can be quantified by the pinning factor (S), ranging from 0 (complete pinning, Bardeen limit) to 1 (no pinning, Schottky limit) [72]. When there is no pinning effect, i.e., the interface trap density is negligible, the barrier height is equal to an ideal Schottky barrier without surface state as indicated in Eq. 3.1.1.

3.2 Metal-oxide-semiconductor capacitor

The structure of metal-oxide-semiconductor (MOS) is done by embedding an insulator, typically an oxide layer, between a conductor and a semiconductor. Based on the MOS structure, various electronic devices, like MOS diode, MOS field-effect transistor are fabricated and widely used in our daily life [73], [74]. The MOS structure, or MOS capacitor (due to its capacitive characteristics), is one of the most useful devices for studying semiconductor surface [75][76].

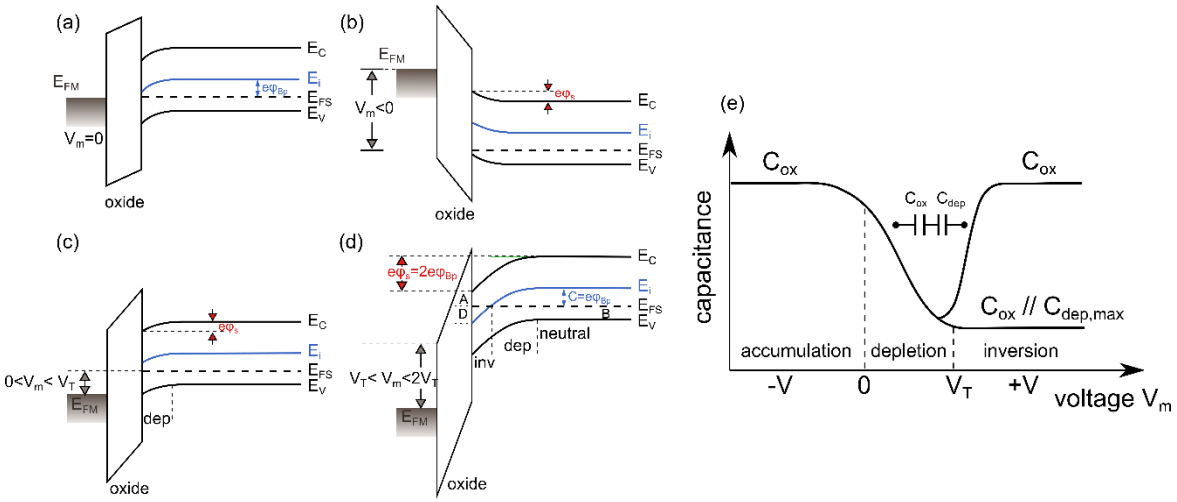


Figure 3.2.1: Schematic of energy band diagrams of MOS capacitors with p-type semiconductor under the condition of (a) no bias, (b) accumulation, (c) depletion, and (d) inversion. (e) Corresponding CV curves with high frequency and low frequency. Partly redraw from [69].

Considering the architecture of the device fabricated in this thesis, the MOS capacitor used as the explanation example in this section is based on a p-type semiconductor. When there is no bias applied to the MOS capacitor, the Fermi level of both, E_{FM} ($e\varphi_{fm}$) for metal and E_{FS} ($e\varphi_{fs}$) for semiconductor, are at the same energy level to keep the system in thermal equilibrium as shown in Fig. 3.2.1 (a). Therefore, depletion occurs as discussed in Sec 3.1.1 for the Schottky junction, associated with a built-in voltage and a potential drop over the insulator. The energy difference between the intrinsic level E_i (in the middle of E_C and E_V) and Fermi level of semiconductor E_{FS} is defined as φ_{Bp} .To achieve a flat-band condition where the energy band (E_c and E_v) of the semiconductor is flat at the interface of oxide layer, an external negative voltage needs to apply to the metal for biasing the capacitor. This flat-band voltage is the difference between the Fermi levels of two terminals as $V_{fb} = \varphi_{fm} - \varphi_{fs}$. The bias is always applied to the metal plate while the semiconductor is the potential reference here and throughout in this section. An ideal insulator layer blocks all current flows.

For negative voltage V_m larger than V_{fb}, the valence band edge is bent upward towards the surface, being more close to the semiconductor Fermi level with the potential of φ_s (Fig. 3.2.1 (b)). Since the energy difference between the Fermi level and valence band is smaller at the surface than in the bulk after band bending, the concentration of majority carriers (here holes) is higher near the semiconductor surface, forming an accumulation region. This is known as accumulation condition. When a small positive voltage is applied, the valence band is bent downwards as shown in Fig. 3.2.1

(c), and the condition turns to be depletion with a depletion region at the interface since both E_C and E_V are far away from the Fermi level that both electron and hole concentration is small. With the increase of applied positive voltage, the depletion regions become wider, until the concentration of electrons (minority carriers) is larger than that of the holes at the surface, inverting the surface from p-type to electron rich n-type. This condition is called inversion condition as shown in Fig. 3.2.1 (d). When this inversion condition is reached, any further applied voltage will drop over oxide layer, so the potential of φ_s, which determining the band bending, will be pinned. The threshold voltage (V_T) can be gained when the surface electron concentration n_s is equal to the bulk hole concentration N_a, i.e., A=B and thus C=D in the schematic that the intrinsic level E_i at the surface crosses over the semiconductor Fermi level. Therefore, the value of φ_s is equal to $2\varphi_{Bp}$. However, the inversion condition is critical in the simple MOS capacitor with a p-type semiconductor due to the lack of electrons in the semiconductor. It is more reliable in a MOS system with extra n-type junction (like in MOSFET) for electron supply [74]. Furthermore, it is worth to mention that in the ideal MOS structure there is no interface trap thus no interface trap charges at the semiconductor surface. Regardless of biasing conditions and resulting MOS capacitor conditions, the only charges that can exist in the capacitor are those at the semiconductor surface and the associated charges with equal but opposite sign at the metal surface.

The capacitance-voltage characteristic of the MOS capacitor is shown in Fig. 3.2.1 (e) with three regions and two possibilities. When the MOS capacitor is under the accumulation condition, the device capacitance raising from the oxide layer, showing as a plateau of C_{ox}. However, with the increase of the voltage, a depletion region appears and widens, acting as an extra depletion-layer capacitor with capacitance C_{dep} that is series connected with the oxide capacitor. The capacitance at the depletion condition can be given by:

$$C = \frac{C_{ox}C_{dep}}{C_{ox}+C_{dep}} \tag{3.2.1}$$

indicating a decrease of capacitance with the increase of voltage at the depletion condition. When the voltage achieves the threshold voltage V_T for the inversion condition, the depletion width is pinned to a maximum value with respect to the pinned φ_s, and the capacitance reaches the minimum value. With the continuous increase of voltage, the capacitance increases again as the inversion layer of electrons forms at the surface until reaches C_{ox} again. This is the case if the frequency is infinitely low for getting the response from inversion charges, referred to as low frequency CV. However, organic semiconductors, even doped one like p-type semiconductor, in this case, cannot supply electrons efficiently to keep up with the small-signal variation in AC measurement. The thermal generation for electrons in p-type semiconductors takes minutes, indicating an extremely small frequency and thus ineffective experimental study and has no practical significance [69]. Therefore, another case that is known as high frequency CV is more important and meaningful in reality. Since the width of the depletion region remains the same at the inversion condition, the device capacitance keeps at the minimum value as Eq. 3.2.1 suggests, resulting a low plateau at high positive voltage region.

3.3 Junctions and diodes

3.3.1 PN junction and diode

The structure of the p-n junction is of great importance in electronic applications like the p-n diode. However, its concept as well as the basic physics of its current-voltage characteristics are based on inorganic semiconductors [77]. The corresponding p-n junction in organic semiconductor in diode is that with low doping concentration, which is not preferable for applications and thus is not the device layout in this thesis. Nevertheless, for getting an understanding of this foundational junction, it is still briefly introduced with the diode application.

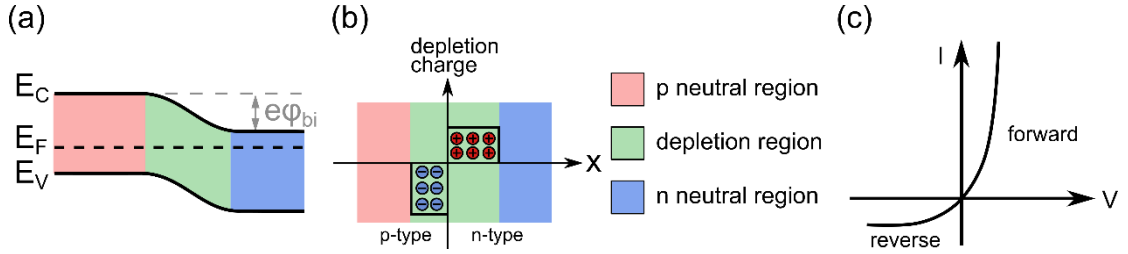


Figure 3.3.1: Schematic of (a) energy band diagram and (b) space charge distribution for an abrupt p-n junction in thermal equilibrium. (c) Ideal I-V characteristics of p-n junction based on Shockley equation.

Similar to the Schottky junction, when a p-type semiconductor is connected with a n-type semiconductor, a constant Fermi level is required throughout the junction in thermal thermal equilibrium. If the impurity concentration in the junction changes abruptly from acceptor impurities (p-type) to donor impurities (n-type), an abrupt junction is formed as shown by the typical Schottky-model in Fig. 3.3.1 (a) and (b). The electrons from n-type region can diffuse across the junction, combine with the holes, leave pocitive ions in the n-region, build up positive space charge and eventually create a depletion region that inhibits any further electron migration. The similar is true for the holes from p-type region. If a forward bias is applied to the p-n junction device, that is p-n diode, a further charge transfer and recombination can be promoted when the bias is higher than built-in potential. As a consequence, a current flow is observed with light emission.

The ideal current-voltage characteristics of p-n diode can be described by Shockley equation with the assumptions that: the p-n junction has abrupt boundaries, and semiconductor is neutral outside of the depletion region (space charge region); the carrier densities at the boundaries are related to the potential distribution; the injected minority carrier density is small compared with the majority-carrier density; there are neither generation nor recombination inside the depletion region, and electron and hole current densities are constant throughout the region. All these assumptions lead to [29]:

$$j(V) = j_o \left[\exp\left(\frac{qV}{k_B T}\right) - 1\right] \tag{3.3.1}$$

where q is the electric charge, and V is the applied voltage. The ideal curve is shown in Fig. 3.3.1 (c).

3.3.2 PIN junction and diode

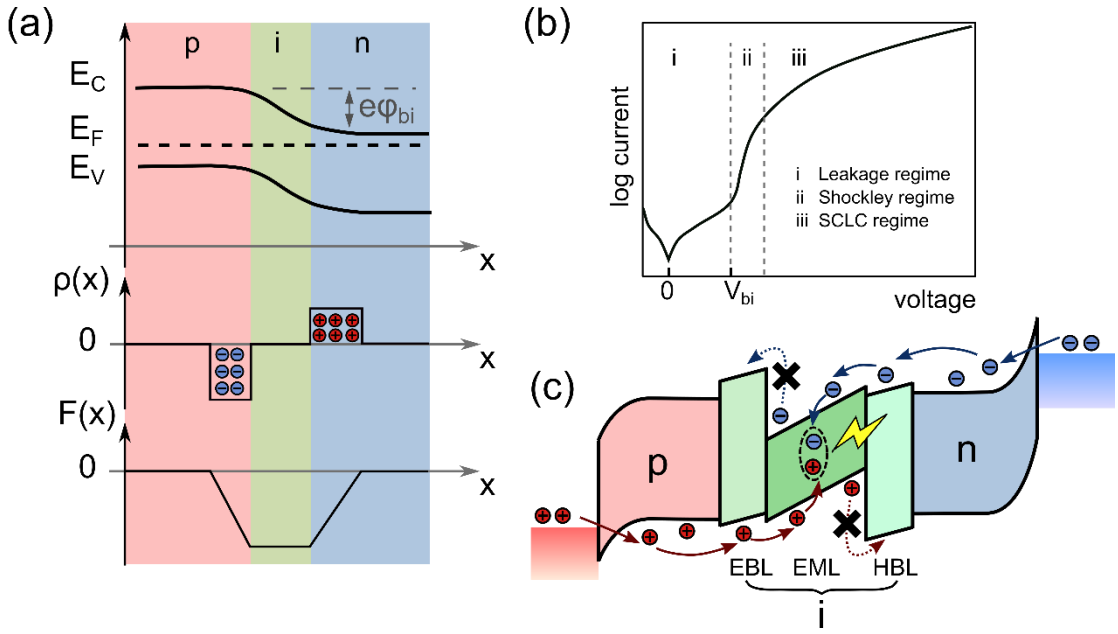


Figure 3.3.2: (a) Schematic of energy band diagram, space charge distribution, and electric field distribution for the abrupt p-i-n junction in thermal equilibrium. (b) Ideal I-V characteristics of the pin-OLED. (c) Schematic illustration of energy band diagram and carrier transfer process of a five-layer pin-diode with a forward bias. The architecture of the OLED is anode/ p-doped hole transport layer/ electron blocking layer (EBL)/ emission layer (EML)/ hole blocking layer (HBL)/ n-doped electron transport layer/ cathode. The intrinsic layers are composed of EBL/EML/HBL, in which blocking layers prevent charges from leaving the intrinsic layers without recombination.

To achieve an efficient charge injection between the organic semiconductor and metal, and thus better device operation in organic diodes, Ohmic contacts via tunneling injection are preferred to Schottky contacts. To achieve this, organic semiconductors are highly doped to have transport states that are close to the Fermi level of electrodes. Thus, the depletion region at the metal-semiconductor interface is extremely thin and charges can easily tunnel through the injection barrier (discussed in Sec. 2.3.2) to form a quasi-Ohmic contact [78]. Since junctions of highly doped p-and n-type organic layers do not produce well working diode, an intrinsic layer is sandwiched between the doped transport layers to obtain better control over the charge transfer and recombination. The structure of the result p-doped transport layer/ intrinsic layer(s)/ n-doped transport layer is called p-i-n junction as shown in Fig. 3.3.2 (a) with abrupt junction. The I-V characteristics of pin-OLED can be divided into three regimes as illustrated in Fig. 3.3.2 (b).

The pin-OLED is a rectifying device. When there is reverse or small bias ($V<V_{bi}$) is applied as marked as regime i, the charge carriers are driven away from the intrinsic layer, widening the depletion regions, and no current flow should be in principle observed. However, due to parasitical currents in the device, a small leakage current flow is often seen in reality, which follows Ohm's law.

When the forward bias is close to the built-in potential ($V\approx V_{bi}$ regime ii), charge carriers are driven towards the intrinsic layers and decrease the depletion layer width. The injected charge carriers can

migrate through the device, radiatively recombine within the intrinsic layer, and emit light. A five-layer layout pin-diode under forward bias is illustrated in Fig. 3.3.2 (c), where the intrinsic layers are composed of an emission layer (EML) and electron, hole blocking layers (EBL and HBL) that confine the charge carriers and excitons. An exponential slope of the I-V curve can be obtained in this regime that happens to be similar to Shockley behavior. However, violating the assumption in the ideal Shockley equation discussed in p-n junction, the recombination within the charge depletion regions or intrinsic layers is not negligible in the pin-diode. Therefore, an ideality factor η is introduced to describe the current behavior more reliable. Although it is not the exact equation, this modified Shockley equation represents an accurate description for most pin-OLEDs as:

$$j(V) = j_o \left[\exp\left(\frac{qV}{\eta k_B T}\right) - 1\right] \tag{3.3.2}$$

where η ranging from 1 to 2 for typical OLEDs [79].

For high electric field conditions, also called high injection conditions ($V>V_{bi}$, regime iii), electrons and holes are injected into the intrinsic layers in a quasi-ohmic manner, and then transport governed by drift across the intrinsic layers without recombination, and finally recombine once reaching the opposite side of the junction. The current is limited by the build-up of space charge as discussed as space charge limited current (SCLC) in Sec. 2.3.1, and the value can be given be Eq. 2.3.4.

Junction breakdown In a significant high reverse field, the p-i-n junction breaks down and conducts a large current flow [80]. Two breakdown mechanisms are normally discussed in organic diode: avalanche multiplication and Zener tunneling. The avalanche multiplication is caused by impact ionization by charge carriers of high kinetic energy, and its voltage is the upper limit of reverse bias. However, the avalanche breakdown is unlikely in organic semiconductors due to the small free path length of charge carriers. Nevertheless, Zener tunneling, which is a form of Fowler-Nordheim tunneling caused by band-to-band tunneling, is often observed in organic p-i-n junction. This interband tunneling effect, that has charge carriers tunneling from HOMO to LUMO states through a triangularly shaped barrier, is well used in organic electronics like field-effect transistor, diode, memory devices [81-84].

Chapter 4

Organic non-volatile memory devices

Organic non-volatile memory devices have been researched intensely and they could be among other application scenarios to play an important role in the vision of internet of things. In this chapter, the architecture, the working mechanisms, and the characteristics of memory devices in terms of organic materials are discussed. A fundamental concept and category of memory devices as well as their performance specifications are first introduced in Sec. 4.1. Following a detailed investigation about organic resistive memory devices in Sec. 4.2, organic transistor-based memory devices are discussed in Sec. 4.3, and organic ferroelectric memory devices in Sec. 4.4. In each section, memory devices are proposed with respect to materials, structures, fabrication, process mechanisms, and integrated matrix circuits.

4.1 Basic concepts

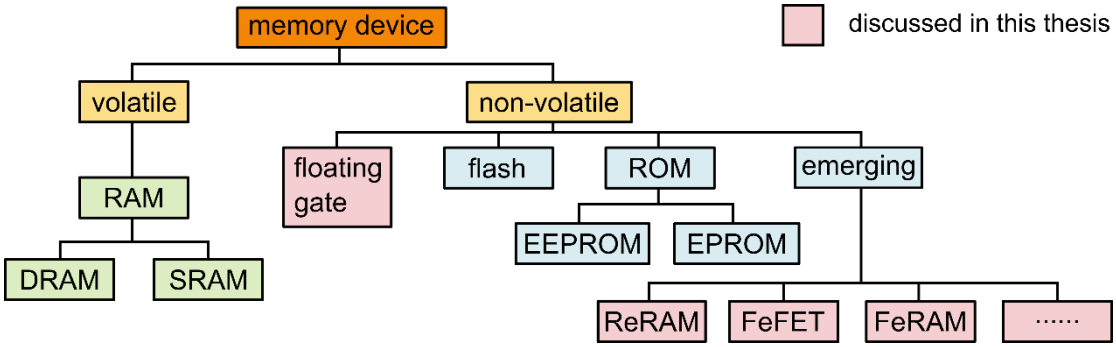


Figure 4.1.1: Flow chart for the semiconductor memory classification according to their functional criteria. Memories in pink frames are main discussing aspects of this thesis. Abbreviations: RAM: random access memory; DRAM: dynamic random access memory; SRAM: static random-access memory; ROM: read-only memory; EEPROM: electrically erasable read-only memory; EPPOM: electrically programmable read-only memory; ReRAM: resistive random access memory; FeFET: ferroelectric field-effect transistor; FeRAM: ferroelectric random access memory.

Organic memory devices are of significant importance in the modern information society as fundamental components of computers, electronic systems, and information stored systems by retaining retrievable digital data over a time interval [85][86]. There are huge economic, scientific and technological motivations to study as well develop organic memory devices. As classified in Fig. 4.1.1, the memory devices can be divided into two groups regarding the ability to maintain their

data/ states when the power is switched off: volatile memories that lose the information and non-volatile memories that last and can be read out nondestructively. Organic non-volatile memory (ONWM) devices will be discussed in detail as it is more attractive to organic semiconductors. Furthermore, the discussion is limited to devices with electrical rewritability like resistive random access memory (ReRAM) devices, floating gate memory, charge trapping memory, ferroelectric random access memory (FeRAM), ferroelectric field-effect transistor (FeFET) and so on [87-93]. The memories in pink frames in the classification flow chart (Fig. 4.1.1) are the ones discussed in this thesis.

For the concept of non-volatile memory, several parameters define the performance:

ON/OFF ratio or difference The ON/OFF ratio or difference is determined by the electronic state difference between the binary "1" on-state (stored-state) and binary "0" off-state (erased state). An improved density, or called multiple-bit storage, is also possible between state "1" and "0". In most cases, the binary units are physically represented by a high ("1") and a low ("0") resistance, i.e., high and low current density at the same voltage. Therefore, the ratio of resistance (R_{ON}/R_{OFF}) or current (I_{ON}/I_{OFF}) is defined as ON/OFF ratio. For different concepts of memory devices, the ratio can vary in a large range depending on different working mechanisms. For the same devices, although in some literature this ratio is only measured in a single cycle of a single device, the distribution ratio, in reality, requires a mean value measured over many devices for being sufficient and reliable.

Writing and erasing time The time consumed to program the memory to a sufficient ON/OFF ratio and then erase it back to initial state is the writing and erasing time, respectively. For most of organic memory devices, especially those based on measuring electrical resistance devices, the writing and erasing process is done via applying different (sign or site) external voltages for a certain time. Therefore, both time scales depends on the value of the switching voltage, or electric field for the same device.

Reading time The time required by circuitry to read the memory state out is the reading time. However, this parameter is usually not mentioned in literature since most of them measure organic memory devices by analyzer-connected probes instead of a readout circuit.

Retention time For the non-volatile memory, one important parameter is the ability to retain the stored data over time. If a device, that in its initial state has a significant ON/OFF ratio, is stored in a natural environment, the ON/OFF ratio at the same reading condition will fall over time due to various reasons like leakage currents, device degradation. Once the ON/OFF ratio falls below a critical value, the memory device cannot be read out and thus lose its data storing functionality. The time interval of reaching this critical value is the retention time for the device. After that, the device is either useless or need another data program process. Relying on the practical application, the demand for retention time can vary from seconds to a hundred years.

Cyclic endurance In a write-erase or write-read-erase-read cycle, the cyclic endurance is the strength of a device to allow being reprogrammed before its ON/OFF ratio falls below a certain

value. For a quantized value, the number of program cycles is defined and reported as cyclic endurance.

In general, a good device is referred to a device with large ON/OFF ratio, short writing, erasing, reading time, long retention time and high cyclic endurance. More factors, especially economic factors like power consumption and device cost are out of the discussion range in this thesis.

Active matrix systems Studies on the widely used resistive or FET-based memory are focused on investigating individual device architecture or involved organic materials. However, for a practical application that use integrated circuit arrays, problems can occur like crosstalk, half-select. Among them, the crosstalk effect can disturb the accurate read-out process of the addressed cell in crossbar array circuits by additional parasitic leakage paths (sneak paths) through neighboring cells with low resistances (or by any other excess currents). To eliminate this crosstalk effect, a switching element like rectifying diode or transistor can be added to each memory cell to compose the one diode-one resistor (1D-1R) or one transistor-one resistor (1T-1R) architectures. The read out then can be performed in the integrated memory arrays without disturbance [94]. In terms of structure, a 1D-1R cell is preferred due to its simple fabrication and less occupied area (4F2, whereas F is the minimum feature size) [95]. The active matrix system in organic memory devices was first demonstrated by combining an electrochromic conducting polymer with a switching element of silicon p-i-n diode into a single cell, and now is well accepted and used in real applications.

4.2 Organic resistive memory devices

Organic resistive memory devices contain active organic materials that possess at least two electrical, bistable, reversible states by applying external voltage. The incorporated active organic materials can be small molecules, polymers, and composites containing nanoparticles (NPs), of which molecular junctions in general sandwiched between a bottom and a top electrode. The conductance switching behavior, showing as the switching phenomena between low (OFF) and high (ON) currents in IV characteristics, has been reported for several molecular memory devices accompanied by electrical hysteresis and negative differential resistance (NDR). The physical understanding of switching behaviors is studied intensively and facilitated by state-of-the-art measurement techniques, although the origin of the operation mechanisms is unclear and diffed with different materials or device architectures [94].

4.2.1 Device architecture and switching behavior

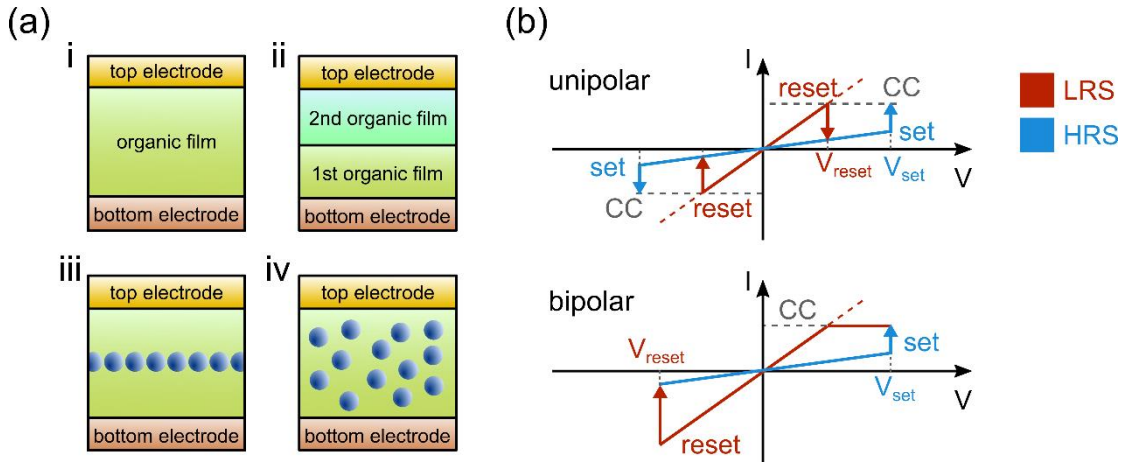


Figure 4.2.1: (a) Four typical architectures of organic resistive memory devices, redrawn from [94]. (b) Typical IV characteristics of organic resistive memory devices with unipolar and bipolar switching behaviors, CC is the compliance current to prevent permanent breakdown.

In general, this kind of two-terminal resistor-type memory called resistive random access memory (ReRAM), can be divided into four device architectures as shown in Fig. 4.2.1 (a): (i) a single-layer architecture that has a capacitor-like structure with a single organic layer without nanoparticles (NPs); (ii) a double-layer architecture that has two different types of polymers; (iii) a triple-layer architecture that has an embedded nano-trapping layer between two organic layers, with the nanotrapping layer containing nanomaterials as controllable charge traps, including nanoparticles (most discussed case), quantum dots, molecules or even 2D nanosheets; (iv) a complex layer that has organic (host matrix) -NPs blends in which nano-traps are randomly surrounded by the host matrix. Regardless of device architectures, the resistance of ReRAM devices can be switched back and forth between a low-resistance state (LRS) and a high-resistance state (HRS) by controlling the applied voltage. Although the exact resistance values at LRS and HRS fluctuate during multiple sweeps, the intrinsic difference is maintained between two states in magnitudes [96].

Two processes, the "set" process that device turns from HRS into LRS state and "reset" process that states inverse, can be observed in the voltage sweep loop with corresponding threshold voltages (V_{set} and V_{reset}) as indicated by IV curves in Fig. 4.2.1 (b) [97]. Depending on the relative polarity of V_{set} and V_{reset}, the IV curves with electrically reversible switching can be categorized into two classes: unipolar and bipolar switching memory. For the unipolar memory devices, there is a curve symmetry regarding the voltage sweep, demonstrating that a voltage sweep or pulse with same voltage polarity is sufficient for both writing and erasing ("set" and "reset") process in real device operation. Therefore, it has various technical advantages. In contrast, the bipolar memory devices require both voltage polarities, one for the "set" and another for the "reset" processes, respectively.

4.2.2 Working mechanisms

The conductivity is defined as the product of charge carrier concentration (N) and their mobility (μ), which can thoroughly describe different mechanisms in terms of change(s) of factor(s) changes

between On and OFF conductance states. Some potential conductance and transition mechanisms are discussed in this section based on well-established physical concepts like Ohmic contact, Schottky emission, tunneling effect, SCLC that introduced in previous chapters.

Filamentary conduction When the current flow in the ON state is limited to highly localized regions in a small fraction of the device area, a phenomenon of filamentary conduction occurs [98]. Two different types of filament bridge paths are widely suggested for ReRAM devices. One type is associated with the carbon-rich filaments formed by local degradation of organic films and then an increase in charge mobility. Another type is related to the metallic filaments resulting from local fusing or electrodes migrating that increases both charge carrier concentration and mobility [99][100].

The switching behavior in filamentary conduction is revealed in IV curve as threshold switching, i.e., there is a threshold voltage for showing memory behavior. With a sufficiently high electric field, an electrical breakdown occurs induced by a thermal runaway. The thermal runaway sites with residual conductivity lead to the local generation of Joule heat and thus increase temperature and current by forming a permanent localized structure [101]. This transient is the process from OFF to ON state. Two different kinds of filaments can occur, depending on electrode thickness, organic film thickness, and environment atmosphere. In an oxygen-free atmosphere like vacuum, the localized high temperatures at the thermal runaway sites result in pyrolysis (thermal decomposition) of the organic materials and the subsequent formation of conductive carbon-rich material as bridge filaments. The switching regime localizes at low voltage with threshold switching at 1 to 5 V. Alternatively in an oxygen-rich atmosphere, a local redox reaction happens at the thermal runaway sites. The organic film is oxidized while the penetrated metal electrode ions or nanometal clusters composited in polymer leads to structural modification and metallic filaments [102], [103]. The metallic filament formation process requires high voltage with threshold switching higher than 20 V. In order to bind to metal ions during the formation of metal filaments, π-conjugated Polymers with strongly coordinating heteroatom like P3HT, polypyrrole, PEDOT:PSS are good candidates [103-105].

Space charges and traps As discusses in Sec. 2.3.1, when the injection barrier between the electrode and organic layer is small and the organic layer is trap-free, the accumulation of charge carriers at the interface build up a space charge region and in turns limits the charge injection according to Eq. 2.3.4. Although traps, especially shallow traps locate at the interface reduce the carrier mobility, they also offering different charge injection currents at different voltages as well as enlarge the memory possibility by being filled and de-trapped [106]. For some conjugated polymer like P6OMe, the density of stored charges in the space charge region can be tuned by different voltage amplitudes [107]. The asymmetric nature of stored charges under the forward and reverse voltage sweep leads to hysteresis in IV curves. Besides this case, the voltage sweep itself can shift the injection mode from Schottky to Ohmic contact. With the increase of voltage, the electric field exceeds the initial small Schottky barrier and turns the metal-organic interface into Ohmic contact. Therefore, the unlimited charge carrier injection forms a space charge region with SCLC limitation. The process can be regarded as a current transformation from thermally generated free carriers to thermionic injection, and then towards Fowler-Nordheim tunneling. Furthermore, the generated

carriers can fill the trap, either intrinsic shallow traps or embedded nano-trapping sites, promising a trap-filled SCLC current with an abrupt enhancement [108][109]. In some cases, a double SCLC injection from both electrodes at high filed also promotes memory behavior [110].

Charge transfer (CT) effect In an electron donor (D)- acceptor (A) complex, charge transfer (CT) occurs as a transfer of a fraction of electronic charges from the donor to the acceptor moiety [111][112]. The electric-field-induced charge transfer effect in CT complex can tune resistive memory effects. Such resistive switching was first observed in Cu-tetracyanoquinodimethane (TCNQ), and then explored to various of organometallic like Li-TCNQ, or all-organic CT complexes like gold nanoparticles-polymer, fullerene- and CNT-polymer for RAAM [53], [111], [113-116]. An organic conductor can form from mixed donor-acceptor molecules by incomplete charge transfer [117].

Tunneling effect A temperature-independent Fowler-Nordheim (FN) tunneling happens through a triangular barrier when the electrode contact is ideal and the electric field is strong (Sec. 2.3.2). In some devices with thin insulator films (polymer, oxide), conduction mechanism changes to electron tunneling under a high applied voltage, resulting in a resistive memory behavior [118-120].

Conformation change Resistive switching and thus memory effect can also arise from electrically induced conformational changes in molecules or molecular bundles [121]. One of the typical examples is the device with Rose Bengal (RB) molecules that embedded in supramolecular matrices of polyelectrolytes [122]. If the RB film has appropriate packing density enabling molecular planes rotation, a conformational change occurs in the wide voltage sweep [123]. During the process of voltage sweep, there are different chemical structures of RB molecules that exist with different presented states. A reduced state, compared with neutral state, already formed at low voltage due to the bias-induced electro-reduction. However, only at high voltage that a further reduced state with conformational change can occur due to presence of two perpendicular planes, resulting in conductance switching in resistive memory device. Other organic system, like poly(2-(9H-carbazol-9-yl)ethyl methacrylate), poly(9-(2-((4-vinylbenzyl)oxy)ethyl)-9H-carbazole), acene-polymers are also reported for the conformation change induced conductance switching [124-127].

Ionic conduction Ionic conduction occurs in polymers containing ionic groups that can move under influence of an applied electric field [128]. Compared with electronic conduction, ionic conduction is characterized by its relatively high activation energy and long transit time. Through various ways, such as the migration of the dopant ions into and out of polymer matrix, slow drift of unscreened dopant ions at depletion region in Schottky contact, or control over ion concentration by electrochemical ion doping process, asymmetrical IV curves can be gained that shows conduction switching [129-131].

4.3 Organic transistor-based memory devices

4.3.1 Organic field-effect transistor and memory devices based thereon

The transistor is a three-terminal electronic device in which the third electrode can control the current flow in the path, which is referred to as channel, between the other two electrodes. The organic field-effect transistor (OFET) which employs an organic semiconductor layer as active channel is one of the most important devices as well as basic device structure in organic electronics. The three terminals of the OFET are source (S) and drain (D) for the charge injection, and gate (G) as the third, channel control electrode. The gate electrode is separated from the channel in the organic semiconductor by an insulating dielectric layer. The applied voltage on the gate electrode can introduce dielectric charge by the associated electric field, results in the formation of channel in the semiconductor at the semiconductor/dielectric interface and capacitively modification of the current flow from source to drain in the channel. The channel length L, which is the distance between the source and drain, and channel width W, which is the device architecture width, are two important parameters in determining the device performance. L is typically in the order of 100 μm while W is up to a few millimeters.

According to the geometries of contact electrodes and gate, there are four traditional planar architectures of OFETs: top gate, top contact OFET; top gate, bottom contact OFET; bottom gate, bottom contact OFET; and bottom gate, bottom contact OFET. The different geometries have different fabrication requirements, and will vary in the quality of the semiconductor/dielectric interface, as well as differ in the charge injection position. However, the working mechanisms are similar and will be discussed with the conventional bottom gate, bottom contact structure with p-type semiconductor as the example.

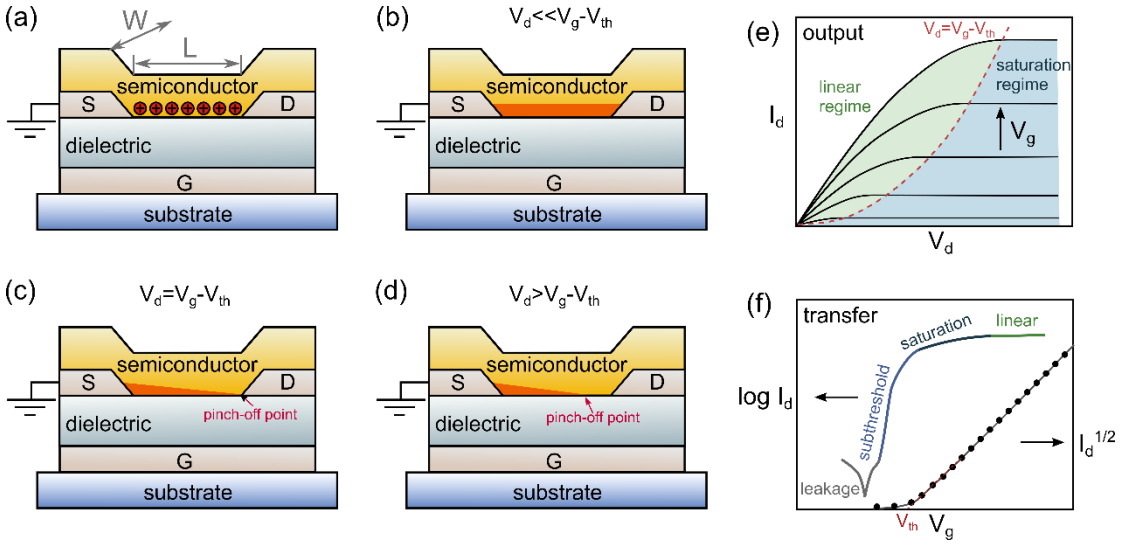


Figure 4.3.1: Schematic of the working mechanisms of a bottom gate, bottom contact OFET with p-type organic semiconductor at (a) applied Vg, (b) linear condition that V_d<<V_g-V_{th}, (c) start of saturation condition with pinch-off that V_d=V_g-V_{th}, and (d) saturation condition that V_d>V_g-V_{th}. The channel is colored in organic

and the pinch-off point is pointed by a pink arrow. The source electrode is grounded. (e) Output and (f) transfer characteristics of an OFET.

The contact between electrode and organic semiconductor is assumed to be an ideal Ohmic contact. The source electrode is grounded to be kept at zero potential. When a negative voltage is applied to the gate electrode while other two contact electrodes kept at zero as indicated by Fig. 4.3.1 (a), the electric field induced charge polarization results in the formation of a thin channel with positive charges in the interfacial semiconductor layer. Due to the presence of traps (and the energy band mismatch at the interface in non-ideal device), the gate voltage needs to exceed a threshold voltage V_{th} to obtain charge accumulation channel, Thus, the effective gate voltage is $V_g - V_{th}$. When a small negative drain voltage is applied ($V_d << V_g - V_{th}$) to the p-type transistor, mobile charges in the channel (shown in orange) contribute a current flow as revealed in Fig. 4.3.1 (b). The charge density per area at a given position *x* along the channel is proportional to the voltage difference as:

$$\mathrm{Q} = \mathrm{C_i}(V_g - V_{th} - V(x)) \tag{4.3.1}$$

where C_i is the capacitance of the insulating dielectric layer per unit area, and *V(x)* increases linearly from zero at the source electrode (x=0) to V_d at the drain electrode (x =L). with the condition of $V_d << V_g - V_{th}$, the gate field is much larger than the source-drain field as well as channel length is usually magnitude longer than dielectric layer. Therefore, the current I_d will obey Ohm's law with Eq. 2.2.2 and can be determined as:

$$I_d = \mathrm{WQ\mu}\frac{dV(x)}{dx} \tag{4.3.2}$$

and then be integrated with Eq. 4.3.1:

$$I_d \int_0^L dx = \mathrm{W\mu C_i} \int_0^{V_d} (V_g - V_{th} - V(x))dV \tag{4.3.3}$$

to yield:

$$I_d = \frac{W}{L}\mu C_i \left[(V_g - V_{th})V_d - \frac{1}{2}V_d^2\right] \tag{4.3.4}$$

in which the term of $V_d^2/2$ can be dropped with the limitation of $V_d << V_g - V_{th}$, achieving a current expression that I_d is increased linearly with V_d. Therefore, without the $\frac{1}{2}V_d^2$ term, the Eq. 4.3.4 is called linear equation and the current is in linear regime.

If V_d increases to reach $V_d = V_g - V_{th}$, the concentration of mobile charge carriers at drain is zero, and the channel becomes pinched-off (Fig. 4.3.1 (c)). The point where the potential is equal to $V_g - V_{th}$ for yielding zero mobile charge carriers is the pinch-off point. The region near the drain electrode is completely depleted of free carriers. A further increase of V_d push the pinch-off point moves slightly toward the source electrode, thus shorten the actual channel and leaving a narrow depletion region near the drain electrode (Fig. 4.3.1 (d)). The high electric field in the narrow depletion region pulls charge carriers across the narrow space charge region from pinch-off point to drain electrode. Therefore, there is still a current flow $I_{d,sat}$ which is dominated by the constant potential drop between the source and the pinch-off point. The current is now in the saturation regime. Replacing the V_d in Eq. 4.3.4 by $V_g - V_{th}$ gives the saturation current:

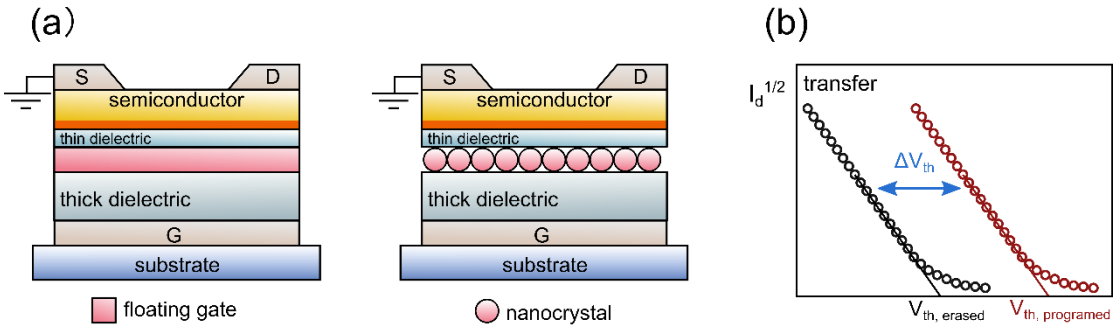
$$I_{d,sat} = \frac{W}{2L}\mu_{sat}C_i\left(V_g - V_{th}\right)^2 \tag{4.3.5}$$

According to it, plotting the $\sqrt{I_{d,sat}}$ as the function of V_g results in a straight line.

The output (in linear axes) and transfer (in semilogarithmic axes) characteristics of OFET are illustrated in Fig. 4.3.1 (e),(f).

Based on the working mechanism of OFET, an introducing of semipermanent charge storage opens the possibility of gaining non-volatile memory device. The transistor-base memory devices have two major groups: floating gate memory devices and the charge trapping memory devices, in which semipermanent charges can be stored in a floating gate or electret layer, respectively, and then shift the threshold voltage. A memory effect can be observed by hysteresis in the transfer curves.

4.3.2 Floating gate memory



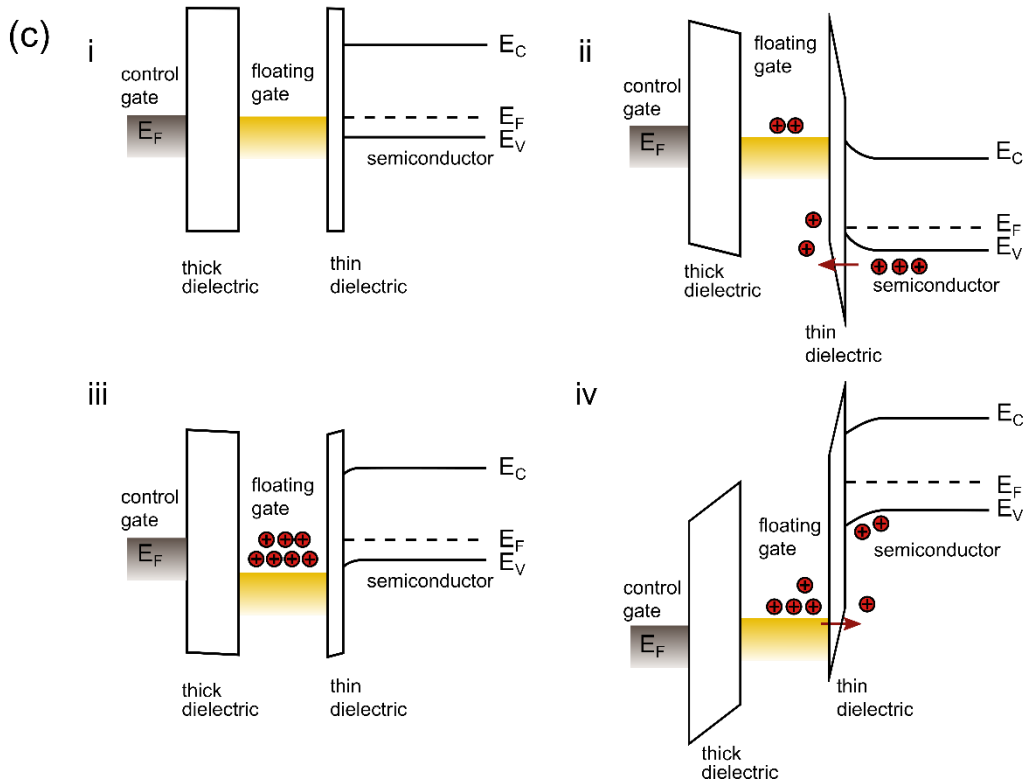


Figure 4.3.2: (a) Schematic of architectures of normal floating gate and nano floating gate. The channel is colored in orange. (b) Illustration of the shift of threshold voltage in transfer curves after programming and erasing. (c) Schematic of energy band diagrams of floating gate transistor memory device at different states: i. initial state; ii. programming by FN tunneling; iii. device at ON state with charged state; iv. erasing the stored charges at floating gate.

In the floating gate memory, charges are injected through a thin insulating layer and then stored in a conducting or semiconducting floating gate layer that is embedded in two insulating layers, resulting a shift of threshold voltage [132]. The architectures of the floating gate memory are referred to as metal-thick insulator-metal-thin insulator-semiconductor (MIMIS) structure in which the embedded floating gate metal layer can be either concrete-like polysilicon gate, or discrete like metal nanoparticles, nanocrystals (Fig. 4.3.2 (a)) [133-135]. The latter case is also referred to as nano floating gate memory devices. When the forward voltage is applied to the gate electrode, the thin insulating layer between the floating gate and the semiconductor produces a sufficiently high electric field to allow the injection of charges, yet prevents back- tunneling. The thickness of it needs to compromise between the voltage required to inject sufficient charges into the floating gate and the charge leakage from the floating gate, the latter setting an upper limit on the retention time [136]. The thick insulating layer between the floating gate and the gate electrode, however, prevents further injection and leakage currents. Thus, charges can be store in the floating gate and result in memory behavior. For widely investigated Si-based FET memory, there are several charge exchange mechanisms. Among them, hot-carrier injection, direct tunneling, and Fowler-Nordheim (FN) tunneling are three main programming mechanisms [137]. However, organic semiconductor suffers low carrier mobility so that the drift velocity of organic carriers in OFET is usually several orders of magnitude smaller than that in a silicon-based transistor. Therefore, the hot carrier mechanism is not applicable in OFET memory [17]. Furthermore, direct tunneling requires extremely thin insulating layer with several nanometers, which is not easy to achieve in most OFET memory devices [138]. Thus, the programming mechanism of OFET memory is usually dominated by FN tunneling. After programming, the total stored charge Q_{FG} corresponds directly to the threshold voltage shift of the device given by:

$$\Delta V_{th} = \frac{Q_{FG}}{C_{FG}} \tag{4.3.6}$$

where C_{FG} is capacitance of thick insulating layer between the control gate and the floating gate.

To discharge the floating gate, also called erasing process, a reversed voltage is applied to the control gate to remove the stored charges out of the floating gate. The erasing process is the reverse process of the tunneling discussed above. The full process memory behavior as well as the electrical characteristics are illustrated in Fig. 4.3.2 (b), (c).

4.3.3 Charge trapping memory

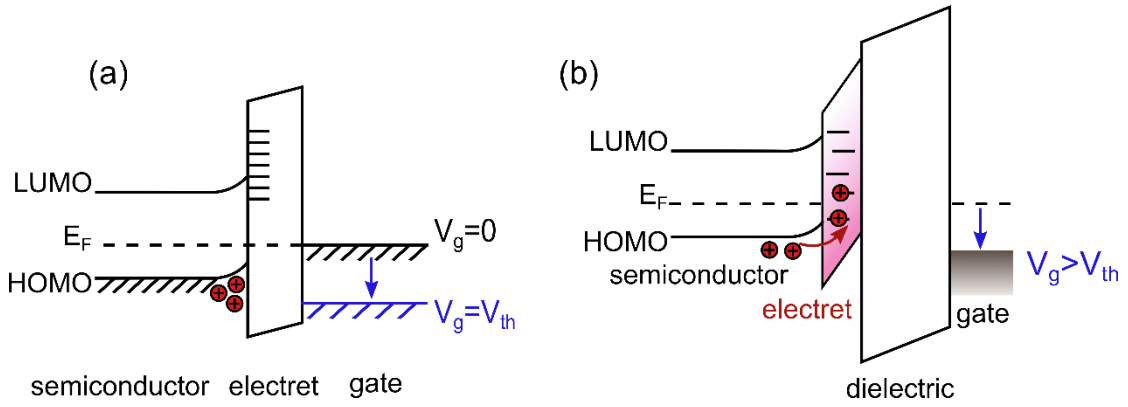


Figure 4.3.3: Schematic of charge trapping memory with (a) polarized gate, and (b) trapping electret gate for charge transfer and trapping. Redrawn from [139][140].

The charge trapping OFET memories store charges in an appropriate electret layer by trapping. The trapped charges can lead to memory behavior by either charge accumulation/depletion at the semiconductor/electret interface, or turning the electret layer itself into an additional gate electret (similar to floating gate but does not require another thin insulating layer).

For the former case, the memory effect is persistent but needs an assistant of pre-annealing after corona charging. One of typical architectures is: control gate/ polymer glass resin like poly(phenyl-methyl-silsesquioxane) (pPMSSQ) as polarized gate with trapped charges/ oligomer semiconductor like 5,5'-bis(4-hexylphenyl)-2,2'-bithiophene oligomer/ contact source and drain. As revealed in (Fig. 4.3.3 (a)), the electrostatic induction effects of charged electrets in the glass resin gate dielectric and the related controllable effective surface potential (of glass resin gate dielectrics) governing the charge accumulation or depletion mode at the OFET channel and thus shift the OFET transfer characteristics [139][141]. With the use of a grid-controlled charging and subsequently annealing process after the deposition of electret layer, the shifting of V_{th} can be modulated. However, this memory effect, although programmed by electrical corona charging, is electrically unrewritable and still lacks long-term circuit tuning due to the stability of stored charges.

Another class of charge trapping OFET memory is composed of gate/ insulating layer/ charge-trapping gate electret/ organic semiconductor/ contact source and drain. Unlike typically inorganic metal-nitride-oxide-silicon (MNOS) memory where charges tunnel and then are trapped in nitride, the injected charged can directly trap in the electret, of which behaviors as a floating gate discussed before [132][140][142]. By voltage application and/or light illumination, the potential barrier at the interface between organic semiconductor and gate electret is lowered, facilitating charge transfer and subsequently charge trapping, eventually showing a memory behavior by the shift in V_{th} (Fig. 4.3.3 (b)).

4.4 Organic ferroelectric memory devices

Ferroelectrics are polar materials in which the electric spontaneous polarization can be reversed or reoriented by an external electric field *E* [143]. In an electric displacement field *D* which is defined as

$$D \equiv \varepsilon_0 E + P \tag{4.4.1}$$

where *P* is polarization density and ε_0 is the vacuum permittivity, ferroelectrics are described by a non-linear relationship between *D* and *P* since the ferroelectric polarization *P* has a non-linear component. That is:

$$D = \varepsilon_0 \varepsilon_{0r} E + P_{ferro}(E) \tag{4.4.2}$$

where ε_r is the relative permittivity.

However, for the widely used dielectrics, the dielectric polarization *P* is proportional to the electric field *E*, thus only has the first term in Eq. 4.4.2.

The spontaneous polarization in ferroelectrics originates from the alignment of intrinsic dipole moments inside the ferroelectric material. By applying an external filed, the dipoles can be charged to have an up or down orientation according to the direction of the field, thus leading to a ferroelectric switching. However, due to the absence of the external applied field, the associated depolarization field can negate the ferroelectric polarization. Therefore, compensation charges at the surfaces are required for avoiding depolarization, which can be easily done by introducing conductive materials, i.e., electrodes, at both surfaces and connected.

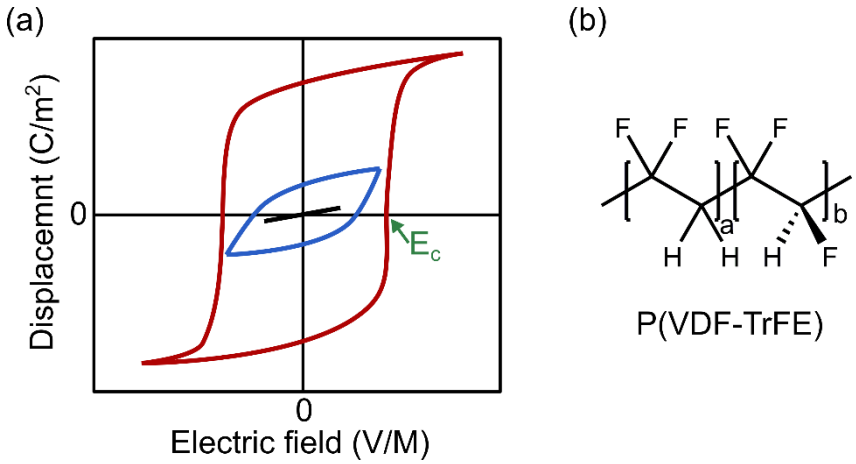


Figure 4.4.1: (a) Schematic of charge displacement D as the function of electric field E of ferroelectric memory. Redrawn from [144]. (b) Chemistry structure of organic ferroelectric material P(VDF-TrFE) copolymers.

The polarization property can be utilized as the memory effect. As illustrated in the schematic of electric displacement as a function of field strength (Fig. 4.4.1 (a)), there are filed strength dependent curves, some of which have hysteresis between opposite polarities [145]. The minimum electric field for ferroelectric switching is defined as the coercive field (E_c) in ferroelectrics. At low field where the field strength is not strong enough to affect the ferroelectric polarization, the curve in black shows a linear dielectric displacement. At higher field strength closer to the coercive field, the corresponding blue curve starts to show ferroelectric polarization. At sufficient high filed strength

presented by red curve, the memory behavior is clear and polarization reaches saturation at a critical field strength. The value of coercive field can be obtained from the intersections at x-axis under polarization saturation, while remanent polarization of the material can be observed by the intersections at y-axis [146]. The bistability in polarization states is referred to as state "1" and "0" in memory concept.

In particular, ferroelectric materials for memory devices are based on the capacitor, transistor, diode, or a mixture of them like 1T-1C (T-transistor, C-capacitor), enabling various possibilities including ferroelectric random access memory (FeRAM), ferroelectric field-effect transistors (FeFET) [147][148].

4.4.1 Ferroelectric capacitor memory

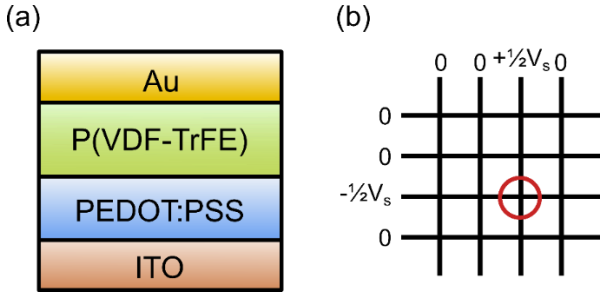


Figure 4.4.2: (a) Schematic of ferroelectric capacitor memory that employs PEDOT:PSS as bottom interface and P(VDF-TrFE) as organic ferroelectric material. (b) Matrix arrays in ferroelectric capacitor memory. The encircled cell is the one to be addressed.

As mentioned above, the property of ferroelectric materials is that maintaining electric switchable permanent polarization already promises a memory effect with bistability. Therefore, the simplest structure of non-volatile ferroelectric memory is the thin-film capacitor that stored the information by aligning the direction of the internal polarization either up or down with an external applied field, called ferroelectric capacitor memory. Reading out the information can be done by applying a constant sign of voltage and track whether or not the sign (direction) of polarization changes. Obviously, the read-out process is destructive since the stored information can be altered [149]. Therefore, a followed corresponding write operation (reset voltage) has to be applied for writing the bit back. Several disadvantages come along with the destructive read-out: the complexity in both read-out and writing process increases; higher cyclic endurance is required; the memory density per device is limited.

For organic ferroelectric materials, polymers are normally used including poly(vinylidene fluoride) (PVDF) and its copolymers with trifluoroethylene (TrFE), "odd" nylons, cyanopolymers, polyureas and polythioureas, and ferroelectric liquid-crystalline (FLC) polymers [150]. Among all of them, the P(VDF-TrFE) copolymers have been widely used due to their large spontaneous polarization, excellent polarization stability, low leakage level, short switching time, and no need for high-temperature process thus low fabrication cost [151-155]. The chemical structure of it is shown in Fig. 4.4.1 (b). Nevertheless, P(VDF-TrFE) copolymers have a relatively high coercive field of 50 MV/m, requiring a sub-100 nm thickness for achieving a low voltage switching (below 10 V), which

can be done by spin coating or Langmuir-Blodgett deposition technologies [156-161]. However, the remanent polarization and switching time get worse for thin film compare with bulk materials. To solve this problem, conductive polymer like PEDOT:PSS (poly(3,4-ethylenedioxythiophene):poly(styrene sulfonic acid)) shown in Fig. 4.4.2 (a), or Ppy:PSS (polypyrrole-poly(styrene sulfonic acid)) are comprised in the electrode stack as interfacial layers [162], [163].

Integrated ferroelectric capacitor memories Memory network with integrated multiple memory devices is essential for practical applications. However, arrays of ferroelectric capacitor memories in crossbar structure suffer from so-called "half-select" problem, especially for inorganic ferroelectric materials. As illustrated in Fig. 4.4.2 (b), for addressing one bit in the array, half the switching voltage ($+½V_s$) is applied to one row (word line) while another half the opposite switching voltage ($-½V_s$) is applied to one column (bit line). Ideally, only the selected bit is activated by the true switching voltage. Unfortunately, such activation field actually results in $½V_s$ half-select row/column occasionally being disturbed, or unintentionally switched, or selecting a neighboring bit on the same row/column as the addressed bit [145]. Therefore, data corruption, also called bit-error, can occur. This half-select disturb can be eliminated by using a transistor behind each ferroelectric memory cell for inorganic ferroelectric memory, or simply by using organic ferroelectric material P(VDF-TrFE) [164]. Compared to inorganic ferroelectrics, the relatively long switching time of P(VDF-TrFE) reduces or avoids the half-select problem as well as lessens the problem of destructive read-out [165-167]. The good performance of cross-point arrays of P(VDF-TrFE) ferroelectric capacitors enables it to be commercialized by Thin Film Electronics ASA (Norway).

4.4.2 Ferroelectric transistor memory

Employing charge displacement as the signal in ferroelectric capacitor memory not only suffers from destructive read-out, but also has the problem in device downscaling since the charge displacement response scales with the surface area of the capacitors [145]. Fabricating ferroelectric memory based on the field-effect transistor architecture can easily alleviate these problems. For ferroelectric field-effect transistors (FeFET), the gate dielectric in normal FET is replaced by a ferroelectric material, of which the ferroelectric polarization controls attenuation of the surface charge density in the semiconductor channel and thus guarantees memory functionality [168]. By applying a high gate voltage, the ferroelectric polarization can be aligned. When the polarization directions meet ON state, mobile charge carriers are accumulated in the channel associated with a source-drain current flow as discussed in Fig. 5.3.1 in normal FET [169]. When the opposite polarization directions meet OFF state, there are no channel accumulation charges and no source-drain current flow. The states can be read-out nondestructively by conductance states via low drain voltage that does not disturb the ferroelectric polarization. Furthermore, due to the presence (ON state) or absence (OFF state) of counter-charges, the ferroelectrics remain in the state after removing the gate voltage, which is, non-volatile memory behavior. Moreover, the FeFET cell can be scaled down without affecting the drain current read-out signal. Although, due to the limitation of thickness, the scaling is suggested to end at ca. 22 nm [169]. To obtain all-organic FeFET, polymer or small molecule semiconductors are

employed, for example: amorphous polymer MEH-PPV (poly(2-methoxy,5-(20-ethylhexyloxy)-p-phenylenevinylene) or rr-P3HT (regioregular poly(3-hexylthiophene)) or pentance with ferroelectric P(VDF-TrFE) [144], [170-172].

Integrated ferroelectric transistor memories As illustrated in Fig. 4.4.3 (a), FeFETs can be integrated into a memory circuit based on the single-cell layout. The switching is done by applying a voltage to the gate line GL, while information tracking is achieved by applying a small read voltage between two source-drain lines SDL 1 and SDL 2. However, the crosstalk effect and the half-select problem discussed above can occur in such FeFET arrays and disturb the information. Furthermore, the read-out process requires the supply of an additional gate voltage to non-addressed cells along the SDL line with the addressed cell to keep them off, introducing a potential polarization disturbing. To solve this problem, several active matrix layouts are proposed, as one of them is shown in Fig. 4.4.3 (b) where a one memory transistor is combined with one selection transistor [173][174]. For writing process, the select line SL is under voltage supply to turn the selection transistor on, subsequent an appropriate switching voltage on the gate line GL. For read-out process, a low voltage difference between SDL 1 and SDL 2 is applied while SL and GL kept grounded. By doing this, the non-addressed cells will not be disturbed anymore, and the read-out is nondestructive.

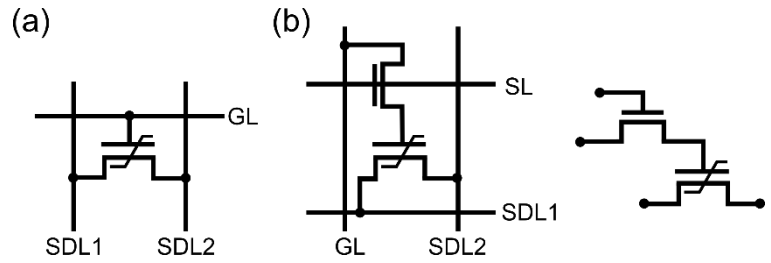


Figure 4.4.3: Schematic illustrations of single memory circuit with (a) one FeFET per cell, (b) one selection transistor and one FeFET per cell. Partly redrawn from [145].

4.4.3 Ferroelectric diode memory

The three-terminal FeFETs have elaborate device architecture that complicates the circuit layout for large integrated memory arrays. Compared to that, two-terminal ferroelectric capacitor takes advantages at a simple structure, but suffers from destructive read-out, half-select problem, and limited downscaling. Providing rectifying properties and resistive switching can alleviate these issues, i.e., ferroelectric diode [175].

The bistability arising from the modulation of the surface depletion width via ferroelectric polarization driven by electric field. The first reported ferroelectric Schottky diode was based on ferroelectric $PbTiO_3$ and employed Au as the electrode [176]. The memory behavior is achieved by shifting the device from Schottky contact with high resistance at one polarization direction that anti the built-in field, to almost Ohmic contact with small resistance at the opposite polarization direction. The resistance states can be readout by a low voltage that does not affect the ferroelectric polarization. For organic ferroelectric diode memory, polymer blends are widely used since the phase separation stem from their low enthalpy of mixing and small entropic gain enables a diode-like architecture. A blend of insulating ferroelectric polymer and semiconducting polymer leads to distinct ferroelectric

and semiconducting regions in one device. Thus, a conductance switching between a diode and a capacitor can be done by controlling the ferroelectric materials. One example of ferroelectric diodes is the device in which P3HT-enriched domains in a P(VDF-TrFE) matrix act as rectifying diode in a sandwich architecture between LiF/Al and silver electrodes [177]. A conductance switching between space charge limited and injection limited transport can be achieved by ferroelectric switching, where the polarization charges in the former case result in counter-charges accumulation and thus band bending that lowers the injection barrier.

Integrated ferroelectric diode memories Integrated ferroelectric diodes have advantages over FeFETs with simple two-terminal crossbar geometry. The half-select problem inside circuits can be suppressed by using the organic ferroelectric material P(VDF-TrFE) as mentioned above, but the crosstalk effect cannot be avoided. Reading out the logic state of a device is impossible due to the leakage paths provided from neighboring devices. For large arrays, the obtained resistance is equal to that of the addressed cell, parallel to the resistances of all cells in other word and bit lines. One solution is introducing an additional rectifying diode that connected with each memory cell in series to isolate it electrically. The high resistance in reverse direction in the diode prevents the leakage paths from neighboring cells, leading to an addressing with free of crosstalk effects.

Chapter 5

Experimental methods

In this chapter, the information about fabrication, device characterization, and involved materials are described in detail. The technical methods for device preparation are discussed in Sec. 5.1, including atomic layer deposition for creating insulating oxide layers, and thermal vapor evaporation for preparing standard OLED stacks. The technical details of sample characterization are subsequently introduced in Sec. 5.2 with regard to their application to organic light-emitting diodes (OLEDs) and organic non-volatile memories (ONVMs). Finally, materials which are incorporated in the organic devices are discussed in Sec. 5.3 based on their chemical structure and general electronic properties.

5.1 Device fabrication

Substrate and cleaning Borosilicate glass with four pre-structured finger-like indium tin oxide (ITO) electrodes (Corning Inc., Thin Film Devices, USA) are used as substrates for both diodes and memory devices in the thesis. All substrates are cleaned by a standard procedure: the pre-structured ITO stripes are first cleaned with acetone, then with ethanol by using a cotton tissue before the whole substrates are ultrasonicated with N-Methyl-2-pyrrolidone (NMP) for 15 min. Afterward samples were rinsed with deionized water for more than 5 min, followed by an ultrasonic bath in deionized water, ethanol for 10 min and 15 min, respectively. The samples are subsequently exposed to oxygen plasma for 10 min and finally stored in the nitrogen-filled glovebox.

Atomic layer deposition After the substrate cleaning, atomic layer deposition (ALD) is employed to fabricate a 50 nm insulating aluminum oxide (Al_2O_3) layer directly on the ITO pre-structured substate without shadow mask. The resulting insulator layer has a relative permittivity of 6.4 and high quality to block current flow under high voltage (~40 V). The sample prepared after the ALD process will be stored in the nitrogen-filled chamber before a further layer deposition, which is a standard OLED fabrication process for converting the as-prepared sample into an ONVM device.

Thermal vapor deposition Organic materials are deposited layerwise under high vacuum by thermal vapor deposition. Here one large ITO pre-structured substate with a 6 × 6 sample matrix is used as a single substrate, of which each sample has a size of 2.5 cm × 2.5 cm containing four individual devices. The thermal vapor deposition is done by a Lesker tool (Kurt J. Lesker Company, USA) with an ultra-high vacuum (UHV) of base pressure below 10^{-8} mbar as shown by a schematic in Fig. 5.1.1. It has 11 organic sources, 3 thermal sources for metal, and 1 Cs-dispenser. Each layer is structured by different shadow masks located next to the substrate, which will be discussed in details in the followings. Thickness control is available for each film using slit-wedge tools for the

inner 4 × 4 samples out of the 6 × 6 samples in one large substrate. During the deposition process, the unheated substrate remains at room temperature while the material is evaporated from the heated crucible and then moved towards the substrate. The molecules or metal atoms are subsequently deposited onto the substrate with a relatively low temperature and finally form a film. Both, the film thickness and the deposition rate, are monitored by a quartz crystal microbalance (QCM) which is positioned in a way that the material vapor deposits on it as well. The resonance frequency of the QCM will shift to lower frequencies proportionally to the additional mass of the deposited material. With the properties of the material, the film thickness with an accuracy of less than 1 Å and deposition rate with a unit of Å/s can be calculated. The deposition rate itself, by the way, is controlled by the temperature variation of the crucible which is measured by a thermocouple. Two shutters one for the sample (substrate), and one for the crucible— are set to control the deposition layer more preciously. The crucible shutter will not open until an appropriate deposition rate is achieved, and the sample shutter will close as soon as the film thickness is reached. For a doped film, a co-evaporation of molecules from two crucibles with independent temperature control is required [78][178][179]. Furthermore, two QCMs need to be placed in different positions to detect the deposition parameters of each material independently.

Since the film thickness and the deposition rate are calculated based on the material deposition onto the QCM but not the exact substrate, deviations will come from difference in position. Prior calibrations are then essential for eliminating the influence of the chamber geometry by either depositing the film on a reference QCM mounted in the substrate position or determining the thickness ratio between the real measured film and QCM. However, a small run-to-run deviation cannot be fully avoided.

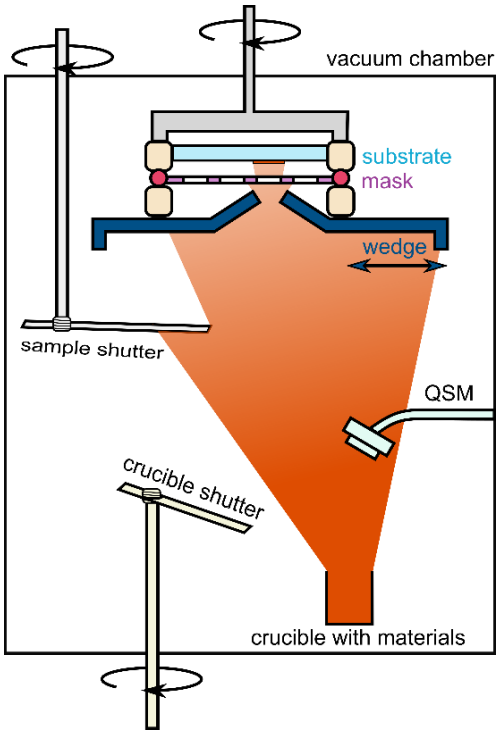


Figure 5.1.1: Schematic for thermal vapor deposition in ultra-high vacuum done by Lesker system.

Device encapsulation To prevent the degradation induced by moisture and oxygen under ambient condition, the finished organic samples are encapsulated with a glass lid and epoxy glue in a nitrogen-filled glove box (O_2 and H_2O < 1 ppm).

Device layout and shadow mask There are three different layouts used in this thesis, two for the OLEDs regarding the p-doped layer size and one for the memory device. As illustrated in Fig. 5.1.2 (a), the substrate of one sample has four individual pre-structured ITO electrodes with a width of 2.54 mm in order create four devices on each sample. For the memory device, an aluminum oxide layer is deposited on top of the substrate before a standard deposition of organic layers and a top electrode layer. The standard organic materials deposition contains a p-doped layer, three intrinsic layers (including an electron blocking layer, an emission layer, and a hole blocking layer), and an n-doped layer, successively. For the unstructured OLED device, all organic layers are fabricated using the same shadow mask with a long stripe of a length of 15.92 mm (Fig. 5.1.2 (b)). However, the doped layers are deposited separately in four small areas with a side length of 3.14 mm for structured OLED (Fig. 5.1.2 (c)), and 1.94 mm for memory device (Fig. 5.1.2 (d)). A top aluminum (Al) layer will be deposited as the top electrode using the shadow mask shown in Fig. 5.1.2 (e). Details on the different architectures for different devices will be discussed with further schematics in their respective chapters.

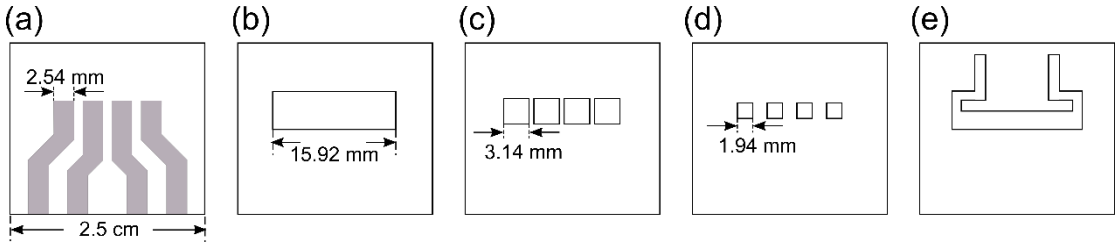


Figure 5.1.2: Schematic of (a) ITO pre-structured substrate, and shadow masks for (b-d) organic layers and (e) top electrode.

5.2 Device characterization

Current-voltage (IV) characteristics For electrical measurements of continuous currents, a high-resolution source-measuring unit (SMU) Keithley 2635 is employed with either steady-state or hold time mode. The steady-state mode limits the deviation between two consecutively measured currents before they are recorded, while the hold time mode keeps applying each set voltage for a specific hold time before the current is recorded. Both modes will be explained in details in Chapter. 6. Temperature-dependent IV measurement is performed in an SMU Keithley 2635 connected vacuum cryostat using a Peltier element controlled by BelektroniG GmbH. Another dual-channel source-measuring unit Keithley 2602A is used for measurements of internal device voltages by setting the input current value of 0 in the current mode and recording the voltage variation. All SMU characteristics are controlled by a home-built software "*SweepMe!*" (sweep-me.net).

Impedance spectroscopy For impedance spectroscopy, impedance spectrometers are used for doing the capacitance-voltage measurement, and the capacitance-frequency measurement. The one in the former case is an HP 4284 A Precision LCR meter from Hewlett Packard (USA) with a

frequency range from 20 Hz to 10^6 Hz, and is used with a modulation amplitude of 10 mV. The latter equipment is an Autolab PGSTAT302N from Metrohm Autolab (Netherlands) with a considerable large frequency range from 10^{-2} to 10^6 Hz since its signal is filtered by a lock-in amplifier. The signal amplitude is 200 mV for the sake of decreasing the noise in the temperature-dependent measurements, of which the equipment is described above. The method is based on complex impedance that has a frequency-dependent response on a small signal superimposed with a constant bias described as followings:

When a small alternative current (AC) voltage is applied to the bias voltage, the signal of the total voltage can be described mathematically as a function of time by:

$$v(\mathrm{t}) = v_0 + v_{peak}\sin(\omega t) \qquad (5.2.1)$$

where v_0 is the constant bias voltage, v_{peak} is the AC signal amplitude, and ω is the angular frequency. The response current has a phase given by:

$$i(\mathrm{t}) = i_0 + i_{peak}\sin(\omega t + \varphi) \qquad (5.2.2)$$

The phase shift angle φ by which the current lags the voltage is induced by the capacitance. For the AC circuit, the complex impedance Z can be represented by a real part (Re) and an imaginary part (Im) as shown in Fig. 5.2.1, in which each type of circuit element is characterized by its own impedance.

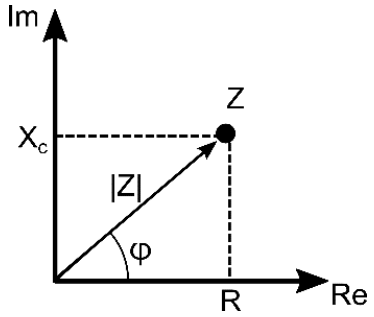


Figure 5.2.1: Schematic diagram of the complex impedance.

Since the current in a resistor R is governed by Ohm's law v = iR, the impedance of a resistor is its Ohmic resistance R. Combined with reactance X_c as imaginary part, Z then can be described by:

$$\mathrm{Z} = \mathrm{R} + \mathrm{j}X_c \qquad (5.2.3)$$

Furthermore, with the absolute impedance which is determined by the ratio between the amplitude of the voltage and the current signal as $|Z| = \frac{v_{peak}}{i_{peak}}$, the R and X_c can also be calculated as:

$$\mathrm{R} = |Z|\cos\varphi \; ; \; X_c = |Z|\sin\varphi \qquad (5.2.4)$$

In this thesis, circuits are RC circuits that are only composed of resistors and capacitors to give the complex impedance. From the definition of capacitance, we can get $\mathrm{v} = \frac{Q}{C}$ and hence $\frac{dv}{dt} = \frac{i}{C}$, the substitution of the complex voltage then yields $j\omega v = \frac{i}{C}$ ($j^2 \equiv -1$). Therefore, the impedance from the capacitance is $X_c = -\frac{1}{\omega C}$, and the capacitance of a single RC element can in turn be expressed as:

$$C = -\frac{X_c}{\omega |Z|^2} \tag{5.2.5}$$

In-situ emission measurements The set-up for the in-situ emission measurements driven by a pulsed voltage is shown by the schematic in Fig. 5.2.2. The low-voltage/high-frequency sine wave signal is generated by an arbitrary waveform generator 33600A from Keysight Technologies, which is then fed into a 50 times voltage amplifier before reaching the device as well as the DPO7354C digital phosphor oscilloscope from Tektronix for collecting electrical data. A camera and a photodiode are mounted on top of the device to obtain the emission images and device luminance, respectively. The photodiode voltage is further synchronized with an amplifier and subsequently connected to the computer for data recording. The pulse and the camera are controlled by the software of *SweepMe!*.

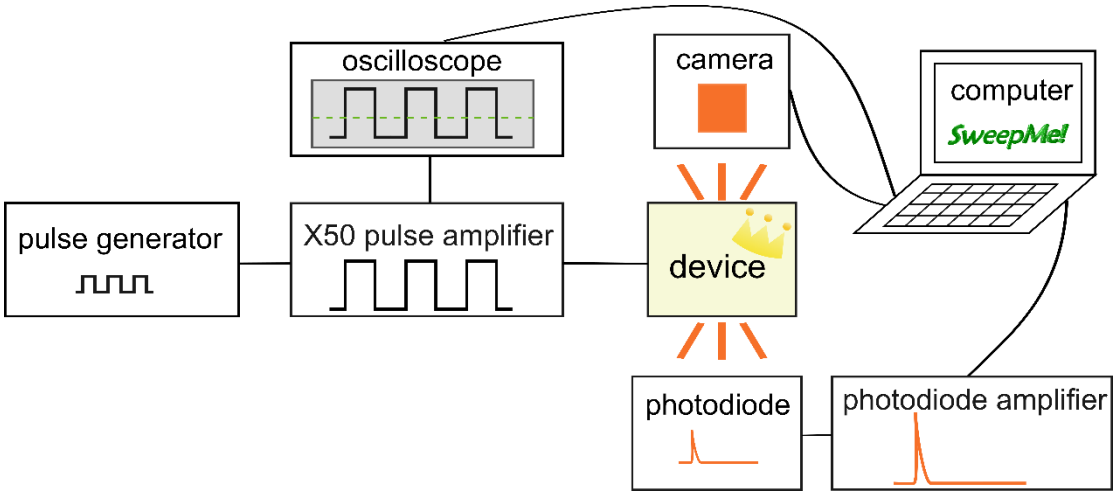


Figure 5.2.2: Schematic illustration of the In-situ emission measurements.

5.3 Materials

As mention in Sec. 5.2, ITO and Al work as the bottom electrode (anode) and the top electrode (cathode) with work functions of 5.0 eV and 4.28 eV, respectively [180]. Al_2O_3 with a 6.4 relative permittivity is used as the insulator layer in the memory device. With respect to the band energy, the functions of other small molecules, including dopant can be categorized into charge transport, charge blocking, and light emission.

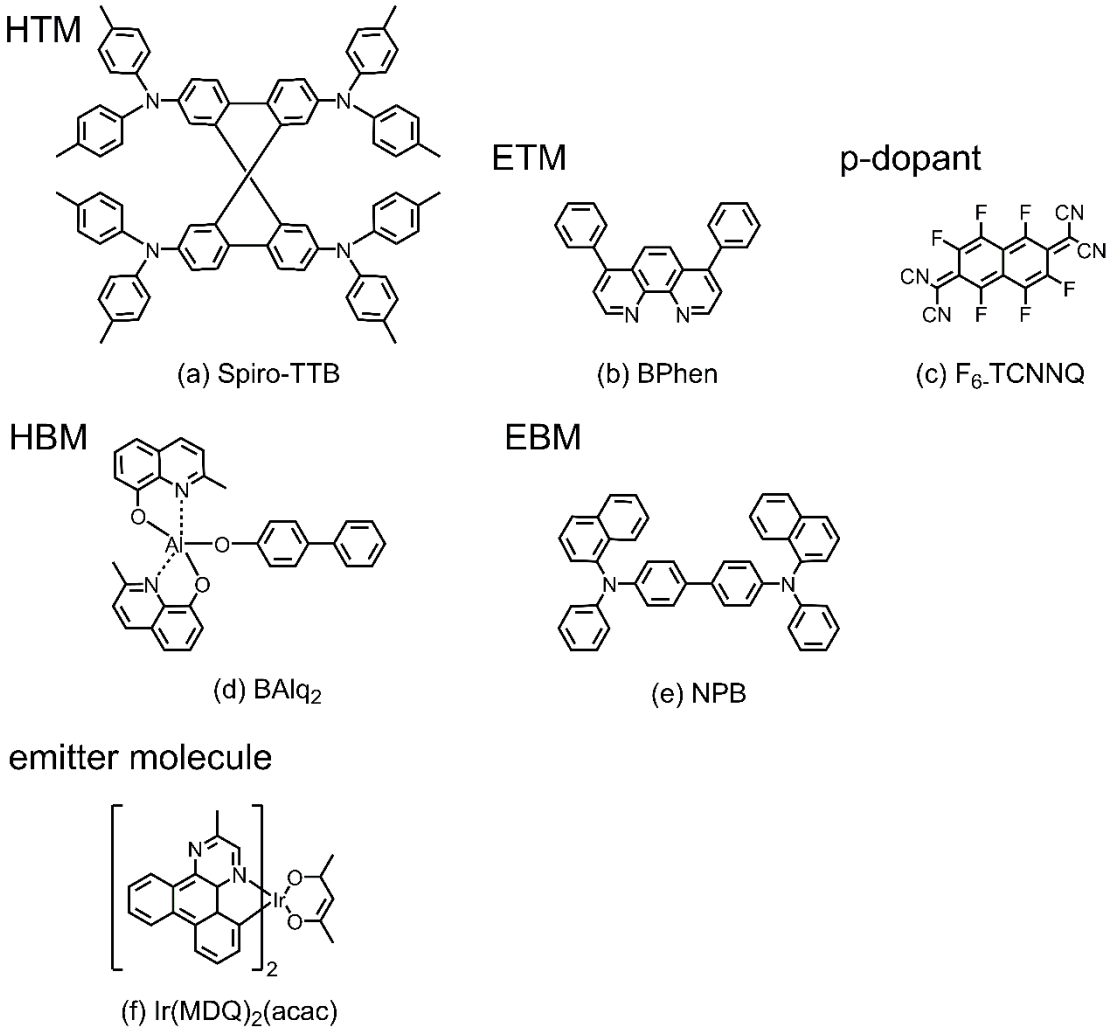


Figure 5.3.1: Chemical structure of organic materials used in the thesis.

Charge transport layer materials The p-doped layer for hole transport consists of a host made from 2,2',7,7'-tetrakis-(N,N-di-methylphenylamino)-9,9'-spirobifluorene (Spiro-TTB) which is doped with 4 wt% of the p-dopant F_6-TCNNQ. The LUMO level of the dopant F_6-TCNNQ (-5.37 eV) is lower than the HOMO level of the host Spiro-TTB (-5.25 eV), so molecular dopants can accept electrons from the hosts and increase the density of free holes [181][182]. Similarly, the n-doped layer for electron transporting contains 4,7-diphenyl-1,10-phenanthroline (BPhen) with is doped 1:1 with cesium (Cs). Cesium has low ionization energy of ca. 3.89 eV and thus strong donating ability for being used used as n-dopants [183]. In this case, the high work function 2.3 eV of Cs enables it to be a suitable electron donor though electron transfer to BPhen, which has a LUMO level of -2.9 eV [184][185]. The chemical structure of the hosts, including the hole transpot material (HTM) and electron transport material (ETM) and dopant for charge transport layer materials are depicted in Fig. 5.3.1.

Charge blocking layer materials The hole blocking layer is embedded between the n-doped layer and emission layer with bis(2-methyl-8-quinolinolate)-4-(phenylphenolato)aluminum (BAlq2) whereas the electron blocking layer is deposited in the other side next to the p-doped layer with

N,N'-di(naphthalen-1-yl)-N,N'-diphenyl benzidine (NPB). The hole blocking material $BAlq_2$ has low HOMO of -6.1 eV, and the electron blocking material NPB has high LUMO of -2.4 eV [185]. Compared with the band energy of charge transporting materials, both blocking materials provide a sufficient energy barriers to restrict the charge carrier flow while the device operation voltages will not increase substantially. The chemical structures of both types of blocking materials, i.e., hole blocking material (HBM) and electron blocking material (EBM) are shown in Fig. 5.3.1

Emission layer materials The red phosphorescence emission system has a conventional host-guest phosphorescent system in which the host material is NPB with wide energy gap, and guest material is the red phosphor of bis(2-methyldibenzo-[f,h]-chinoxaline)(acetylacetonate) ($Ir(MDQ)_2(acac)$) with 10 wt% doping concentration. The chemical structures of the phosphorescent host and guest materials are shown in Fig. 5.3.1.

Chapter 6

Lateral current flow in semiconductor devices having crossbar electrodes

6.1 Introduction

The crossbar architecture, in which the bottom and the top electrodes are designed to cross each other to define the active area as their geometric overlap region, is widely employed in organic electronic devices with semiconductor stack sandwiched in between [186][187]. Leakage current and semiconductor conductivity are two key factors which influence the performance of such organic electronics like organic light-emitting diodes (OLEDs), organic solar cells (OSCs), and organic memory devices (OMDs) [188]. For pursuing excellent performance, the former factor is required to be small while the latter one needs to be high. Regarding high conductivity, doped layers with high conductivity are then commonly used in organic devices, including those fabricated in crossbar architectures, to achieve low operation voltages [189]. However, the side effects like leakage current when operating devices in such a system are either ignored or give rise to misinterpretations regarding the device performance or layer quality.

For the sake of simplification, currents in the organic devices are typically assumed to flow exclusively along the vertical direction between two electrodes, even though the conductivities of doped organic layers are sufficiently high to generate significant lateral current flows. The lateral current flows will charge up the outside active area, introduce the leakage current, affect both device performance and characterization. Nonetheless, the scientific research field is still lacking a systematic analysis of how lateral charge transport and related leakage current is present in device characteristics and to which extent it influences the interpretation of measurement.

In this chapter, the effect of the lateral current flow in OLEDs with crossbar electrodes is studied, showing the influence of the related leakage current, and the possible utilization to investigate properties of the doped layers. First, two different device structures with doped layer structured or unstructured are introduced in Sec. 6.2. Then in Sec. 6.3, the presence of lateral charge transport is proven by a charging effect comparison between these two structure devices. The study of current-voltage and capacitance-frequency characteristics reveal that the lateral current flow, which can be suppressed by simply structuring the doped layers, is the culprit for both high leakage current in IV measurement and an abnormal capacitance increase at low frequency in CF measurement.

Subsequently in Sec. 6.4, the relation to doped layer conductivity is studied by performing layer thickness-dependent and temperature-dependent capacitance-frequency measurements via impedance spectroscopy. A distributed RC circuit model is then applied in Sec. 6.5 to the experimental data to extract fundamental information about the thickness, the conductivity, and the corresponding activation energy of both, the n-doped and the p-doped layers, simultaneously. We demonstrate in Sec. 6.6 that the lateral charging behavior can easily be misinterpreted as impactions from trap states in general trap analysis. A pseudo trap analysis is produced in details to find out the similarities. Finally, a summary is given in Sec. 6.7.

6.2 Device architecture

The current flow in OLEDs is generally assumed to flow vertically between the two electrodes as the blue arrows I_v shown in Fig. 6.2.1. However, organic doped layers already achieved a reasonable conductivity for enabling the non-negligible lateral current transport shown as the red arrow I_L. Such lateral current flow results in charged up doped layers as well as in introducing leakage current. The higher the conductivity of the doped layers is, the more significant this phenomenon is. This is an issue especially for those electronics which have a commonly used sandwich layer architecture stacked between two electrodes in a crossbar layout with an active area that is smaller than the doped layer area.

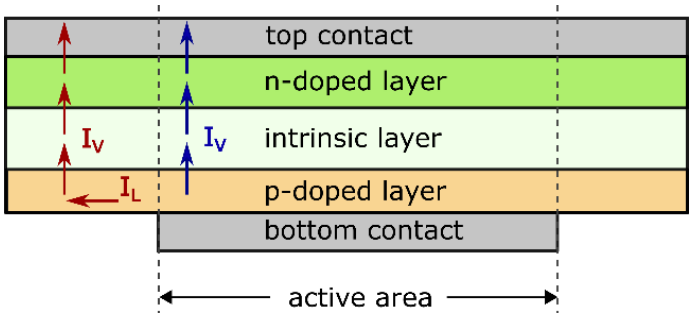


Figure 6.2.1: Schematic cross-section of the current flow in OLED.

To study the lateral current flow, OLED samples with two different layouts are fabricated. All OLED samples used in this section were fabricated following the steps introduced in Sec. 5.1 leading to a typical electrode crossbar architecture containing a p-doped/intrinsic/n-doped (pin) junction. Two 10 nm blocking layers are inserted next to both sides of the 20 nm emitting layer between the p- and n-doped layer. As illustrated in Fig. 6.2.2, on the pre-structured finger-like ITO electrodes, two different device layouts, with structured or unstructured doped layers, are fabricated to study the influence of lateral charge flow in the doped layers.

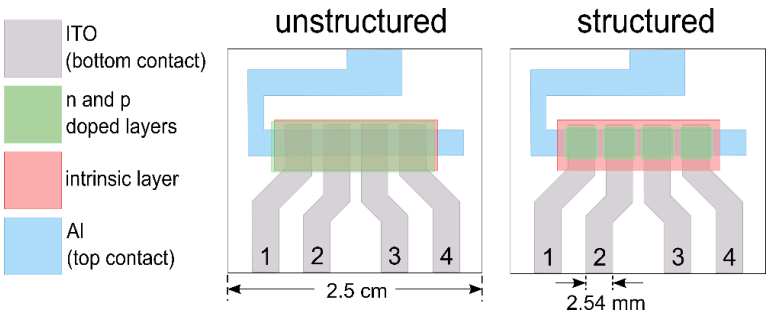


Figure 6.2.2: Top view of unstructured and structured samples.

Each sample involves four individual devices numbered by the position of the pixel as 1, 2, 3, 4. The active area is defined by the overlap between the top and bottom electrodes, being 2.54 × 2.54 mm^2 per device. Although the deposition of bottom ITO anode, top Al cathode, and embedded intrinsic layer are the same for both samples, the difference in the doped layers distinguishes them. For the left unstructured sample, all four devices share continuous doped layers, which align with the intrinsic organic layer within an area of 5.09 × 15.92 mm^2. In contrast, instead of using a continuous strip as used for the intrinsic layer in the unstructured sample, the structured sample has its n-doped and p-doped layers in separated, independent areas of 3.14 × 3.14 mm^2. Comparing the area between the structured doped layers (3.14 × 3.14 mm^2) and the device active area given by the electrodes (2.54 × 2.54 mm^2), a 300 µm larger area in all direction still exists. This additional area is designed to make sure that the doped layers always fully cover the device active area without any connection between them, even in case of any evaporation-induced misalignment.

6.3 Characteristics comparison between unstructured and structured devices

Based on the above OLEDs with two different layouts, several measurements are done to prove the presence of lateral charge transport, as well as studying the influence of it in details.

6.3.1 Charging measurement

The presence of lateral charge flow can be vertified by measuring the potential of the charged doped layers between adjacent pixels. As illustrated in Fig. 6.3.1, different constant voltages were applied to pixel 2 step by step, and the potential drop at the neighboring pixel 3 which has no connection to the external voltage source was measured over time.

To discharge the device to an initial state, 0 V was first applied to the pixel 2, and then followed by 1 V, 3 V, 1 V, and again 0 V. Each voltage was maintained for more than a minute. For the unstructured sample in the red curve, the measured voltage at the pixel first increased then decreased along with the variation of the applied voltage at the pixel 2. The precise charging and discharging behavior in the pixel 3 simulate the circuit curve of a resistor-capacitor (RC) circuit with time-delay. The raise (charging) or drop (discharging) curves are steep at the beginning and then rise slowly to the maximum voltage. Moreover, once 1 V was applied to the pixel 2, the potential of the

neighboring pixel 3 always approaches to 0.83 V after ca. 30 s, regardless of whether a low 0 V or a high 3 V had been applied previously. Similarly, when 3 V was applied to pixel 2, the voltage of pixel 3 further ramped up to 1.77 V, indicating a crosstalk effect between the individual devices.

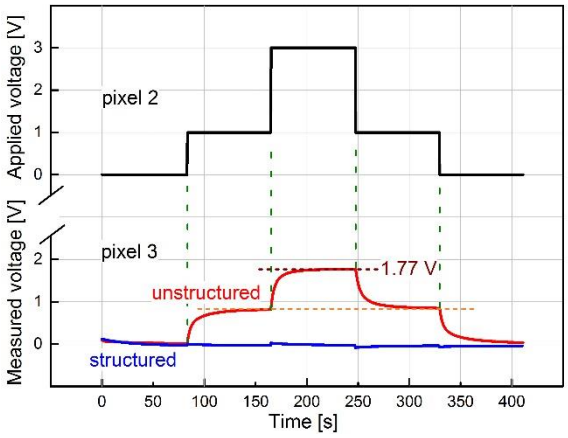


Figure 6.3.1: I-V characteristics for measuring crosstalk between neighboring pixels.

In contrast, whenever the doped layers are structured, the measured voltage at pixel 3 remains almost constant around 0 V as shown by the blue curve, independent of the voltage step applied at pixel 2. The difference in charging measurements proves that the charge can be transmitted from the pixel 2 to the neighboring pixel 3 through the doped layers, resulting in charged up layers. Such lateral charge transport only occurs in the unstructured sample with continuous doped layers since the path is cut in the doped layers structured sample. Therefore, it is necessary to structure semiconductor layers with high conductivities like the doped layers to prevent crosstalk between devices that share crossbar electrodes in integrated circuits [190], [191].

6.3.2 Current-voltage characteristics

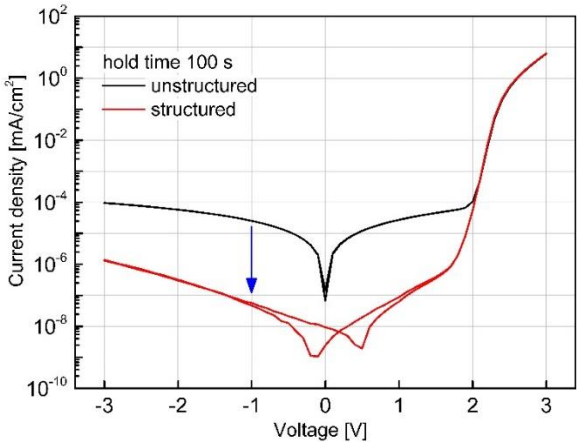


Figure 6.3.2: Comparison between a structured and an unstructured device under steady-state by keeping each applied voltage for 100 s before measurement.

The current-voltage characteristics in Fig. 6.3.2 were measured with a voltage sweep that goes from -3 V up to 3 V and back to -3 V in steps of 0.1 V in the steady-state, meaning each voltage was

applied continuously for 100 s before the current for each point was measured. The lateral charge flow proven above will charges up the neighboring doped layers, resulting in a potential difference, and eventually generating the leakage current which directly influences the current-voltage characteristics. To eliminate the influence of such lateral charging effect, the hold time used here (100 s) is much longer than the typical charge up time (ca. 30 s) obtained in Fig. 6.3.1 for fully charging the nearby doped layer to the greatest extent. For the structured device shown in Fig. 6.3.2 with the red curve, the intrinsic time-independent leakage current is drastically decreased by 2-3 orders of magnitude compared with the black curve gained from the unstructured device, resulting in extremely low leakage currents (herein 10^{-7} mA/cm^2 at -1 V).

There are two different kinds of leakage current: a time-dependent leakage current flow due to the charged up films outside the active area and an intrinsic steady-state leakage current which flows even with fully charged nearby films. Whereas the former one can be depressed by reaching the steady-state (e.g., hold time 100 s), the latter type of leakage current is unavoidable and continuously flows from anode to cathode. Interestingly, the area of the doped layer is only reduced by a factor of 8.1 from 81 mm^2 to 10 mm^2 due to structuring, whereas the reduction of leakage current is in the orders of magnitude of 1-2. This discrepancy points out that the intrinsic steady-state leakage cannot only stem from vertical leakage paths between the electrodes but also related to the lateral transport. Another evidence of inescapable leakage current flows under steady-state can already be seen in Sec. 6.3.1, where the potential of fully charged doped layers is smaller than the applied voltage.

Based on the above discussion and data, we speculate that the lateral charging in unstructured devices extends continuously in the doped layer until it reaches the edge where, due to the fabrication, the doped layers short each other or contact the opposite biased electrode. Thus, the main reason for the high steady-state leakage current in the unstructured device is still assumed to come from the lateral charge flow.

Although structuring the doped layers reduces the steady-state leakage current effectively to a drastically low level, the behavior in the forward direction at high voltage (ca. 2 V), where the current density is comparative high, does not change. This is because of the variation in vertical conductivity (resistivity) of OLEDs at different voltages. Please note that the vertical direction here refers to the perpendicular direction between the two electrodes. When the vertical potential drop stays below ca. 1.7 V, the vertical resistivity is as high as the lateral resistivity that the OLED behaves as an insulator and the lateral charging takes place in the capacitor-like doped layers over a centimeter scale, macroscopic distances. However, when the applied voltage is higher than ca. 1.7 V, the charges recombine, leading to an exponential increase in the vertical current flow. Under this circumstance, the much higher conductivity in the vertical direction prevents the current to flow in the low conductive lateral direction. This also explains why the measured voltage in Fig. 6.3.1 cannot be raised above 1.77 V even if 3 V is applied.

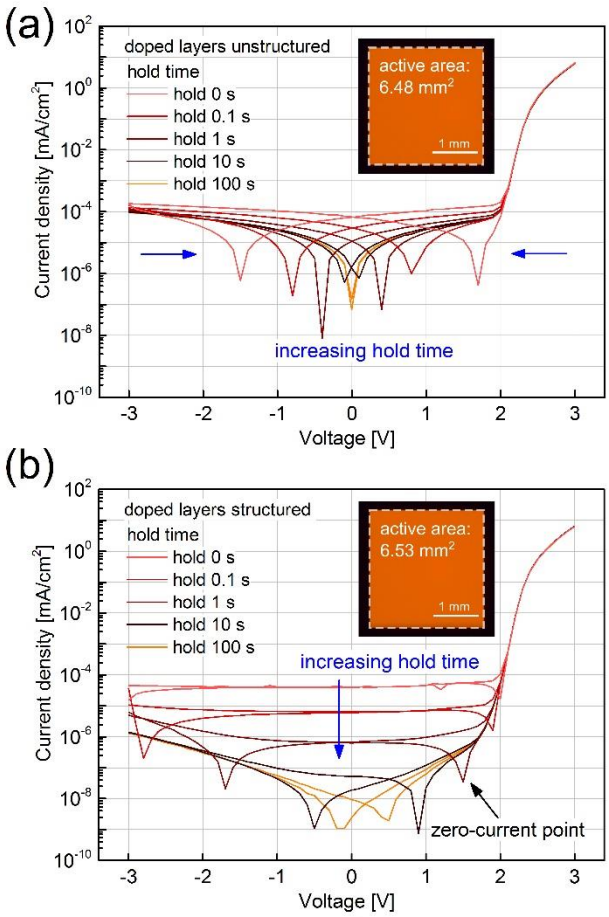


Figure 6.3.3: Different hold times were used for measuring the current-voltage curves in (a) for an unstructured and in (b) for a structured device. Insets: Picture of an operating OLED at 3V.

For a detailed discussion about the influence of lateral charging, the current-voltage characteristics for both unstructured and structured device are shown in Fig. 6.3.3 with different hold times per applied voltage. As discussed above, the impact of lateral charging on current behavior at high positive voltages is negligible. An overlap of curves above ca. 2 V can be obtained in both structured and unstructured device. Accordingly, emission images of the devices operated at 3 V, shown by the inserts in Fig. 6.3.3, prove that structuring does not influence the size of the active area.

Now we focus on the hold time variation. If no hold time was applied, a pronounced hysteresis between the forward and backward sweep directions can be obtained in both devices. As we plot the absolute value of the current density in this semi-logarithmic plot, the curve has a steep valley whenever the sign of the current changes. In one sweep, there are two crossing zero-current points: one at the negative voltage during the forward sweep, and one at the positive voltage during the backward sweep. With increasing hold time, the hysteresis becomes smaller as the crossing zero-current points shift toward 0 V. Finally at 100 s hold time, both devices achieve almost identical curves in forward and backward sweeps. However, the unavoidable high steady-state leakage in the unstructured device always keep it in a relatively high leakage current level. Such measurements have previously been reported in the literature, revealing a similar behavior [192].

In the literature, the behavior of crossing zero-current points is often explained by deep trap states which have to be fully charged or discharged before reaching the steady-state [193]. However, the results presented here support the explanation that such phenomena are possibly related to lateral current flow in a crossbar architecture which we will further discuss in this chapter. Besides this, these early-stage results demonstrate that it is also essential even for lab-scale samples to structure the highly conductive semiconductor layers, e.g., doped layer, to eliminate the lateral current flow [194], [195]. By doing this, it is then possible to do further detail investigation like study recombination mechanisms in the pronounced exponential regime, or explore the nature of the real vertical leakage current flow.

6.3.3 Capacitance-frequency characteristics

Impedance spectroscopy (IS) is extensively used to characterize the time-dependent electrical properties of organic semiconductors. In order to gain in-depth information about the lateral charging behavior in the frequency domain, the frequency-dependent capacitance (CF) measurement is provided in Fig. 6.3.4 for both samples with all four pixels represented devices per sample. Considering the symmetry of sample geometry between the two inner pixels (pixel 2, 3), their CF curves have a perfect identity and themselves can be regarded as a pair. This is also true for the two outer pixels (pixel 1,4).

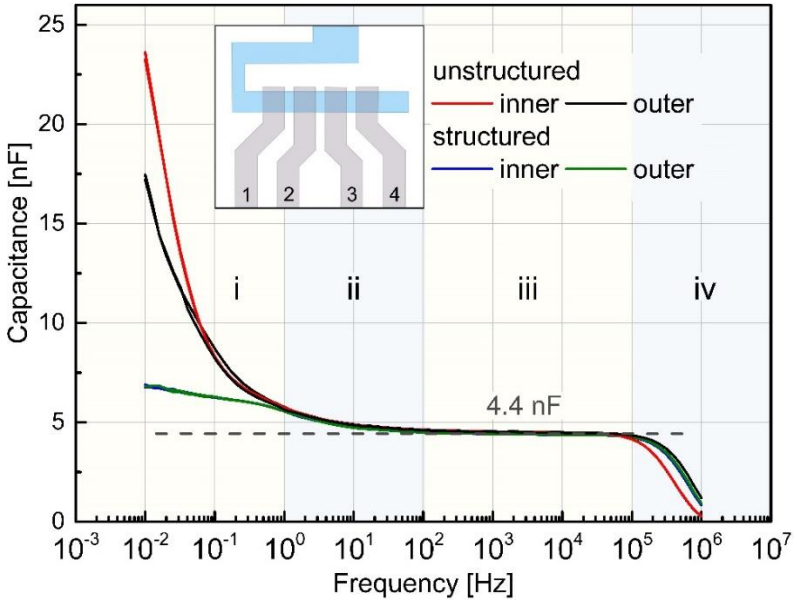


Figure 6.3.4: Capacitance-frequency curves of inner (pixel 2,3) and outer (pixel 1,4) pixels from structured and unstructured devices, each color contains two position-symmetrical devices. All four curves of the structured devices from one sample are identical, while curves for unstructured devices are symmetric to the sample geometry. Inset: Schematic of pixel position in one sample.

The most significant difference between structured and unstructured sample occurs at low frequencies between 10^{-2} Hz to 10^{1} Hz, corresponding to the hold time between 1 s to 100 s in Fig. 6.3.3, where the lateral current flow dominates the capacitance increase. In the structured devices, all four pixels have identical CF curves, showing absolute location independence. In contrast, four

pixels in the unstructured sample have precise different location-related CF performance since the lateral charging effect has distance dependence. The inner two pixels behave identically as a pair while the outer two pixels have another pair of nearly identical CF curves. The total capacitance of the outer pair is smaller than the inner pair since the former one has a more limited of doped layer area for lateral charging.

The full-frequency range spans eight orders of magnitude and can be divided into four regimes as marked by roman numbers in Fig. 6.3.4, according to their capacitance contribution:

In the regime iii with frequencies between 10^2 Hz and 10^5 Hz, the capacitance plateau of 4.4 nF is attributed to the intrinsic layer with a thickness of 40 nm, which can be calculated by using the plate capacitor equation:

$$\mathrm{C} = \varepsilon_0 \varepsilon_r \frac{A_{act}}{d} \tag{6.3.1}$$

where A_{act} is the device active area, which is 2.54 mm^2 defined as the cross area of two electrodes, the mean relative permittivity ε_r is 3.1 for the combined intrinsic layer stack.

The regime iv is defined at higher frequencies between 10^5 Hz and 10^6 Hz. In this regime, the capacitance drops significantly due to the influence of series resistance. For example, the ITO electrode has a sheet resistance of approx. 26.5 Ω/□ and can easily contribute a resistance about 50-100 Ω based on our geometry. Such ITO resistance already leads to an RC cutoff frequency at ca. 5×10^5 Hz. The slight difference between the curve-to-curve in regime iv is likely due to a device-to-device variation in series resistances.

In regime ii where frequencies spans between 10^0 Hz and 10^2 Hz, all curves in Fig. 6.3.4 for both unstructured and structured samples behave similar although the lateral charging at the outside active area starts introducing the capacitance increase for decreasing frequency. According to the discussion in Sec. 6.3.2, the capacitance stemming from outside area increases proportionally to the relative area increase outside the active area. A certain frequency decides the hold time and the related available charged up area along with the resulting capacitance. Based on the sample layout, the doped layers in all devices, regardless of the structuring or pixel position, are identical in the first 0.3 mm around the active area. Therefore, the CF spectra of all devices coincide in regime ii.

For frequency below 10^0 Hz, i.e., the regime i, the available charged up area via the doped layers outside the active area differs in structuring and position. As a consequence, the CF curves split following the position dependence discussed above. With the decrease of frequency, the capacitance increase in structured devices is constrained by the structured doped layer to be only slight, while the unstructured devices ramp up dramatically. Although it is out of experimentally accessible range, we would expect a further capacitance increase for the unstructured device at frequency smaller than 10^{-2} Hz, as the capacitance increases by almost a factor of 5 and no saturation is in reach. Moreover, the missing saturation shows that 100 s hold time (10^{-2} Hz) is not sufficient to eliminate the lateral charging effect in the unstructured devices entirely for achieving a low leakage current level. Considering the size of the sample, a centimeter-scale lateral charging via the n-doped and p-doped layers actually must be expexted. However, for the structured device, we assume that for either low

frequencies (<10^{-2} Hz) or long hold times (100 s), the entire doped layer is charged up, and the electric potential between the doped layers outside the active area is close to the applied potential.

The capacitance-frequency characteristics reveal that structuring the doped layers is essential for getting rid of the pixel position dependence, as well as obtaining reliable and reproducible data from the impedance spectroscopy. Furthermore, the doped layer should be structured as close as possible to the electrode defined active area for preventing the residual capacitance increase observed in regimes i and ii in Fig. 6.3.4.

6.4 Influence of conductivity of doped layers

6.4.1 Dependence on doped layers thickness

Since the lateral charge flow in the doped layers is responsible for the capacitance increase at low frequencies in the CF measurement and high leakage current in the IV measurement, the thickness of doped layers, which is related to their conductivity and thus lateral resistivity, should modulate the device performance. To get more precise control over the lateral charging, all doped layers mentioned in this Sec. 6.4.1 are structured to be 300 µm larger in all directions compared with the active area as mentioned before.

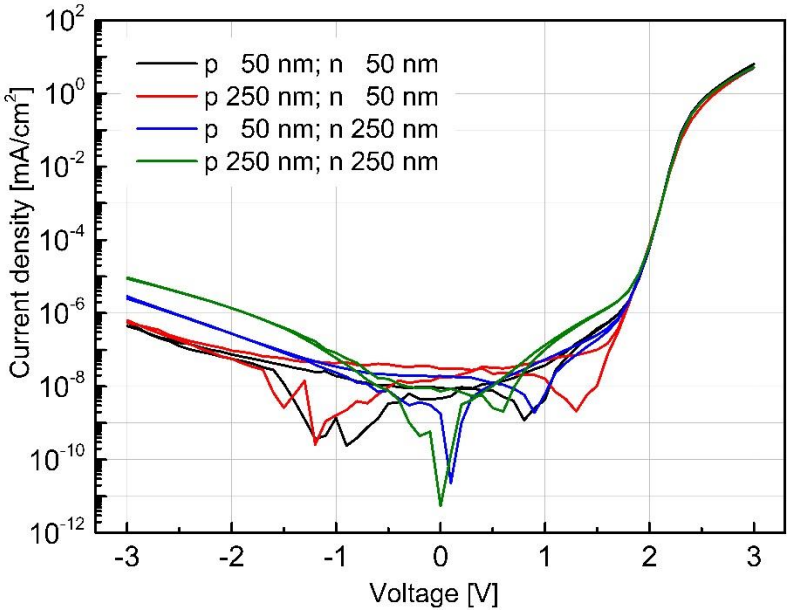


Figure 6.4.1: Current-voltage characteristics of OLEDs with structured doped layers. The thickness of the p-doped and the n-doped layers are 50 nm or 250 nm.

For the reasons of saving time, the IV curves in Fig. 6.4.1 are measured with a steady-state function, which captures at least two values for one spot, and only records the value if the difference between the measured two is within 2%. The translated equivalent hold time is around 10 s to 20 s, depending on voltage. Once the lateral charging is limited by the structuring and the steady-state is reached, no evident variation with the thickness of the doped layer can be obtained at high current densities. However, the sign of the conductivity dependence can still be perceived. The thicker the doped

layers are, the smaller the lateral resistivity is and the clearer the lateral charging effect can be. Thus, the highest leakage current is achieved for the device that has 250 nm doped layers for both n and p type (green curve), whereas the lowest leakage current results for the thinnest device with 50 nm doped layers (black curve). If the thickness of two doped layers is chosen to be 50 nm for one and 250 nm for another, the curves would locate in between all 50 nm and 250 nm curves. The more efficient control over the n-doped layer conductivity is due to its low conductivity, combined with precise thickness control.

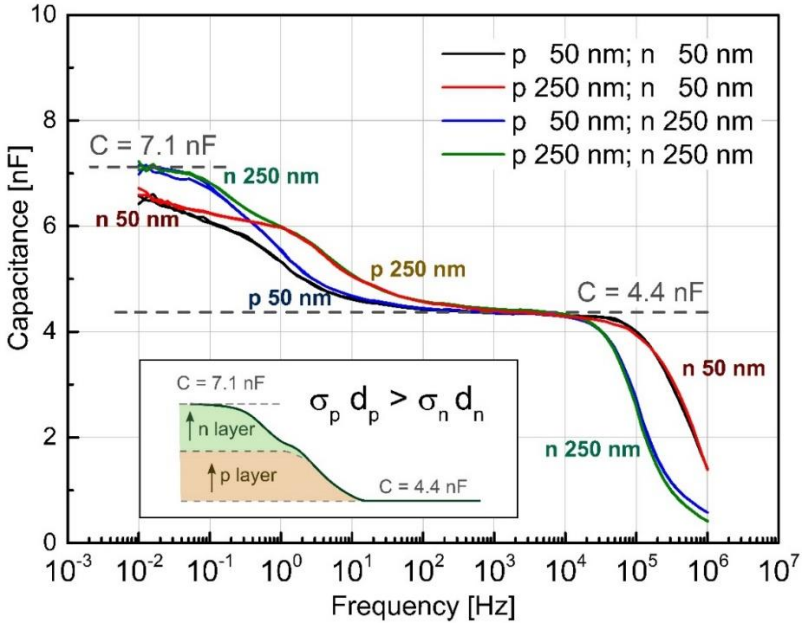


Figure 6.4.2: CF measurements of structured samples with different doped layer thickness, each color contains two devices, the thickness and the type of doped layer which are same for the overlap curves are shown next to them; insert: schematic of contribution from n-doped and p-doped layers.

In contrast, CF curves shown in Fig. 6.4.2 reveal a clear thickness dependence of the doped layers. In Fig. 6.2.2, four samples with each containing two structured devices were fabricated with all combinations of 50 nm and 250 nm thick n-doped and p-doped layers. The capacitance plateau of 4.4 nF which contributed from the OLED intrinsic layers remains the same for all cures at frequency between 10^3 Hz to 10^4 Hz. However, the two curves separate in the high and low frequency regime, respectively. Especially at low frequency, the CF spectra for each sample split differently, but such that in each region there are always pairs of coinciding curves. It is clear that whenever two curves coincide, they share a thickness for one out of two doped layers, e.g. a 250 nm p-doped layer thickness, and these two overlapped parts are therefore marked with specific colors in such cases.

As we will discuss below, the capacitance increase from lateral charging depends on both the frequency and doped layer conductivity. Therefore, the variation of the doped layer thickness is expected to shift the CF curve in that frequency band. In the low frequency regime ($f<10^2$ Hz) where the capacitance is dominated by lateral charging, the CF curves of samples with the thicker n-doped or p-doped layer shift to higher frequencies, although to different degrees. For example, between 10^0 Hz and 10^2 Hz, the influence of n-doped layer thickness is insignificant. The total capacitance has clear dependence only on p-doped layer thickness, i.e., samples with a p-doped layer of 250 nm

rise at higher frequencies than samples with a p-doped layer of 50 nm. The factor of the shift between two sets of curves is in good agreement with the thickness ratio of 5 given by the p-doped layers. A similar behavior can be found for the thickness variation of the n-doped layer at frequency between 10^{-2} Hz to 10^{0} Hz where the conductivity of the p-doped layer has a slight influence. Overall, such a thickness dependence shows a direct relationship with lateral charging, as thicker layers reduce the sheet resistance

$$R_{\square} = \frac{1}{\sigma d} \tag{6.4.1}$$

of the doped layers and enables a faster charge up of external (outside active area) capacitance. Here, σ and d are the conductivity and the thickness of the doped layer, respectively.

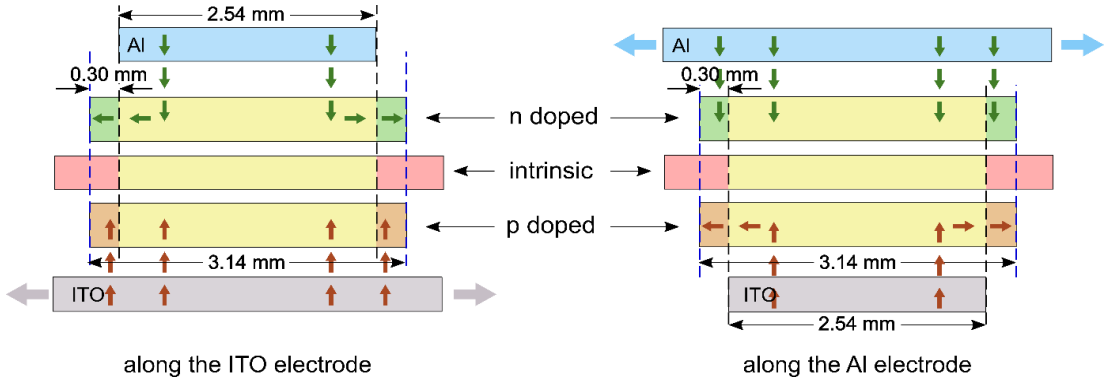


Figure 6.4.3: Schematic cross-section of the crossbar architecture along ITO (left) and along Al (right) of a structured device.

Furthermore, the type of the doped layer that dominates the increase in capacitance varies with the frequency, indicating independent capacitance contributions from two doped layers. Due to the crossbar architecture of the device, lateral charging has a preference for a semiconductor type on each sides. For example, along the ITO electrode as depicted in Fig. 6.4.3 left, the lateral current only flows at the Al cathode side to charge the external capacitance in the green area over macroscopic distances via the n-doped. However, at the ITO anode side where the ITO layer overlaps with the whole p-doped layer, the extra capacitor can be charged directly in the vertical direction over tens of nanometer only distance via the p-doped layer. Nevertheless, the situation is opposite along the Al electrode side (Fig. 6.4.3 right). The lateral charging only occurs near the ITO side to charge up the layers via the p-doped layer, whereas the capacitance increasing at the Al side is governed by the vertical charging via the n-doped layer. The final capacitance increase at low frequency is the extra lateral charge up along both electrode sides while the preference at different electrode sides translates into individual charging contribution from different areas, related to the n-doped and the p-doped layers as visualized in Fig. 6.4.4.

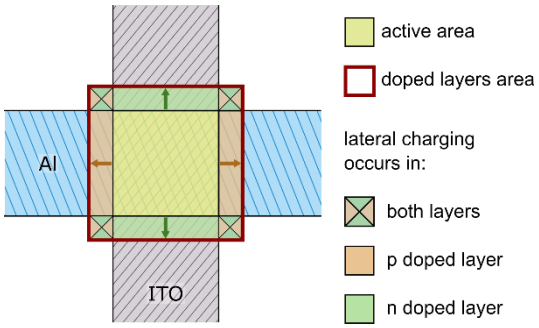


Figure 6.4.4: Top view of a single pixel having a structured doped layer (thick dark red square).

Electrical conductance determining factors like film thickness, resistance directly influence the curve behavior in CF measurements. Therefore, a kink is observed for all four CF curves in Fig. 6.4.2 since the doped layers have different sheet resistances and thus different frequencies at which the capacitance saturates. The p-doped layer can be identified here as the layer with the lowest sheet resistance (highest conductivity) as it shows the thickness variation dependence at the high frequency regime.

A complete charge up of the outside area takes merely place at lowest frequencies and only for doped layers with small sheet resistance (Fig. 6.4.2). It is also an exciting feature that the overall capacitance 7.1 nF achieved at the lowest frequency (10^{-2} Hz) in Fig. 6.4.2 is following what we expect to get based on the lateral dimensions of the structured doped layers. The ideal value of overall capacitance $C_{max,doped}$ can be extrapolated from OLED active area-defined capacitance C_{act} as

$$C_{max,doped} = C_{act}\frac{A_{doped}}{A_{act}} \tag{6.4.2}$$

which is based on the geometric ratio of the active area to the structured doped layer area. The calculated ideal capacitance is 6.9 nF, within a reasonable deviation compared to be experimental capacitance of 7.1 nF. The nicely fitting values also indicate that the lateral charging via the doped layers is the exclusive path for extra and does not proceed if only intrinsic layers are available.

The lateral current flow is prevented at high frequency between 10^4 Hz to 10^6 Hz due to its low mobility. Therefore, the capacitance in the CF spectra (Fig. 6.4.2) is only dominated by the vertical charging of the intrinsic layers in the vertical direction within the active area [196], [197]. Because of the sufficiently high vertical conductance of the p-doped layer, it can prevent a high frequency cutoff below 10^6 Hz regardless of its thickness. As a result, only the thickness variations in the n-doped layer can be observed as a frequency-dependent curve shift. In contrast to lateral charging, thicker doped layer now leads to smaller capacitance, or in another word, a shift of capacitance drop towards the low frequency since the vertical resistance increases with layer thickness.

6.4.2 Dependence on temperature

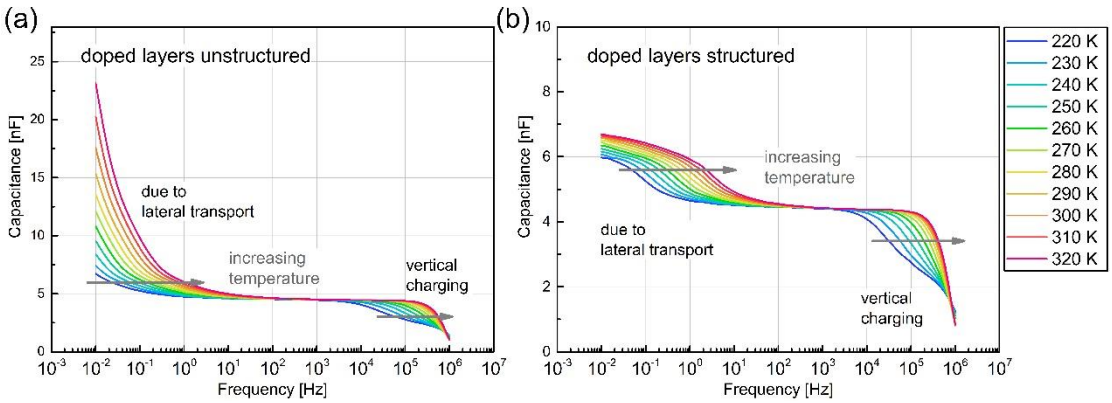


Figure 6.4.5: Temperature-dependent CF curves of (a) unstructured and (b) structured of a 50 nm doped layer structured device with pin layer stack embedded into the crossbar. For clear curve observation, please note that there is a difference in y axis scales.

As mentioned before, the sheet resistance of the doped layers influences the frequency-dependent lateral charging, which should also reflect on the temperature dependence since the conductivity of the doped layers can be varied easily by the temperature. Fig. 6.4.5 shows the CF spectra of the unstructured and structured device with 50 nm doped layers with the temperature variation from 230 K to 320 K in the step of 10 K. Being structured or not does not decide the underlying temperature-dependent capacitance trend. At the same frequency, the value of capacitance increases gradually with the rise of temperature at both low and high frequency regimes, matching with the thermally activated charge mobility and doping efficiency[198], [199]. Alternatively, in another description, the higher the temperature gets, the more the curves are shifted to higher frequencies corresponding to the expected increased conductivity of the organic semiconductor with temperature. Once the conductivity is high enough like under 310 K to 330 K, such a shift tendency may not be visible at high frequency due to the cutoff point that stems from the temperature-independent external series resistance.

Similar as in Sec. 6.3.3, curves with the same temperature but different doped layer structures behave identical at frequencies higher than 10^0 Hz, which is the point at which the lateral charging starts. After that, the unstructured device with no limitation for lateral charging in Fig. 6.14.5 (a) demonstrates stronger dependence on temperature, revealing as an increase of curve steepness along with the increase of temperature. Finally, the highest capacitance can be gained at 10^{-2} Hz with 320 K. More precise control over the structured doped layers enables a detailed investigation on the temperature dependence in Fig. 6.4.5 (b). In the low frequency regime, it can be observed that although all curves horizontally shift along with the frequency, the qualitative shape of the curve remains the same. The same situation can be seen for the kink, which is attributed to the conductivity difference between the two doped layers. A visible horizontal kink movement confirms the conductivity increase in the p-doped layer with temperature. Moreover, unlike the unstructured device, the curve shift will also approach saturation once the maximum capacitance is achieved at low frequency, especially for the highest temperature.

Despite the curve variation at low and high frequency regimes, the 4.4 nF plateau capacitance at 10^3 Hz does not change with temperature. If the temperature is assumed to change the number of free charge carriers in the doped layers, the capacitance of the intrinsic layers should also change as the width of the depletion region shrinks according to the Mott-Schottky-analysis [83]. However, the fact that this assumption is not valid suggests that the observed temperature dependence of the conductivity is mainly given by a temperature-dependent charge carrier mobility and not so much by an increased density of dopants.

6.5 Lateral charging simulation

The circuit model for OLEDs simulation typically focuses on vertical direction behavior, although the doped layers, which are extensively used in the OLEDs for enhancing the charge injection and the charge transport in the vertical direction, will introduce a strong lateral charging effect as described above. The situation is different for inorganic LEDs, where the doped layer is intentionally designed in the layout to be a pathway for spreading the current flow laterally over the active area. However, there are only a few examples where similar concepts are used in organic electronics and detailed analysis and simulation are still lacking [200-202].

Nevertheless, a similar phenomenon of charging a series of capacitors by a resistive wire was initially described in the field of telegraph lines, leading to a signal delay effect [203]. Such electric signal delay is further well known by the complementary metal-oxide-semiconductor (CMOS) circuit, which suffers from the extra capacitances created by the interconnected conducting line over the insulator layer [204]. The resistive-capacitive delay in CMOS can be simulated using a distributed RC-delay model, identical to the RC network for solving the diffusion equation [204]. Even though the driving force for the lateral current as the lateral differences in the electrical potential is not exactly same as the diffusion of charge carriers, lateral charging still has an inherent diffusion-like nature and can be analyzed by an analog model.

6.5.1 Analytical description

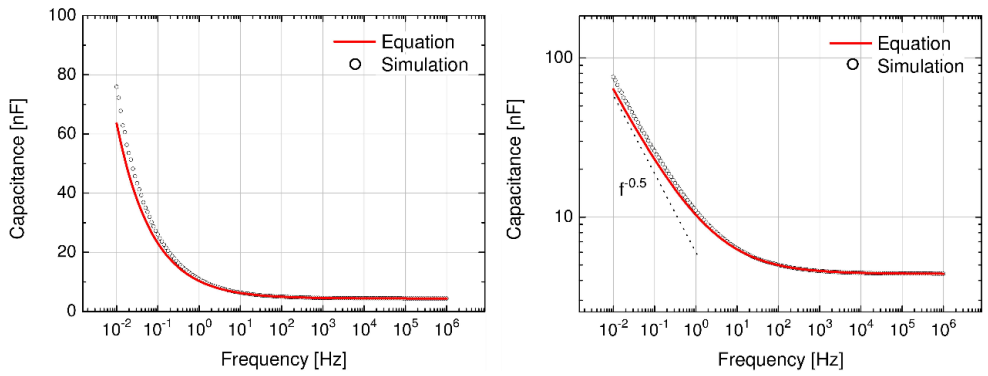


Figure 6.5.1: Comparison between analytical solution and simulation capacitance-frequency dependence for the charge up of a laterally extended capacitance via a resistive layer. The constant capacitance 4.4 nF of the active area has been added to the analytical solution.

Before doing an accurate simulation, a rough estimation of the RC time can be done by assuming that the lateral charging of the capacitance outside the active area is done over the resistance given by the entire distance of the doped layer corresponding to this outside area. To simplify it, the lateral charging is considered to take place in only one direction which starts from the edge of the active area. However, the result based on such assumptions will overestimate the RC time constant as in reality, parts of the area can be charged over a smaller distance to the active area and thus via a lower resistance. The capacitance outside the active area according to assumptions can be expressed as:

$$\Delta \mathrm{C} = \frac{C_{act}}{w^2} \times w \times l = \frac{C_{act}}{w} \times l \tag{6.5.1}$$

where w is the width of the square active area and l is the charged up distance. ΔC and C_{act} are the capacitance from outside and inside the active area, respectively. The related resistance of the doped layer is:

$$\mathrm{R} = \frac{1}{\sigma} \frac{l}{d \times w} \tag{6.5.2}$$

with σ being the electrical conductivity, and d being the thickness of the doped layer. Combining Eq. 6.5.1 and Eq. 6.5.2 yields the following equation as:

$$\mathrm{R} = \frac{1}{\sigma} \frac{1}{d} \frac{\Delta C}{C_{act}} \tag{6.5.3}$$

Once the time constant $\mathrm{R} \times \Delta \mathrm{C}$ is converted into frequency by using $\tau = 1/2\pi f$, a capacitance frequency dependence can be gained as:

$$\Delta \mathrm{C} = \sqrt{\sigma \mathrm{d} C_{act}} \frac{1}{\sqrt{2\pi f}} = \sqrt{\frac{C_{act}}{R_{\square}}} \frac{1}{\sqrt{2\pi f}} \tag{6.5.4}$$

There is a characteristic $\Delta \mathrm{C} \propto f^{-0.5}$ dependence which stems from the fact that the product of $\mathrm{R}\Delta \mathrm{C}$ is proportional to the square of the distance (l) to the active area. From Eq. 6.5.4, it is clear that the frequency at which a certain charge up ΔC can be achieved is:

$$\mathrm{f} = \frac{\sigma d C_{act}}{2\pi (\Delta C)^2} = \frac{C_{act}}{R_{\square}} \frac{1}{2\pi (\Delta C)^2} \tag{6.5.5}$$

depends linearly on σ and d, and thus indirectly proportional to the sheet resistance $R_{\square}$ of the doped layer at a certain achieved ΔC. This relation confirms the conclusion from the previous sections that the conductivity as well as the layer thickness can linearly shift the CF spectra along the frequency axis.

To prove these equations, we compare them with simulation results as shown in Fig. 6.5.1. Although this is a simplified analytical solution, it has a reasonable agreement with the modeled data which is simulated with an identical set of parameters (σ= 1 S/m, $d_{\text{doped layers}}$ = 50 nm, C_{act} = 4.4 nF). Moreover, the analytical $\Delta \mathrm{C} \propto f^{-0.5}$ relation is also reproduced by the simulation. In this frequency regime, the analytical solution has a relative error of the frequency in the range of 30 % and a relative error of the capacitance in the range of 15 %.

6.5.2 RC circuit simulation

The aforementioned analytical solution in Sec. 6.5.1 corresponds to a lumped RC circuit model where the lateral charging is described by a single compressed resistor and capacitor at a certain frequency. In order to obtain the complete information contained in the CF curve, such as different conductivity for doped layers, the whole capacitance behavior needs to be simulated as a function of frequency. For doing this, a finely discretized distributed RC circuit model was developed for explaining the charging in both vertical and lateral direction.

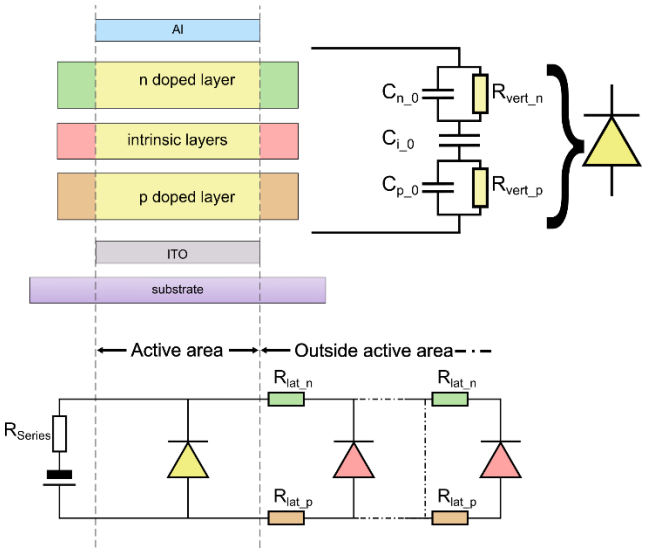


Figure 6.5.2: Schematic RC circuit used for simulation.

As illustrated in the upper panel in Fig. 6.5.2, for each OLED unit consisting of a p-i-n stack unit, the charge is assumed to flow vertically and homogeneously. Thus, the p- and n-doped layer unit can be further divided into a parallel-connected capacitor and resistor, while the intrinsic layers unit can be regarded as a capacitor. A series connection between an n-doped layer (capacitor//resistor), intrinsic layers (capacitor) and a p-doped layer (capacitor//resistor) simulates the vertical charging behavior and is symbolized by a diode following.

Based on this, the circuit responsible for the active area was simulated. Since the lateral charging is negligible within the active area, a single giant diode element colored in yellow was used as the module. The respective resistances $R_{vet,n}$, $R_{vet,p}$ for n-doped layer, p-doped layer are related to the geometry and the conductivity of each layer. The capacitance value C_{i_0} for representing the intrinsic layers in between is the plateau value of 4.4 nF at 10^3 Hz, as shown before in both Fig. 6.4.2 and Fig. 6.4.5. After adding an external series resistance (e.g results from the ITO electrode), the general CF behavior at high frequencies greater than 10^3 Hz can be expressed by this model.

The model for the circuit outside the active area is required for replicating the whole behavior in the low frequency region, which necessitates the introduction of distributed RC elements as sketched in the bottom of Fig. 6.5.2. The situation is more complicated due to the presence of both vertical and lateral charging. For the vertical charging behavior, in spite of the value difference results from the effective area difference, the external vertical layer stack outside the active area has the same

charging behavior as the inside. Therefore, the vertical charging can be presented by finely discretized vertical elements shown as pink diodes. The resistors and capacitances of each unit cell in the pink diode are scaled to the effective area respectively, which is given by the product of the width of the electrode and a discretization length ΔL of 1 μm. For the outside active area region, there are three different regions based on the Fig. 6.4.3 and Fig. 6.4.4:

1. Regions along the ITO electrode with lateral charging via the n-doped layer (Fig. 6.4.3 left).

2. Regions along the Al electrode with lateral charging via the p-doped layer (Fig. 6.4.3 right).

3. Regions close at the corners of the active area with lateral charging via both the n-doped layer and the p-doped layer (Fig. 6.4.4 marked with cross-checks)

For the structured device in which the doped layer is tightly structured to the active area, the lateral charging length is limited to be 300 μm. Thus, the capacitance activated in the area of the last case ($4 \times 0.3 \times 0.3$ mm^2) is neglectable small compared with that from the other two regions ($4 \times 0.3 \times 2.54$ mm^2). Therefore, the last case is not contained in the model for simplification. Although the lateral charging has a side-dependent preference in the type of the doped layers, the equal layout guarantees the symmetric element distribution and results in the parallel connection of two pathways for the lateral current flow. Two unit resistors $R_{lat,n}$ and $R_{lat,p}$ connect each neighboring pink diode element at the outside active area, eventually present a full frequency description RC circuit model. The values of the lateral unit resistors depend on the sheet resistance of each responsible doped layer. The extra capacitance raising at the low frequency now can be well described by the RC circuit that the lateral current flows through the doped layers and then charge up the additional intrinsic layers in the OLED element outside the active area. The end of the RC circuit line is defined by the extra length by which the doped layers exceed the active area.

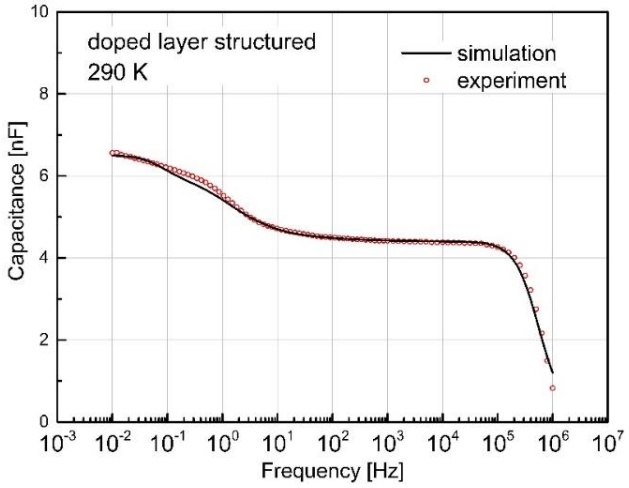


Figure 6.5.3: Comparison of CF curves between experiment and fit at 290 K.

Using this RC circuit model, a simulated CF curve was obtained at room temperature (290 K). Fig. 6.5.3 shows a direct comparison between the simulated curve and experiment curve, which match each other with an acceptable deviation. One thing that needs to be mentioned is that there is always a mask misalignment for the doped layers in the sub-millimeter range in reality. Due to this imperfect

area aligned during the evaporation, the lateral charging length outside the active area can slightly differ for each side. Therefore, a parameter called 'misalignment' on behalf of the shifts of the doped layers along the diagonal of the active area is introduced in the model. The qualitative CF behavior does not charge at all, but an even better agreement with the experiment data is achieved once the doped layer is shifted by 105 µm, which is in is in the range misalignment that is typically observed.

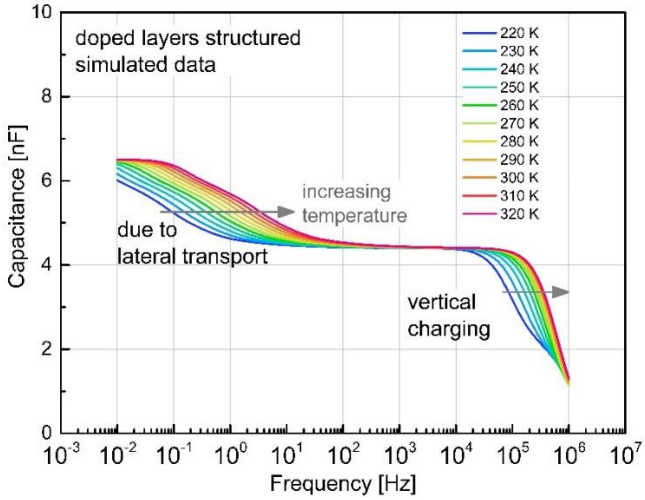


Figure 6.5.4: Simulated temperature-dependent CF curves of a 50 nm doped layer structured device with RC circuit model.

Inspired by the simulation at 290 K, the temperature dependence can be simulated by importing a new parameter 'activation energy E_a' to tune the conductivity of the doped layers following an Arrhenius-like temperature activation:

$$\sigma(T) = \sigma_0 \exp[-\frac{E_a}{k_B}(\frac{1}{T} - \frac{1}{T_0})] \qquad (6.5.6)$$

where σ_0 is the conductivity at the reference temperature T_0 which is 290 K in this case 290, k_B is the Boltzmann constant.

By fitting the simulated curves to the temperature-dependent CF curves for the structured device shown in Fig. 6.4.5 (b), the activation energies for both doped layers can be gained from the simulated data in Fig. 6.5.4. We obtained 0.21 eV and 0.22 eV for the n-doped layer and p-doped layer, respectively. Hence, the experimental temperature dependence can, in turn, be reproduced with the temperature-activated conductivity and the fitted activation energies are within a reasonable range for bulk charge carrier mobility in organic semiconductors [205-207].

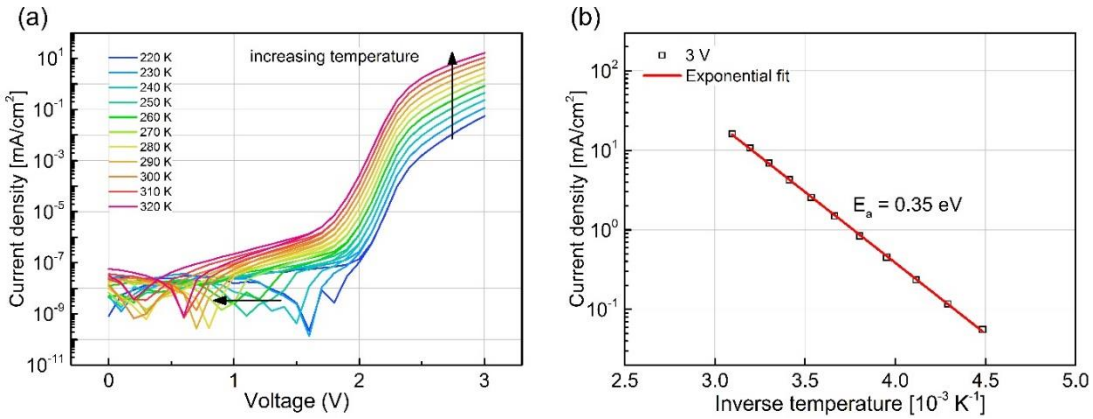


Figure 6.5.5: (a) Temperature-dependent IV characteristics of an OLED with 50nm thick structured doped layers. (b) The corresponding activation energy of the current density at 3 V.

However, the activation energy E_a plotted from the temperature-dependent current density at 3 V in Fig. 6.5.5 is 0.35 eV, which is roughly 0.13 eV higher than the activation energy obtained from CF simulation. One reason might be that the activation energy, determined by CF is related to lateral current flow, whereas the charge mainly flows in a vertical direction in the IV curves when the applied voltages are higher than built-in voltage. Overall, this indicate that the activation energy, and very possible also the conductivity, can vary a lot between vertical and lateral directions, even for evaporated device. Another reason might be that there are multiple processes like charge injection, overcoming internal energy barriers, and charge transport in the intrinsic layers which influence the IV measurement in Fig. 6.5.5 (a). Furthermore, since the activation of the doped layers has not much influence on the activation of device current in forward direction, the CF measurement is a suitable method to study the contribution from the doped layers.

6.5.3 Parameters for doped layers gained by simulation

All parameters used in the distributed RC circuit model are listed in Tab. 6.5.1. The parameters of the individual resistor and capacitor unit of the RC network rely on the device geometry, the discretization length, and the fitting parameters. The fitting parameters, i.e., the information about the doped layers, including the thickness, the conductivity, and the corresponding activation energy of both, the n-doped and the p-doped layers are automatically gained from the fitting. If the fitting parameters are in turn being used to calculate the R&C elements in the lateral charging and vertical charging model circuits, the qualitative frequency dependence on the capacitance is reproduced.

Experimental set of parameters used in the simulation		
A_{act}	2.54^2	mm^2
$A_{doped\ layers}$	3.14^2	mm^2
ΔL	1	μm
ε_r	4.0	
R_{series}	50	Ω
C_i	4.4	nF
misalignment	105	μm
Parameters of the doped layers obtained from simulation		
d	40	nm
σ_n	5.8×10^{-6}	S/cm
σ_p	9.8×10^{-5}	S/cm
$E_{a,n}$	0.21	eV
$E_{a,p}$	0.22	eV

Table 6.5.1: summary of the parameters obtained from fitting the doped layers structured experimental data with the equivalent RC circuit model.

The simultaneously obtained conductivities, which are 5.8×10^{-6} S/cm for the n-doped layer and 9.8×10^{-5} S/cm for p-doped layer, are within a reasonable range for doped semiconductors [206]. Furthermore, instead of a 50 nm thickness as defined during the evaporation, an djusted thickness of the doped layers of 40 nm is used in order to match the low frequency and high frequency behavior. This 10 nm deviation may be the reduction in the effective doped layer thickness, i.e., there are depletion regimes in the doped layers which depress the realistic film thickness in terms of its conductance contribution [208]. Herein, the widely used impedance spectroscopy proved to be a useful tool for post-checking the properties of doped layers in already assembled devices, as well as estimating the success or not for the doped layer fabrication.

Although the justified agreement between the experimental and simulated curves is over eight orders of magnitude in the frequency range, there is still a slight deviation originate from several aspects. Firstly, the area at the four corners of the crossbar structure is neglected in the model for simplification. As shown in Fig. 6.4.4 marked with cross-checks, these corner areas suffer from lateral current via both the n-doped layer and the p-doped layer, which yields one-tenth of the total extra capacitance for the outside active area. This effect is comparatively small but still leads to fitting error. Secondly, the evaporated doped layers, in reality, are not distributed uniformly but have a trapezoidal shape due to the evaporation geometry, so that the sheet resistance of the doped layers increases towards the edge and introduces an error in the simulation. Furthermore, similar to the difference in activition energy for different directions, the conductivities in the lateral and vertical direction of the same doped layer are not necessarily equal, especially since the charge carrier mobility is anisotropic in films that experience layer-by-layer growth, e.g., there can be a higher mobility in the vertical direction due to π-π stacking. Finally, it cannot be ruled out that a certain capacitance in the low frequency regime is rising due to trap states. For the temperature varied CF curves, simulated curves show a more significant deviation at the high frequency regime which is dominated by vertical charging. As discussed before in Sec. 6.5.2, although it is used for the whole

frequency range simulation, the lateral E_a for doped layers which extracted from CF curves at low frequency is 0.13 meV smaller than the vertical one obtained from the IV curves in the exponential regime. Therefore, at the high frequency range in CF measurement, the lateral Ea is too small to repeat the exact behavior of experimental curves, which has a larger frequency shift interval and more conspicuous temperature dependency.

Nonetheless, the simplified RC circuit model covers all fundamental qualitative aspects of the CF measurement and yields reasonable values for the doped layers.

6.6 Pseudo trap analysis

Impedance spectroscopy which is utilized for investigating the doped layers in this chapter is also routinely used to characterize the electrical properties of organic semiconductors. However, the influence of the presence-proved later charging has not been considered yet as a source of error for analysis [209-211]. To explore trap states in crossbar architecture diodes, impedance spectroscopy is commonly employed for measuring the temperature-dependent admittance capacitance-frequency spectra at low frequency to determine the density of occupied states [197], [210], [212], [213]. In the defect trap analysis, the capacitance increase is a crucial factor for the quantitative evaluation, which is same in the lateral charging case. Since both the electronic trap states and lateral charging behaviors eventually shown as capacitance increase at the low frequency regime in CF measurement, they are easy to be confused. Therefore, it is necessary to study in details about the consequence of two fundamentally different reasons hidden behind the same CF characteristics.

6.6.1 The pseudo trap density of states determination

Before the discussion, it has to be pointed out again that the neighboring charging measurement shown in Fig. 6.3.1 already clearly proves the existence of lateral current flow, as well as its centimeter-scale transportability for mainly contributing to the CF behavior. After clarifying this point, a pseudo-trap analysis is performed by applying the method proposed by Walter et al. [214]

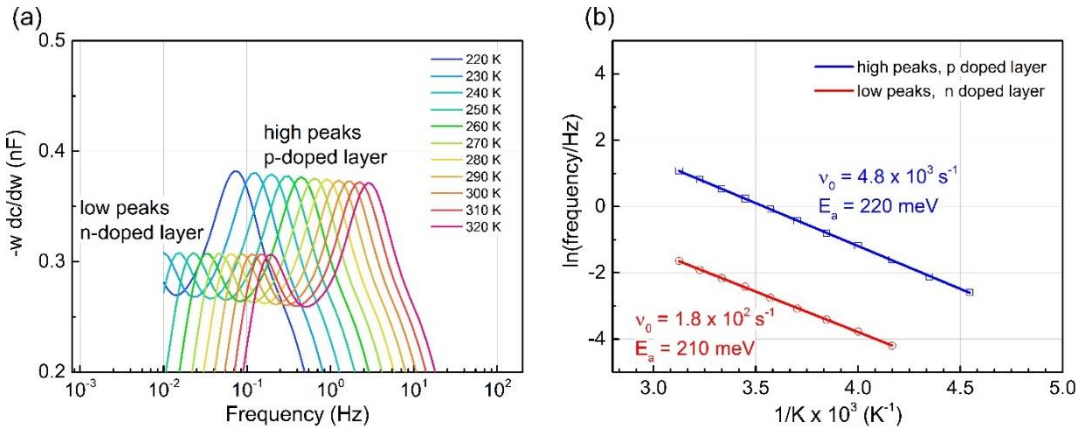


Figure 6.6.1: (a) Frequency dependence of the trap contribution to the capacitance change for the simulated CF curve (T=220 K - 320 K), the peak is the value of the emission frequency. (b) Arrhenius plot of the emission frequencies ω_0.

In theory, the trap capacitance obtained by impedance spectroscopy reflects the slowly trapped and released charge carriers that need to be activated, e.g., via electrical activation at low frequency or thermal activation, to contribute to the overall capacitance. The derivative of the frequency spectrum $-\omega dC/d\omega$, which describes trap-contributed capacitance change, can be used to determine the attempt-to-escape frequency υ_0 from the emission frequency ω_0 with temperature variation. As plotted in Fig. 6.6.1 (a), the frequency correspondings to the maximum in the capacitance change for each temperature is the emission frequency ω_0, which represents the emission rate of the responding trap states. By plotting the ω_0 at which the peak occurs against inverse temperature in Fig. 6.6.1 (b), the thermal activation energy E_a as well as the attempt-to-escape frequency υ_0 can be extracted by fitting the Arrhenius plots with:

$$E_a = k_B T ln \frac{2\upsilon_0}{\omega_0} \tag{6.6.1}$$

However, since the real reason behind the capacitance change is the lateral charging, which has doped layer conductivity dependence, Fig. 6.6.1 (a) reveals two groups of peaks due to the conductivity difference of the two doped layers. The capacitance contribution from higher frequencies belongs to the layer with higher conductivity, which is the p-doped layer in this case, while peaks at lower frequencies come from the less conductive n-doped layer. Two groups of emission frequency ω_0, therefore, acquired in Fig. 6.6.1 (a) that yields two attempt-to-escape frequency υ_0 and two activation energy E_a in Fig. 6.6.1 (b). The activation energies, which are 210 meV for the n-doped layer and 220 meV for the p-doped layer, are the same values of the respective E_a gained from lateral charging simulation (Tab. 6.5.1). The resulting υ_0 are 1.8×10^2 Hz and 4.8×10^3 Hz for the p-doped and the n-doped layer, respectively.

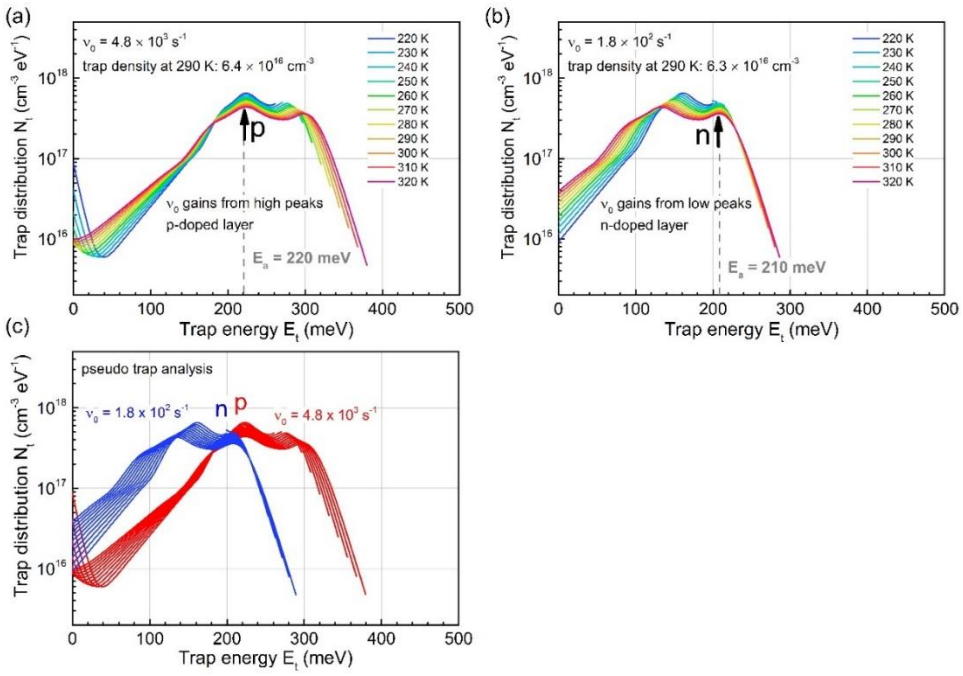


Figure 6.6.2: Pseudo trap analysis based on the Walter analysis using υ_0 gained from (a) p-doped layer, (b) n-doped layer, and (c) direct comparison between these two groups of curves. This is performed to indicate the similarity between the lateral charging and trap states.

With the parameters calculated above, the energetic profile of the trap density of states (tDOS) distribution $Nt(E_\omega)$ is reconstructed from the CF spectra at different temperatures using the equation:

$$N_T(E_\omega) = -\frac{V_{bi}}{qW}\frac{dC}{d\omega}\frac{\omega}{k_B T} \tag{6.6.2}$$

wherein q is the elementary charge, V_{bi} is the built-in potential guessed to be 2 V and W is the depletion width chosen to be 40 nm as the thickness of intrinsic layers.

Two trap distributions can be obtained by the Walter method based on two different υ_0 values, aiming to fit with the respective doped layer. As reported from Eq. 6.6.1, a conversion from the frequency axis in the CF spectra into the energy axis requires the knowledge of a correct attempt-to-escape frequency υ_0, which is fitted in such a way that the calculated trap distribution curves of the same device coincide in the energy range at different temperatures [214]. As shown in Fig. 6.6.2, two groups of overlapping peaks are apparent visible with different but close trap energy as well as trap densities. For Fig. 6.6.2 (a) which is plotted with υ_0 on behalf of the p-doped layer, a good overlay of the spectra around the peak position at different temperatures for p-doped layer peaks indicates the correct determination of υ_0 for this layer. The peaks corresponding to the n-doped layer are rather spread out and don't overlap as the p-doped layer peaks. The opposite is in the case for Fig. 6.6.2 (b) where a good peak superposition is now visible for the n-doped layer curves with the correct υ_0. In both cases, the peaks for the p-doped layer appears more in the left based on its higher conductivity, which translates into smaller activation energies being activated to increase the capacitance. A direct comparison of pseudo trap analyses can be seen in Fig. 6.6.2 (c).

The trap energy E_t in Fig. 6.6.2 is defined as the energy between the trapped charge carrier and the transport level. The value of it at the peak position is equal to the activation energy of respective doped layer. As already indicated in Fig. 6.6.1 (b), the pseudo trap energy derived from the peak position matches perfectly to the E_a listed in Tab. 6.5.1 as both of them related to the thermally activated charge transport in the doped layers. Despite the type of the doped layers, the pseudo energy gained here locates within the typical expectation range for organic semiconductor, suggesting the possibility in misinterpreting the data. Furthermore, the pseudo trap density calculated by integrating over the whole energy range is ca. 6×10^{16} cm^{-3} at 290 K for both υ_0 cases, being a reasonable value for facilitating the confusion. Moreover, the energetic width of the Gaussian distributed curves is in the range of several 10 meV, again situated in the range of expected values although the exact value is vague in the pseudo one [197], [210]. The only parameter outside the typical range is the magnitude smaller derived attempt-to-escape frequency. However, there are also some similarly small order of magnitude frequencies reported previously like polyhexylthiophene (P3HT) [197], [210], [212], [213]. The most pronounced pseudo appearance in the trap analysis is the number of the group of peaks in Fig. 6.6.2, of which there are two instead of one due to conductivity and activation energy difference. However, from the composed curves in Fig. 6.6.2 (c), one nearly blended groups of peaks can be seen once the attempt-to-escape frequencies are separated fitted for two doped layers.

In principle, the lateral charging, which is a process of laterally flowing charge carriers being 'trapped' outside the active area and introducing capacitance, is possible to disguise itself as the trap-like behavior by producing similar CF characteristics. More specifically, the characteristic of

lateral charging that can generate the capacitance increase at the low frequency of which has a temperature dependence over the spread CF curves is the typical fingerprint of the presence of trap states. Such an effect is lurking in all crossbar architecture devices with conductive semiconductors (doped layers) and has to be on guard.

6.6.2 The pseudo trap analysis under simulated identical conditions

Fig. 6.6.2 (c) shows a high risk of mixing lateral charging with trap states behavior with ideal attempt-to-escape frequencies, which is not difficult to achieve if doped layers have similar conductivity. To make this statement more clear by revealing more details about the similarity of effects from trap states and lateral charging, the Walter method was applied in Fig. 6.6.3 again with simulated identical data to get undisturbed behaviors.

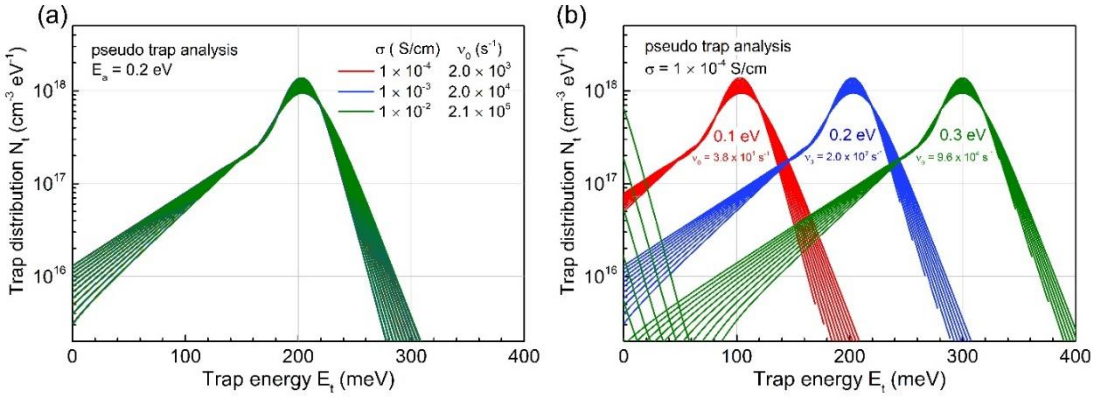


Figure 6.6.3: Pseudo trap analysis under identical conditions with (a) same activation energy but different conductivity, and (b) same conductivity but different activation energy.

The identical pseudo trap analysis was done with the following assumptions:

1. Both doped layers and the active area are perfectly aligned in the center.

2. Both doped layers share the same conductivity σ and thermal activation energy E_a.

3. Any external series resistance, e.g., from ITO electrode or metal electrode, is reduced to 0.1 Ω to move the limitation of RC time and thus the cut off out of the measurable frequency range from 10^{-2} Hz to 10^6 Hz.

4. Since the lateral resistance of the doped layer is inversely proportional to the thickness of the doped layers according to Eq. 6.5.2., the thickness of doped layers is limited to 20 nm for enlarging the influence of doped layer conductivity.

5. The temperature is varied from 220 K to 320 K in 10 K steps.

6. All other simulation parameters remain constant in this chapter unless mentioned otherwise.

Fig. 6.6.3 (a) reveals the influence of the variate activation energy E_a. As discussed above, the value of the activation energy is always presented as the trap energy depth in the pseudo trap analysis. As long as E_a is fixed to be 0.2 eV in the simulation, the trap distributions curves in Fig. 6.6.3 (a) would

always coincide in the full trap energy range with the same peak value of 0.2 eV, regardless of the value of the conductivity to be 10^{-2}, 10^{-3} or 10^{-4} S/cm. That is to say, in the Arrhenius plot of the emission frequencies ω_0, fitting curves for varied conductivities share the same fitting slope but with different attempt-to-escape frequency υ_0 as noted previously in Fig. 6.6.1. Since υ_0 follows the trend of the conductivity increase geometrically according to Eq. 6.6.1, the doped layer with a conductivity of 10^{-2} S/cm yields the reasonable υ_0 of 2.1×10^5 Hz for common semiconductors. Thus, special attention needs to be paid to semiconductors with high conductivity like C_{60} in trap analysis. This misidentification is also noteworthy for lower conductivity semiconductor if the film is thick. The next simulation is varied the E_a from 0.1 to 0.3 eV with the same conductivity of 1×10^4 S/m as shown in Fig. 6.6.3 (b). Three groups of curves shift along the trap energy as expected, with the same shape but different corresponding υ_0 which shift with the E_a as well.

Overall, the simulation once again points out the serious possibility of lateral charging in introducing an ambiguity which has to be ruled out by further experiments, e.g. by next pixel charging experiment as shown in Fig. 6.3.1. This is a potential risk not only for trap analysis by Walter method but also for other measurement methods where traps are aimed to be identified, e.g. thermally stimulated currents [215]. It needs to be emphasized finally that all characteristic electrical behaviors produced in this chapter can be mainly explained by lateral charging effect and do not rely on any significant trap state population.

6.7 Summary

This chapter investigates the centimeter scale lateral charge up of capacitances outside the active area due to doped layers in devices with crossbar electrodes. The resulting time-dependent leakage current can be dramatically reduced to an ultimate low level of 10^{-7} mA/cm^2 at -1 V by structuring the doped layer close to the active area. Achieving this low leakage current level which is typically tricky for devices employing doped layers offers the opportunity to study recombination related physical processes at low excitation as well as the mechanisms behind the undisturbed real vertical leakage current in the future. The position dependence in capacitance-frequency measurement can also be solved by structuring, leading to individual uniform devices. Impedance spectroscopy was employed to investigate the lateral charging role in the capacitance increase at low frequency as well as its dependence on temperature, doped layer conductivity. A distributed RC circuit model was proposed to fit the experimental CF data in the entire frequency range over eight magnitudes and allows for parameters extraction simultaneously including the thickness, the conductivity, thermal activation energy of both, the n-doped and the p-doped layers, corresponding to the lateral charge up at low frequency. Consequently, the rich and detailed information opens up the utility possibility in properties checking of doped layers in the fabrication finished or even packaged finished devices.

Furthermore, capacitive effects stemming from lateral charging have such similarity to those associated with deep trap states that this can potentially create a misinterpretations at the capacitance-frequency characteristics. After analyzing the pseudo trap distribution using simulation data of both realistic and identical parameters, a caution sign was to be placed on trap analysis without a suppression of lateral current flow in the widely-used crossbar structure.

The results from the chapter are not limited to OLED with doped layers, but also applicable to any crossbar structure where semiconductor materials, especially those with high conductivities are involved. Moreover, our results will aid the design and characterization of electronic devices either kill the leakage current like for memory devices or in turn exploit the lateral charge flow as device concept [202] [216].

Chapter 7

The pinMOS memory: novel diode-capacitor memory with multiple-bit storage

7.1 Introduction

The significant reduction of leakage current by eliminating the lateral charge up in organic devices promises the realization of organic non-volatile memory (ONVM) devices based on crossbar architecture OLEDs, which have been intensively investigated in this work as the new concept of data storage media. The main research of ONVM devices concentrates on resistive memories, which are often referred to as memristors [217]. The charges are stored in electronic traps or nanoparticles like in resistive random access memory (ReRAM) devices or single transistor-based memory devices, although the former one is difficult in achieving multiple-bit storage while the latter one is limit to the further downscaling due to their inherent minimum channel length requirement [218-220][144]. However, another concept of storage, the capacitive memory or referred to as memcapacitor, in which the information is stored in the local charge up of an integrated capacitance and presented by capacitance, received far less attention.

In this chapter, a diode-based, simple fabrication, organic capacitive memory is demonstrated. The novel p-i-n-metal-oxide-semiconductor (pinMOS) memory has the capability to store multiple bits and to read them out electrically or optically via various pathways, i.e., it can be programmed by voltage or UV light stimuli, as well as being read out by capacitance or light emission (which will be discussed in detail in the next chapter). The dual operation in writing and reading processes makes the pinMOS memory attractive for future use in integrated electronic and photonic circuits. First, the structure of diode-based pinMOS memory is introduced in Sec. 7.2, and the leakage current is proved to be reduced effectively by preventing the lateral charging as discussed in the Chapter. 6. Then in Sec. 7.3, the relationship between CF and CV curves with or without defined memory states are discussed, showing the memory phenomenon of the pinMOS memory device with excellent repeatability, reasonable switching behavior of 10^4 write-read-erase-read cycles and currently already over 24 h retention time. The working mechanisms under both dynamic and steady-state operation are investigated in Sec. 7.4 as an essential basis to identify further optimization steps. The memory window tunability is studied in details in Sec. 7.5 with operation parameters, ultraviolet light illumination, and variation of the intrinsic layer thickness, indicating programmable multiple-

bit storage by either voltage application or light illumination. An early-stage study of pinMOS memory in synaptic behavior in Sec. 7.6 reveals its potential application in neuromorphic computing or visual memory systems in the future. Finally, a summary of this reliable capacitive memory device is given in Sec. 7.7.

7.2 Device architecture

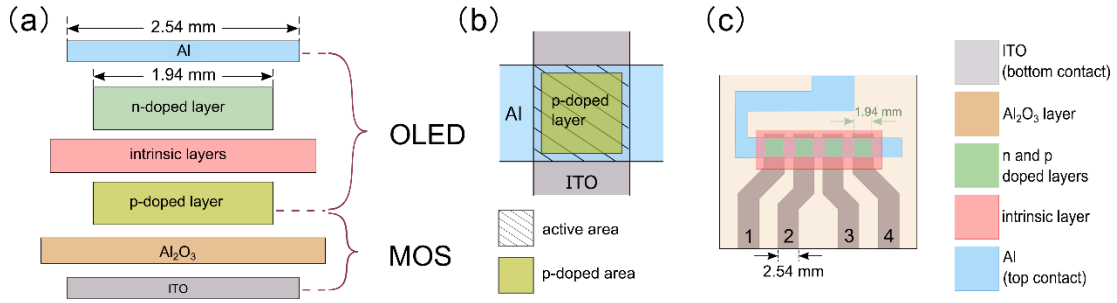


Figure 7.2.1: (a) Schematic cross-section of architecture for the pinMOS memory. Top view of (b) showing the relative position of the structured p-doped layer and crossbar electrodes, (c) one sample contains four pixel-presented devices.

The novel programmable, non-volatile p-i-n-metal-oxide-semiconductor (pinMOS) memory is an easy-fabrication, simple diode-capacitor based memory device, of which the OLED based memory devices are seldom studied in the literature. As shown in Fig. 7.2.1 (a), the pinMOS memory was fabricated on top of a 50 nm aluminum oxide (Al_2O_3) layer with a typical crossbar architecture comprising a standard red-emitting OLED stack. The OLED stack here, including materal, was deposited following the steps introduced in the previous sections, yields a p-doped/intrinsic/n-doped (p-i-n) junction with 50 nm p-doped layer /40 nm intrinsic including 20 nm emitting layer and two layers of 10 nm blocking layer at each side/ 50 nm n-doped layer. The thickness remains the same for all devices in this chapter unless otherwise explicitly stated. The p-doped layer in the OLED stack, which is neighboring to the oxide layer, has high conductivity and cannot be entirely depleted due to its 50 nm thickness. Therefore, the p-doped layer decouples itself as well as bridges the OLED stack (p-i-n junction) and the MOS (metal-oxide semiconductor) capacitor in the pinMOS memory.

In Chapter 6, we proved the presence of doped layer induced lateral charging and demostrate magnitudes lower leakage current by cutting off the lateral flow pathways via structuring the doped layers. Thus, to prevent the leakage current from later charging completely, both doped layers were intentionally structured to be 0.3 mm smaller in all directions compared to the active area given by the crossbar electrodes as illustrated in Fig. 7.2.1 (b). A more detailed device layout can be seen in Fig. 7.2.1 (c). On the pre-structured finger-like ITO electrodes, the oxide layer was deposited by atomic layer deposition (ALD) to cover the whole sample, of which contains four individual devices numbered by the position of the pixel as 1, 2, 3, 4. Both doped layers were structured to be 1.94 × 1.94 mm^2, while the embedded intrinsic organic layer has a continous ribbon-like area of 5.09 × 15.92 mm^2. Although it is not applicable in the pinMOS memory, the active area in the conventional sense defined by the overlap between the top and bottom electrodes is 2.54 × 2.54 mm^2 per device.

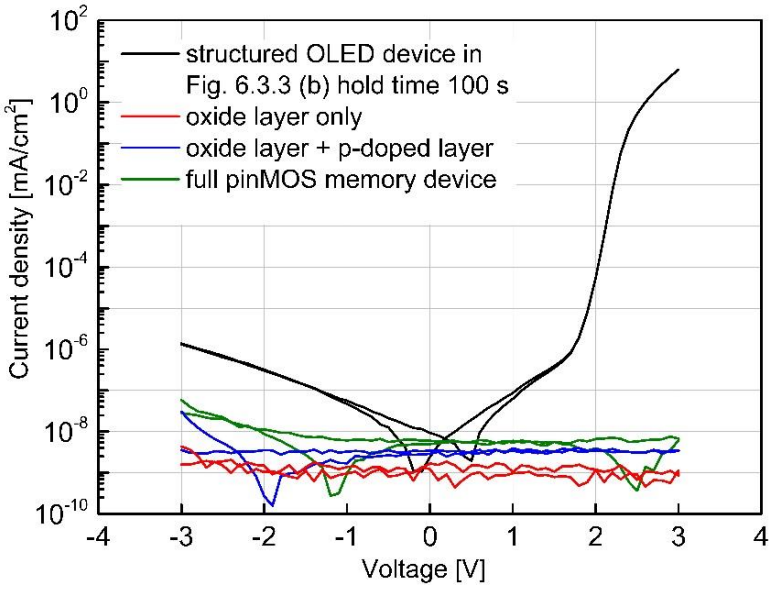


Figure 7.2.2: Current-voltage characteristics of different devices.

The leakage current is a crucial concern for a memory device application, which accounts for short retention time, destroyed information, high power consumption, and poor device performance in general. Here for the pinMOS memory, both a structured doped layers layout and an ALD-deposited insulator layer are utilized to achieve an extremely low leakage current. To examine this, the current-voltage (IV) characteristics of three different devices were performed with previous described steady-state function in Fig. 7.2.2: one with 50 nm Al_2O_3 layer only (red curve), one with 50 nm Al_2O_3 layer and 50 nm p-doped layer (blue curve), and a full pinMOS memory device (green curve). Regarding the low leakage current, a structured OLED device from Chapter 6, Fig. 6.3.3 (b), which was measured with hold time of 100 s, is plotted in a black curve as a reference. The reference OLED device and the OLED stack in the pinMOS memory device share the same materials and corresponding layer thicknesses. All devices have almost constant leakage current around 10^{-8} mA/cm^2 over a range of ±3 V. The values are comparatively low or even one magnitude lower than the already excellent performance of the original OLED device. However, the more layers are introduced, the higher leakage current is obtained, verified by more and more obvious crossing zero-current points as well. Since the path of lateral current flow is restricted, the leakage currents here are most probably the intrinsic vertical leakage current flows in the doped layers, e.g., from surface traps. Characteristics for pinMOS memory device

7.2.1 Dependence on layout and pixel

Impedance spectroscopy was employed in Fig. 7.3.1 to investigate the frequency-dependent capacitance of devices with varied layers. Each color stands for one specific stack, containing four devices from one sample but four different pixel positions. All curves have a cutoff at high frequency region due to RC limitation stemming from an external series resistance. Devices in black curves which are only comprise of an oxide layer remain at a high capacitance of 7.3 nF over a broad frequency range that spans six orders of magnitude as expected from an oxide layer. If an

extra p-doped layer is deposited onto the oxide layer as shown in red curves, a frequency-dependent capacitance increase can be seen along with the decrease of frequency, steming from the gradually undepleted p-doped layer. Once the frequency is smaller than 10^0 Hz, the overall capacitance of the device only contributes from the oxide layer, as revealed by the overlapped plateaus with the oxide only devices in Fig. 7.3.1. Since the lateral charging is suppressed by structuring the doped layers to be smaller than the active area, no further capacitance increase can be observed at the lowest frequencies. Furthermore, the good overlap of four red curves indicates the nice repeatability in the frequency-dependent depletion behavior. The introduction of series-connected intrinsic layers for the devices represented by the blue and green curves leads to a reduction of the plateau capacitance from 7.3 nF to 2.9 nF. Like the p-doped layers in red curves, the n-doped layers in blue curves do not show any further charging at the lowest frequency. Meanwhile, the depletion of the n-doped layer now produces only negligible capacitance contributions to the overall small value, losing its dominating role in high frequency region and leaving almost constant blue curves.

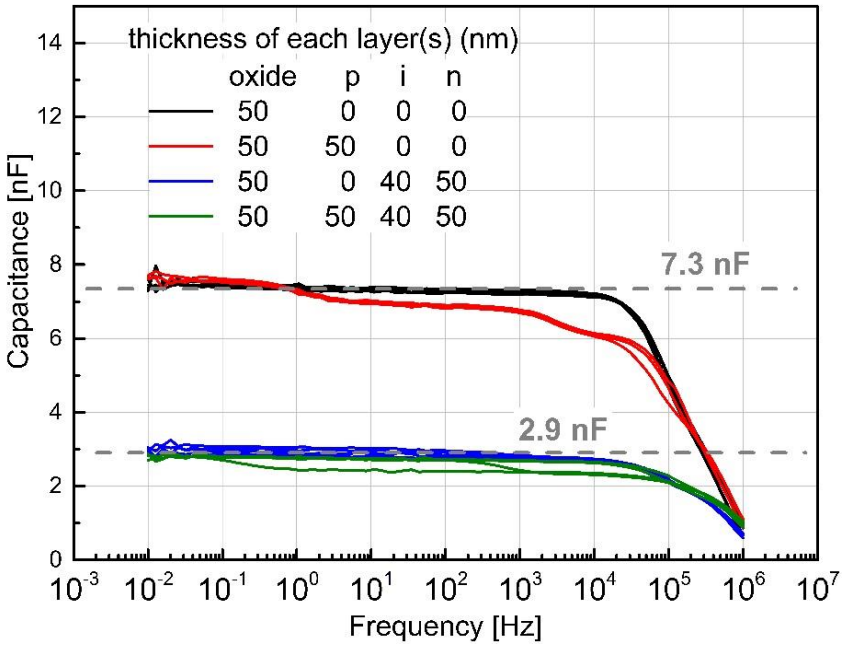


Figure 7.2.3: Capacitance-frequency curves of samples with different layouts. Each color symbolizes one sample contains four devices.

However, when p-doped layers were also introduced as shown in the green curve to produce full pinMOS memory devices, the curves have device-to-device variation in capacitance behavior. Two out of four devices have similar behavior as the blue curves without p-doped layers, achieving the high plateau of 2.9 nF beyond the cutoff frequency. Nevertheless, the other two devices showing a capacitance shift between a low plateau of ca. 2.6 nF and a high plateau of 2.9 nF. The non-constant threshold frequency for capacitance variation locates in a large range, herein shown both at a high frequency of 10^3 Hz and a low frequency of 3×10^{-1} Hz. Since the latter low frequency is magnitude smaller than 10^0 Hz, the frequency-dependent depletion behavior in the p-doped layer discussed for red curves cannot explain the capacitance increase in green curves anymore. Unlike the former two devices where the doped layers, either the p- or the n-type, are connected to one side electrode

directly, the p-doped layers in the pinMOS memory devices are embedded in two carrier blocking layers. Therefore, the fabrication induced additional stored charges may be the reason for device-to-device variations.

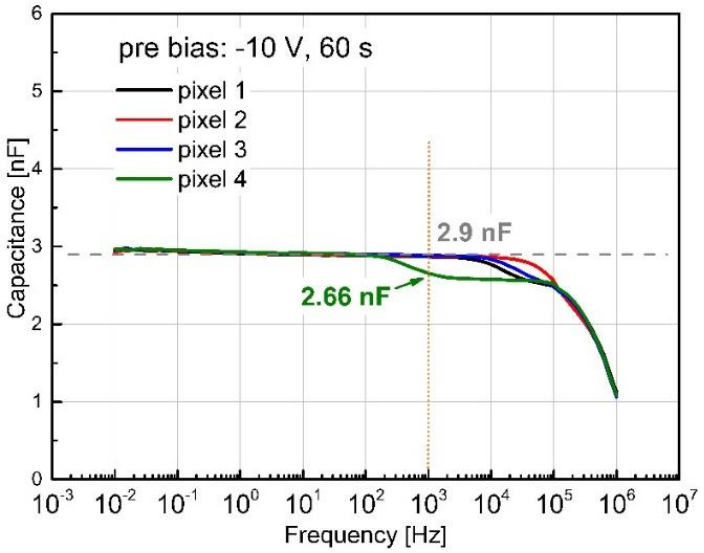


Figure 7.2.4: CF measurement for four devices in one sample with pre-bias of -10 V for 60 s.

In order to gain identical curves for the full pinMOS memory devices, a pre-bias of -10 V was applied for 60 s before the CF measurement to drive them to a certain state by adding charges which will be explained later in the following sections. The resulting curves from four pixels in one sample are revealed in Fig. 7.3.2. Although the capacitance shifting is still observable, the curves are comparable identically than ones without pre-bias since most of the upwards shift now happens in the high frequency range of 10^4 Hz to 10^5 Hz, except the one at ~10^3 Hz,. Following the threshold frequency shifts of pixel 4 from 3×10^{-1} Hz (in Fig. 7.3.1) to 2×10^3 Hz, all devices can now reach the highest 2.9 nF plateau before 10^2 Hz.

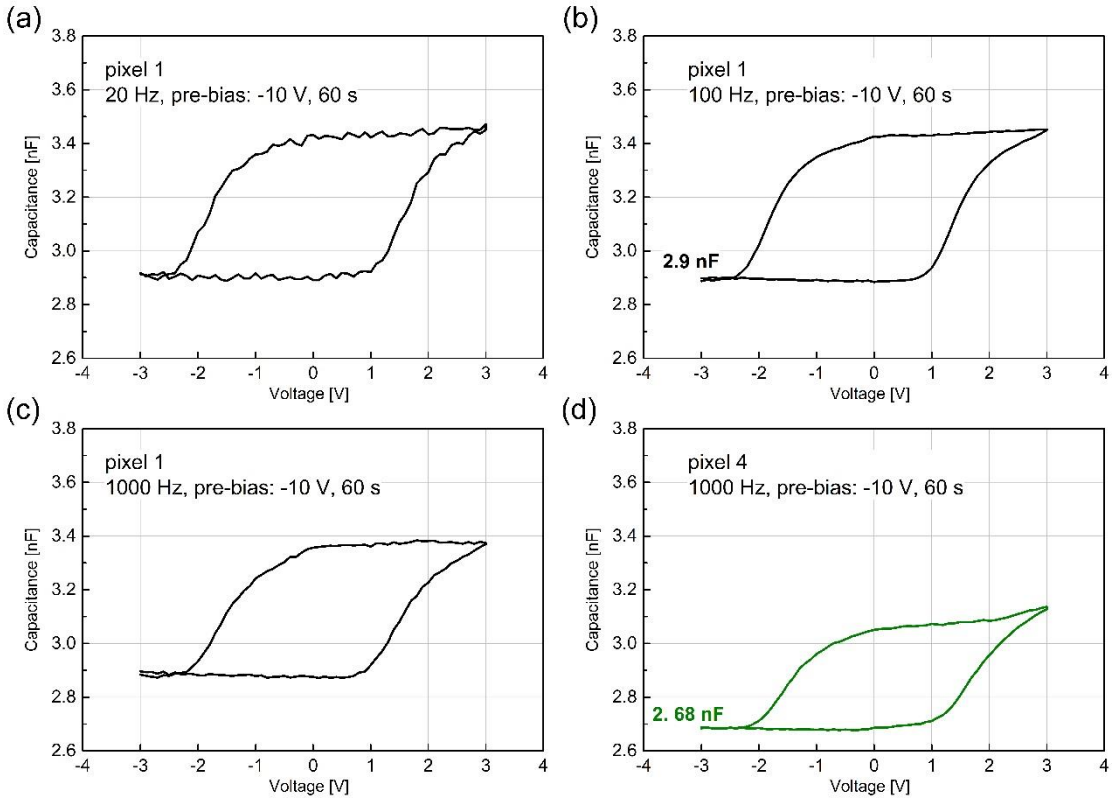


Figure 7.2.5: Capacitance-voltage measurements with the frequency of (a) 20 Hz, (b) 100 Hz, (c) 1000 Hz for pixel 1, respectively and (d) 1000 Hz for pixel 4 after a pre-bias of -10 V applied for 60 s.

The curve shifting in CF measurement indicates a successful manipulation of the capacitance by applying the pre-bias, which is a hint for memory phenomenon where the pre-bias application can be defined as writing process. The CF curve measured in this chapter are taken with a voltage of 0 V (amplitude is 20 mV) for all frequencies. When CF curves are translated into CV curves with an exact frequency, the corresponding capacitance points in the CF curves should be presented at the point of 0 V in CV curves. Therefore, before a detailed investigation of the capacitance-voltage behavior of the pinMOS memory device is done, the best frequency of the measurement must be determined to eliminate the device-to-device capacitance variation. For doing this, capacitance-voltage measurements with different frequencies for both pixel 1 and 4 were done with a pre-bias of -10 V, 60 s as shown in Fig. 7.3.3. Due to the equipment measurement limitation, the lowest frequency is set to be 20 Hz instead of 10 Hz. In the initial section of this CV related discussion, we will introduce the electrically assessed memory effect and its characteristics with the language remaining quite general, e.g. stored information/charges, etc., before we discuss our current understanding of the complex physical working mechanism in more detail.

After applying -10 V for 60 s, all devices were swept from -3 V to 3 V and then back to -3 V in steps of 1 V. A significant hysteresis from forward and backward sweeps can be obtained for all devices, directly revealing a memory effect as discussed in details later in the following sections. Regardless of the frequency of 20, 100, or 1000 Hz, CV curves driven from pixel 1 have a similar shape with the same low plateau value of 2.9 nF. The similarity in the CV behavior is consistent with the frequency-independent capacitance behavior for pixel 1 in the corresponding CF curve at low

frequency region (<10^3 Hz). Moreover, the obtained lowest capacitance of 2.9 nF in the CV curve is the same value to the constant capacitance in the CF curve. To verify the capacitance uniformity, the CV measurement was also performed for the pixel 4 at 1000 Hz, which situates in the capacitance transition region of the CF measurement. As a consequence, the overall capacitance drops, although the hysteretic shape remains. The lowest capacitance value of 2.68 nF, however, is consistent with the 2.66 nF capacitance value in CF curve of pixel 4 at 1000 Hz. For a specific frequency, the curve translation between CF and CV measurements can be concluded as the same capacitance value at the CF point and the low plateau of CV curve. On the other hand, the rising behavior of capacitance, as well as the final high plateau value in the CV curve, are invisible in CF curve with an amplitude of ±20 mV, indicating that the capacitance hysteresis in CV curves is driven by sweep voltage. To ensure the data uniformity, the frequency for CV measurements in the following is kept fixed at 100 Hz, for which the capacitance plateau can be achieved for all pixels.

7.2.2 Fundamental memory behavior characterization

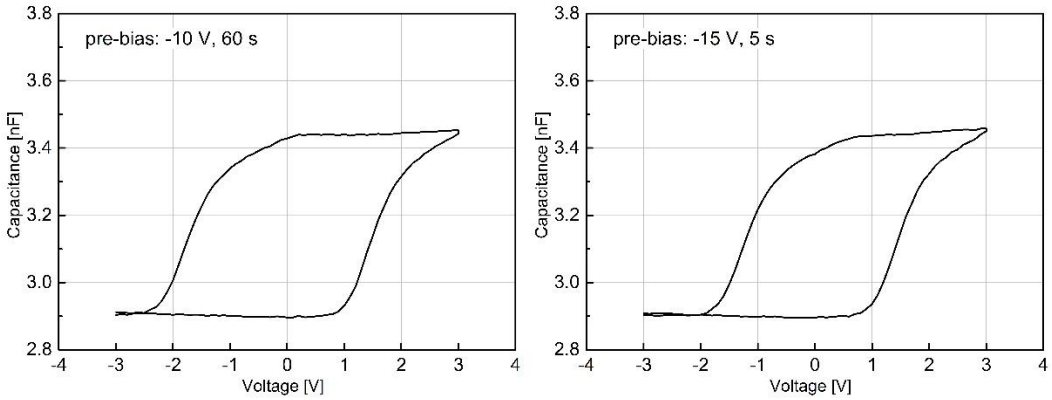


Figure 7.2.6: CV caparison between different pre-bias conditions.

After an early-stage demonstration of the memory phenomenon, a detailed study in capacitance-voltage measurement is required for the memory behavior investigation. The pre-bias, which seems to play a role in setting the state of the pinMOS memory device, is an essential and frequently-used parameter. If the assumption of its function is correct, the most probable way to fulfill this is by injecting or driving charge flows in the pinMOS memory device, which has a dependence on both voltage value and applied time. Based on the above speculations, a voltage of -15 V was applied to the same device for 5 s as a comparison with the one of -10 V, 60 s (Fig. 7.3.4). Please note that all frequencies used in the rest of the chapter are 100 Hz unless mentioned otherwise.

The hysteretic capacitance behavior, as well as the plateau values of both low and high, remain the same for a pre-bias with larger value bur shorter applied time, indicating the flexible choice of the pre-bias. Although the left curve shifts roughly 0.5 V to more positive voltages, pre-bias with parameters of '-15 V, 5 s' is still regarded to be better than '-10 V, 60 s' due to the comprehensive consideration of less time consuming and acceptable curve shift. Therefore, the standard CV measurement parameters are set to be: pre-bias of -15 V, 5 s; measuring frequency of 100 Hz.

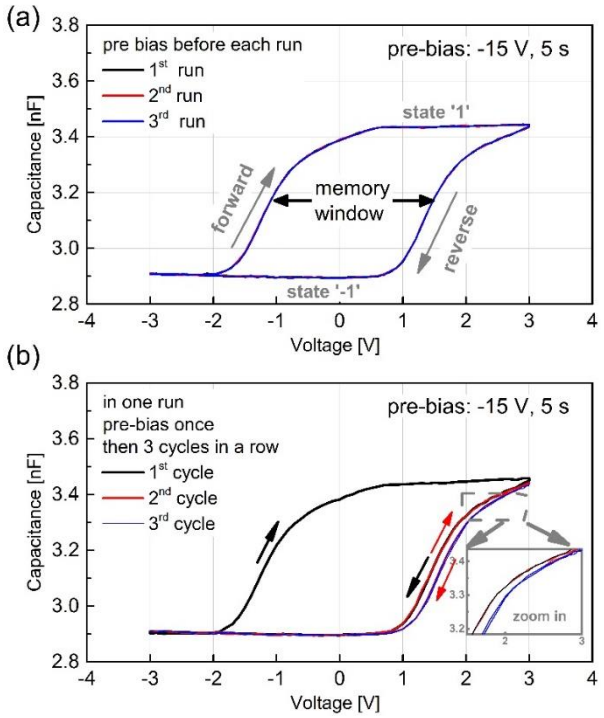


Figure 7.2.7: (a) Three repeated capacitance-voltage (CV) runs and (b) Three continued CV cycles in one run of pinMOS memory after applying a pre-bias of -15 V for 5 s. Insert: Zoom in image of reverse curves.

To verify the data storage capability of the pinMOS memory device, the capacitance-voltage characteristics were investigated as shown in Fig. 7.3.5 (a) by employing the impedance spectroscopy with the standard measurement parameters discussed before. Applying of the pre-bias of -15 V can be regarded as the writing process for bringing the device into a defined state. As previously indicated, with a bias sweep from -3 V to +3 V (forward direction) and back to -3 V (reverse direction) in steps of 1 V, a pronounced hysteresis can be seen with excellent repeatability, as evidenced by the fact that the three consecutive runs of pre-bias and ±3 sweeps perfectly coincide. Following the increase of voltage at the forward direction, the capacitance increases steeply from ~ -1.7 V and achieves a plateau of ~ 3.4 nF at 0.8 V. At the reverse sweep direction, the capacitance of reverse curve drops dramatically to reach steady low capacitance of ~ 2.9 nF at 0.7 V. The 2.4 V voltage difference ΔV gained here between two curves from two sweep directions is the memory window we obtain, which clearly is the result of the charge "information" stored by the application of a pre-bias to the device being erased when the voltage is swept to +3 V. During this cycle, two distinct capacitance plateaus of 3.4 nF and 2.9 nF become apparent at the same 0 V voltage, defined as the state '1'(ON) and '-1'(OFF) of the pinMOS memory device, respectively, while 0 V is referred to as the read-out cvoltage.

The pinMOS memory also possesses a bias-history-dependent capacitance. If the bias sweep was done three times in a row after one initial writing process but without repeating the pre-biasing at -15 V in between, we obtained three different cycle shapes (Fig. 7.3.5 (b)). The full memory window is only visible in the first black cycle and totally gone in the last blue cycle where the state '1' cannot be observed anymore. After the main charge "information" is erased at the end of the first cycle, the following cycles cannot represent the initial full "information" due to the absence of the writing

process (pre-bias application), which will bring charge "information" back to the device. Therefore, the rest cycles only repeat the information left in the last cycle, showing as the forward curves of the subsequent cycles 2 and 3 that coincide with the reverse curves of cycles 1 and 2, respectively (compare colored arrows in Fig 5.3.5 (b) and zoomed inset). The small remaining hysteresis in the 2nd cycle stems from a still not fully completed erasure of the memory during the 1st cycle, whereas no hysteresis can be measured in the 3rd cycle. The magnitude of the threshold voltages for capacitance increase or decrease and their dependence on the measurement parameters will be further discussed below.

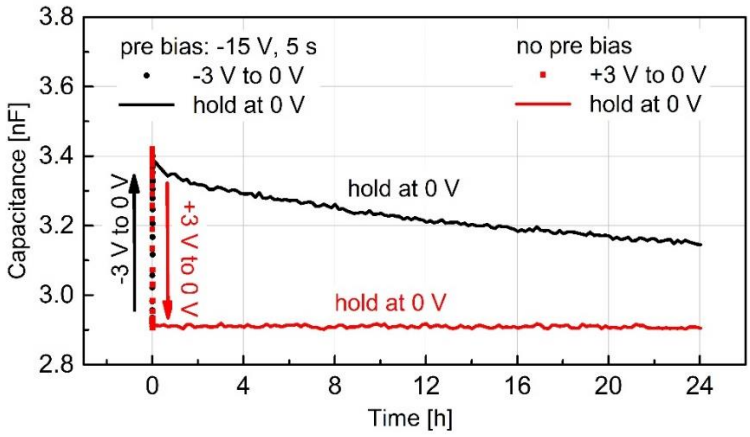


Figure 7.2.8: Retention characteristics of pinMOS memory device.

The memory states of the pinMOS memory devices are nonvolatile and even at this early state development, showing fairly promising retention characteristics, as shown in Fig. 7.3.6. Samples were observed to have better retention after some time of fabrication, which is assumed due to the probably reduction of leakage current over time. Here, we show devices that are two weeks old. Based on the separable extracted capacitance from Fig. 7.3.5 for '1' and '-1' states, 0 V was chosen to be the reading voltage for the retention time test. A -15 V pre-bias was first applied for 5 s to program the pinMOS memory device to the written state. Then a single voltage sweep was taken from -3 V to 0 V followings the previous CV measurement, and subsequently the capacitance at state '1' at 0 V was being recorded as a function of time in intervals of 10 min. The state '1' capacitance exhibited a slow decrease from initial 3.40 nF to 3.15 nF in over the course of 24 h. For the equivalent test for state '1', a positive voltage +3 V was supplied to the same device for several seconds to completely switch it to state '-1' before the voltage was swept back from 3 V to 0 V and held there. Additional writing pre-biases were not applied anymore. Under this state, the reading capacitance at 0 V maintains excellent with a slight fluctuation over 24 h. The capacitance of both states can be well distinguished over 24 h, as well as maintained at least 93% of the initial charge "information", suggesting a stable charge-storing retention capability.

Please note that during this measurement, the measurement equipment encountered was consciously connected all the time to the device for simulating the environment in realistic applications, which basically allows the device to discharge at any time. Meanwhile, the time interval for each data extraction plot is 10 min, much shorter than 0.5 h or even hours from literature which claims days or months of retention time [202][221]. Furthermore, the memory devices in a lot of literature that

based on a charge up of an internal reservoir (e.g., folating gate memeory, memory with charged-up nanoparticles), are commonly electrically connected and probed only intermittently (point-wise) over a long time span. The performance deviation for the same device lies between our measuring method and some literature method. The latter way of assessing retention time leads to artificially inflated values, since without electrical connection leakage currents that destroy the stored information cannot flow. However, for our pinMOS memory case, it fits the industry working environment. Regarding the performance, although the leakage current is more apparent due to all-time connection and short measuring intervals, pinMOS memory still exhibits stable 24 h retention time and the potential of extending to days or even months under more favorable measurement conditions.

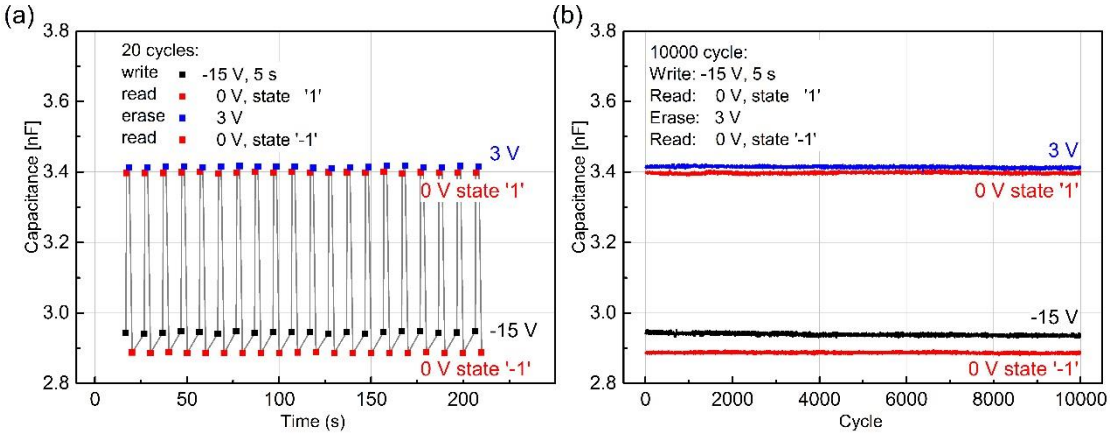


Figure 7.2.9: Cyclic sweep endurance of a pinMOS memory device.

As seen in Fig. 7.3.7, the reliability of the pinMOS memory device was also investigated via cyclic sweep endurance by measuring the reading capacitance after the application of circular writing/erasing biases. The cyclic sweep is completed with a writing process of applying -15 V for 5 s, following with the reading at voltage 0 V and then erasing the information at 3 V before another 0 V readout shown in Fig. 7.3.7 (a). The two states of the pinMOS memory can be clearly distinguished even after 10^4 cycles without many fluctuations, revealing a reliable endurance characteristic (Fig. 7.3.7 (b)).

The reliability of the memory device is crucial for nonvolatile data storage. The easy fabrication capacitive pinMOS memory device presents excellent performance with an endurance of up to 10^4 cycles and a retention time of over 24 h at this early stage with crucial measuring conditions. Such outstanding performances hold great potentials for future information storage.

7.3 Working mechanism

The basic functions of pinMOS as a memory device have been demonstrated in the previous sections. For a further exploration of the functions and properties, the working mechanism and companied capacitance variation need to be discussed.

7.3.1 Working mechanism of quasi-steady states

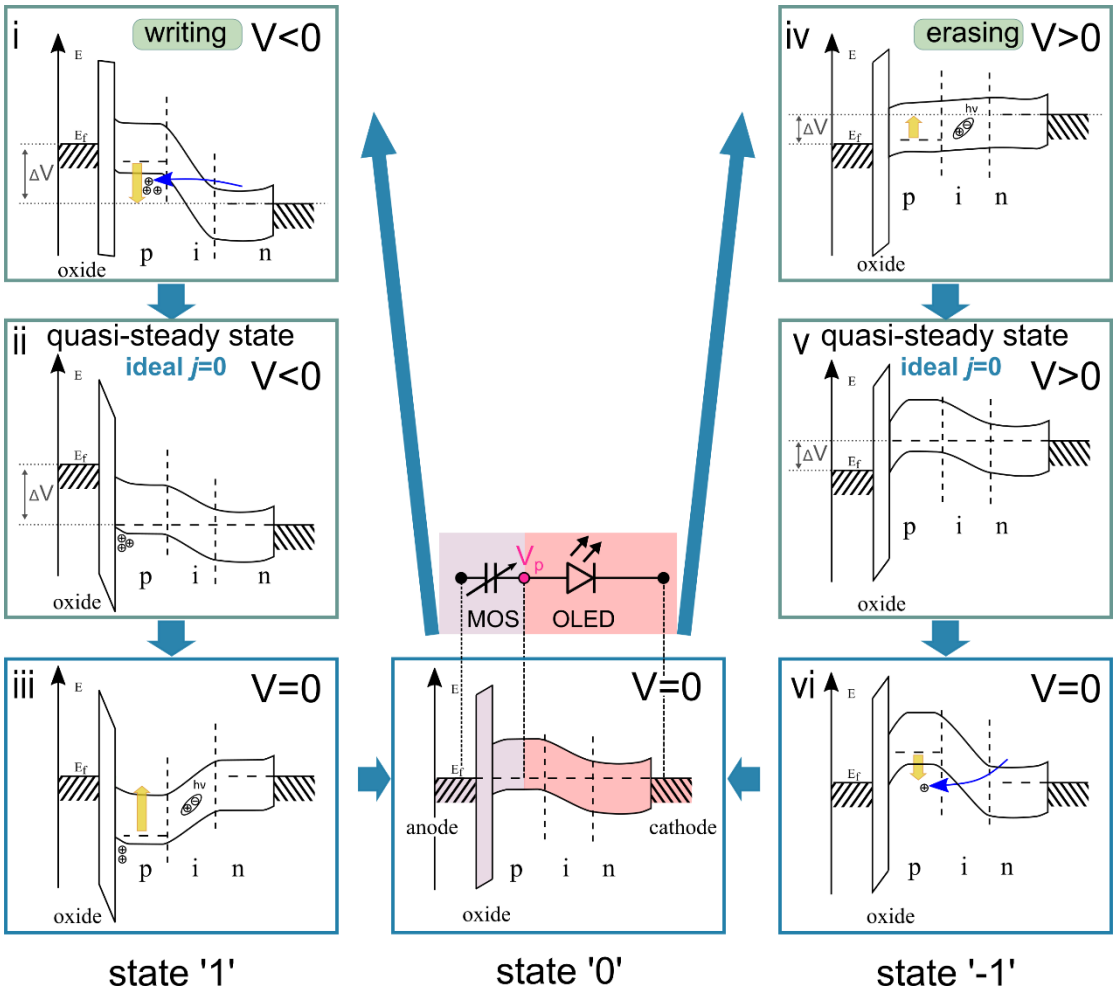


Figure 7.3.1: Overview of working mechanisms in pinMOS memory.

Assumption To better understand how information is stored and released by the pinMOS memory, it is helpful to not only look at the static bias-free states, but also consider the quasi-steady states when applying one negative or positive voltage consistently (Fig. 7.4.1). First, we have to assume that the 50 nm p-doped layer with high conductivity, which is embedded between the 50 nm insulator and 40 nm intrinsic layers, will never be entirely depleted at any of the voltages applied here. Therefore, there is always a region, which is possibly thin, in the p-doped layer that retains the original concentration of free charge carriers and is able to hold its own potential. Based on this assumption, the left and the right side of the p-doped layer can now be treated as two decoupled parts, accounting for the pinMOS memory that can be understood as two series-connected individual elements: a MOS (metal-oxide-semiconductor) capacitor and an OLED as visualized in Fig. 7.4.1 in the middle. Since the p-doped layer decouples itself and thus the pinMOS memory into two elements, the local potential of the undepleted region of the p-doped layer can be defined and symbolized as Vp as shown in the middle circuit schematic in Fig. 7.4.1. Then, as indicated by V_p, the Fermi level in the undepleted p-doped layer can be utilized as a reference to define the voltage that drops over the insulator in the left side of the device (MOS element) as well as the p-i-n structure

in the right side of device (OLED element), respectively. Based on the above descriptions, the working mechanism can be explained in more details.

Initially, before applying any bias, the memory device is in the initial state '0' as shown in Fig. 7.4.1 middle, where the device is in full thermal equilibrium with its environment, i.e., the Fermi level is entirely flat and V_p equals the externally applied potentials.

Writing process The writing process in Fig. 7.4.1 left is first discussed as a start: once we apply a negative voltage to the pinMOS memory, the Fermi level of the anode, as well as the n-doped layer in the OLED element, will first increase with respect to the cathode as shown in Fig.5.4.1 (i). However, the Fermi level of the p-doped layer in the MOS capacitor and the corresponding defined V_p remains the same. The voltage difference ΔV between the Vp and the potential of anode is the voltage applied. Nevertheless, with continuous voltage supply, this non-equilibrium situation will tend towards quasi-equilibrium and eventually result in a new quasi-steady state at which no current can flow as the insulator is assumed to be ideal for blocking any flow of carriers between the semiconductor and the metal at all voltages. The only case in which no current flows in the p-i-n structure is when there is no potential drop over it, as schematically shown in Fig. 7.4.1 (ii). Thus, it is essential to realize that any externally applied voltage drops over the insulator entirely in the idealized quasi-steady state. In other words, the initial V_p in subfigure (i) has to go through the process of approaching to the potential of the cathode as illustrated by the yellow arrow. To increase the potential of V_p, there has to be a charge exchange in the p-doped layer, either holes injection or electrons extraction. Here as the band energy illustrated, Zener tunneling effect within the p-i-n junction which tunnels holes from the conduction band in the n-doped layer to the valence band in the p-doped layer, is the only realizable way to change the electric potential difference in the pinMOS memory.

The tunneling effect is often used in organic memory devices for carrier injection into the device, especially for the floating gate memory devices [202], [220], [222]. In our pinMOS memory case, a significant potential drop across the OLED element in the reverse direction just after switching the device to a large negative voltage, results in the Zener tunneling effect which leads to holes tunneling into the p-doped region [83], [222], [223]. While the holes accumulate in the p-doped layer close to the insulator side, the Fermi level of the p-doped layer gradually lowers from case (i) to case (ii) of Fig. 7.4.1, left, pursuing the quasi thermal equilibrium. Once the applied voltage is reduced back to 0 V (Fig. 7.4.1 (iii)), the remaining potential across over the oxide will be as big and but opposite to the voltage drop over the p-i-n stack. As a consequence, the OLED element of the device will be biased in the forward direction, i.e. charges will flow into the intrinsic region, recombine, emit light, and exhausted.

Since the pinMOS memory is a device based on an OLED, one key to understanding its operation is to consider the IV behavior of the orginal OLED device as the approximate IV curve for pinMOS, regardless of the coordinate axises. The current-voltage characteristics as shown in Fig. 7.4.2, could represent the current flow behavior in the OLED part of the pinMOS memory qualitatively. The asymmetry in OLED current density indicates different behaviors of pinMOS memory when the incorporated OLED element is biased in different directions.

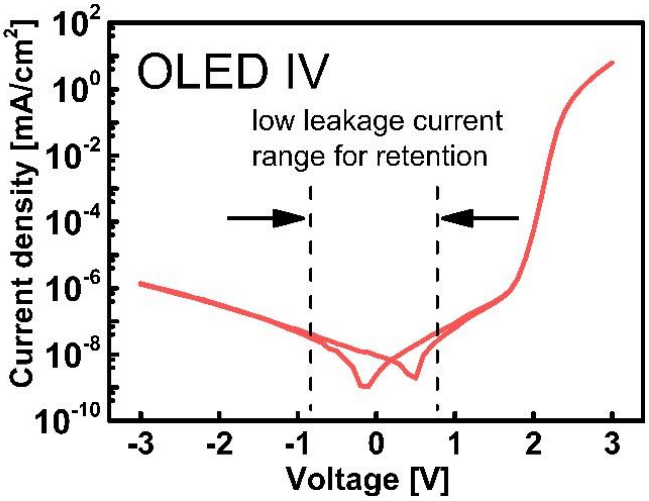


Figure 7.3.2: I-V characteristics of individual OLED element.

A high current density can be observed when the OLED is operated with positive voltages shown in Fig. 7.4.2, especially when the voltage is high than ca. 1.8 V. The high current density will be reproduced in the pinMOS memory device when the incorporated OLED element is biased in the forward direction like the case (iii), i.e., the currents in the OLED element flow from the p-doped layer to the n-doped layer. Meanwhile, the V_p in this case is readily relaxing towards the potential of the cathode, which is 0 V herein, to build another equilibrium state by charge exchange. However, the potential drop over the p-i-n structure also shrinks rapidly with the fast decrease of V_p, leading to a sharp or even exponentially decrease of current flow as well. Once the current density is lower than the level of leakage current density range like the dashed line demonstrated in Fig. 7.4.2, a further discharge of the pinMOS memory will be almost stopped since only the negligibly small dark leakage current flow in the OLED element forward direction remains as the reason for charge exchange. The time consumed from the "stressed" state '1' in the case (iii) to the initial state '0' in the case middle is then the retention time of the pinMOS memory discussed before, which mainly depends on the leakage current through either the oxide insulator or the p-i-n structure.

Erasing process After considering the writing process, we now discuss the erasing process as shown in Fig. 7.4.1 right: unlike the writing process that requires a high external voltage and thus high electric field for activating the Zener tunneling effect, a small voltage is sufficient for operating the erasing process. When a small positive voltage is applied to the pinMOS memory in the state '0' (initial state), charges are injected into the OLED element, holes from the p-doped layer and electrons from the cathode (Fig. 7.4.1 (iv)). The charges form excitons that radiatively recombine and photons are emitted, companied by currents that flow in the forward direction since the OLED element is biased in the forward direction in this case. However, the ideal insulator blocks the carrier injection from the anode and then eventually results in holes exhaustion in the p-doped layer close to the oxide layer, which creates a growing depletion region towards the p-side of the OLED. Similar to the writing process, in order to be in a new quasi-steady state '-1' in Fig. 7.4.1 (v) without internal current flow, the full external potential has to drop over the insulator layer. Meanwhile, the V_p in subfigure (iv) has to change according to the potential of the cathode, also showing as a raise of the Fermi level of the p-doped layer revealed by the yellow arrow. During the process of approaching

the quasi-equilibrium (case (iv) to case (v)), the OLED element keeps operating in the forward direction, so that erasing can be quite fast since high current densities are easily achieved in the forward direction of the OLED element as indicated by Fig. 7.4.2.

If the applied voltage is reduced back to 0 V, the internal potential drops in turn over the p-i-n stack of OLED element will now be in the reverse direction as demonstrated in Fig. 7.4.1 (vi). Considering the small dark current density in the reverse direction of the OLED element, the repopulation of holes back into the p-doped layer will be very slow. The destruction of state '1' will be caused by any process that leads to hole transport back to the p-doped layer, e.g., light absorption, Zener tunneling, or generally leakage through either the oxide insulator or the p-i-n junction.

Short summary The working mechanism discussed above suggests that the information storing (writing) and releasing (erasing) processes of the pinMOS memory rely on the internal potential V_p. Due to the presence of the insulator, all electrical currents that flow after an external bias potential is applied, will flow in the p-i-n stack exclusively (apart from leakage through the insulator) which will, no matter which sign of external potential is applied, lead to quasi-steady states in which the applied potential eventually drops entirely over the insulator. The current characteristics during writing or erasing processes is shown in Fig. 7.4.3. In both cases, a typical charging curve of capacitor is observed that has the highest current at the beginning and then the current decreases over time. The current drops until it reaches the limitation of the measurement equipment (Source-measuring unit model Keithley 2635) at a magnitude of 10^{-12} A. Still, we can see that writing at -15 V is not as efficient as erasing at +3 V because the curve decays slower. This observation is in agreement with our memory measurement that shows that we have to apply the high writing voltage of -15 V much longer than the erasing voltage of +3 V.

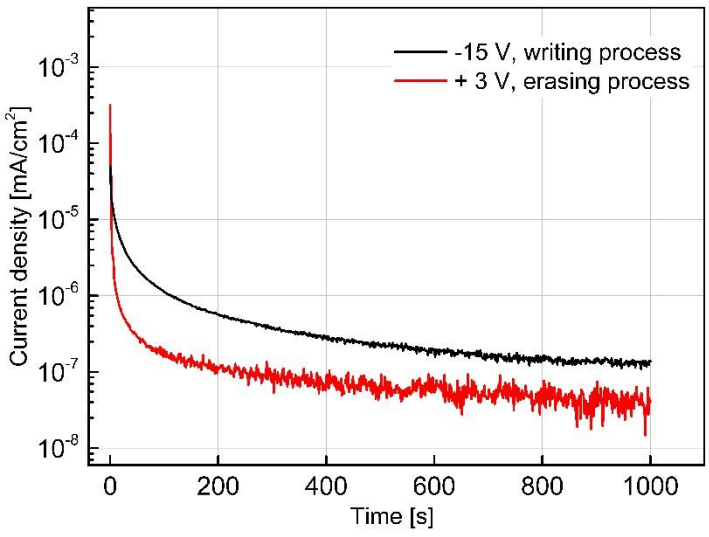


Figure 7.3.3: Current density as the function of time during writing and erasing processes.

The complete process can be understood as a destruction and reconstruction circulation of equilibrium states. Depending on the sign of the external voltage and the status in which the device is, the MOS capacitor and OLED (p-i-n junction) element are operated in varied directions separately as listed in Tab. 7.4.1, generating different magnitudes of internal current density and thus different period of the process. Especially for the OLED element, its reverse operation direction in case (i) limits the writing speed of the integral pinMOS memory device as well as requires high writing voltage.

Process	Status Transformation	Element	
		MOS	OLED
Writing process	i to ii	F	R
	ii to iii	F	F
Erasing process	iv to v	R	F
	v to vi	R	R

Table 7.3.1: Operation direction for MOS and OLED element in the different processes. F is short for the forward direction while R is short for the reverse direction.

These assumptions are based on an idealized scenario. In reality, any leakage currents through the insulator will prevent the internal potential V_p to be fully aligned with the potential of the cathode in the quasi-steady states. Nonetheless, the qualitative description of the idealized case remains valid also for the real device.

Reading process Besides the writing and the erasing processes, the readout of the actual device state is also crucial. Reading basically means to distinguish between state '1' and state '-1' at a chosen voltage, e.g., 0 V. Based on the working mechanism discussed above, there are two possible readout methods: i) readout of the capacitance difference at different states. and ii) checking whether light emission occurs with forward bias application. The first method will remain the device state while the second is destructive, i.e., may switch the state from '-1' to '1'.

7.3.2 Working mechanism of dynamic states

From the quasi-steady states working mechanism, the processes of writing and erasing the pinMOS memory device are accompanied by a series of behaviors including hole accumulation and hole depletion in the MOS capacitor, Zener tunneling and carrier recombination in the p-i-n stack. Therefore, the capacitance of integral pinMOS memory varies as the two voltage-dependent capacitances from the two abstract device elements, the MOS-capacitor and the p-i-n junction, vary during the writing and erasing processes. Due to the series connection of both sub-device capacitors (MOS-capacitor, p-i-n junction), they contribute differently to the total device capacitance, i.e., the lower one will predominantly define the device capacitance that we can measure by the impedance spectroscopy.

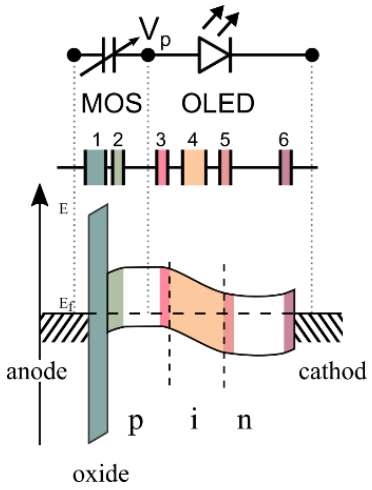


Figure 7.3.4: Schematic for capacitance contribution.

The capacitance form two sub-devices can be further divided into six different contributors, including two dielectric layers (1, 4) and four depletion zones (2, 3, 5, 6) as numbered and colored in Fig. 7.4.4, respectively. The device capacitance varies from 2.9 nF to 3.4 nF in one complete voltage sweep, although the capacitances from oxide (region 1) and intrinsic layers (region 4) stay the same. Furthermore, as the working mechanism illustrated in Fig. 7.4.1, the Schottky barrier between the n-doped layer and cathode remains the same even when the total device capacitance differs. Thus the capacitor contribution from the region 6 can be excluded for the primary cause of capacitance variation. Therefore, the nano-Farad scale modulation of the capacitance in the voltage sweep process results from the variable depletion zones in the incorporated doped layers, which are numbered as region 2, 3, 5 in Fig. 7.4.4.

As the quasi-steady states working mechanism indicated, the capacitance difference between state '1' and state '-1' at 0 V is a result between holes accumulation and depletion in the p-doped layer of the MOS element, as referred as the region 2 in Fig. 7.4.4. However, this explanation is more applicable to a pulse measurement, where the applied voltage has a certain duration time for reaching the quasi-steady states. Regarding the CV curves we obtained with dynamic voltage sweeps, the dominating capacitance contributors may not be the depletion region close to the oxide layer (region 2) anymore. A circumstantial evidence is the closed-loop we gained in all CV curves, which cannot be explained by the hole accumulation and depletion in the region 2: if the hole accumulation results in the high capacitance and hole depletion leads to the low capacitance in the swept CV curve, the capacitance for the forward curve with accumulation regimes should stay in high until the erasing voltage +3 V is reached, i.e., the capacitance at -3 V measured right after the pre-bias application should be 3.4 nF instead of 2.9 nF, and a full CV cycle should be open at negative voltages. Therefore, the capacitance variation is likely coming from the width change of depletion zones shown as region 3 and 5 in Fig. 7.4.4.

A simplified calculation is estimated to prove the rationale behind above assumptions. From CF curves in Fig. 7.3.1, the capacitance of the oxide layer C_{oxide} and intrinsic layers C_i is extracted as 7.3 nF and 4.8 nF, respectively. The thickness of the intrinsic layers is fabricated to be 40 nm. Due to the diffusion of carriers, the width of the space-charge region that is generated by the depletion in

the p-i-n junction decreases (will be explained later in detail), and is eventually assumed here to be 30 nm, resulting in a new intrinsic layer capacitance C_{i_new} of 6.4 nF.

Thus, the low plateau capacitance can be calculated with an accumulated region 2 as:

$$C_{low} = \frac{1}{\frac{1}{C_{oxide}} + \frac{1}{C_i}} = \frac{1}{\frac{1}{7.3} + \frac{1}{4.8}} = 2.9\ nF \tag{7.3.1}$$

While the high plateau capacitance is:

$$C_{high} = \frac{1}{\frac{1}{C_{oxide}} + \frac{1}{C_{i\_new}}} = \frac{1}{\frac{1}{7.3} + \frac{1}{6.4}} = 3.4\ nF \tag{7.3.2}$$

which matches the data gained from the experiment with the low plateau being at 2.90 nF and the high plateau being at 3.44 nF. If we also include the depletion region of the p-doped layer at the oxide interface for the high plateau calculation, the C_{high} will be ca. 3.3 nF, based on the 6.8 nF capacitance at 100 Hz extracted from the oxide-p-doped layer device in Fig. 7.2.3. Again, close to the experimental value of 3.44 nF. Although this calculation is a simplified situation of an ideal accumulation-depletion case, the resulting simulated capacitances are within a reasonable range relative to the experimental data, proving the assumptions we made for the working mechanisms of dynamic states during voltage sweep. The voltage-dependent capacitance variation in the p-i-n junction sub-device drives the dominating device capacitance variation in the voltage sweep process.

To discuss the working mechanisms for the pinMOS memory integrally under dynamic states, we now focus on the p-i-n junction, including intrinsic layers and depletion zones of the incorporated p- and n-doped layers (Fig. 7.4.5). This sub-regime, which is region 3, 4, 5 in Fig. 7.4.4, is colored as one for easy understanding as shown in Fig. 7.4.5 (a).

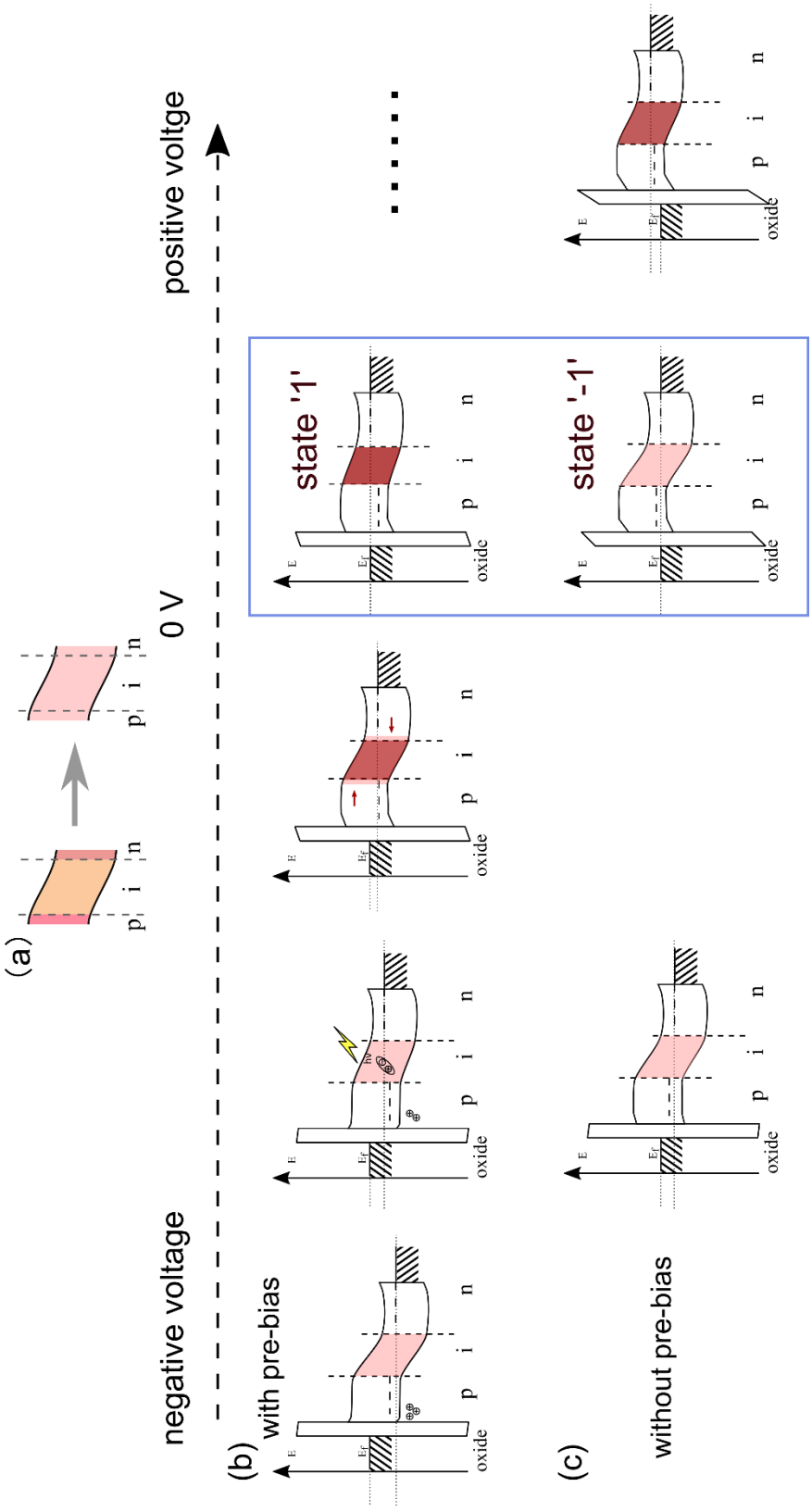


Figure 7.3.5: Overview of working mechanisms in pinMOS memory under forward sweep voltage (a) with or (b) without application of pre-bias.

Two different cases will be discussed during the voltage sweep process. The first case is the one in Fig. 7.4.5 (b) with the pre-bias application. The p-doped layer in this case has excessive amounts of holes generated via Zener tunneling and holds the low capacitance. The Zener tunneling of HOMO band electrons from the p-doped region into the n-doped region replenishes the hole concentration in the p-doped region, thereby leaving sufficient amount of hole in the p-doped layer region. With the voltage sweep from negative to positive (forward direction), the excess holes (compare to the initial state before pre-bias application) enables charges that flow back and recombine at negative voltage. Therefore, the OLED element will be turned on with light emission before 0 V. The width difference in depletion zone results from the hole exhaustion near the oxide layer that has a small fluctuation influence to the total device capacitance as discussed above. Nevertheless, the two space charge zones, which are adjacent to the intrinsic layers at the two sides, will be narrowed due to the increase of external potential, resulting in capacitance increase from 2.9 nF to 3.4 nF and eventually stays at the high plateau state '1'. The switch between state '-1' to state '1' is repeatable as long as there are excess holes for recombination during the forward sweep direction.

If there is no pre-bias application after holes exhaustion, the situation for the same forward voltage sweep process will be as Fig. 7.4.5 (c). Both the large built-in potential and the lack of holes fail to guarantee the light emission under negative voltage as in the case with the pre-bias application, which will be discussed in Chapter 8. Furthermore, the width of the space charge zones near the intrinsic layers will not decrease until a comparable high positive voltage, e.g., + 0.8 V, is applied to the device. Therefore, the capacitance of the device stays at the 2.9 nF low plateau before 0.8 V, resulting in the memory window we obtained in the general ±3 V sweep. At the same reading voltage shown in the purple frame in Fig. 7.3.5, the pinMOS memory with pre-bias achieve the state "1" with significant higher capacitance, while the case without pre-bias stays at the state "-1" with low capacitance. For the device without pre-bias, the voltage-dependent width variation and the accompanied capacitance variation during the sweep has a voltage symmetry, i.e., the forward and reverse curves will overlap with no hysteresis, which is proven by the disappearance of the memory window in blue curves in the Fig. 7.3.5 (b).

One important information is hidden behind this working mechanism: the threshold voltage for capacitance increase during the forward sweep is precisely the voltage for light emission in the OLED element. Therefore, by varying the number of accumulated holes via changing writing parameters like voltage duration or voltage value, the threshold voltage and corresponding forward curve can be tuned.

7.4 Tunability of the memory effect

As discussed in Section 5.4, one attractive property of the pinMOS memory device is its potential to store multiple bits, i.e., the tunability of the memory window based on changes to the operation parameters. Furthermore, with the same process conditions, the memory window can still be tuned by varying the intrinsic layers thickness, which affects the tunneling effect as well as the width of space charge zones according to proposed working mechanisms.

7.4.1 Operation parameters

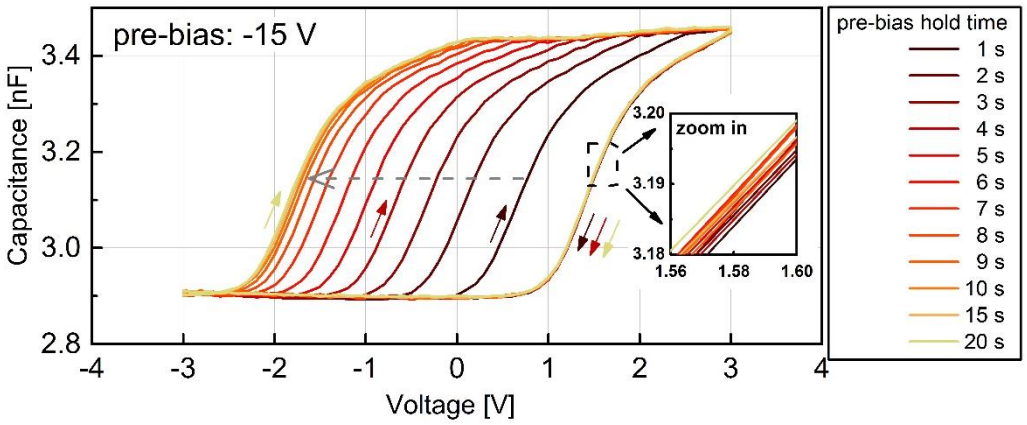


Figure 7.4.1: CV curves measured under same pre-bias -15 V but different hold time. Inset: Zoom in image of reverse curves.

For example, under the same '-3 to +3 to -3 V' sweep range in Fig. 7.5.1, the threshold sweep-voltage for capacitance increase in the forward sweep direction can shift from 0 V to -2.5 V by varying the hold time of the pre-bias (-15 V) from 1 s to 10 s. Since the field strength over the p-i-n junction remains the same with the fixed writing voltage, the amount of extra holes is decided by the duration of tunneling processes, i.e., longer hold time in the writing process results in more accumulated holes. As the dynamic states mechanism indicates, hole accumulation situation is the main factor for determining the threshold voltage for capacitance increase in the forward sweep. Therefore, the forward curve will shift horizontally towards the negative voltage with the increase of the pre-bias hold time. Nevertheless, instead of being directly proportional to the hold time, the intervals of forward curves gradually become smaller with the increase of hold time. This is because of the unavoidable reconstruction process of quasi-steady state revealed in Fig. 7.4.1 from sub-figure (i) to (ii), in which the potential that drops over the p-i-n junction, as well as the field-dependent tunneling effect, becomes smaller or weaker. Eventually, the expansion of the memory windows will be limited, showing as the similar curve behavior between the device with the long hold time of 15 s or 20 s and the one with shorter time of 10 s. For the erasing process, the overlap of the reverse curves demonstrates the effectiveness of the application of the erasing voltage of +3 V to erase the memory (Fig. 7.5.1, inset).

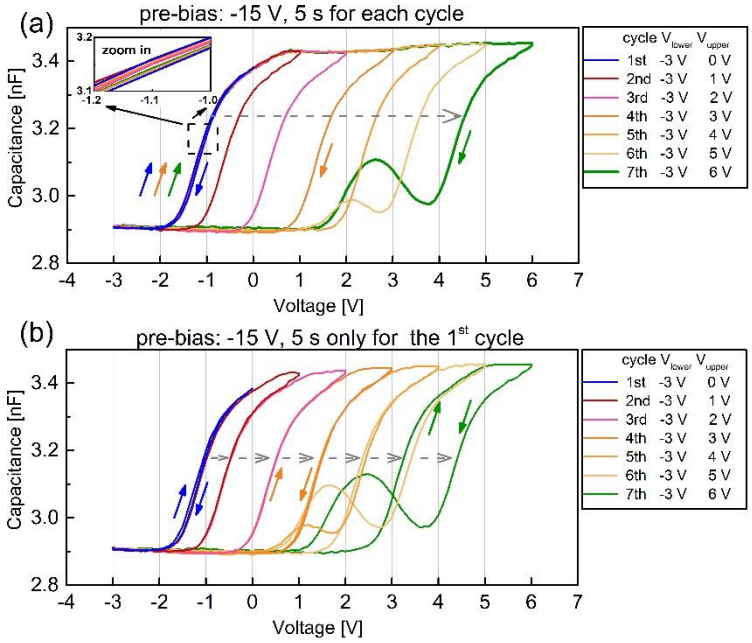


Figure 7.4.2: CV curves swept under different ranges with applied pre-bias (a) for each cycle or (b) only for the 1st cycle.

Another possibility to modulate the amount of charges stored in the devices is to vary the upper sweep voltage as shown in Fig. 7.5.2 (a) to manipulate the erasing process. Opposite to the curves from the hold time variation, the reverse curves now horizontally shifted to more and more positive voltages while the forward curves remain the same and overlap. The overlap of the forward curves can easily be understood as the excellent forward curve reproducibility with the same writing process, while the shift of reverse curves is a combination of several processes. After reaching the high plateau at ca. 0.8 V, the high capacitance of the device will be held as long as the applied voltage is increased continuously. Although the device is under the voltage sweep with dynamic states, the approaching of the '-1'quasi-steady state shown in Fig. 7.4.1 (v) is ongoing, despite being incrementally destroyed by the increased external voltage. The electron injection from the increased voltage promise the width of the space charge zones and somehow holds the balance for leaving away of influence from the nature of achieving the quasi-steady state. However, once the positive voltage decreases, the balance will be broken and a rapid drop of the capacitance due to the broader space charge zones will occur and as visible as the reverse curve. Regardless of the hold time or the sweep range, both the high and low capacitance plateaus of the series of curves remain the same. Nevertheless, the capacitance value has so many complicated variables that some phenomena like the hump that occurs at the reverse sweep direction for high upper voltage of 5 V or of 6 V are unclear currently and cannot be explained at the moment.

The information stored in the device by the application of the initial writing process can be released in fractional amounts via different sweep ranges, giving rise to what is in principle multiple-bit storage (Fig. 7.5.2 (b)). After a defined state '1' was written by an initial pre-bias -15 V, 5, a cyclic sweep with lower voltage -3 V and upper voltage of 0 V was applied to obtain the 1st cycle. Further sweeps without additional pre-bias application were performed with the same lower voltage -3 V but stepwise varied upper voltage from 1 V to 6 V. The sequential positive shift of the memory

windows proves that the device information is preserved between the previous reverse cycle and the next forward cycle. With the increase of the upper cycle voltage, more and more of initial stored information is "released", corresponding to a gradual shift of both forward and reverse curves. For any individual curve in the pinMOS memory, it can extract the "old" information by reproducing the last reverse curve, and then display the "new" information as well as leaving it for the next sweep.

Comparing the curves with the same sweep range in Fig. 7.5.2 (a) and (b) one by one, the reverse curves from the same sweep range behave similarly although the forward curves differ. However, the initial forward curves with pre-bias application beforehand are again the same for both experiments. A conclusion can be that the amount of charge left in the device decides the forward curve behavior, while the upper voltage limits the reverse curve behavior.

7.4.2 Photoinduced tunability

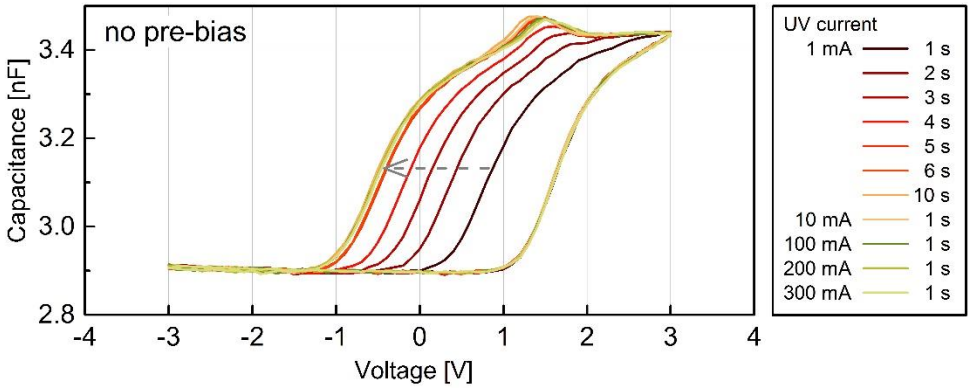


Figure 7.4.3: CV curves measured under a pre-illumination of UV light.

According to the working mechanisms, one of the reading methods is readout by light, i.e., upon the application of forward bias, the light emission only comes out if the pinMOS memory device was in the state '1', which will be examined in details in the next chapter. If we can read out the information by visible light emission, it would be exciting and for certain applications also highly desirable to be able to write the device by light as well.

To demonstrate the basic function of this concept for our pinMOS device, an ultraviolet (UV) LED with a wavelength of 375 nm, which is known to create free charge carriers in our general stack of red OLEDs, was used as the UV light source [224]. By pre-illuminations, a series of memory windows can be obtained in Fig. 7.5.3 with different but functionally working memory behaviors. The illumination intensity that is controlled by the UV LED current and the duration of the exposure have an evident influence on the shape of the CV curve. This programmable writing effect is similar to applying a high negative electrical bias with the most significant difference that instead of Zener tunneling, a full process of band-to-band excitation, electron-hole pairs generation (in the intrinsic layer), and then hole extraction under the UV illumination controls the holes population in the p-doped layer. Despite different writing mechanism, the primary memory behavior remains the same for both cases. Except for the hump at the high-capacitance plateau around 1.3 V, the CV curves have similar behaviors in forward curves seriatim shifting and reverse curves stabilization as voltage

stimuli curves. Furthermore, compared to the electrically obtained CV curve hysteresis, the capacitance values of both low and high plateaus remain unchanged, although the hole regeneration mechanism in the p-doped layer is different. This confirms that two series-connected sweep-voltage dependent capacitances, namely those of the MOS-capacitor and the p-i-n junction are not generally affected by the writing method.

For the UV light stimulation, exposure to the UV light from the UV LED driven at 1 mA for 1 s already generated enough carriers for observing a memory window of 1 V. The intensity exposure directly to the device is ca. 8×10^{-2} mW/cm^2 under 1 mA. The most pronounced memory window could be achieved under a 1 mA UV LED for 5 s. Any further increase in light intensity or duration time will not change the saturated memory window. Although the maximum memory window (2.0 V) obtained from UV illumination is smaller than the one obtained electrically (2.4 V), a controllable memory behavior can still be obtained through UV irradiation. The reason for the hump in the high-plateau at 1.3 V is unclear, but it amplifies the capacitance difference between the '1' and '-1' state at this specific voltage instead of eliminating the information. Such a hump is both "well repeatable" and "removable", i.e., it is overlapped for saturated curves stimuli with different illumination conditions, and will disappear when the device is measured again after an electrical writing by pre-bias.

Since the pinMOS memory can be programmed by optical stimulations and readout by electrical operations or even light signal, it can, in principle, be used as an optoelectronic organic memory device for neuromorphic vision sensor. Furthermore, the pinMOS memory shown in Fig. 7.5.3 is able to output light-dosage-dependent (i.e., light-dependent characteristics based on both light intensity and illumination time) and history-dependent capacitance states, for which holds promise for optical storage. One hint is that the light intensity tunability and duration dependence behavior in ways like sensing information as neural signals with light-tunable and time-dependent plasticity [225]. Moreover, not only the capacitance switched by sensing applied UV light, but the emission possibility is recorded in the pinMOS memory, thus realizing the detection, memory and exhibition capacities all by the light. Combined with a photodetector, the sensed image through UV illumnation can directly be represented by the human visible red light [226].

7.4.3 Intrinsic layer thickness

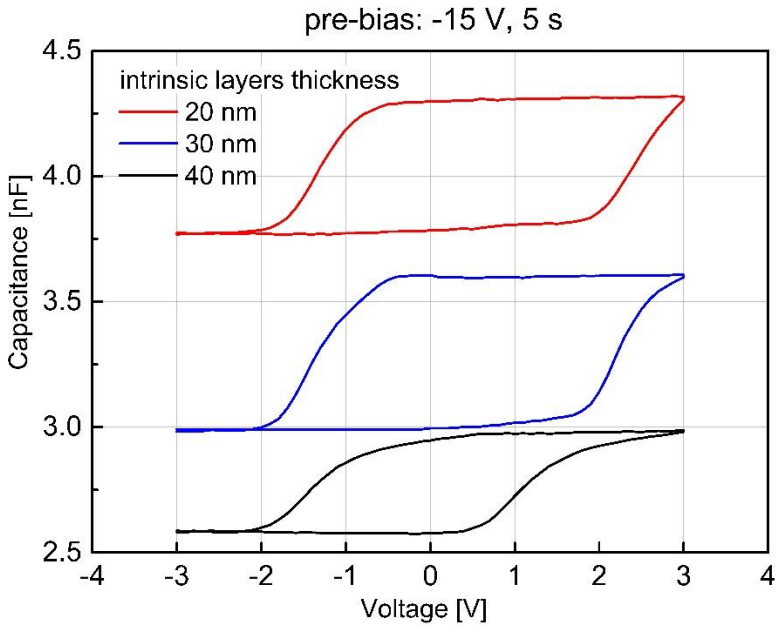


Figure 7.4.4: CV curves operated with the same parameters for pinMOS memory devices but different intrinsic layer thickness.

The thickness of intrinsic layers, which decides the field strength across the p-i-n junction at the same potential drop, is essential to be studied in detail. The intrinsic layers used for pinMOS memory are composed of three different layers: an electron blocking layer (EBL) at the p-doped layer side, an emissive layer (EML) sandwiched in between, and a hole blocking layer (HBL) at the n-doped layer side. For all devices used above, two blocking layers are 10 nm while the emissive layer is 10 nm, summed up to be 40 nm. To obtain a higher field strength and thus more effective tunneling effect according to the proposed working mechanisms, the thickness of the intrinsic layers was reduced to 30 nm (5 nm for EBL and HBL, 20 nm for EML) and 20 nm (5 nm for EBL and HBL, 10 nm for EML) and then compared with the 40 nm case as shown in Fig. 7.5.4. The three devices with varied intrinsic layers, including the 40 nm reference device, were fabricated from the same Lesker run to minimize the run-to-run difference. For the 40 nm reference device (black curve), it behaves similar to the same 40 nm but different Lesker run produced device used in the previous sections with the same 2.4 V memory window, same trends for both forward and reverse curves, but different plateau capacitances. However, if we accept the 2.6 nF as the new thickness reference for the low plateau and calculate the values for the other two devices in terms of $C = \frac{\varepsilon_0 \varepsilon_r A}{d}$, the gained 3.1 nF and 3.8 nF is close the experimental 3.0 nF and 3.8 nF obtained in Fig. 7.5.4. Therefore, the thickness variation data still are comparable, although there is a run-to-run difference of unknown origin.

All devices show the basic voltage-dependent capacitive memory effect. With the decrease of intrinsic layer thickness, the low capacitance increases in an inverse ratio, and same to the corresponding high capacitance. Surprisingly, the threshold voltage for capacitance increase does not shift much. However, the curve steepness in both the increasing forward direction and decreasing

reverse direction becomes larger in the thinner devices, eventually results in a larger memory window. Meanwhile, in the same voltage sweep rage, the rapid capacitance increase and decrease also broader the voltage ranges for keeping in state '1' and '-1', respectively. For the sake of increasing responsiveness of the capacitance change, the intrinsic layer thickness can be designed to be thinner in the future.

7.5 Potential in neuromorphic computing application

In literature, most studies focus on using resistance-switching non-volatile memory for storing and releasing information, some of which can be used in artificial neural networks as neuromorphic devices [227]. By electrical switching, they show rich hysteretic IV characteristics which, in effect, are memristive behaviors and the devices are referred to as memristors [21]. The pinMOS memory devices studied in this chapter have similar electrical switching, but showing as capacitance instead of resistance, demonstrating another type of memory device—the memcapacitor. Memcapacitor-based circuit can significantly lower the static power of the circuit as well as mimic the neural functionalities better since the signal is expressed as a voltage rather than a current [26]. Therefore, the novel non-volatile pinMOS memory device has potential building the capacitive artificial neural networks if it can emulate neural functionalities, including long-term plasticity (LTP), short-term plasticity (STP), and spike timing dependent plasticity (STDP) [228].

In this section, an early-stage investigation on the mimicking of some of these basic features of synaptic plasticity was done for pinMOS memory.

7.5.1 Extracting capacitance at 0 V sequentially

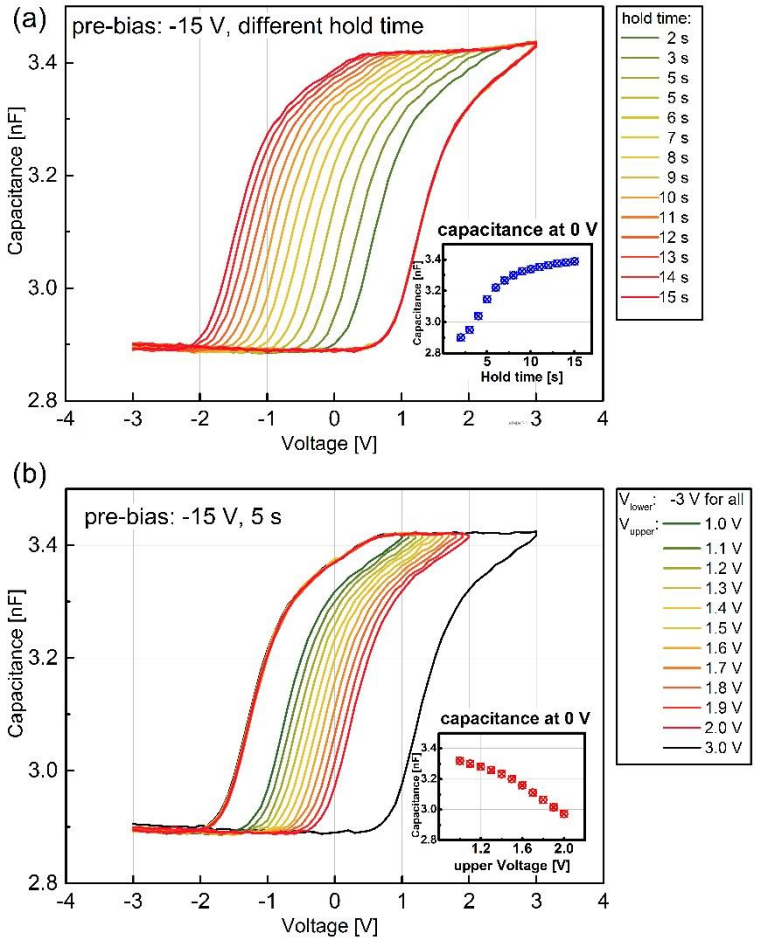


Figure 7.5.1: CV curves show the capability to store multiple bits by incremental adding or removal of charges. Insets: capacitance continuously increases or decreases at 0 V with different operation parameters.

The storage capacity of multiple-bits has been proved in the previous sections by showing the shift of the memory window. However, in order to demonstrate the multiple-bit application in neural networks, more precise control over the memory windows with a specific range is needed to obtain a series of capacitance bits at the same reading voltage. There are at least two possibilities for extracting a series of continuous capacitance values at the same reading voltage: vary the hold time of the pre-bias in the writing process to store different amounts of charges (Fig. 7.6.1 (a)), or vary the upper (erasing) voltage during the voltage sweep to remove different amounts of charges (Fig. 7.6.1 (b)). The shift of the forward curves in the former case, and the displacement of the reverse curves in the latter case, will result in a series of increasing or decreasing capacitance values at the reading voltage, serving as multiple-bit storage.

As shown in Fig. 7.6.1 (a), the pre-bias of -15 V was applied to the device for a hold time varies from 2 s to 15 s before a ±3 V voltage sweep with steps of 0.1 V. The capacitance at 0 V in the forward curves raise from 2.9 nF to 3.4 nF with a steep increase at the first five points (hold time 2 s to 7 s), and then a gradually saturated increase at the rest points (hold time 8 s to 15 s). For obtaining the continuous capacitance decrease at 0 V shown in Fig. 7.6.1 (b), the pre-bias condition is fixed to

be -15 V, 5 s, while the sweep range varied with upper voltages from 1.0 V to 2.0 V but with the lower voltages remaining at -3 V. A curve with an upper voltage of 3 V is run as performance check. With the increase of upper voltage, the capacitance of device decrease from 3.3 nF to 2.9 nF almost linearly (upper voltage of 3 V is not plotted in the inset figure). The multiple-bit storage at 0 V reading voltage can be tuned easily and efficiently. The reading voltage is not limited to 0 V, any voltage in between the voltage range can be the reading voltage for obtaining different bits, but the number of bits differs.

7.5.2 Mimicking the long-term plasticity (LTP) behavior

Synaptic plasticity is the ability of synapses to strengthen or weaken over time to control the effectiveness of the communication between two neurons [229]. It functions as the response to increases or decreases in the activity, including short-term plasticity (STP) of short-term synaptic enhancement and depression, long-term plasticity (LTP) of long-term potentiation and depression. Long-term synaptic plasticity lasts anywhere from minutes to hours, days, or years, and dominates the brain storage, while the short-term synaptic plasticity lasts for sub-second timescale and reverts to "normal" soon afterward [230]. For the synaptic resistive random access memory device, the basic features of synaptic plasticity can be mimicked based on formation and rupture of conducting filament [231]. Temporary increase and spontaneous decay of conductance level in pulse measurement emulate the STP while the frequent stimulation results in a transition to more important LTP.

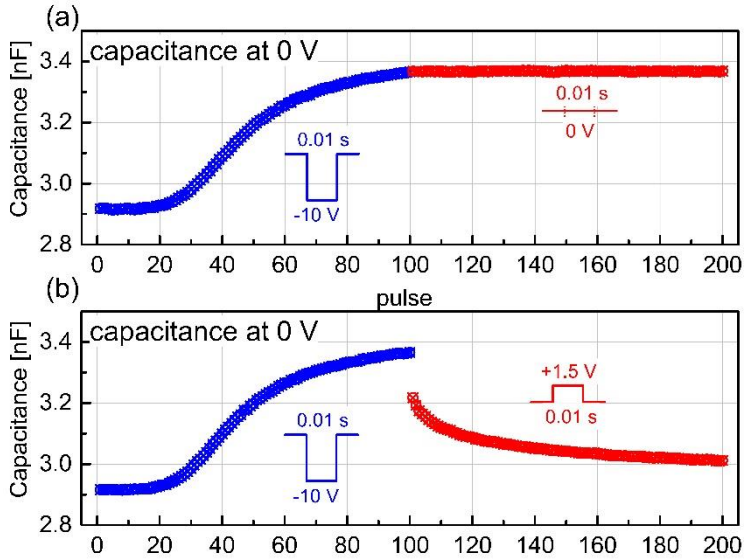


Figure 7.5.2: Programming of the pinMOS memory at applying -10 V writing voltage for 0.01 s for first 100 pulses and then (a) keep at 0 V or (b)) erasing it with +1.5 V, 0.01 s. The reading voltage is 0 V.

To mimic the long-term plasticity of both long-term potentiation and depression, different voltage pulse schedules were run in Fig. 7.6.2. Due to the limitation of the set up at this moment, a millisecond pulse measurement is not available. Therefore, a rough but functional works pulse is operated by following the example of the writing process: the writing voltage with a -10 V and duration of 0.01 s is considered as the pulse value and pulse width, respectively. The time gap

between the reading (at 0 V) and writing is then the pulse interval for the pulse, which is constant. With the pulse repetition, a gradual increase of capacitance can be gained, presenting a switch of memory states from '-1' to '1'. The plateau-like curve at the last 5 stimulation pulses out of 100 indicates a sign of getting a long-lived transition to the higher-capacitance state when the repetition number is increased to a certain value. The stability of long-term potentiation, which is defined as a state maintaining the capacitance of, here 3.36 nF, was then recorded at 0 V for another 100 pulses as seen in Fig. 7.6.2 (a). To keep pace with the pulse interval, the voltage of 0 V was 'applied' for 0.01 s before the reading as in the writing process. There is no drop as well as noticeable fluctuations for the capacitance curve as a function of pulse numbers, proving a stable long-term potentiation behavior. Considering the retention time measurement in Fig. 7.3.6, the high capacitance state can last at least hours. The long-term depression can also be achieved by changing the pulse voltage from a negative erasing voltage of -10 V to a positive erasing voltage of +1.5 V, while keeping the pulse width (0.01 s) and pulse interval as shown in Fig. 7.6.2 (b). The decrease of capacitance, although not ideal linearly, shows the effective depression. Therefore, an analog tuning through more than 50 capacitance states by applying the writing and erasing pulses. A more symmetric curve may be obtained if the pulse width and interval can be adjusted more subtly in real pulse measurements. Nevertheless, synaptic behavior of LTP in the pinMOS device is demonstrated in principle.

Because of the long retention time for the pinMOS memory, the short decay, which is required for STP is not achievable at the moment. However, introducing the leakage current to the device will solve this problem. One thing that needs to be pointed out is that the long long-term potentiation is also optically available by UV light, and the device brightness can be treated as the output optical signal to replace the electrical capacitance signal. Overall, early-stage synaptic behaviors are presented by the pinMOS memory, and a more detailed synaptic-behavior based pulse measurements are required for further investigations with precise defined pulse width and interval.

7.6 Summary

In this chapter, we fabricated a non-volatile, multiple-bit storage, capacitive pinMOS memory that provides optoelectronic control in both the writing and reading processes. The relatively simple fabricated, diode-capacitor based pinMOS (p-i-n-metal-oxide-semiconductor) memory has a bias-history-dependent capacitance, showing good device repeatability, excellent device performance with an endurance of over 10^4 cycles and retention times over 24 h with the equipment remaining connected. During the writing and erasing processes, there is always a remaining undepleted region in the p-doped layer with its own potential, decoupling itself and thus the pinMOS memory into two individual elements: a MOS capacitor and an OLED (p-i-n junction). A destruction and reconstruction cycle of equilibrium state and the accompanying energy band variations in the two sub-devices is indicated by the quasi-steay state working mechanism we proposed, which accounts for the property of tunability. Accompanied by hole accumulation and hole depletion in the MOS capacitor, Zener tunneling and carrier recombination in the p-i-n stack, the capacitance of the pinMOS memory varies under the dynamic states during the voltage sweep, showing as a controllable memory window. The depletion-accumulation mechanism, distinguished from the

conventional charge-trapping or charge tunneling based devices, enables tunability in various pathways for reading, erasing and writing, i.e., tuning the memory window by incremental adding or removal of charges via programmable operation parameters or light illumination, readout the memory states, electrically or optically.

Furthermore, the information stored in the device can be released in fractional amounts, giving rise to what is in principle multiple-bit storage. The possibility of pinMOS memory being programmed by optical stimulation and output light-dosage-dependent as well as history-dependent capacitance states, holds promise for optical storage. With the early-stage evidence of the long-term plasticity synaptic behavior, the pinMOS memory has potential in creating new opportunities for the development of the photonic memory devices, artificial visual memory system, and photosensing systems. However, the excellent retention time limits the mimicking of short-term plasticity and spike timing-dependent plasticity. Furthermore, the optical readout pathways, which can reveal the device states by visible light emission, are so far theoretically only and need to be verified by pulse measurements with a photodiode practically.

Chapter 8

Optoelectronic properties of pinMOS memory

8.1 Introduction

The working mechanism of the non-volatile pinMOS memory device introduced in Chapter 7 indicates an additional reading accessibility via light emission. The capability to store charge and the current flow in p-i-n stack are critical aspects of this new programmable pinMOS memory, leading to multiple-bit storage with optoelectronic control in the reading processes. Since the pinMOS memory was proven to be operable by UV light illumination in Chapter 7, the visible-light emission from the OLED element for readout can further broaden its application, like being a UV-to-visible-light transponder in an optical-electrical-optical repeater systems. To investigate the optical reading potential, pulse characteristics as well as corresponding optical properties are essential to be studied in detail.

In this chapter, a series of pulse measurements was applied to the pinMOS to prove the optical reading pathway and study the controllability over programmable operation parameters. The measurement set up with a mounted camera and a photodiode was first introduced in Sec. 8.2. The device emission images in Sec. 8.3 then demonstrate the possibility of an optical readout. A photodiode was employed in Sec. 8.4 for investigating the device brightness (light intensity) response during the pulse measurements as well as its dependence on repetition rate, duty cycle, writing and erasing voltage. Such optical dependence of pinMOS memory device with pulse measurements is summarized in Sec. 8.5.

8.2 Measurement setup

According to the working mechanism discussed in Sec. 7.4, holes will be exhausted due to recombination when applying a DC voltage, which is partly verified by the disappearance of memory window in Fig. 7.3.5 (b) with no pre-bias. Since there is no emission under DC bias application, voltage pulses with varied pulse parameters were applied to the pinMOS memory.

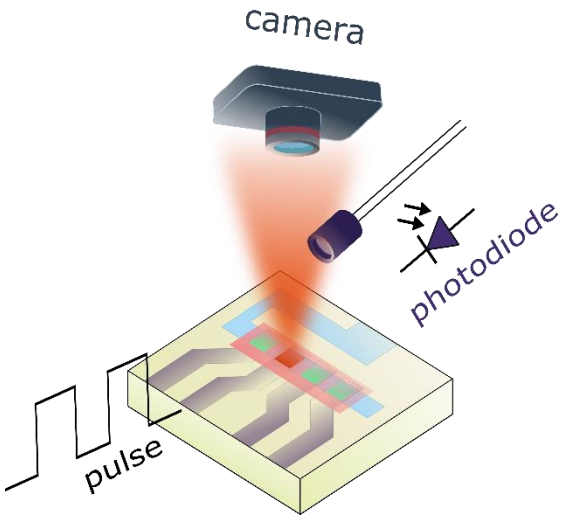


Figure 8.2.1: Schematic of the pulse measurement setup.

To verify and record the state-dependent light emission from the pinMOS device, a pulse measurement setup was created in Fig. 8.2.1 that consists of a photodiode and a camera which were mounted directly on top of an OLED to record the pulse-varying luminance signals and emission images. A 50 times magnification voltage amplifier was connected to the pulse generator for applying high voltages to the device in order to bring sufficient amount of charge in the limited milliseconds. Unless otherwise mentioned, the repetition rate of pulse is 100 Hz in keeping with Chapter 7. Here, the pulse width is controlled by the duty cycle, which is defined as the percentage occupied by the upper voltage.

8.3 pinMOS memory emission intensity

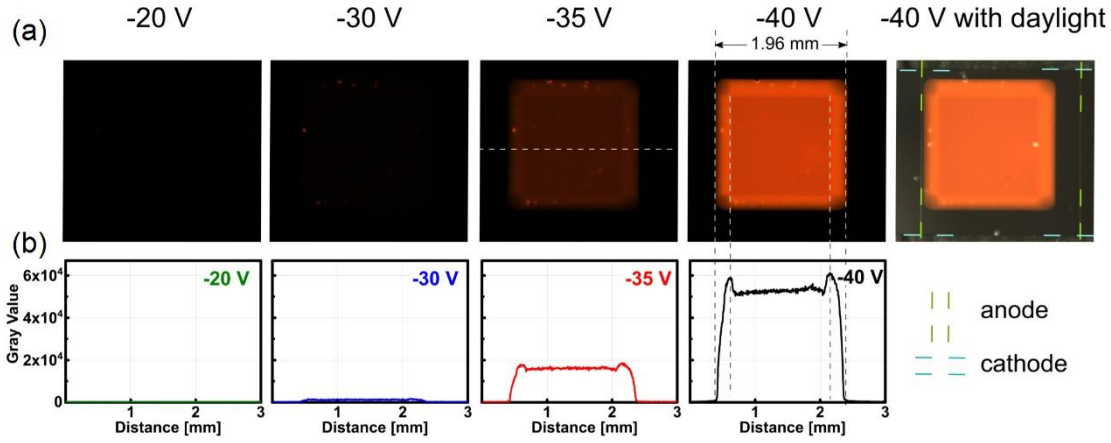


Figure 8.3.1: (a) Images of a pinMOS memory device under different pluses. (b) The corresponding light intensities.

To first qualitatively prove the light emission of the pinMOS memory as well as to define the emission area, we used a pulse with a repetition rate of 100 Hz and a duty cycle of 20%, with a writing voltage (lower voltage) pulses in the range of -20 V to -40 V for a duration of 8 ms, and an erasing voltage (upper voltage) pulses of 3 V (constant) for a duration of 2 ms. The images and the

corresponding light densities after a 5 s integration of the emission were recorded by the camera mounted on top of the emission device as shown in Fig. 8.3.1. All images in Fig. 8.3.1 (a) were taken in the dark except the last one was in daylight. The x-axes in Fig. 8.3.1 (b) correspond to the horizontal positions in the images in Fig. 8.3.1 (a), and the light intensity values for all conditions are extracted along the horizontal white dashed line shown in the image with -35 V. The case of -20 V writing voltage shows no emission intensity distribution. The non-luminous device suggests that within the 8 ms writing pulse duration, although the Zener tunneling is activated, -20 V is not sufficient for substantial Zener tunneling currents that would repopulate the p-doped region with large numbers of holes (that could then radiatively recombine during the reading pulse). Since the device dimensions have not been scaled down compared with the device used in Chapter 7, state switch between '-1' and '1' requires higher field intensity with the 100 times smaller application duration (8 ms *v.s.* ca. 0.8 s). To repopulate the p-doped layer in 8 ms, the writing voltage was increased to -30 V, -35 V and -40 V, and light emissions as well as an increase in overall light intensities were then obtained, since more holes tunneling into the p-doped layer in the presence of the stronger electric fields across the p-i-n junction.

The light emission area is a homogeneous square area with a side length of 1.96 mm, which is smaller than the active area given by the overlap of the electrodes as observed with daylight in Fig. 8.3.1 (a), but in good agreement with the size and area of the p-doped layer as structured during the fabrication. The emission area is not correctly center aligned with the active area as designed, but still within the overlap area of the electrodes. A uniform center area in emission intensity that confirmed by the line cut with little fluctuations can be observed in Fig. 8.3.1 (b). However, a small variation of lateral distribution at the edge and corner, as well as some random bright spots are also detectable. This emission non-uniformity comes from unavoidable thickness variation due to sample rotation during the fabrication, which leads to four slightly brighter side areas and the four darker corners, as well as some bright spots.

In general, conversion from electrical to optical signal in the pinMOS memory is verified by the emission signal and the structuring of the doped layers efficiently dominates the emission area. Higher writing voltage is required for bringing sufficient holes in the pulse measurements due to its dramatically smaller duration (pulse width).

8.4 Pulse characteristics and device brightness

After the qualitative proof of the device emission, a more detailed study of the pulsed measurements and the corresponding optical properties is further necessary. A photodiode was mounted in an appropriate position above the pinMOS memory device (Fig. 8.2.1) to collect the light and then reveal the device brightness by its voltage.

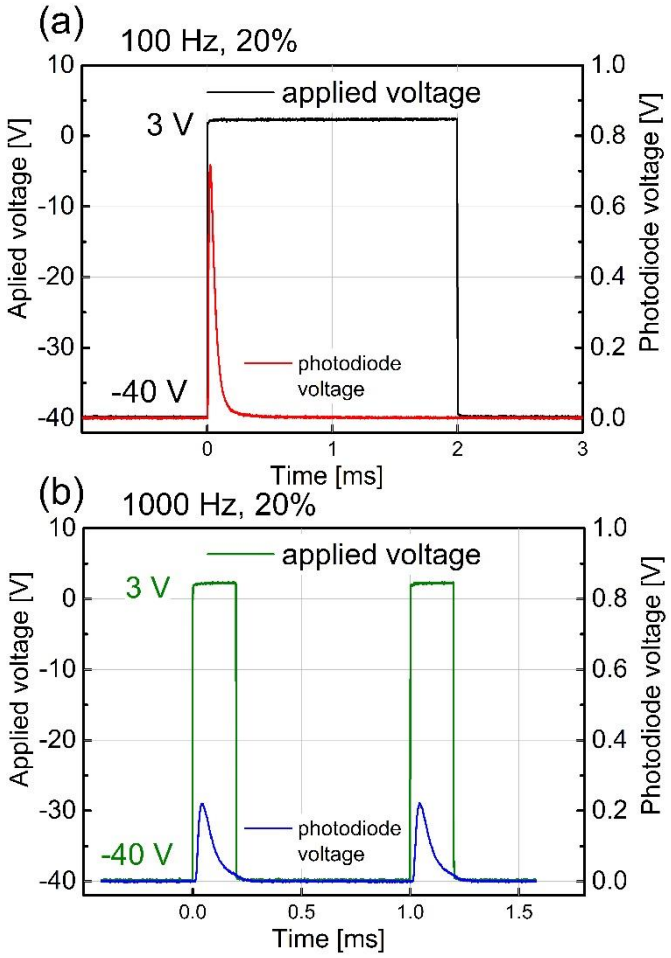


Figure 8.4.1: Device brightness with the same pulse but different repetition rates of (a) 100 Hz and (b) 1000 Hz.

Repetition rate Although 100 Hz is set as the default repetition rate for pulse measurements of pinMOS memory devices, a simple comparison between 100 Hz and 1000 Hz was still done for checking its influence. To ensure the holes repopulation, the writing voltage was chosen to be -40 V and the erasing voltage was 3 V with the duty cycle of 20% (Fig. 8.4.1). For both repetition rates, a light intensity peak (photodiode voltage peak) was observed immediately after the pulse switches from writing to erasing process every time, and then disappear until the next pulse. A more detailed discussion will be shown later with pulse variations. The writing process lasts 8 ms and 0.8 ms, while the erasing process lasts for 2 ms and 0.2 ms for the repetition rate of 100 Hz (Fig. 8.4.1 (a)) and 1000 Hz (Fig. 8.4.1 (b)), respectively. The tenfold writing duration in the former case results in a ca. 3.5 higher emission intensity peak.

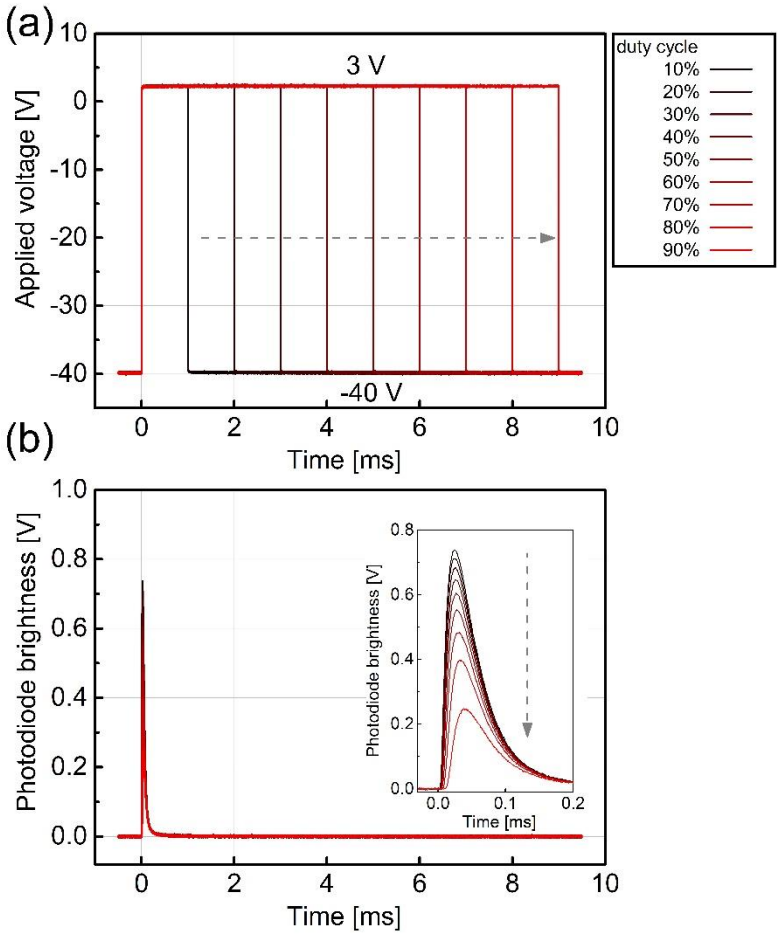


Figure 8.4.2: Time-resolved measurements of pulses with (a) varied duty cycles and (b) corresponding device brightness. Insert: Zoom in images of device brightness.

Duty cycle The repetition rate is set back to the default 100 Hz in the followings. The duty cycle was varied from 10% to 90% in steps of 10% with the pulse of writing voltage (lower voltage) -40 V, erasing voltage (upper voltage) 3 V as shown in Fig. 8.4.2. In the certain 10 ms pulse period defined by the 100 Hz repetition rate, the increase of duty cycle from 10% to 90% in Fig. 8.4.2 (a) identify with a decrease of writing pulse width from 9 ms to 1 ms, companied by the corresponding erasing pulse width increases from 1 ms to 9 ms in turns. As the longer writing process creates large amounts of excess holes with the same tunneling flux, the light intensity decrease with the increase of duty cycle as shown in Fig. 8.4.2 (b), inset. Despite the light intensity values, all peaks appear within the first 0.2 ms, sharing spike-like shapes with a similar time-axis for the peak value, and then no longer present in the rest of the erasing duration. The peak similarity reveals that the carriers always recombine and emit light in the OLED element once the pinMOS memory device is switched to a positive voltage, and that the device then quickly runs out of excess holes, regardless their initial amount. The increment in light intensity, or photodiode voltage, is not in direct proportion to the increment of writing duration but gradually becomes smaller. Such saturation behavior corresponds to the memory window saturation of the CV curves driven from the same pre-bias but different hold time (Fig. 7.5.1), which is due to the decrease of the potential drop over the p-i-n junction during the process of achieving the quasi-steady state under a constant voltage application.

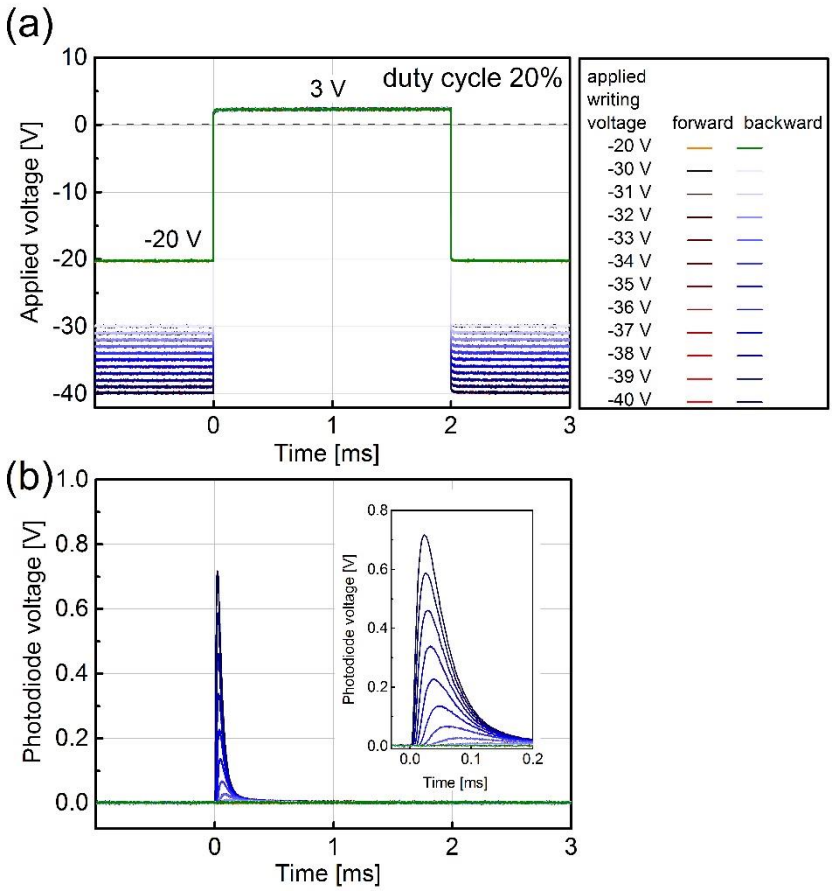


Figure 8.4.3: Time-resolved measurements of applied device voltages with (a) varied writing voltages and (b) corresponding device brightness. Insert: Zoom in images of device brightness.

Writing voltage The duty cycle is set back to the default 20% and the repetition rate is 100 Hz in the followings. As the emission images shown in Fig. 8.3.1, the writing voltages (lower voltages of pulses) directly decide the light intensities. Therefore, the writing voltage was again varied in Fig. 8.4.3 (a) while the erasing voltage under which light is emitted was fixed to be 3 V. The corresponding device brightness was recorded by the photodiode (same color groups in Fig. 8.4.3 (b)). The curves in green and orange (obscured by the green) are corresponding to a device operated with -20 V writing voltage, which as revealed in Fig. 8.3.1, is not satisfactory to sufficiently replenish the p-doped layer within the 8 ms duration time and thus show no device brightness. To lighten the pinMOS memory, the lower voltage was stepwise increased from -30 V to -40 V (red-tone curves) and back to -30 V (blue-tone curves) in steps of 1 V. The near-perfect overlap between the two groups of brightness curves hides the forward curves (orange and red-tone) and thus confirms excellent repeatability of the pulse emission.

Only if a high negative writing voltage is applied beforehand is it that a light emission can be observed. With the increase in writing voltage magnitude, a higher strength electric field across the p-i-n junction promotes stronger Zener tunneling effect to push more charges to be accumulated, which then results in higher and sharper brightness curves. Regardless of the device brightness value, the photodiode traces reveal again a series of sharp emission peaks, indicating the same process of the emission at the first moment of switching to +3 V erasing voltage, and the following quenching

with 0.2 ms. From the duty cycle test and emission images, both the values and the respective pulse durations of applied voltages are responsible for the number of charges that can be stored. This experiment once again shows that for a short duration like the 8 ms here, a larger voltage such as -30 V is required for sufficient tunneling of holes. Furthermore, the larger the voltage, the more holes can be repopulated in 8 ms, and the higher the peak brightness can be.

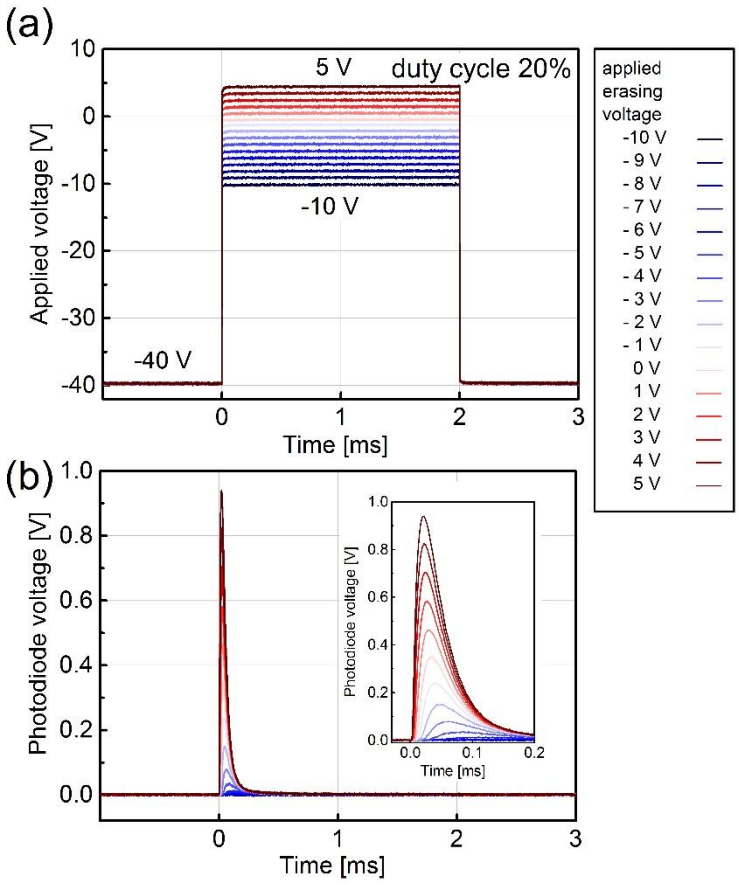


Figure 8.4.4: Time-resolved measurements of applied device voltages with (a) varied erasing voltages and (b) corresponding device brightness. Insert: Zoom in images of device brightness.

Erasing voltage The relationship between erasing voltage (upper voltage) and light emission is also evaluated in Fig. 8.4.4. For doing this, the erasing voltage, under which the emission comes up, was varied stepwise from -10 V to +5 V while the writing voltage was now fixed to the constant -40 V (Fig. 8.4.4 (a)). The curves for a negative erasing voltage are in blue and all other curves are in red tones. Similarly, the larger the erasing voltage is, the sharper and higher the brightness curve can be, owing to the larger net potential drops in the p-i-n stack (OLED element) in the forward direction. In contrast to a typical OLED, light emission is available at negative erasing voltages shown in Fig. 8.4.4 (b), i.e., the OLED element can be turned on with a pulse smaller than 0 V. This can be explained by the working mechanism proposed in Chapter 7 based on the change from subfigure (i) to (iii) in Fig. 7.4.1: the large negative writing voltage accumulates a significant number of excess holes in the p-doped layer, which lowers the Fermi level of the p-doped layer and enables charges to flow back into the OLED element to recombine and emit light even at an applied upper voltage of -4 V.

8.5 Conclusion

In this chapter, we studied the optical characteristics of pinMOS memory with pulse measurements. The states switch is proven to be accessible optically by the visible light emission from the OLED element of the pinMOS memory device. The emission area is governed by the area of structured doped layers, and the corresponding device brightness can be manipulated by varying the operation parameters, including repetition rate, pulse duty cycle, writing and erasing voltages. As the working mechanism proposed in Chapter 7 suggests, when the OLED element is operated in the forward direction (can be voltage smaller than 0 V), the holes that accumulated in the p-doped layer during the writing process will flow back to the OLED element, recombine with electrons, then emit transient light and eventually be exhausted. This process can be confirmed in this chapter by the spike-like peak in the device brightness measurements, which further verifies our speculations regarding the pinMOS memory. Furthermore, the gradual increase in the peak brightness indicate that the tunability of the multiple-bit storage pinMOS memory shown in Chapter 7 is also applicable when electrical signals are converted optically. The observed trends in the optical signals obtained during the measurements in this section can all be nicely explained by the proposed working mechanism. The device emission as determined by the incorporated OLED element is not limited to red. In principle, by changing the emission layers with the same device layout, the emission from the pinMOS memory can cover the full spectrum.

Chapter 9

Conclusion

The main focus of this work was devoted to a novel, non-volatile memory device called p-i-n-metal-oxide-semiconductor (pinMOS) memory. With precise control of doped layers to prevent lateral charge transport, the pinMOS memory device is designed to be an OLED based integrated capacitor, in which charges can be added or removed stepwise. The pinMOS memory has multiple-bit storage, good device performance, possibility for downscaling, ability to be programmed and read out electrically as well as optically. Similar to the OLEDs, the diode-based architecture of memory devices enable a simple layer-by-layer fabrication. Furthermore, the working mechanisms in principle are applicable to all memory devices with pinMOS structure, indicating that different combinations of a variety of good insulator layer (oxide, polymer) and p-i-n junction OLED with every color can be chosen to behave as capacitive pinMOS memory.

Firstly, the device structure where large, continuous doped layers are sandwiched between two electrodes is studied in terms of OLEDs for optimization in reducing the leakage current. It is proven by both the neighboring device charging measurement and capacitance-frequency measurement that charge carrier can flow along the lateral direction of doped layers outside the active area. The active area which is usually defined by the overlap of the crossbar electrodes, however, is smaller than the area of large doped layers, rendering this common definition of active area invalid. The lateral transport in doped layers can span centimeters, and can be reduced via increasing the hold time during measurement, or easily, by structuring the doped layers. Otherwise, such lateral transport will charge up the area outside the active area, resulting in a capacitance increase at low frequency in CF measurement, as well as introducing leakage current shown in IV measurement. Although such lateral current flows only occur in the OLED at low voltage regime where vertical device resistance is high, it is still a tricky problem for memory devices since the associated leakage current can erase the stored charges. Fortunately, the leakage current can drastically decrease by 2-3 orders of magnitude by structuring the doped layers, leading to extremely low steady state leakage currents in OLED (here 10^{-7} mA/cm^2 at -1 V).

Furthermore, the identified lateral charging behavior can be utilized for exploring properties of doped layers in a fabricated device. An RC circuit model is developed to fit the CF experimental data in the extended frequency range from 10^{-2} Hz to 10^{6} Hz, which then allows extracting information about the conductivity as well as the corresponding activation energy of both, n-doped

and p-doped layer simultaneously at the low frequency. Moreover, by means of a pseudo-trap-analysis, it is demonstrated that the electronic effects of the lateral charging in such crossbar architectures can easily be misinterpreted as trap states. To exclude the lateral transport effect in the memory device, the doped layers are structured to be smaller than the active area to be referred to as the effective area.

Secondly, the pinMOS memory device with well-structured doped layers is investigated with a straight-forward fabrication of insulating oxide layer, p-doped layer, intrinsic layers, n-doped layer, and Al electrode on ITO pre-structured substrate. A pronounced 2.4 V memory window can be observed via applying -15 V for 5 s and subsequently sweep from -3 V to +3 V (forward direction) and back to -3 V (reverse direction) in steps of 1 V with nice repeatability. The pinMOS memory also shows long cyclic endurance over 10^4 as well as good retention time of over 24 h. In the pinMOS memory, an undepleted region in the p-doped layer where the original free hole carrier concentration is retained can be thought of dividing the p-doped layer and thus the pinMOS memory into two series-connected individual elements: a MOS (metal-oxide-semiconductor) capacitor and an OLED. When a DC voltage is applied to the device, either for the writing process with a negative bias or the erasing process with a positive bias, the electrical currents will only flow internally in the p-i-n stack. This will result in quasi-steady states in which all external voltage drops entirely over the insulator, leaving no current flow since the insulator is assumed to block any flow of carriers between the semiconductor and the metal at all voltages. Once the applied voltage is removed, an equal but opposite built-in potential will drop over the p-i-n stack again, revealing a non-equilibrium state which is shown as capacitive memory behavior. The electrically assessed writing effect is achieved through Zener tunneling in the p-i-n stack, while the erasing effect is caused by carrier recombination in the OLED element. There are several layers and incorporated depletion/accumulation regions that can contribute to the modulation of the capacitance, but the variation of space charge zones in the doped layers that are adjacent to the intrinsic layers dominate the total device capacitance. As a consequence, the memory state can be read out by capacitance difference at the same reading voltage (like 0 V). Furthermore, the memory behavior in pinMOS memory can be programmed by varying the voltage value or hold time for both writing and erasing processes so that the operation in circuits with multiple-bit becomes feasible. The tunability of the memory window, both forward and backward curves, all indicate flexible control over the stored information.

Thirdly, pinMOS memory can serve as optical storage memory, indicated by the UV light- induced tunability and visible light emission read-out. The UV light with a wavelength of 375 nm can create free charge carriers in the stack of red OLEDs, resulting in charge accumulation similar to the Zener tunneling effect in the electric writing process. Therefore, similar memory behavior can be achieved and varied by the UV light illumination with different intensity and time. Moreover, the diode-based memory device can emit light when the state shifted from “-1” to “1”. The emission area is limited by the effective area defined by the structured doped layers, while the emission intensity can be tuned by the voltage value, the application time (duty cycle), and the repetition rate in the pulse measurement. The light writing possibility, in terms of neuromorphic language, paves the way for optical storage since the pinMOS device shows light dosage-dependent as well as history-dependent capacitance states with optical stimulation. Moreover, the optical read-out possibility further hold

promise for artificial visual memory system, and photosensing systems. An early-stage study already shows the potential of using pinMOS memory to mimic long-term synaptic plasticity, although other features like short-time plasticity remain to be developed.

Bibliography

[1] D. H. Kim, J. Xiao, J. Song, Y. Huang, and J. A. Rogers, "Stretchable, curvilinear electronics based on inorganic materials," *Adv. Mater.*, vol. 22, no. 19, pp. 2108-2124, 2010.

[2] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488-492, 2004.

[3] K. Fukuda, Y. Takeda, Y. Yoshimura, R. Shiwaku, L. T. Tran, T. Sekine, M. Mizukami, D. Kumaki, and S, Tokito, "Fully-printed high-performance organic thin-film transistors and circuitry on one-micron-thick polymer films," *Nat. Commun.*, vol. 5, no. 1, p. 4147, 2014.

[4] J. E. Anthony, "Addressing challenges," *Nat. Mater.*, vol. 13, no. 8, pp. 773-775, 2014.

[5] Y. Wang, Y. Qiu, S. K. Ameri, H. Jang, Z. Dai, Y. Huang, and N. Lu, "Low-cost, μm-thick, tape-free electronic tattoo sensors with minimized motion and sweat artifacts," *npj Flex. Electron.*, vol. 2, no. 1, p. 6, 2018.

[6] M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K. Kuribara, T. Tokuhara, M. Drack, R. Schwödiauer, I. Graz, S. B. Gogonea, S. Bauer, and T. Someya, "An ultra-lightweight design for imperceptible plastic electronics," *Nature*, vol. 499, no. 7459, pp. 458-463, 2013.

[7] C. J. Bettinger and Z. Bao, "Biomaterials-based organic electronic devices," *Polym. Int.*, vol. 59, no. 5, pp. 563-567, 2010.

[8] M. Berggren, D. Nilsson, and N. D. Robinson, "Organic materials for printed electronics," *Nat. Mater.*, vol. 6, no. 1, pp. 3-5, 2007.

[9] https://www.samsung.com/global/galaxy/galaxy-fold/.

[10] B. Zimmermann, H. F. Schleiermacher, M. Niggemann, and U. Würfel, "ITO-free flexible inverted organic solar cell modules with high fill factor prepared by slot die coating," *Sol. Energy Mater. Sol. Cells*, vol. 95, no. 7, pp. 1587-1589, 2011.

[11] S. Wang, J. Xu, W. Wang, G. J. N. Wang, R. Rastak, F. M. Lopez, J. W. Chung, Si. Niu, V. R. Feig, J. Lopez, Ting Lei, S. K. Kwon, Y. Kim, A. M. Foudeh, A. Ehrlich, A. Gasperini, Y. Yun, B. Murmann, J. B. H. Tok, and Z. Bao, "Skin electronics from scalable fabrication of an intrinsically stretchable transistor array," *Nature*, vol. 555, no. 7694, pp. 83-88, 2018.

[12] S. Nau and E. J. W. L. Kratochvil, W.C. Chen (Ed.), *Foreword: Introduction to organic memory technologies*, Cambridge: Royal Society of Chemistry, 2015.

[13] B. Zhang, Y. Chen, K.G. Neoh, E.T. Kang, W.C. Chen (Ed.), *Organic electronic memory devices*, Cambridge: Royal Society of Chemistry, 2015.

[14] S. Raoux, G. W. Burr, M. J. Breitwisch, C. T. Rettner, Y. C. Chen, R. M. Shelby, M. Salinga, D. Krebs, S. H. Chen, H. L. Lung, and C. H. Lam, "Phase-change random access memory: A scalable technology," *IBM J. Res. Dev.*, vol. 52, no. 4.5, pp. 465-479, 2008.

[15] J. Rivnay, S. Inal, A. Salleo, R. M. Owens, M. Berggren, and G. G. Malliaras, "Organic electrochemical transistors," *Nat. Rev. Mater.*, vol. 3, no. 2, p. 17086, 2018.

[16] F. Pan, S. Gao, C. Chen, C. Song, and F. Zeng, "Recent progress in resistive random access memories: Materials, switching mechanisms, and performance," *Mater. Sci. Eng. R Reports*, vol. 83, pp. 1-59, Sep. 2014.

[17] W. L. Leong, N. Mathews, B. Tan, S. Vaidyanathan, F. Dötz, and S. Mhaisalkar, "Towards printable organic thin film transistor based flash memory devices," *J. Mater. Chem.*, vol. 21, no. 14, p. 5203, 2011.

[18] R. Guo, L. You, Y. Zhou, Z. S. Lim, X. Zou, L. Chen, R. Ramesh, and J. Wang, "Non-volatile memory based on the ferroelectric photovoltaic effect," *Nat. Commun.*, vol. 4, no. 1, p. 1990, 2013.

[19] W. C. Chen, (Ed.), *Electrical memory materials and devices*. Cambridge: Royal Society of Chemistry, 2015.

[20] E. J. Yoo, M. Lyu, J. H. Yun, C. J. Kang, Y. J. Choi, and L. Wang, "Resistive switching behavior in organic-inorganic hybrid $CH_3NH_3PbI_{3-x}Cl_x$ perovskite for resistive random access memory devices," *Adv. Mater.*, vol. 27, no. 40, pp. 6170-6175, 2015.

[21] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80-83, 2008.

[22] L. Chua, "Memristor-The missing circuit element," *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507-519, 1971.

[23] Y. V. Pershin and M. Di Ventra, "Experimental demonstration of associative memory with memristive neural networks," *Neural Networks*, vol. 23, no. 7, pp. 881-886, 2010.

[24] D. Biolek, Z. Biolek, and V. Biolkova, "SPICE modeling of memristive, memcapacitative and meminductive systems," in *2009 European Conference on Circuit Theory and Design*, pp. 249-252, 2009.

[25] M. Di Ventra and Y. V. Pershin, "Memcapacitive neural networks," *Electron. Lett.*, vol. 50, no. 3, pp. 141-143, 2014.

[26] Z. Wang, M. Rao, J.W. Han, J. Zhang, P. Lin, Y. Li, C. Li, W. Song, S. Asapu, R. Midya, Y. Zhuo, H. Jiang, J.H. Yoon, N.K. Upadhyay, S. Joshi, M. Hu, J.P. Strachan, M. Barnell, Q. Wu, H. Wu, Q. Qiu, R.S. Williams, Q. Xia, and J.J. Yang, "Capacitive neural network with neuro-transistors," *Nat. Commun.*, vol. 9, no. 1, pp. 1-10, 2018.

[27] S. Lee, H. Seong, S. G. Im, H. Moon, and S. Yoo, "Organic flash memory on various flexible substrates for foldable and disposable electronics," *Nat. Commun.*, vol. 8, no. 1, p. 725, 2017.

[28] https://www.printedelectronicsworld.com/articles/5064/largest-flexible-memory-arrays-to-date.

[29] A. Köhler and H. Bässler, *Electronic processes in organic semiconductors*. Weinheim: Wiley-VCH Verlag GmbH & Co. KGaA, 2015.

[30] W. A. Harrison., *Electronic structure and the properties of solids: the physics of the chemical bond*. New York : Dover Publications, 1989.

[31] P. Atkins and Ronald Friedman, *Molecular quantum Mmchanics*. UK: Oxford University, 1983.

[32] S. Furukawa, M. Fujita, Y. Kanatomi, M. Minoura, M. Hatanaka, K. Morokuma, K. Ishimura, and M. Saito, "Double aromaticity arising from σ- and π-rings," *Commun. Chem.*, vol. 1, no.

1, p. 60, 2018.

[33] D. Casanova and P. Alemany, "Quantifying the symmetry content of the electronic structure of molecules: Molecular orbitals and the wave function," *Phys. Chem. Chem. Phys.*, vol. 12, no. 47, pp. 15523-15529, 2010.

[34] L. Verlet, "Computer 'Experiments' on Classical Fluids. I. Thermodynamical properties of Lennard-Jones molecules," *Phys. Rev.*, vol. 159, no. 1, pp. 98-103, 1967.

[35] R. Heller, "Theory of some van der Waals molecules," *J. Chem. Phys.*, vol. 9, no. 2, pp. 154-163, 1941.

[36] L. Friedman, "Transport properties of organic semiconductors," *Phys. Rev.*, vol. 133, no. 6A, pp. A1668-A1679, 1964.

[37] Z. Shuai, D. Beljonne, R. J. Silbey, and J. L. Brédas, "Singlet and triplet exciton formation rates in conjugated polymer light-emitting diodes," *Phys. Rev. Lett.*, vol. 84, no. 1, pp. 131-134, 2000.

[38] M. Schwoerer and H. C. Wolf, *Organic molecular solids*. Weinheim: Wiley-VCH Verlag GmbH & Co. KGaA, 2007.

[39] K. Nagashima, and S. S. Velan, "Understanding the singlet and triplet states in magnetic resonance," *Concepts Magn. Reson. Part A*, vol. 42, no. 5, pp. 165-181, 2013.

[40] J. M. Ziman, *Electrons and phonons*. Oxford University Press, 2001.

[41] N. Karl, "Charge carrier transport in organic semiconductors," *Synth. Met.*, vol. 133-134, pp. 649-657, 2003.

[42] W. Warta and N. Karl, "Naphthalene: High, electric-field-dependent," *Phys. Rev. B*, vol. 32, no. 2, pp. 1172-1182, 1985.

[43] L. Kleinman, "Theory of Phonon-Assisted Tunneling in Semiconductors," *Phys. Rev.*, vol. 140, no. 2A, pp. A637-A648, 1965.

[44] P. Pipinys and A. Kiveris, "Variable range hopping and/or phonon-assisted tunneling mechanism of electronic transport in polymers and carbon nanotubes," *Open Phys.*, vol. 10, no. 2, pp. 271-281, 2012.

[45] C. Deibel and V. Dyakonov, "Polymer-fullerene bulk heterojunction solar cells," *Reports Prog. Phys.*, vol. 73, no. 9, p. 096401, 2010.

[46] H. Bässler, "Charge transport in disordered organic photoconductors a monte carlo simulation study," *Phys. status solidi*, vol. 175, no. 1, pp. 15-56, 1993.

[47] S. Reineke, F. Lindner, G. Schwartz, N. Seidler, K. Walzer, B. Lüssem, and K. Leo, "White organic light-emitting diodes with fluorescent tube efficiency," *Nature*, vol. 459, no. 7244, pp. 234-238, 2009.

[48] H. Uoyama, K. Goushi, K. Shizu, H. Nomura, and C. Adachi, "Highly efficient organic light-emitting diodes from delayed fluorescence," *Nature*, vol. 492, no. 7428, pp. 234-238, 2012.

[49] Y. J. Cheng, S.-H. Yang, and C. S. Hsu, "Synthesis of conjugated polymers for organic solar cell applications," *Chem. Rev.*, vol. 109, no. 11, pp. 5868-5923, 2009.

[50] G. Horowitz, "Organic field-effect transistors," *Adv. Mater*, vol. 10. no. 5, pp. 356-375, 1998.

[51] H. Sirringhaus, "Device physics of solution-processed organic field-effect transistors," *Adv. Mater.*, vol. 17, no. 20, pp. 2411-2425, 2005.

[52] K. Asadi, D. M. De Leeuw, B. De Boer, and P. W. M. Blom, "Organic non-volatile memories from ferroelectric phase-separated blends," *Nat. Mater.*, vol. 7, no. 7, pp. 547-550, 2008.

[53] J. Ouyang, C. W. Chu, C. R. Szmanda, L. Ma, and Y. Yang, "Programmable polymer thin film and non-volatile memory device," *Nat. Mater.*, vol. 3, no. 12, pp. 918-922, 2004.

[54] V. I. Arkhipov, H. von Seggern, and E. V. Emelianova, "Charge injection versus space-charge-limited current in organic light-emitting diodes," *Appl. Phys. Lett.*, vol. 83, no. 24, pp. 5074-5076, 2003.

[55] J. L. Bredas, "Mind the gap!," *Mater. Horiz.*, vol. 1, no. 1, pp. 17-19, 2014.

[56] P. W. M. Blom, M. J. M. de Jong, and J. J. M. Vleggaar, "Electron and hole transport in poly(p-phenylene vinylene) devices," *Appl. Phys. Lett.*, vol. 68, no. 23, pp. 3308-3310, 1996.

[57] P. N. Murgatroyd, "Theory of space-charge-limited current enhanced by Frenkel effect," *J. Phys. D. Appl. Phys.*, vol. 3, no. 2, pp. 151-156, 1970.

[58] J. A. Röhr, D. Moia, S. A. Haque, T. Kirchartz, and J. Nelson, "Exploring the validity and limitations of the Mott-Gurney law for charge-carrier mobility determination of semiconducting thin-films," *J. Phys. Condens. Matter*, vol. 30, no. 10, 2018.

[59] H. Bässler and A. Köhler, "Charge transport in organic semiconductors," 2011, pp. 1-65.

[60] W. Barford, *Electronic and optical properties of conjugated polymers.* UK: Oxford University, 2005.

[61] U. Wolf, V. I. Arkhipov, and H. Bässler, "Current injection from a metal to a disordered hopping system. I. Monte Carlo simulation," *Phys. Rev. B*, vol. 59, no. 11, pp. 7507-7513, 1999.

[62] H. J. Wintlet, "Schottky injection currents in insulators: The effect of space charge on the time dependence," *IEEE Trans. Electr. Insul.*, vol. EI-12, no. 6, pp. 424-428, 1977.

[63] P. R. Emtage and J. J. O'Dwyer, "Richardson-Schottky effect in insulators," *Phys. Rev. Lett.*, vol. 16, no. 9, pp. 356-358, 1966.

[64] A. J. Heeger, I. D. Parker, and Y. Yang, "Carrier injection into semiconducting polymers: Fowler-Nordheim field-emission tunneling," *Synth. Met.*, vol. 67, no. 1-3, pp. 23-29, 1994.

[65] Y. N. Gartstein and E. M. Conwell, "Field-dependent thermal injection into a disordered molecular insulator," *Chem. Phys. Lett.*, vol. 255, no. 1-3, pp. 93-98, 1996.

[66] K. Walzer, B. Maennig, M. Pfeiffer, and K. Leo, "Highly efficient organic devices based on electrically doped transport layers," *Chem. Rev.*, vol. 107, no. 4, pp. 1233-1271, 2007.

[67] K. C. Kao, *Dielectric phenomena in solids with emphasis on physical concepts of electronic processes*. Amsterdam: Elsevier, 2004.

[68] A. Vilan and D. Cahen, "Chemical modification of smiconductor surfaces for Molecular electronics," *Chem. Rev.*, vol. 117, no. 5, pp. 4624-4666, 2017.

[69] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2006.

[70] C. Kang, H. Shin, and C. Lee, "High-frequency organic rectifiers through interface engineering," *MRS Commun.*, vol. 7, no. 4, pp. 755-769, 2017.

[71] J. Bardeen, "SurfacesStates and rectification at a metal-semiconductor contact," *Phys. Rev.*, vol. 71, no. 10, pp. 717-727, 1947.

[72] Z. Yang, C. Kim, K.Y. Lee, M. Lee, S. Appalakondaiah, C. Ra, K. Watanabe, T. Taniguchi, K. Cho, E. Hwang, J. Hone, and W.J. Yoo, "A Fermi-evel-pinning-free 1D electrical contact at the intrinsic 2D MoS_2-metal junction," *Adv. Mater.*, vol. 31, no. 25, p. 1808231, 2019.

[73] Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, "Effects of traps on charge storage characteristics in metal-oxide-semiconductor memory structures based on silicon nanocrystals," *J. Appl. Phys.*, vol. 84, no. 4, pp. 2358-2360, 1998.

[74] C. Hu, J. Bokor, T. J. King, E. Anderson, C. Kuo, K. Asano, H. Takeuchi, J. Kedzierski, W. C. Lee, D. Hisamoto, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320-2325, 2000.

[75] A. S. Grove, B. E. Deal, E. H. Snow, and C. T. Sah, "Investigation of thermally oxidised silicon surfaces using metal-oxide-semiconductor structures," *Solid. State. Electron.*, vol. 8, no. 2, pp. 145-163, 1965.

[76] Z. Yatabe, J. T. Asubar, and T. Hashizume, "Insulated gate and surface passivation structures for GaN-based power transistors," *J. Phys. D. Appl. Phys.*, vol. 49, no. 39, p. 393001, 2016.

[77] C. Sah, R. Noyce, and W. Shockley, "Carrier generation and recombination in P-N junctions and P-N junction characteristics," *Proc. IRE*, vol. 45, no. 9, pp. 1228-1243, 1957.

[78] B. Lüssem, M. Riede, and K. Leo, "Doping of organic semiconductors," *Phys. status solidi*, vol. 210, no. 1, pp. 9-43, 2013.

[79] K. Harada, A. G. Werner, M. Pfeiffer, C. J. Bloom, C. M. Elliott, and K. Leo, "Organic homojunction diodes with a high built-in potential: Interpretation of the current-voltage characteristics by a generalized Einstein relation," *Phys. Rev. Lett.*, vol. 94, no. 3, p. 036601, 2005.

[80] O. Breitenstein, J. Bauer, K. Bothe, W. Kwapil, D. Lausch, U. Rau, J. Schmidt, M. Schneemann, M.C. Schubert, J. M. Wagner, and W. Warta, "Understanding junction breakdown in multicrystalline solar cells," *J. Appl. Phys.*, vol. 109, no. 7, p. 071101, 2011.

[81] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329-337, 2011.

[82] H. Sun, Q. Guo, D. Yang, Y. Chen, J. Chen, and D. Ma, "High efficiency tandem organic light emitting diode using an organic heterojunction as the charge generation layer: An investigation into the charge generation model and device performance," *ACS Photonics*, vol. 2, no. 2, pp. 271-279, 2015.

[83] H. Kleemann, R. Gutierrez, F. Lindner, S. Avdoshenko, P.D. Manrique, B. Lüssem, G. Cuniberti, and K. Leo, "Organic Zener diodes: Tunneling across the gap in organic semiconductor materials," *Nano Lett.*, vol. 10, no. 12, pp. 4929-4934, 2010.

[84] S. J. Kim, Y. S. Park, S. H. Lyu, and J. S. Lee, "Nonvolatile nano-floating gate memory devices based on pentacene semiconductors and organic tunneling insulator layers," *Appl. Phys. Lett.*, vol. 96, no. 3, p. 033302, 2010.

[85] L. Zhou, J. Mao, Y. Ren, S.-T. Han, V. A. L. Roy, and Y. Zhou, "Recent advances of flexible data storage devices based on organic nanoscaled materials," *Small*, vol. 14, no. 10, p. 1703126, 2018.

[86] Yoshio Nis, *Advances in mon-volatile memory and storage technology*. Amsterdam:

Elsevier, 2014.

[87] Q. D. Ling, D. J. Liaw, C. Zhu, D. S. H. Chan, E. T. Kang, and K. G. Neoh, "Polymer electronic memories: Materials, devices and mechanisms," *Prog. Polym. Sci.*, vol. 33, no. 10, pp. 917-978, 2008.

[88] H. Akinaga and H. Shima, "Resistive random access memory (ReRAM) based on metal oxides," *Proc. IEEE*, vol. 98, no. 12, pp. 2237-2251, 2010.

[89] V. Gupta, S. Kapur, S. Saurabh, and A. Grover, "Resistive random access memory: A review of device challenges," *IETE Tech. Rev.*, pp. 1-14, 2019.

[90] C. Liu, X. Yan, X. Song, S. Ding, D. W. Zhang, and P. Zhou, "A semi-floating gate memory based on van der Waals heterostructures for quasi-non-volatile applications," *Nat. Nanotechnol.*, vol. 13, no. 5, pp. 404-410, 2018.

[91] M. Sup Choi, G.-H. Lee, Y.-J. Yu, D.-Y. Lee, S. Hwan Lee, P. Kim, J. Hone, and W. Jong Yoo, "Controlled charge trapping by molybdenum disulphide and graphene in ultrathin heterostructured memory devices," *Nat. Commun.*, vol. 4, no. 1, p. 1624, 2013.

[92] Q. Zhao, H. Wang, Z. Ni, J. Liu, Y. Zhen, X. Zhang, L. Jiang, R. Li, H. Dong, and W. Hu, "Organic ferroelectric-based 1T1T random access memory cell employing a common dielectric layer overcoming the half-selection problem," *Adv. Mater.*, vol. 29, no. 34, p. 1701907, 2017.

[93] B. E. Park, H. Ishiwara, M. Okuyama, S. Sakai, and S. M. Yoon (Eds.), *Ferroelectric-gate field effect transistor memories*, vol. 131. Dordrecht: Springer, 2016.

[94] B. Cho, S. Song, Y. Ji, T. W. Kim, and T. Lee, "Organic resistive memory dvices: Performance enhancement, integration, and advanced architectures," *Adv. Funct. Mater.*, vol. 21, no. 15, pp. 2806-2829, 2011.

[95] B. Cho, T.-W. Kim, S. Song, Y. Ji, M. Jo, H. Hwang, G. Y. and Jung, T. Lee, "Rewritable switching of one diode-one resistor nonvolatile organic memory devices," *Adv. Mater.*, vol. 22, no. 11, pp. 1228-1232, 2010.

[96] J. C. Scott and L. D. Bozano, "Nonvolatile memory elements based on organic materials," *Adv. Mater.*, vol. 19, no. 11, pp. 1452-1463, 2007.

[97] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories - nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, no. 25-26, pp. 2632-2663, 2009.

[98] G. Dearnaley, A. M. Stoneham, and D. V Morgan, "Electrical phenomena in amorphous oxide films," *Reports Prog. Phys.*, vol. 33, no. 3, p. 306, 1970.

[99] L. F. Pender and R. J. Fleming, "Memory switching in glow discharge polymerized thin films," *J. Appl. Phys.*, vol. 46, no. 8, pp. 3426-3431, 1975.

[100] Y. Segui, B. Ai, and H. Carchano, "Switching in polystyrene films: Transition from on to off state," *J. Appl. Phys.*, vol. 47, no. 1, pp. 140-143, 1976.

[101] C. N. Berglund and N. Klein, "Thermal effects on switching of solids from an insulating to a conductive state," *Proc. IEEE*, vol. 59, no. 7, pp. 1099-1110, 1971.

[102] S. Sivaramakrishnan, P. J. Chia, Y. C. Yeo, L. L. Chua, and P. K.-H. Ho, "Controlled insulator-to-metal transformation in printable polymer composites with nanometal clusters,"

Nat. Mater., vol. 6, no. 2, pp. 149-155, 2007.

[103] W. J. Joo, T. L. Choi, K. H. Lee, and Y. Chung, "Study on threshold behavior of operation voltage in metal filament-based polymer memory," *J. Phys. Chem. B*, vol. 111, no. 27, pp. 7756-7760, 2007.

[104] W. J. Joo, T. L. Choi, J. Lee, S.K. Lee, M. S. Jung, N. Kim, and J.M. Kim, "Metal filament growth in electrically conductive polymers for nonvolatile memory application," *J. Phys. Chem. B*, vol. 110, no. 47, pp. 23812-23816, 2006.

[105] U.S. Bhansali, M.A. Khan, D. Cha, M.N. AlMadhoun, R. Li, L. Chen, A. Amassian, I.N. Odeh, H.N. Alshareef, "Metal-free, single-polymer device exhibits resistive memory effect," *ACS Nano*, vol. 7, no. 12, pp. 10518-10524, 2013.

[106] D. M. Taylor, "Space charges and traps in polymer electronics," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 13, no. 5, pp. 1063-1073, 2006.

[107] H. S. Majumdar, A. Bandyopadhyay, A. Bolognesi, and A. J. Pal, "Memory device applications of a conjugated polymer: Role of space charges," *J. Appl. Phys.*, vol. 91, no. 4, pp. 2433-2437, 2002.

[108] H. T. Lin, Z. Pei, and Y. J. Chan, "Carrier transport mechanism in a nanoparticle-incorporated organic bistable memory device," *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 569-571, 2007.

[109] L. D. Bozano, B. W. Kean, V. R. Deline, J. R. Salem, and J. C. Scott, "Mechanism for bistability in organic memory elements," *Appl. Phys. Lett.*, vol. 84, no. 4, pp. 607-609, Jan. 2004.

[110] Q. D. Ling, Y. Song, S. L. Lim, E.Y. H. Teo, Y. P. Tan, C. Zhu, D.S.H. Chan, D. L. Kwong, E. T. Kang, and K. G. Neoh, "A dynamic random access memory based on a conjugated copolymer containing electron-donor and -acceptor moieties," *Angew. Chemie Int. Ed.*, vol. 45, no. 18, pp. 2947-2951, 2006.

[111] R. S. Potember, T. O. Poehler, and D. O. Cowan, "Electrical switching and memory phenomena in Cu-TCNQ thin films," *Appl. Phys. Lett.*, vol. 34, no. 6, pp. 405-407, 1979.

[112] C. W. Chu, J. Ouyang, J. H. Tseng, and Y. Yang, "Organic donor-acceptor system exhibiting electrical bistability for use in memory devices," *Adv. Mater.*, vol. 17, no. 11, pp. 1440-1443, 2005.

[113] W. R. Hertler, H. D. Hartzler, D. S. Acker, and R. E. Benson, "Substituted quinodimethans. III. displacement reactions of 7,7,8,8-tetracyanoquinodimethan," *J. Am. Chem. Soc.*, vol. 84, no. 17, pp. 3387-3393, 1962.

[114] J. Ouyang, C. W. Chu, D. Sieves, and Y. Yang, "Electric-field-induced charge transfer between gold nanoparticle and capping 2-naphthalenethiol and organic memory cells," *Appl. Phys. Lett.*, vol. 86, no. 12, p. 123507, 2005.

[115] B. Pradhan, S. K. Batabyal, and A. J. Pal, "Electrical bistability and memory phenomenon in carbon nanotube-conjugated polymer matrixes," *J. Phys. Chem. B*, vol. 110, no. 16, pp. 8274-8277, 2006.

[116] J. Lin, M. Zheng, J. Chen, X. Gao, and D. Ma, "Negative differential resistance and memory effect in diodes based on 1,4-dibenzyl C_{60} and zinc phthalocyanine soped polystyrene hybrid material," *Inorg. Chem.*, vol. 46, no. 1, pp. 341-344, 2007.

[117] Sequeira Cesar and D. Santos (Eds.), *Organic conductors: Fundamentals and applications*.

New York: Woodhead, 1994.

[118] K. Yano, "Information storage using conductance change of Langmuir-Blodgett film and atomic force microscope/scanning tunneling microscope," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 14, no. 2, p. 1353, 1996.

[119] W. J. Yoon, S. Y. Chung, P. R. Berger, and S. M. Asar, "Room-temperature negative differential resistance in polymer tunnel diodes using a thin oxide layer and demonstration of threshold logic," *Appl. Phys. Lett.*, vol. 87, no. 20, p. 203506, 2005.

[120] S. Paul, A. Kanwal, and M. Chhowalla, "Memory effect in thin films of insulating polymer and C_{60} nanocomposites," *Nanotechnology*, vol. 17, no. 1, pp. 145-151, 2006.

[121] Z. J. Donhauser, B. A. Mantooth, K. F. Kelly, L. A. Bumm, J. D. Monnell, J. J. Stapleton, D. W. Price Jr., A. M. Rawlett, D. L. Allara, J. M. Tour, P. S. Weiss, "Conductance switching in single molecules through conformational changes," *Science*, vol. 292, no. 5525, pp. 2303-2307, 2001.

[122] A. Bandyopadhyay and A. J. Pal, "Multilevel conductivity and conductance switching in supramolecular structures of an organic molecule," *Appl. Phys. Lett.*, vol. 84, no. 6, pp. 999-1001, 2004.

[123] B. Mukherjee and A. J. Pal, "On the origin of multilevel conductance and memory in ultrathin organic films," *Synth. Met.*, vol. 155, no. 2, pp. 336-339, 2005.

[124] J. A. Meyers, "Switching in polyacrylonitrile," *J. Non. Cryst. Solids*, vol. 79, no. 1-2, pp. 57-74, 1986.

[125] S. L. Lim, Ling, E. Y. H. Teo, C. X. Zhu, D. S. H. Chan, Kang, and K. G. Neoh, "Conformation-induced electrical bistability in non-conjugated polymers with pendant carbazole moieties," *Chem. Mater.*, vol. 19, no. 21, pp. 5148-5157, 2007.

[126] A. Szymanski, D. C. Larson, and M. M. Labes, " a temperature-independent conducting state in tetracene thin," *Appl. Phys. Lett.*, vol. 14, no. 3, pp. 88-90, 1969.

[127] H. J. Yen and G. S. Liou, "Solution-processable triarylamine-based high-performance polymers for resistive switching memory devices," *Polym. J.*, vol. 48, no. 2, pp. 117-138, 2016.

[128] E. Lim and R. Ismail, "Conduction mechanism of valence change resistive switching memory: A survey," *Electronics*, vol. 4, no. 3, pp. 586-613, 2015.

[129] J. H. A. Smits, S. C. J. Meskers, R. A. J. Janssen, A. W. Marsman, and D. M. de Leeuw, "Electrically rewritable memory cells from poly(3-hexylthiophene) schottky diodes," *Adv. Mater.*, vol. 17, no. 9, pp. 1169-1173, 2005.

[130] D. M. Taylor and C. A. Mills, "Memory effect in the current-voltage characteristic of a low-band gap conjugated polymer," *J. Appl. Phys.*, vol. 90, no. 1, pp. 306-309, 2001.

[131] X. Zhu, J. Lee, and W. D. Lu, "Iodine vacancy redistribution in organic-inorganic Halide perovskite films and resistive switching effects," *Adv. Mater.*, vol. 29, no. 29, p. 1700527, 2017.

[132] D. Kahng and S. M. Sze, "A floating gate and its aplication to memory devices," *Bell Syst. Tech. J.*, vol. 46, no. 6, pp. 1288-1295, 1967.

[133] A. Facchetti, J. Letizia, M.-H. Yoon, M. Mushrush, H. E. Katz, and T. J. Marks, "Synthesis

and characterization of diperfluorooctyl-substituted phenylene-thiophene oligomers as n-type semiconductors. Molecular structure-film microstructure-mobility relationships, organic field-effect transistors, and transistor nonvolatile memory element," *Chem. Mater.*, vol. 16, no. 23, pp. 4715-4727, 2004.

[134] K. J. Baeg, Y. Y. Noh, H. Sirringhaus, and D. Y. Kim, "Controllable shifts in threshold voltage of top-gate polymer field-effect transistors for applications in organic nano floating gate memory," *Adv. Funct. Mater.*, vol. 20, no. 2, pp. 224-230, 2010.

[135] M. Kang, K. J. Baeg, D. Khim, Y. Y. Noh, and D. Y. Kim, "Printed, Ffexible, organic nano-floating-gate memory: effects of metal nanoparticles and blocking dielectrics on memory characteristics," *Adv. Funct. Mater.*, vol. 23, no. 28, pp. 3503-3512, 2013.

[136] T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai, and T. Someya, "Organic nonvolatile memory transistors for flexible sensor arrays," *Science*, vol. 326, no. 5959, pp. 1516-1519, 2009.

[137] L. Zhen, W. Guan, L. Shang, M. Liu, and G. Liu, "Organic thin-film transistor memory with gold nanocrystals embedded in polyimide gate dielectric," *J. Phys. D. Appl. Phys.*, vol. 41, no. 13, p. 135111, 2008.

[138] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "Metal nanocrystal memories. I. Device design and fabrication," *IEEE Trans. Electron Devices*, vol. 49, no. 9, pp. 1606-1613, 2002.

[139] C. Huang, J. E. West, and H. E. Katz, "Organic field-effect transistors and unipolar logic Gates on charged electrets from spin-on organosilsesquioxane resins," *Adv. Funct. Mater.*, vol. 17, no. 1, pp. 142-153, 2007.

[140] K. J. Baeg, Y. Y. Noh, J. Ghim, S. J. Kang, H. Lee, and D. Y. Kim, "Organic non-volatile memory based on pentacene field-effect transistors using a polymeric gate electret," *Adv. Mater.*, vol. 18, no. 23, pp. 3179-3183, 2006.

[141] M. Mushrush, A. Facchetti, M. Lefenfeld, H. E. Katz, and T. J. Marks, "Easily processable phenylene-thiophene-based organic field-effect transistors and solution-fabricated nonvolatile transistor memory elements," *J. Am. Chem. Soc.*, vol. 125, no. 31, pp. 9414-9423, 2003.

[142] T. B. Singh, N. Marjanović, G. J. Matt, N. S. Sariciftci, R. Schwödiauer, and S. Bauer, "Nonvolatile organic field-effect transistor memory element with a polymeric gate electret," *Appl. Phys. Lett.*, vol. 85, no. 22, pp. 5409-5411, 2004.

[143] M. E. Lines and A. M. Glass, *Principles and applications of ferroelectrics and related materials*. UK: Oxford University, 2001.

[144] R. C. G. Naber, C. Tanase, P. W. M. Blom, G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh, D. M. de Leeuw, "High-performance solution-processed polymer ferroelectric field-effect transistors," *Nat. Mater.*, vol. 4, no. 3, pp. 243-248, 2005.

[145] R. C. G. Naber, K. Asadi, P. W. M. Blom, D. M. de Leeuw, and B. de Boer, "Organic nonvolatile memory devices based on ferroelectricity," *Adv. Mater.*, vol. 22, no. 9, pp. 933-945, 2010.

[146] Y. Noguchi and M. Miyayama, "Large remanent polarization of vanadium-doped $Bi_4Ti_3O_{12}$," *Appl. Phys. Lett.*, vol. 78, no. 13, pp. 1903-1905, 2001.

[147] C. A. P. D. Araujo, L. D. McMillan, B. M. Melnick, J. D. Cuchiaro, and J. F. Scott, "Ferroelectric memories," *Ferroelectrics*, vol. 104, no. 1, pp. 241-256, 1990.

[148] J. F. Scott and C. A. Paz de Araujo, "Ferroelectric Memories," *Science*, vol. 246, no. 4936, pp. 1400-1405, 1989.

[149] V. Garcia, S. Fusil, K. Bouzehouane, S. Enouz-Vedrenne, N.D. Mathur, A. Barthélémy, M. Bibes, "Giant tunnel electroresistance for non-destructive readout of ferroelectric states," *Nature*, vol. 460, no. 7251, pp. 81-84, Jul. 2009.

[150] H. S. Nalwa and and Marcel Dekker (Edt.), *Ferroelectric polymers: Chemistry, physics, and applications*. New York: CRC press, 1995.

[151] S. Ducharme, T. J. Reece, C. M. Othon, and R. K. Rannow, "Ferroelectric polymer Langmuir-Blodgett films for nonvolatile memory applications," *IEEE Trans. Device Mater. Reliab.*, vol. 5, no. 4, pp. 720-735, 2005.

[152] T. Furukawa, M. Date, M. Ohuchi, and A. Chiba, "Ferroelectric switching characteristics in a copolymer of vinylidene fluoride and trifluorethylene," *J. Appl. Phys.*, vol. 56, no. 5, pp. 1481-1486, 1984.

[153] T. Furukawa, "Phenomenological aspect of a ferroelectric vinylidene fluoride/trifluoroethylene copolymer," *Ferroelectrics*, vol. 57, no. 1, pp. 63-72, 1984.

[154] T. Furukawa, H. Matsuzaki, M. Shiina, and Y. Tajitsu, "Nanosecond switching in thin fims of vinylidene fluoride/trilluoroethylene copolymers," *Jpn. J. Appl. Phys.*, vol. 24, no. Part 2, No. 8, pp. L661-L662, 1985.

[155] A. V. Bune, V.M. Fridkin, S. Ducharme, L.M. Blinov, S.P. Palto, A. V. Sorokin, S.G. Yudin, and A. Zlatkin, "Two-dimensional ferroelectric films," *Nature*, vol. 391, no. 6670, pp. 874-877, 1998.

[156] K. Kimura and H. Ohigashi, "Polarization behavior in vinylidene fluoride-trifluoroethylene copolymer thin films," *Jpn. J. Appl. Phys.*, vol. 25, no. 3, pp. 383-387, 1986.

[157] Y. Tajitsu, "Effects of thickness on ferroelectricity in vinylidene fluoride and trifluoroethylene copolymers," *Jpn. J. Appl. Phys.*, vol. 34, no. 9B, pp. 5418-5423, 1995.

[158] G. Vizdrik, S. Ducharme, V. M. Fridkin, and S. G. Yudin, "Kinetics of ferroelectric switching in ultrathin films," *Phys. Rev. B*, vol. 68, no. 9, p. 094113, 2003.

[159] Q. M. Zhang, H. Xu, F. Fang, Z. Y. Cheng, F. Xia, and H. You, "Critical thickness of crystallization and discontinuous change in ferroelectric behavior with thickness in ferroelectric polymer thin films," *J. Appl. Phys.*, vol. 89, no. 5, pp. 2613-2616, 2001.

[160] S. Fujisaki, H. Ishiwara, and Y. Fujisaki, "Low-voltage operation of ferroelectric poly(vinylidene fluoride-trifluoroethylene) copolymer capacitors and metal-ferroelectric-insulator-semiconductor diodes," *Appl. Phys. Lett.*, vol. 90, no. 16, p. 162902, 2007.

[161] S.J. Kang, I. Bae, Y.J. Park, T.H. Park, J. Sung, S.C. Yoon, K.H. Kim, D.H. Choi, C. Park, "Non-volatile ferroelectric poly(vinylidene fluoride-co-trifluoroethylene) memory based on a single-crystalline tri-isopropylsilylethynyl pentacene field-effect transistor," *Adv. Funct. Mater.*, vol. 19, no. 10, pp. 1609-1616, 2009.

[162] H. Xu, J. Zhong, X. Liu, J. Chen, and D. Shen, "Ferroelectric and switching behavior of poly(vinylidene fluoride-trifluoroethylene) copolymer ultrathin films with polypyrrole interface," *Appl. Phys. Lett.*, vol. 90, no. 9, p. 092903, 2007.

[163] R. C. G. Naber, P. W. M. Blom, A. W. Marsman, and D. M. de Leeuw, "Low voltage switching of a spin cast ferroelectric polymer," *Appl. Phys. Lett.*, vol. 85, no. 11, pp. 2032-

2034, 2004.

[164] K. Kim and Y. J. Song, "Integration technology for ferroelectric memory devices," *Microelectron. Reliab.*, vol. 43, no. 3, pp. 385-398, 2003.

[165] H. Gudesen, P. Nordal, and G. Leistad, "WO 99/12170," 1999.

[166] M. Thompson, R. Womack, and G. Gustafsson, "WO 02/25665," 2002.

[167] P. Nordal, P. Bröms, M. Johansson, and H. Gudesen, "WO 02/05288," 2002.

[168] S. Y Wu, "A new ferroelectric memory device, metal-ferroelectric-semiconductor transistor," *IEEE Trans. Electron Devices*, vol. 21, no. 8, pp. 499-504, 1974.

[169] Y. Arimoto and H. Ishiwara, "Current status of ferroelectric random-access memory," *MRS Bull.*, vol. 29, no. 11, pp. 823-828, 2004.

[170] T. Furukawa, "Ferroelectric properties of vinylidene fluoride copolymers," *Phase Transitions*, vol. 18, no. 3-4, pp. 143-211, 1989.

[171] S. Steudel, S. De Vusser, S. De Jonge, D. Janssen, S. Verlaak, J. Genoe, and P. Heremans, "Influence of the dielectric roughness on the performance of pentacene transistors," *Appl. Phys. Lett.*, vol. 85, no. 19, p. 4400, 2004.

[172] D. J. Gundlach, T. N. Jackson, D. G. Schlom, and S. F. Nelson, "Solvent-induced phase transition in thermally evaporated pentacene films," *Appl. Phys. Lett.*, vol. 74, no. 22, pp. 3302-3304, 1999.

[173] M. H. Kim, G. J. Lee, C. M. Keum, and S. D. Lee, "Concept of rewritable organic ferroelectric random access memory in two lateral transistors-in-one cell architecture," *Semicond. Sci. Technol.*, vol. 29, no. 2, p. 025004, 2014.

[174] T. N. Ng, B. Russo, B. Krusor, R. Kist, and A. C. Arias, "Organic inkjet-patterned memory array based on ferroelectric field-effect transistors," *Org. Electron.*, vol. 12, no. 12, pp. 2012-2018, 2011.

[175] Y. Watanabe, "Review of resistance switching of ferroelectrics and oxides in quest for Uunconventional Eelectronic mechanisms," *Ferroelectrics*, vol. 349, no. 1, pp. 190-209, 2007.

[176] P. W. M. Blom, R. M. Wolf, J. F. M. Cillessen, and M. P. C. M. Krijn, "Ferroelectric Schottky diode," *Phys. Rev. Lett.*, vol. 73, no. 15, pp. 2107-2110, 1994.

[177] K. Asadi, D. M. de Leeuw, B. de Boer, and P. W. M. Blom, "Organic non-volatile memories from ferroelectric phase-separated blends," *Nat. Mater.*, vol. 7, no. 7, pp. 547-550, 2008.

[178] M.L. Tietze, J. Benduhn, P. Pahner, B. Nell, M. Schwarze, H. Kleemann, M. Krammer, K. Zojer, K. Vandewal, and K. Leo, "Elementary steps in electrical doping of organic semiconductors," *Nat. Commun.*, vol. 9, no. 1, p. 1182, 2018.

[179] X. Zhou, J. Blochwitz, M. Pfeiffer, A. Nollau, T. Fritz, and K. Leo, "Enhanced hole injection into amorphous hole-transport layers of organic light-emitting diodes using controlled p-type doping," *Adv. Funct. Mater.*, vol. 11, no. 4, pp. 310-314, 2001.

[180] H. B. Michaelson, "The work function of the elements and its periodicity," *J. Appl. Phys.*, vol. 48, no. 11, pp. 4729-4733, 1977.

[181] P. K. Koech, A. B. Padmaperuma, L. Wang, J. S. Swensen, E. Polikarpov, J. T. Darsell, J. E. Rainbolt, and D. J. Gaspar, "Synthesis and application of 1,3,4,5,7,8-hexafluorotetracyanonaphthoquinodimethane (F6-TNAP): A conductivity dopant for

organic light-emitting devices," *Chem. Mater.*, vol. 22, no. 13, pp. 3926-3932, 2010.

[182] R. A. Belisle, P. Jain, R. Prasanna, T. Leijtens, and M. D. McGehee, "Minimal effect of the hole-transport material ionization potential on the open-cCircuit voltage of perovskite solar cells," *ACS Energy Lett.*, vol. 1, no. 3, pp. 556-560, 2016.

[183] Z. Bin, G. Dong, P. Wei, Z. Liu, D. Zhang, R. Su, Y. Qiu, and L. Duan, "Making silver a stronger n-dopant than cesium via in situ coordination reaction for organic electronics," *Nat. Commun.*, vol. 10, no. 1, p. 866, 2019.

[184] K. S. Yook, S. O. Jeon, S. Y. Min, J. Y. Lee, H. J. Yang, T. Noh, S. K. Kang, T. W. Lee, "Highly efficient p-i-n and tandem organic light-emitting devices using an air-stable and low-temperature-evaporable metal azide as an n-dopant," *Adv. Funct. Mater.*, vol. 20, no. 11, pp. 1797-1802, 2010.

[185] J. H. Jou, S. Kumar, A. Agrawal, T. H. Li, and S. Sahoo, "Approaches for fabricating high efficiency organic light emitting diodes," *J. Mater. Chem. C*, vol. 3, no. 13, pp. 2974-3002, 2015.

[186] M. Johnson, A. Al-Shamma, D. Bosch, M. Crowley, M. Farmwald, L. Fasoli, A. Ilkbahar, B. Kleveland, T. Lee, Tz-yi Liu, Quang Nguyen, R. Scheuerlein, K. So, and T. Thorp, "512-Mb PROM with a three-dimensional array of diode/antifuse memory cells," *IEEE J. Solid-State Circuits*, vol. 38, no. 11, pp. 1920-1928, 2003.

[187] A. Fischer, P. Pahner, B. Lüssem, K. Leo, R. Scholz, T. Koprucki, J. Fuhrmann, K. Gärtner, A. Glitzky, "Self-heating effects in organic semiconductor crossbar structures with small active area," *Org. Electron.*, vol. 13, no. 11, pp. 2461-2468, 2012.

[188] H. Klauk, (Ed.), *Organic electronics: Materials, manufacturing, and applications*. Weinheim: Wiley-VCH Verlag GmbH & Co. KGaA, 2006.

[189] B. Lüssem, M. Riede, and K. Leo, "Doping of organic semiconductors, " *Phys. Status Solidi A*, vol. 210, no. 1. pp. 9-43, 2013.

[190] G. Gelinck, P. Heremans, K. Nomoto, and T. D. Anthopoulos, "Organic transistors in optical displays and microelectronic applications," *Adv. Mater.*, vol. 22, no. 34, pp. 3778-3798, 2010.

[191] M. Diethelm, L. Penninck, S. Altazin, R. Hiestand, C. Kirsch, and B. Ruhstaller, "Quantitative analysis of pixel crosstalk in AMOLED displays," *J. Inf. Disp.*, vol. 19, no. 2, pp. 61-69, 2018.

[192] W. Brütting, S. Berleb, and A. G. Mückl, "Device physics of organic light-emitting diodes based on molecular materials," *Org. Electron.*, vol. 2, no. 1, pp. 1-36, 2001.

[193] P. H. Nguyen, S. Scheinert, S. Berleb, W. Brüiting, and G. Paasch, "The influence of deep traps on transient current-voltage characteristics of organic light-emitting diodes," *Org. Electron. physics, Mater. Appl.*, vol. 2, no. 3-4, pp. 105-120, 2001.

[194] A. Fischer, M. Pfalz, K. Vandewal, S. Lenk, M. Liero, A. Glitzky, and S. Reineke, "Full Electrothermal OLED Model Including Nonlinear Self-heating Effects," *Phys. Rev. Appl.*, vol. 10, no. 1, p. 1, 2018.

[195] G. A. H. Wetzelaer, M. Kuik, H. T. Nicolai, and P. W. M. Blom, "Trap-assisted and Langevin-type recombination in organic light-emitting diodes," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 83, no. 16, pp. 1-5, 2011.

[196] J. Lee, J. D. Cohen, and W. N. Shafarman, "The determination of carrier mobilities in CIGS

photovoltaic devices using high-frequency admittance measurements," *Thin Solid Films*, vol. 480-481, pp. 336-340, 2005.

[197] L. Xu, J. Wang, and J. W. P. Hsu, "Transport effects on capacitance-frequency analysis for defect characterization in organic photovoltaic devices," *Phys. Rev. Appl.*, vol. 6, no. 6, pp. 1-10, 2016.

[198] M. L. Tietze, L. Burtone, M. Riede, B. Lüssem, and K. Leo, "Fermi level shift and doping efficiency in p-doped small molecule organic semiconductors: A photoelectron spectroscopy and theoretical study," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 86, no. 3, pp. 1-12, 2012.

[199] T. Menke, D. Ray, H. Kleemann, M. P. Hein, K. Leo, and M. Riede, "Highly efficient p-dopants in amorphous hosts," *Org. Electron. physics, Mater. Appl.*, vol. 15, no. 2, pp. 365-371, 2014.

[200] E. Fred Schubert, *Light-Emitting Diodes*. UK: Cambridge University, 2006.

[201] X. Quo and E. F. Schubert, "Current crowding in GaN/InGaN light emitting diodes on insulating substrates," *J. Appl. Phys.*, vol. 90, no. 8, pp. 4191-4195, 2001.

[202] I. Slowik, A. Fischer, H. Fröb, S. Lenk, S. Reineke, and K. Leo, "Novel organic light-emitting diode design for future lasing applications," *Org. Electron. physics, Mater. Appl.*, vol. 48, pp. 132-137, 2017.

[203] S. Hamilton, *An analog electronics companion: Basic circuit design for engineers and scientists*. UK: Cambridge University, 2007.

[204] M. T. Bohr, "Interconnect scaling-the real limiter to high performance ULSI," 2002, pp. 241-244.

[205] B. Lüssem, C. M. Keum, D. Kasemann, B. Naab, Z. Bao, and K. Leo, "Doped organic transistors," *Chemical Reviews*, vol. 116, no. 22. pp. 13714-13751, 2016.

[206] K. Walzer, B. Männig, M. Pfeiffer, and K. Leo, "Highly efficient organic devices based on electrically doped transport layers," *Chemical Reviews*, vol. 107, no. 4. pp. 1233-1271, 2007.

[207] J. V Li, A. M. Nardes, Z. Liang, S. E. Shaheen, B. A. Gregg, and D. H. Levi, "Simultaneous measurement of carrier density and mobility of organic semiconductors using capacitance techniques," *Org. Electron. physics, Mater. Appl.*, vol. 12, no. 11, pp. 1879-1885, 2011.

[208] A. You, M. A. Y. Be, and I. In, "Controlled formation of charge depletion zones by molecular doping in organic pin-diodes and its description by the Mott-Schottky relation," *J. Appl. Phys.*, vol. 111, no. 12, 2012.

[209] J. Scherbel, P. H. Nguyen, G. Paasch, W. Brütting, and M. Schwoerer, "Temperature dependent broadband impedance spectroscopy on poly-(p-phenylene-vinylene) light-emitting diodes," *J. Appl. Phys.*, vol. 83, no. 10, pp. 5045-5055, 1998.

[210] J. Fischer, D. Ray, H. Kleemann, P. Pahner, M. Schwarze, C. Koerner, K. Vandewal, and K. Leo, "Density of states determination in organic donor-acceptor blend layers enabled by molecular doping," *J. Appl. Phys.*, vol. 117, no. 24, 2015.

[211] S. Nowy, W. Ren, A. Elschner, W. Lövenich, and W. Brütting, "Impedance spectroscopy as a probe for the degradation of organic light-emitting diodes," *J. Appl. Phys.*, vol. 107, no. 5, 2010.

[212] P. P. Boix, J. Ajuria, I. Etxebarria, R. Pacios, and G. Garcia-Belmonte, "Kinetics of occupancy of defect states in poly(3-hexylthiophene):fullerene solar cells," *Thin Solid Films*,

vol. 520, no. 6, pp. 2265-2268, 2012.

[213] J. A. Carr, M. Elshobaki, and S. Chaudhary, "Deep defects and the attempt to escape frequency in organic photovoltaic materials," *Appl. Phys. Lett.*, vol. 107, no. 20, 2015.

[214] T. Walter, R. Herberholz, C. Müller, and H. W. Schock, "Determination of defect distributions from admittance measurements and application to Cu(In,Ga)Se2 based heterojunctions," *J. Appl. Phys.*, vol. 80, no. 8, pp. 4411-4420, 1996.

[215] V.C. Nikolis, J. Benduhn, F. Holzmueller, F. Piersimoni, M. Lau, O. Zeika, D. Neher, C. Koerner, D. Spoltore, and K. Vandewal, "Reducing Voltage Losses in Cascade Organic Solar Cells while Maintaining High External Quantum Efficiencies," *Adv. Energy Mater.*, vol. 7, no. 21, pp. 1-8, 2017.

[216] S. Schubert, Y.H. Kim, T. Menke, A. Fischer, R. Timmreck, L. M, Meskamp, and K. Leo, "Highly doped fullerene C_{60} thin films as transparent stand alone top electrode for organic solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 118, pp. 165-170, 2013.

[217] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80-83, 2008.

[218] E. Linn, R. Rosezin, C. Kügeler, and R. Waser, "Complementary resistive switches for passive nanocrossbar memories," *Nat. Mater.*, vol. 9, no. 5, pp. 403-406, 2010.

[219] S. Möller, C. Perlov, W. Jackson, C. Taussig, and S. R. Forrest, "A polymer/semiconductor write-once read-many-times memory," *Nature*, vol. 426, no. 6963, pp. 166-169, 2003.

[220] C. Liu, X. Yan, X. Song, S. Ding, D. W. Zhang, and P. Zhou, "A semi-floating gate memory based on van der Waals heterostructures for quasi-non-volatile applications," *Nat. Nanotechnol.*, vol. 13, no. 5, pp. 404-410, 2018.

[221] W. Y. Lee, H. C. Wu, C. Lu, B. D. Naab, W. C. Chen, and Z. Bao, "N-type doped conjugated polymer for nonvolatile memory," *Adv. Mater.*, vol. 29, no. 16, pp. 1-7, 2017.

[222] J. S. Lee, "Review paper: Nano-floating gate memory devices," *Electron. Mater. Lett.*, vol. 7, no. 3, pp. 175-183, 2011.

[223] Y. Ji, D. F. Zeigler, D. S. Lee, H. Choi, A .K. Y. Jen, H. C. Ko, and T. W. Kim, "Flexible and twistable non-volatile memory cell array with all-organic one diode-one resistor architecture," *Nat. Commun.*, vol. 4, pp. 1-7, 2013.

[224] J. Wu, A. Fischer, and S. Reineke, "Investigating free charge-carrier recombination in organic LEDs using open-circuit conditions," *Advanced Optical Materials*, vol. 7, no. 7. 2019.

[225] F. Zhou, Z. Zhou, J. Chen, T.H. Choy, J. Wang, N. Zhang, Z. Lin, S. Yu, J. Kang, H.-S.P. Wong, and Y. Chai, "Optoelectronic resistive random access memory for neuromorphic vision sensors," *Nat. Nanotechnol.*, 2019.

[226] S. Chen, Z. Lou, D. Chen, and G. Shen, "An artificial flexible visual memory system based on an UV-motivated memristor," *Adv. Mater.*, vol. 30, no. 7, pp. 1-9, 2018.

[227] Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G. L. Li, H. L. Xin, R. S. Williams, Q. Xia, and J.J . Yang, "Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing," *Nat. Mater.*, vol. 16, no. 1, pp. 101-108, 2017.

[228] Y. V. D. Burgt, E. Lubberman, E. J. Fuller, S. T. Keene, G. C. Faria, S. Agarwal, M. J.

Marinella, A. A. Talin, and A. Salleo, "A non-volatile organic electrochemical device as a low-voltage artificial synapse for neuromorphic computing," *Nat. Mater.*, vol. 16, no. 4, pp. 414-418, 2017.

[229] J. R. Hughes, "Post-tetanic potentiation," *Physiol. Rev.*, vol. 38, no. 1, pp. 91-113, 1958.

[230] T. Ohno, T. Hasegawa, T. Tsuruoka, K. Terabe, J. K. Gimzewski, and M. Aono, "Short-term plasticity and long-term potentiation mimicked in single inorganic synapses," *Nat. Mater.*, vol. 10, no. 8, pp. 591-595, 2011.

[231] E. J. Fuller, S. T. Keene, A. Melianas, Z. Wang, S. Agarwal, Y. Li, Y. Tuchman, C. D. James, M. J. Marinella, J. J. Yang, A. Salleo, and A. A. Talin, "Parallel programming of an ionic floating-gate memory array for scalable neuromorphic computing," *Science*, vol. 364, no. 6440, pp. 570-574, 2019.

List of Figures

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List of Abbreviations

pinMOS	p-i-n-metal-oxide-semiconductor
OLED	organic light-emitting diode
OFET	organic field-effect transistor
OSC	organic solar cell
DRAM	dynamic random access memory
ReRAM	resistive random access memory
FeRAM	ferroelectric random access memory
FeFET	ferroelectric field-effect transistor
ONVM	organic non-volatile memory
MOS	metal-oxide-semiconductor
HOMO	highest occupied molecular orbital
LUMO	lowest unoccupied molecular orbital
DOS	density of states
ILC	injection limited current
SCLC	space charge limited current
EML	emission layer
EBL	electron blocking layer
HBL	hole blocking layer
RAM	random access memory
DRAM	dynamic random access memory
SRAM	static random-access memory
ROM	read-only memory
EEPROM	electrically erasable read-only memory

EPPOM	electrically programmable read-only memory
1D-1R	one diode-one resistor
1T-1R	one transistor-one resistor
NP	nanoparticle
NDR	negative differential resistance
LRS	low-resistance state
HRS	high-resistance state
CT	charge transfer
FN	Fowler-Nordheim
RB	Rose Bengal
MNOS	metal-nitride-oxide-silicon
ALD	atomic layer deposition
UHV	ultra-high vacuum
QCM	quartz crystal microbalance
IV	current-voltage
SMU	source-measuring unit
AC	alternative current
HTM	hole transpot material
ETM	electron transpot material
HBM	hole blocking material
EBM	electron blocking material
OMD	organic memory device
RC	resistor-capacitor
IS	impedance spectroscopy
CF	capacitance-frequency
CMOS	complementary metal-oxide-semiconductor

LTP	long-term plasticity
STP	short-term plasticity
STDP	spike timing dependent plasticity
DC	direct current

Publications

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Yichu Zheng, Axel Fischer, Natalia Sergeeva, Sebastian Reineke, Stefan C. B. Mannsfeld, Exploiting lateral current flow due to doped layers in semiconductor devices having crossbar electrodes, ***Org. Electron.***, 2019, 65, 82-90.

Cecilia Teixeira da Rocha, Katherina Haase, **Yichu Zheng**, Markus Löffler, Mike Hambsch, Stefan C. B. Mannsfeld, Solution coating of small molecule/polymer blends enabling ultralow voltage and high-mobility organic transistors. ***Adv. Electron. Mater.***, 2018, 4, 1800141.

Katherina Haase, Cecilia Teixeira da Rocha, Christoph Hauenstein, **Yichu Zheng**, Mike Hambsch, Stefan C. B. Mannsfeld, High-mobility, solution-processed organic field-effect transistors from C8-BTBT:polystyrene blends. ***Adv. Electron. Mater.***, 2018, 4, 1800076.

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