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RESEARCH PAPER

Dual-band impedance transformation networks for integrated power amplifiers

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This paper shows that the two most common impedance transformation networks for power amplifiers (PAs) can be designed to achieve optimum transformation at two frequencies. Hence, a larger bandwidth for the required impedance transformation ratio is achieved. A design procedure is proposed, which takes imperfections like losses into account. Furthermore, an analysis method is presented to estimate the maximum uncompressed output power of a PA with respect to frequency. Based on these results, a fully integrated PA with a dual-band impedance transformation network is designed and its functionality is proven by large signal measurement results. The amplifier covers the frequency band from 450 MHz to 1.2 GHz (3 dB bandwidth of the output power and efficiency), corresponding to a relative bandwidth of more than 100%. It delivers 23.7 dBm output power in the 1 dB compression point, having a power-added efficiency of 33%.

Keywords: Power amplifiers and linearizers, Modeling, Simulation and characterizations of devices and circuits

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I. INTRODUCTION

Current wireless communication and broadcast standards such as Long Term Evolution (LTE) or Digital Video Broadcasting – Terrestrial (DVB-T) allow the operation in a wide frequency range with a demand for a high linearity power amplifier (PA). In addition, those standards require a certain output power of the transmitter. Since the breakdown voltage of the transistors is continuously decreasing due to further scaling of the technology, the load at the transistor of the PA must be very low-ohmic to still achieve the required output power. Thus the design of the impedance transformation network gets more challenging. Especially, bandwidth and impedance transformation ratio are contradictory.

To circumvent this problem, transformers and dual-band impedance transformation networks can be used. The usage of transformers is very promising [1], but they can hardly be efficiently integrated for circuits in the sub- and low GHz range. Dual-band impedance transformation networks have been investigated mainly for low-noise amplifiers (LNA) [2]. For PAs, the published approaches use either separated signal paths [3, 4] or are based on discrete passives [5]. Dual-band impedance transformation networks are seldom applied for fully integrated PAs since they usually require more bulky inductors [6] which increases chip size and which makes them usually less efficient than an impedance transformation network for a single frequency.

We will show that already the common impedance transformation networks for PAs have the ability for dual-band operation. Hence, we propose a very flexible design procedure that can also take imperfections like losses into account. Based on that, the two most common networks are discussed. Finally, the theory is validated by measurement results of an integrated PA for DVB-T, which can cover more than the UHF IV and V band.

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II. DESIGN

A) Architecture

For PAs, LCL, or LLC impedance transformation networks like shown in Fig. 1 are usually used. In this regard, the bias inductor L_B is often considered as an unavoidable element for biasing since it does not directly contribute to the impedance transformation. Its inductance is often designed such that it compensates the parasitic capacitance C_T of the transistor.

In contrast to this, we propose to design the inductance L_B and the capacitance C_T to achieve the desired impedance transformation at two frequencies. Therefore, no additional inductor is required and the operating band is enlarged. The symbols introduced in Fig. 2 are used for further calculations.

B) Design of the network

To achieve the maximum uncompressed output power, the load at the intrinsic transistor has to be resistive and has to fit to the operating point [7]. For the classical design approach, this is only ensured for a single frequency. But the applied networks have the ability to implement the required load impedance for two frequencies. Therefore, the input impedance of

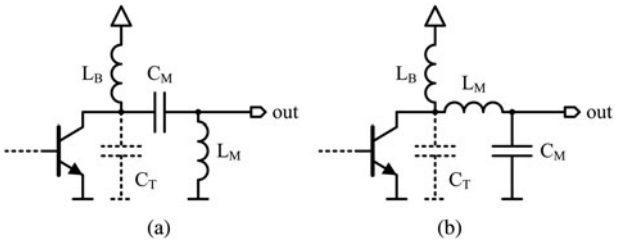

Fig. 1. LCL and LLC impedance transformation networks of typical PAs. (a) LCL, (b) LLC.

the transformation networks is considered. For the LCL network it is given by

$$Z_i(\omega, Z_a) = \frac{1}{\frac{1}{j\omega L_B} + j\omega C_T + 1/\left(\frac{1}{j\omega C_M} + \frac{1}{1/(j\omega L_M) + 1/Z_a}\right)} \tag{1}$$

and for the LLC network by

$$Z_i(\omega, Z_a) = \frac{1}{\frac{1}{j\omega L_B} + j\omega C_T + 1/\left(j\omega L_M + \frac{1}{j\omega C_M + 1/Z_a}\right)}, \tag{2}$$

where Z_a is the load connected to the transformation network, which is typically 50 Ω.

To achieve dual-band operation, the input impedance of the transformation network has to reveal a certain value for each of the two frequencies. Hence the problem is given by

$$Z_i(2\pi f_1, Z_{a1}) \stackrel{!}{=} Z_{i1} \text{ and } Z_i(2\pi f_2, Z_{a2}) \stackrel{!}{=} Z_{i2}, \tag{3}$$

where the impedances Z_{i1} and Z_{i2} are the required load impedances of the transistor and Z_{a1} and Z_{a2} are the externally connected load impedances for the two frequencies of interest, f_1 and f_2. Considering the real and the imaginary parts, those definitions give four equations that are sufficient to solve the problem for the four real parameters L_B, C_T, C_M, and L_M.

Unfortunately, the problem is nonlinear, but a numerical solution can be found by appropriate mathematical tools. Therefore, it is beneficial to normalize the problem with respect to frequency and impedance level. We normalized the frequencies by

$$f_{norm} = \sqrt{f_1 \cdot f_2} \tag{4}$$

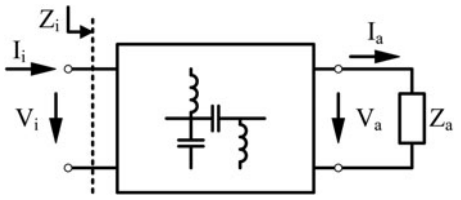

Fig. 2. Definition of the symbols.

and the impedances by

$$R_{norm} = \sqrt[4]{|Z_{i1}| \cdot |Z_{i2}| \cdot |Z_{a1}| \cdot |Z_{a2}|} \tag{5}$$

to achieve a good accuracy of the solution.

For example, the parameters of a lossless LCL network that yields an impedance transformation from 50 to 13 Ω at 600 and 700 MHz are

$$\begin{aligned} L_B &= 1.75\,\text{nH}, \quad C_T = 29.6\,\text{pF}, \\ C_M &= 10.4\,\text{pF}, \quad L_M = 6.74\,\text{nH}. \end{aligned} \tag{6}$$

Unfortunately, the quality factor of integrated inductors at those frequencies is just in a range of 8–10. For single-frequency impedance transformation networks the impact of the equivalent series resistances R_B and R_M is small but for the dual-band approach they should be considered. The problem is not getting more complicated by introducing series resistors into Eq. (1). Thus the values of the given example change to

$$\begin{aligned} L_B &= 2.42\,\text{nH}, \quad R_B = 1.3\,\Omega, \quad C_T = 19.6\,\text{pF}, \\ C_M &= 10.2\,\text{pF}, \quad L_M = 7.16\,\text{nH}, \quad R_M = 2.9\,\Omega \end{aligned} \tag{7}$$

assuming a quality factor of 8 and 10 at the frequency f_2 for L_B and L_M, respectively.

Finally, the calculated parameters of the impedance transformation network implement the required impedances at two frequencies. The effect on the compression of the PA around these frequencies and the efficiency of the impedance transformation will be investigated in the following section.

C) Analysis of the compression

One of the main ideas of the load line theory [7] is to design the load such that the current compression and the voltage compression happen at the same level of excitation. Current compression happens when the transistor switches off. The voltage compression is introduced by bringing the bipolar or the MOS transistor into saturation or into the triode region, respectively. Assuming linear operation up to one or the other compression effect, the maximum uncompressed output power can be calculated as a function of the load impedance and the operating point.

The transfer function from the voltage at input to the voltage at the output of the impedance transformation network is required for this calculation and is for the LCL network

$$v_{ai} = \frac{V_a}{V_i} = \frac{j\omega C_M}{j\omega C_M + 1/Z_a + 1/(j\omega L_M)} \tag{8}$$

and for the LLC network

$$v_{ai} = \frac{V_a}{V_i} = \frac{1}{1 + j\omega L_M(j\omega C_M + 1/Z_a)}. \tag{9}$$

The maximum voltage amplitude $\hat{V}_{i,max}$ at the transistor is

$$\hat{V}_{i,max} = V_{DC} - V_{sat} \tag{10}$$

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with the supply voltage V_{DC} and the saturation voltage V_{sat}. For class A amplifiers, the maximum current amplitude $\hat{I}_{i,max}$ is given by the operating point current $I_{C,OP}$ of the transistor and is

$$\hat{I}_{i,max} = I_{C,OP}. \tag{11}$$

Now, the maximum uncompressed output power can be calculated for voltage and for current compression, which is

$$P_{a,V} = \frac{1}{2}|v_{ai}(\omega) \cdot \hat{V}_{i,max}|^2 \cdot \Re(1/Z_a) \quad \text{and} \tag{12}$$

$$P_{a,C} = \frac{1}{2}|v_{ai}(\omega) \cdot Z_i(\omega) \cdot \hat{I}_{i,max}|^2 \cdot \Re(1/Z_a). \tag{13}$$

The achieved output power is the minimum of those two. The curves of the two output powers for the lossless and the lossy case are illustrated in Fig. 3, where the powers are normalized to the maximum uncompressed power the transistor can deliver, which is

$$P_{i,max} = \frac{1}{2}\hat{V}_{i,max} \cdot \hat{I}_{i,max}. \tag{14}$$

The two curves for either the lossless or the lossy case intersect at the frequencies, at which the load is designed to fit to the operating point. These are the points of maximum uncompressed output power of the transistor. The degradation of the efficiency at these frequencies is only introduced by the losses of the transformation network. At all other frequencies the efficiency is further reduced by deviations from the optimum load for the transistor.

It can be seen that for the lossless case the curves for the LCL and LLC networks are similar. This is plausible since the LCL network can be transformed to the LLC network by the low-pass high-pass transformation [8]. But for the lossy case, they differ. It is an interesting fact that the efficiency of the impedance transformation network at the designed frequencies is equal for the LLC network but not for the LCL network. However, the maximum efficiency of the LCL network is higher than of the LLC network. In contrast to this, it can be shown that the efficiency of an LLC and an LCL network is equal for the single-frequency approach for equal quality factors of the inductors.

If now the impedance transformation network is considered in combination with the amplifier, it is convenient to describe the amplifier with its Y parameters given by

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} I_1 \\ -I_i \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = Y \begin{pmatrix} V_1 \\ V_i \end{pmatrix}. \tag{15}$$

Then, the voltage gain from the input of the amplifier to the voltage at the load is

$$v_{a1}(\omega) = \frac{V_a}{V_1} = v_{ai}(\omega)\frac{-Y_{21}}{1/Z_i + Y_{22}}. \tag{16}$$

From this, the power at the load can be expressed by

$$P_a = |V_a|^2 \Re(1/Z_a) = \left| v_{ai}(\omega)\frac{Y_{21}}{1/Z_i + Y_{22}} V_1 \right|^2 \Re(1/Z_a). \tag{17}$$

For the assumption that the voltage gain from the generator's open circuit voltage V_o to the voltage V_1 is frequency independent, e.g. by a broadband active driver, the transducer gain G_T is proportional to

$$G_T \propto \left| v(\omega)\frac{Y_{21}}{1/Z_i + Y_{22}} \right| \Re(1/Z_a). \tag{18}$$

If Y_{22} is negligible and if Y_{21} is constant and taking Eq. (13) into account, it reveals that

$$G_T \propto P_{a,C}. \tag{19}$$

Under all these conditions, the transducer gain can be used for verification.

Although the given relation exists, we like to point out that this is only valid for all given assumptions and that this just describes one of the two effects leading to compression. Hence, proving the bandwidth of PAs only by measuring the small-signal transducer gain is not possible.

The whole design approach is neither limited to PA applications nor to the discussed topologies. It can be easily extended to other structures that are more suited for dual-band operation and it can also include transmission lines.

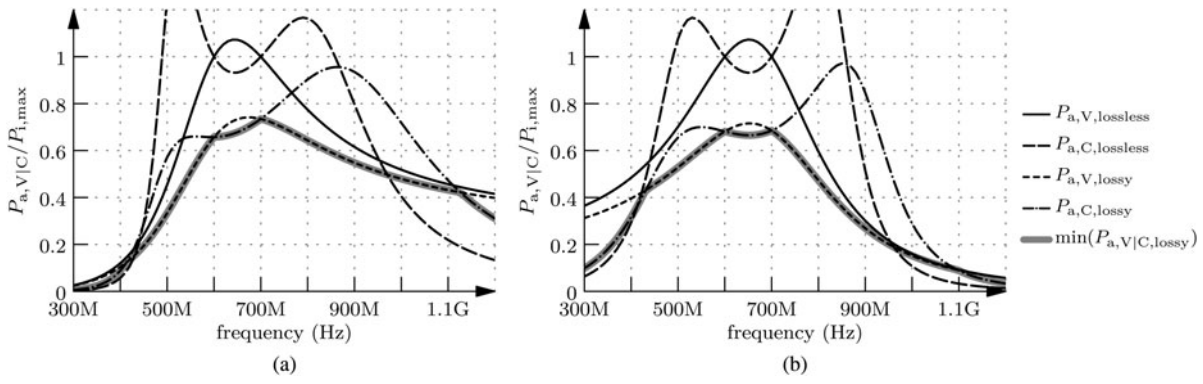

Fig. 3. Curves of the calculated output power for LCL and LLC networks for the cases of voltage and current compression for a lossless and a lossy impedance transformation network; the achieved output power is the minimum of the corresponding curves shown as bold gray line for the lossy case. (a) LCL, (b) LLC.

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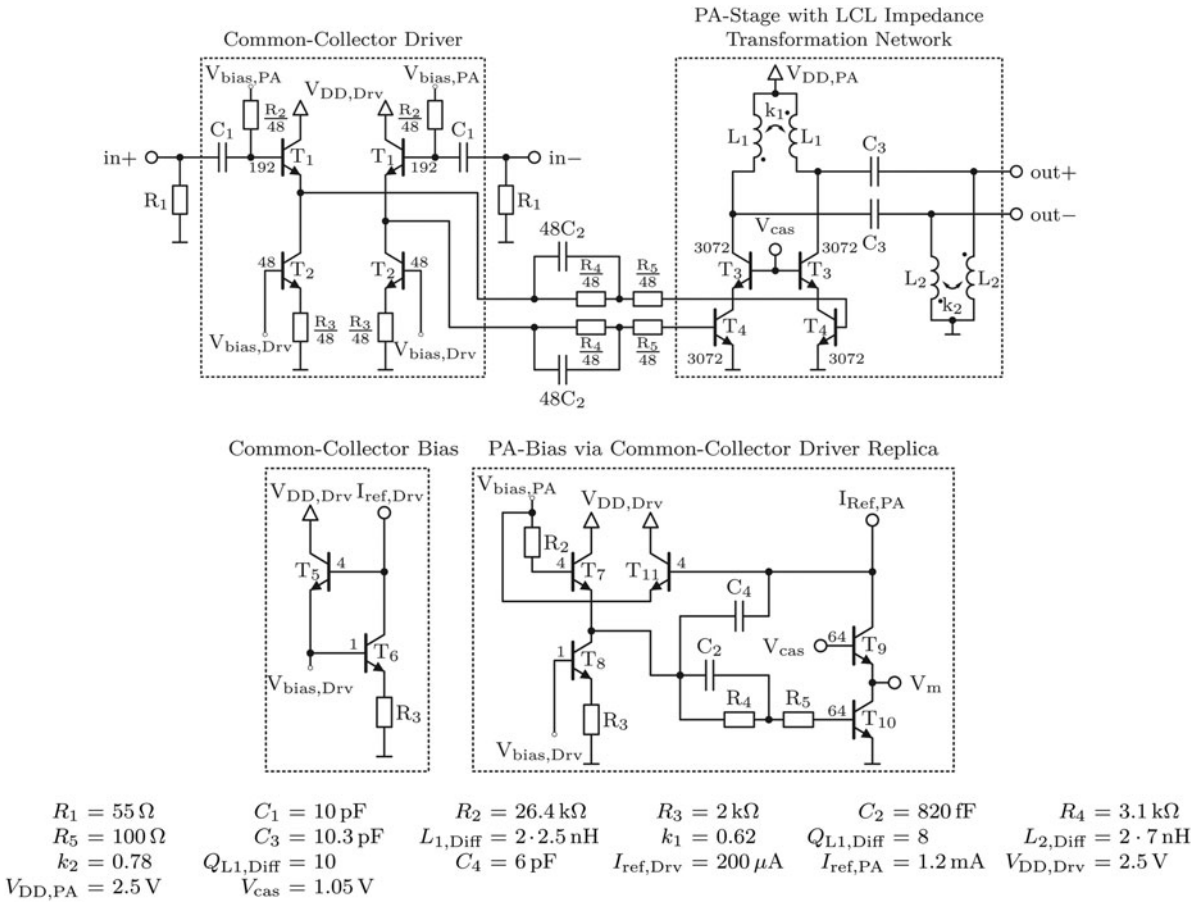

Fig. 4. Schematic representation of the whole differential power amplifier and bias circuits.

For PA applications, alternative networks require more inductors, which increase chip size and which are therefore not beneficial. However, since the transformation network relies on C_T as a parameter of the transistor, it has to be pointed out that in case of C_T being too small to allow the desired transformation at two frequencies, other options can be considered such as changing the size or layout of the transistor array, using another arrangement of L_M and C_M or changing the transformation frequencies.

III. VERIFICATION

A) Description of the integrated circuit

A chip using an LCL network designed with the described approach was implemented in IHP's 250 nm SiGe BiCMOS technology. The schematic representation of the PA is shown in Fig. 4. It consists of a common-collector driver stage and the cascode power stage with the described dual-band output network. Furthermore, biasing networks

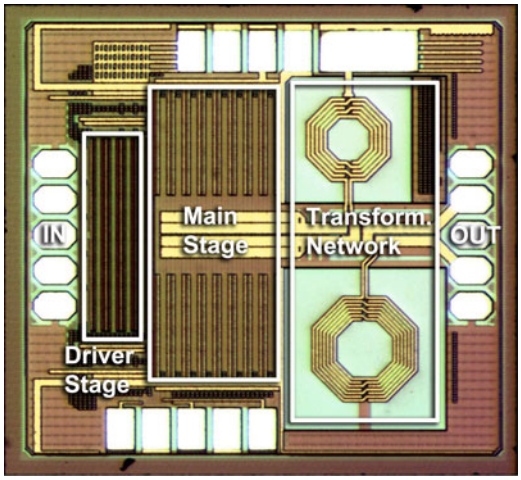

Fig. 5. Chip micrograph, size 1.3 × 1.2 mm².

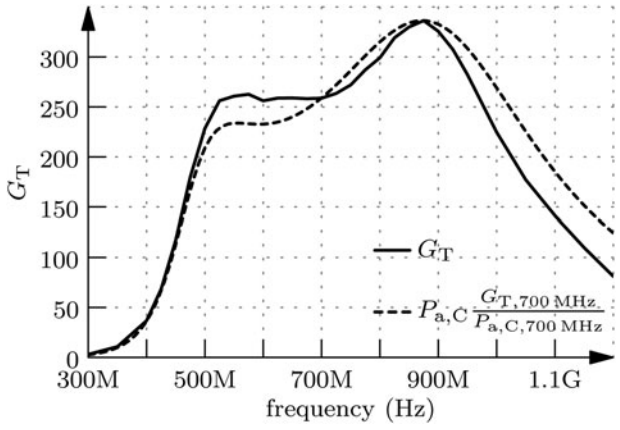

Fig. 6. Measured and calculated transducer gain versus frequency.

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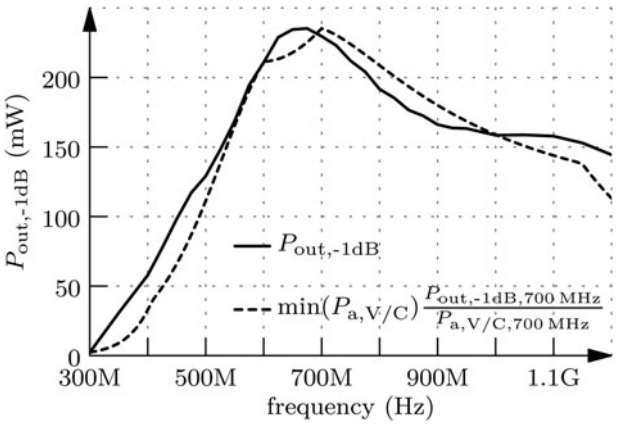

Fig. 7. Measured and calculated output power at the 1 dB compression point versus frequency.

are shown for the driver and the power stage using a replica-biasing scheme to set the current in the driver and output stage. A micrograph of the chip is presented in Fig. 5. The chip size is 1.3 mm × 1.2 mm. The implemented circuit is differential and uses a cascode for the main stage. Since the cascode output node is highly decoupled from the input node, resulting in a very small S_{12} of the stage, the Rollet's factor and therefore stability is improved. The capacitance C_T is formed only by the parasitic capacitances of the transistor field. To achieve the maximum bandwidth, an active driver in combination with a resistive input matching is applied.

Furthermore, a passive network between the driver and the main stage has been introduced. Since the exponential characteristic of the bipolar transistors leads to an expansion of their collector currents, the average collector current with excitation is higher than the operating point current. For a well-defined limitation of this effect, while the collector current expands the gain has to remain constant. The task of the network consisting of R_4 and R_5 is to limit the expansion of the average collector current of the main stage, since the base current flowing through the resistors tends to expand in the same way and works against the effect. Therefore the gain is more flat and the linearity is increased.

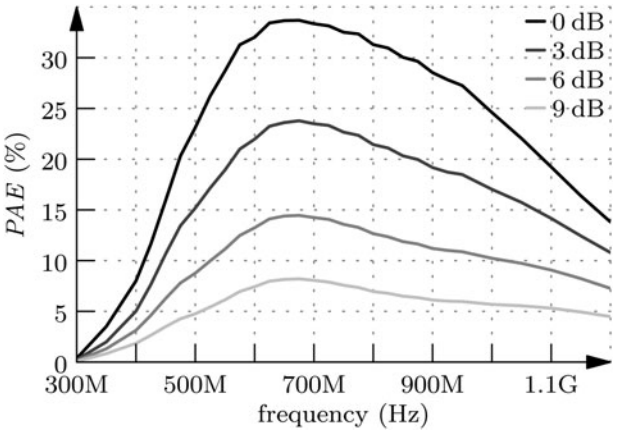

Fig. 8. Measured power added efficiency versus frequency for 0–9 dB back-off.

B) Measurement results

The circuit was measured on-wafer. Compression measurements were performed by a Rhode & Schwarz network analyzer ZVA 67. The transducer gain G_T is shown in Fig. 6. For comparison the transducer gain is plotted in linear scale and $P_{a,C}$ is scaled to the value of G_T at the frequency f_2. Thus, it can be seen that its shape fits well to $P_{a,C}$ in Fig. 3. Deviations for higher frequencies can be explained by impacts from the driver circuit. The compression point measurements were performed in steps of 50 MHz. The output power at the 1 dB compression point is depicted in Fig. 7. Again, a linear scale is chosen to be able to compare the trace with Fig. 3. Although its shape differs slightly from the prediction, it can be seen that a linear model can be used to estimate the linear uncompressed output power. The measured 3 dB large-signal bandwidth is more than 700 MHz around the center frequency of 700 MHz leading to a relative bandwidth of more than 100 %. Finally, the power added efficiency PAE at the 1 dB compression point as a function of the frequency is shown in Fig. 8. Also thereby, the large bandwidth is proven. In addition, the values are also given for 3, 6, and 9 dB back-off. Table 1 compares the designed power amplifier with dual-band impedance transformation network to other state-of-the-art wideband power amplifiers.

Table 1. State-of-the-art wideband power amplifiers.

Ref.	Tech.	f_c (MHz)	Rel. BW (%)	G_T (dB)	P_a (dBm)	$\eta_{-1\,dB}$ (%)	Imped. transf. ratio	Fully integrated	Size (mm)^2	Remark
[9]	n.a. (Si)	915	22*	24	24	44	1.8*	No	n.a.	Commercially available conventional power amplifier
[10]	90 nm CMOS	930	48†	28	27.7	19*	4	Yes	3.3	Integrated distributed transformer with four-way power combiner
[1]	90 nm CMOS	5800	n.a.	n.a.	20.5	16	4	Yes	0.81	Integrated conventional transformer with four -way power combiner
[11]	SiGe BiCMOS	3500	n.a.	13.0	24.6	33*	4	Yes	1.65	Integrated auto-transformer
[12]	SiGe BiCMOS	2000	40	23.8	26.2	34	1	Yes	1.0	Stacked power amplifier
This work	SiGe BiCMOS	700	100	22.1	23.6	33	3.8	Yes	1.6	Dual-band impedance transformation network

*Estimated.
†Determined as saturated output power instead of output power at 1 dB compression point.

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The presented chip reaches the highest relative bandwidth in comparison.

IV. CONCLUSION

It was shown that the common impedance transformation networks for PAs have the ability to implement the required impedance transformation for two frequencies without additional inductors. This increases the frequency range of operation. The dimensioning of the circuit can be done by numerically solving the nonlinear system of equations. Also, imperfections like losses can be considered leading to a fast design process. Based on this, the maximum uncompressed output power of a PA can be estimated. The theory is validated by implementing and measuring an integrated PA.

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REFERENCES

[1] Haldi, P.; Chowdhury, D.; Reynaert, P.; Liu, G.; Niknejad, A.: A 5.8 GHz 1 V linear power amplifier using a novel on-chip transformer power combiner in standard 90 nm CMOS. IEEE J. Solid-State Circuits, **43** (5) (2008), 1054–1063.

[2] Martins, M.; Fernandes, J.; Silva, M.: Dual-band CMOS low-noise amplifier without switches and with continuously adjustable gain. Electron. Lett., **43** (17) (2007), 920–921.

[3] Silicon Storage Technology. 2.4–2.5 GHz/4.9–5.8 GHz dual-band power amplifier module SST13LP05. *Datasheet*, 2009.

[4] Bischof, W. et al.: SiGe-power amplifiers in flipchip and packaged technology, in IEEE Radio Frequency Integrated Circuits (RFIC) Symp. Digest of Papers, 2001, 35–38.

[5] Uchida, K.; Takayama, Y.; Fujita, T.; Maenaka, K.: Dual-band GaAs FET power amplifier with two-frequency matching circuits, in Asia-Pacific Microwave Conf. Proc. (APMC), vol. 1, 2005, 4.

[6] Ghajar, M.; Boumaiza, S.: Concurrent dual band 2.4/3.5 GHz fully integrated power amplifier in 0.13 μm CMOS technology, in Eur. Microwave Integrated Circuits Conf. (EuMIC), 2009, 375–378.

[7] Cripps, S.C.: RF power amplifiers for wireless communications, 2nd ed., *Artech House*, Norwood, 2006.

[8] Vielhauer, P.: Lineare Netzwerke, 1st ed., *VEB Verlag Technik*, Berlin, 1982.

[9] Maxim Integrated: MAX2232, MAX2233 power amplifier. *Datasheet*, 2000.

[10] Francois, B.; Reynaert, P.: A Fully integrated watt-level linear 900-MHz CMOS RF power amplifier for LTE-applications. IEEE Trans. Microw. Theory Tech., **60** (6) (2012), 1878–1885.

[11] Solomko, V.; Weger, P.: A Fully Integrated 3.3–3.8 GHz power amplifier with autotransformer Balun. IEEE Trans. Microw. Theory Tech., **57** (9) (2009), 2160–2172.

[12] Fritsche, D.; Wolf, R.; Ellinger, F.: Analysis and design of a stacked power amplifier with very high bandwidth. IEEE Trans. Microw. Theory Tech., **60** (10) (2012), 3223–3231.

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