UNIVERSITÀ DEGLI STUDI DI TRENTO

DIPARTIMENTO DI FISICA

PHD THESIS

Silicon Nanocrystal Based Light Emitting Devices

for Silicon Photonics

Supervisor   **Candidate**

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List of Publications

Portions of this thesis have been drawn from the following publications:

1. **J.M. Ramírez, F. Ferrarese Lupi, O. Jambois1, Y. Berencén, D. Navarro-Urrios, A. Anopchenko, <u>A. Marconi</u>, N. Prtljaga, A. Tengattini, L. Pavesi, J.-P. Colonna, J.-M. Fedeli and B. Garrido.** Erbium emission in MOS light emitting devices: from energy transfer to direct impact excitation. *Submitted to Nanotechnology*

2. **D. Di, I. Wurfl, L. Wu, Y. Huang, <u>A. Marconi</u>, A. Tengattini, A. Anopchenko, L. Pavesi, G. Conibeer.** Electroluminescence from Si nanocrystal/c-Si heterojunction light-emitting diodes. *Submitted to Nano Letters.*

3. **F. Sgrignuoli, G. Paternoster, <u>A. Marconi</u>, P. Ingenhoven, A. Anopchenko, G. Pucker, and L. Pavesi.** Modeling of Silicon Nanocrystals Based Down-Shifter for Enhanced Silicon Solar Cell Performance. *Submitted to J. Appl. Phys.*

4. **O. Jambois, J.M. Ramírez, Y. Berencén, D. Navarro-Urrios, A. Anopchenko, <u>A. Marconi</u>, N. Prtljaga, A. Tengattini, P. Pellegrino, N. Daldosso, L. Pavesi, J.-P. Colonna, J.-M. Fedeli, and B. Garrido.** Effect of the Annealing Treatments on the Electroluminescence Efficiency of SiO_2 Layers Doped with Si and Er. *Submitted to Journal of Physics D: Applied Physics.*

5. **A. Anopchenko, <u>A. Marconi</u>, M. Wang, G. Pucker, P. Bellutti, and L. Pavesi.** Graded-Size Si Quantum Dot Ensembles for Efficient Light-Emitting Diodes. *Accepted Appl. Phys. Lett.* 2011, Vol. 99, p. 181108.

6. **<u>A. Marconi</u>, A. Tengattini, A. Anopchenko, G. Pucker, and L. Pavesi.** Power Efficiency of Silicon Nanocrystal Based LED in Pulsed Regime. *Proceedings of the 7th IEEE International Conference on Group IV Photonics.* 2011.

7. **A. Tengattini, <u>A. Marconi</u>, A. Anopchenko, N. Prtljaga, L. Pavesi, J.M. Ramírez, O. Jambois, Y. Berencén, D. Navarro-Urrios, B. Garrido, F. Milesi, J.-P. Colonna, and**

J.-M. Fedeli. 1.54 μm Er doped Light Emitting Devices: Role of Silicon Content. *Proceedings of the 7th IEEE International Conference on Group IV Photonics.* 2011.

8. <u>**A. Marconi, A. Anopchenko, G. Pucker, and L. Pavesi.**</u> Silicon Nanocrystal Light Emitting Device as a Bidirectional Optical Transceiver. *Semicond. Sci. Technol.* 2011, Vol. 26, p. 095019; image selected for the cover of the issue.

9. <u>**A. Marconi,**</u> **A. Anopchenko, G. Pucker and L. Pavesi.** Power Efficiency Estimation of Silicon Nanocrystals Based Light Emitting Devices in Alternate Current Regime. *Appl. Phys. Lett.* 2011, Vol. 98, p. 201103; selected for the May 30, 2011 issue of Virtual Journal of Nanoscale Science and Technology.

10. **Z. Yuan, G. Pucker,** <u>**A. Marconi,**</u> **F. Sgrignuoli, A. Anopchenko, Y. Jestin, L. Ferrario, P. Bellutti and L. Pavesi.** Silicon Nanocrystals as a Photoluminescence Down Shifter for Solar Cells. *Solar Energy Materials and Solar Cells.* 2011, Vol. 95, p. 1224.

11. **N. Prtljaga, D. Navarro-Urrios,** <u>**A. Marconi,**</u> **A. Anopchenko, J.-P. Colonna, F. Milesi, N. Daldosso, O. Jambois, B. Garrido, J.-M. Fedeli, and L. Pavesi.** Erbium Implanted Silicon Rich Oxide Thin Films Suitable for Slot Waveguides Applications. *Optical Materials.* 2011, Vol. 33, p. 1083.

12. <u>**A. Marconi,**</u> **A. Anopchenko, G. Pucker and L. Pavesi.** High efficiency and long-term stability of nanocrystalline silicon based devices. *Proceedings of the 6th IEEE International Conference on Group IV Photonics.* 2010, p. 219.

13. **Z. Yuan, C. Schuster, G. Pucker, A. Anopchenko,** <u>**A. Marconi,**</u> **and L. Pavesi.** Photovoltaic properties of Si nanostructure based solar cells fabricated on quartz. *Proceedings of the 6th IEEE International Conference on Group IV Photonics.* 2010, p. 90.

14. **A. Anopchenko,** <u>**A. Marconi,**</u> **E. Moser, S. Prezioso, M. Wang, G. Pucker, P. Bellutti, and L. Pavesi.** Low-Voltage Onset of Electroluminescence in Nanocrystalline-Si/SiO$_2$ Multilayers. *J. Appl. Phys.* 2009, Vol. 106, p. 033104.

15. **A. Marconi, A. Anopchenko, M. Wang, G. Pucker, P. Bellutti, and L. Pavesi.** High Power Efficiency in Si-nc/SiO$_2$ Multilayer Light Emitting Devices by Bipolar Direct Tunneling. *Appl. Phys. Lett*. 2009, Vol. 94, p. 221110.

16. **M. Wang, A. Anopchenko, A. Marconi, E. Moser, S. Prezioso, L. Pavesi, G. Pucker, P. Bellutti, and L. Vanzetti.** Light Emitting Devices Based on Nanocrystalline-Silicon Multilayer Structure. *Physica. E.* 2009, Vol. 41, p. 912.

17. **A. Anopchenko, A. Marconi, E. Moser, M. Wang, G. Pucker, P. Bellutti, and L. Pavesi.** Bipolar injection in nanocrystalline-Si LEDs with low turn-on voltages and high power efficiency. *Proceedings of the 5th IEEE International Conference on Group IV Photonics.* 2009, p. 229.

18. **A. Marconi, A. Anopchenko, E. Moser, M. Wang, G. Pucker, P. Bellutti, and L. Pavesi.** Electroluminescence from nanocrystalline-Si/SiO$_2$ multilayers with an electron injection barrier. Proceedings of the 4th IEEE International Conference on Group IV Photonics. 2008, p. 46.

19. **A. Shatveryan, A. Anopchenko, S.M. Hossain, A. Marconi, M. Wang, G. Pucker, P. Bellutti, and L. Pavesi.** Photovoltaic effect in ultra-thin a-Si/SiO$_2$ multilayered structures. Proceedings of the 4th IEEE International Conference on Group IV Photonics. 2008, p. 390.

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Table of Contents

1.   Introduction

1.1.   Silicon Technology

The progresses in microelectronics and photonics have revolutionized telecommunications and information science and engineering during the 20th century. It would be difficult to identify any other contemporary technology that has had a more pervasive and beneficial influence on our everyday living. These high technology areas permeate everything, from a space shuttle to a washing machine, and are equally important from the perspective of an air force pilot or a homemaker. A good example is the growth of the Internet, with the number of users continuing to double every few months. Microelectronics and photonics have incredible implications for industry, employment, strategic position of countries and, even, for the future organization of the society. It is natural that everyone wonders which new applications of microelectronics and photonics are most likely to come into life in the near future and what difference these applications might make for the 21st century.

In the 20th century, mainstream electronics evolved from vacuum tubes and discrete copper wires to individual transistors and batch-fabricated, printed wiring boards to its current form, which integrates more than a billion transistors and copper interconnections in a single silicon chip. Until the past decade, designers neglected the electrical performance of wires or metal interconnections. They effectively addressed this problem simply by increasing transistor channel width to provide larger drive currents, and thus enable transistor-level circuit performance. Unfortunately, this simple fix is no longer adequate: interconnect latency and energy dissipation now tend to dominate key metrics of transistor performance. For example, for current state-of-the-art technology, the latency of a 1-mm-long interconnect benchmark is approximately six times longer than that of a corresponding transistor. Moreover, the energy dissipation to send a bit over a1-mm-long interconnection is approximately five times larger than that used in a transistor commutation. This scales rapidly in future silicon technology generations.

Consequently, in the near- and medium-term future, exponential increases in transistors per chip, as Moore's law [1] eloquently projects (Fig. 1.1.1), will necessarily emphasize advances in interconnects technology. These advances will be extremely diverse and will include new interconnect materials and processes, optimal reverse scaling, micro-architectures that shorten interconnects, 3D structures and I/O enhancements, interchip optical interconnects and more powerful computer-aided design tools for chip layout and interconnect routing.
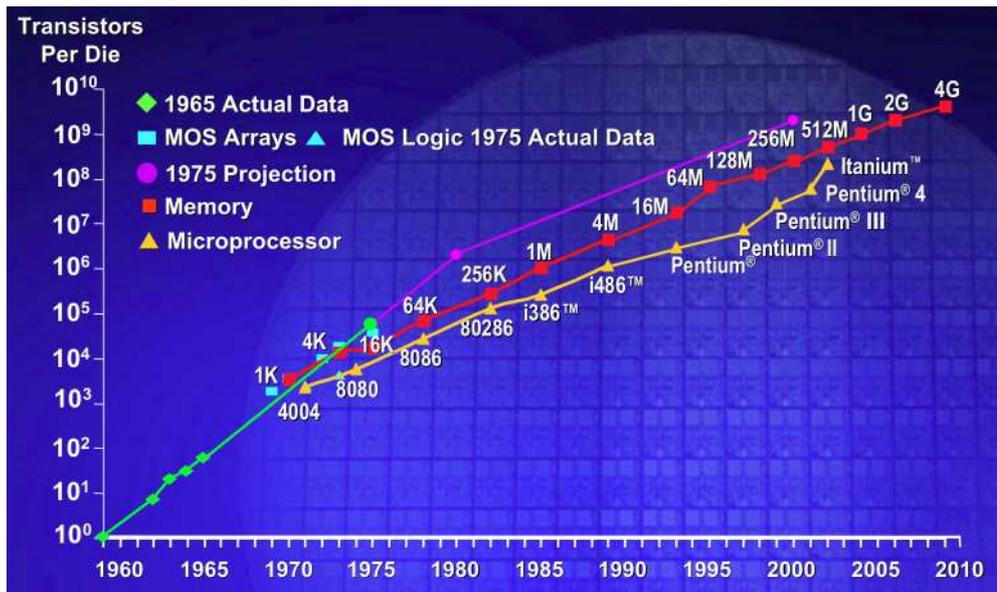
Figure 1.1.1: Number of transistor for integrated circuits showing the historical accuracy of Gordon Moore's prediction of an exponentially increase in the integrated circuit complexity.

1.2. Optical Interconnects

Many expect photonics to provide the long term solution. In optical interconnect schemes, the copper wires between regions of an integrated circuit would be replaced by a system of lasers, modulators, optical waveguides and photo-detectors. [2] The potential benefits of this approach include the virtual elimination of delay, cross talk, and power dissipation in signal propagation, although significant new challenges will be introduced in signal generation and detection. [3] The integration density and data rate that can be achieved by using conventional electrical interconnects set very high performance requirements for any optical interconnect system to be

viable. [4] Stable laser sources, interferometric modulators, dense wavelength division multiplexer (DWDM), and low loss planar waveguides will all be necessary components of an optical interconnect. [5] These photonic technologies are now applied primarily in the long-haul telecommunications industry, where individual component cost and size do not drive the market. Data transfer rates and the cost per transmitted bit through optical fiber networks have improved dramatically in performance over the last few decades, [6] following exponential progress curves that are even faster than Moore's Law.

Microphotonics refers to efforts to miniaturize the optical components used in long distance telecommunications networks so that integrated photonic circuits can become a reality. [7] Work in this field spans many subjects, including planar waveguides and photonic crystals, integrated diode detectors, modulators, and lasers. Advances in the related and often overlapping field of nanophotonics suggest the possibility of eventually controlling optical properties through nanoscale engineering. [8]

The success of photonic interconnect critically depends on high-speed energy-efficient transmitters and receivers. Monolithically integrated 4×10 Gb/s WDM silicon photonic transceivers [9] were reported. Owing to less advanced CMOS technology and power hungry Mach-Zehnder modulator (MZM), the transmitter and receiver consumed power of 575 mW (not including the laser power) and 120 mW, respectively. Hybrid integrated 4×12.5 Gb/s WDM silicon photonics link has also been demonstrated recently. [10] The MZM used in this demonstration alone consumes a few tens to hundreds of mW.

Tremendous progress has also been made in efficient silicon photonic device development. On the transmitter side, carrier-depletion microdisk [11] and microring [12] modulators have demonstrated an energy efficiency of a few 10s fJ/bit at 10 Gb/s. Optimized racetrack ring modulators with reduced voltage swing can further improve efficiency to about 10 fJ/bit. [13] On the receiver side, very low parasitic Ge photodetectors have reported high responsivity and bandwidth. [14]

1.3. Silicon Photonics

The goal of silicon photonics is to create high performance optical devices from with CMOS compatible materials so that photonic components can be made using the mature silicon fabrication technology. CMOS stands for Complementary Metal Oxide Semiconductor, and refers to logic circuit designs that pair p-channel transistors with n-channel transistors to limit the quiescent currents that waste power when a circuit is not otherwise active. CMOS circuits have incredible power efficiency advantages and are the building blocks for all microprocessors. It is important to ensure that all materials used in a CMOS facility do not contaminate these fundamental components of the circuit. CMOS compatibility contains an additional connotation of cost effective economic scaling. In silicon photonics, most of the problems encountered are related to materials issues, in either integration or stability in fabrication or operation.

Silicon itself is a CMOS compatible material that can be considered for photonics. Many of the properties that make silicon a good choice for electronic chips are helpful in optical applications as well. It is an abundant material, with good thermal conductivity and good mechanical strength. It also has a high index of refraction and a small intrinsic absorption at infrared photon wavelengths. However, silicon is a poor material for making lasers, which are the necessary signal sources in optical communication. Silicon also makes a poor material for light emitting devices, because it has an indirect band structure (Fig. 1.3.1). This means that the least energetic conduction band electrons in silicon are in motion relative to the most energetic valence band electron states. In order for silicon to absorb or emit a photon at visible frequencies, an electron must undergo a band-to-band transition between two of these states. This transition requires the simultaneous absorption or emission of a phonon in order to accommodate the momentum mismatch, making it much less likely to occur. Because a radiative transition is unlikely, competing nonradiative recombination channels tend to dominate the relaxation of the excited state electrons. Ultimately this makes photon emission in silicon extremely inefficient: the quantum efficiency is on the order of 10^{-7} - 10^{-4}.
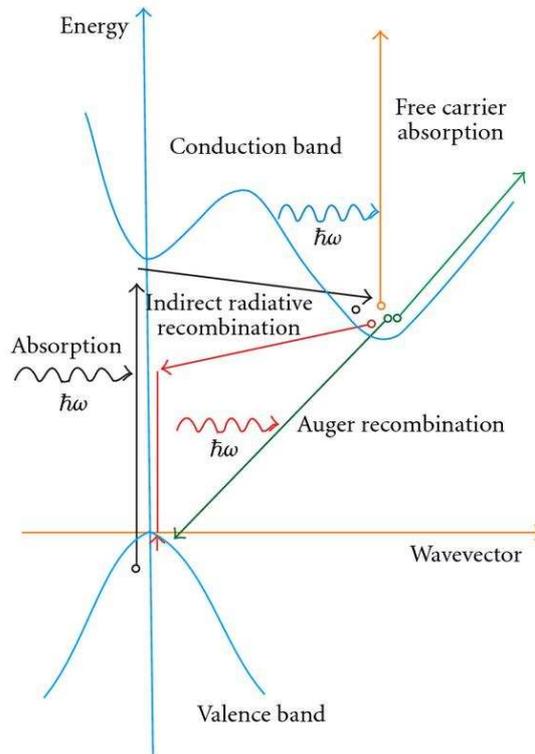
Figure 1.3.1: In the band structure of silicon, the lowest-energy states in the conduction band are offset in momentum space from the highest-energy valence band states at the center of the Brillouin zone.

The recently reported first silicon laser [15] did not rely on the emission of photons by excited conduction band electrons. This laser instead operated by Raman scattering in which sub-band gap photons interact only with phonons. The crystallinity of silicon makes Raman scattering relatively strong in relation to amorphous glasses, but intense optical pumping is still required to create a population inversion of the excited virtual phonon state. While these results are impressive, it is clear that Raman lasers do not have a practical future because they require optical excitation by a pump laser and have a relatively small spectral range in which gain can be achieved.

Materials that have superior optical properties, such as alloys of Group III and V elements, are used to make the lasers for long-haul telecommunication networks. These materials are not CMOS compatible, primarily because of mismatched crystal lattice constants with respect to silicon. However, the list of materials that are CMOS compatible is always expanding as new methods of integration are introduced. This strategy is currently being pursued by start-up

photonics companies such as Luxtera, as well as Intel's silicon photonics research group. Both companies have recently demonstrated electrically pumped lasers on silicon substrates that use integrated III-V materials to achieve gain. [16] [17]

An alternative is to exploit quantum mechanical effects to improve the optical properties of silicon or other currently CMOS compatible materials. Following this approach, nanostructured silicon has been identified for many years as a promising candidate material for silicon photonics.

1.4.   Silicon Nanocrystals

The optical emission in silicon nanocrystals [18] was shown over fifteen years ago with the first report of photoluminescence from porous silicon. Similar optical observations have since been made in nanostructured silicon materials fabricated by ion implantation, aerosol synthesis, sputtering, laser ablation, chemical vapor deposition, and reactive evaporation of Si-rich oxides.

The quantum mechanical effects are responsible for the enhanced photonic materials properties. Quantum mechanics describes the behavior of all physical systems, but conflicts with the predictions of classical physics only for systems that we can study at the length scale of the de Broglie wavelength. For electrons this corresponds to sizes on the order of nanometers, a regime that we can access experimentally and engineer to create useful devices that take advantage of quantum mechanical phenomena. Qualitatively the effect of confinement in a quantum mechanical system can be understood by considering the simple particle in a box problem. In order to satisfy boundary conditions, the characteristic ground state energy scales inversely with the square of the width of the confining potential well. Confinement raises the energy of the ground state, tends to create a discrete density of states at low energies, and introduces uncertainty into the momentum of the particle. It is possible to improve the approximation of a quantum dot by considering the particles of interest, excitons, in a three-dimensional spherical confinement potential representing the insulating matrix around the semiconductor nanocrystal. Excitons are electron-hole bound composite that are coupled together by Coulomb attraction. The mathematics

16

used to describe an exciton is identical to the model for the hydrogen atom. It is possible therefore predict from first principles a Bohr radius for the ground state of the exciton corresponding to the critical length scale for confinement effects. The Bohr radius of an exciton can be thought of as the typical separation distance. In silicon, the exciton Bohr radius is about 5 nm. This tells us that we can expect to observe quantum confinement effects in silicon nanocrystals that are smaller than approximately 5 nm in diameter.
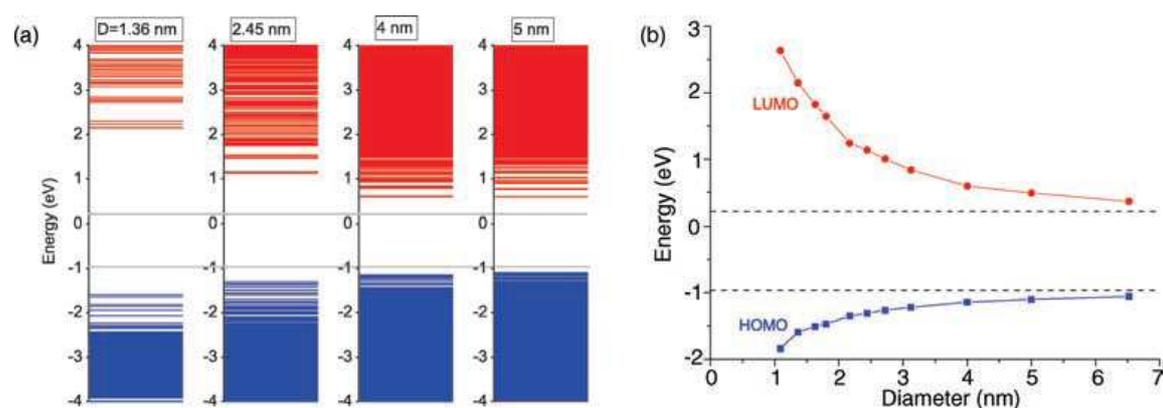

Figure 1.4.1: (a) The evolution of states for four increasing diameters of Si NCs and (b) HOMO and LUMO variation with respect to diameter. The bulk band edges of Si are marked with a dashed line for comparison.

Figure 1.4.1 shows the scale of the change in effective band gap for a nanocrystal and Figure 1.4.2 shows the size-dependent silicon nanocrystal band gap. Poor agreement between theory and experiments is found for small silicon nanocrystals and is commonly attributed to silicon oxygen double bond defect states at the surface of the nanocrystal that can capture and localize the exciton. It is worth noting that native surface oxides on silicon are typically of about 2 nm thick. Therefore a silicon nanocrystal is essentially "all surface" and might be expected to be very sensitive to surface chemistry.
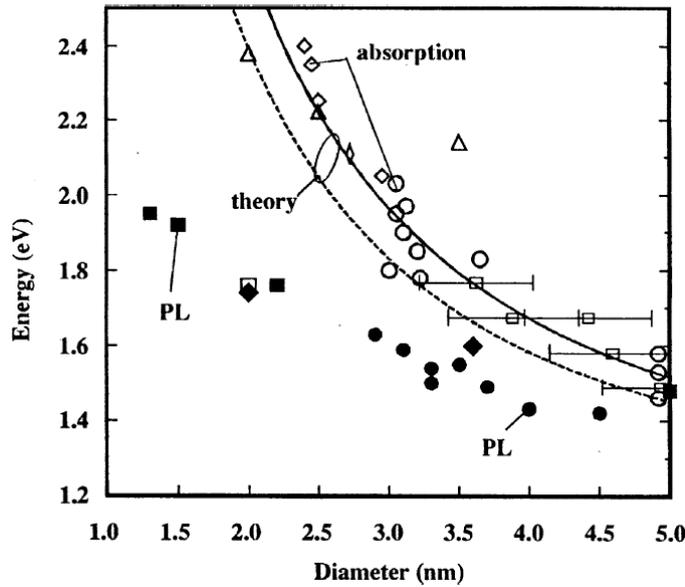
Figure 1.4.2: Theoretical and experimental values for band-gap in Si nanocrystals (after Delerue et al. [19]) Dashed and solid line represents theoretical values with and without excitonic correction.

In addition to causing the blue shift of the silicon band edge emission into the near infrared or red spectral range, quantum confinement in silicon nanocrystals results in orders of magnitude brighter emission than is observed from bulk silicon. The brighter emission must be explained by some combination of enhancement in the absorption cross section and radiative recombination rate and decrease in the rate of nonradiative recombination. Experiments suggest that the absorption cross section in silicon nanocrystals shows little or no enhancement over bulk silicon on a per-atom basis. Of the remaining two factors, most of the improvement in radiative recombination efficiency comes from a dramatic decrease in the nonradiative recombination rate. Nonradiative exciton recombination in bulk silicon is typically dominated by Shockley-Hall-Read recombination at mid gap defect states corresponding to defects and impurities in the crystal. In nanocrystals that are small enough to show quantum confinement effects, such defects are thermodynamically unfavorable and tend to grow out of the quantum dot. There are two factors that contribute to improvement in the radiative recombination rate in silicon nanocrystals. The first can be understood in the context of Fermi's Golden Rule for quantum mechanical transitions, which can be derived using time dependent perturbation theory. In the formalism of Fermi's Golden Rule, the rate of an optical dipole transition is proportional to the magnitude of an off-

18

diagonal matrix element calculated by evaluating an overlap integral that connects the electron and hole wavefunctions together through the dipole operator. Because the nanocrystal forms a potential well that confines the electron and the hole spatially, these wavefunctions overlap more in position space and the matrix element for the transition increases. [20] At the same time, the uncertainty in momentum space that confinement introduces relaxes the momentum conservation rule and allows a greater proportion of the phonon density of states to assist in the indirect band-to-band transition. [21] On the other hand two other recombination mechanisms that contribute to the inefficiency of light emission in bulk silicon, recombination at surface defects and Auger recombination, in which the energy of the exciton is transferred to a third charge carrier can be worse in silicon nanocrystals than in bulk silicon. The enhanced sensitivity to surface recombination can be understood by noting the high surface-to-volume ratio, while the rapid Auger recombination rate in charged nanocrystals results from the large effective carrier concentration that a single carrier represents in the small nanocrystal volume.

1.5. Silicon Nanocrystal Based Light Emitting Devices

Despite the advantages that nanostructured silicon offers in comparison to bulk silicon, it is still a relatively poor optical material in comparison to direct gap III-V semiconductors. The radiative rate, which ultimately limits the optical power that can be radiated by a volume of material, is perhaps one or two orders of magnitude faster than bulk silicon at 10 kHz. However it is four orders of magnitude slower than the 1 GHz emission rates found in materials such as GaAs. While the radiative recombination efficiency is high, the insulating matrix that surrounds and defines the quantum dot complicates the electrical injection of carriers. The emission wavelengths are always blue shifted by confinement with respect to the bulk silicon band gap at 1.1 μm and can therefore be absorbed by bulk silicon. The emission is also far from the 1.3 μm and 1.5 μm telecommunications spectral windows, in which silica fibers have a transmission maximum, making silicon nanocrystals less attractive for data transfer applications, including optical interconnects.

In display applications, the blue shifted emission of silicon quantum dots is an advantage. Red and orange emission is fairly easy to attain in nanocrystals embedded in silicon oxide. Concerns about the achievable brightness in a silicon nanocrystal based display remain because luminosity in the saturation regime is proportional to radiative rate, and the radiative rate of silicon nanocrystals is relatively low (1-100 kHz).

Traditional light emitting diodes (LEDs) work by injecting minority charge carriers into complementarily doped regions across the depletion width of a semiconductor pn-junction in forward bias. The minority carriers form excitons with majority carriers and can recombine to emit light. This process requires a current to flow through the device which consumes energy in Joule heating in proportion to the resistance of the diode. Because silicon nanocrystals must be embedded in an insulating matrix a LED made out of nanocrystal doped material would have a low conductivity and resistive heating would limit the electroluminescence power efficiency. Inadvertently doping the silicon nanocrystals could also be problematic. A single donor or acceptor in a nanocrystal creates a degenerate free carrier concentration that turns on strong nonradiative Auger quenching of any injected excitons. Instead, electrically pumped light emitting devices have been made with intrinsic silicon nanocrystals. These designs typically rely on impact ionization to create excitons. The process is the inverse of Auger recombination: an injected carrier with excess thermal energy relaxes to the band minimum by promoting an electron from the valence band into the conduction band of the quantum dot. Impact ionization requires relatively large voltages in order to create the electric fields that induce carriers to tunnel through the insulating barrier to the nanocrystal. Excitation is more efficient with highly energetic hot carriers, but this process can damage the quality of the insulating matrix over time and reduces device longevity. Some reports claim that impact ionization can be achieved without introducing hot carriers.

While silicon nanocrystals alone cannot emit light in the infrared telecom bands, they can be coupled to the emission of erbium ions to create a promising hybrid optical material. [22] When incorporated in silicon oxide, Er^{3+} ions exhibit a weakly allowed atomic transmission at 1.5 μm

that is well aligned with the transmission maxima in optical fiber. For this reason erbium doped fiber amplifiers are commonly used in long distance telecommunications to restore the intensity of optical signals. Because the transition is an atomic dipole, the cross section for the optical excitation of an erbium ion is very small (10^{-21} cm^2) and further requires that the exciting wavelength be resonant with another atomic transition of the ion. In contrast, the excitation cross section for silicon nanocrystals is nearly five orders of magnitude larger and nanocrystals can be excited by photons of any energy above the confined band gap. Because the radiative rate of silicon nanocrystals is fairly low, nonradiative near field energy transfer to erbium ions placed in close proximity to the nanocrystal can be the dominant recombination pathway for excitons. In this way, silicon nanocrystals have been shown to be effective sensitizers for erbium ions (Fig. 1.5.1) in optically pumped waveguide amplifiers.
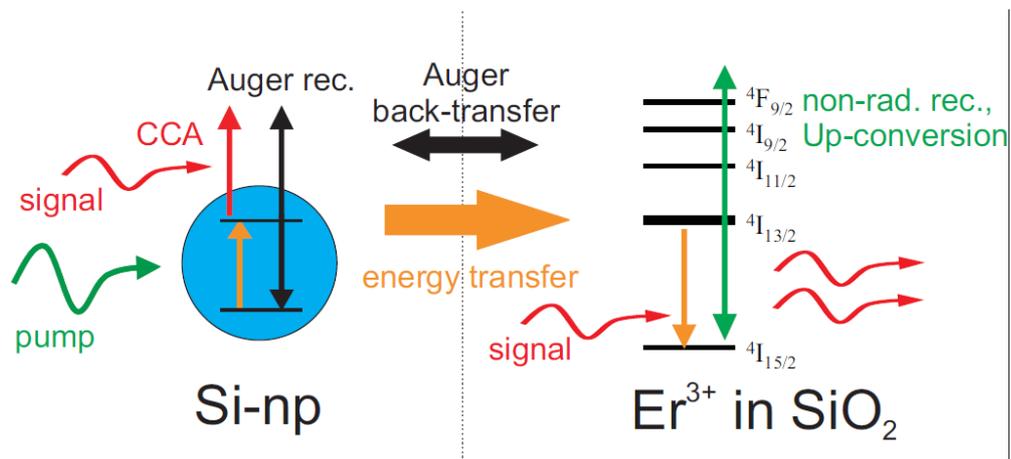

Figure 1.5.1: Schematic of the relevant physical mechanisms in Si-np and Er3+ ions regarding the energy transfer effect.

1.6.   Outline of This Thesis

This thesis presents experimental work developing silicon nanocrystal based light emitting devices for silicon photonics. The chapters are organized as follows:

In chapter 2, fabrication and characterization of silicon nanocrystal based devices are presented. In collaboration with Intel Corporation and Bruno Kessler Foundation and thanks to

the support of European Commission through the project No. ICT-FP7-224312 HELIOS and through the project No. ICT-FP7-248909 LIMA, it is shown that layers and devices containing silicon nanocrystals can be formed in a production silicon-fab on 4 and 8 inch silicon substrates via PECVD and subsequent thermal annealing. Devices produced by single layer and multilayer deposition are studied and compared in terms of structural properties, conduction mechanisms and electroluminescence properties. Power efficiency is evaluated and studied in order to understand the relation between exciton recombination and electrical conduction. A band gap engineering method is proposed in order to better control carrier injection and light emission in order to enhance the electroluminescence power efficiency.

In chapter 3, the power efficiency of silicon nanocrystal light-emitting devices is studied in alternating current regime. An experimental method based on impedance spectroscopy is proposed and an electrical model based on the constant phase element (CPE) is derived. It is, then, given a physical interpretation of the electrical model proposed by considering the disordered composition of the active material. The electrical model is further generalized for many kinds of waveforms applied and it is generalized for the direct current regime. At the end, time-resolved electroluminescence and carrier injection in alternate current regime are presented.

In chapter 4, erbium implanted silicon rich oxide based devices are presented. The investigation of opto-electrical properties of LED in direct current and alternate current regime are studied in order to understand the injection mechanism and estimate the energy transfer between silicon nanocrystals and erbium. At the end a device layout and process flow for an erbium doped silicon nanocrystal based laser structure are shown.

In chapter 5, some other applications of silicon nanocrystal are presented. An example of all-silicon solar cell is shown. The photovoltaic properties and carrier transport of silicon nanocrystal based solar are studied. At the end, the combination of emitting and absorbing properties of silicon nanocrystal based LED are used to develop an all-silicon based optical transceiver.

22

2. Light Emitting Devices Under Direct Current Excitation

2.1. Introduction

In this chapter, fabrication and characterization of silicon nanocrystal based devices will be presented. In collaboration with Intel Corporation and Bruno Kessler Foundation and thanks to the support of the European Commission through the project No. ICT-FP7-224312 HELIOS and through the project No. ICT-FP7-248909 LIMA, it is shown that layers and devices containing silicon nanocrystals can be formed in a production silicon-fab on 4 and 8 inch silicon substrates via PECVD and subsequent thermal annealing. Devices produced by single layer and multilayer depositions are studied and compared in terms of structural properties, conduction mechanisms and electroluminescence properties. Power efficiency is evaluated and studied in order to understand the relation between exciton recombination and electrical conduction. The band gap engineering of the tunneling rates is proposed in order to control carrier injection and light emission in order to enhance the electroluminescence power efficiency.

2.2. Single Layer and Multilayer Based Light Emitting Devices

2.2.1. Electrical Conduction and Electroluminescence in Single Layer LEDs

The problem of charge injection in the nc-Si LED arises as a result of embedding nanocrystals into the silicon oxide dielectric matrix. To obtain an efficient light emitter, balanced bipolar charge injection into the nanocrystals has to be realized. Good nanocrystal passivation and isolation have to be optimized with charge injected into the nanocrystals under low voltages. In principle, this could be possible when the thickness of the silicon oxide between the nanocrystals is reduced at a value that direct tunneling currents become important. Direct tunneling is a

conduction mechanism that leads to large injected electrical currents at low applied voltages without leading to the oxide degradation. Typical silicon nanocrystal LEDs work under high voltages (above 5 V) at which unipolar Fowler-Nordheim tunneling is the main charge injection mechanism. [23] [24] The Fowler-Nordheim tunneling induces a positive charge in the silicon oxide and leads to its degradation. [25] There is some discussion in the literature about electroluminescence (EL) quenching due to charge trapping in nc-Si LED. [26] On the other hand, in stoichiometric oxide based MOS devices and depending on the oxide thickness direct or trap-assisted tunneling (TAT) can dominate. [27] The direct tunneling current is larger than the trap-assisted one for an oxide thickness thinner than 2.6 nm, where the main contribution to the direct tunneling current is from electrons that belong to the conduction band. [27]

Devices Fabrication

Different MOS-like capacitors were realized using either silicon rich oxides (SRO) or silicon-rich oxynitrides (SRON) deposited by PECVD as gate dielectric material. First, the active layer of the LED was deposited by PECVD on 4 inch Si substrates. The substrates were p-type doped (100) Si with a resistivity of 12-18 Ω cm. During PECVD deposition[1], the ratio among the precursor gasses (SiH$_4$, N$_2$O, and NH$_3$) was varied to control the excess amount of both Si and N in the SiO matrix. The different deposited layers are identified by a symbol Γ, which is defined as the ratio between the N$_2$O and the SiH$_4$ fluxes used during the deposition process. Γ is inversely proportional to the Si content inside the oxide matrix. In addition, in order to evaluate the role of the N content, 40 SCCM (SCCM denotes cubic centimeter per minute at STP) of NH$_3$ were added in the deposition chamber during the deposition of a few SRON layers. In this case, the devices are labeled with an index "N" following the Γ value. The thickness of the SRO layers was around 50 nm for all devices (see Table 2.2.1.1 for details).

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[1] LED fabricated at FBK [111]

24

Device	SRO thickness (nm)	Refractive index at 600 nm	Si content[a] (at. %)	O content[a] (at. %)	N content[a] (at. %)	SRO Capacitance (pF)	SRO dielectric constant
Γ3	42 ± 4	2.49 ± 0.01	52	44	4	56 ± 1	8.5 ± 1.0
Γ3N	32 ± 4	2.58 ± 0.01	54	38	8	88 ± 2	10.1 ± 1.5
Γ10	50 ± 2	1.82 ± 0.01	48	47	5	34 ± 1	6.1 ± 0.4
Γ10N	47 ± 2	1.81 ± 0.01	48	44	8	36 ± 1	6.1 ± 0.4
Γ15	49 ± 2	1.69 ± 0.01	44	50	6	31 ± 1	5.5 ± 0.4

[a]Atomic percentages of oxygen, nitrogen, and silicon were calculated from XPS measurements using atomic sensitivity factors.

Table 2.2.1.1: Device structural, optical, and electrical characteristics.

After deposition, wet oxidation was performed at 1050 °C for 1 h to grow both 480 nm thick field oxide (for active area isolation) and Si nanocrystals in the gate dielectric. Then, the devices were processed by using a standard MOS process. The gate was formed with a semitransparent 30 nm thick layer of n-type in situ doped polysilicon. Different geometries were used for the metallization: circular geometry with a ring-shaped metal line for emission study (LED) and disk geometry entirely covered by the metal contact for electrical studies (capacitor). Metallization was done with a 500 nm thick layer of Al (1% Si), which is used to connect the gate area of 7.94×10^{-4} cm^2 in the LED (capacitor for electrical characterization had a gate area of 3.14×10^{-4} cm^2) with the bonding pad. In the LED geometry, the poly-Si is covered by an antireflective coating formed by a 50 nm thick Si_3N_4 layer and a 120 nm thick SiO_2 layer in order to improve light extraction. Figure 2.2.1.1 reports the schematic cross section and top view of the devices.

A series of monitor wafers were prepared, which followed the process flow of the devices except for the definition of the device areas and contacts by photolithography and metallization. These monitor wafers were used for evaluation of layer thickness and structural analysis.
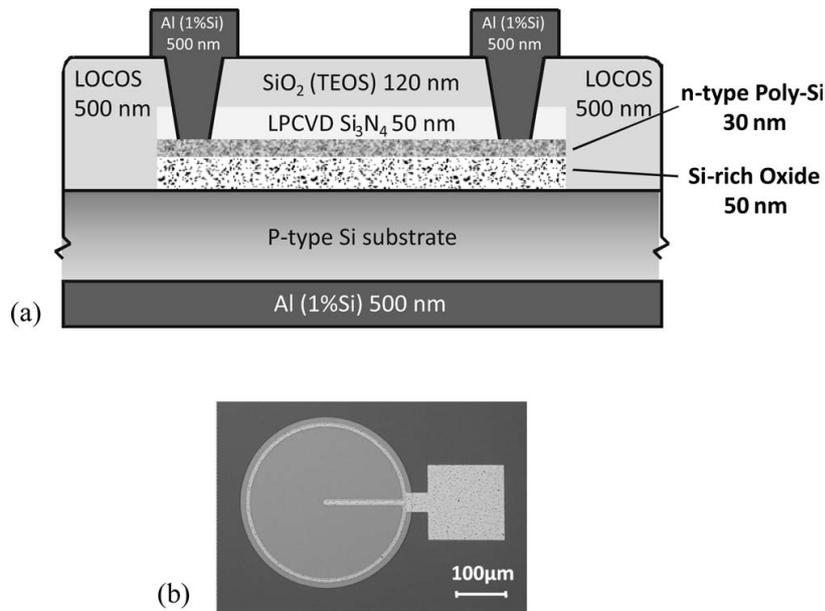
Figure 2.2.1.1: The schematic cross section (a) and the top view of the devices (b).

SRO and SRON characterization techniques

Layer thickness after annealing was controlled by variable angle spectroscopic ellipsometry and depth profiling of sputter craters from secondary ion mass spectrometry (SIMS) on the monitor wafers[2]. The SIMS measurement has been employed to obtain direct information about the thickness and the amount of excess silicon in the SRO layer. X-ray photoelectron spectroscopy (XPS) measurements were performed using a Scienta Esca-200 system equipped with a monochromatic Al Kα (1486.6 eV) source. An overall energy resolution of 0.4 eV was routinely used. Si 2p, O 1s, N 1s, and C 1s core levels were collected. All core level peak energies were referenced to the saturated hydrocarbon in C 1*s* at 285.0 eV. Photoluminescence (PL) measurements with a 488 nm Ar$^+$ laser have been performed to confirm the formation of nanocrystals in the SRO layer after the annealing.

The current-voltage (I-V) characteristics were obtained using the Agilent 4156C precision semiconductor parameter analyzer. The capacitance-voltage (C-V) measurements were done with HP 4284A precision LCR meter. A 2-m-long extension cable was used. The open and short circuit corrections were performed according to the operation manual. The alternating current

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[2] Ellipsometry and SIMS measurement performed at FBK [112]

(AC) signal voltage level was 50 mV. The C-V data were collected at two frequencies, 1 and 100 kHz. The delay time in the I-V and C-V measurements was 1 s to balance measurement speed and measurement integrity. The scanning voltage step was 100 mV. The impedance spectroscopy was utilized in the case of high-silicon excess and hence high-conductive $\Gamma3$ and $\Gamma3N$ devices, to obtain an equivalent electric circuit of the device and estimate the circuit capacitance. Impedance magnitude and phase were measured in the frequency range of 1-300 kHz. The bias swept from -4 to 4 V.

The EL was collected with a Spectra-Pro 2300i monochromator coupled with a nitrogen cooled charge coupled device (CCD) camera. The monochromator was set to the zero order configurations to measure the emission integrated over the whole visible range. The total light intensity was then calculated by integrating the CCD camera signal over the illuminated pixels. The measurements were performed at room temperature in a dark room. A control MOS device with the stoichiometric SiO_2 gate dielectric was prepared using PECVD technique and its I-V and C-V characteristics was measured. C-V modeling shows a good agreement with the experimental data. The good agreement indicates that the control SiO_2 device has good MOS-structure properties, namely, oxide layer is a good insulator, the oxide is free from charge, and planar interface Si/SiO_2 is free from electronic trap levels and space charge.

Nanocrystals formation: XPS and PL analyses

The PL spectra of the various deposited layers are shown in Fig. 2.2.1.2. The PL spectra reflect the formation of nc-Si in the SiO_2 matrix. It can be seen that when the Γ value is decreased (i.e., increasing the excess silicon content) the PL peak wavelength red shifts, indicating the formation of large nanocrystals. For the highest Γ value ($\Gamma15$) the PL peak has been found at around 720 nm, while for the lowest Γ value ($\Gamma3$) the spectrum peaks at wavelengths longer than 900 nm. From the PL peak wavelength for high Γ values ($\Gamma10$, $\Gamma10N$, and $\Gamma15$) the band gap can be estimated to fall in the range of 1.6-1.7 eV. On the other hand, for low Γ values the band gap of the nanocrystals is very close to that of bulk Si. It is noteworthy that PL peak intensity

decreases in the following order: Γ10, Γ10N, and Γ15 in correspondence with the decrease in the Si excess estimated from the XPS analysis. Later it will show that the PL decrease contradicts the increase in charge storage capacity of the devices.
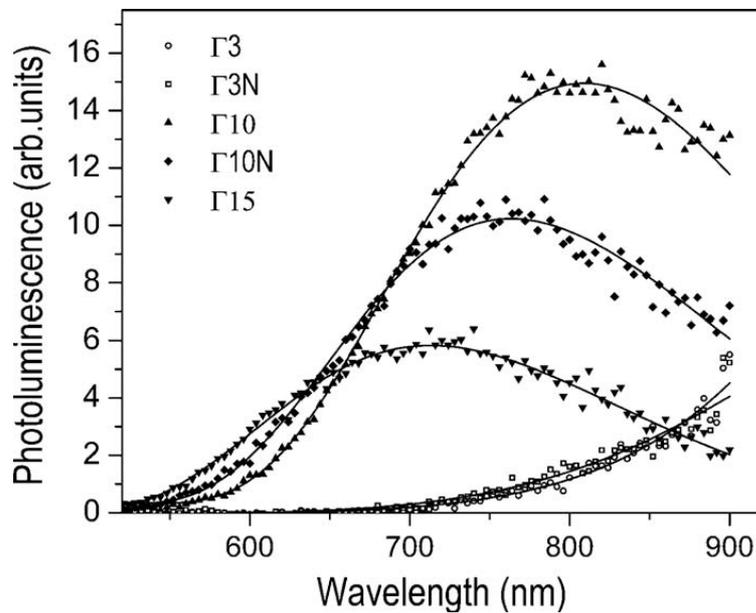

Figure 2.2.1.2: PL spectra collected from the monitor wafers with Ar laser at 488 nm. Incident power was 50 mW. The spectra are normalized for spectrograph response. The devices are indicated in the figure legend.

Conduction mechanism and equivalent electric circuit of the LED

The logarithms of the absolute value of current density through the device layer for the various LED are shown in the Fig. 2.2.1.3 as a function of the applied gate voltage. The current-voltage (I-V) characteristics were collected scanning the gate voltage from positive to negative values and then in the opposite direction, from negative to positive voltages. The positive gate voltages correspond to a reverse bias. This is the gate polarity at which the depletion (inversion) layer is formed in the p-type silicon substrate. By analogy, the negative voltages correspond to a forward bias: the MOS device is in accumulation. The device conductivity increases to a large extent when the silicon content increases.
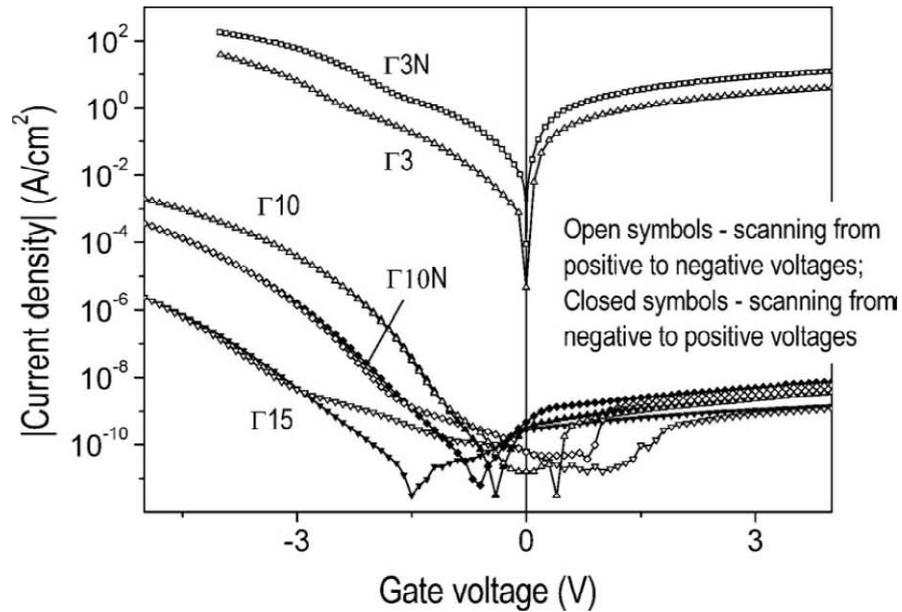
Figure 2.2.1.3: Absolute value of MOS-LED gate current density as a function of applied gate voltage, I-V characteristics. Open symbols: scanning the MOSLED from inversion to accumulation. Closed symbols: scanning from accumulation to inversion. Devices are marked.

The high-Γ devices (Γ10, Γ10N, and Γ15) have been found to be less conductive as well as highly rectifying. The reverse currents in these devices were of the order of a few picoamperes whereas the forward currents were around few microamperes (at 5-10 V of biasing voltage). The I-V characteristics of the high-Γ devices resemble that of a p-n junction diode, demonstrating an exponential dependence at low forward voltages and the effect of a series resistance at high forward voltages. The poor quality of the diode is reflected in an ideality factor (which gives the slope of forward-biased I-V in the straight region) that deviates significantly from unity, being smaller for the low-Γ devices (Γ10). The excess of nitrogen in the SRO layer decreases the conductivity. I-V hysteresis is observed for high-Γ devices (low silicon content). The hysteresis width is larger for the devices with lower conductivity although no hysteresis was observed for the low-Γ devices with high conductivity (Γ3 and Γ3N). The hysteresis originates from the charge accumulated within the SRO layer. Positive charge is accumulated under the negative (forward) bias. Negative charge is accumulated under the positive (reverse) bias. As it will be shown later this accumulated charge is trapped near the nanocrystal interfaces in the oxide layer. The low-Γ devices (Γ3 and Γ3N) are more conductive, and are poor rectifiers. The large reverse-bias current

is due to the presence of electron traps (electron generation centers) in the nc-Si layer. The reverse current increases linearly with increasing bias. It is noteworthy than the I-V characteristics for Γ3 and Γ3N devices under forward bias show a kink at the gate voltage around -2.4 and -1.6 V, respectively. This kink is associated with the energy barrier height at the interface between the silicon substrate and the active SRO layer.

To clarify the electric transport mechanism in these devices, some I-V experiments at several elevated temperatures were undertook. The I-V characteristics of Γ3 device are shown in the Fig. 2.2.1.4. When temperature increases the device conductivity increases, demonstrating a larger increase at low gate voltages.
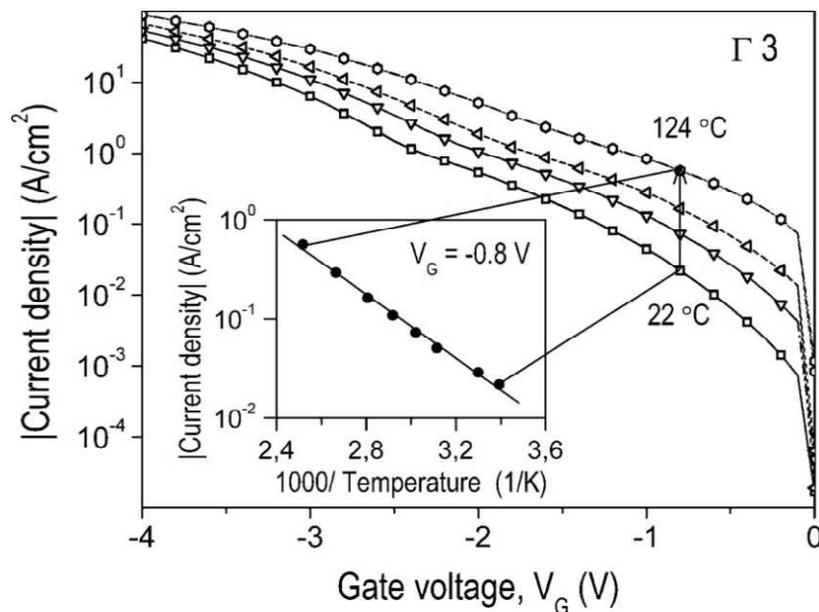

Figure 2.2.1.4: Forward-bias I-V characteristics of Γ3 device (shown in Fig. 2.2.1.3) at several elevated temperatures between 22 and 124 °C. Inset: Arrhenius plot of current density at the gate voltage value of -0.8 V.

This temperature increase is not consistent with any known tunneling mechanisms. It should be noticed that the change in the forward-bias voltage for a 10 °C temperature change is much larger than the typical -17.3 mV value for the ideal p-n junction diode. The increase obeys the Arrhenius law (see the inset), which is characteristic for a charge emission process. At voltages higher than the voltage value of the I-V kink, the temperature dependence is moderate,

30

which points to a change in the conduction mechanism above and below the kink. The electric field assisted thermal emission, also called Poole-Frenkel emission, is the most probable conduction mechanism at low electric fields. Poole-Frenkel emission is not a tunneling mechanism, and, in general, dominates at room temperature and moderate electric fields, and is governed by the following equation: [28]

$$I_{PF} \propto V \, exp \left[-\frac{q}{rkT} \left(\varphi_t - \sqrt{\frac{qV}{d\pi\varepsilon}} \right) \right]$$

Equation 2.2.1.1: Poole-Frenkel emission.

q is the unit charge, d is the oxide thickness, ε is the oxide permittivity, k is the Boltzmann's constant, T is the absolute temperature, φ_t is the trap energy level, V is the gate voltage, and r is a parameter ranging from 1 to 2 depending on the position of the Fermi level. Electron emission could occur through interface trap states. The interface trap states are probably located at the nc-Si interfaces, as it wills show later. For a trap to experience the Poole-Frenkel effect, it must be neutral when filled and positive when empty. [28] The slope of the plot of log (I/V) versus $\sqrt{V}$, which is also called Poole-Frenkel plot, will yield the dielectric constant of the device under test (the flatband voltage and surface potential are neglected being small). Figure 2.2.1.5 shows the Poole-Frenkel plot of the Γ3 device at 22 °C, where a linear variation can be identified in the intermediated applied field. A linear regression through the data points gives a dielectric constant of 10.2 ± 0.6, which is a good estimate for Γ3 nanocrystal composite and agrees well with the value obtained from C-V measurements, as it wills show in the following.

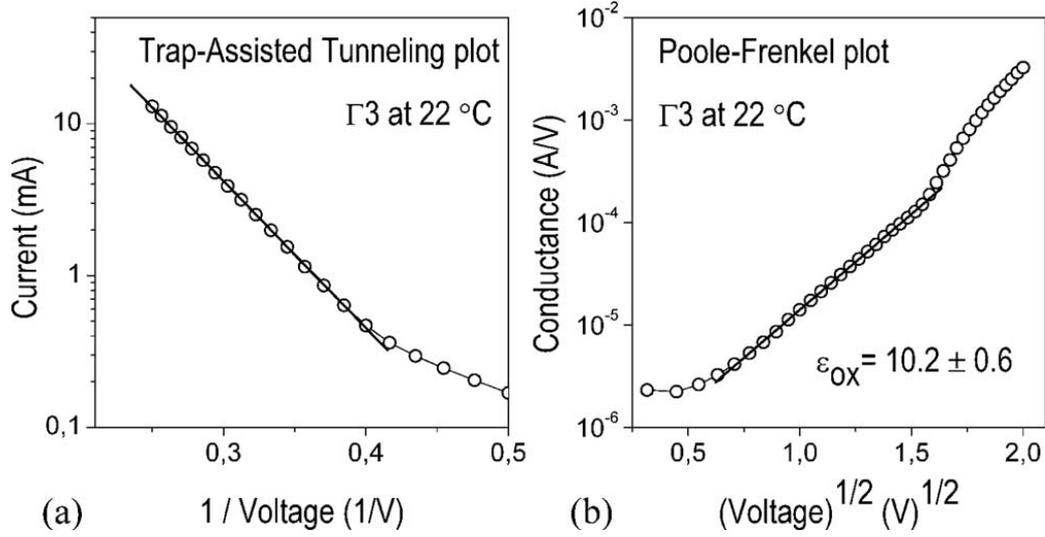**Figure 2.2.1.5: Forward-bias I-V characteristic of Γ3 device at 22 °C (the same as shown in Figs. 2.2.1.3 and 2.2.1.4). Left (a): TAT plot for the high-voltage region (above the kink). Right (b): the Poole-Frenkel plot showing a straight-line region at moderate voltages. The dielectric constant value calculated from the straight-line fit is 10.2 ± 0.6.**

The Fig. 2.2.1.5 shows also the high-voltage part of the same I-V characteristic, which is plotted in the so-called TAT (Trap Assisted Tunneling) plot, which is $\log(I)$ versus $1/V$. The TAT current is governed by the following equation at high electric fields: [29]

$$I_{TAT} = exp\left[-\frac{8\pi d\sqrt{2qm^*}}{3hV}\sqrt{\varphi_t^3}\right]$$

Equation 2.2.1.2: Trap Assisted Tunneling Current.

m^* is the electron effective mass in the SRO layer, and h is Planck's constant. A straight-line dependence is observed indicating a TAT of electrical charges under forward bias above the kink voltage of 2.4 V. This is the tunneling mechanism where electrons from the gate electrode are able to tunnel directly into the nc-Si/SiO$_2$ interface trap states and, then, tunnel into the silicon substrate. To gain more insights into the electrical transport in these devices an equivalent electrical circuit of the LED using impedance spectroscopy experiments is derived. The complex impedance of Γ3 and Γ3N device was measured in a broad frequency range and plotted in the log-impedance plot (Fig. 2.2.1.6) also called Nyquist or Cole–Cole plot. The lines through the data points are nonlinear least-squares fits, which model the equivalent circuit shown in the inset. The

fit parameters for series and parallel resistances of the Γ3 device are 992 ± 138 Ω and 622 ± 2 kΩ, respectively, and 449 ± 29 Ω and 24.1 ± 0.1 kΩ for the Γ3N device. The circuit capacitance values are listed in Table 2.2.1.1. The circuit was derived for the gate voltages bracketing zero bias. The equivalent circuit resembles a small-signal equivalent circuit of the forward-biased p-n junction diode in which the circuit capacitance is the parallel combination of the junction and diffusion capacitances. The diffusion capacitance is the change in the stored minority carrier charge beyond the space charge region, which is alternately being charged and discharged through the junction as the voltage across the junction changes. The junction or depletion layer capacitance is normally much smaller than the diffusion capacitance and might be neglected.
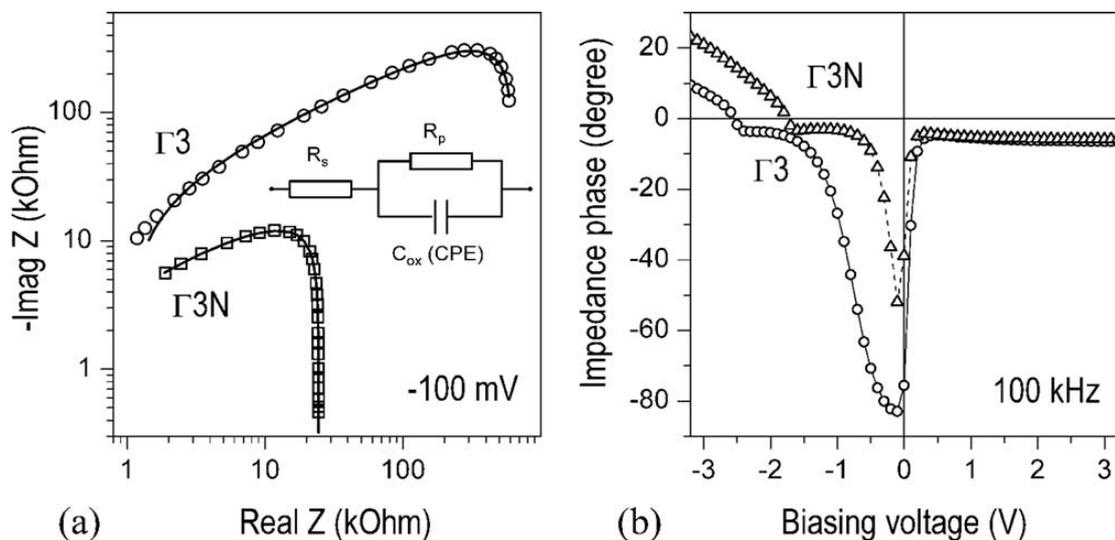

Figure 2.2.1.6: Left: (a) Log-complex impedance plot for Γ3 and Γ3N devices. The small-signal frequency spans the range of 1-300 kHz. The gate voltage is -100 mV. The inset shows an equivalent electrical circuit model for the LED (CPE stands for the constant phase element). Right: (b) The complex impedance phase as a function of the gate biasing voltage at the small-signal frequency of 100 kHz.

As the gate bias increases (being forward or reverse) the conductivities of the Γ3 and Γ3N device increase very rapidly and the equivalent circuit, which was described above, is no longer valid. The impedance phase as a function of the gate bias voltage is shown in the Fig. 2.2.1.6 at the fixed driving frequency of 100 kHz. As the forward voltage increases, the impedance phase decreases from around -90° (capacitive) to around -5°, and its derivative has a discontinuity at the kink voltage. Then, shortly after this, the phase becomes positive (inductive). This indicates that a

larger amount of charges is able to tunnel through the oxide layer without being trapped. [30] It is noteworthy that the bulk silicon edge emission was collected under these voltages (above the kink). The electrons tunnel through the oxide layer and ionize the silicon substrate where inefficient radiative recombinations take place.

Charge trapping: Capacitance-Voltage characterizations

Some high-frequency C-V measurements were undertaken in order to clarify the trap-assisted charge transport model described above. Figure 2.2.1.7 shows the C-V characteristics for $\Gamma 10$, $\Gamma 10N$, and $\Gamma 15$ devices.
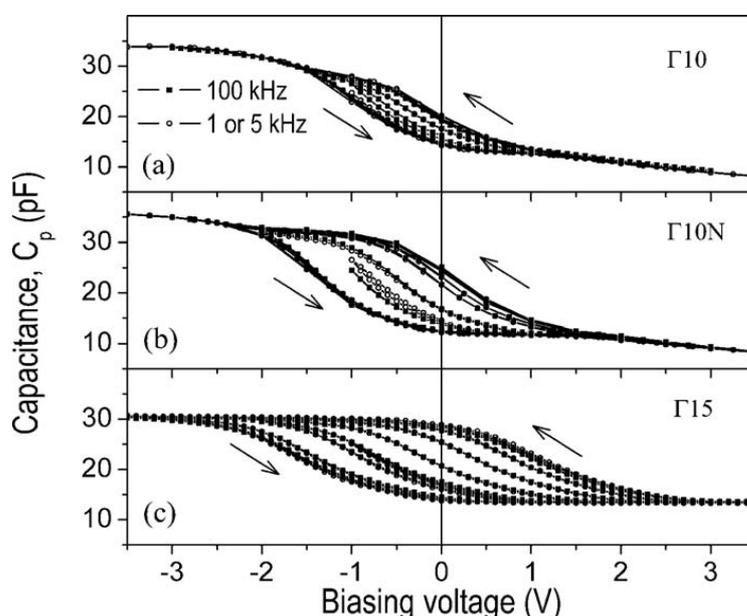

Figure 2.2.1.7: The hysteresis of capacitance-voltage characteristics for the high-Γ devices: Γ10 (a), Γ10N (b), and Γ15 (c). The small-signal frequency was 1 (or 5) and 100 kHz. The arrows indicate the scanning direction.

The measurements were performed in a progressive cycling manner around zero biasing voltage. The cycling start at zero voltage and the device was first swept to -1 and then to +1 V. In the subsequent cycling scans the absolute values of the biasing voltage increased by 1 V. C-V hysteresis was found at ±1 V cycle (the "scanning" voltage value is 1 V) and became wider and wider until the scanning voltage reaches the value of 6 V. The C-V curves have a distorted shoulder-like shape, which is more evident in the case of $\Gamma 10$ device. This shoulder might be attributed to the mechanism of charge trapping at the nc-Si/SiO$_2$ interface or near the interface

34

region. [31] There is another interpretation of the shoulder. It might be linked to the mechanism of charge tunneling into the nanocrystals, which is similar to the observations on quantum dots in compound semiconductors. [32] The hysteresis is counterclockwise (the arrows in the Fig. 2.2.1.7 point at the voltage scanning direction), that is the indication of a net positive charge accumulated in the oxide layer. No dependence of the C-V characteristic on the small-signal AC frequency was observed. This is attributed to a low density of the interface states at the SRO/substrate interface. [33] The C-V hysteresis correlates very well with the hysteresis observed in the I-V characteristic. Its width is larger for the high-Γ devices. The shift in the flatband voltage and the hysteresis width is larger for the $\Gamma10N$ device than for the $\Gamma10$ one, namely, it is 1.5 versus 0.75 V in the latter case. The $\Gamma10N$ device has around 3 at. % of nitrogen in excess with respect to the $\Gamma10$ device (see Table 2.2.1.1). The excess of nitrogen in the oxide matrix, which was introduced in the form of NH_3, slows down the formation of the nanocrystals. Nitrogen is bonded differently when deposited using NH_3 than nitrogen originating from N_2O which might be bonded to oxygen forming an O-N bond. In $\Gamma3N$ and $\Gamma10N$ devices nitrogen is threefold bonded to silicon as in Si_3N_4. This conclusion is derived from our XPS data analysis. Nitrogen tends to migrate to nc-Si interface where it is bonded to silicon and where it works as a diffusion barrier for oxygen. [34] This slows down the nanocrystal formation and creates interface trap states, which are due to the excess of Si-N dangling bonds. The C-V hysteresis width should scale linearly with the integrated PL intensity because both C-V hysteresis width and PL intensity depend on the nanocrystal density. [35] However, this does not hold for the measurements. The PL intensity values are in a reverse relation to the hysteresis width (Fig. 2.2.1.2). PL peak position for $\Gamma15$ is blue-shifted with respect to $\Gamma10$, which means that nanocrystals in $\Gamma15$ are smaller than in $\Gamma10$. The same holds for $\Gamma10$ and $\Gamma10N$ devices, as confirmed by XPS analysis. Taking this fact into account, the interface to volume ratio is increasing when Γ increases and hence the interface trap density will increase too. The smaller are the nanocrystals (the PL peak blue-shift is more pronounced) the larger is the hysteresis width.
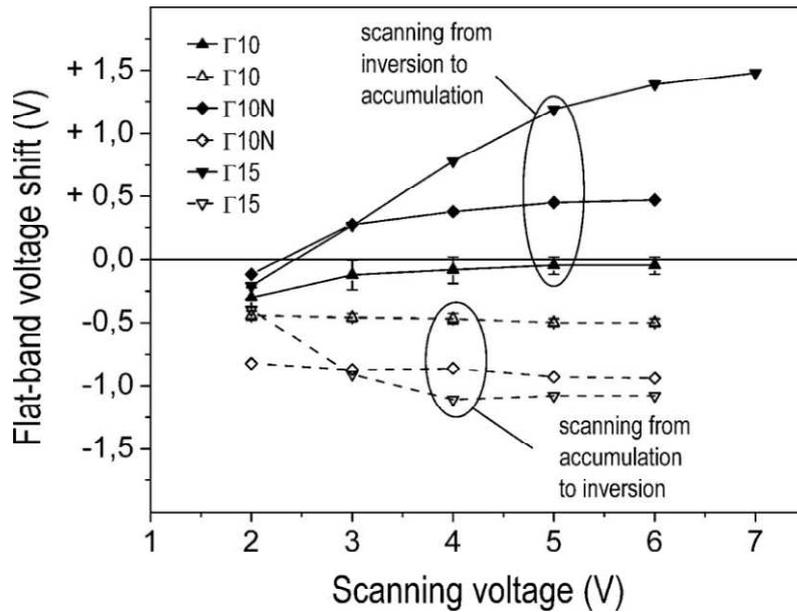
Figure 2.2.1.8: The flatband voltage shift as a function of the scanning voltage for the C-V measurements shown in the Fig. 2.2.1.7. Closed symbols: negative charge branches, open symbols: positive charge branches. See the text for details.

Estimating the flatband capacitance of the MOS structures, a shift in the flatband voltage, V_{FB}, with respect to the theoretical flatband voltage of about -0.9 V was found. The results are shown in the Fig. 2.2.1.8. A zero value of the flatband voltage shift corresponds to the neutral state of the oxide, while positive and negative values indicate the accumulation of net negative and positive charges, respectively. All fresh devices show some positive charge accumulated in the oxide layer. The bias change from positive to negative values (inversion to accumulation) leads to the negative charging of the oxide (electrons injection). Scanning in the opposite direction, from accumulation to inversion, charges the oxide positively. The positive and negative branches (open and closed symbols in Fig. 2.2.1.8, respectively) demonstrate different voltage dependencies for the Γ10 and Γ10N devices. Scanning from inversion to accumulation (electrons injection) brings about the neutral state for the Γ10 device and negative charge trapping for the Γ10N device under the scanning voltage above 2 V. Higher scanning voltages are needed to reach the neutral/negative oxide state (reverse bias), while the positive oxide state is almost voltage independent. This points to a different origin of the positive and negative charges in the oxide layer: the positive charge come from detrapped interface states at the nc-Si/SiO$_2$ interface, while

the negative charge is due to injected electrons, which become trapped at the nc-Si/SiO$_2$ interface. The process of charge trapping/detrapping is reversible. In the case of Γ15 device, the number of detrapped interface states and, hence, the net positive charge of the oxide increases when the forward-bias voltage increases. At the scanning voltage of 4 V the net positive charge saturates. It is noteworthy that Γ10N and Γ15 have a larger capacity to trap injected electrons in excess with respect to the Γ10 device. To summarize, the observed C-V hysteresis is due to the trapping and detrapping of injected electrons at the nc-Si/SiO$_2$ interface rather than charging and discharging of silicon nanocrystals itself. The trap density is estimated from the following equation: $N_t = C_{OX}V/qA_G$, where N$_t$ is the trap density, A$_G$ is the gate area, C$_{OX}$ is the oxide capacitance, and V is the hysteresis width. The estimates are 5×10^{11} and 10^{12} cm^{-2} for Γ10 and Γ10N devices, respectively. The oxide capacitance value, C$_{OX}$, could be read directly from the measured C-V characteristic. These values for all devices are listed in the Table 2.2.1.1. The oxide capacitance values allow estimating the oxide dielectric constant (see the Table 2.2.1.1). The dielectric constant value for the Γ3 device agrees well with the value obtained from the Poole-Frenkel model, which supports the model for trap-assisted electrical conduction.

Electroluminescence

Figure 2.2.1.9 shows the integrated EL as a function of injected current and gate voltage. No EL emission from nanocrystals was recorded for low-Γ devices, Γ3 and Γ3N, where PF and TAT are the main conduction mechanisms below and above the kink voltage, respectively. Only silicon bulk edge emission is present in these devices at the applied voltages above the kink value, when electrons are injected directly into the oxide conduction band and, being accelerated through the oxide layer, gain sufficient energy to generate electron-hole pairs in the silicon substrate. It is clear from Fig 2.2.1.9 that the Γ10 device shows the highest external power efficiency. At the same injected current the Γ10 device shows the largest emission at the lowest applied voltage. The power efficiency value was conservatively estimated to be 2×10^{-4} % (measured with a silicon photodiode placed a few millimeters above the device; no corrections for the collection geometry

were taken into account). The lack of EL emission under low forward-bias voltages (injected currents, respectively) and the low value of the external power efficiency are attributed to the TAT that is larger in these devices than the direct tunneling. At high injected currents the EL intensity becomes a sublinear function of the current, because of an increase in the rate of nonradiative processes. At the current value of 10 µA the EL intensity from $\Gamma 15$ device becomes larger than the EL intensity from $\Gamma 10$ device. However, the gate voltages that provide this EL intensity are much higher for $\Gamma 15$ than for $\Gamma 10$. As a result, the EL spectra of $\Gamma 15$ are much broader having an emission wing that extends to short wavelengths.
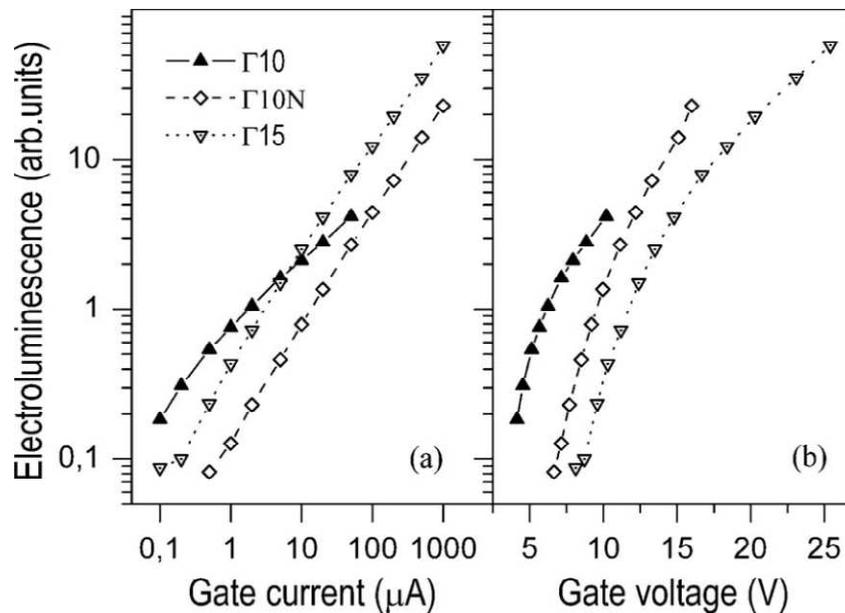

Figure 2.2.1.9: Total integrated EL intensity as a function of the injected current (a) and applied gate voltage (b).

The EL spectra collected at the injected currents of 5 and 50 µA are shown in the Fig. 2.2.1.10. The short-wavelength wing appears in the EL spectra of all devices at the current of 50 µA. This wing in EL emission might be attributed to the recombination of electron-hole pairs generated by hot electrons injected under high forward-bias voltages. [36] A broad visible EL emission was also recorded under large reverse bias. This white EL emission from a reverse-biased silicon p-n junction has been already observed in similar nanostructures, and it has been well studied. [37] The clear differences between the PL and EL spectra provide another argument

for the hot-electron mechanism of EL emission. The red-shift in the EL spectrum of Γ10 device at low injected currents can be also rationalized with the fact that only large nanocrystals could be luminescent as a result of rapid carrier tunneling. [38]
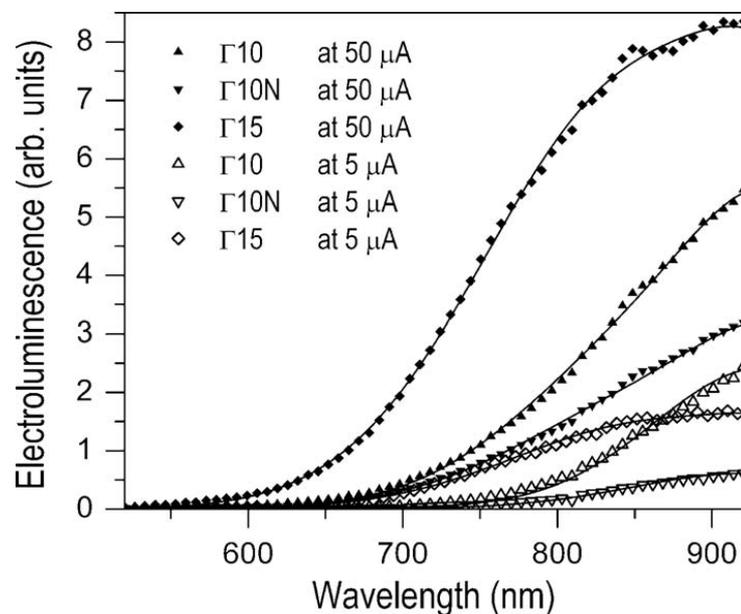

Figure 2.2.1.10: EL spectra for high-Γ devices at the injected currents of 5 and 50 µA. The spectra are normalized for spectrograph response.

Conclusions

The nc-Si LEDs were grown by PECVD technique, and their electrical conduction mechanism and light emission were analyzed in detail. An equivalent electrical circuit for the LED was derived from the complex impedance experiment. The hysteresis effect found in the current-voltage and capacitance-voltage characteristics is explained by electron trapping at nc-Si/SiO$_2$ interface traps. The decrease in silicon content and/or increase in nitrogen content promote the formation of smaller nanocrystals and, hence, increase the nc-Si/SiO$_2$ interface trap density, which serves as electron generation-recombination centers. The absence of the EL emission under low forward-bias voltages might be attributed to a large number of interface trap states and TAT. The EL emission observed under forward-bias voltages above 5 V is due to the hot-electron injection and impact ionization. The TAT and charge trapping near the nc-Si interface are the main reason behind the low power efficiency of the devices.

2.2.2. Multilayer LEDs Properties

Among all the techniques used to produce passivated nc-Si, [39] [40] layer by layer deposition [41] [42] of amorphous silicon or SRO and SiO_2 is a promising approach offering a better control over the density of nc-Si as well as their size distribution. It has been also reported that the self-organization of the silicon nanocrystals in the layer-growth direction could be promoted in nc-Si superlattice structure, through which the resonant tunneling occurs and facilitates the carrier transport perpendicular to the layers. [43] [44] Although there are plenty of results of structural and PL studies, electroluminescence (EL) devices and carriers transport of nc-Si superlattice structure are not well understood yet. [45] [46]

As for device application, it is essential to understand the carrier transport inside the nc-Si systems. When separated by relatively thick oxide barrier, carriers can be injected into nc-Si by Fowler-Nordheim tunneling. [47] [48] This energetic tunneling process degrades the oxide and causes reliability problem to the devices. However, considerable carrier injection is necessary to achieve enough output for nc-Si LED. Therefore, reducing the barrier thickness at the value where direct tunneling occurs could be a solution to decrease the driving-voltage, thus making more reliable devices.

Devices Fabrication

The SRO/SiO_2 multilayer[3] was deposited by PECVD on (100) p-type silicon (8-20 Ω cm) substrate. Before deposition a HF dip was applied to all substrates to remove the native oxide. The deposition procedure started with a SiO_2 deposition. After that, the PECVD chamber was pumped down, and filled with a new ratio of SiH_4 and N_2O for SRO deposition. SRO layer was grown after gas stabilization. The alternative growth of SiO_2 and SRO was repeated for 5 periods and ended with an addition SiO_2 deposition. Two samples with 3 nm or 4 nm (nominal thickness) SRO layers are investigated and their structures were verified by the variable angle spectroscopic ellipsometry. Some details are shown in Table 2.2.2.1. The total thickness of the structure varies from 20 to 30 nm depending on the layer thickness.

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[3] Fabbricate at FBK

Nominal Multilayer Thickness	SRO layer thickness (nm)	SiO$_2$ layer thickness (nm)	Total thickness (nm)
SRO 4nm/SiO$_2$ 2nm	3.12 ± 0.02	1.52 ± 0.03	24.72 ± 0.28
SRO 3nm/SiO$_2$ 2nm	1.94 ± 0.02	1.84 ± 0.03	20.74 ± 0.28

Table 2.2.2.1: Layer thicknesses of the as-deposited SRO/SiO$_2$ multilayer structures obtained from ellipsometry, total thickness of the structures is calculated from the layer thickness and the number of the layers (5 layers of SRO and 6 layers of SiO$_2$)

The atomic composition of the films was obtained by X-ray photoelectron spectroscopy[4]. The SRO layer in the multilayered stack is composed by 52 at. % of silicon, 44 at. % of oxygen, and 4 at.% of nitrogen. Assuming the composition of SiO$_2$ as 33 at. % of silicon and 67 at. % oxygen, the average silicon content is 45 at. % in the (SRO 4nm/SiO$_2$ 2nm)×5 multilayer and 44 at. % in (SRO 3nm/SiO$_2$ 2nm)×5 multilayer.

After the multilayer deposition, 100 nm n-type doped polysilicon was deposited on the multilayered structure as the semi-transparent gate electrode. Wet oxidation was then performed at 1150 °C for 30 minutes to grow both 480 nm thick field oxide for device isolation and nc-Si in the gate dielectric. Different geometries were used for the metallization: a circular geometry with a ring-shaped metal line for emission study (LED) and disc geometry entirely covered by the metal contact for electrical studies (capacitor). In the LED geometry, the poly-Si is covered by an anti-reflective coating formed by a 50 nm thick Si$_3$N$_4$ layer and a 120 nm thick SiO$_2$ layer to improve light extraction. The integrated effect of 100 nm poly-Si plus 50 nm Si$_3$N$_4$ and 120 nm SiO$_2$ layer is to optimize the transmittance (T) in a wide spectral range: T is larger than 50% at 500 nm and larger than 85% from 650 nm onwards.
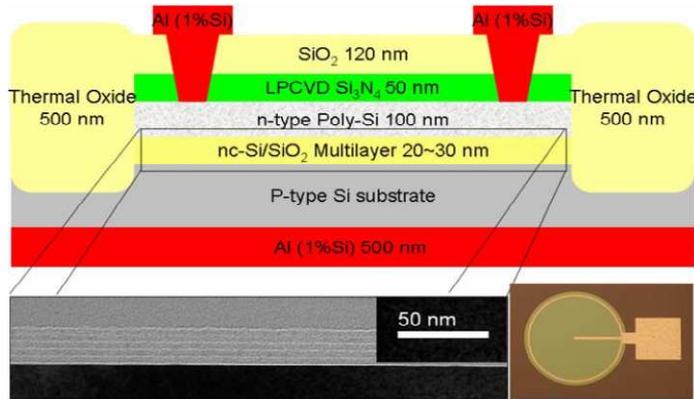
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[4] Performed at FBK

Figure 2.2.2.1: LED schematic cross-section (top), top view of the LED (bottom right) and TEM image (bottom left) of the nc-Si/SiO$_2$ multilayer (annealed structure of SRO 4 nm/SiO$_2$ 2 nm, 5 periods).

Fig. 2.2.2.1 reports the schematic cross section, top view of the device and the cross-sectional TEM image of the nc-Si/SiO$_2$ multilayer. The periodic structure is revealed as alternating white and grey stripes, which are SiO$_2$ layers and nc-Si layers, respectively. The multilayered LED characteristics will be compared with the best characteristics of the single active layer LED prepared and studied in the previous section (Γ15). The single active layer has the thickness of 49 $\pm$ 2 nm and the composition of 44 at. % of silicon, 50 at. % of oxygen and 6 at. % of nitrogen. It has to be noticed that the average silicon content value of the single layer LED is very close to the value of the multilayered LED.

Ellipsometry and photoluminescence studies

The layer thickness of as-deposited SRO/SiO$_2$ multilayered structure shown in Table 2.2.2.1 was obtained from ellipsometry measured with three angles (50°, 60° and 70°) in the spectral range from 300 nm to 850 nm. The refractive index and extinction coefficient versus wavelength of SRO and SiO$_2$ materials were determined from single layers in advance. By modeling the multilayered structure with those predetermined parameters, layer thickness of SRO and SiO$_2$ in multilayer was obtained as well as the total thickness of structures. One should notice that the actual layer thickness is less than the nominal value estimated from deposition rate. The origin of this difference is in the delay of plasma ignition. After annealing, silicon nanocrystals grow from the SRO layer.

As an alternative, TEM image of annealed structure is shown in Fig. 2.2.2.2. One should notice that the nc-Si layer is thicker than the initial SRO layer if we compare the SRO layer thickness in Table 2.2.2.1 with the TEM image. The thickness difference points to the fact that during high temperature annealing Si atoms diffuse perpendicular between the layer, which, as a result, roughens the layer interface and moves the boundary into the SiO_2 layer.
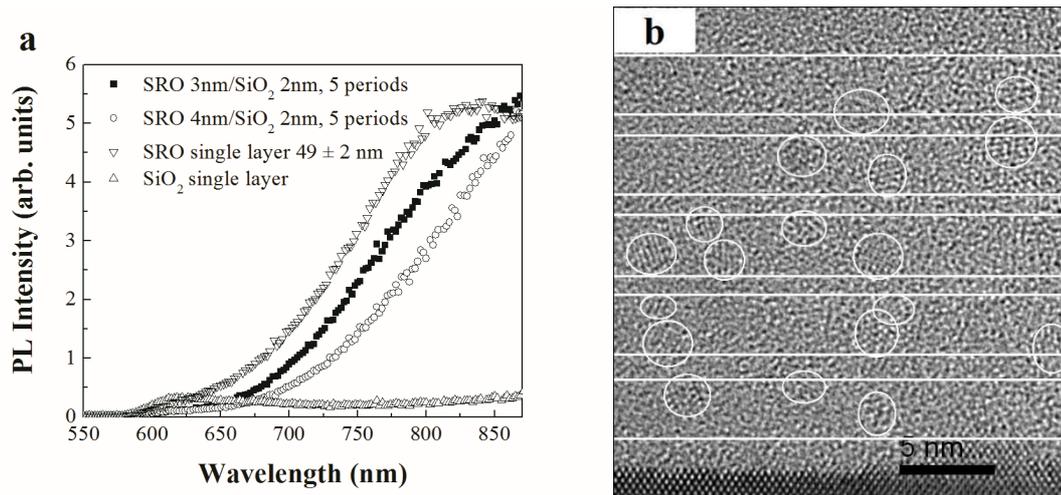

Figure 2.2.2.2: (a) Photoluminescence spectra of the nc-Si/SiO$_2$ multilayers (Ar laser line at 488 nm, ~15 W/cm^2). Single layer of SRO and SiO$_2$ are shown for comparison. The thickness of the SRO single layer is 49 ± 2 nm. SRO single layer was annealed at 1050 °C for 1 hour. The total thickness of multilayered structure is between 20 ~ 30 nm (see Table 2.2.2.1), and annealed at 1150 °C for 30 minutes. (b) High resolution TEM image of multilayer SRO 4nm/SiO$_2$ 2nm is shown. The average size of silicon nanocrystals is around 2.5 nm. For clarity, the visible nanocrystals are highlighted by circles and the layers are indicated by the lines.

In Fig. 2.2.2.2 (a), the PL spectra of multilayered structures are compared with PL of SRO and SiO_2 single layer. PECVD SiO_2 film only shows weak luminescence around 630 nm which can be assigned to non-bridging oxygen hole center. [49] Since all the spectra were collected from the area covered by poly-Si, the absence of infrared luminescence in the SiO_2 sample excludes the presence of poly-Si light emission in this spectra range. The spectrum of SRO single layer shows a typical nc-Si emission band around 800 nm. Compared to similar systems which have been reported in Ref. (50) and Ref. (42), the average nc-Si size should be close to 2 nm. For multilayered structures with the initial SRO layer thicker than 2 nm, the PL bands red-shift into the near infrared and their maxima do not appear in the spectra range of Fig. 2.2.2.2 (a). Moreover, the PL spectrum of multilayer SRO 4nm/SiO$_2$ 2nm is further red-shifted than SRO

3nm/SiO$_2$ 2nm, which can be explained by the quantum confinement effect. The PL intensity of multilayered devices is comparable with the intensity of the single layer device while the thickness of single layer is about twice of the thickness of the multilayer. This might suggest that an higher nc-Si density was achieved by using multilayered approach. In Fig. 2.2.2.2 (b), the high resolution TEM image of multilayer SRO 4nm/SiO$_2$ 2nm is shown. The average size of silicon nanocrystals is around 2.5 nm, larger than the nanocrystal size we expect for single layer, which accounts for the red-shift of PL spectrum. Note that only crystals having the right orientation with respect to the incident electron beam can be seen by their lattice images. Most of the nanocrystals are contained inside the SRO layers while some of them grew over into the SiO$_2$ layer. This also should be attributed to the silicon diffusion between the layers which is enhanced by high annealing temperature.

Electro-optical characteristics

To compare the I-V characteristics of devices with single layer and multilayer, gate current density is plotted against the applied electric field, in Fig 2.2.2.3. Only the forward bias branch in the I-V curves is presented (applying negative voltage on the n-type poly gate and grounding the substrate). The measured electric field is calculated from the applied gate voltage and the total thickness of the structure (shown in Table 2.2.2.1).
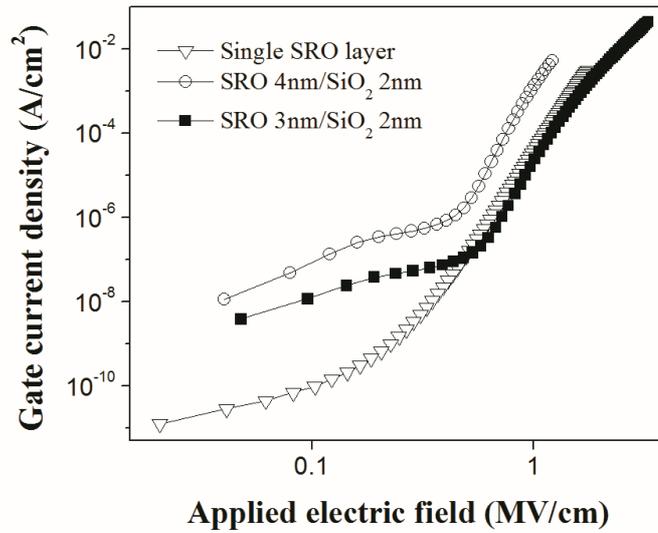
Figure 2.2.2.3: Gate current density as a function of applied electric field. Two distinct regions can be observed in this log-log plot. Multilayered devices show much higher current density in the low electric field region. The multilayer SRO 3nm/SiO$_2$ 2nm has the same average silicon content as the single layer and lower silicon content than the SRO 4nm/SiO$_2$ 2nm.

In Fig. 2.2.2.3, two distinct regions can be observed in the log-log plot, which are more evident in the multilayered devices. The current density show a weak increase in the low electric field region (for multilayered devices, it is up to ~0.5 MV/cm) and increases much faster in the region of high fields. The device with SRO 3nm/SiO$_2$ 2nm structure shows a current density two orders of magnitude larger than that of the single layer LED at the low electric fields. With the increasing of the field, the difference of the current density between single layer and multilayer becomes smaller. Taking into account the same average silicon content, the device with SRO 3nm/SiO$_2$ 2nm structure has the same high-field I-V characteristic as the single layer LED. In the whole field range, the device with SRO 4nm/SiO$_2$ 2nm structure shows higher current density than the other devices. This observation is consistent with the difference in the silicon content.
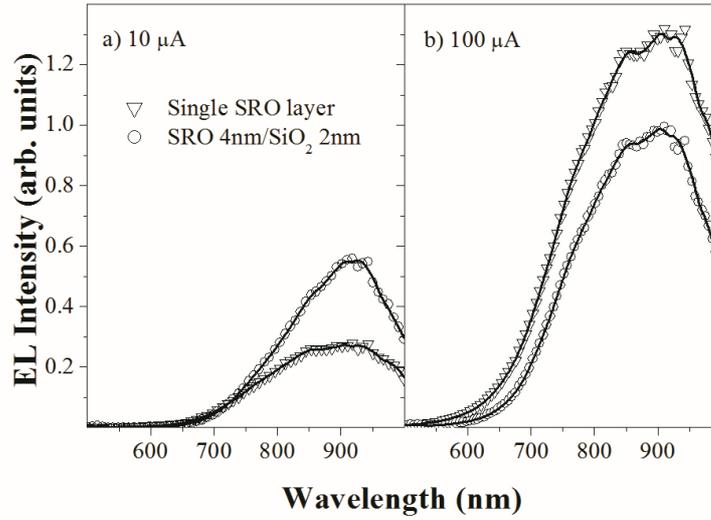
Figure 2.2.2.4: Electroluminescence spectra at the injection current of 10 µA (a) and 100 µA (b). (a) The gate voltage is 13.5 V and 3.4 V for the single layer LED and multilayer LED (SRO 4nm/SiO₂ 2nm), respectively. (b) The gate voltage is 18.4 V and 5.2 V for the single layer LED and multilayer LED (SRO 4nm/SiO₂ 2nm), respectively.

The device with thicker SRO layer has higher silicon content and, possibly, larger nc-Si size, which leads to the higher conductivity. The enhanced currents at the low electric fields in multilayered device originates from the direct charge tunneling from the substrate into the silicon nanocrystals and then into the gate. In the multilayered structure, high nanocrystal density is expected. Silicon nanocrystals grow closer to each other both in the layer plane and vertical direction. The oxide thickness is reduced between the nanocrystals which facilitates the carrier transport.

Electroluminescence spectra collected from the single layer and multilayered LEDs are shown in the Fig. 2.2.2.4. The spectra from SRO 4nm/SiO₂ 2nm and SRO single layer devices peak at about the same wavelength, 920 nm under low (10 µA) and high (100 µA) injected current. At the same injected current of 10 µA, EL peak intensity almost doubles in multilayered device, while the applied gate voltage is four times smaller than single thick layer LED (Fig. 2.2.2.4 (a)). Although the decrease in the applied voltage is partially due to the thickness difference, the higher EL intensity at the same injection level still indicates an efficient electrical excitation in the

46

multilayer. The power efficiency measured at 10 µA is 2×10^{-4} % for the single layer device and 10^{-3} % for the multilayered device. However, at 100 µA the EL emission is larger in the single layer LED (Fig. 2.2.2.4 b), which points to a change in the light emission mechanism at this high applied bias (18.4 V). In the previous section 2.2.2 it is shown that the EL emission at high voltage originates from hot-electron injection and impact ionization, and it is more sensitive to the applied voltage rather than injection current. Moreover the efficiency of both LEDs decreases as the injected current increases. Under high injection level, nonradiative recombination processes, such as Auger process, [51] become prominent, at the same time the electric stress induced oxide defects could be multiplied under a high voltage. Both of them reduce EL efficiency.

Under low applied voltage, the carriers are injected mostly through tunneling process. [52] As discussed in Fig. 2.2.2.3, the current is increased probably due to the contribution of direct tunneling component. Therefore, it is reasonable to believe that this direct tunneling component increases the EL efficiency at an applied bias as low as 3.4 V in multilayered device.

Conclusions

The structural and electro-optical properties of nc-Si/SiO$_2$ multilayered LEDs have been studied. The as-deposited and annealed multilayered structures grown by PECVD were examined by ellipsometry and TEM. Higher nc-Si density was indicated for multilayered structure by comparing the PL intensity of multilayer with thick single layer under similar average silicon content. The PL band located into the near-infrared region can be tuned by the size of nc-Si depending on the thickness of SRO layer. The carrier transport and EL are dominated by different mechanisms under low and high electric fields. At high fields, the EL originates from impact ionization showing a low efficiency. While at low fields, the injected current is increased by two orders of magnitude due to higher nc-Si density in the multilayered devices. For the multilayer LED, the EL intensity is increased even under low bias (3.4 V) showing higher power efficiency. This phenomenon might suggest bipolar injection of electron and hole into nc-Si through the direct tunneling under low bias.

2.3. Power Efficiency Under Unipolar and Bipolar Carrier Injection

Based on the previous results we optimized LED to achieve a bipolar (electrons and holes) current injection into silicon nanocrystals in thin nanocrystalline-Si/SiO₂ multilayers. To confirm the bipolar character, different devices were grown, with and without a thick silicon oxide barrier at the multilayer contact electrodes.

Devices Fabrication

The device structure is a metal oxide semiconductor capacitor where alternating stoichiometric SiO_2 and silicon-rich oxide (SRO) layers with large Si excess is used as the gate oxide (shown in previous section 2.2.2.2). The nominal thickness of SRO and oxide layer within a ML is 3 and 2 nm, respectively. Silicon nanocrystals were formed by annealing the ML at 1150 °C for 30 min in nitrogen. Si p-type substrate was used.
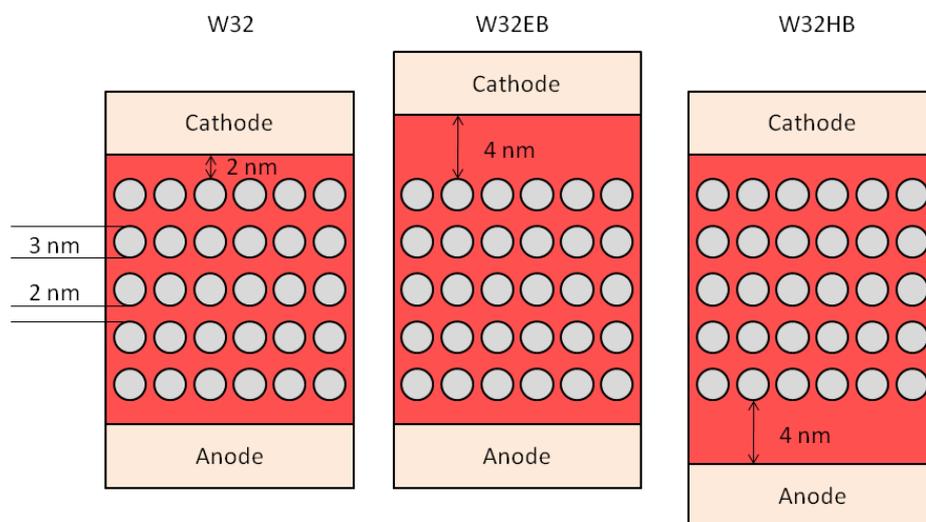

Figure 2.3.1: Schematic cross section of three devices: W32, W32EB, and W32HB. Silicon nanocrystals (grey dots) and silicon oxide matrix (red background). Note that the overall SiO₂ thickness facing the electrodes is 2 nm for W32 and 2 nm or 4 nm for W32EB and W32HB.

Details on fabrication, structural characterization could be found in section 2.2. The gate area of the LED is $1.02{\times}10^{-3}$ cm^2. Three structures with five ML periods were grown (Fig. 2.3.1): W32, the ML with 2-nm-thin oxide at both top (gate) and bottom (substrate) of the ML stack; W32HB,

the ML with 2-nm-thick oxide at the top and 4-nm-thick at the bottom of the ML, which serves as a tunneling barrier for holes; W32EB, the ML with 2-nm-thick oxide at the bottom, and 4-nm-thick oxide at the top of the ML which serves as the tunneling barrier for injected electrons.

Power Efficiency Measurement

Figure 2.3.2 shows power efficiency as a function of injected current density for W32. The maximum power efficiency of 0.17% is achieved at the smallest injected current density of 4.9×10^{-4} mA/cm^2, where the optical power density is 1.4×10^{-3} µW/cm^2. The applied gate voltage is 1.7 V, which corresponds to an electric field of 1.1 MV/cm. (The applied electric field is calculated as the ratio of the applied gate voltage to the actual ML thickness, which is 15.6 nm for W32, and 17.3 nm for both W32EB and W32HB).
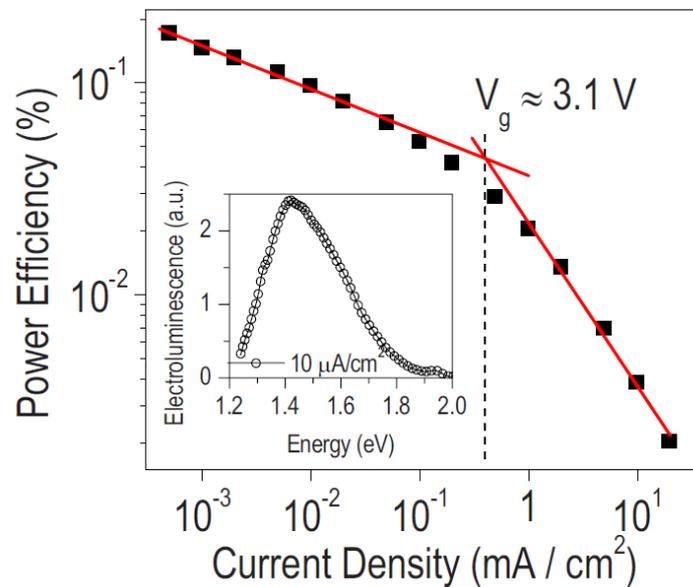

Figure 2.3.2: Power efficiency as a function of the injected current density for the ML device without a thick injection barrier (W32). The dashed line indicates the current density which separates dominant bipolar injection, which is more efficient, from dominant unipolar injection through the FN tunneling. The inset shows the electroluminescence spectrum of W32 recorded for an injection current of 10 µA/cm^2. The spectrum is normalized to a spectrograph response.

The high power efficiency is attributed to the radiative recombination of excitons formed by both electron and hole injection into silicon nanocrystals via direct tunneling mechanism. The maximum optical power density of 2.6 µW/cm^2 is reached at the largest injected current density

of 20 mA/cm^2 when the power efficiency is the smallest, 2×10^{-3} %. The power efficiency dependence on injected current shows two distinct regions: a region of low currents, when the efficiency decreases slowly, and a region of high currents, when it decreases rapidly. The first region is attributed to the bipolar (electrons and holes) injection into silicon nanocrystals under the direct tunneling regime. The direct tunneling is the dominant charge transport mechanism in structures with thin, < 2.6 nm, oxide layers. [27] The high power efficiency measured shows that direct tunneling is important to achieve it. The second region of high current densities is due to the dominant unipolar (electron) injection into silicon oxide conduction band by the field-enhanced FN tunneling. [53] The transition between these two regions occurs at the applied voltage of 3.1 V (an applied field of 2.0 MV/cm), which corresponds to the energy barrier height (band offset) for electrons at the Si/SiO$_2$ interface. The electron barrier height controls the onset of FN tunneling. In the second region, i.e., above 3.1 V, electrons from the gate are injected in the conduction band of the silicon oxide: these hot electrons loose energy by electron-hole pair generation in nc-Si or by creating defects in the oxide matrix. The power efficiency in the FN regime of this LED is comparable to the one of Ref. (54), which has power efficiency of 5.6×10^{-3} % (external quantum efficiency of 0.2 % with an operating voltage of 36 V). This shows that the FN regime yields lower efficiency than the direct tunneling regime.

Bipolar Carrier Injection

In order to prove the bipolar character of charge injection at low bias, the electro-optical characteristics of W32HB and W32EB were studied. The thick oxide layer in W32HB will blocks injection of holes from the anode (p-type Si substrate). Likewise, the thick oxide at the cathode side (n-type polycrystalline Si gate) blocks the electron injection in W32EB.
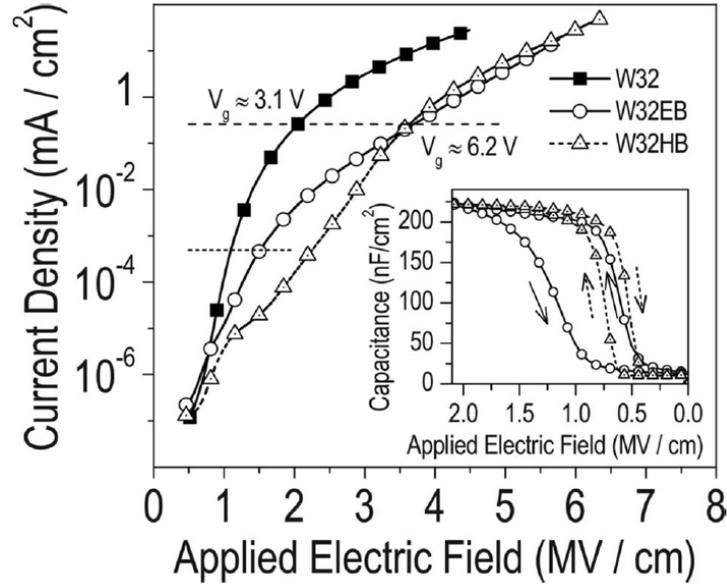
Figure 2.3.3: Current density as a function of the applied electric field (I-V characteristics) for three MLs: without thick injection barriers (solid squares), with the electron injection barrier at the gate (open circles) and with the hole injection barrier at the substrate (dotted triangles). The dashed line shows the transition current density (Fig. 2.3.2). The dotted line shows the onset of EL for W32 and W32EB. Inset shows capacitance-voltage characteristics for W32EB and W32HB devices. Arrows indicate the scanning direction of the hysteresis loop.

Figure 2.3.3 shows the I-V characteristics for the three devices in forward bias (negative bias is applied on the gate). W32HB shows smaller current densities than W32EB at the low/medium applied electric field, i.e., in the regime of direct tunneling. At higher electric fields when the FN tunneling becomes dominating, the same current densities are achieved. At the same current density, the applied electric field for both W32HB and W32EB is larger than that for W32. This is because of a large voltage drop in the thicker oxide layer, i.e., the carriers barrier. The electric field in the barrier oxide was calculated from the I-V curves as the voltage difference between the I-V curves of W32 and W32EB (W32EH) at the same current density and then divided by the oxide thickness, i.e., 4 nm. The barrier oxide field increases linearly with the applied electric field at low fields and then saturates at high applied fields. At low applied fields, part of the electrical charge is trapped close to the ML/barrier interface. In the case of W32HB this trapped charge is negative, while in the case of W32EB, the charge is positive. This is supported by capacitance-voltage (C-V) experiments. The C-V characteristics show a hysteresis behavior (inset in Fig. 2.3.3). The hysteresis is clockwise for W32HB meaning the trapping of net

negative charge at the ML/barrier interface. In contrast, the C-V hysteresis is counterclockwise for W32EB, meaning the trapping of net positive charge. The amount of the net trapped charge in W32EB is larger than in W32HB, which is supported by a difference in the C-V hysteresis width. The tunneling mobility and the barrier height are larger for holes than for electrons. Therefore the net trapped positive charge is larger than the negative charge. The screening of the applied electric field by the trapped charge at the ML/barrier interface is larger and the voltage drop in the barrier oxide is smaller in W32EB than in W32HB.

When the electric field across the barrier oxide in W32HB reaches the value of around 7.5 MV/cm, the oxide electric field pins because the accumulated electrons at ML/barrier interface start to tunnel into the conduction band of silicon oxide via the FN mechanism. In contrast, the linear regime in W32EB extends to larger applied electric fields because larger fields are required for the FN tunneling of holes. At the applied electric field of about 3.5 MV/cm (7.5 MV/cm across the barrier oxide), the field-enhanced FN tunneling of electrons becomes the dominant injection mechanism in both W32EB and W32HB. Above this threshold, the same current densities in W32HB and W32EB are observed.

Electro-Optical Characteristics

The light-current characteristics of the three devices are shown in Fig. 2.3.4. Very weak light emission from W32HB device is observed under high applied electric fields only. Even under the FN tunneling regime, the light emission is about two orders of magnitude lower than that for W32.
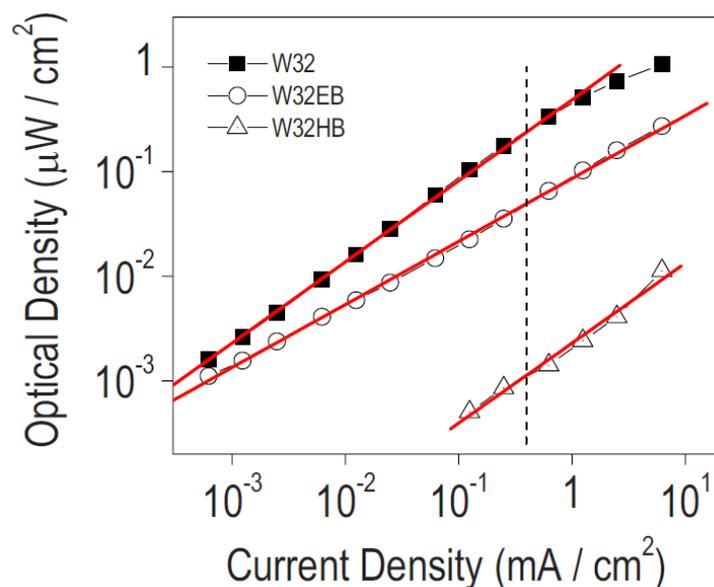
Figure 2.3.4: Optical power density as a function of current density for the MLs shown in the Fig. 2.3.3. The dashed line indicates the onset of FN tunneling.

In the direct tunneling regime, the light emission from W32EB starts at an applied field of about 1.5 MV/cm (the current density is lower than 1 $\mu A/cm^2$) and is much stronger than that of W32HB. This shows that indeed the holes are more difficult to inject than the electrons. In W32HB the oxide barrier blocks the injection of holes into the Si-nc and no electroluminescence emission is observed. When the applied electric field across the ML reaches the value of the field-enhanced FN tunneling, 3.5 MV/cm, weak EL signal appears which is attributed to impact ionization of electrons injected from the top electrode. The slope of the light-current characteristic is related to the internal quantum efficiency (i.e., the ratio of the radiative emission rate to the sum of radiative and nonradiative emission rates). From Fig. 2.3.4, W32EB has a smaller slope than W32, 0.60 ± 0.01 versus 0.77 ± 0.01, respectively. This difference in the slope values might be attributed to the hot carrier injection that takes place in W32EB. The presence of the oxide barrier at the top of the nc-Si ML and the accumulated positive charge at the nc-Si ML/barrier interface create an extra electric field across the oxide layer that accelerates the injected electrons. W32HB shows the same slope as W32, namely 0.77 ± 0.05. There is no extra acceleration of the injected electrons from the gate and the radiative to nonradiative rate ratio in the W32HB is equal to the rate ratio in W32.

Bipolar charge injection in ML nc-Si LED yields the highest power efficiency. The electrons and holes are injected into nc-Si from both top and bottom electrodes through the direct tunneling mechanism. This study also shows that the limiting phenomenon is the injection of holes.

2.4.   Power Efficiency Controlled by Band-Gap Engineering

Engineering of energy band gap of semiconductor nanocrystals promises a high impact in photonic and biomedical applications, as demonstrated with colloidal nanocrystals of compound semiconductors. [55] Band gap engineering of silicon nanocrystals (nc-Si) and their dense structurally ordered ensembles is studied to a much less extent (see for example Ref. (56)) even though nc-Si has a high potential impact in photonic applications. [57]

Here, it is proposed to engineer the energy band gap of dense nc-Si quantum dot ensembles via thickness/composition profiling of a multilayer nc-Si/SiO$_2$ structure. A multilayer (ML) approach allows the independent control of nc-Si size and density. [42] Upon annealing at a high-temperature, the thickness of non-stoichiometric silicon-rich silicon oxide (SRO) in the ML structure confines the nanocrystals size, while the excess silicon content of the SRO layer determines the nanocrystal density. [58] A control over the silicon oxide thickness is possible which ensures efficient injection and tunneling currents in nc-Si light emitting diodes (LEDs).

Since in ML LEDs the bipolar tunneling of electrical charges at low voltages was achieved, here a significant improvement of this scheme is proposed where the sizes of the nanocrystals increase from the active region towards the electrodes. In this way, the energy levels of the confined states in each layer gradually increase from the silicon value, so that reducing the energy difference between adjacent tunneling states. Moreover, the luminescence efficiency increases due to the presence of small nanocrystals in the active region. [59]

Devices Fabrication

 The details on the fabrication of the ML nc-Si LED and of their properties are reported in the previous section. The ML structure and formation of nc-Sis were confirmed by both ellipsometry and high resolution TEM. The actual thicknesses of the individual layers within the ML stack were somewhat smaller than the nominal thickness values.
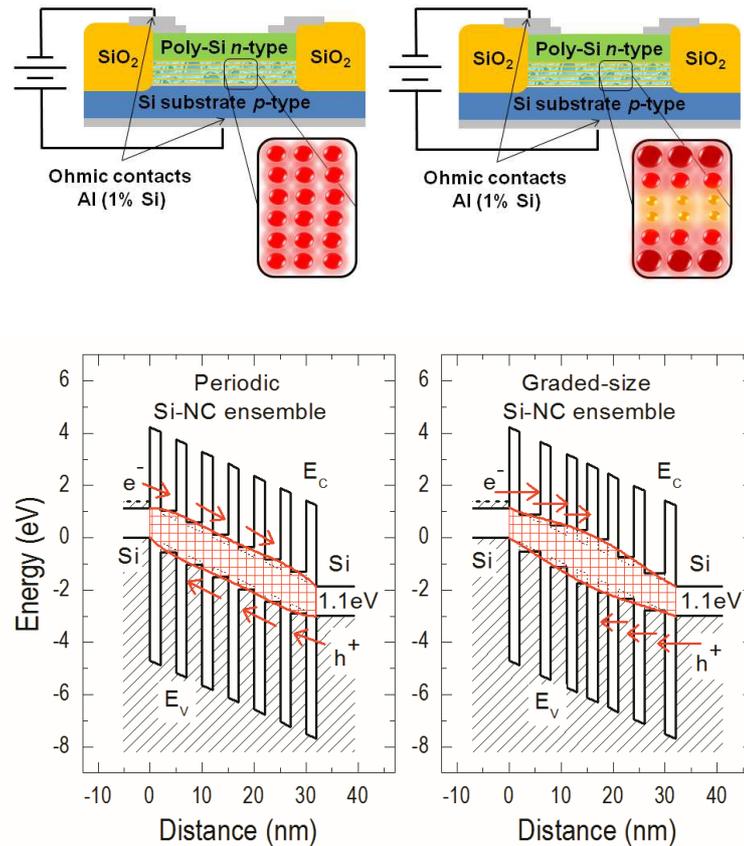

Figure 2.4.1: (top) Schematic of the ML nc-Si LED with periodic (left) and graded size (right) nc-Si ensembles. (bottom) Energy band diagram for a periodic (left) and the graded nanocrystal size ML nc-Si LED (right). E_C and E_V stand for the bottom of the conduction and the top of the valence energy bands, respectively. The red areas highlight the difference in the energy band gap of the active recombination region of the two LEDs. Notice an even alignment of the (electron and hole) ground states of Si-NC quantum dots and wider band gap in the middle of the active region of the graded-size LED. The arrows show direct tunneling (followed by a rapid thermalization) of electrons (e⁻) and holes (h⁺) from the cathode and anode, respectively.

The total ML thickness is found to decrease of about 30% of its nominal value. Several nc-Si ML structures are studied: periodic MLs with a nominal ML period of 4 nm (2 nm SiO_2 / 2 nm SRO),

5 nm (2 nm SiO$_2$ / 3 nm SRO) and 6 nm (2 nm SiO$_2$ / 4 nm SRO), having five ML periods each, and a ML with graded SRO thickness.

The graded ML has a stepwise decrease in the SRO thickness toward the ML centre (exact sequence of SRO layer thicknesses, in nanometers, is 4-3-2-2-3-4, see Fig. 2.4.1) and approximately the same average silicon content as the periodic ML of 3 nm SRO. All the SRO layers have the same composition. A schematic energy band diagram of a periodic and the graded-size (energy gap) nc-Si MLs are shown in Fig. 2.4.1. When an external bias is applied, the energy bands of the graded-size nc-Si ensemble align at low voltages (Fig. 2.4.1) which makes it easier for charges to tunnel into the central recombination region.

Electro-Optical Characteristics

The formation of nc-Si in ML structures is evidenced by the electroluminescence (EL) spectra shown in Fig. 2.4.2. The EL spectra of three MLs were collected at the same injection current density of 1 mA/cm^2. The peak EL intensity of the graded nc-Si ML is about 3 times larger than the one of the reference periodic ML with 3-nm-thick SRO layer (approximately the same average excess silicon content). The peak wavelength blue-shifts when the applied voltage increases which is shown in the inset of Fig. 2.4.2. This blue-shift is ascribed to small variations in the nanocrystal size of a periodic ML structure.
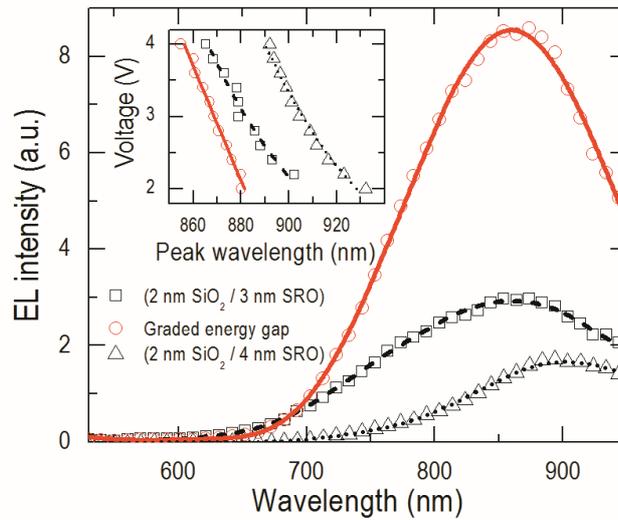
Figure 2.4.2: EL spectra of three nc-Si ML LEDs: periodic LED, 2 nm SiO$_2$ / 3 nm SRO; periodic LED, 2 nm SiO$_2$ / 4 nm SRO; and the LED with a graded energy gap. The spectra are taken at the same injection current density of 1 mA/cm^2. The spectra are normalized to the spectrometer response. The inset shows the peak wavelength dependence on the applied voltage. Lines are a guide to the eye.

In the whole range of applied voltages, the peak wavelength of the graded ML is smaller than the peak wavelength of the periodic ML with 3-nm-thick SRO, which is in turn smaller than the peak wavelength of the ML with 4-nm-thick SRO. This is in a good agreement with the quantum confinement effect. Together with the minor blue-shift of the peak wavelength and large EL intensity, it also indicates that the light emission of the graded ML originates mostly from the 2-nm-large nanocrystals in the centre of the ML stack. No PL was observed in the ML with 2-nm-thick SRO.

Electrical Characteristics

Another evidence for the improved charge injection in the graded ML and light emission originating from the smallest nanocrystals could be found in Fig. 2.4.3. It shows current-voltage (I-V) characteristics of the three ML devices. The charge injection is enhanced in the graded ML with respect to the reference periodic ML with 3-nm-thick SRO. The ML with 4-nm-thick SRO is more conductive due to higher average silicon content, larger nc-Sis and, hence, smaller band offset with respect to the silicon electrodes. On the contrary, the ML of 2 nm SiO$_2$ / 2 nm SRO

shows poor electrical conduction, which becomes unstable when high voltages are forced, and no EL. This is attributed to the large band offset with respect to the silicon electrodes, and to the low average silicon excess.
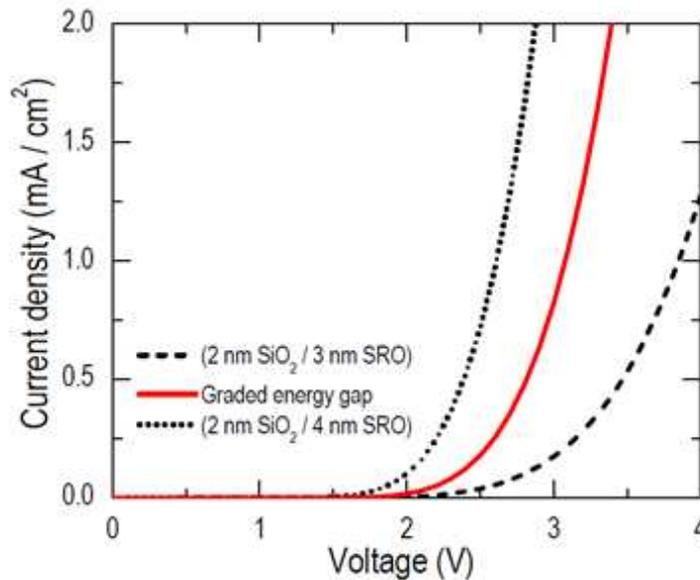

Figure 2.4.3: Forward I-V characteristics of the same three devices as in Fig. 2.4.2.

The graded-size structure is a good compromise between an ensemble of large nc-Sis with high electrical conductivity, but low luminescence, and an ensemble of small nc-Sis with high luminescence, but poor electrical conductivity. Indeed, radiative recombination rate increases when nanocrystal size decreases and, hence, an ensemble of small nanocrystals have larger emission efficiency than an ensemble of large nanocrystals. However, injection into small nanocrystals is hindered by a larger band offset of small nc-Si with respect to bulk silicon than that of large nc-Si. In contrast, an ensemble of large nc-Si (with lower energy band offset) exhibits large conductivity, but low emission efficiency. The graded gap structure, with a step-like increase in band offset, provides a desired compromise between high recombination rates (in small nc-Si) and large injection currents (in an ensemble of large nc-Si). When external bias is applied, energy band alignment of the graded-size nc-Si ensemble is achieved over a range of low voltages (Fig. 2.4.1)

58

Power Efficiency

Optical power density of these devices, along with the corresponding power efficiency η, as a function of the injection current density, J, is shown in Fig. 2.4.4.
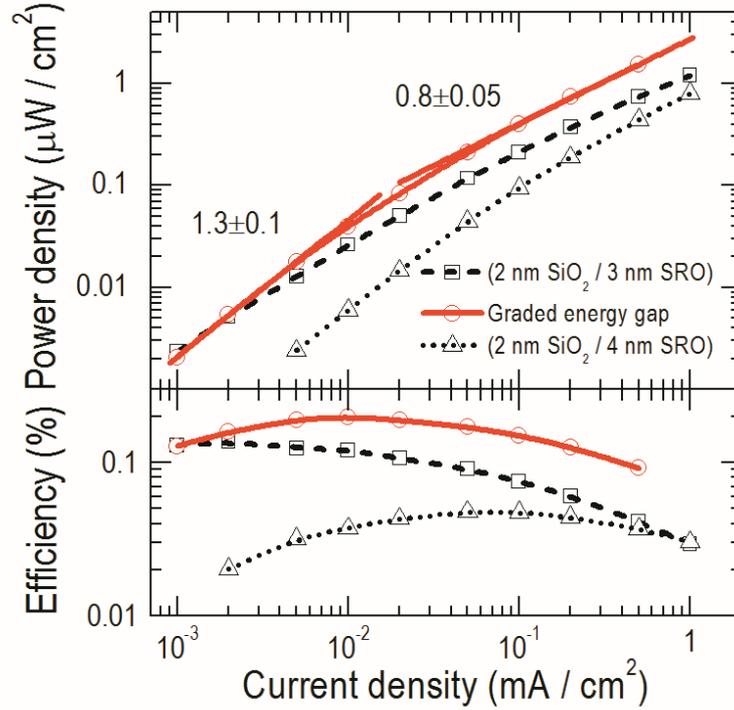

Figure 2.4.4: Optical power density as a function of injected electrical current density for the same three LEDs as in Fig. 2.4.2. Numbers indicate slope values of linear regressions. The bottom panel shows the corresponding power efficiency.

The optical power dependence obeys a power law, $\sim J^s$. A super-linear increase with s = 1.3 ± 0.1 at low J and a sub-linear increase with s = 0.8 ± 0.1 at high J are observed. The super-linear dependence is attributed to the presence of radiative and nonradiative competing recombination channels. As J increases, the radiative recombination of excitons in nc-Si takes over the recombination at nonradiative centres in the oxide matrix. At J ~ 10 $\mu A/cm^2$, recombination at the nonradiative centres saturates and optical power becomes an almost linear function of the current. At J ≥ 10 $\mu A/cm^2$, nonradiative Auger recombination becomes dominant and EL becomes a sub-linear function of J. η of the graded-size LED reaches a maximum of 0.2 % at J = 10 $\mu A/cm^2$ and

59

applied voltage of 2 V. η is about twice η of the corresponding periodic ML LED at the same J. The maximum optical power density is as high as 10 $\mu W/cm^2$.

Conclusions

In conclusion, the energy band gap engineering of nc-Si ensembles grown by PECVD or a similar CMOS compatible technique is possible with the size-controlled ML approach. The graded-size nc-Si LED shows superior performance in terms of power efficiency than periodic ML nc-Si LED. Therefore it is shown that tunneling engineering (control of the tunneling barrier and injection energy) of electrical injection into nc-Si might further improve the emission properties of the LED.

3.   Light Emitting Devices Under Pulsed Excitation

3.1.   Introduction

In this chapter, the power efficiency of silicon nanocrystal light-emitting devices is studied in alternating current regime. An experimental method based on impedance spectroscopy is proposed and an electrical model based on the constant phase element (CPE) is derived. It is, then, given a physical interpretation of the electrical model proposed by considering the disordered composition of the active material. The electrical model is further generalized for many kinds of waveforms applied and it is generalized for the direct current regime. At the end, time-resolved electroluminescence and carrier injection in alternate current regime are presented.

3.2.   Power Efficiency Under Pulsed Excitation

Alternating current (AC) light modulation with silicon based light emitting devices is a way to produce data stream for on-chip optical networks. In addition, AC driving is also believed to increase the efficiency of these devices. In most of the works in which the AC power efficiency measurements are shown, the value of power efficiency is not quoted [23] [60] [61] [62] or the accuracy of its estimation is unclear. [63] This is mainly due to the difficulty to measure the low currents flowing through the devices and it is complicated by the driving frequency values. In AC regime, the electroluminescence (EL) as a function of driving frequency shows a dependence similar to those in Fig. 3.2.1 (b). It is observed that the EL increases significantly as the frequency increases, it reaches a maximum and, then, it decreases. In the literature, this increase in EL is attributed to an efficiency increase while the decrease, at higher frequencies, is attributed to the Auger suppression of EL due to the finite exciton recombination lifetime.
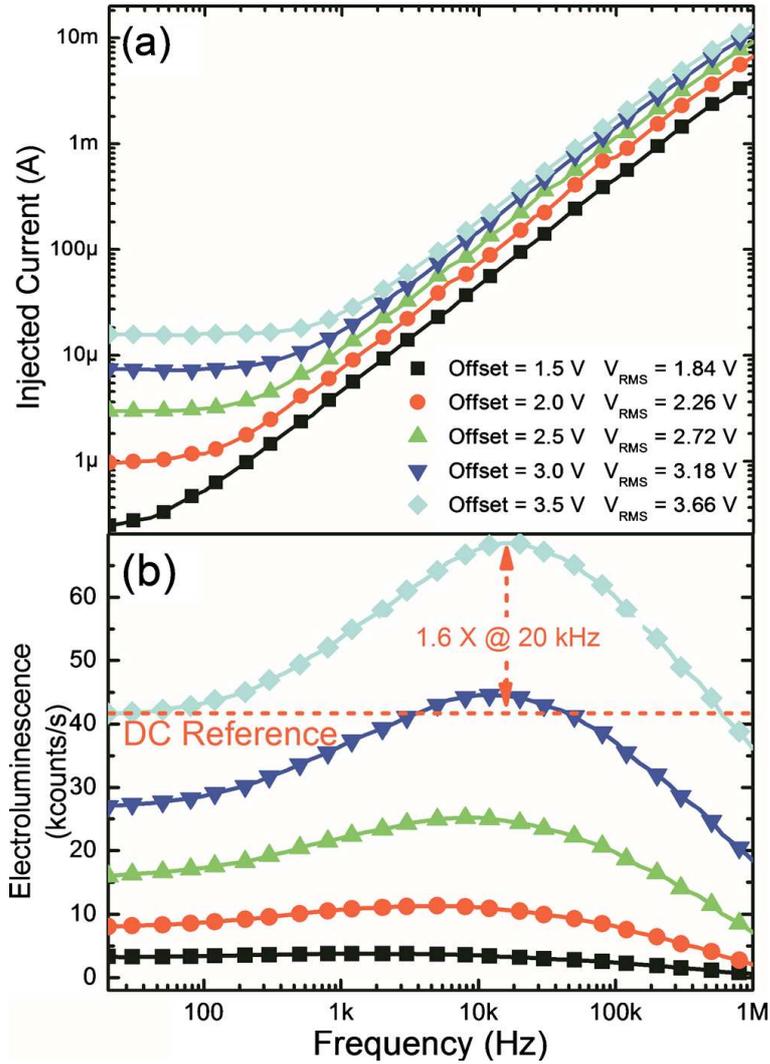
Figure 3.2.1: (a) Estimated RMS injected current as a function of frequency and different offsets applied and (b) EL as a function of frequency. The MOS-LED is biased by a sinusoidal waveform. The DC reference is measured with a DC bias equal to 3.66 V.

Here a detailed study of the efficiency in AC regime by measuring the injected electrical power with accuracy is presented. For this reason an experimental method to estimate the efficiency based on large signal impedance spectroscopy was developed.

Device Fabrication

The device used in this section is a multilayer silicon nanocrystal based metal-oxide-semiconductor (MOS) LED which shows high DC efficiency. The active material is composed by 5 layers of 3 nm thick silicon-rich-oxide (SRO) separated by layers of 2 nm thick SiO_2[5].

Electrical Power Estimation in AC regime

In order to estimate the electrical power injected under a sinusoidal modulation, the values of the time dependent voltage (V) and current (I) which are defined by the applied waveform and by the reaction of the device are considered. In the case of a sinusoidal waveform, the dissipated electrical power is given by the average electrical power:

$$P_{AC} = V_{RMS} \cdot I_{RMS} \cdot cos\varphi$$

V_{RMS} and I_{RMS} are the root mean square values of V(t) and I(t) and φ is their relative phase shift. While V_{RMS} is easily calculated from the driving bias, I_{RMS} estimation is difficult because of the typical reactive characteristic of the device (spikes, distortions, etc.), its low value and the frequency range of the applied signals. A way to circumvent this problem is to measure the device complex impedance, $Z(\omega,V)$, as a function of angular frequency, ω, in the interested range of frequencies and signals, and then, by applying the generalized Ohm's law, to calculate I_{RMS}. The injected electrical power in AC regime can be written as:

$$P_{AC} = \frac{V_{RMS}^2}{|Z|} \cdot cos\varphi$$

where φ is the phase of Z.

A wide range of modulations conditions (different waveforms, different peak-to-peak voltages, and different offset voltages), geometrical factors (different devices area and shapes), and material properties (SiO_2 barrier thickness and SRO thickness) were studied. Here, the results

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[5] Produced at FBK

obtained with sinusoidal waveform of a fixed peak-to-peak voltage (V_{pp}) value of 3 V and for different offset voltages as a representative set are presented. Figure 3.2.1 (a) shows I_{RMS} for different offset voltages. The range of offsets (from 1.5 to 3.5 V) is determined on the basis of the EL turn-on DC voltage of 2 V and of the maximum driving voltage before device failure of 5 V.
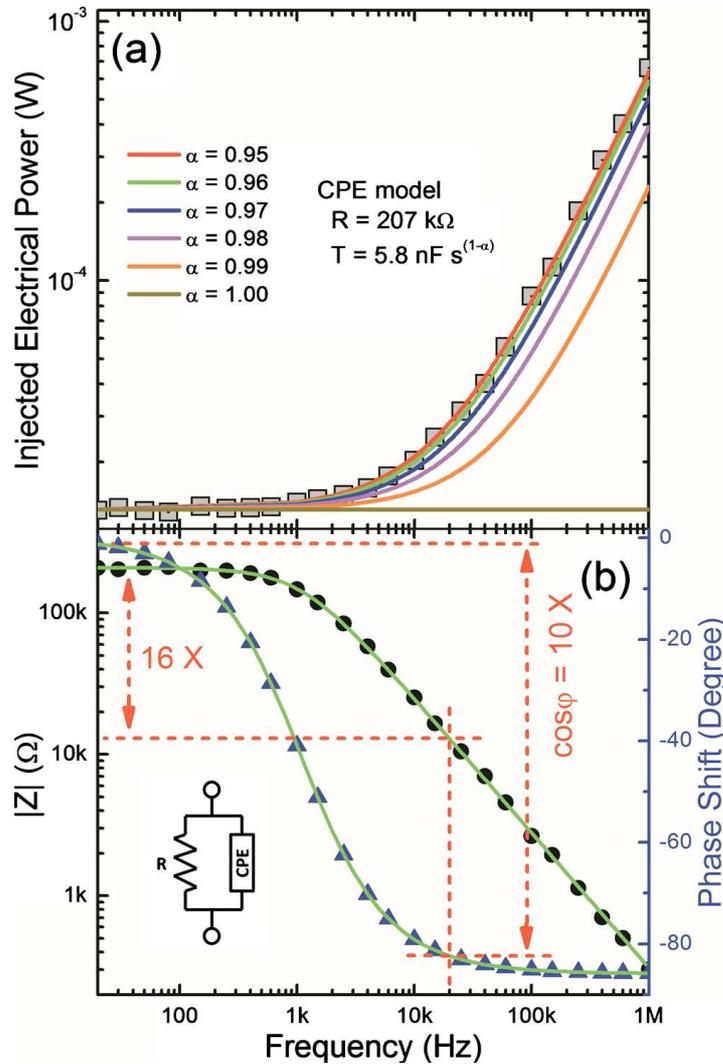

Figure 3.2.2: a) (Squares) Estimated injected electrical power; (lines) CPE model fits as a function of α value; b) (dots) module of complex impedance characteristics as a function of frequency; (triangles) phase of complex impedance as a function of frequency; (lines) fit of the data by R-CPE parallel equivalent model (inset): R = 207.2 ± 0.7 kΩ, T = 5.8 ± 0.3 nF s$^{-0.05}$, and α =0.95 ± 0.01. Measurement data are for an offset = 3.5 V and V_{RMS} = 3.66 V.

The measurements show an increase in the injected current of few orders of magnitude as a function of frequency. During the frequency scan, V_{RMS} was kept constant. Thus, the maximum enhancement of the ac EL by a factor of 1.6 (Fig. 3.2.1 (b)) cannot compensate the increase in

injected power, as it will be shown later. Consequently, the power efficiency decreases. More in details, Fig. 3.2.1 (a) shows that the dependence of the current on the frequency is first constant and then rises rapidly. The frequency range of the flat part depends on the voltage offset. This is due to the fact that the span in voltage, during a modulation period, covers different region of the I-V characteristics.

More insights can be obtained by looking at the impedance characteristics of the device. As an example, Fig. 3.2.2 (b) shows the characteristics when the EL is the strongest: offset of 3.5 V and V_{RMS} = 3.66 V. The impedance is well fitted by a parallel combination of a resistor (R) and a constant phase element (CPE). [64] The impedance of CPE is defined as $Z_{CPE} = 1/T(j\omega)^{\alpha}$, where T is a constant (with units F s$^{\alpha-1}$), ω the angular frequency and α ($-1 \leq \alpha \leq 1$) is related to the angle of rotation of a purely capacitive line on the complex plane plots. The fitting model impedance is thus $Z = R/[1 + (j\omega\tau)^{\alpha}]$, where $\tau = (TR)^{1/\alpha}$. CPE has been considered to represent a circuit complex element with limiting behavior as a capacitor for $\alpha = 1$, a resistor for $\alpha = 0$ and an inductor for $\alpha = -1$. For the device under test α is about 0.95 which means that the CPE describes a system with an average behavior similar to a distributed capacitor or a transmission line network. Practically, this model describes, in a compact way, a network of RC elements connected together. [65] The RC network is thus representative of the various Si nanocrystals (the capacitors) and of the leakage current paths (the resistors). At low frequencies, a weak current flows through the resistor network via one or more percolation paths, which connect the various nanocrystals. Injection into the nc-Si looks like the charging of a capacitor. Indeed nc-Si are used as storage elements in memories. At high frequencies, charging and discharging of the capacitors, formed by separately charged nanocrystals, dominate the conductivity: in this regime high current can flow at the expenses of the bipolar injection into the silicon nanocrystals. This explains the decrease in the EL power efficiency while the injected current increases. Another way to look at this problem is to consider the active layer as a composite with phases of different conductivities which has an average conductivity which increases with frequency. This is because the space over which carriers move is determined by the frequency: the span is short at high

frequency while it is long at low frequency. Thus, at high frequency the charge carriers move in high conductivity regions, while at low frequencies charge transport is limited by bottlenecks of poorly conducting regions. On the considered range of frequencies, from 20 Hz to 1 MHz, the module of impedance decreases by three orders of magnitude with increasing frequency and the phase shift changes from 0° to 85° (Fig. 3.2.2 (b)). With these values the dissipated electrical power increases by about 70 times as a function of frequency (Fig. 3.2.2 (a)). It is also interesting to note that a pure RC model ($\alpha = 1$) cannot fit the data since it yields a constant power as a function of frequency.

Power Efficiency Estimation

During the impedance characterization the spectrally integrated (400–1000 nm) EL was measured too. Thus, with one single measurement, all the parameters to estimate the power efficiency in AC regime (V_{RMS}, I_{RMS}, α and P_{OPT}) are achievable. When $V_{RMS} = 3.66$ V and offset $= 3.5$ V, the EL increases by 1.6 times from the low frequencies value, quasi-DC regime, to the peak value, while I_{RMS} increases by three orders of magnitude. Since V_{RMS} was kept constant, the power efficiency decreases.
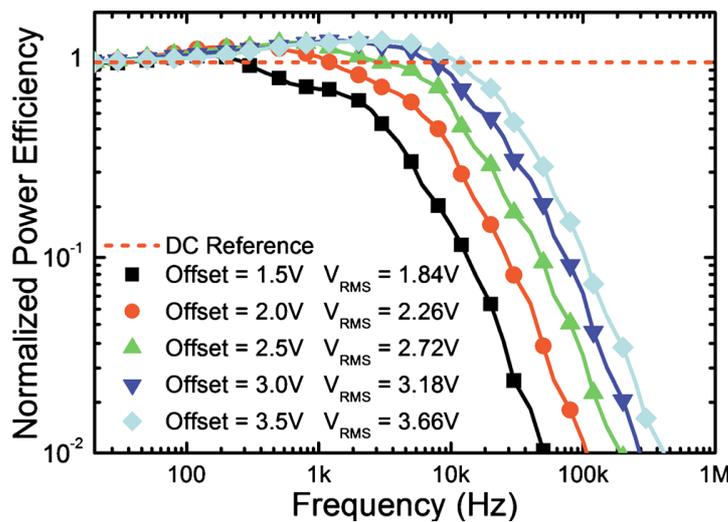

Figure 3.2.3: Normalized power efficiency as a function of frequency and different applied offsets; power efficiency level in DC at $V_{DC} = V_{RMS}$ (horizontal dashed line), the absolute DC power efficiency is 0.05%.

To define the starting point DC value, we set $V_{DC} = V_{RMS}$ and confirm that the EL intensity is the same for the two measurements.

Finally, Fig. 3.2.3 shows the power efficiency in DC (as a level) and in AC as a function of frequency for different offsets. The DC level is reached for quasi-DC regime. As the frequency increases, the power efficiency slightly increases and, then, dramatically decreases. In DC regime, charge transport is dominated by the tunneling among nc-Si and by the accumulation of charges at interface states at the contacts/active material interface. The charge accumulation screens the applied electric field and decreases the effective injection. When the LED is driven in AC, the mean amount of accumulated charges decreases and the injection becomes more efficient. In this case, the bias modulation enhances the efficiency. Figure 3.2.3 shows that at an offset equal to 3.5 V, the efficiency enhancement at 4 kHz is up to 50 % of the DC value, while the EL intensity increase, at the same offset, is about 160 % at 20 kHz (Fig. 3.2.1 (b)). Note that the EL is due to bipolar injection into the nc-Si, which means that the electron and hole have to be injected into the same nc-Si simultaneously. Low frequency means long distances that a carrier can cover, i.e., the probability that an electron encounters a hole into a nc-Si is large. For higher frequencies the efficiency decreases dramatically because the injected charges are constrained to move on short distances or in short dissipative paths. The encounter probability thus decreases and, in turn, the EL drops. It is thus evident that the efficiency in AC is governed by a competition between field screening, charge transport and dissipative processes. This occurs for frequencies where recombination is not lifetime limited.

This analysis suggests that, to increase the power efficiency, one has to keep the conductivity constant in a wide frequency range by working on the geometry (large area or smaller thickness) of the device and on the properties of the active material (large dielectric constant)

3.3. Physical Interpretation of the CPE Model

The Constant Phase Element (CPE) is a non-intuitive circuit element that was discovered (or *invented*) while looking at the response of real-world systems. In some systems the Nyquist plot (also called the Cole-Cole plot or Complex Impedance Plane plot) was expected to be a semicircle with the center on the x-axis. However, the observed plot was indeed the arc of a circle, but with the center some distance below the x-axis.

These depressed semicircles have been explained by a number of phenomena, depending on the nature of the system being investigated. However, the common thread among these explanations is that some property of the system is not homogeneous or that there is some distribution (dispersion) of the value of some physical properties of the system.

Mathematically, a CPE's impedance is given by:

$$\frac{1}{Z} = T(i\omega)^{\alpha}$$

where T has the numerical value of the admittance (1/ |Z|) at ω = 1 rad/s. The units of T are S·s$^{\alpha}$. A consequence of this simple equation is that the phase angle of the CPE impedance is independent of the frequency and has a value of $-90 \times \alpha$ degrees. This gives the CPE its name. When α = 1, this is the same equation as that for the impedance of a capacitor, where T = C. When α is close to 1, the CPE resembles a capacitor, but the phase angle is not 90°. It is constant and somewhat less than 90° at all frequencies.
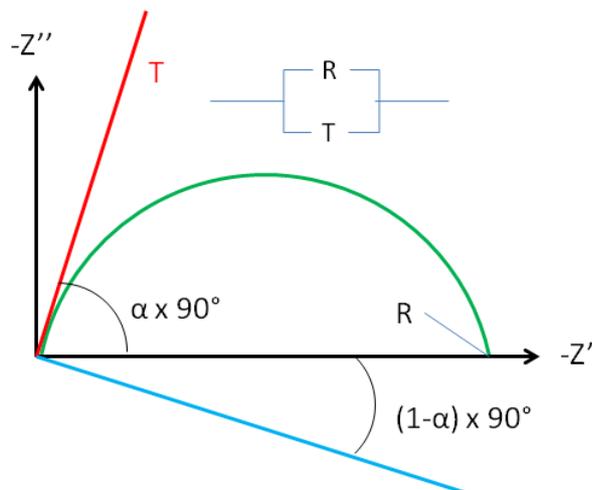
Figure 3.3.1: The Nyquist (Complex Impedance Plane) Plot of a CPE is a simple one. For a solitary CPE (symbolized here by T), it is just a straight line which makes an angle of (α x 90°) with the x-axis as shown in red. The plot for a resistor (symbolized by R) in parallel with a CPE is shown in blue. In this case the center of the semicircle is depressed by an angle of (1-α) x 90°.

What Does It Cause a CPE?

CPE could be originate by different mechanisms. In particular:

- **Surface Roughness**

One physical explanation put forth for CPE behavior is electrode roughness. For a rough, fractal, surface, the fractal dimension (D) of the surface is between 2 and 3: translated, this means that the surface fills between 2 dimensions (*i.e.*, it's absolutely flat) and 3 dimensions (*i.e.*, the surface fills three dimensions, branching every-which-way through space, and resembling a porous cube.) It has been shown [66] that for these electrodes, the interfacial impedance (electron transfer or double layer capacitance) is modified by an exponent, $n = 1/(D-1)$. For a smooth surface the fractal dimension (D) is 2.0 and $n = 1$: The impedance is unchanged. For a highly contorted surface (D = 3), and $n = 0.5$.

For many real metals or solid electrodes, the measured impedance in the double-layer region (no faradaic current) follows a power law, such as that for the CPE, with a value of α between 0.9 and 1.0. The phase angle of this "capacitance" is not 90°, but is given by (α x 90°). The observed angle is something between 80° (α = 0.89) and 90° (α = 1.0). When this "capacitance" is in

parallel with a charge-transfer resistance (R), the Nyquist plot is the arc of a circle, but with the center of the circle below the x-axis: It is the "depressed semi-circle" shown in Fig. 3.3.1.

- **A Distribution of Reaction Rates**

Another explanation is inhomogeneous reaction rates on a surface. This might be seen at the polycrystalline metal surfaces or carbon electrodes with a distribution of active sites (with varying activation energies) on the surface. A recent article [67] shows that for a glassy carbon electrode, the CPE exponent correlates with the fraction of exposed edge plane orientations, not with the fractal dimension of the surface.

- **Varying Thickness or Composition**

A third possible explanation may be a varying thickness or composition of a coating. For example, if the bulk conductivity of a coating changes with distance through the coating [68], then the resultant impedance spectrum can closely approximate that of a CPE.

- **Non-uniform Current Distribution**

At the 2004 EIS Symposium, Tribollet [69] presented a paper in which the impedance of the whole electrode was measured in the traditional way and the spectrum above 1 Hz was fit to a Randles Cell containing a CPE with an α-value of 0.91.

The local impedance was also measured by placing a sub-mm current probe a short distance over the electrode. The local impedance was measured as a function of the distance along the radius of the electrode. Near the center, the α-value for the CPE was 1.0, indicating a true capacitance. However, at the edge of the electrode, the α-value for the CPE was 0.83. We would expect the current density to be fairly homogeneous near the center of the electrode, and normal to the surface. Near the edge, the current density will certainly be perturbed by "edge effect". Current flow will also not be perfectly normal to the surface. Both effects are likely to change the α-value for the CPE.

Another publication "The RC time "constant" at a disk electrode" [70] discusses the same phenomenon, but from a slightly different perspective. Oldham showed that the local RC time

70

constant (uncompensated- or solution-resistance times double layer capacitance) varies from 0 to 2 RC over the disk.

Universality of ac conduction in disordered solids

Materials like glass or plastic have electrical properties remarkably in common. For example, with few exceptions the DC conductivity is Arrhenius temperature dependent. It is almost always possible to scale measurements of the frequency-dependent conductivity at different temperatures into one single master curve. Different solids have quite similar master curves. In particular, AC electronic and ionic conduction cannot be distinguished. The only common feature of the numerous different solids exhibiting this AC universality is their disorder. Below two models for AC conduction in disordered solids are presented, a macroscopic model and a microscopic model. These models have essentially just one ingredient: disorder. For both models the AC conductivity is independent of the details of the disorder when the local mobilities cover many orders of magnitude. For both models AC universality is caused by an underlying percolation conduction at extreme disorder. In modern condensed-matter physics the extreme disorder limit is not often considered. For AC conduction in disordered solids this limit leads to unusual non-power-law universalities. Similar universalities may very well occur elsewhere in "disordered" physics.

Solids are classified into metal and nonmetals. A metal has a large weakly temperature-dependent DC conductivity, a nonmetal has a much smaller DC conductivity which, however, increases strongly with increasing temperature. Only for disordered nonmetals AC conduction is different from DC observed far below phonon frequencies. As mentioned before, these solids have quite similar AC conductivities. Examples of solids with universal AC properties are ion conducting, amorphous semiconductors, polycrystalline semiconductors, electron conducting polymers, ion conducting polymers, transition metal oxides, metal cluster compounds, organic-inorganic composites, and doped single-crystal semiconductors at helium temperatures (where the disorder due to the random positions of the doping atoms becomes important). While ion conduction is a classical barrier crossing process, electron conduction in disordered solids usually

proceeds via quantum-mechanical tunneling between localized states (i.e., states with wave functions decaying exponentially in space).

Macroscopic model

Any solid consisting of phases with different conductivity has an overall conductivity which increases with frequency. This is because at high frequencies localized charge carrier motion makes it possible to take maximum advantage of well conducting regions, while at lower frequencies charge transport must extend over longer distances and is limited by bottlenecks of poorly conducting regions. This can be described with the circuit shown in Fig. 3.3.2. It is tempting to interpret the resistor currents as the free charge currents and the capacitor currents as the bound charge currents. This is not correct, however, because in that case according to Kirchhoff's current law there could be no charge accumulation at any node of the circuit, i.e., anywhere in the solid. So, the resistor currents are the free charge currents, this follows simply from the definition of the resistors as being proportional to the local free charge resistivity. The capacitor currents are less straightforward: the charge on any capacitor is the capacity times the potential drop across the capacitor. In a periodic field the current through the capacitor is the displacement current.
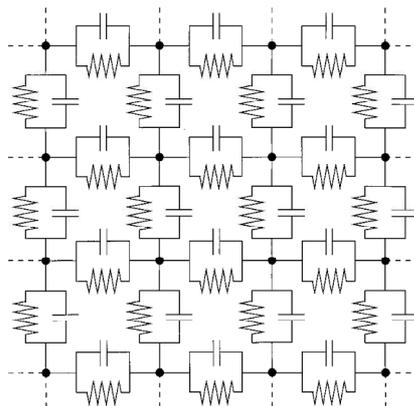

Figure 3.3.2: Electrical equivalent circuit fr a CPE. This circuit and its higher dimensional analog describe the macroscopic model. All capacitors are proportional to the bound charge dielectric constant while each resistor is proportional to the inverse free charge conductivity at the corresponding position in the solid. When the circuit is subjected to a potential difference applied to two opposing faces the electrostatic potentials at the nodes are found by solving Kirchhoff's equations.

To extract the overall AC conductivity from the circuit one imagines a periodic potential applied across two opposing faces acting as electrodes. The average resistor current determines the free charge AC conductivity.

Symmetric hoping model

The macroscopic model does not apply for solids that are strongly disordered on the atomic scale. We now consider a model with microscopic disorder. While the macroscopic model via Gauss's law includes all Coulomb interactions, to keep things simple these interactions are ignored in the model. We call it the hoping model. The term hopping refers to sudden displacement of a charge carrier from one position to another close. We shall only consider the simplest hopping model. This model has non interacting charge carriers placed on a cubic lattice with only nearest neighbor jumps allowed. The jump rates (jump probabilities per unit time) are assumed symmetric, i.e., they are the same for jumps forwards or backwards between two sites. The more general asymmetric hopping model has been applied to study, e.g., protein dynamics or viscous liquid flow.
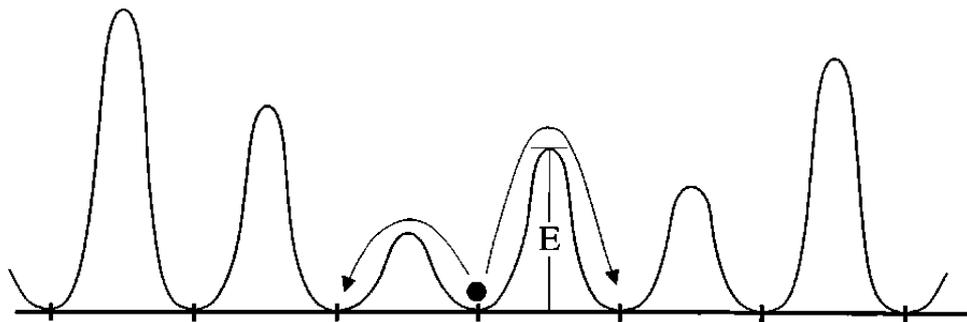

Figure 3.3.3: Typical potential for a system described by the symmetric hopping model (random barrier model) in one dimension. The arrows indicate the two possible jumps for the charge carrier shown. The term "symmetric" refers to the fact that the jump rate is the same for jumps forwards and backwards across a given barrier. The symmetric hopping model corresponds to the discrete version of motion in this potential, where non interacting charge carriers reside on a lattice defined by the minima.

Figure 3.3.3 gives a one-dimensional example of the kind of potential leading to the symmetric hopping model (also referred to as the random barrier model). The symmetric hopping

model may seem completely unrealistic for the following three reasons: (i) it ignores that charge carriers repel each other; (ii) it allows an arbitrary number of charge carriers at each site, but whether the charge carriers are ions or localized electrons there is room for just one at each site; (iii) it does not allow site energies to vary. A more realistic model has randomly varying site energies with room for just one charge carrier at each site. Surprisingly, when this "Fermi model" is linearized with respect to an external electric field, the resulting equations are the same as those of the symmetric hopping model. This traditionally serves as the justification of the symmetric hopping model. [71] The linearization, however, involves the nontrivial assumption that the occupation number (0 or 1) may be replaced by a continuous variable. Although the connection to the "Fermi" model is not rigorous, it is believed that in the extreme disorder limit it is likely that these two models have identical universal AC conductivities. Because the charge carriers by assumption are non interacting it is enough to consider the motion of just one of them.

3.4. CPE Based Model for General Electrical Driving

The CPE based model presented in the previous sections is a very powerful and compact tool to fit and to explain the experimental data in the alternated current regime when the bias is a sinusoidal waveform. Looking at the IV characteristics (Fig 3.4.2) of a device, it is very non linear, so the previous CPE model is a linearization of the true model. With the linear model it is not possible to fit the IV characteristics, i.e. direct current regime, and a generalization for other possible driving waveforms applied has to be performed. In Fig. 3.4.1 is shown the full model based on the CPE. The resistor is replaced by a pair of "diodes" in series. The device is a silicon pin junction with the SRO multilayer as the i layer. In this case, the top diode of the model is a real diode and represents the pn junction of the device:

$$I = I_S \left[exp \left(\frac{V}{nV_T} \right) - 1 \right]$$

Equation 3.4.1: Diode equation.

I_S is the reverse bias saturation current, n the ideality factor and V_T the thermal voltage.

The second diode is a multi-barrier tunnel diode. The tunneling is through the silicon oxide barriers between the silicon nanocrystals. The analytical equation for the tunneling through a general barrier was given by J.G. Simmons. [72] G. Michael *et al.* [73] generalized the Simmons's equation for a multilayer stacks. The current through a multilayer structure is given by:

$$I = I_{forward} - I_{backward}$$

$$I_{forward} = I_0 \frac{(qV)^2}{4} \left\{ \sum_i \varepsilon_i \sqrt{m_i^*} \sqrt{(\emptyset_i - eV_i)} - \sqrt{(\emptyset_i - eV_{i+1})} \right\}^{-2}$$

$$\times exp\left\{ -\frac{2A}{3qV} \sum_i \varepsilon_i \sqrt{m_i^*} \left[\sqrt{(\emptyset_i - eV_i)^3} - \sqrt{(\emptyset_i - eV_{i+1})^3} \right] \right\}$$

$$I_{backward} = I_0 \frac{(qV)^2}{4} \left\{ \sum_i \varepsilon_i \sqrt{m_i^*} \sqrt{(\emptyset_i + eV - eV_i)} - \sqrt{(\emptyset_i + eV - eV_{i+1})} \right\}^{-2}$$

$$\times exp\left\{ -\frac{2A}{3qV} \sum_i \varepsilon_i \sqrt{m_i^*} \left[\sqrt{(\emptyset_i + eV - eV_i)^3} - \sqrt{(\emptyset_i + eV - eV_{i+1})^3} \right] \right\}$$

Equation 3.4.2: Tunnel equation.

$I_{forward}$ is the current that flows from one electrode to the other and $I_{backward}$ the current that flows in the opposite direction. I_0 and A are constants, q the electron charge, ε_i the dielectric constant for each barrier, Φ_i the effective barrier high, V_i the voltage drop, m_i^* the effective barrier mass, and i is the number of barriers.
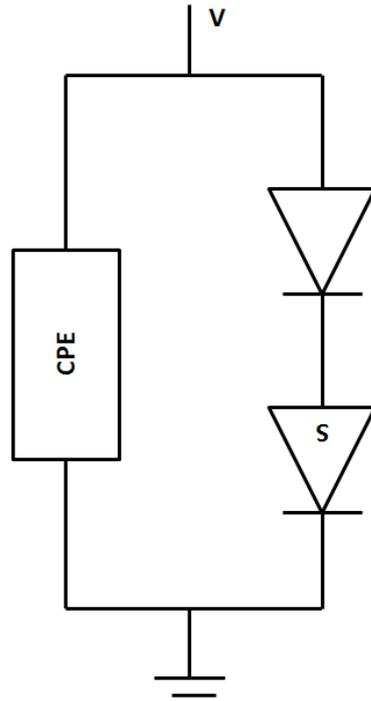
The CPE element gives some contribute only in alternate current regime. Figure 3.4.2 shows the IV characteristics of a device and a fit done by using the full model of Fig. 3.4.1.
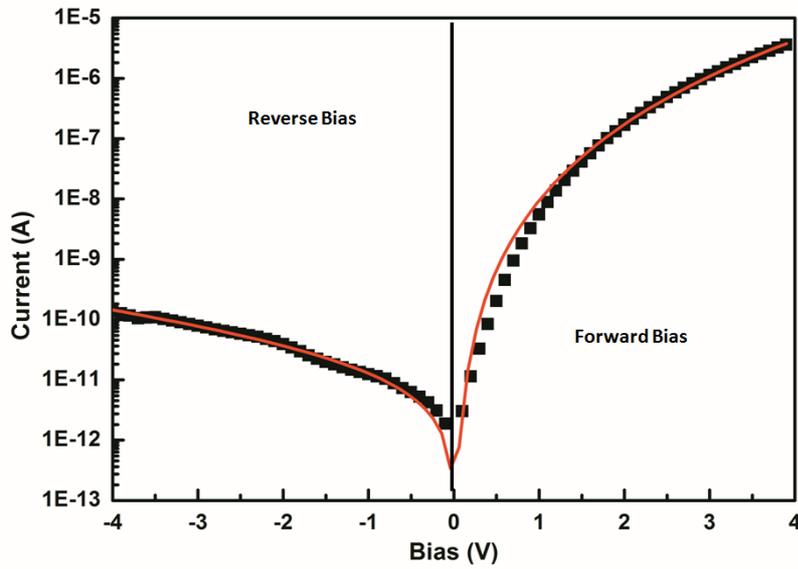
The two diodes limit the conduction in two different polarization. In forward bias the current is limited by the tunneling through the nanocrystals while in reverse bias the current is limited by the saturation current of the pn diode.

The expression for the current in DC is expressed by a complicate equation but it have the advantage to be an analytical expression, so all the further calculation can be treated formally. With the full model it is possible to calculate the RMS value and it is also possible to draw the current and voltage temporal evolution. In Fig. 3.4.3 the temporal evolution of a sinusoidal bias applying and the resulting current (the CPE is not taken in to account yet) are shown.
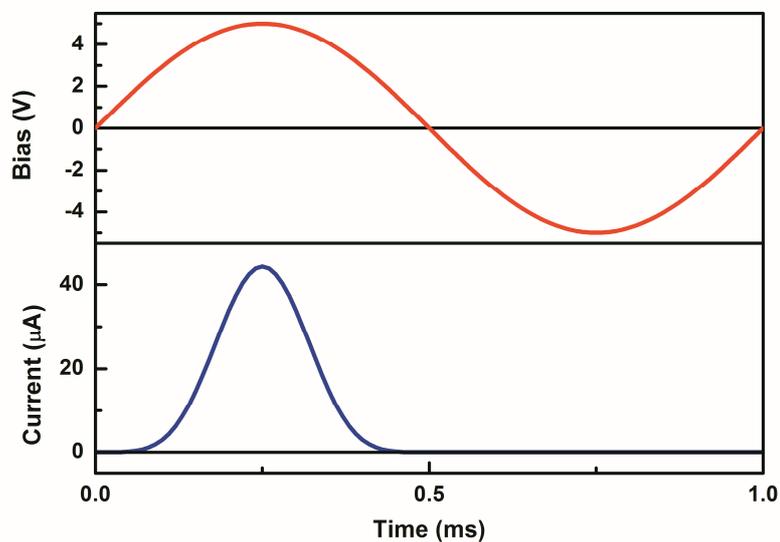

Fig 3.4.3: Bias and resulting current as a function of time for a applied waveform with V_{offset}=0V, V_{pk}=5V and frequency=1kHz.

The RMS values of voltage, current and electrical power can be calculated analytically:

$$V_{RMS} = \sqrt{\frac{1}{T} \int_0^T V^2(t)dt}$$

$$I_{RMS} = \sqrt{\frac{1}{T} \int_0^T I^2(t)dt}$$

$$P_{RMS} = \sqrt{\frac{1}{T} \int_0^T V(t)I(t)dt}$$

Equation 3.4.3, 3.4.4 and 3.4.5

Adding a capacitor in parallel to the diodes (instead of the CPE) the total current is the sum of the current from the diodes plus the current from the capacitor, which is simply:

$$I_{cap} = C\frac{d}{dt}V(t)$$

Equation 4.3.6

Figure 3.4.4 shows the temporal evolution of a sinusoidal bias and the resulting current. Comparing the current with that in Fig. 3.4.3 the effect of the capacitor current is visible.
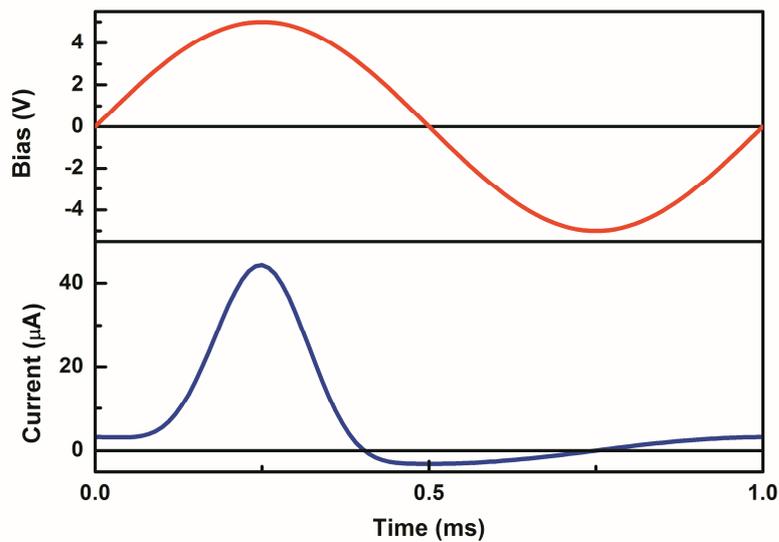

Fig 3.4.4: Bias and resulting current as a function of time for a waveform applied with V_{offset}=0V, V_{pk}=5V and frequency=1kHz (Diodes + Capacitor).

From the point of view of the RMS values the V_{RMS} is constant because it is defined by the applied waveform, the I_{RMS} increases as a function of the frequency due to the increase of the capacitor current, while the P_{RMS} value is constant. An ideal capacitor is a non dissipative device, so only the displacement current increases, but there is not higher dissipation as a function of frequency. In other word, the electrical power is constant as a function of frequency because the increase in current is compensate by the phase shift with the bias. I_{RMS} and P_{RMS} as a function of frequency are shown in Fig. 3.4.5.
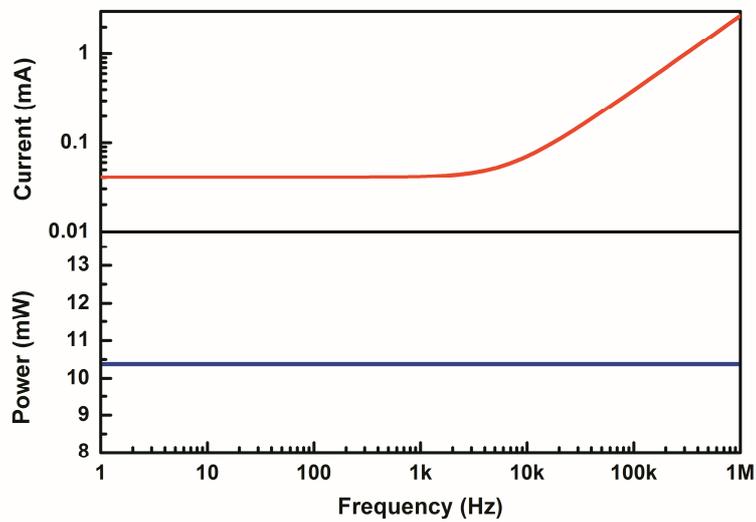

Figure 3.4.5: RMS values of current and electrical power as a function of frequency for a full model with a capacitor applied. The dissipated power is constant because the increase in current is compensated by the phase shift with the bias.

When CPE is in parallel to the diodes the total current is still the sum of the current from the diodes plus the current from the CPE but the CPE current is calculated as:

$$I_{CPE} = C \frac{d^{\alpha}}{dt^{\alpha}} V(t)$$

Equation 3.4.7

which is the α-derivative of the applied bias. As shown in section 4.2 α is a parameter that can assume all the real value between -1 and 1. This means that the related derivative is a fractional one. The ways to solve a fractional derivative are many and they are applied in different fields.

Dalir [74] lists different definitions for the fractional derivative and various applications. For periodic signals, i.e. waveforms, the best way to calculate the fractional derivative is to use the Fourier's definition:

$$\frac{d^\alpha}{dt^\alpha} f(t) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} g(k)(-ik)^\alpha e^{-ikt} dk$$

where

$$g(k) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} f(t)e^{-ikt} dk$$

Equation 3.4.8

For sinusoidal waveform it is particularly simple to perform the α-derivative because it adds only a phase factor of $\alpha \frac{\pi}{2}$ to the original function:

$$\frac{d^\alpha}{dt^\alpha} sin(t) = sin\left(t + \alpha \frac{\pi}{2}\right)$$

Equation 3.4.9

In this case, as a function of the frequency, the current is no more compensated by the phase factor and the electrical power becomes function of the frequency as shown in Fig. 3.4.6.
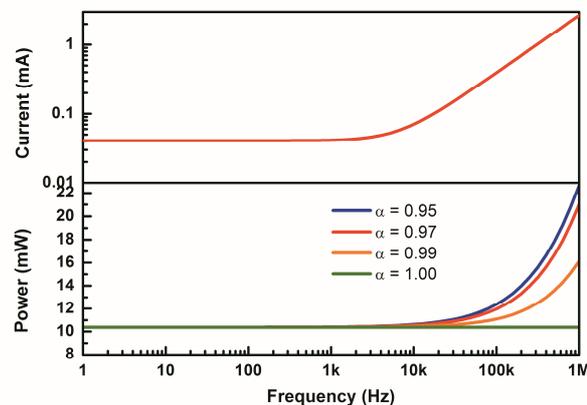

Figure 3.4.6: RMS values of current and electrical power as a function of frequency for a full model with a CPE applied. The dissipated power is not constant because the increase in current is not compensated by the phase shift with the bias.

The Fourier's definition is particularly useful in order to generalize the model to other bias waveforms. In fact, any waveforms can be written by the Fourier's expansion as the sum of sinusoidal waveforms. The fractional derivative is, then, the sum of sinusoidal waveforms with a phase factor of $\alpha \frac{\pi}{2}$. As a limit, Equation 3.4.10, shows V(t) and I(t) in Fourier's expansion for a square waveform:

$$V(t) = \sum_{z=1}^{\infty} \frac{1}{2z-1} \sin((2z-1)t)$$

$$I(t) = \sum_{z=1}^{\infty} (2z-1)^\alpha \sin\left((2z-1)t + \alpha \frac{\pi}{2}\right)$$

Equation 3.4.10

In conclusion a full model based on the CPE was derived in order to fit the I-V characteristics in DC regime and to estimate the values of voltage, current and electrical power in AC regime for any kind of bias waveforms.

3.5. Time Resolved Electroluminescence and Carrier Injection

3.5.1. Time-resolved and pulsed-current electroluminescence

The device structure is a metal-oxide-semiconductor (MOS) capacitor. Alternating layers of stoichiometric SiO_2 and silicon rich silicon oxide (SRO) with a large Si excess were grown by plasma-enhanced chemical vapor deposition (PECVD)[6]. These are used as the gate oxide in the MOS. The SRO layer within the ML structure has the following composition: 52 at. % of silicon, 44 at. % of oxygen, and 4 at. % of nitrogen, which has been measured by x-ray photoelectron spectroscopy. The pair of SiO_2 and SRO layers forms the ML period. Here are detail, in particular, two devices: the thicknesses of the SRO layer within the ML period were 3 nm for the W9 device and 4 nm for the W10 device. The thickness of the oxide layer was 2 nm in both

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[6] Fabbricate at FBK

devices. This layer thickness is a nominal value based on a previous careful characterization of the deposition rates. The number of ML periods is 5. The gate is formed by 100 nm thick n-type in situ doped polycrystalline silicon (poly-Si), while 500 nm thick Al (1 % Si) is used to connect the gate area of 7.94×10^{-8} m^2 with the bonding pad. The poly-Si is covered by an antireflective coating formed by a 50 nm thick Si$_3$N$_4$ layer and a 120 nm thick SiO$_2$ layer to improve light extraction. Wet oxidation was performed at 1150 °C for 30 min to grow both a 480 nm thick field oxide (for active area isolation) and the Si nanocrystals in the gate dielectric. The total thickness of the ML was 27 nm (32 nm, depending on the thickness of the SRO), which was controlled by both profilometry and variable angle spectroscopic ellipsometry. The substrate was p-type (100) Si with 12–18 Ω cm resistivity. The device layout is shown in the previous section 2.2.2.

Characterization Techniques

The EL signal was collected with a single photon-counting module SPCM-AQR. The total light emission intensity (counts/s) was integrated over the whole visible spectrum. A function generator, Tektronix AFG 3252, was used to drive the device under alternating current (AC) or pulsed-current injection scheme. Time-resolved EL signal was recorded with a multichannel scaler SR430. The measurements were performed at room temperature in a dark room.

Opto-Electrical Characterizations

When the direct current (DC) voltage is swept abruptly from positive-to-negative value and vice versa the EL of the nc-Si MOS-LED shows a peak. This was predicted theoretically in Ref. (75) and demonstrated experimentally in Ref. (23). In the former work, bipolar charge injection into nc-Si is studied by Monte Carlo simulations. A perturbation of the static electric field was induced by a larger electric field. This perturbation increases the e-h density in the nc-Si and gives rise to an enhanced EL emission. Alternatively a field-effect EL model was developed in Ref. (23) based on an alternate polarity charge injection from the silicon substrate into the nc-Si which was followed by exciton formation and recombination in the nanocrystals. Both electrons

and holes are injected from the silicon substrate into the nc-Si through Fowler-Nordheim tunneling. The injection is not simultaneous and charge leakage brings about an asymmetry in the EL peak intensities at different bias transitions. These proposed effects are explored here by applying a square waveform signal to the gate of our LED. Figure 3.6.1.1 shows the peak EL emission at both negative-to-positive and positive to- negative bias transitions for the W9 device. It also shows the EL peak decay during the period of constant bias with a root-mean-square (RMS) value of 4 V. Figure 3.6.1.1. (a) shows EL peak and decay after forward-to-reverse bias transition while Fig. 3.6.1.1. (b) shows the EL peak and decay after reverse-to-forward bias transition. The time axis is given in unit less values, t /T, where T is the period of the driving square-form voltage signal. The following reasoning might explain the peak EL emission at the bias transitions. Under a constant bias, the holes accumulate at the anode side of the oxide layer containing the nc-Si and the electrons at the cathode side. [75] [76] At the bias transitions these charge populations will exchange positions moving toward each other and bringing the peak of EL emission.
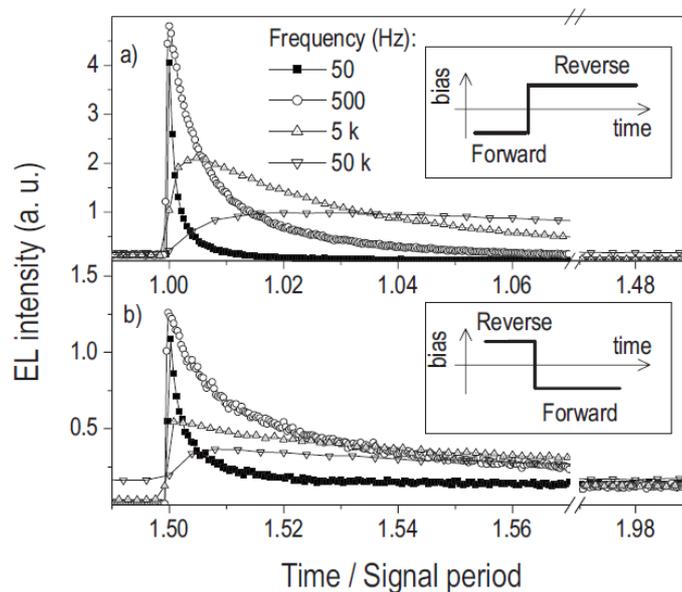

Figure 3.6.1.1: Time-resolved EL signal in device with 2 nm SiO_2/3 nm SRO. The driving gate signal is a square waveform with the RMS voltage value of 4 V. (a) EL emission decay at the bias transition from forward to reverse, which is sketched in the inset; (b) EL decay at the bias transition from reverse to forward. The driving gate frequency value is shown in the figure legend.

The amplitude of the EL peaks is about four times larger for the forward-to-reverse bias transition than for the reverse-to-forward one. This asymmetry might be explained by the difference in electron and hole injection efficiencies from the n-type polysilicon gate and p-type Si substrate. [23] Under forward bias, holes accumulate in the gate oxide in a greater amount than under reverse bias, because hole injection takes place from the accumulation layer in Si substrate. There is a constant EL signal under the forward bias to which the EL peak emission decays after reverse-to-forward bias transition. This constant EL signal under the forward bias is the direct current EL emission. Figure 3.6.1.1 shows the EL peak decay for several driving frequencies. The peak EL emission decreases when the driving frequency increases for both transitions. This is due to the decrease in the time available for storing charges in the nc-Si layers with increasing frequency. The EL decay could be fitted by a stretched exponential decay equation:

$$I(t) = I(0) \exp\left[-\left(\frac{t}{<\tau>}\right)^{\beta}\right]$$

Equation 3.6.1.1:

where $<\tau>$ is an effective recombination lifetime (named EL decay time) and the exponent β accounts for deviation from the single exponential decay curves ($\beta = 1$). The stretched exponential decay is related to the energy transfer relaxation processes among nanocrystals with different dimensions in a dense ensemble. Figure 3.6.1.2 shows the EL decay parameters as a function of the driving frequency for the same device in Fig. 3.6.1.1. Figure 3.6.1.2 (a) shows the dependence of the EL decay time for both bias transitions. The EL decay time is larger for the reverse-to-forward bias transitions than for the forward-to-reverse transitions and both decay times decrease when frequency increases. This is because when the driving frequency increases, the injected electrical power increases too. The decrease in EL decay time of Si p-i-n diode after application of a reverse bias potential was observed in Refs. (77) and (78) and attributed to the change in the width of the space-charge region. [78] Although no dependence on the current pulse amplitude was observed in these works, a small decrease in the EL decay time with increasing the density of the extra peak current under a pulsed excitation was reported in Ref. (62). Figure 3.6.1.2 (b) shows

the frequency dependence of the stretched exponent. The difference in the exponent values and the effective decay time corresponding to the two bias transitions might be attributed to the difference in the mobility of electrons and holes that migrate among the nanocrystal in ML ensemble. Electrons have larger mobility than holes and, hence, shorter times and larger exponent value.
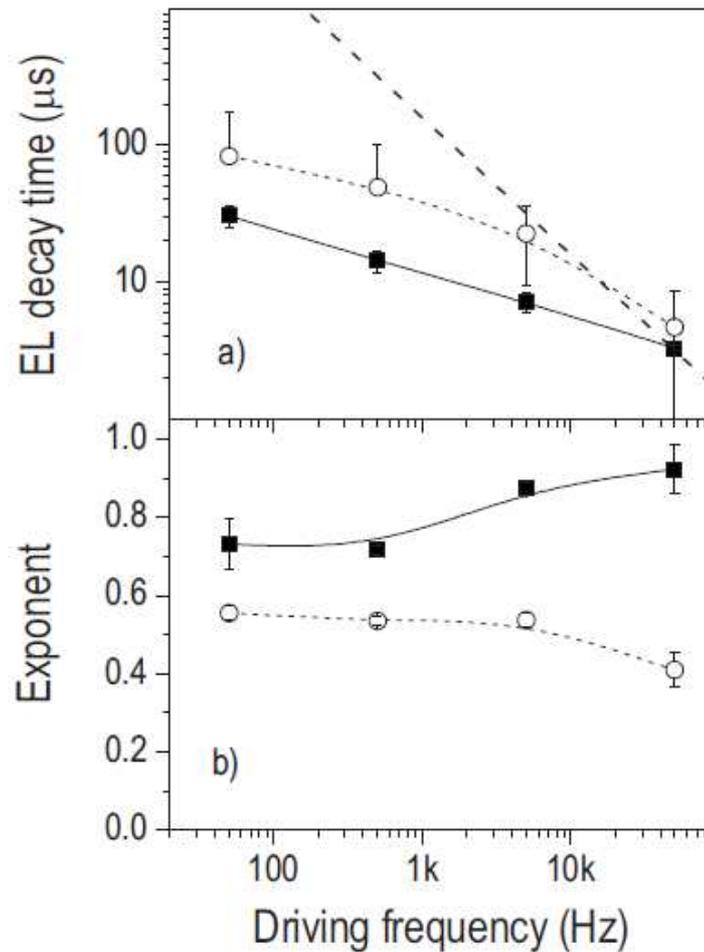

Figure 3.6.1.2: Parameters of the time-resolved EL signals (Fig. 3.6.1.1) obtained from a fit against the stretched exponential function. Solid symbols correspond to the bias transition from forward to reverse (Fig. 3.6.1.1 (a)); open symbols correspond to the bias transition from reverse to forward (Fig. 3.6.1.1 (b)).

The total integrated EL emission as a function of the driving gate frequency is shown in Fig. 3.6.1.3. Figure 3.6.1.3 shows the EL signal integrated over a 30 s period by a CCD camera. At low frequency, the EL emission is the same as under dc bias. When the driving frequency increases, the number of bias transitions in 30 s increases too. Although the peak EL emission at

the bias transition decreases when the frequency increases, the EL signal collected in the 30 s period will increase. It peaks at a value of 50 kHz because the mean radiative lifetime becomes equal to the driving gate frequency at this value (the dashed line in Fig. 3.6.1.2 a). The EL emission under such a pulsed excitation scheme is larger than for dc by a factor of 4 at the peak (optimal) gate driving frequency. A stronger emission is present up to a gate modulation frequency of 1 MHz. A full modulation of the EL signal exists until the frequency reaches its optimal value of 50 kHz (Fig. 3.6.1.1). The full modulation means that EL emission peaks at the bias transition, decays exponentially, and reaches a steady-state value at longer times. At higher frequency the EL modulation is partial, i.e., the steady-state value is not reached.
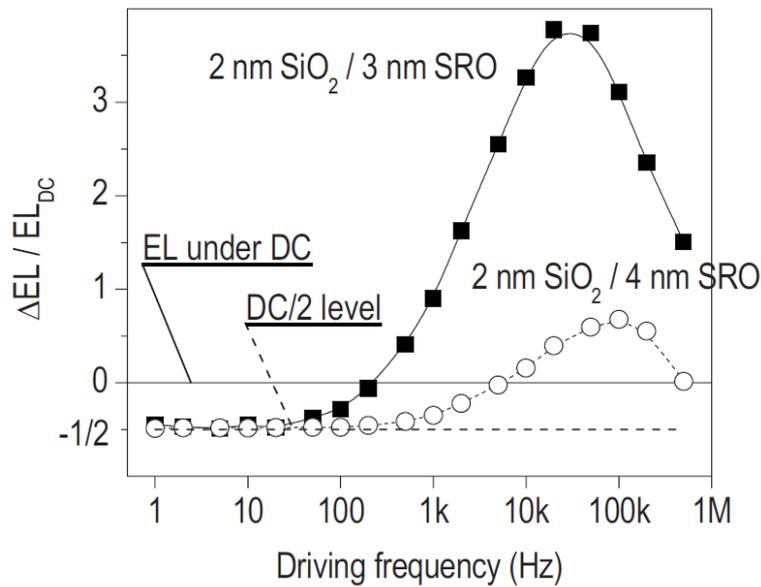

Figure 3.6.1.3: The increase in total EL emission under AC injection over the EL emission under <u>DC</u> (at the forward voltage of 4 V). The total EL intensity was collected with a CCD camera for the period of 30 s. The AC driving signal is a square waveform with the RMS voltage value of 4 V. Solid symbols: device with 2 nm SiO$_2$/3 nm SRO; open symbols: device with 2 nm SiO$_2$/4 nm SRO.

Estimation of the power efficiency under pulsed voltage excitation is a difficult task. It requires knowledge of the load impedance, which could not be measured under the pulsed excitation waveform we used. Besides, the measurement is impeded by parasitic capacitances and resistances of the electrical circuit. Charging currents show very sharp and intense peaks at the bias transitions which decay at the nanosecond timescale. [79] The field-effect EL power efficiency

of similar devices was estimated in Ref. (80) based on the electrical power provided by the voltage source. The value is 0.1%–1%. [80] Our estimate of the power efficiency shows that power efficiency decreases with the driving frequency and it is about four times smaller at 50 kHz than the value at dc. Our estimate is based on the frequency dependence of measured RMS value of AC current through the device.
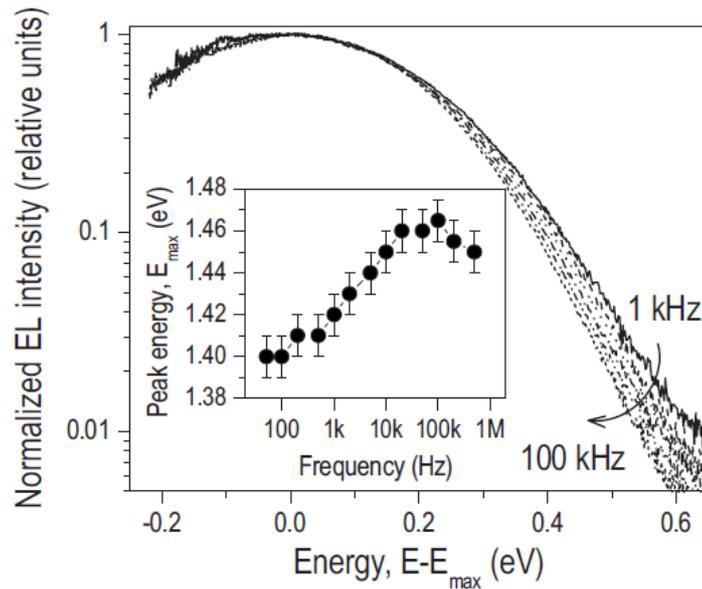

Figure 3.6.1.4: Normalized EL spectra collected at different AC driving voltage frequencies for the device with 2 nm SiO$_2$/3 nm SRO. The frequencies are (from the top to the bottom, in kHz): 1, 2, 5, 10, 20, and 100. The driving gate signal is a square waveform with the RMS voltage value of 4 V. The inset shows the EL spectrum peak energy as a function of driving frequency.

EL spectra collected at different frequencies are shown in Fig. 3.6.1.4. The spectra are normalized to the peak intensity and peak energy. The peak energy dependence on the driving frequency is shown in the inset. This dependence is consistent with the dependence of the total EL emission shown in Fig. 3.6.1.3. The EL peak energy shifts to higher energies and has a maximum at about 50 kHz, the optimal frequency of EL emission. This blue-shift is connected to the decrease in the EL decay lifetime shown in Fig. 3.6.1.2. As it was shown in Ref. (81), EL emission at shorter wavelengths peaks at larger driving frequencies than emission at longer wavelengths. Therefore, charge injection into small nanocrystals _more efficient _ occurs faster than injection into large nanocrystals. [81] When the gate modulation frequency increases, the EL

peak wavelength blueshifts and the effective EL decay time decreases. Variation in the optimal driving frequency at different emission wavelengths was studied in Ref. (81) and used later on to build a white light LED. [82] Very recently an alternative explanation for the field effect EL was suggested by Carreras et al. [82] The authors developed a multitunnel-junction model to simulate charge transport in nc-Si MOS field-effect transistor structures and field-effect EL using a simple rate equation. Showing good agreement with their model, the authors stated that impact excitation of the nanocrystals by electrons and holes injected from the same silicon substrate is the origin of the field effect EL. A large difference in the tunneling times of electrons and holes is the main argument of their work. The tunneling times were calculated within the Wentzel– Kramers– Brillouin approximation. However, tunneling time dependence on bias voltage has a more complex serrated shape, 25 and so this argument should be taken with some precaution.

Conclusions

Time-resolved EL experiments were performed by driving the LED with a square waveform voltage. Under such a pulsed excitation, an enhanced EL emission is observed at the gate bias transitions, which decays in the time scale of a few tens of microseconds. The EL emission is enhanced by a factor of 4 at the driving frequency of 50 kHz. This could be of interest for the applications in which LED is driven with an AC.

4. Erbium Doped Silicon Nanocrystal Based Devices

4.1. Introduction

In this chapter, erbium implanted silicon rich oxide based devices are presented. The investigation of opto-electrical properties of LED in direct current and alternate current regime are studied in order to understand the injection mechanism and estimate the energy transfer between silicon nanocrystals and erbium. At the end a device layout and process flow for an erbium doped silicon nanocrystal based laser structure are shown.

4.2. Erbium doped Light Emitting Devices: Role of Silicon Content

A multilayer approach in the growth of the nc-Si composite material allows the independent control of nanocrystals size and density. After a high-temperature annealing, the thickness of the SRO layer in the multilayer structure determines the nanocrystals size, while the excess silicon content of the SRO layer determines the nanocrystal density. In addition, a tight control over the silicon oxide layer quality and thickness which separates silicon nanocrystals in the multilayer structure is possible. These features are enough to create an easy recipe in order to engineer the band gap energy of nc-Si via thickness/composition profiling of a multilayer SRO/SiO$_2$ structure. Comparison between light emitting diodes based on single and multi-layer structures, with different silicon content, in terms of light emitting power efficiency of erbium ions is presented.

Sample Description

The device structure is a MOS capacitor with alternating stoichiometric SiO$_2$ and silicon-rich oxide (SRO) laser. In addition, all the samples were implanted with Er^{3+} ions (Fig. 4.2.1).
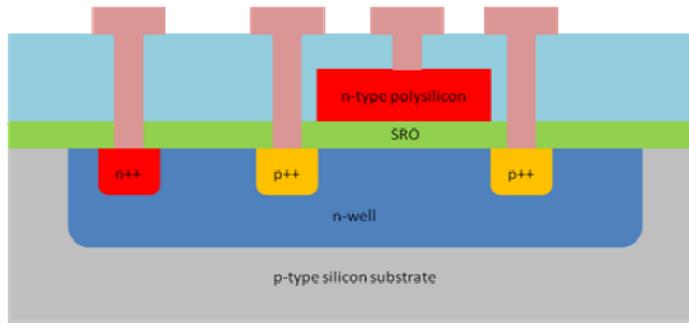
Figure 4.2.1: Device description: the cross-section is a MOS capacitor in which the gate oxide is replaced by Er^{3+} ions sensitized silicon-rich oxide.

The samples[7] were grown by LPCVD. The silicon nanocrystals were formed by annealing the layers at 900 °C for 1 hour in a nitrogen atmosphere. The erbium ion concentration was around 4×10^{20} cm^{-3}, obtained by Er^{3+} implantation with a fluence of 10^{15} ions/cm^2 and energy equal to 20 keV. Post implantation annealing was performed at 800 °C for 6 hours. The basic geometry of the device is a 300 μm x 300 μm square with n-type polysilicon gate. The devices presented in this work are summarized in Table 4.2.1.

Device	Structure	SRO	Si Excess (%)
P1	Multilayer	LPCVD (2nm 0% + 3nm 20%)x10	11.5
P2	Multilayer	LPCVD (2nm 0% + 3nm 20%)x10	14.4
P3	Multilayer	LPCVD (2nm 0% + 3nm 20%)x10	16
P4	Single Layer	LPCVD 50nm	12

Table 4.2.1: Summary of the devices under study

Samples P1, P2 and P3 have as active layer a multilayer structure, formed by an alternance of SRO and of silicon oxide layers. The three devices chosen for this work only differ in silicon content and are used to evaluate the effect of the silicon excess on the power efficiency of the devices. Sample P4 is a single layer device, with a thickness of 50 nm and silicon excess equal to

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[7] Projected by Gianfranco Dallabetta UNITN

12%. This latter was selected in order to compare single thick layer with multilayer devices, while the silicon content excess is constant.

Results and Discussions

The light emitting diodes under study have low silicon excess and hence low conductivity, which means high operating voltages. In direct current (DC) regime, the Er^{3+} ions are excited by impact excitation, as high energy transitions of erbium were clearly observed in the visible region of the spectra. Figure 4.2.2 shows the integrated electroluminescence intensity of the peak at 1.54 μm as a function both of the injected current and of the applied voltage. It is reported for P1, which is the best multilayer sample under study, and P4, in order to do a comparison between the single and the multilayer light emitting devices. Both P1 and P4 active materials have the same thicknesses (50 nm) and about the same average silicon excess. We found larger voltages for the multilayered device. This is due to the different distribution of nanocrystals inside the active layer, providing higher injection energy barriers for multilayered devices compared with the single ones. However, both devices show very similar EL intensities.
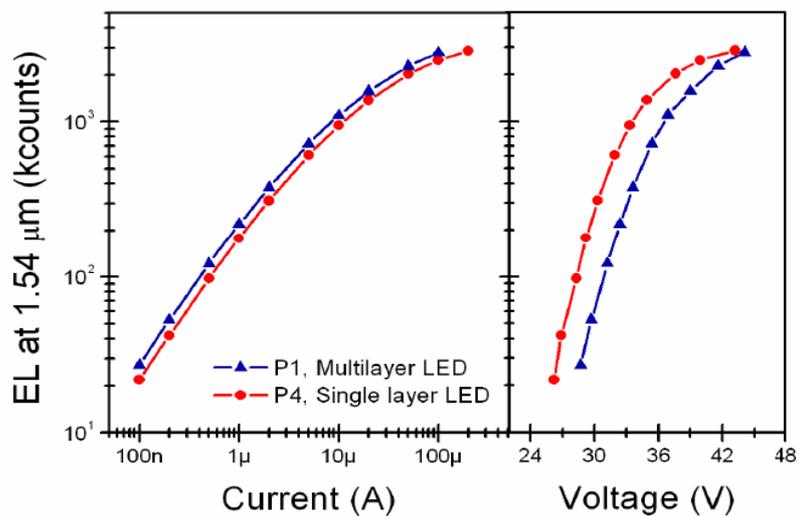

Figure 4.2.2: Electroluminescence behavior vs. injected current and applied voltage for a multilayer (blue) and a single layer (red) light emitting diode.

Starting from this, the power efficiency in the infrared was evaluated and Figure 4.2.3 shows it as a function of the injected current. In the figure, only P1 and P4 are reported. The most

important result is that the multilayers have allowed increasing the power efficiency of the devices by about 1.5 times with respect to the single layer device. The maximum value of power efficiency achieved is 1.5×10^{-2} %, referred to P1 at an injected current equal to 100 nA.
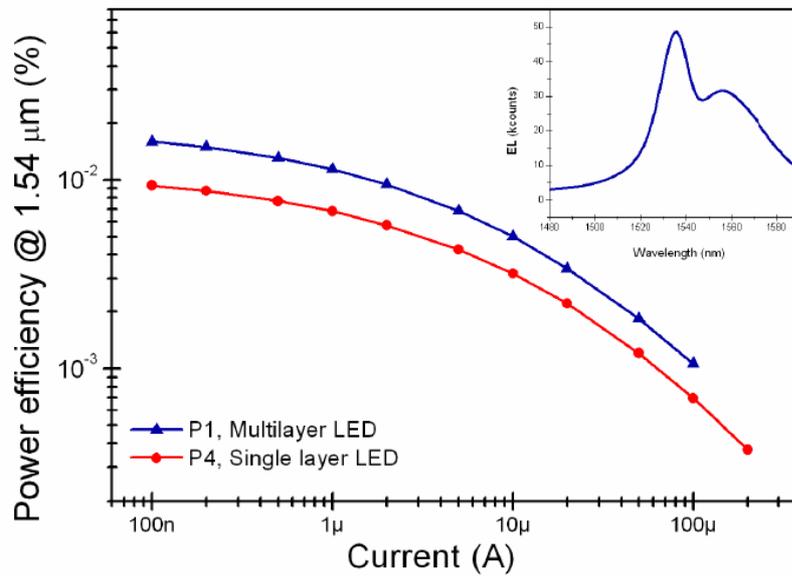

Figure 4.2.3: Power efficiency as a function of the injected current for a multilayer (blue) and a single layer (red) light emitting diode. In the inset, an example of the EL spectrum for P1 is shown (injected current of 50 µA).

Figure 4.2.4 shows the external quantum efficiency (E.Q.E.) as a function of the injected current for multilayer LEDs with different thicknesses of oxide and SRO, different concentration of silicon nanocrystals and different silicon content excess.
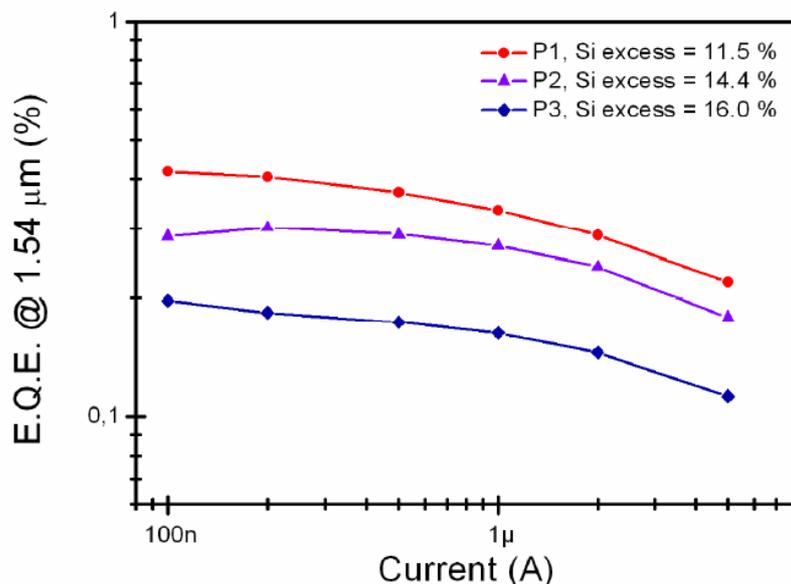
Figure 4.2.4: External quantum efficiency as a function of the injected current for P1, P2 and P3, multilayers with different average content of Si excess.

The maximum value of E.Q.E. is achievable with P1, and it is equal to 0.4%. This value is once again higher than the one achieved with the single layer light emitting diode. The best result was obtained on the multilayer with lowest silicon excess and this suggests that more studies need to be performed on the role of the silicon excess in the multilayered devices.

Figure 4.2.5 shows the infrared electroluminescence intensity as a function of the silicon excess in different multilayer devices, with silicon excess in the range between 9 and 16 %. Extrapolating the EL intensity dependence on silicon excess (Figure 4.2.5) to zero value gives an higher value of the EQE than the one measured in the Er^{3+}-doped LPCVD and thermal silicon oxide. The same value of EQE is reached at about 6% of silicon excess. This figure also shows (right axis, red symbols) that lower operating voltages are achievable with higher silicon excess and/or thinner silicon oxide scaffold that confines nc-Si. These LEDs operate at voltages below 5 V and emit at around 850 nm.
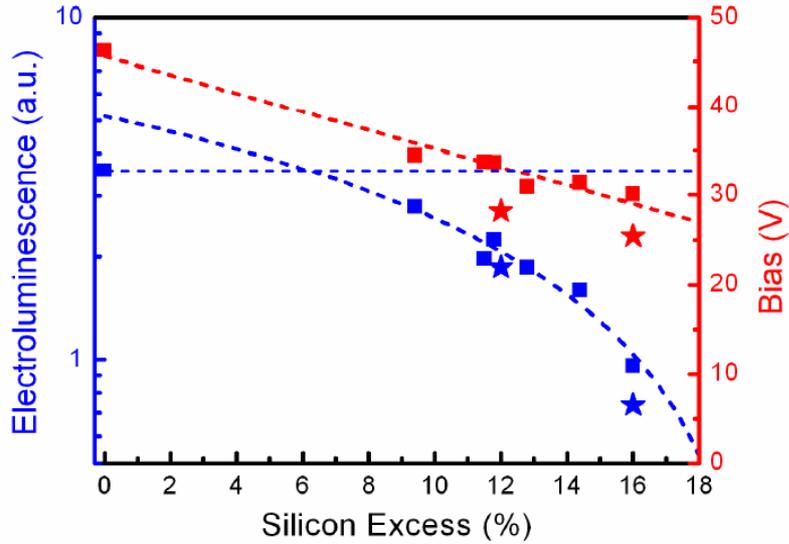
Figure 4.2.5: Electroluminescence intensity at 1.54 µm (left axis, blue symbols) at a fixed injected current of 1 µA as a function of average content of silicon excess for a series of multilayer LEDs (squares) and single layer LEDs (stars) and corresponding driving voltages (right axis, red symbols).

The electroluminescence behavior as a function of the silicon content confirms that, increasing the silicon excess, the IR emission decreases. Anyway, from this plot, it is observed that for the same silicon content the multilayer devices show higher power efficiency than the single layer ones. However, there is still the problem of the high operating voltages both for the single and multilayers devices.

Conclusions

In conclusion, it was shown that LED with single or multilayer composition of the active layer operate at high voltages, where impact excitation of Er^{3+} and unipolar injection are the main excitation mechanisms. The multilayers have allowed increasing the power efficiency roughly by 1.5 times with respect to the single layer devices. The value of the power efficiency at a fixed injected current decreases with the increase of the silicon content.

4.3. Bipolar Pulsed Excitation of Erbium Doped Nanosilicon LEDs

The energy transfer mechanism between silicon nanocrystals (nc-Si) and erbium ions is well documented under optical excitation, Walters et al. [23] and Peralvarez et al. [83] demonstrated sequential injection of electrons and holes into Si nanocrystals under the bipolar pulsed excitation of nc-Si LED. Priolo et al. suggested this excitation scheme as a solution to overcome nonradiative Auger de-excitation of Er^{3+} in nc-Si:Er^{3+} LEDs. [84] Miller et al. calculated a modal gain of 2 dB/cm in a slot waveguide confined nc-Si:Er^{3+} under the pulsed excitation which mitigates excited carrier absorption. [85] In this section, will evaluate the erbium excitation mechanisms and emission in nc-Si:Er^{3+} LED under electrical pumping using both direct current and bipolar pulsed excitation schemes, i.e., when the polarity of the applied voltage pulse is periodically changed.

Experimental

The nc-Si are formed during 1-hour high temperature anneal at 900 °C of a silicon-rich silicon oxide layer with a nominal 12% of silicon excess (9% measured by X-ray photoelectron spectroscopy) grown by LPCVD. As measured by secondary ion mass spectrometry, peak Er^{3+} concentration of ~ $4x10^{20}$ cm^{-3} is obtained by Er^{3+} implantation with a fluence of 10^{15} ions/cm^2 and energy of 25 keV. Post-implantation anneal is performed at 800 °C for 6 hours. A schematic layout of the n-type nc-Si:Er^{3+} LED is shown in Fig. 4.3.1.
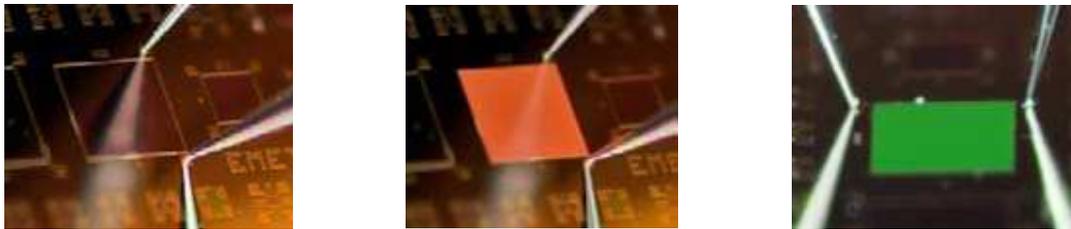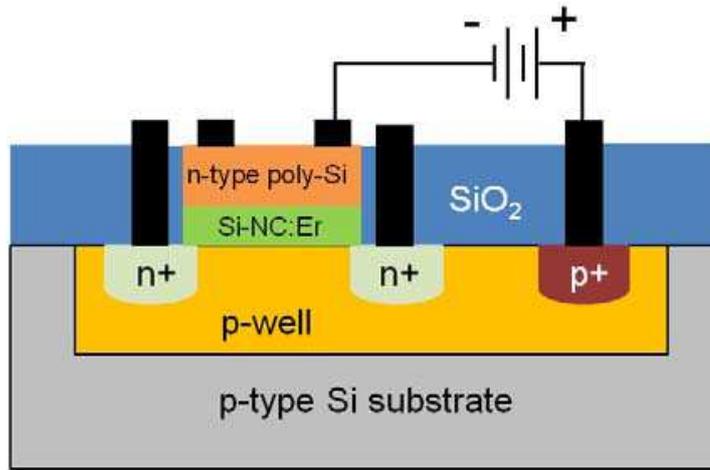
Figure 4.3.1: (top) A schematic cross section of the n-type CMOS nc-Si:Er3+ LED layout. Green color stands for the Er3+-doped nc-Si layer, blue – oxide, and black – titanium-aluminum-copper metal contact sandwich. (bottom, left to right) Photographs of the unbiased nc-Si LED, an orange emitting nc-Si LED under forward bias (a red square at the probe tips) and green emitting nc-Si:Er3+ LED.

The thickness of the active layer is 50 nm. A semitransparent window is formed by a conductive 150- nm-thick polycrystalline silicon layer and an antireflection coating of 93 nm of Si_3N_4 and 136 nm of SiO_2. The device studied in this work has a square gate area with a size of 500 μm × 500 μm and an n-type polysilicon gate. The direct current (DC) bias polarity convention is shown in Fig. 4.3.1. Electrical and optical measurements are performed at room temperature. Current-voltage (IV) characteristics are recorded with an Agilent B1500A semiconductor device analyzer. High frequency, 100 kHz, capacitance-voltage (C-V) measurements are performed with HP 4284A precision LCR meter. A 2-meter-long extension cable is used. The open circuit corrections are performed according to the operation manual. The alternating current (AC) signal voltage level is 50 mV. A function generator, Tektronix AFG 3252, coupled with a high-voltage amplifier, Falco Systems WMA-300, is used to drive the device in time-resolved electroluminescence (EL) measurements. Time-resolved EL signal is collected with a single-

photon detector module, id-Quantique 201, and recorded with a multichannel scaler, SRS 430. EL spectra are collected using a fiber bundle and analyzed with a Spectra-Pro 2300i monochromator coupled with nitrogen cooled charge-coupled device (CCD) cameras (one in visible and one in infrared, IR). Emitted optical power and EQE of the nc-Si:Er^{3+} LED are measured using both a calibrated LED and a Ge photodiode. The acceptance angle of optical systems is taken into account.

Direct current excitation

Electrical charge transport in these nc-Si LEDs is due to electric field-enhanced tunneling of electrons with the involvement of either defects [86] or confined energy states of nc-Si. [87] Erbium implantation produces deep energy trapping levels which change the transport properties of the nc-Si LED. [88] This is supported by the DC I-V and C-V characteristics shown in Fig. 4.3.2. The I-V curves of both nc-Si and Er^{3+}-doped nc-Si LEDs are shown in a voltage range where EL signal is observed under forward bias (Si substrate is in accumulation, see Fig. 4.3.1). The I-V curves are well describe by the Fowler-Nordheim field-enhanced tunneling law with effective energy barrier heights of 1.4 and 1.9 eV for nc-Si and nc-Si:Er^{3+} LED, respectively (assuming an effective electron mass of 0.3 m$_0$). The Er^{3+}-doped device is less conductive than the undoped device, which we ascribe to charge trapping at deep energy levels due to Er^{3+} ion implantation. [89] This is also supported by the C-V measurements (Fig. 4.3.2). The anticlockwise hysteresis loop of the C-V curves, which is due to positive charge trapping, is wider for the Er^{3+}-doped nc-Si LED than for the undoped nc-Si LED. Trapped charge density estimated from C-V hysteresis width of the nc-Si LED is 4.3x10^{12} cm^{-2}. Assuming one trapped electron per nc-Si, this value serves as a good estimate of the nc-Si area density. [90]
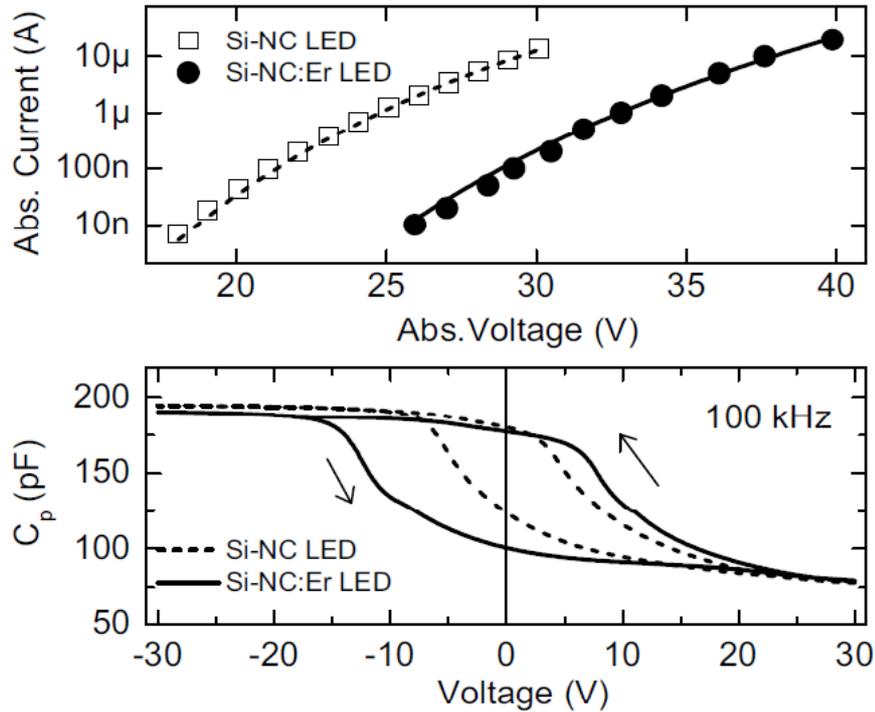
Figure 4.3.2: (top) Forward current-voltage characteristics of nc-Si and nc-Si:Er^{3+} LEDs. Symbols are experimental data values at which EL is observed, lines are fits to the Fowler-Nordheim tunneling law. **(bottom)** Capacitance-voltage characteristics of the Er^{3+}-doped and undoped nc-Si LEDs. The signal frequency is 100 kHz. The arrows show bias scanning direction in the C-V measurements.

Figure 4.3.3 (top panel) shows the integrated spectral EL intensity of the nc-Si and nc-Si:Er^{3+} LEDs as a function of injection DC current in the visible range and at wavelengths bracketing the 1.54 μm Er^{3+} emission, respectively. For low injection currents, EL intensity at 1.54 μm increases linearly with the DC current. However, at high currents a sublinear growth with injected current is observed. On the contrary, the visible emission from nc-Si increases almost linearly (with a slope of 0.91±0.01 in the log-log coordinates) as a function of the current. The saturation of the 1.54 μm emission may be attributed to both a limited amount of optically active Er^{3+} ions and to the onset of non-radiative recombination processes.
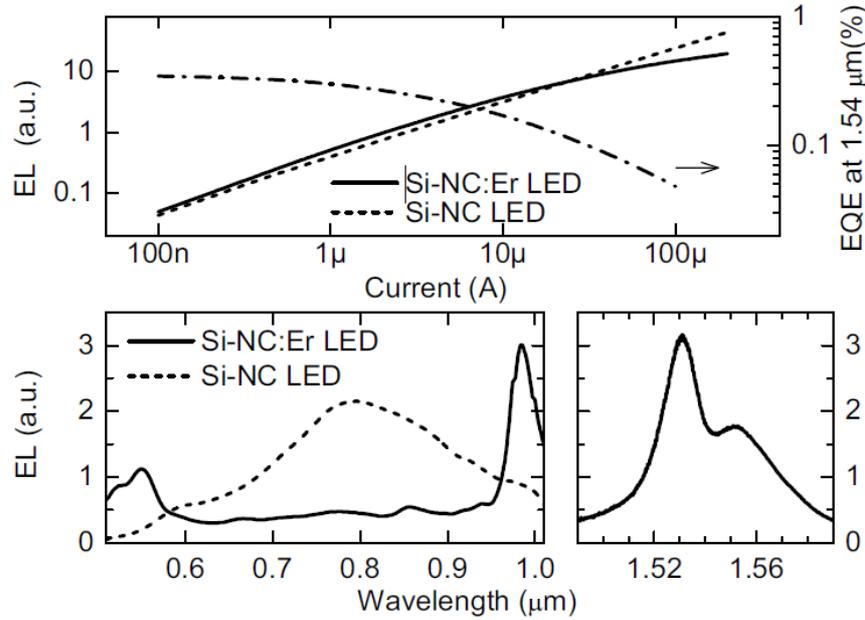
Figure 4.3.3: Integrated EL spectral intensity with wavelengths bracketing 1.54 μm (left axis, solid line) and in the visible range (left axis, dot line) for nc-Si:Er^{3+} LED and nc-Si LED, respectively, as a function of DC injected current. Please note that absolute values of the EL intensity in the visible and IR ranges are not to compare (the y-axes are not the same). The dash-dot line shows the corresponding EQE values at 1.54 μm (right axis). (bottom) EL spectra at the injected current of 2μA. The spectra are normalized to the detection system response.

The presence of the last is evidenced by the decrease of the luminescence decay time shown in Fig. 4.3.4, which will be discuss later. Figure 4.3.3 also shows the EQE of Er^{3+}-doped nc-Si LED emitting at 1.54 μm. It is noteworthy that these EQE values are among the best values reported so far for the Er^{3+}-doped silicon LED. The EL spectra of the nc-Si LED and of the nc-Si:Er^{3+} LED for a same injected current of 2 μA are shown in the bottom panel of the Fig. 4.3.3. The emission of the nc-Si LED is characterized by a broad peak centered at around 770 nm which originates from excitonic recombinations in the nc-Si. The nc-Si:Er^{3+} LED emission spectrum shows in addition to the broad nc-Si emission several sharp peaks at around 550, 660, 850, 980, and 1535 nm due to the excited Er^{3+} states emission (presence of the peaks at 660 and 850 nm is more evident at higher currents). High driving voltages (Fig. 4.3.2) along with the presence of the multiple Er^{3+} peaks indicate that Er^{3+} emission is mainly due to direct impact ionization of Er^{3+} ions and not to indirect Er^{3+} excitation via energy transfer from nc-Si. Energy transfer between nc-Si and Er^{3+} ions cannot be completely ruled out since, the nc-Si emission peak is much weaker in

the nc-Si:Er^{3+} LED than in the undoped device. Another argument for the interaction between Er^{3+} and nc-Si is the value of the excitation cross-section of Er^{3+}. This can be estimated by measuring the exponential rise and decay time of EL. The result is shown in Fig. 4.3.4. The excitation cross-section value extracted from the data is $(5 \pm 2) \times 10^{-14}$ cm^2. Note that the evaluation is based only on the rise and decay times for driving voltages larger than 30 V.
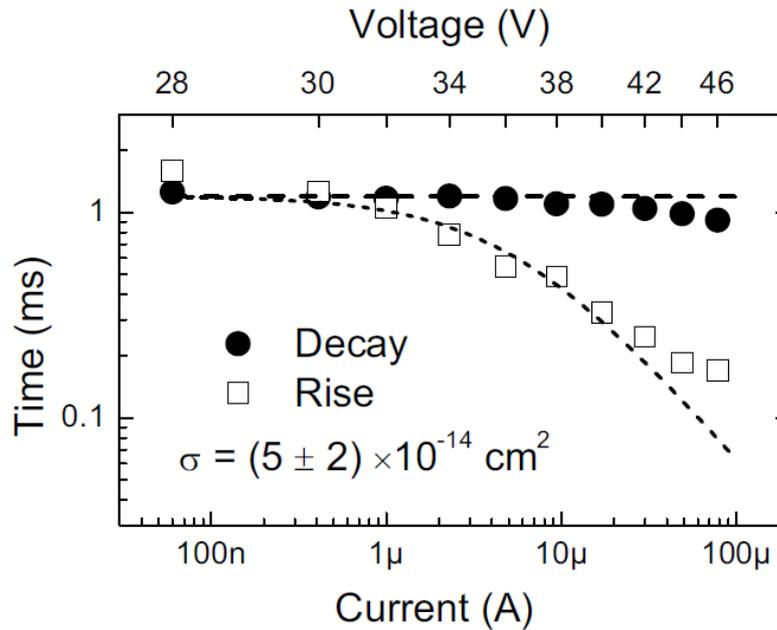

Figure 4.3.4: Exponential decay and rise times of an integrated EL spectral intensity in IR as a function of LED driving voltage (top x-axis) and the corresponding current taken from the DC I-Vs in Fig. 4.3-2 (bottom x-axis). Measurement uncertainty is smaller than the symbol sizes. The Er^{3+} excitation cross-section value estimated from the data is $(5 \pm 2) \times 10^{-14}$ cm^2. The lines are fitted functions with a constant value of the decay time of 1.2 ms and an excitation cross-section value of 5.9×10^{-14} cm^2.

For lower driving voltages, the 1.54 μm EL^{3+} rise time exceeds 1.20 ± 0.02 ms, which is equal to the EL^{3+} decay time. It should be also noted that the EL decay time is similar to the measured 1.54 μm photoluminescence (PL) lifetime of 1.31 ± 0.05 ms. The excitation cross-section value measured is larger than the known value of direct impact excitation of Er^{3+} in SiO$_2$, $(6 \pm 2) \times 10^{-15}$ cm^2, and which is close to the indirect Er^{3+} excitation cross-section value for Er^{3+} coupled to nc-Si. It is noteworthy that the decrease in the decay lifetime only moderately accounts for the decrease in EQE shown in Fig. 4.3.3. Saturation of optically active Er^{3+} concentration might account for the rest of this decrease. In summary, the results of the DC excitation presented

in this section suggest that electrical current is due to electron tunneling mediated by nc-Si in the nc-Si LED and Er^{3+}-related defects in the nc-Si:Er^{3+} LED. They also show that Er^{3+} is primarily excited by impact of high energy electrons.

Bipolar pulsed excitation

Figure 4.3.5 shows the spectrally integrated EL intensity at 770 nm and 1.54 µm as a function of the driving frequency for a bipolar pulsed excitation scheme.
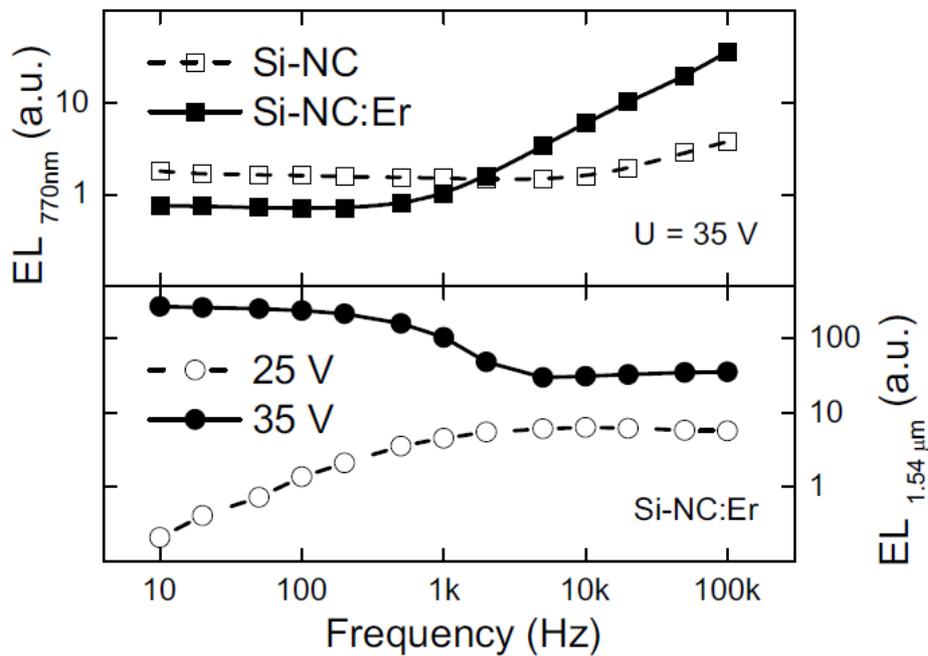

Figure 4.3.5: (top panel) Peak EL intensity at 770 nm as a function of bipolar-pulse driving frequency with a fixed RMS voltage of 35 V for both Si-NC and nc-Si:Er^{3+} LEDs. (bottom panel) Integrated EL spectral intensity in a wavelength range bracketing 1.54 µm as a function of bipolar-pulse driving frequency at a fixed RMS voltage of 25 and 35 V for the nc-Si:Er^{3+} LEDs. The meaning of the different symbols is stated in the figure legend.

Here the LEDs are driven by varying the bias periodically and rapidly (within <400 ns) from forward to reverse and from reverse to forward with a square waveform at a frequency f. At low driving frequencies, f ≪ 1 kHz, the EL intensity at 1.54 µm (bottom panel in Fig. 4.3.5) decreases a little with the frequencies for high driving voltages and increases for low driving voltages, being much weaker for the low bias. As the driving frequency approaches 1 kHz, which corresponds to the inverse of Er^{3+} emission lifetime, the EL intensity decreases (increases) for

high (low) bias. In a frequency range f >> 1 kHz, which we name a moderate frequency range, it changes only slightly for both the high and low bias. This behavior is accompanied by an increase of the peak EL intensity at 770 nm (Fig. 4.3.5, top panel; high bias). It should be noted that the onset frequency of this increase is 1 kHz unlike the undoped nc-Si LED where the EL starts to significantly increase above 10 kHz. The EL decay lifetime of nc-Si is around 5 μs (measured by both PL and EL), which corresponds to a frequency of 200 kHz. These high frequencies are not available with our instruments and, so that, the lifetime of nc-Si does not limit the EL intensity in the studied frequency range.
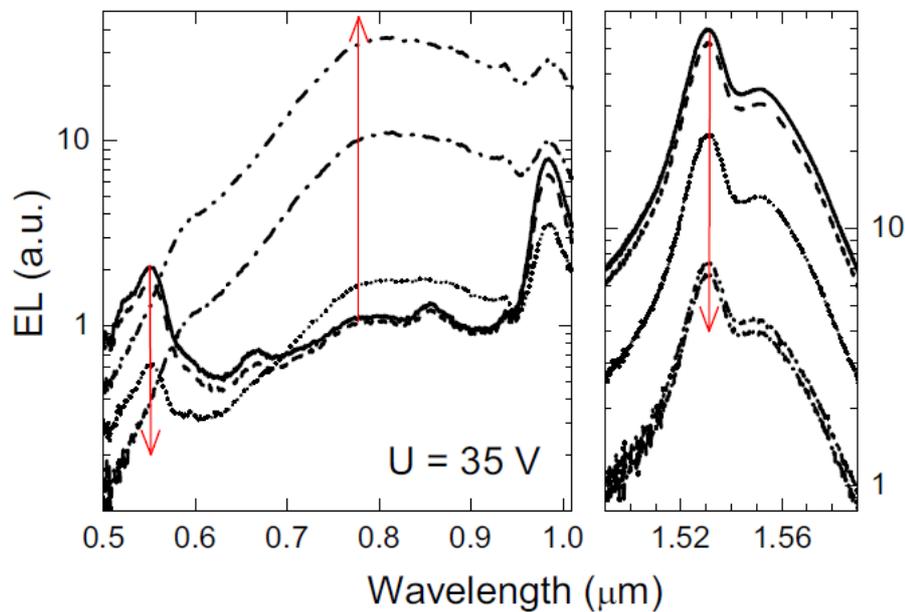

Figure 4.3.6: The EL spectra at 10, 100, 1 k, 10 k, and 50 kHz for the nc-Si:Er^{3+} LEDs shown in Fig. 4.3.5. The ascending frequency order is indicated by the arrows.

The frequency dependence of the EL intensity is reflected in evident changes of the nc-Si:Er^{3+} LED spectral characteristics, which are shown in Fig. 4.3.6. The multiple excited Er^{3+} states emission peaks weaken, but the peaks at 980 and 1535 nm. The nc-Si emission peak emerges. These changes has to be attributed to a change in the dominant excitation mechanism of Er^{3+} ions: from electron impact to the energy transfer between nc-Si and Er^{3+} ions. Under the pulsed excitation scheme, sequential injection of electrons and holes into nc-Si takes place. If the injection frequency is smaller than the Er^{3+} emission rate of about 1 kHz, both nc-Si and Er^{3+} are

in relaxed states and follow the frequency. If the excitation frequency is higher than the Er^{3+} emission rate (while still smaller than the Si-NC emission rate of 200 kHz), Er^{3+} stays in an excited state and barred from impact. However, more efficient injection into nc-Si at high injection frequencies provides additional indirect Er^{3+} excitation by means of the energy transfer.
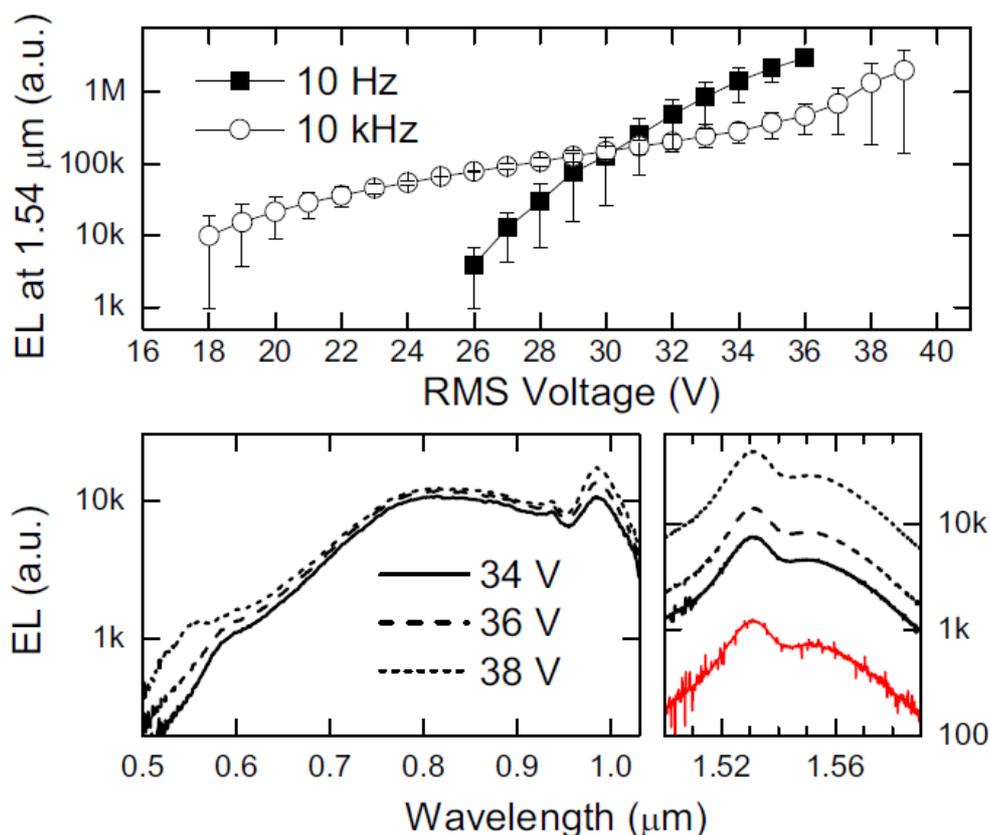

Figure 4.3.7: EL intensity at 1.54 μm as a function of RMS voltage under bipolar pulsed electrical excitation for two driving frequencies 10 Hz (squares) and 10 kHz (circles). The low panels show EL spectra at 34, 36, and 38 V_{RMS} at 10 kHz. Notice an appearance of the Er^{3+} emission band at 550 nm at 38 V. The lowest red line at the right – is the EL spectrum for 30 V_{RMS} at 10 Hz. No light emission was detected in the visible region at 30 V_{RMS} and 10 Hz.

Note that in these samples only ~1% of the total Er^{3+} population is coupled to the nc-Si therefore it is this 1% of Er^{3+} ions which shows an increased excitation due to a better energy transfer from the nc-Si. The fact that the energy transfer between nc-Si and Er^{3+}-ions becomes a dominant Er^{3+} excitation mechanism at the moderate frequency range is further supported by the voltage dependence of EL intensity at 1.54 μm shown in Fig. 4.3.7. The voltage dependence is stronger for low than for moderate injection frequencies. It is important that the EL signal in the

moderate frequency range is observed at lower driving voltages than in DC or low frequency excitation, namely the onset of EL was measured at around 18 V_{RMS} (Fig. 4.3.7). Beyond this value, charge trapping in the oxide arrests EL. The energy transfer remains the main excitation mechanism of Er^{3+} up to about 36 VRMS at moderate frequencies. This is supported by the EL spectra shown in Fig. 4.3.7. There are no Er^{3+} related peaks at wavelengths below 980 nm at low-to-moderate voltages, while an Er^{3+} peak centered at around 550 nm is observed at 38 V_{RMS}. At high voltages, ca. 36 V_{RMS}, and moderate frequencies, the EL emission is dominated by impact.

Conclusions

It was observed a change in the Er^{3+} excitation mechanism under pulsed electrical injection and studied its dependence on the injection frequency and voltage pulse amplitude. We ascribe Er^{3+} emission at high voltages (for both DC and pulsed injection) to the impact excitation by high energy electrons while Er^{3+} emission is due to the non-radiative energy transfer from nc-Si at low voltages. The Er^{3+} emission at the low voltages becomes accessible only at moderate injection frequencies which are larger than the inverse of Er^{3+} emission lifetime of a few milliseconds. This behavior is quite general since a similar trends was observed on a number of other nc-Si:Er^{3+} LEDs with various structural parameters.

4.4.   Erbium Doped Silicon Nanocrystal Based Laser: Process Flow

The study of erbium doped silicon nanocrystal material shows interesting results as shown in the previous sections. More interesting is the use of this material in optical cavities in order to achieve optical amplification. In this section, I will present the process flow developed to fabricate laser structures. In order to ensure electrical pumping and wave guiding, an horizontal slot waveguide configuration was chosen. Figure 4.4.1 shows the slot waveguide in which the active material is in between two wall of doped silicon. The doped wall are used to build the slot waveguide as well as electrical contacts.
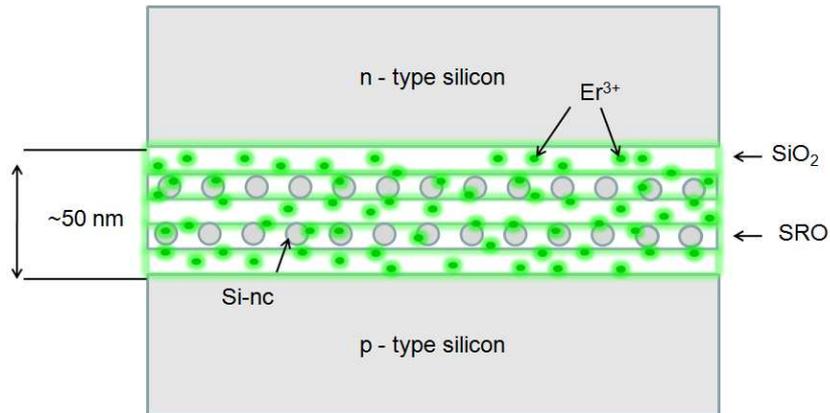
Figure 4.4.1: Active material cross-section. Final material composition as well as other parameters (time, type, temperature of annealing, number of layers etc.) will be decided on basis of control devices results (shown in the previous sections).

Figure 4.4.2 shows the devices final cross-section. The "wings" of the slot waveguide have two functions:

- to be used as contact (top and bottom);

- to space apart the areas of high doping and the metal contacts from the optical modal area of the active region.
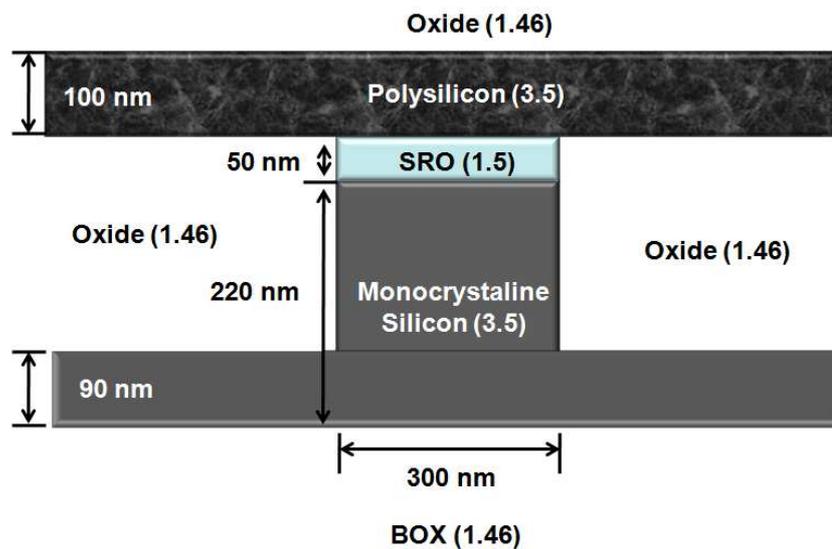

Figure 4.4.2: Slot waveguide cross-section. In the brackets the refractive indexes of the materials are shown.[8]

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[8] Design Optimizaion by Nikola Prtliaga

Two types of cavities were designed (Fig. 4.4.3):

- ring resonators coupled to a waveguide;
- Fabry-Perot based on two Brag gratings.

Different ring radius, waveguide widths and coupling distances were designed in order to find the best trade-off between electrical injection, optical amplification and signal extraction. As well, for the Fabry-Perot, waveguide widths and cavity lengths were varied.
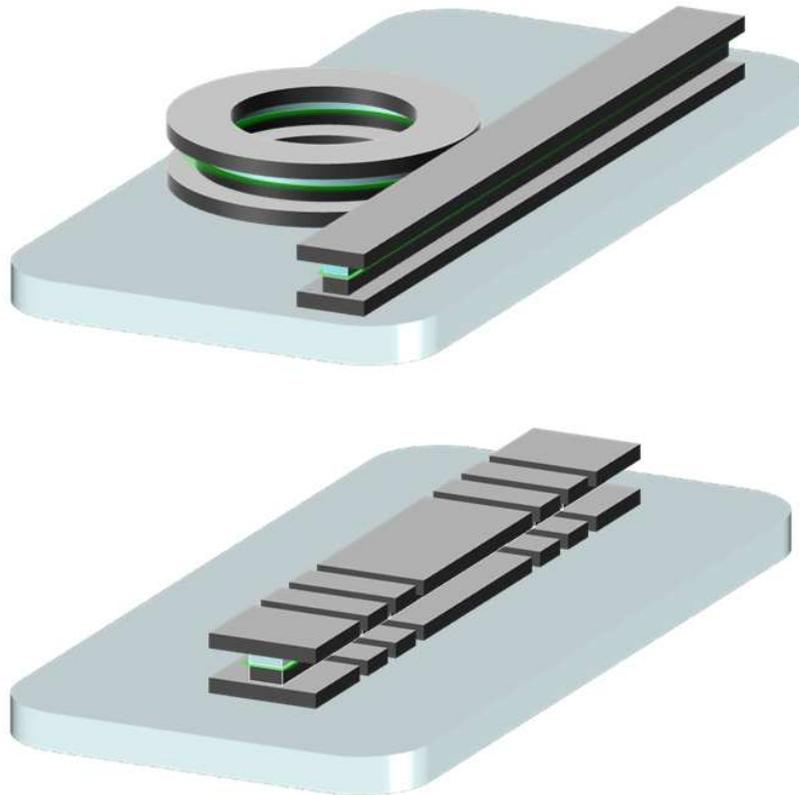

Figure 4.4.3: Type of cavities. (top) ring resonators coupled to a waveguide, (bottom) Fabry-Perot based on two Bragg gratings

In the following I describe the detailed process flow. Four structure are presented at the same time:

a) waveguide;

b) Fabry-Perot based on two Bragg gratings;

c) ring resonator coupled to a waveguide;

d) cross-section view.

106

Figure 4.4.4 shows the substrate cross-section. The starting point is a p-type (10^5 at./cm^3) SOI (silicon on insulator) wafer, i.e. 220 nm of monocrystalline device layer silicon on top of 2 µm of buried silicon oxide (BOX).
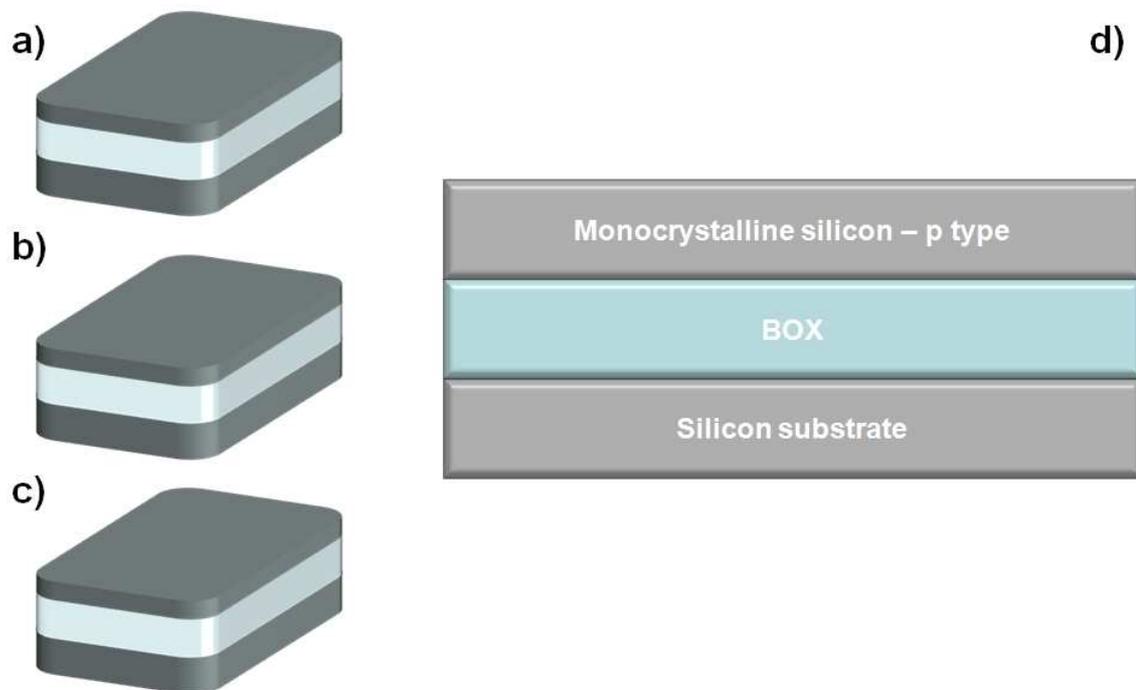
Figure 4.4.4: Substrate cross-section. Four types of structures are represented: a) waveguide, b) Fabry-Perot based on two Bragg gratings, c) ring resonator coupled to a waveguide and d) cross-section view.

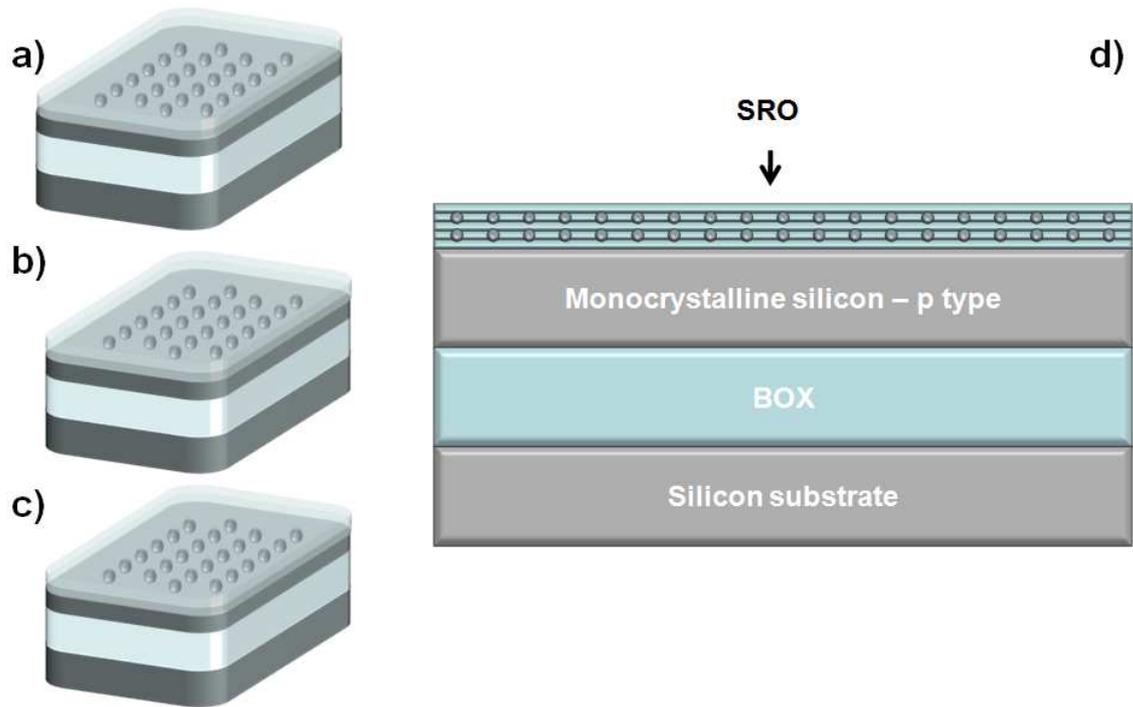The process starts with the SRO deposition and the thermal treatment (Fig. 4.4.5).

Figure 4.4.5: SRO deposition and thermal treatment.

The next step is the definition of the erbium doped regions and proceed as follow (Fig. 4.4.6):

a) photo-resist deposition;

b) resist photo-lithography of the erbium doped zone;

c) erbium implantation;

d) post-implantation annealing;

e) photo-resist removal.
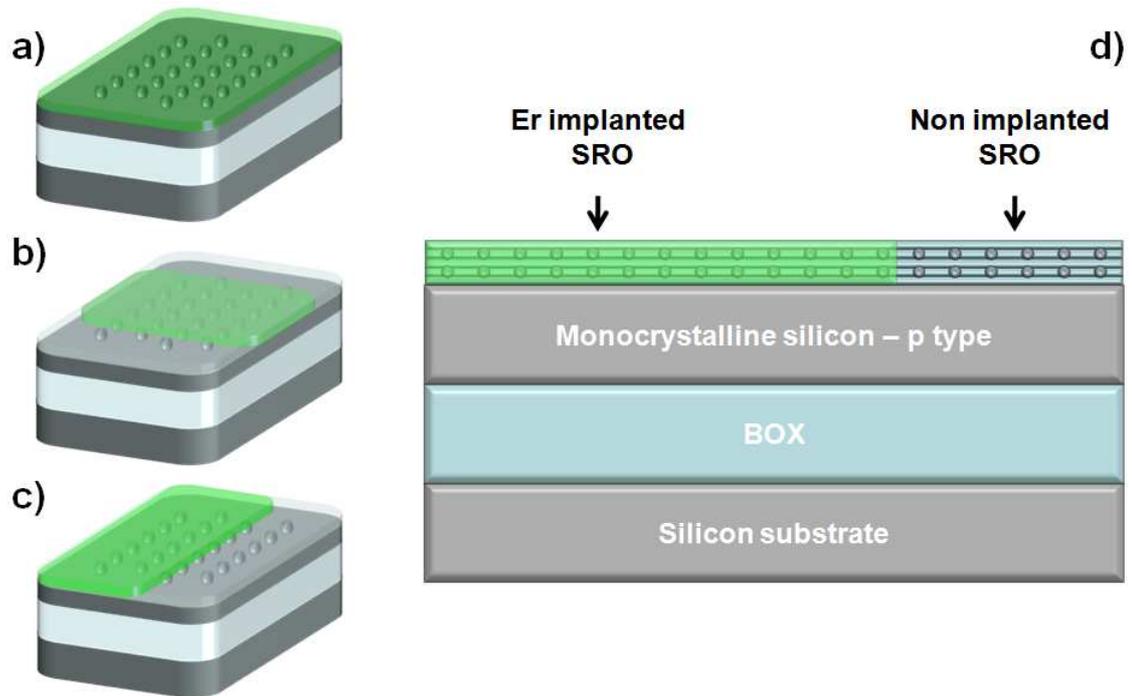
Figure 4.4.6: Erbium doped regions definition and erbium implantation.

Figure 4.4.7 shows the result of the process after:

a) polysilicon deposition;

b) hard-mask deposition;

c) photo-resist application;

d) photo-lithogrphy of the structures;

e) etching of the hard-mask;

f) stripping;

g) polysilicon etching;

h) SRO etching;

i) partial silicon etching;

j) heavy p-type dopping ($\sim 10^{20}$ at./cm^3);
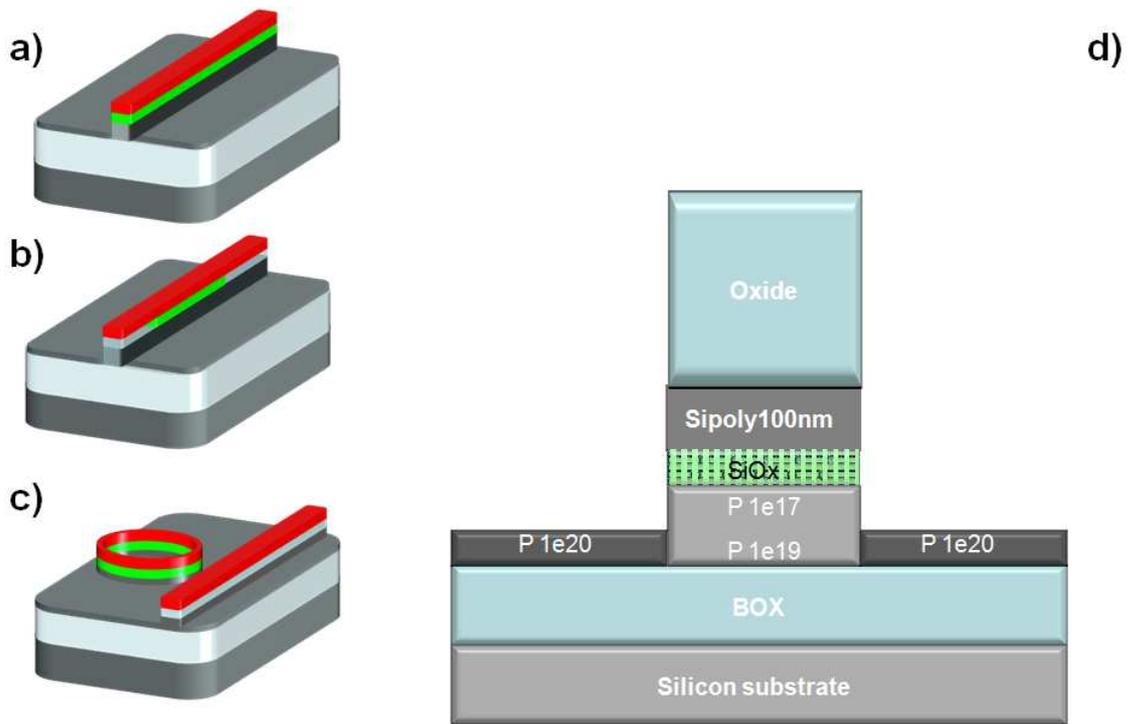
k) dopants thermal activation.

Figure 4.4.7: Structures definition. Green represents the Er³⁺ doped active region; Red represents polysilicon top layer.

After a silicon oxide deposition, through a chemical-mechanical polishing (CMP) the structures are planarized and the polysilicon thickness reduced to about 20 nm (Fig. 4.4.8).
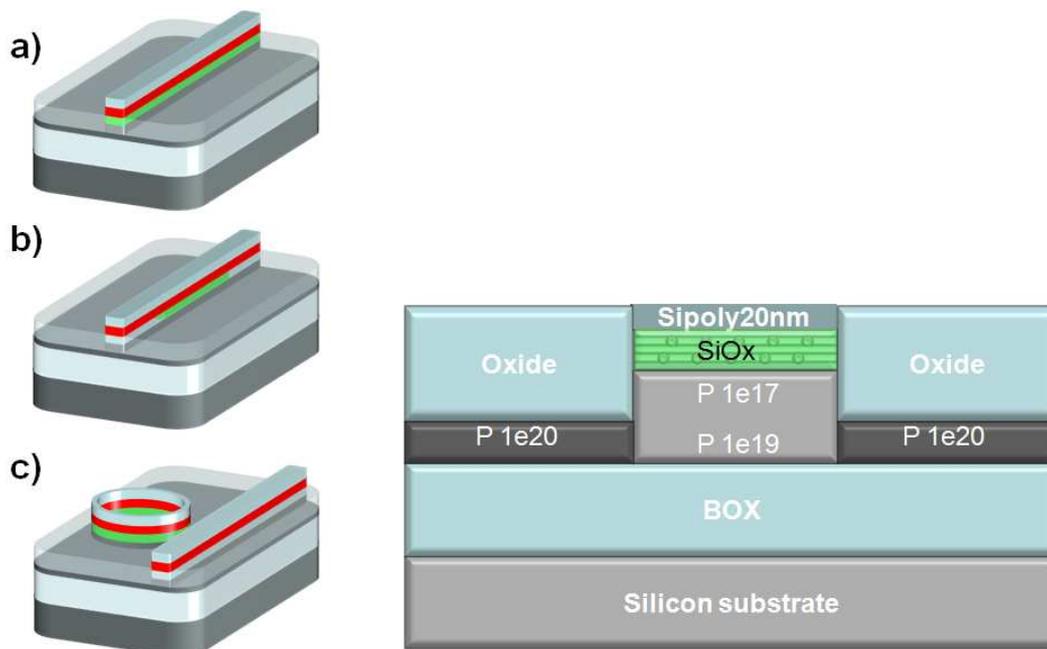

Figure 4.4.8: Structures after CMP.

110

The process proceed with a deposition of 100 nm of polysilicon and the doping of the contact regions (Fig. 4.4.9).
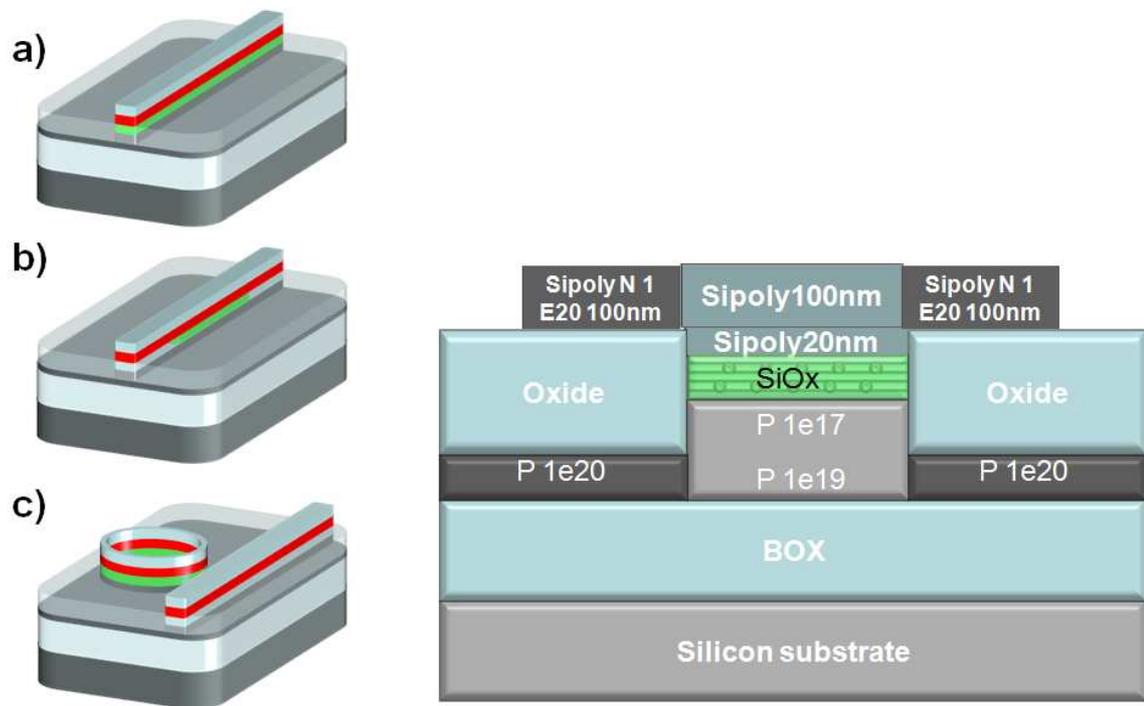

Figure 4.4.9: Top wing formation and contact doping.

After the contacts definition, the metallization and the definition of the electrical pads complete the process. The final results is shown in Fig. 4.4.10.
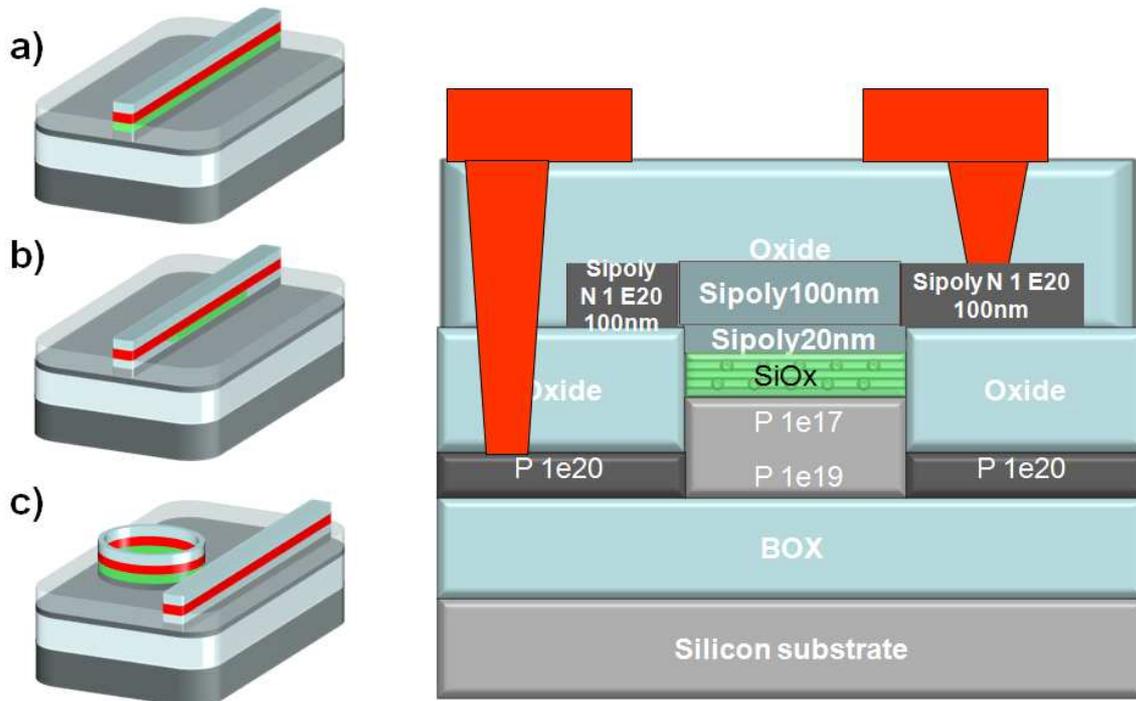
Figure 4.4.10: Final cross-section of the structures.

The mask layout is shown in Fig. 4.4.11. The die is divided in three regions. One region is dedicate to the ring resonator structures. 27 different structures are present and they are the combinations of 3 waveguide widths, 3 ring radius per waveguide width and 3 coupling distances per ring radius. Another region is dedicated to the Fabry-Perot cavities. 6 different structures are present and they are divided in 3 different waveguide widths and 2 cavity length per waveguide width. The third region is dedicate to the test structures. In that region, slot waveguides of different widths and lengths are present in order to estimate the waveguide propagation losses. Structures composed by a series of bend with different waveguide widths and radii are used to estimate the bend losses. Several other structures are dedicated to the electrical tests in order to evaluate the contact resistivity in the lateral and longitudinal directions.

112

Figure 4.4.11: Die layout.

Figure 4.4.12 and figure 4.4.13 show more details on the ring resonators and Fabry-Perot cavities lay-out.

HIGH Reflectivity FP Mirror

Short Fabry-Perot 31.5 mm

FP_60_WG_300_NM

FP Mirror Periods **Waveguide Width**

LongFabry-Perot 120.2 mm
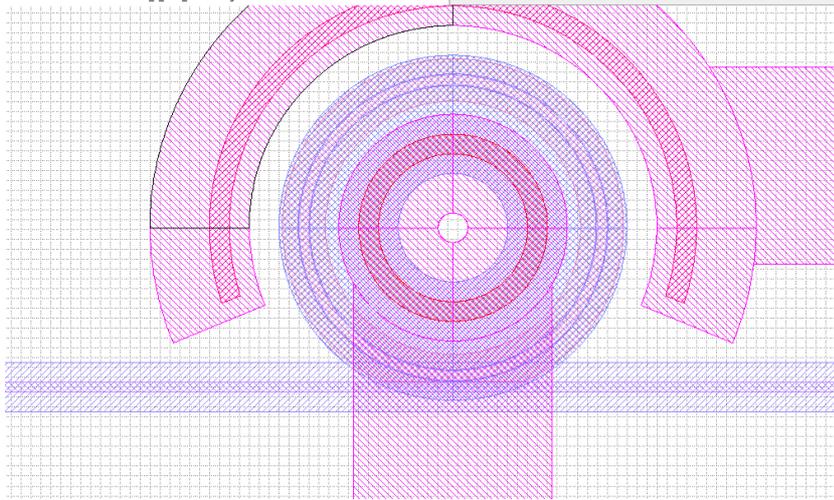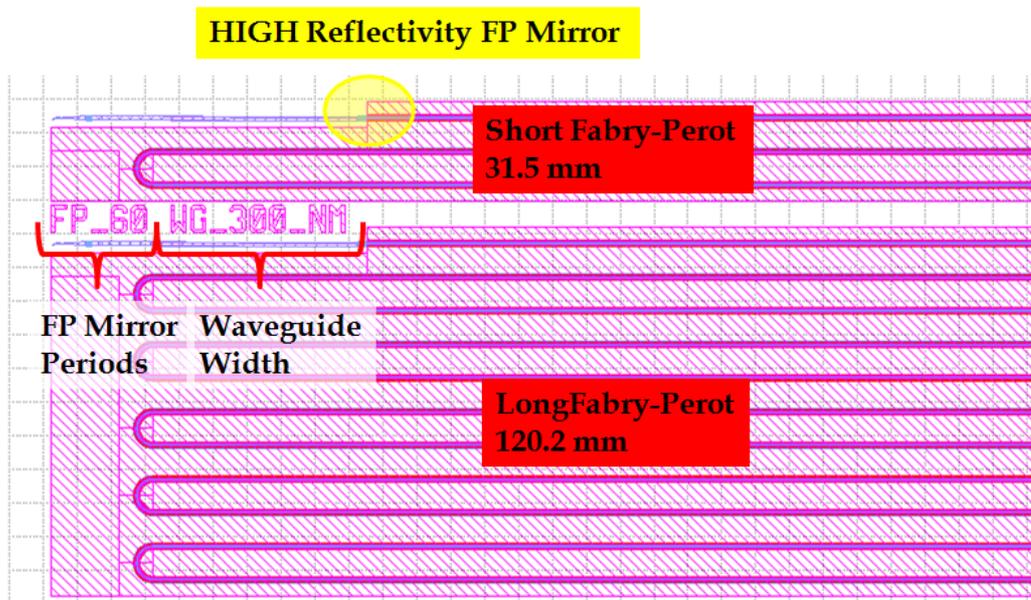
Figure 4.4.13: Fabry-Perot details

I note that the Fabri-Perot structures were designed by Nikola Prtljaga while the ring-waveguide structures by Nicola Daldosso. I personally draw the mask layout and prepared the GDS file.

5. Other Applications of Silicon Nanocrystal Based Devices

5.1. Introduction

In this chapter, some other applications of silicon nanocrystal are presented. An example of all-silicon solar cell is shown. The photovoltaic properties and carrier transport of silicon nanocrystal based solar are studied. At the end, the combination of emitting and absorbing properties of silicon nanocrystal based LED are used to develop an all-silicon based optical transceiver.

5.2. Photovoltaic properties of Si nanostructure based solar cells

Recent results have shown the possibility of using silicon nanostructures to develop 3rd generation photovoltaics, [91] where the theoretical efficiency is well beyond the Shockley-Queisser efficiency limit. [92] The most promising applications of Si nanostructures in 3rd generation solar cells are all-silicon tandem cells, [93] photoluminescence down shifter, [94] and hot-carrier solar cells. [95] So far, only a few examples of all-silicon tandem solar cell have been reported. [96] These are stacks of p/n junctions where the active materials have different energy thresholds each absorbing a different band of the solar spectrum. Usually they are connected together in series. In a silicon nanostructure tandem cell, the active material of the sub-cell absorbing photons with higher energy than that of the bulk silicon is formed by silicon nanostructures, which have larger and tunable bandgap than that of bulk silicon. This cell geometry offers a significant improvement in efficiency without increasing appreciably the manufacturing costs per unit, even for large-volume production, which results in a corresponding decrease in installed system costs. The theoretical efficiency limits for two-cell and three-cell stacks are 42.5% and 47.5%, respectively. There are many methods to fabricate Si-nanostructures. Their photovoltaic properties and carrier transport

should be compared between different silicon nanostructures to optimize the all-silicon tandem cell. Moreover, the sub-cell of an all-silicon tandem cell should be preliminary studied to elucidate the role and properties of the silicon nanostructures independently of the underneath silicon. Here silicon nanostructure based solar cells fabricated on a quartz wafer are presented.

Experimental

All cells were fabricated on 500 µm thick 4 inch quartz wafers. The geometry and layer sequence of the cells are shown in Fig. 5.2.1. A 180 nm thick layer of polycrystalline p-doped silicon layer was deposited on quartz by low pressure chemical vapor deposition (LPCVD) followed by boron ion-implantation to obtain the p^+ silicon layer. Its resistivity after dopant activation is 0.05 Ω cm.
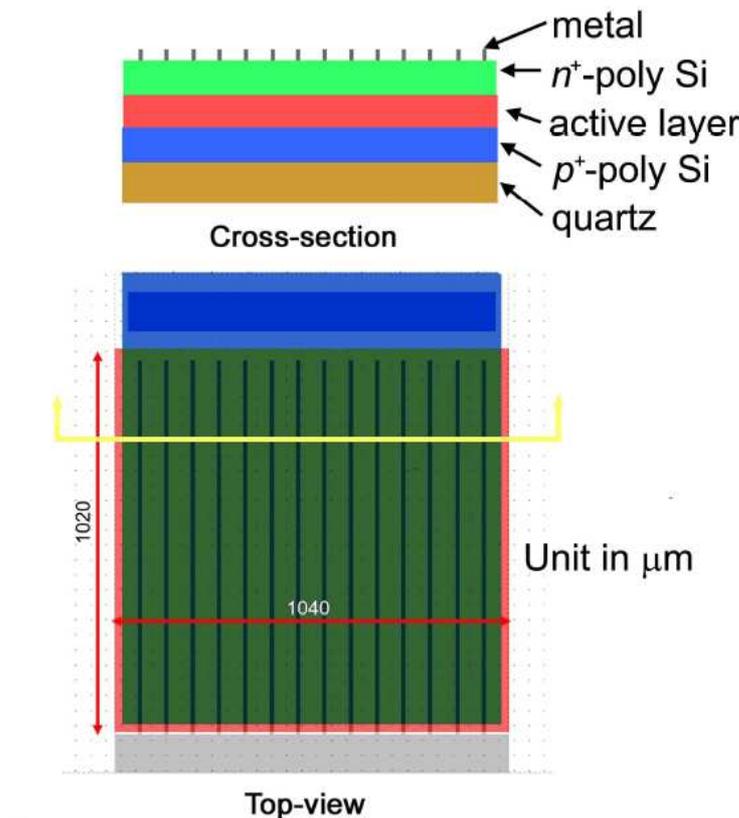

Figure 5.2.1: Top-view and cross-section of the devices.[9]

The active layer was deposited by plasma enhanced chemical vapor deposition (PECVD) followed by a furnace annealing at 1050 °C in N_2 for 60 min. Three different active layer

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[9] Fabricated by FBK

116

compositions are compared: an amorphous silicon (a-Si)/SiO$_2$ superlattice (Q1), a silicon-rich silicon oxide (SRO)/SiO$_2$ superlattice (Q2) and a silicon-rich silicon nitride (SRN)/Si$_3$N$_4$ superlattice (Q3). The three different active layers are composed by superlattices of 5 periods where the nominal thickness of the silicon nanostructure is 3 nm and the thickness of the barrier layer is 1 nm. For SRO layers, the gas ratio between N$_2$O and SiH$_4$ in PECVD chamber is 3, the plasma power is 30 W. While the ratio is 30 for the SiO$_2$ layer. The a-Si was deposited by PECVD using Ar diluted SiH$_4$ as precursor and 50 W plasma power. For SRN layers, the gas ratio between NH$_3$ and SiH$_4$ in PECVD chamber is 1:3 with N$_2$ as diluent. While for Si$_3$N$_4$ layer, the gas ratio between NH$_3$ and SiH$_4$ is 8:11. Both layers are deposited at 50W plasma power. The substrate temperature of all thin films deposited by PECVD was maintained at 300 °C. Finally, a 70 nm thick poly-crystalline n$^+$-doped silicon layer was deposited by LPCVD and in situ doped, with a resulting resistivity of 1.0×10^{-3} Ω cm. The bottom poly-p and top poly-n electrodes were surface contacted by Al metal layer and grid, respectively. All cells have a working area of 1.06 mm^2. Current-voltage (I-V) characteristics have been recorded both in dark and under light illumination in a micro-probe station by an Agilent B1500A. Spectral response has been measured by a LH 151 Xenon arc lamp (1000 W) coupled with a monochromator GM 252. The measurements were performed at room temperature. A 550 W ABET SUN 2000 solar simulator with AM1.5G spectrum was used for the photovoltaic parameter measurement.

Results and Discussions

A multilayer structure has been used to fabricate silicon nanostructures to finely control the size of the silicon nanostructures. When amorphous silicon is used, after annealing, a quantum well-like silicon nanostructure is obtained where the carriers are confined in one dimensional (vertical to the amorphous layers) by the two adjacent SiO$_2$ layers whereas, when a silicon rich dielectric is used, a quantum-dot like nanostructure arranged in a vertical superlattice geometry is obtained where the carriers are three dimensionally confined. In this case, the nc-Si diameter is defined by the thickness of either the SRO or SRN layers. Size control is crucial because both the conductivity as well as the bandgap of the sub-cell depend on it.
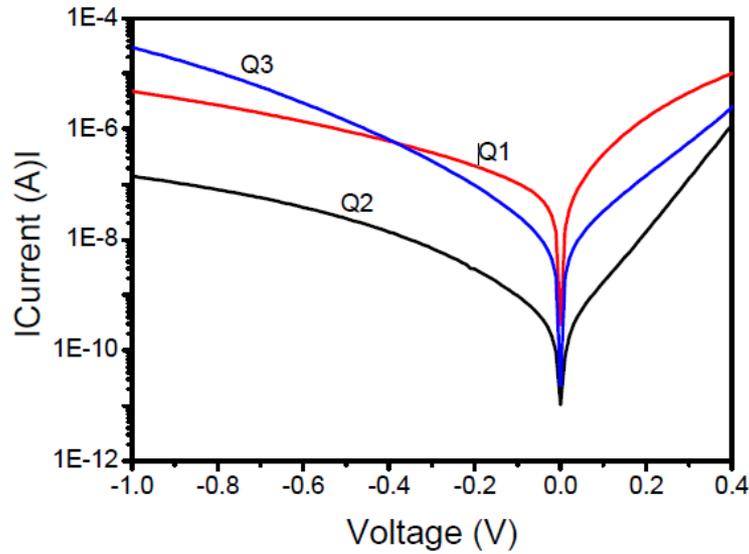
Figure 5.2.2: I-V curves of the devices. The different curves refer to different active layer structures as indicated.

Figure 5.5.2 shows the current-voltage (I-V) curves of the devices. According to the I-V measurements, conductivity of the Q1 device is higher than those of the other devices under forward bias. This is expected since Q1 has a larger Si content. The current of Q3 is larger than that of Q1 under reverse bias larger than -0.4 V due to a larger defect content which provides current shunt paths. If we compare the nc-Si superlattices Q2 and Q3 devices, we found that nitride based nanostructures (Q3) conduct better than oxide based nanostructure (Q2). The conductivity in the three devices is mainly affected by two factors. Firstly, although silicon nanostructures have been formed by phase separation in all devices, their particular structure differs. After the high temperature annealing, the a-Si crystallizes into brick-shaped nanostructures [97] (Q1) while spherical nc-Si precipitate from SRO and SRN layers through phase separation mechanism [98] (Q2 and Q3). Secondly, the dielectric matrix where the nanostructures are formed, influence the transport. In fact, the tunneling probability is mainly dependent on the barrier height between the barrier layer and the nc-Si. Si_3N_4 has a lower barrier height than SiO_2 with respect to Si. Thus Si_3N_4 layer is more transparent for charge flow than SiO_2. Photovoltaic properties of different devices were investigated under 1 sun illuminations. A representative result for Q1 is shown in Fig. 5.2.3. A short circuit current $I_{sc} = 6 \, \mu A$ was found, an open circuit voltage

V_{oc} =220 mV and a fill factor FF=0.30, due to poor shunt and high series resistances. The conversion efficiency is 0.04% which is mostly due to a low absorption (less than 10 percent of the incident light) by the active layer and bad transport properties.
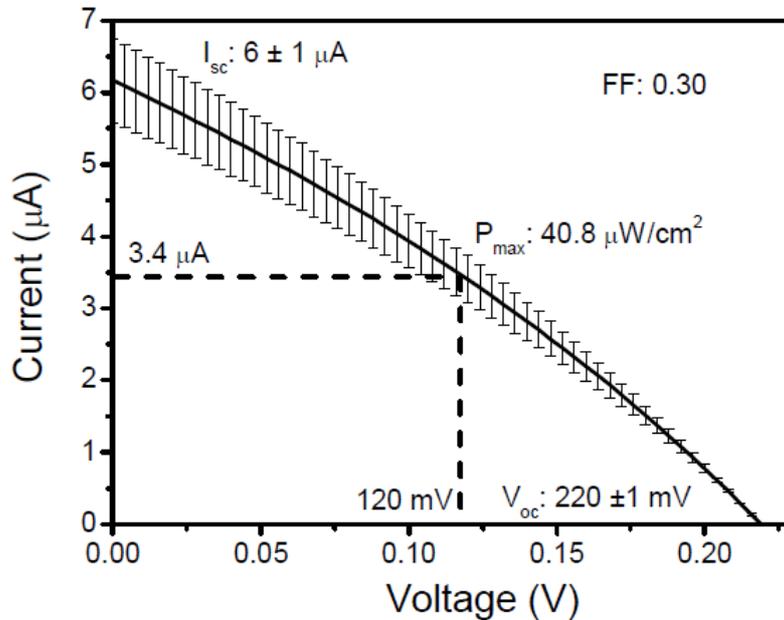
Figure 5.2.3: Photovoltaic characteristics of Q1 under illumination of a solar simulator at 1 sun with AM1.5G spectrum.

Photoresponsivities of the three devices are shown in Fig. 5.3.4. It is observed that the photoresponsivity follows the trends of the I-V data. Q1, which has the highest conductivity, has also the largest photoresponsivity. In addition, the photoresponse does not only scale with the conductivity but also with the absorbance of the nanostructure layer. Since the silicon content is larger in Q1, also the optical density is higher which in turn means a higher absorbance in the a-Si/SiO$_2$ quantum well superlattice than that in the other superlattices. The larger photoresponse of the nitride based superlattice with respect to the oxide based superlattice is due to a larger conductivity.

Figure 5.2.4: Photoresponsivity of the devices. The different curves refer to different active layer structures as indicated.

Conclusions

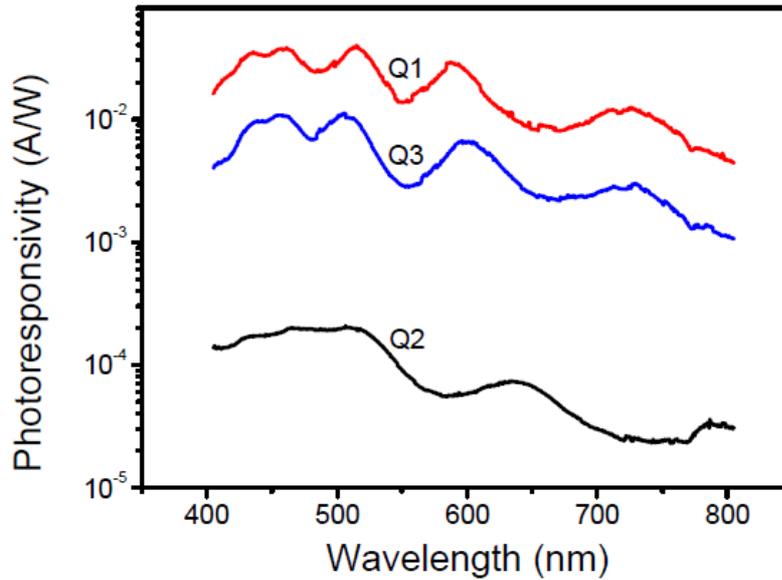In conclusion, different silicon nanostructure-based solar cells fabricated on quartz have been investigated to test their potentiality as sub-cell in all-silicon tandem solar cell. a-Si/SiO$_2$ quantum well superlattice seems to be the best since it shows a larger photovoltaic effect with respect to the other investigated nanostructures.

5.3. Silicon Nanocrystal Based Bidirectional Optical Transceiver

Silicon photonics is a demonstrated technology to enable interchip or intrachip optical interconnects. [99] [100] [101] Optical links able to send 50Gb/s over 200 m span have been fabricated. [102] The actual implementation of the light source and of the detector in silicon photonics is based on an heterogeneous approach where a III-V semiconductor act as the active laser material and a Ge semiconductor as the active detector material. [103] Therefore, there is still an interest to evaluate the potential of an all-silicon approach for optical interconnects. This could have lower performances, which implies different than high speed interconnect applications, but should be

120

cheaper and easier to fabricate within a standard CMOS factory. Among different possibilities, silicon nanocrystals (nc-Si) show interesting optoelectronic properties. nc-Si based light emitting diodes (LED) have been fabricated with standard CMOS processing. The power efficiency of nc-Si LED is still order of magnitude lower than III-V based LED one. However, it is of interest to investigate whether nc-Si LED can be used as one node of an optical link. Here, a nc-Si LED which is used as a light emitter as well as a light detector in an optical link (Fig. 5.3.1) is presented.
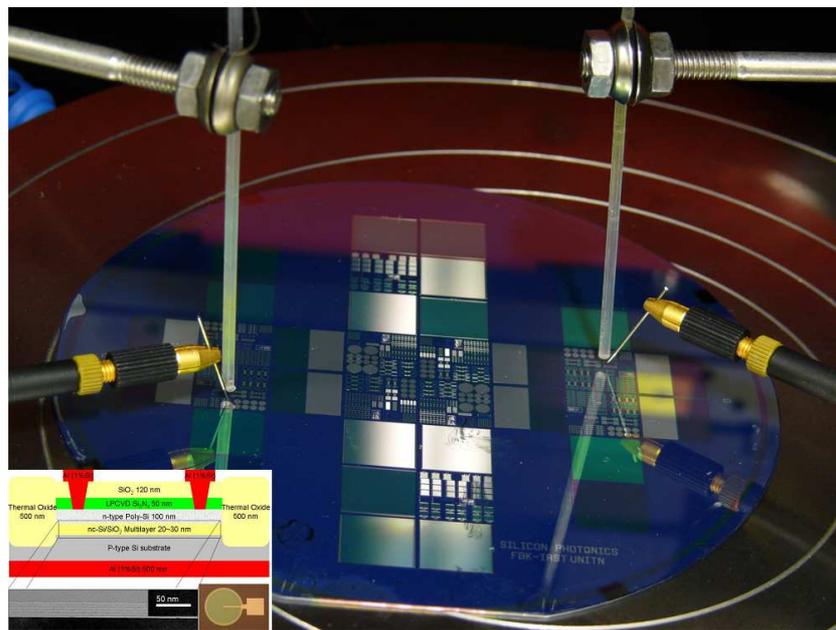
Figure 5.3.1: Image of the transceiver. The electrical signals are transmitted and collected by the top contacts, the chuck provide the reference bottom contact. The optical signals are transmitted through a 1 mm core optical fiber coupled on top of the devices. (Inset) Device schematic cross section and top view of the device.

The nc-Si LED structure is a metal oxide semiconductor capacitor where 5 alternating stoichiometric SiO_2 and silicon-rich oxide (SRO) layers are used as the active material which replaces the gate oxide.[10] (Inset of Fig. 5.3.1) The nominal thickness of SRO and of the oxide layers within the multilayer (ML) stack is 3 and 2 nm, respectively. Silicon nanocrystals were formed by annealing the ML at 1150 °C for 30 min in nitrogen atmosphere. The ML was deposited on a Si p-type wafer.

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[10] Fabricated at FBK

When the nc-Si LED is forward biased (gate negative), an external power efficiency of up to 0.2% and an emission peak centered at about 750 nm are observed (see Ref. (104) for more details). When illuminated, the nc-Si LED shows a photovoltaic effect. [105] In addition, when reverse biased (gate positive) the nc-Si LED behaves as a photodector for visible/infrared light (from 400 nm to 1100 nm) with an average photoresponsivity of about 1 mA/W.
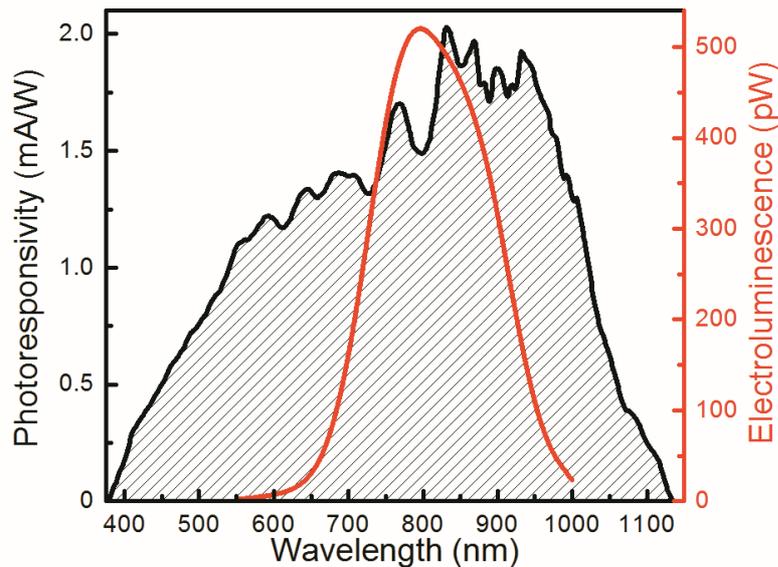

Figure 5.3.2: (Color online) (Filled area) Photoresponsivity of the device in detection mode: reverse biased at 5 V; (Empty area) Electroluminescence of the device in emission mode: forward biased at -5 V.

Figure 5.3.2, shows the optoelectronic properties (electroluminescence and photoresponsivity) of a characteristic nc-Si LED. The electroluminescence spectrum is measured under a forward biased of -5 V (ground on the bottom of the LED). The photoresponsivity spectrum of the nc-Si LED is measured for a reverse bias of 5 V. It could be noted that the emission spectrum under forward bias matches the high photoresponsivity region. In fact, two different device regions are responsible for the two different responses: the electroluminescence is due to emission of the nc-Si while the photoresponse is due to absorption in the silicon substrate. This combination has an advantage with respect to other all silicon approach for transceivers since the emission wavelength is spectrally separate from the absorption band-edge. As an example, J. Zhao *et al* [106]. reported an optical link between two similar silicon diodes. The performances of the link were limited by the fact that emission occurs at the silicon absorption band-edge.

An optical link between two equal 300 µm diameter nc-Si LED by coupling on top of the surface emitting LED a multimode 1 mm core plastic fiber is realized. Coupling losses (L_C) between the LED and the fiber are estimated to be 3dB. Two different configurations where the two LED are part of two different dies (i.e. electrically isolated and physically separated) or are on the same wafer (i.e. only electrically isolated, see Fig. 5.3.1) were tested. No differences in the results have been found. One of the LED was forward bias while a reverse bias was applied to the other LED. The results are not dependent on the choice of the LED. Both LED can work as receiver or as transmitter; this is the reason why the single LED is called a transceiver.
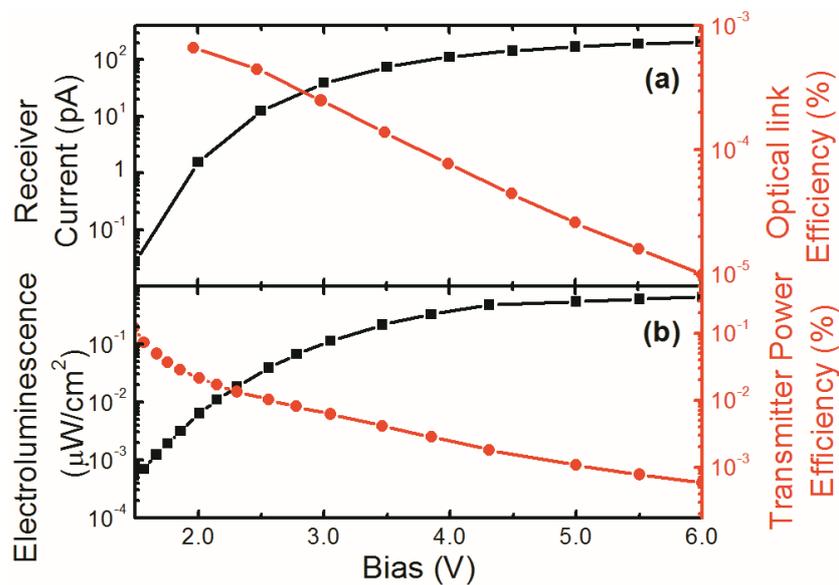
Figure 5.3.3: (a) Receiver photocurrent (Squares) and Optical link efficiency (Circles) as a function of transmitter bias; (b) Transmitter electroluminescence (Squares) and Transmitter power efficiency (Circles) as a function of transmitter bias.

Figure 5.3.3 a shows the receiver photocurrent and the optical link efficiency as a function of the transmitter bias. The transmitter bias was scanned from 0 V to -6 V while the receiver LED was kept at a constant reverse bias of 5 V. A significant receiver current is observed when the transmitter bias is larger than -2V. Figure 5.3.3 b shows the transmitter electroluminescence and transmitter power efficiency as a function of the transmitter bias. It is observed that the photocurrent is almost linear with the electroluminescence that is the receiver has a constant photoresponsivity. On the other hand, the transmitter power efficiency is strongly dependent on

the transmitter bias. From the ratio of the electrical power generated at the receiver (P_R) to the electrical power dissipated by the transmitter (P_T) we calculate the efficiency (η) of the optical link:

$$\eta = \frac{P_R}{P_T} = \frac{i_R V_R}{P_T} = \frac{\Re P_R^0 V_R}{P_T} = \frac{\Re L_C L_P L_C P_T^0 V_R}{P_T} = \frac{\Re L_C L_P L_C \eta_T P_T V_R}{P_T} = \Re L_C L_P L_C \eta_T V_R \approx 5 \times 10^{-4} \%$$

Equation 5.4.1

where i_R and V_R are the photocurrent and the reverse bias of the receiver, $\Re = 2\text{mA/W}$ and P_R^0 the photoresponsivity and the optical power reaching the receiver, L_C and $L_P = 0\text{dB}$ the coupling and the fiber losses, P_T^0 and $\eta_T = 0.2\%$ the transmitter emitted power and the transmitter power efficiency. The estimate agrees with the measured data as it is evident from Fig. 5.3.3. Note that in Fig. 5.3.3, P_R is calculated as the total power measured at the receiver ($P_{R,\text{tot}}$) minus the measured power in dark condition ($P_{R,\text{dark}}$): $P_R = P_{R,tot} - P_{R,dark}$. In Fig. 5.3.3 it is also clear that when the driving bias is increased, the link efficiency drops due to the decrease of the power efficiency of the transmitter. It is also important to emphasize that the system shows a good stability over time particularly with respect to the emitter that is most affected by stress.
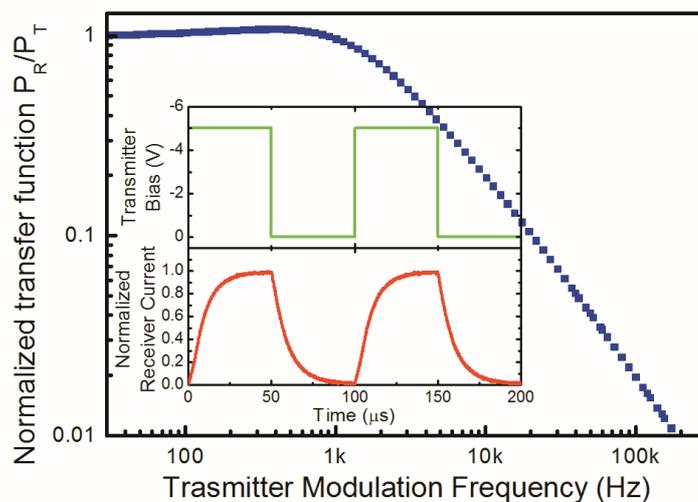

Figure 5.3.4: Normalized transfer function as a function of transmitter modulation frequency; (inset): Electrical bias of the transmitter (Top) and electrical output of the receiver (Bottom) as a function of time.

Figure 5.3.4 shows the frequency response of the optical link. The transmitter was drove under square wave forward bias (0,-5V) and variable frequency. A trans-resistive amplifier (50 Ω resistor) was used to measure the receiver signal with an oscilloscope operated in alternate current coupling. A typical lineshape is reported in the inset of Fig. 5.3.4. The receiver current follows the modulation of the transmitter bias. The cut-off frequency (3dB frequency) is at 3.3 kHz which is mainly due to the frequency limit of the transmitter. [107] However still at 100 kHz we are able to measure a modulated receiver current, though very weak.

An estimate of the power per bit needed to run the optical link can be found by the following arguments. Since the transmitter is switched on/off, while the receiver is always on: the power is dissipated during the on state (sending a bit) for the transmitter and during the waiting time for the receiver (when illuminated the receiver generates electrical power). The injected current in the transmitter at the -5V bias is 50 µA. If we consider a 10 kHz frequency, i.e. a 50 µs bit width, the dissipated power by the transmitter is 125 µW. On the receiver side, the bias is fixed at 5 V which corresponds to an injected current of 50 fA under dark condition, so the maximum dissipated power is 250 fW. Therefore, the main contribution to the dissipated power comes from the transmitter. Thus 125 µW per bit corresponds to an energy per bit of 1.25 µJ/bit.

In conclusion, an optical link based on a silicon nanocrystals device operated as a bidirectional transceiver was demonstrated. The link performances have been evaluated and found suitable for niche applications where the most important metrics are integrability and low cost, e.g. for lab-on-a-chip applications or for slow data communication in consumer electronics. Indeed, the performance of the optical link is not at all comparable to the state-of-the-art interconnect technology available in silicon photonics.

6. Conclusions

In this thesis, fabrication and characterization of silicon nanocrystal based devices were presented. In collaboration with Intel Corporation and Bruno Kessler Foundation and thanks to the support of European Commission through the project No. ICT-FP7-224312 HELIOS and through the project No. ICT-FP7-248909 LIMA, it was shown that layers and devices containing silicon nanocrystals can be formed in a production silicon-fab on 4 and 8 inch silicon substrates via PECVD and subsequent thermal annealing. Devices produced by single layer and multilayer deposition were studied and compared in terms of structural properties, conduction mechanisms and electroluminescence properties. Power efficiency was evaluated and studied in order to understand the relation between exciton recombination and electrical conduction. A band gap engineering method was proposed in order to better control carrier injection and light emission in order to enhance the electroluminescence power efficiency.

The power efficiency of silicon nanocrystal light-emitting devices were studied in alternating current regime. An experimental method based on impedance spectroscopy was proposed and an electrical model based on the constant phase element (CPE) was derived. It was, then, given a physical interpretation of the electrical model proposed by considering the disordered composition of the active material. The electrical model was further generalized for many kinds of waveforms applied and it was generalized for the direct current regime. Time-resolved electroluminescence and carrier injection in alternate current regime were presented.

Erbium implanted silicon rich oxide based devices were presented. The investigation of opto-electrical properties of LED in direct current and alternate current regime were studied in order to understand the injection mechanism and estimate the energy transfer between silicon nanocrystals and erbium. A device layout and process flow for an erbium doped silicon nanocrystal based laser structure were shown.

Some applications of silicon nanocrystal were presented. An example of all-silicon solar cell was shown. The photovoltaic properties and carrier transport of silicon nanocrystal based solar were studied. The combination of emitting and absorbing properties of silicon nanocrystal based LED were used to develop an all-silicon based optical transceiver.

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