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# EFFECT OF CHANNEL LENGTH VARIATION ON ANALOG AND RF PERFORMANCE OF JUNCTIONLESS DOUBLE GATE VERTICAL MOSFET

K. E. KAHARUDIN, F. SALEHUDDIN*,
A. S. M. ZAIN, AMEER F. ROSLAN

MiNE, Centre for Telecommunication Research and Innovation (CeTRI),
Faculty of Electronics and Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), Hang Tuah Jaya, Durian Tunggal, 76100 Melaka
*Corresponding Author: fauziyah@utem.edu.my

## Abstract

This paper investigates the effect of channel length ($L_{ch}$) variation upon analogue and radio frequency (RF) performance of Junctionless Double Gate Vertical MOSFET (JLDGVM). The study has been performed under the fixed level of process parameters by considering the dependence of analogue and RF properties on the channel length. Furthermore, this paper aims to give a comprehensive insight on possible improvement in the performance of analogue and RF of the JLDGVM device. The structure and characteristics of the device are developed and extracted respectively via 2D TCAD simulation. The results show that both transconductance generation factor (*TGF*) and transconductance ($g_m$) of the JLDGVM device are tremendously increased by 83% and 74% respectively as the scale of channel length is reduced from 12 nm to 9 nm. On the other hand, the unity gain cut-off frequency ($f_T$) and the gain-band-width product (*GBW*) tremendously improved by ~93% and ~74% respectively as the channel length of the device is scaled from 12 nm to 9 nm.

Keywords: Cut-off frequency, Gain-band-width product, Transconductance, Transconductance generation factor.

## 1. Introduction

Future nanoelectronic industries require an advanced fabrication of ultra-small components to be densely packed in a single chip, which demands an extreme miniaturisation of transistor sizes. Hence, it is crucial to provide fine solutions for this significant challenge in term of introducing new device structures and fabrication processes. For many years, an attempt to shrink the dimension of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) has been conducted to realize Moore's prediction, especially when the channel length ($L_{ch}$) is now being scaled down below ten-nanometer regime.

A traditional MOSFET's structure consists of two opposite type of junctions known as the P-N junctions. The distance between the PN junctions, commonly known as the effective channel length between the source and the drain region is isolated by the inverse type of dopant [1]. A conventional n-channel MOSFET normally utilizes n-type dopant (e.g., Arsenic) at a high concentration ($10^{18}$ to $10^{20}$ atom/cm$^3$) on the source/drain regions and p-type dopant (e.g., boron) at concentration range between $10^{14}$ to $10^{18}$ atom/cm$^3$ on the channel region [2]. Such formation requires extremely high doping concentration gradients, especially at the nano-scale regimes. Fabrication for this formation absolutely requires an extremely low thermal budget processing in order to avoid dopant redistribution, which would affect the device performance [3-6]. Lee et al. [7] mentioned that for instance, a commonly flash annealing methods employed to heat the silicon substrate for a very minimal period of time for reducing or even eliminating the diffusion, might not effectively agitate the ion implantation process in attaining a perfectly abrupt junction with extremely high concentration gradients. Thus, a lot of alternative device structures have been proposed in recent years to sort out the aforementioned issue.

Silicon-on-insulator (SOI) is one of the alternative formations that provide the full dielectric isolation, where its working principle relies on the accumulation-mode in which, the channel region employs similar polarity of the doping as the source/drain regions (junctionless). Junctionless configuration has been found to be implemented to most of SOI structures such as FinFETs, Multigate FETs, Gate-all-around FETs and etc. [8-10]. Another alternative structure for junctionless configuration is a fully depleted structure in which, the current conduction is totally based on bulk phenomena. Since the current conduction is a bulk phenomenon, the channel requires to be formed as thin as possible to allow the gate voltage to instantly switch off the device. In addition, the channel region of the fully depleted device must be highly doped in order to let the drain current saturates in a much faster rate. Junctionless configuration has also been applied to most of the fully depleted devices such as planar double-gate devices, vertical double-gate devices and nanowire devices [10-14].

A junctionless vertical transistor is one of the promising device structures, capable of lessening fabrication and performance issue related to the heavily doped junction. The vertical structure offers a wide range of scalability in which, the channel length ($L_{ch}$) can be scaled at the nano-meter regime without having a drastic deterioration in device performance. Scaling the transistor's dimension is a very crucial part in most of the transistor's structures. Basically, the geometrical and process parameters are the most important elements to be considered in the design consideration in which, their variation could contribute a significant impact on the

transistor characteristics. Carrier concentration ($N_A$) is one of the important parameters that decides the behaviour of a transistor. The magnitude of $N_A$ is commonly sourced from the ion implant parameters are known as channel doping ($N_{ch}$) and source/drain doping ($N_{sd}$). Besides, the variation of channel length and width are also important to determine the drain current ($I_D$) of a transistor. It increases linearly with the decrease of the physical channel length, which usually provides an improvement in the circuit speed.

Several previous reports on performance analysis of junctionless vertical double-gate MOSFET has been comprehensively studied in [14-16]. The study has revealed a significant insight into the performance boost in junctionless device compared to the conventional junction device, particularly in term of leakage behaviour. According to Rahul et al. [15], the results have shown that the off-state current ($I_{OFF}$) of the junctionless device was 600 times lower than the junction device at similar technology, mainly due to the elimination of the reverse p-n junction [15]. The impact of high-*k*/metal-gate integration on the performance of junctionless double-gate vertical MOSFET has also been conducted [14]. The results revealed that the on-state current ($I_{ON}$) was significantly increased by ~59% as the high-*k*/metal-gate integration was applied. Besides that, the impact of work function (*WF*) variation on $I_{ON}$ magnitude has also been observed in which, the device with a lower *WF* demonstrated a higher $I_{ON}$ magnitude [16].

However, the previous researches have not yet considered the impact of channel length variation on the device performance. Channel length ($L_{ch}$) is a critical parameter for most transistors as it decides the overall electrical performance. The shorter channel length is always desired in transistor's design because it could reduce the time taken for the transistor to turn from on-state to off-state or vice versa as the path for the current travels in the channel across the source/drain regions is minimized. However, the variation in the channel length is commonly associated with the device performance in term of DC and AC behaviours. Although it is accepted that junctionless configurations have contributed a positive impact on analogue and RF properties in previous researches [17-21], none have explored the effect of channel length ($L_{ch}$) variation, especially on the vertical structure. Therefore, this current research might contribute a significant insight on design consideration of junctionless vertical MOSFET, particularly in term of the impact of channel length variation on analogue and RF properties. In the next section, the effect of channel length variation on analogue and Radio Frequency (RF) performance of Junctionless Double Gate Vertical MOSFET (JLDGVM) will be comprehensively explored.

## 2. Device Model

Figure 1 depicts the structure of the recessed channel in the vertical transistor. Depending on bias conditions and the depletion width, the vertical ultrathin channel might be able to operate in full depletion mode. Computation of the depletion is needed with consideration of the carrier concentration ($N_A$) and the pillar thickness ($T_p$). The maximum depletion thickness under the gate can be measured as:

$$w_{d,\max} = \left( \frac{4\varepsilon_{si}\phi_{fp}}{q.N_A} \right)^{1/2} \tag{1}$$

where $q$ is the electronic charge, $\mathcal{E}_{si}$ is the permittivity of silicon and $\phi_{fp}$ is the surface potential. The surface potential ($\phi_{fp}$) for the maximum depletion can be measured as:

$$\phi_{fp} = V_T \ln\left(\frac{N_A}{N_i}\right) \tag{2}$$

where $V_T$ is thermal voltage and $N_i$ is the intrinsic silicon concentration. The magnitude of $N_A$ plays a crucial role in tuning the magnitude of threshold voltage ($V_{TH}$).

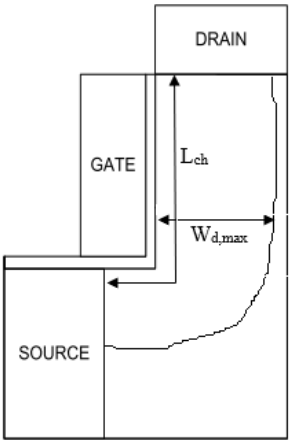


**Fig. 1. Structure of recessed channel in vertical transistor.**

For the *n*-channel transistor, the implantation of the positive ions lowers the $V_{TH}$ magnitude while the implantation of the negative ions increases the $V_{TH}$ magnitude. The $V_{TH}$ of the vertical channel transistor can be mathematically described as:

$$V_{TH} = 2\phi_{fp} + \frac{\sqrt{2\varepsilon_{Si} q N_A 2\phi_{fp}}}{C_{ox}} + V_{fb} \tag{3}$$

where,

$$V_{fb} = \phi_{ms} - \frac{Q_{fc}}{C_{ox}} \tag{4}$$

where $\phi_b$ is the bulk potential, $\varepsilon_{Si}$ is the permittivity of the silicon ($1.06 \times 10^{-12}$ Farads/cm), $C_{ox}$ is the gate-oxide capacitance, $Q_{fc}$ represents the fixed charge due to imperfections in the silicon-oxide interface and doping, $\phi_{ms}$ is the work function difference between the gate material and silicon substrate ($\phi_{gate}$-$\phi_{Si}$), $N_A$ is the density of the carriers in doped device substrate, $N_i$ is the carrier concentration of intrinsic (undoped) silicon ($1.45 \times 10^{10}$ $cm^{-3}$ at 300 $^oK$). Similar with the conventional MOSFET, the drain current ($I_D$) of the vertical transistor can be measured as:

$$I_D = \frac{W_{d,\max}}{L_{ch}} \mu C_{ox} (V_G - V_{TH}) V_D \tag{5}$$

where $W_{d,max}$ is the maximum depletion width, $L_{ch}$ is the effective channel length, $\mu$ is the carrier mobility in the channel (assumed constant here), $V_G$ is the gate voltage, and $V_D$ is the drain voltage and $V_{TH}$ is the threshold voltage.

## 3. Device Structure and Simulation

The schematic 2D view of a junctionless double-gate vertical MOSFET (JLDGVM) is depicted in Fig. 2. The $L_{ch}$ of the symmetric device is scaled between 9 nm to 12 nm. The silicon substrate is etched to form an ultrathin vertical pillar with 9 nm of a thickness ($T_p$). The ultrathin pillar of the device would raise the package density, could avoid the lithography limitation, and open alternative approaches for optimizing the doping profile with multiple levels of pillar thickness and doping concentrations. The vertical pillar is sandwiched by two symmetrical metal gates (tungsten silicide) that would enhance the gate control over the channel [22, 23].

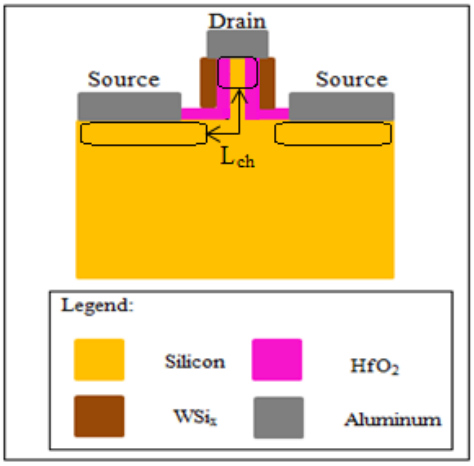


**Fig. 2. Schematic cross-sectional structure of JLDGVM device.**

A channel region for the n-channel device is heavily doped with $1x10^{18}$ atom/cm$^3$ of arsenic dose. Similarly, the source/drain (S/D) regions for the *n*-channel device are also heavily doped with $1 \times 10^{18}$ atom/cm$^3$ of arsenic dose in order to form $n^+$ $n^+$ $n^+$ configuration (junctionless). A similar type of dopant is employed for the channel and S/D regions in order to completely eliminate the gradient of doping concentration so that no diffusion would take place, which indirectly neglects the need for costly ultrafast annealing processes and opens the possibility of device fabrication with shorter channels [1]. The proposed structure utilizes hafnium dioxide ($HfO_2$) as the high-*k* dielectric. The $HfO_2$ insulator has been paired with metal-gate in various transistor structures, exhibiting a significant boost in drain current [24-28]. Application of metal-gate technology is very crucial to avoid poly-gate depletion effect associated with degradation of electrical performance. Using correct metal-gate work function, the desired threshold voltage ($V_{TH}$) can be achieved and the mobility degradation issue would be alleviated. Table 1 lists the detailed geometrical and process parameter used in the simulated n-channel devices. The $L_{ch}$ acts as a tunable variable in order to study its impact on

the analog and RF performance of the device while the other variables are remained at a constant magnitude.

**Table 1. Parameters used in simulated JLDGVMs.**

| Variables | Units | Value |
|---|---|---|
| **Channel length, $L_{ch}$** | nm | 9-12 |
| **Pillar thickness, $T_p$** | nm | 9 |
| **Channel doping, $N_{ch}$** | Atom/cm$^3$ | 1.0E18 |
| **S/D doping, $N_{sd}$** | Atom/cm$^3$ | 1.0E18 |
| **Metal work-function, *WF*** | eV | 4.5 |

The 2D ATLAS simulator [29] is used to simulate the electrical characteristics for both n-channel JLDGVM devices. The ATLAS module of Silvaco is a physically-based two and three-dimensional device simulator, which capable of predicting the electrical characteristics of specified device structures and provides a detailed insight into the internal physical structure associated with the device operation.

The device structure is used as an input by the ATLAS module in which, the electrical characteristics of the device will be predicted and associated with the specified bias condition. Therefore, it is possible to link simulation very closely to technology development, resulting in many benefits from the use of simulation. For this study, the drain bias is fixed at $V_D$ = 0.5 V and the analogue and RF performance are analyzed with a variable gate voltage ($V_G$), ranging from 0 to 1 V.

The performance analysis of analogue and RF behaviours of the JLDGVM device is conducted with $V_D$ = 0.5 V in order to comprehensively investigate the subthreshold behaviors. The threshold voltage ($V_{TH}$) is extracted from the $I_D$–$V_G$ transfer curve at $V_D$ = 0.5 V. The $V_{TH}$ is then utilized to compute the gate overdrive voltage ($V_{GT}$), which is represented as:

$$V_{GT} = V_{GS} - V_{TH} \tag{6}$$

The analysis of analogue and RF performance in the JLDGVM devices includes the mobility degradation within the channel region suffered due to higher surface scattering near the silicon to the high-*k* dielectric interface. Hence, the device simulation utilizes the Lombardi CVT and temperature mobility model in order to accurately analyze the JLDGVM's behaviours.

The implementation of the Shockley–Read–Hall Recombination (SRH) model meanwhile is to contemplate on the phonon transition effects in extracting the off-state current ($I_{OFF}$).

The simulation requires an accurate prediction of the electrical properties of JLDGVM devices, including the quantum effects. The quantum drift-diffusion models are considered as carrier transport of the JLDGVM devices to magnify the accuracy of extracted electrical properties, especially when the channel is scaled below 20 nm of length.

Figure 3 depicts the doping profile across the JLDGVM device, displaying the net doping for silicon, hafnium dioxide, tungsten silicide and aluminium.

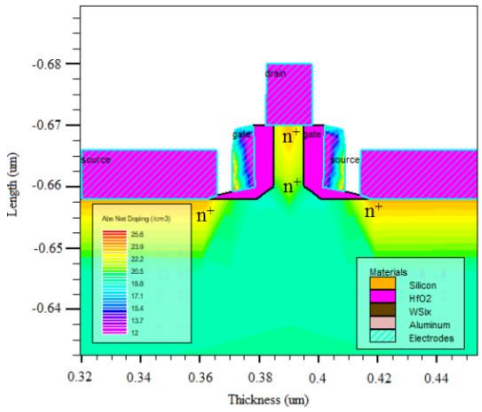


**Fig. 3. Contour mode of JLDGVM layout.**

## 4. Results and Discussion

The $I_D$-$V_G$ transfer characteristics in a linear scale for n-channel JLDGVM device is shown in Fig. 4. It shows the impact of different channel length ($L_{ch}$) on the $I_D$ response curves at $V_D$ = 0.5 V as the gate voltage ($V_G$) is shifted from 0 V to 1 V. From the curves, it is observed that $I_D$ magnitude of the n-JLVDGM is significantly increased by ~68% as the $L_{ch}$ is reduced from 12 nm to 9 nm. The shorter channel length improves the current flow due to less resistance in the channel region. In the junctionless configuration, the peak majority carrier concentration coincides with the channel region that has the lowest electric field. Once the channel is reduced in length, the junctionless configuration of vertical structure would result in much higher on-state current ($I_{ON}$) than the inversion-mode. The decrease of the carrier's mobility in junctionless-mode is less pronounced due to lower electric field perpendicular to the current flow.

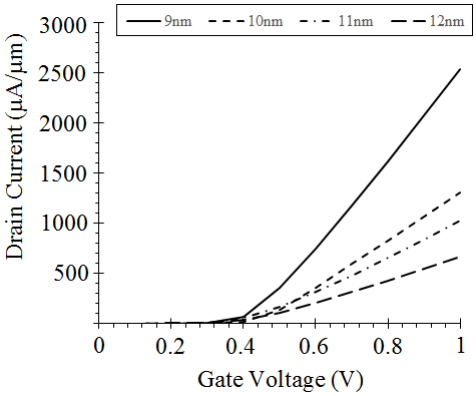


**Fig. 4. Drain current ($I_D$) vs. gate voltage ($V_G$) at drain voltage ($V_D$=0.5V).**

### 4.1. Analogue performance

The most crucial characteristics for analogue have been simulated via Atlas Silvaco software namely in $g_m$ and *TGF* as well as output conductance ($g_d$) and early voltage

($V_{EA}$) in order to analyze the analogue performance of JLDGVM device. The transconductance of the JLDGVM device is very important for measuring the amplifier's gain, which is mathematically denoted as:

$$g_m = \frac{\partial I_D}{\partial V_G} \tag{7}$$

If the size of the interval approaches zero, the change in gate voltage would deliberately reduce, thus, the value of $\partial I_D / \partial V_G$ approaches the slope of the tangent to the curve of a certain point. The slope of this line represents the theoretical transconductance of a FET for a certain input of $V_g$ and $I_D$. A higher transconductance of the device implies that the channel has higher transport efficiency, which could be opted for analogue applications. On the other hand, the *TGF* implies how effective the $I_D$ for achieving a suitable magnitude of the $g_m$. A higher magnitude of *TGF* is anticipated in order to design analogue circuits, especially for low power operation. The *TGF* of JLDGVM device is mathematically expressed as:

$$TGF = \frac{g_m}{I_D} \tag{8}$$

A combined plot of $g_m$ and *TGF* as a function of $V_{GT}$ is depicted in Fig. 5. It is shown that the JLDGVM device with 9 nm of channel length demonstrates the highest *TGF* and transconductance. The *TGF* and transconductance ($g_m$) of the JLDGVM device are tremendously increased by 83% and 74% respectively as the channel length is scaled from 12 nm to 9 nm.

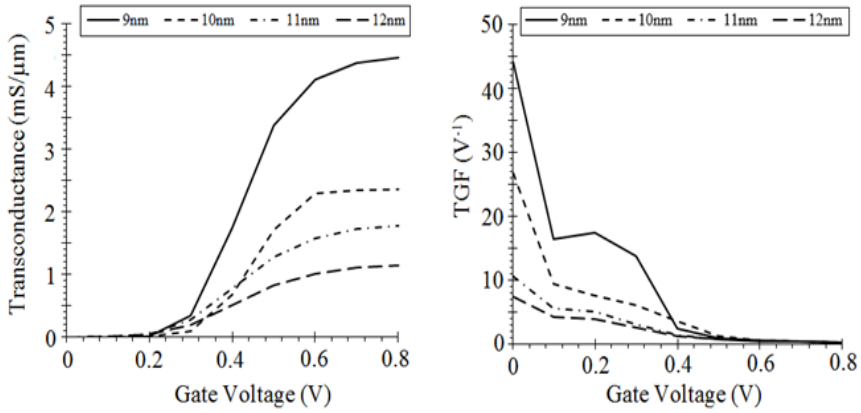


**Fig. 5. Transconductance ($g_m$) and Transconductance Generation Factor (*TGF*) as a function of gate overdrive voltage ($V_{GT}$).**

The highest *TGF* and $g_m$ are exhibited by the device with 9 nm of channel length, which are measured at 44 $V^{-1}$ and 4.46 mS/$\mu$m respectively. The improvement in transconductance is mainly due to tunnelling volume in the channel. This implies that the reduction in channel length could tremendously improve the transconductance of JLDGVM device. The ideal magnitude of *TGF* is normally restricted to approximately 40 $V^{-1}$ at minimum subthreshold slope of 60 mV/decade.

The *TGF*'s disparity presents at the subthreshold region of device operation for all the investigated channel length. The $g_m/I_D$ ratio of the device is observed to be increased as the channel length being decreased. Thus, the channel length of the device should be carefully scaled as an extremely high *TGF* does not quite applicable for high linearity microwave systems. Pradhan et al. [30] mentioned that on the other hands, a lower *TGF* would not be a major disadvantage from the time when the power intake in the subthreshold region is extremely small. The output conductance ($g_d$) is an important parameter that determines the performance of JLDGVM devices in analogue circuits. In most of the bulk devices, impact ionization effects (e.g., kink effect, parasitic bipolar action) could not be avoided, which would eventually result in the degradation of output conductance ($g_d$) [31]. Therefore, a fully-depleted device is used to minimize this degradation. From the perspective of vertical MOSFET, a fully depleted configuration can be realized by having an ultrathin pillar ($T_p$ = 9 nm) that is sandwiched by two side gates. The output conductance ($g_d$) of JLDGVM device is calculated as:

$$g_d = \frac{\partial I_D}{\partial V_D} \tag{9}$$

Figure 6 depicts the plot of $g_d$ for the *n*-JLDGVM device as a function of drain voltage ($V_D$). It shows the effect of increasing drain voltage on output conductance ($g_d$) for n-JLDGVM device and it is observed that the device with 9 nm of channel length demonstrates the highest $g_d$ at a maximum drain voltage of 1 V.

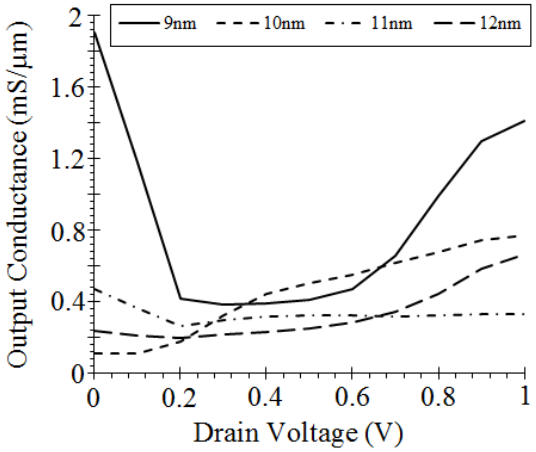


**Fig. 6. Output conductance ($g_d$) as a function of drain voltage ($V_D$).**

CMOS analogue circuits require a very low $g_d$ to acquire the high gain, in which, higher $g_d$ implies the channel has low output resistance, which subsequently magnifies the $I_D$ against $V_D$ particularly in the saturation region. Furthermore, a low $g_d$ could provide a significant boost in the drain current ($I_d$) to output conductance ($g_d$) ratio, known as early voltage ($V_{EA}$). The $V_{EA}$ is mathematically expressed as:

$$V_{EA} = \frac{I_D}{g_d} \tag{10}$$

Figure 7 depicts the disparity of $V_{EA}$ as a function of d $V_D$. The device with 11 nm of channel length exhibits the highest early voltage at maximum drain current. It is observed that the devices with 10 nm and 11 nm of channel length demonstrate a linear rise on the early voltage ($V_{EA}$) as the drain voltage is increased from 0 V to 1 V. Table 2 summarizes the magnitude of analogue performance (*TGF*, $g_m$, $g_d$ and $V_{EA}$) for different channel length.

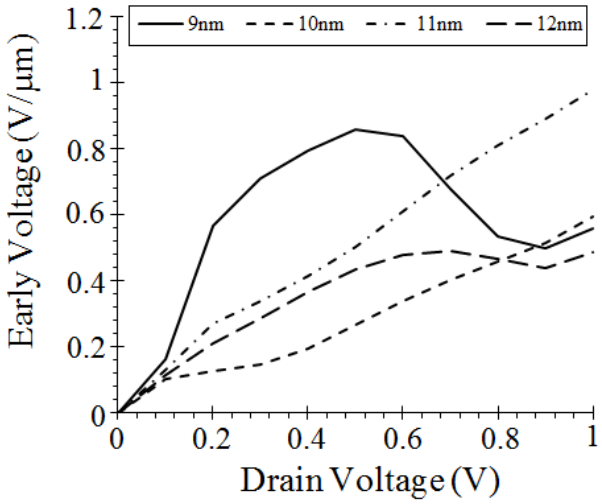


**Fig. 7. Early voltage ($V_{EA}$) as a function of drain voltage ($V_D$).**

**Table 2. *TGF*, $g_m$, $g_d$ and $V_{EA}$ for different channel length.**

| Characteristics | Units | Channel length, $L_{ch}$ | | | |
|---|---|---|---|---|---|
| | | 9 nm | 10 nm | 11 nm | 12 nm |
| ***TGF*** | $V^{-1}$ | 44 | 26.7 | 10.6 | 7.5 |
| $g_m$ | mS/$\mu$m | 4.46 | 2.35 | 1.77 | 1.14 |
| $g_d$ | mS/$\mu$m | 1.41 | 0.77 | 0.33 | 0.66 |
| $V_{EA}$ | V/$\mu$m | 0.56 | 0.59 | 0.98 | 0.49 |

## 4.2. RF Performance

The significance of high frequency (RF) parameters in JLDGVM device includes gate-to-source capacitance (Cgs), gate-to-drain (Cgd), parasitic capacitance (Cgg), intrinsic gate delay (τint), dynamic power dissipation (Pdyn), cut-off frequency (FT) and gain-bandwidth product (GBW). The curves in Figs. 8 and 9 depict both Cgs and Cgd as a function of VGT for subthreshold regime respectively. The intrinsic capacitances are extracted via small-signal analysis after DC analysis. The capacitances between regions are computed by a single AC frequency (f) of 1 MHz as the gate overdrive voltage (VGT) is shifted with 0.01 V of step from 0 V to 1 V.

Based on Fig. 8, the $C_{gs}$ for the devices with 10 nm, 11 nm and 12 nm channel length are almost constant as the $V_{GT}$ is swept from 0 V to 0.8 V. However, the device with 10 nm of channel length exhibits a slight increase in $C_{gs}$ as the $V_{GT}$ reaches 0.3 V. Such occurrence is mainly caused by the presence of the density of fringing field in short channel device [32]. The device with 9 nm of channel length

demonstrates the lowest $C_{gs}$ magnitude, substantially due to much weaker capacitive coupling between the gate region and the source region.

From Fig. 9, it is observed that all the channel lengths demonstrate a significant decrease in $C_{gd}$ as the $V_{GT}$ is swept from 0 V to 0.8 V. The $C_{gd}$ value should be a decline, approaching zero as the drain current enters the saturation regime. The device with 9 nm of channel length exhibits a sharp decline in $C_{gd}$ value, implying a significant increase in the saturated drain current. Based on the plot for both $C_{gs}$ and $C_{gd}$, it can be seen that the variation in channel length does not significantly decide the magnitude of the intrinsic capacitances as it has been dominantly influenced by the fringing field between gate and source/drain region. The parasitic gate capacitance ($C_{gg}$) is also a crucial AC parameter to be considered as it significantly influences the propagation delay of the device. Figure 10 depicts the plot of the parasitic gate capacitance ($C_{gg}$) as a function of $V_{GT}$.

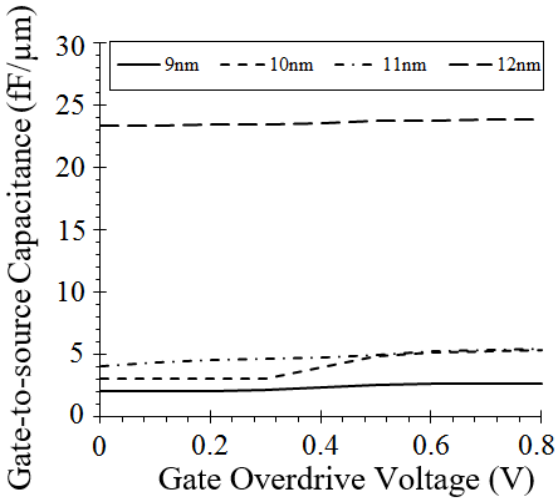


**Fig. 8. Gate-to-source capacitance ($C_{gs}$) as a function of $V_{GT}$.**

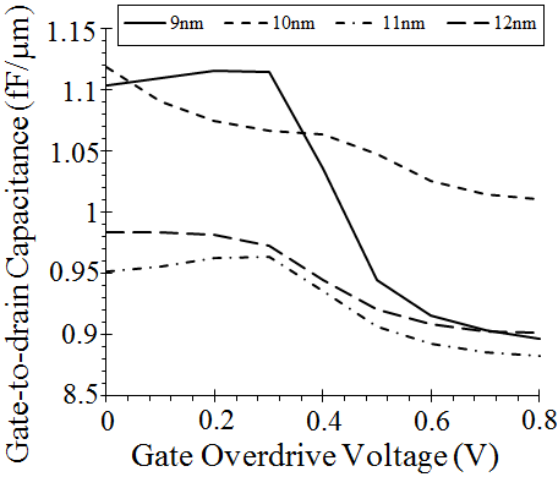


**Fig. 9. Gate-to-drain capacitance ($C_{gd}$) as a function of $V_{GT}$.**

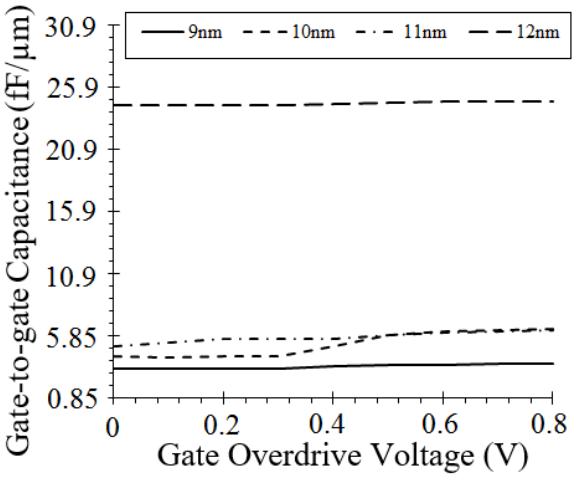


**Fig. 10. Gate-to-gate capacitance as a function of $V_{GT}$.**

It is observed that the device with 12 nm of channel length exhibits the highest $C_{gg}$ value among others. An extremely large $C_{gg}$ magnitude would contribute a significant rise in intrinsic gate delay. The intrinsic gate delay is used to indicate the limit of the frequency of the JLDGVM device. It significantly relies on the magnitude of both drain current ($I_D$) and parasitic gate capacitance ($C_{gg}$), which can be mathematically expressed as:

$$\tau_{\text{int}} = \frac{C_{gg} \times V_{DD}}{I_D} \tag{11}$$

where, $\tau_{int}$ represents the intrinsic gate delay. Figure 11 depicts the plot for the $\tau_{int}$ as a function of $V_D$.

Based on Fig. 11, it is clearly shown that the device with 9 nm of channel length has the lowest intrinsic gate delay as the drain voltage is shifted from 0V to 1V. Since the magnitude of drain current is quite large compared to $C_{gg}$ magnitude, the variation of drain current plays a dominant role in influencing the intrinsic gate delay. Besides that, dynamic power dissipation ($P_{dyn}$) is also a crucial AC characteristic for transient analysis of the JLDGVM device. The dynamic power dissipation can be calculated as:

$$P_{dyn} = C_{gg} V_{DD}{}^2 f \tag{12}$$

for which, $f$ is representing the operating frequency and $P_{dyn}$ represents the dynamic power dissipation. Figure 12 depicts the plot of dynamic power dissipation as a function of $V_D$ for JLDGVM device.

The device with 12 nm of channel length demonstrates the highest power dissipation among the others as the drain voltage is swept from 0 V to 1 V. The devices with 9 nm and 10 nm of channel length exhibit almost the similar rate of dynamic power dissipation as the drain current increases. Since the AC frequency is kept at a constant magnitude, the $P_{dyn}$ is directly controlled by the $C_{gg}$ and $V_{DD}$ magnitude. In this case, the device with 9 nm of channel length exhibits the lowest $P_{dyn}$ because it has the lowest parasitic capacitance compared to others. Based on

studies by Sharma and Bucher [33], it is very important to keep the dynamic power dissipation of JLDGVM device as low as possible in order to avoid any significant rise in temperature that could influence the device performance either in "OFF" or "ON" condition.

The RF performance of JLDGVM device analysis heavily relies on the cut-off frequency ($f_T$) as an important parameter. Fundamentally, $f_T$ is the frequency while the unity is achieved at the current gain and it is mathematically defined as:

$$f_T = \frac{g_m}{2\pi(C_{gg})} \tag{13}$$

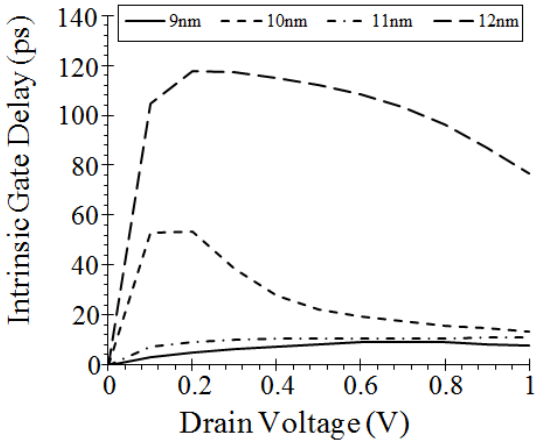


**Fig. 11. Intrinsic gate delay as a function of drain voltage.**

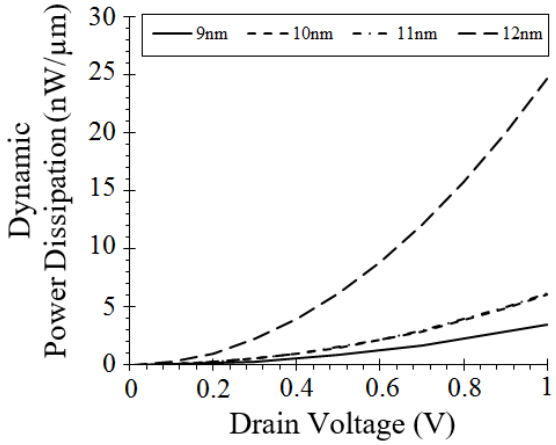


**Fig. 12. Dynamic power dissipation as a function of drain voltage.**

Figure 13 represents $f_T$ for JLDGVM device as a function of $V_G$ at $V_D$ of 0.5 V. It shows that the unity gain cut-off frequency ($f_T$) for JLDGVM device could boost up to approximately 93% as the reduction of the channel length scale is reduced from 12 nm to 9 nm, shifting the $f_T$-$V_G$ characteristics to maximum gate voltage. The distinctive improvement in the magnitude of $f_T$ for JLDGVM device with 9 nm

of channel length is mainly influenced by its high transconductance and low parasitic capacitance. The high $f_T$ is desirable for high-speed operation of numerous RF applications. For the purpose of high-frequency transient analysis, the gain-band-width product (*GBW*) is considered and calculated as:

$$GBW = \frac{g_m}{2\pi(C_{gd})} \tag{14}$$

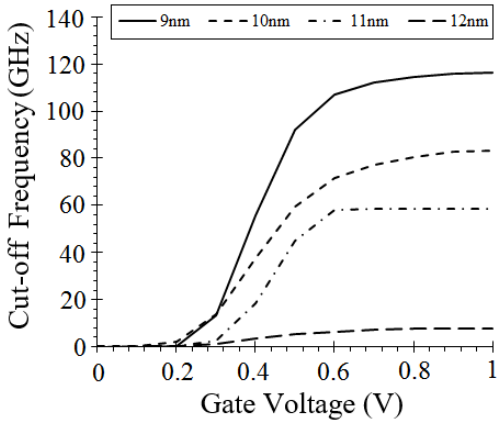


**Fig. 13. Unity gain cut-off frequency ($f_T$) as a function of gate voltage.**

Figure 14 depicts the *GBW* as a function of the $V_G$ at $V_D$ of 0.5V. The *GBW* for JLDGVM device could be increased by approximately 74% as the scale of the channel length is reduced from 12 nm to 9 nm, shifting the *GBW*-$V_G$ characteristics towards maximum gate voltage. The distinctive improvement of *GBW* observed in JLDGVM device with 9 nm of channel length is explicitly affected by high transconductance and tremendous decline of $C_{gd}$ as it is approaching the maximum gate voltage. The device with high *GBW* is suitable for low bias and high-speed applications such as RF amplifiers. Table 3 summarizes the magnitude of RF performance ($C_{gs}$, $C_{gd}$, $C_{gg}$, $\tau_{int}$, $P_{dyn}$, $f_t$ and *GBW*) for different channel length.

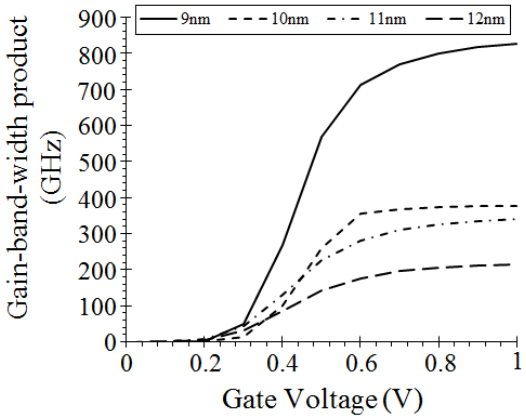


**Fig. 14. Gain-band-width product (*GBW*) as a function of gate voltage.**

**Table 3. $C_{gs}$, $C_{gd}$, $C_{gg}$, $\tau_{int}$, $P_{dyn}$, $f_t$ and *GBW* for different channel length.**

| Characteristics | Units | Channel length, $L_{ch}$ | | | |
|---|---|---|---|---|---|
| | | 9 nm | 10 nm | 11 nm | 12 nm |
| $C_{gs}$ | fF | 2.68 | 5.36 | 5.43 | 23.8 |
| $C_{gd}$ | fF | 0.9 | 1.01 | 0.88 | 0.9 |
| $C_{gg}$ | fF | 3.58 | 6.37 | 6.31 | 24.7 |
| $\tau_{int}$ | ps | 7.7 | 13.5 | 10.8 | 76.9 |
| $P_{dyn}$ | nW | 3.5 | 6 | 6.2 | 24.7 |
| $f_t$ | GHz | 116.4 | 83.3 | 58.6 | 7.9 |
| *GBW* | GHz | 825.1 | 376.5 | 339.8 | 214.8 |

From the observation, it can be concluded that the device with 9 nm of channel length has demonstrated good and acceptable analogue and RF performance compared to others. It has the lowest intrinsic gate delay, which is essential for data propagation from the input gate to the output. It also has exhibited the highest *ft* and *GBW*, which is very suitable for high-frequency RF application. On top of that, the device with 9 nm of channel length exhibits the highest $I_{ON}$ magnitude measured at 2534.2 $\mu$A/$\mu$m (refer to Fig. 4), which is very desirable for the high speed switching operation. Several electrical characteristics of different junctionless device structures [34] have been compared to some of the results of the current study as shown in Fig. 15.

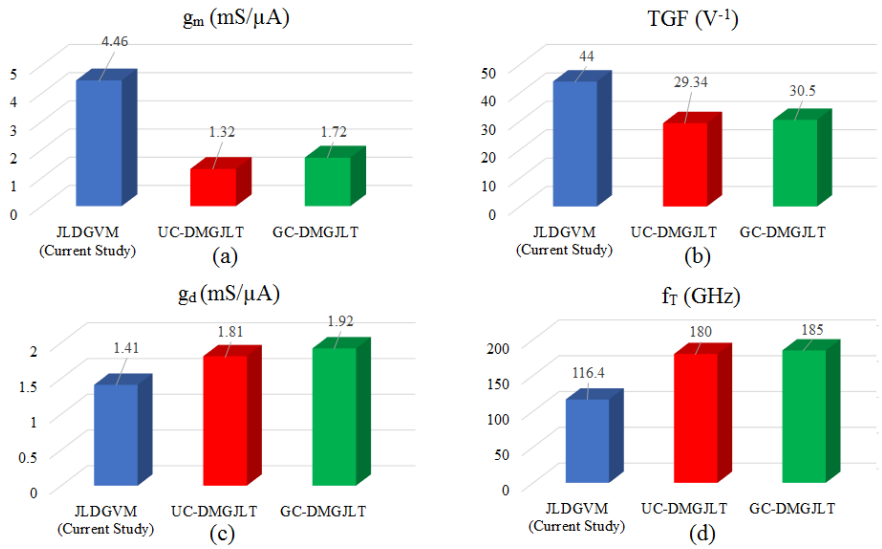


**Fig. 15. Benchmark of junctionless double gate vertical MOSFET (JLDGVM) with uniform channel dual material gate junctionless transistor (UC-DMGJLT) and graded channel dual material gate junctionless transistor (GC-DMGJLT) for a) $g_m$, b) *TGF*, c) $g_d$, d) $f_T$.**

The JLDGVM device has exhibited the highest magnitude of $g_m$ and *TGF* compared to other junctionless architectures, owing to its high saturated drain current. However, the device experiences degradation in $g_d$ and $f_T$ magnitude compared to others. A slight degradation in $g_d$ magnitude is mainly due to the larger

drain current variation with a drain voltage variation at constant gate voltage. Both UC-DMGJLT and GC-DMGJLT have demonstrated higher $f_T$ magnitude, probably due to its higher intrinsic capacitance that totally governs the $f_T$ over their lower $g_m$ magnitudes. The analogue and RF performance of the JLDGVM have also been compared to different double-gate transistor technologies (e.g., dual material, graded channel dual material and gate stack) as summarized in Table 4.

**Table 4. Benchmark of analogue and RF performance with different double-gate transistor technologies.**

| Device | $g_m$ (mS/$\mu$m) | *TGF* ($V^{-1}$) | $g_d$ (mS/$\mu$m) | $V_{EA}$ (V/$\mu$m) | $f_t$ (GHz) |
|---|---|---|---|---|---|
| **Mohapatra et al. [35] GS-DG-M** | 2.56 | 39.395 | 0.035 | 9.71 | 547 |
| **Mohapatra et al. [36] SM-GS-DG** | 3.40 | 39.514 | 0.007 | 6.175 | 286.75 |
| **Mohapatra et al. [36] DM-GS-DG** | 3.63 | 37.328 | 0.003 | 11.82 | 425.91 |
| **Mohapatra et al. [36] DM-SH-GS-DG** | 3.57 | 35.757 | 0.0015 | 13.82 | 421.33 |
| **Sharma, and Bucher [37] DG** | 2.44 | 12.7 | n/a | 1.39 | 476 |
| **Sharma, and Bucher [37]** DMDG | 2.19 | 13.5 | n/a | 1.5 | 439 |
| **Sharma, and Bucher [37]** GCDG | 2.91 | 13.4 | n/a | 1.14 | 546 |
| **Sharma, and Bucher [37]** GCDMDG | 2.79 | 14.1 | n/a | 1.27 | 534 |
| **JLDGVM (Current work)** | 4.46 | 44 | 1.41 | 0.56 | 116.4 |

Based on Table 4, the analogue performance such as *TGF*, $g_m$ and $g_d$ of JLDGVM device are much higher than the rest of double-gate transistor technologies, implying the device has faster on-off switching transition. The JLDGVM device also exhibits the lowest $V_{EA}$ compared to others, implying that the device only experiences a smaller early effect, which would subsequently result in higher drain current. In term of RF performance, the JLDGVM device exhibits the lowest $f_T$ magnitude compared to other technologies. However, the $f_T$ of the device might be increased by reducing the channel length in accordance with the trend depicted in Fig. 13. The channel length variation seems to be very sensitive to the JLDGVM analogue and RF behaviours. For instance, as the channel length increases to 12 nm, the device suffers severe deterioration in transconductance, intrinsic gate delay, dynamic power consumption and cut-off frequency. Furthermore, some of the analogue and RF parameters demonstrates inconsistent behaviours as the channel length is further downscaled. For that reason, it can be concluded the channel length variation is not the only parameter that causes the fluctuations in analogue and RF performances of JLDGVM device. Other input parameters such as channel doping, source/drain doping, metal-gate work function, high-*k* material, pillar thickness should be considered for further investigation. Hence, various optimization methods could be applied [38-43] to minimize the variation of multiple input parameters in achieving the improved JLDGVM's analogue and RF performance.

## 5. Conclusions

In summary, the effect of channel length variation on analogue and RF performance of Junctionless Double Gate Vertical MOSFET (JLDGVM) were comprehensively investigated by using 2-D process (Athena) and device (Atlas) simulator. The Lombardi CVT and temperature mobility model were utilized for transport device simulation to measure the delay and power dissipation performance. The JLDGVM properties comprised a number of important analogue and RF parameters such as transconductance, output conductance, early voltage, reduced propagation delay, dynamic power dissipation, cut-off frequency and gain-band-width product. The results showed the reduction in channel length of JLDGVM device did improve the transconductance, cut-off frequency and gain-band-width product. However, it was assumed that the channel length was not the only input parameter that caused the uncertainty fluctuation in most of the analogue and RF performances. Hence, for future work, more input parameters besides channel length will be optimized by using appropriate statistical methods for robust analogue and RF performance. Based on the overall results, it is concluded that the JLDGVM device can be regarded as a potential type of transistor suitable for low power and high-frequency applications.

## Nomenclatures

| | |
|---|---|
| $C_{gd}$ | Gate-to-drain capacitance, $fF/\mu$m |
| $C_{gg}$ | Gate-to-gate capacitance, $fF/\mu$m |
| $C_{gs}$ | Gate-to-source capacitance, $fF/\mu$m |
| $C_{ox}$ | Gate-oxide capacitance, $fF/\mu$m |
| $f$ | Frequency, MHz |
| $f_T$ | Cut-off frequency, GHz |
| $g_d$ | Output conductance, mS/$\mu$m |
| $g_m$ | Transconductance, mS/$\mu$m |
| $HfO_2$ | Hafnium dioxide |
| $I_{OFF}$ | Off-state current, A/$\mu$m |
| $I_{ON}$ | On-state current, A/$\mu$m |
| $L_{ch}$ | Channel length, nm |
| $N_A$ | Carrier concentration, atom/cm$^{-3}$ |
| $N_{ch}$ | Channel doping, atom/cm$^{-3}$ |
| $N_i$ | Intrinsic silicon concentration, atom/cm |
| $N_{sd}$ | Source/drain doping, atom/cm$^{-3}$ |
| $P_{dyn}$ | Dynamic power dissipation, watt/$\mu$m |
| $Q_{fc}$ | Fixed charge due to imperfections in the silicon-oxide interface and doping |
| $q$ | Electronic charge |
| $T_p$ | Pillar thickness, nm |
| $V_D$ | Drain voltage, V |
| $V_{DD}$ | Supply voltage, V |
| $V_{EA}$ | Early voltage, V |
| $V_{fb}$ | Flat band voltage, V |
| $V_G$ | Gate voltage, V |
| $V_{GT}$ | Gate overdrive voltage, V |
| $V_T$ | Thermal voltage, V |
| $V_{TH}$ | Threshold voltage, V |

| | |
|---|---|
| $W_{d,max}$ | Maximum depletion thickness, $\mu$m |
| $WSi_x$ | Tungsten silicide |

***Greek Symbols***

| | |
|---|---|
| $\tau_{int}$ | Intrinsic gate delay, ps |
| $\phi_{fp}$ | Permittivity of silicon |
| $\phi_{ms}$ | Surface potential |
| | Workfunction difference between the gate material and silicon substrate |
| $\mu$ | Carrier mobility |

**Abbreviations**

| | |
|---|---|
| AC | Alternate Current |
| DC | Direct Current |
| FET | Field Effect Transistor |
| GBW | Gain-Band-Width Product |
| JLDGVM | Junctionless Double Gate Vertical MOSFET |
| MOSFET | Metal-Oxide-Semiconductor Field Effect Transistor |
| RF | Radio Frequency |
| S/D | Source/Drain |
| SOI | Silicon-on-Insulator |
| TGF | Transconductance Generation Factor |
| WF | Work Function |

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