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Design of Peak Current Mode Synchronous Buck DC-DC Converter

Mao Fan[1*], Shuzhuan He[2], Baoning Zhang[2]

[1]Nanjing Ningkey Intelligent Computing Chip Research Institute of Nanjing University, Nanjing 210000, China.
E-mail: fanm@ningkey.cn

[2]VLSI Design Institute, Nanjing University, Nanjing 210000, China

Abstract: In this article, a design scheme of peak current mode synchronous buck DC-DC converter is proposed based on synchronous rectification technology. The specific design scheme of the DC-DC converter is described from the overall structure design of control circuit, key circuit design and slope compensation. At the same time, the whole circuit simulation analysis of the DC-DC converter shows that the DC-DC converter has high performance.

Keywords: Peak Current Mode; DC-DC Converter; Slope Compensation

1. Introduction

For DC-DC converter, it has the advantages of high integration, smaller ripple and more stable output power, so it is widely used in a variety of portable electronic devices. From the point of view of portable electronic devices, the requirements for power supply are more stringent, and higher conversion efficiency is required, which promotes the service life of batteries. Therefore, it is necessary to design a peak current mode synchronous buck DC-DC converter with low power consumption and high conversion efficiency.

2. Design of peak current mode synchronous buck DC-DC converter

2.1 Overall structure design of control circuit

In the design of this DC-DC converter, the synchronous rectifier switch is mainly introduced. The main functional modules are: pulse width modulation comparator, pulse frequency modulation comparator, oscillator, current sampling circuit, slope compensation circuit, soft start circuit, error amplifier, reference voltage source, pulse width modulation control logic and power transistor driving circuit. The overall structure block diagram of the DC-DC converter control circuit is as follows.

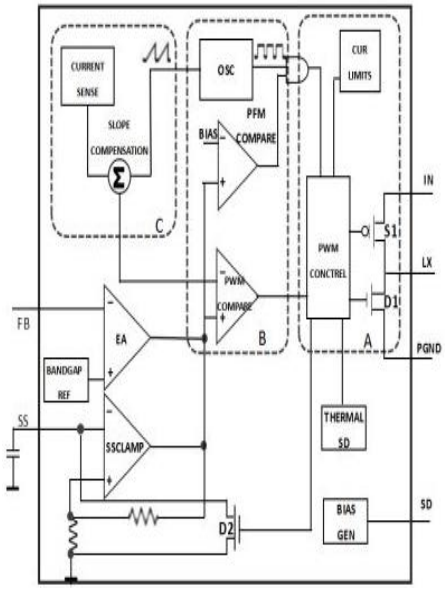

Figure 1. Overall structure of control circuit of peak current mode synchronous buck DC-DC converter.

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Among them, S1 represents the main power switch; N1 represents the synchronous distillation switch; IN represents the input voltage; SS connection soft start capacitor; FB represents the input end of output voltage feedback signal; LX connector external filter inductance[1].

The operation flow of the DC-DC converter is as follows: under normal working conditions, the clock signal generated by the internal oscillator will trigger trigger the trigger RS in any period to make the main power switch turn on, and the power supply can output current to the external inductor under the support of the main switch; the current sampling circuit enters the current sampling working state and inputs the slope compensation in the form of voltage. At this time, the output voltage is compared with the peak value modulation of RS, and the output voltage is compensated when the current reaches the peak value. The peak current threshold of the inductor is set.

In the actual operation process, if the load of the chip increases, the feedback voltage signal will decrease, which makes the output of the error amplifier increase and the peak current threshold increase until the new load current matches the average inductance current. When the main power switch is turned off, the synchronous rectifier switch will conduct freewheeling. When the next clock cycle comes, or when the zero current comparator detects that the inductance current is reversed, the freewheeling will stop.

2.2 Key circuit design

2.2.1 Design of pulse width modulator with frequency hopping function

In the key circuit of this DC-DC converter, the structure of pulse width modulator with frequency hopping function is shown in the Figure below. The main modules include pulse width modulation comparator, pulse frequency modulation comparator and oscillator. Under the condition of light load or heavy load, the modulator can be regarded as an ordinary single edge pulse width modulator; under the condition of extremely light load or no load, the main operation mode of the modulator is frequency hopping mode.

Pulse width modulation comparator is an important structure module in this DC-DC converter. Its circuit structure is shown in **Figure 3.** In general, the pulse width modulation comparator is mainly composed of inverter, MOS tube M8 and M9. In the actual operation process, when the VCONTROL is at low level, the gates of m4-m7, M13 and M13 are pulled to the low-level state, prompting the comparator to stop running; when the VCONTROL is at high level, the comparator operates normally[2].

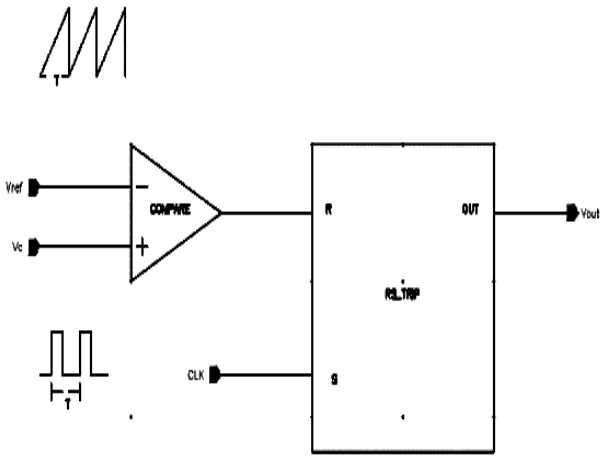

Figure 2. Structure of pulse width modulator with frequency hopping function under light load**.**

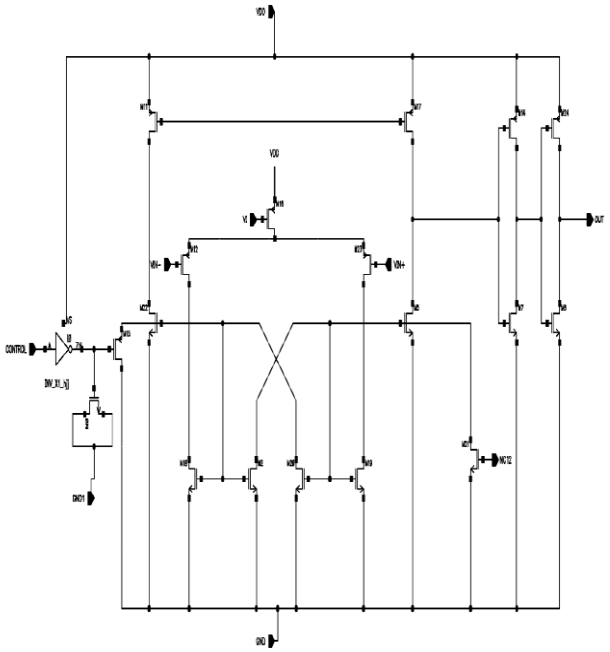

Figure 3. Circuit structure of pulse width modulation comparator.

2.2.2 Current sampling and slope compensation circuit design

Current sampling technology is mainly used in DC-DC converter power tube over-current protection and loop control. It is required to complete the accurate sampling of the current value in the power transistor, and achieve the effect of reducing the additional loss caused by the sampling circuit. Slope compensation technology is mainly used to complete the harmonic compensation of inductor current to eliminate the generation of sub harmonic oscillation, and ensure that the DC-DC converter can always be stable in normal operation.

In this DC-DC converter design, the current sampling circuit is mainly improved and optimized, as shown in **Figure 4.** In the actual operation process, the current in the power tube is detected and converted into voltage signal output; after V-1 transformation, the voltage signal is superimposed with the slope compensation signal, and the output of the error amplifier is compared, so as to achieve the effect of inner tube control. At the same time, such a current sampling circuit design can operate normally in 1.2V low voltage state, and consumes less power[3].

In the design of DC-DC converter, V-1 conversion circuit is generally used to convert slope compensation signal and current sampling signal to current signal, and then to sum current. In this case, only a resistor is needed to convert the sum current into a voltage signal.

2.2.3 Pulse width modulation control logic and power transistor drive circuit design

In DC-DC converter, pulse width modulation control logic and power transistor drive circuit occupy a very important position. For PWM control logic, the size of main power switch and synchronous rectifier tube is relatively large, so it is necessary to config drive circuit to realize the control of power switch and synchronous rectifier. The structure of PWM control logic circuit is shown in **Figure 5.** In practice, when the power transistor is turned on, the inductance current will gradually increase, and the level of the inverter input of the pulse width modulation comparator will increase; when the level increase value exceeds the level of the in-phase input terminal, the output signal of the pulse width modulation comparator will change from high level to low level, and the ncontrol signal will be converted into high level; after passing through the drive circuit, the power switch will be turned off, and the same will happen. The results show that the inductor current and the level of the invert end of the comparator decrease when the reverse phase of the comparator drops below the in-phase input terminal, the output signal of the comparator is modulated by pulse width to change the low-level into the high-level, and the pcontrol signal is transformed into the high-level, and the ncontrol signal is converted to the low-level; after passing through the drive circuit, the

synchronous rectifier tube is turned off state, the main power switch is in the on state[4].

The design of the power transistor drive circuit structure is shown in **Figure 6.** In actual operation, when the output signal PC is at high level, the power tube is in the off state; when the output signal NC is high level, the synchronous rectifier tube is in the open state; when the output signal PC is low level, the synchronous rectifier tube enters the closed state.

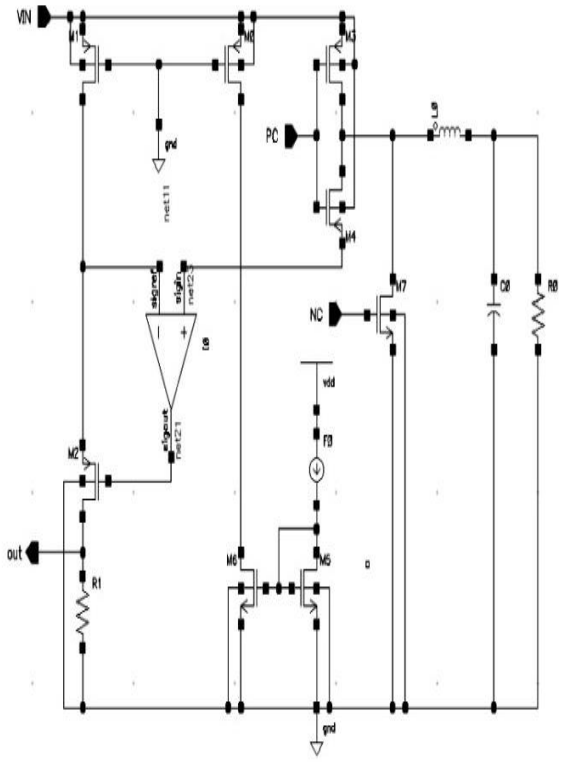

Figure 4. Improved and optimized current sampling circuit**.**

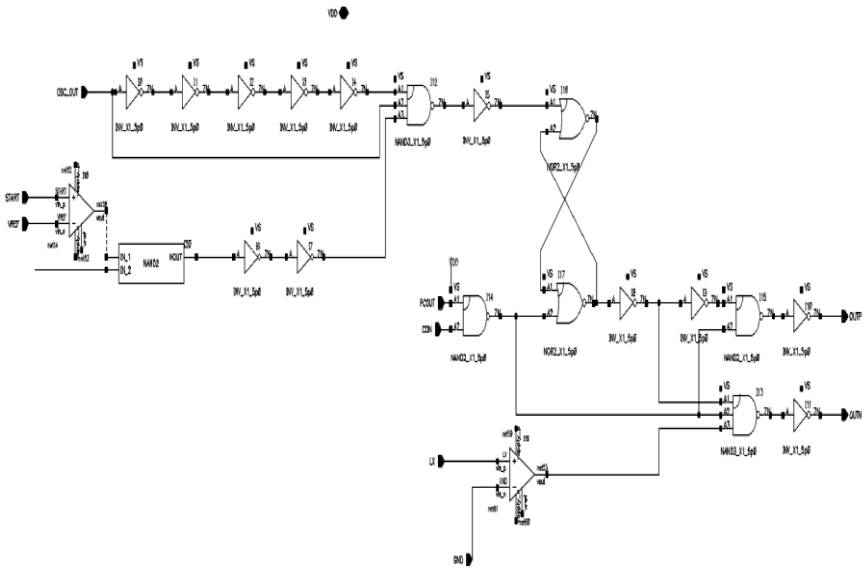

Figure 5. Structure of PWM control logic circuit**.**

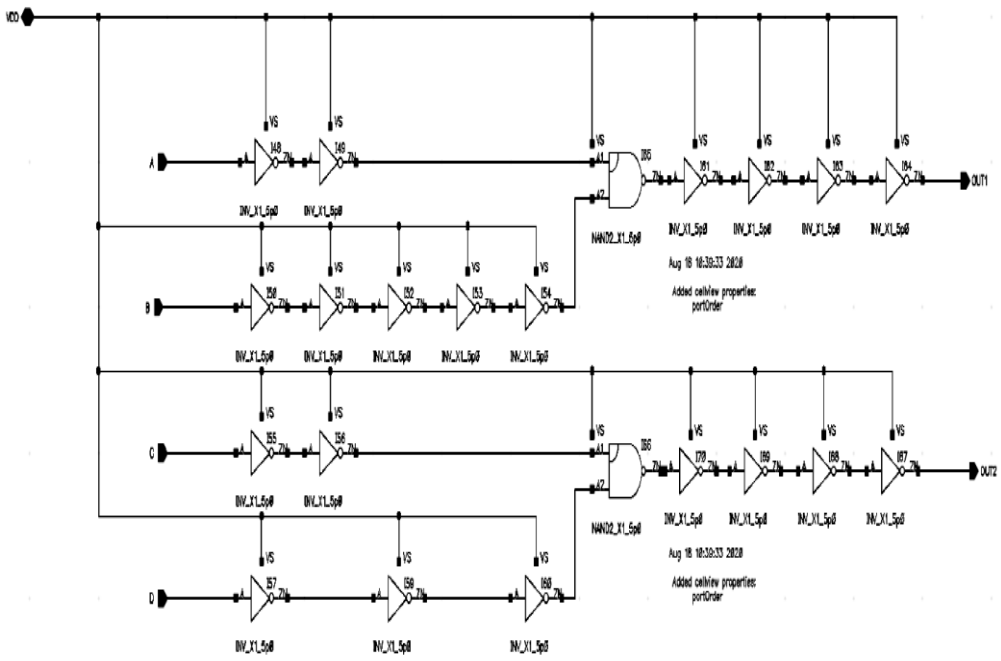

Figure 6. Power transistor drive circuit structure diagram**.**

3. Analysis and treatment of instability

3.1 Simulation verification conditions

In order to ensure the scientific and practical design of the DC-DC converter, the whole circuit simulation is carried out, and the working performance of the DC-DC converter is analyzed and determined. HSPICE was used as the tool of simulation verification, and 0.35 μm CMOS process was used, as well as different operation modes of the chip, such as start-up and transient operation. The connection mode of control circuit and peripheral circuit used in the simulation process is shown in the following **Figure 7**[5].

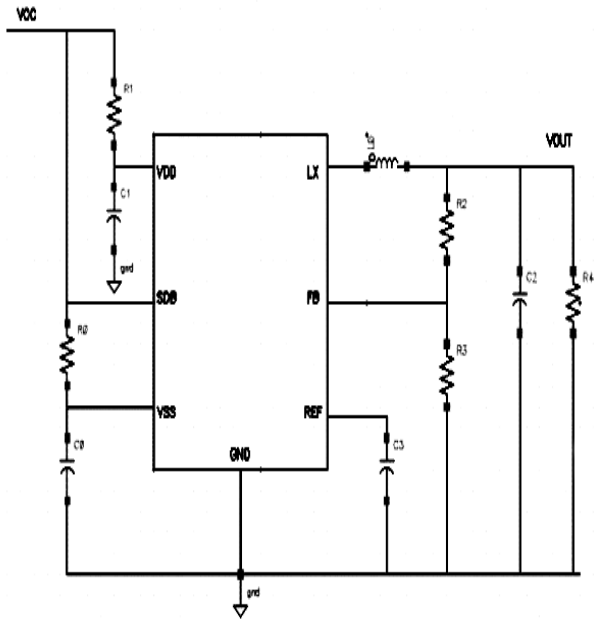

Figure 7. DC-DC converter control chip and interconnection with peripheral circuits**.**

3.2 Turn off mode

When the chip enable signal input is low level, the chip will enter the sleep state, and all functional modules outside the reference circuit will stop running. In other words, the whole DC-DC converter circuit is in sleep state, and the power consumption is lower. When the operating temperature is high and the output voltage is low, the chip will also enter the sleep state.

3.3 Normal operation mode

The soft start mode introduced in this paper is as follows: the large capacitor is attached to the chip, the voltage is gradually raised to control the duty cycle, and the duty cycle is slowly increased. The results show that the output voltage of DC-DC converter increases rapidly and can produce large surge current; under the condition of fixed load current, if the soft start capacitor increases, the start-up process will be longer.

In this study, the CCM mode under heavy load, DCM mode under light load, frequency hopping mode under extremely light load and no-load are simulated and analysed. The results show that: under heavy load, the power transistor will turn on in all cycles, and the inductor current will fluctuate continuously; under light load, the inductance current will cross zero; under extremely light load and no-load condition, the power transistor will no longer step by step. At this time, the main power switch is in the off state, and the inductance current will be reduced to zero[6].

The simulation results of transient performance show that the output voltage can reach a new steady value after a short dynamic recovery time after the sudden change of load (it is proved that the corresponding time of the system to the transient load change is shorter); there is a steady-state error of o.o1v between the new steady-state value and the original output voltage.

4. Conclusion

To sum up, the synchronous rectification technology can adaptively complete the selection of suitable working state according to the change of load current, and promote the efficiency of light load. Based on the introduction of modulator, current sampling circuit and slope compensation circuit, the design of peak current mode synchronous buck DC-DC converter is realized. The simulation results show that the DC-DC converter has better performance and meets the design requirements.

References

1. Michal V, Nicolò Z, Matteo A. Low-complexity inductance estimation for switched-mode power converters using peak-current mode control. IET Power Electronics 2020; 13(11): 2269–2273, 19.
2. Pal K, Pattnaik M. Performance of a synchronous buck converter for a standalone pv system: An experimental study. 2019 IEEE 1st International Conference on Energy, Systems and Information Processing (ICESIP); Chennai, India. 2019. p. 1–6.
3. Zhou M, Low Q, Siek L. A high efficiency synchronous buck converter with adaptive dead-time control. 2016 International Symposium on Integrated Circuits (ISIC); Singapore. 2016. p. 1–4.
4. Šviković V, Cortés JJ, Alou P, and *et al*. Multiphase current-controlled buck converter with energy recycling Output Impedance Correction Circuit (OICC). IEEE Transactions on Power Electronics 2015; (30): 9: 5207–5222.
5. N. Kondrath and M. K. Kazimierczuk, Control-to-output and duty ratio-to-inductor current transfer functions of peak current-mode controlled dc-dc PWM buck converter in CCM. Proceedings of 2010 IEEE International Symposium on Circuits and Systems; Paris: 2010; p. 2734–2737.
6. Miao M, Bing Y. Research on low dropout operation of current-mode DC-DC buck converters with heavy loads. 2011 IEEE 3rd International Conference on Communication Software and Networks; Xi'an. 2011. p. 735–739.