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Accurate modeling techniques for power delivery

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ACCURATE MODELING TECHNIQUES FOR POWER DELIVERY

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ABSTRACT

Power delivery is essential in electronic systems to provide reliable power from voltage sources to load devices. Driven by the ambitious user demands and technology evolutions, the power delivery design is posed serious challenges. In this work, we focus on modeling two types of power delivery paths: the power distribution network (PDN) and the wireless power transfer (WPT) system.

For the modeling of PDN, a novel pattern-based analytical method is proposed for PCB-level PDN impedance calculations, which constructs an equivalent circuit with one-to-one correspondences to the PCB's physical structure. A practical modeling methodology is also introduced to optimize the PDN design. In addition, a topology-based behavior model is developed for the current-mode voltage regulator module (VRM). This model includes all the critical components in the power stage, the voltage control loop, and the current control loop of a VRM device. A novel method is also proposed to unify the modeling of the continuous and discontinuous conduction modes for transient load responses. Cascading the proposed VRM model with the PCB-level PDN model enables a combined PDN analysis, which is much needed for modern PDN designs.

For the modeling of WPT system, a system-level model is developed for both efficiency and power loss of all the blocks in WPT systems. A rectifier characterization method is also proposed to obtain the accurate load impedance. This model is capable of deriving the power capabilities for both the fundamental and higher order harmonics. Based on the system model, a practical design methodology is introduced to simultaneously optimize multiple system parameters, which greatly accelerates the design process.

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1. INTRODUCTION

Power delivery is essential in electronic systems to provide reliable power from voltage sources to load devices. Driven by the ambitious user demands and technology evolutions, the operation voltage of active devices is progressively lower to meet faster and more efficient data processing requirements [1]. In addition, modern integrated circuits (ICs) are dealing with more sophisticated scenarios. As a result, the amplitude and slew rate of load currents keep increasing while the voltage tolerance margin becomes tighter [2]. Therefore, the power delivery design is posed new challenges in efficiency, stability, and impedance optimizations [3-5].

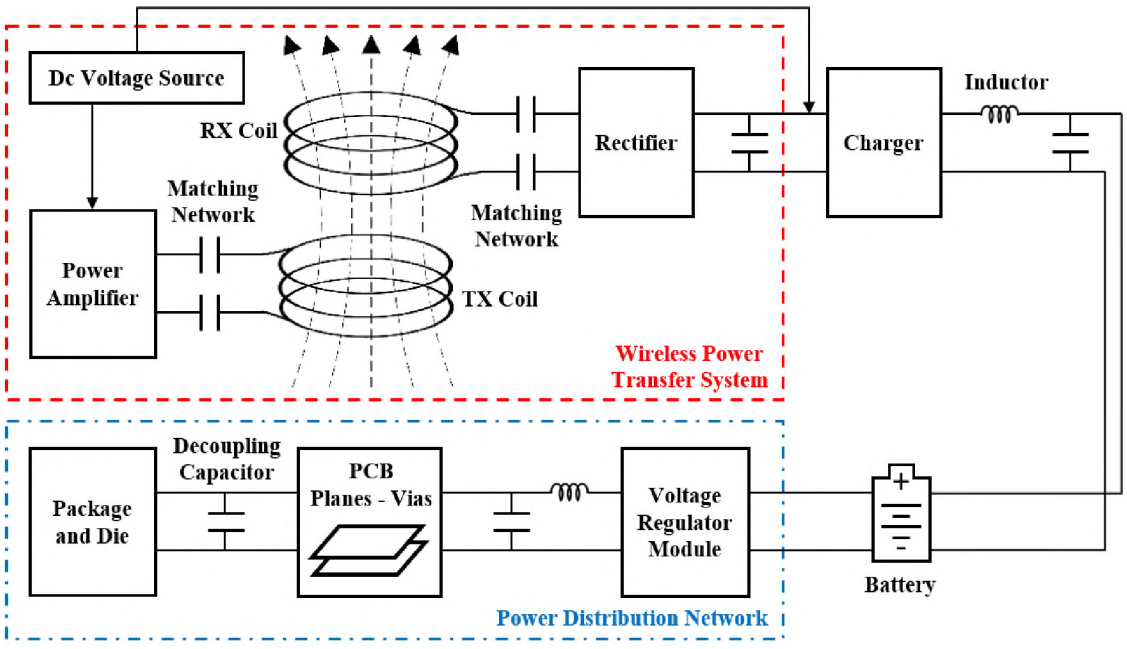


Figure 1.1. Power delivery paths in electronic devices.

As depicted in Figure 1.1, the power delivery paths consist of various components, such as power converters, inductors, decoupling capacitors, power-ground planes in printed circuit boards (PCBs), and vias between PCB layers. It is desired to accurately model all the key components and propose pratical optimization methodologies. In this dissertation, we focus on modeling two common types of power delivery paths: the power distribution network (PDN) and the wireless power transfer (WPT) system. This section introduces the background of the study, the state-of-the-art modeling methods, and the major contributions of the included articles.

1.1. POWER DISTRIBUTION NETWORK

The primary objective of the PDN design is to ensure normal IC operations by minimizing voltage fluctuations. As shown in the blue dot-dashed block of Figure 1.1, the end-to-end PDN has four main parts: (1) voltage regulator module (VRM); (2) PCB-level PDN; (3) package-level PDN; and (4) on-die PDN. The high frequency response is mainly determined by the package/die parasitics (usually above 100 MHz), the middle frequency response is affected by the PCB design (usually 300 kHz ~ 100 MHz), and the low frequency response is typically dominated by the VRM (usually below 300 kHz). With the increasingly complicated load current profile, a successful PDN design needs to optimize all the parts and satisfy the target impedance from dc to high frequencies.

In the past few decades, the modeling of PDN has been extensively studied. For the VRM modeling, the simple first-order linear resistor-inductor (RL) or the second order 4-element RL circuits were commonly used to fit the output impedance [6]. However, these discrete passive elements are not able to represent the control loop behaviors of modern

VRMs. A behavior model was proposed by simplying the control loop as a boost converter [7]. This unrealistic simplication has no physical meaning and leads to inaccurate results. A losed-loop mathematical model was developed to calculate the output impedance of VRMs [8], but this approach is purely mathematical and not intuitive to provide insights to improve the VRM design. The VRM vendors could provide encrypted device models using the commercial circuit simulators, such as SIMPLIS [9]. However, this model is only applicable to a specific device and the detailed implementations are confidential. For the PCB-level and package-level PDNs modeling, the fast transmission-line method (TLM) [10] and cavity model method [11-13] were commonly used to model the multilayered PCB. The partial-element equivalent circuit (PEEC) could also be applied to the chip-package hierarchical PDN structures [14-16]. In addition, full-wave electromagnetic modeling methods, including the finite-difference time-domain (FDTD) [17], the finite-element method (FEM) [18], and the method-of-moments (MOM) [19], were integrated into simulations tools for PCB and package PDN impedance. However, the existing methods may either become impractical or have limitations to model the PDN impedance in some new applications, such as the PCB design in the mobile platform.

1.2. WIRELESS POWER TRANSFER SYSTEM

WPT is an emerging technology that brings great convenience to charging a large variety of electronic devices. As shown in the red dashed block of Figure 1.1, a typical WPT system consists of four parts: (1) the power amplifier which converts dc voltage to ac power; (2) the transmitter (TX) coil with its matching network; (3) the receiver (RX) coil with its matching network; and (4) the rectifier which inversely regulates ac power to

dc output voltage. There are also industrial standards for WPT applications to improve the safety and interoperability, such as Wireless Power Consortium (WPC) Qi for consumer wireless charging devices and Society of Automotive Engineers (SAE) J2954 for wireless charging vehicles. In addition to the standards and regulations, it is crucial to minimize the power loss and improve the efficiency of WPT systems.

Various studies have been carried out to investigate WPT designs at both coil and system levels. A magnetic coil design method was presented in [20]. Other system parameters, such as the input voltage level, the coil matching networks, the operating frequency, and the load impedance, are also critical for efficiencies. The power transfer efficiency and capability were analyzed under different matching networks in [21] and [22]. However, the output load of the coils was assumed to be purely resistive and the nonlinear effects of the rectifier was not considered. The impacts of rectifier impedance were discussed in [23] and [24], but the authors only focused on the resonant condition and ignored the nonlinearity caused by the line-commutation process. Analytical expressions of coil-to-coil efficiency for both frequency and voltage tuning WPT systems were developed in [25]. However, the derivations were based on the First Harmonic Approximation (FHA), which becomes inaccurate when the system is operating at off-resonant frequency or the load quality factor is decreasing. In sum, it is desired to overcome the impractical assumptions of existing methods and develop an accurate system-level model for WPT applications.

1.3. CONTENTS AND CONTRIBUTIONS

This dissertation presents accurate modeling techniques for PDN and WPT systems. The outlines and contributions of this dissertation are summarized.

In the first paper, a novel pattern-based analytical method for PDN impedance calculation is proposed. This method focuses on the localized patterns formulated by adjacent vias. Therefore, it can easily decompose the complicated PCB structures in mobile platforms and avoid the extensive workload to identify the absolute positions of all the vias and decoupling capacitors at different layers. In addition, the proposed method uses analytical equations to calculate the impedance based on the localized via patterns, which provides more flexibility to optimize the PDN design compared to the complicated numerical solutions, especially in the pre-design stage. A practical modeling methodology is also developed based on the pattern-based analytical model to optimize the PCB-level PDN design. It constructs an equivalent circuit with one-to-one correspondences to the PCB's physical geometry, which is helpful to identify the most critical component contributing to the total impedance and improve the overall PDN design.

In the second paper, a topology-based generic behavior model is developed for the VRM in PDN design. This model includes all the interior topology-level components in the power stage, the voltage control loop, and the current control loop of a VRM device. Thus, it is helpful to provide more insights of the VRM's operations to improve the PDN design. A novel method is proposed to unify the modeling of the continuous and discontinuous current modes (CCM and DCM) for different load conditions. It enables a simplified procedure to implement the current control loop. In addition, a measurement-based characterization method is proposed to optimize the model parameters. This method

can be applied to any provided VRM devices to bypass the confidential concerns. By cascading the proposed VRM model with the PCB-level, the package-level, and the on-die PDN models, a combined PDN analysis integrating the VR control can be established, which is much needed for modern PDN designs.

In the third paper, a system-level model is developed for both dc-to-dc efficiency and power loss of each interior part in WPT systems. This model is capable of deriving the power capability for both the fundamental and higher order harmonics analytically, without the impractical assumptions used by the existing methods. A rectifier characterization method is also proposed to obtain the accurate load impedance for the system-level model. This method is flexible and applicable to any provided rectifier devices. Based on the proposed WPT model, a practical design methodology is introduced to simultaneously optimize multiple system parameters, which greatly accelerates the design process compared with the conventional trial-and-error method. They will become powerful tools to improve the system performance and the thermal design of WPT applications.

PAPER

I. A PATTERN-BASED ANALYTICAL METHOD FOR IMPEDANCE CALCULATION OF THE POWER DISTRIBUTION NETWORK IN MOBILE PLATFORMS

ABSTRACT

Power distribution network (PDN) is essential in electronic systems to provide reliable power for load devices. With faster load transient current and lower voltage tolerance margin for the microprocessors in mobile platforms, it is crucial to optimize the PCB design to satisfy the strict target impedance. The conventional modeling methods become impractical in mobile platforms due to the characteristics of high density interconnect PCB and limited layout space. To overcome these issues, a pattern-based analytical method for the PDN impedance calculation is presented. Based on the localized patterns formulated by the relative relationships between the adjacent vias, the parasitic elements are analytically determined for different regions of the entire PCB structure. With the assistance of this method, a practical modeling methodology is developed to construct an equivalent circuit with one-to-one correspondence to the PCB's physical geometry. As a result, the PDN design can be efficiently optimized especially for the pre-design stage to accelerate the development process. Finally, the proposed method is validated through measurements and full-wave simulations using a real mobile phone PCB in production.

1. INTRODUCTION

Power distribution network (PDN) is essential in electronic systems to provide reliable power for load devices [1]. The primary objective of the PDN design is to ensure normal IC operations by minimizing voltage fluctuations [2]. With the evolution in technologies, modern active devices are being designed with lower voltage to meet faster and more efficient data processing demands. As a result, the current draw and slew rate keep increasing, while the voltage tolerance margin becomes tighter [3]. The mobile platform, being a typical industrial application that follows these trends, is posed serious challenges on the PDN design. Driven by the ambitious user requirements, more aggressive architectures for mobile processors have been deployed to provide significant performance improvements [4]. However, it also results in a fast transient current and a strict target impedance at both dc and higher frequencies [5]. Furthermore, the high density interconnect (HDI) PCB is commonly used in mobile platforms to increase the circuitry density. The complicated interconnect structure brings non-negligible parasitic effects. In addition, the slim form factor of mobile phones limits the layout space and the number of surface mount decoupling capacitors, which causes difficulties to lower the PDN impedance. Thus, the PCB-level PDN design, including the parasitic elements associated with vias/power-ground planes and the decoupling capacitors, becomes more and more critical for mobile platforms.

Over the past few decades, PDN modeling has been extensively investigated. First, full-wave electromagnetic modeling methods were applied to study this problem, including the finite-difference time-domain method (FDTD) [6], the finite-element method (FEM)

[7], the method-of-moments (MOM) [8], and the partial-element equivalent circuit (PEEC) [9]–[11]. In addition, a fast and straightforward transmission-line method (TLM) compatible for SPICE implementation was developed to model planes with bypass capacitors [12]–[14]. Another fast method based on the cavity model was commonly used to calculate the input impedance between the power-ground planes [15], [16]. The reduction techniques for cavity model were also proposed to combine parasitic via inductance and generate equivalent circuits [17], [18]. However, due to the characteristics of the PCB in mobile phones, the existing methods either become impractical or have limitations to model the PDN in mobile platforms.

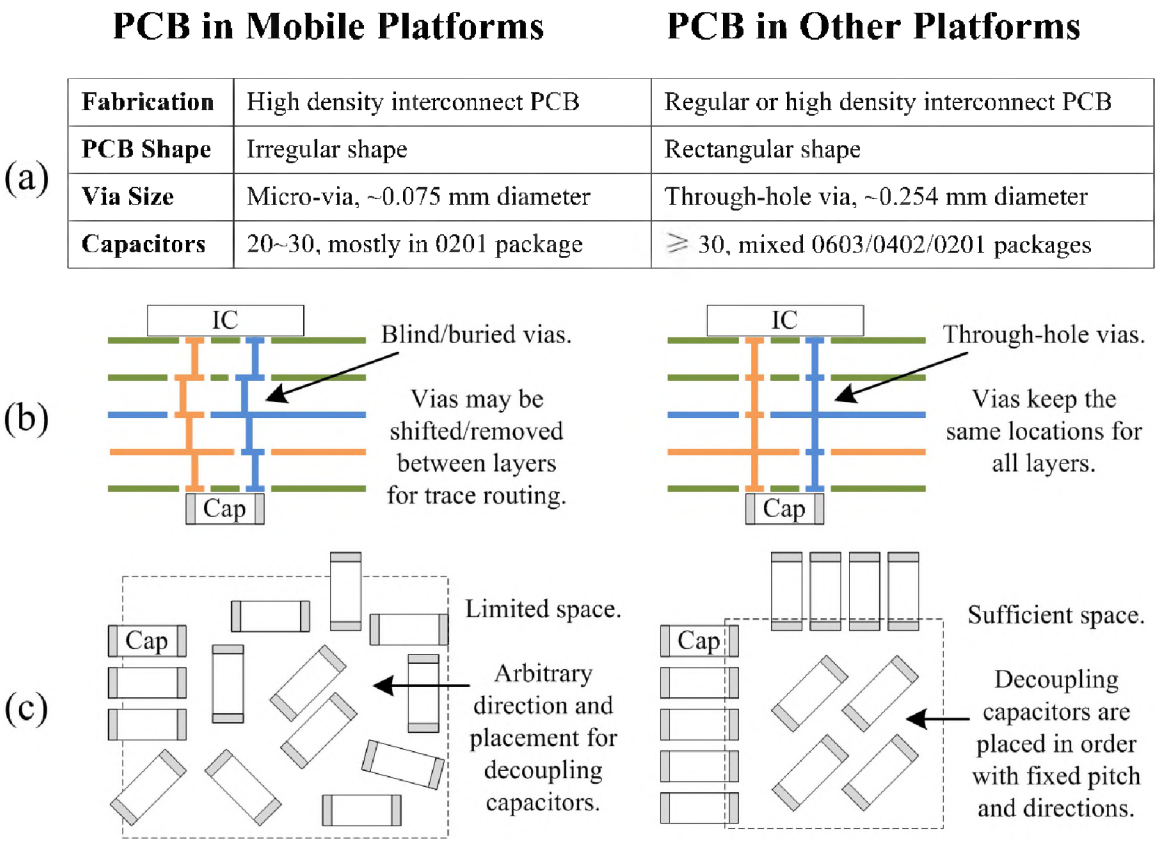


Figure 1. Comparison of PCB in mobile platforms and PCB in other platforms.

Figure 1 compares the PCBs in mobile platforms and other common platforms, such as server or personal computer. The interconnect structure of PCB can be very complicated, especially for the HDI PCB in mobile platforms. As shown in Figure 1 (a), the 0.075 mm diameter micro-vias in mobile platform PCB could result in a huge number of mesh cells for full-wave electromagnetic modeling methods. Hence, the computational burden is heavy and the simulation time is long. Similarly, due to the complexity of the geometry, the TLM model has to use a large number of circuit elements to converge with good simulation accuracy. Figure 1 (b) illustrates the difference in via types. All the vias in mobile platform PCB are blind/buried, while those in regular PCB are through-hole. The cavity model method, which requires the positions of all the vias as the model's ports, is only suitable for the through-hole case. For through-hole vias, the port locations for all the cavities formed by different plane pairs are exactly the same. Thus, the positions only need to be identified once using one cavity, then they can be applied to other cavities for further calculation. However, the blind/buried vias may be removed or shifted between cavities to make room for routing traces within a limited layout space. In this case, the via positions have to be determined separately for every cavity, which significantly increases the workload. In addition, the cavity model method cannot handle the "dog-bone" traces between the blind/buried vias easily. Another factor related to the port locations is depicted in Figure 1 (c). Since the decoupling capacitors should be placed close to the power/ground vias to minimize the parasitic inductance, the positions of decoupling capacitor's power/ground pads can be used to identify the port locations of the cavity model. For the regular PCB with sufficient layout space, the decoupling capacitors are placed in order with fixed pitch size and the same direction, so their positions can be easily determined. But for

the mobile platform PCB with limited layout space, the decoupling capacitors are arbitrarily placed with random directions. It is difficult to find the absolute positions for all the decoupling capacitors. Therefore, the cavity model method is impractical to model the PCB in mobile platforms. At last, technical change and new product proliferation have made the mobile phone industry extremely dynamic [19], which places greater demands on accelerating the development process. In spite of the existing methods that only focus on the post-validation stage (PCB layout is completed), the PDN design and modeling in the pre-design stage are rarely investigated. Thus, it is desired to develop a PDN modeling method that is suitable for mobile platforms and applicable in the pre-design stage.

To overcome the limitations of the existing methods for the PCB in mobile platforms, a novel pattern-based analytical method is proposed for PDN impedance calculation. Our method aims to achieve three major improvements, as shown in Figure 2. Firstly, instead of using the absolute positions of all the vias and decoupling capacitors, the parasitic elements are calculated based on the localized patterns. The formulation of pattern and its benefits are discussed in Section 2. Secondly, the complicated numerical solutions lack flexibility in the pre-design stage, so we integrate the analytical equations and introduce a modeling methodology applicable to both pre-design and post-validation stages in Section 3. Thirdly, in addition to modeling the whole PCB structure, our method is capable of conducting region-by-region analysis. These regions still maintain one-to-one correspondences to the physical geometry. So it is helpful to identify the dominant factors in PDN design. In Section 4, our method is validated by both whole structure and region-by-region comparisons using a real mobile phone PCB in production. Section 5 concludes this article.

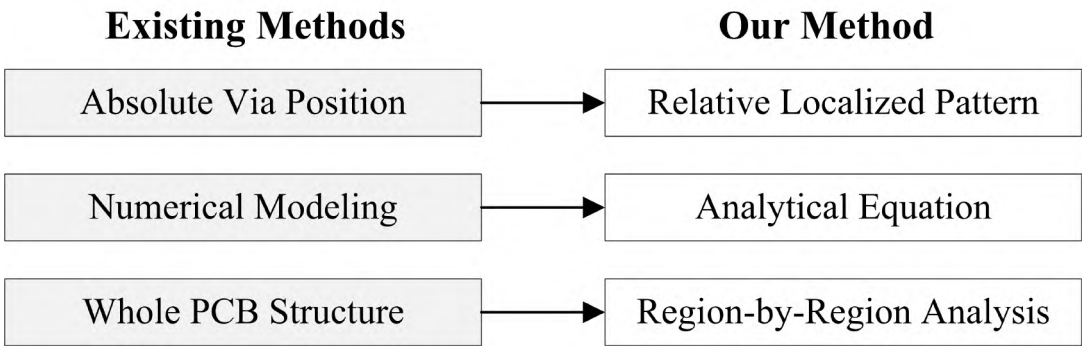


Figure 2. Major improvements of the proposed pattern-based analytical method.

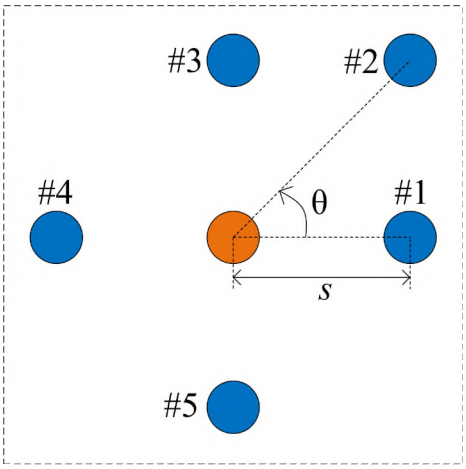
2. PATTERN FORMULATION AND CALCULATION

A novel approach to calculate the parasitic elements of vias is presented in this section based on the localized via patterns. Compared with the conventional methods using the absolute via positions, our method possesses better flexibility to handle the complicated PCB structures in mobile platforms. The accuracy of our method is validated through RF simulations under various conditions. Since the via pattern is a 2-D structure, the sensitivity of the edge-effect is also investigated.

2.1. PATTERN FORMULATION

As discussed earlier, the conventional PDN modeling methods become impractical in mobile platforms. It is desired to develop a new modeling method based on the characteristics of the mobile platform PCB. With the limited layout space and tight trace routing restriction, the via-in-pad technique is extensively used for space optimizations. As a result, the relative relationships (distance and angle) between the adjacent vias on the top and bottom layers can be directly obtained from the IC's pinout and decoupling capacitor's

footprint. If the blind/buried via is shifted or removed on the internal layers, only the moved via needs to establish new relative distance and angle with its adjacent vias, while the relative relationships of all other vias remain the same. Therefore, the relative distances and angles of the power and ground vias can be easily determined across all layers. Another attribute of the mobile platform PCB, as shown in Figure 1 (a), is the usage of decoupling capacitors with the same package. Restricted by the limited space, almost all the surface mount decoupling capacitors use the small 0201 package. It not only simplifies the PCB layout, but also reduces the variations of the relative distance between the power and ground vias for all the decoupling capacitors.



Ground Via	Distance (s)	Angle (θ)
#1	s_{min}	0°
#2	$\sqrt{2}\,s_{min}$	45°
#3	s_{min}	90°
#4	s_{min}	180°
#5	s_{min}	270°

Power Via Ground Via

Figure 3. Localized via pattern around the power via.

To represent the relative relationships between the adjacent vias, the localized via pattern is defined to include each power via and its surrounding ground vias. To effectively identify each via's position, the via pattern records the distance s and angle θ between each ground via and the centered power via, as illustrated in Figure 3. Note that the zero-degree

axis can be defined from any ground via, because we only care about the relative relationships of the vias. Based on the information in Figure 3, the distance between any two ground vias can be further calculated. Thus, the relative positions of the included vias can be uniquely determined by the via pattern.

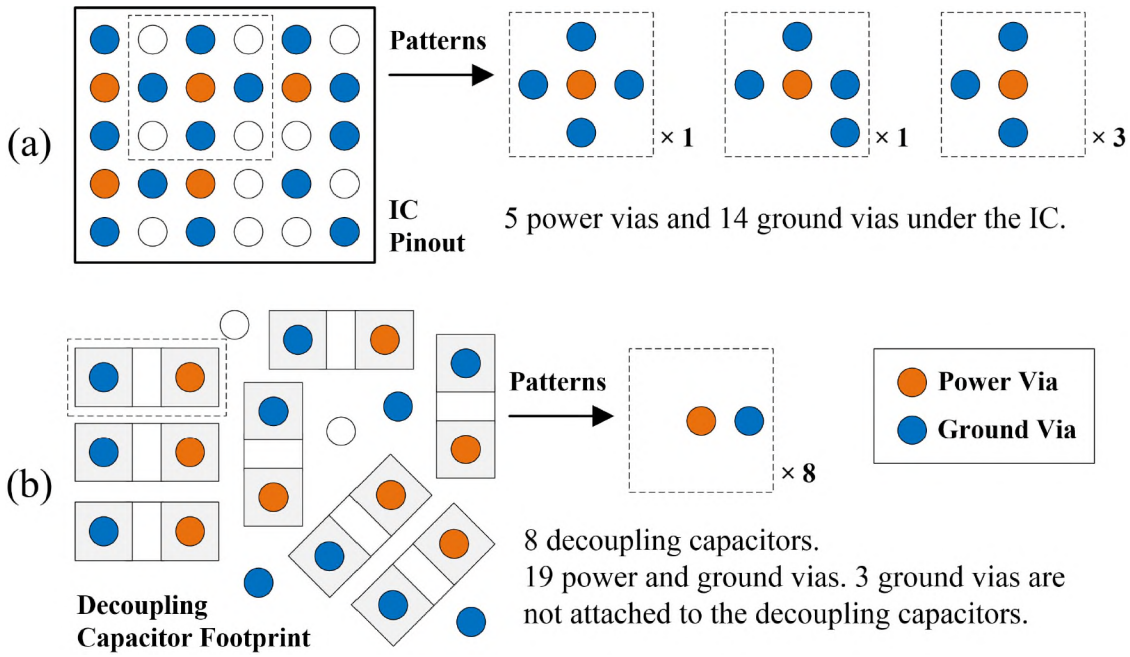


Figure 4. Formulated via patterns of two categories.

Depending on the connected components, there are mainly two categories of vias on the top and bottom layers: the IC vias and the decoupling capacitor vias. Examples of these two categories are depicted in Figure 4.

- For the IC vias in Figure 4 (a), three patterns are formulated based on the IC pinout. Since the pads under IC are well organized with the fixed pitch size, by applying the via-in-pad technique, the distances between the power and ground vias can be

easily determined by either 1 or $\sqrt{2}$ times of the pitch size. The angles are simply multiples of 45^o.

- For the decoupling capacitor vias in Figure 4 (b), only one pattern is needed to represent all eight decoupling capacitors in the same package. This pattern is formulated by the two vias in each capacitor's power and ground pads, as it provides the least impedance path for the current. Even though these capacitors are randomly placed and the absolute via positions are difficult to determine, the relative distance between the power and ground vias in each pattern is identical because of the same package size.

At last, if the blind/buried vias are moved on the internal layers, the via patterns need to be adjusted accordingly based on the formulated patterns from the top or bottom layers.

This pattern formulation approach assumes the power and ground vias in the IC region are alternately placed, as illustrated in Figure 4 (a). It is because the alternating via placement achieves lower parasitic via inductance than the grouped via placement [20], [21]. As a result, the magnetic flux is confined between the power via and its surrounding ground vias, so the coupling among the power vias can be neglected in practical PCB designs. The examples in Figure 4 demonstrate the flexibility of our pattern-based method to handle the complicated PCB structures in mobile platforms. The localized via patterns serve as the fundamental units to calculate the parasitic via inductance and resistance for the entire PCB structure.

2.2. PATTERN CALCULATION

One of the most critical parasitic elements in the PDN design is the via inductance. It is caused by the current induced magnetic flux penetrating through the loop formed by the adjacent power and ground vias.

Figure 5 (a) shows a simple case that contains one power via carrying current I and one ground via with the same return current. h is the via length, s is the distance between these two vias, and r is the via radius. Since the power and ground vias are typically placed between paralleled planes, they can be regarded as relatively long straight wires based on the image theory (equivalent to the h ≫ r condition) [22]. From the Biot- Savart law for this case, the magnetic flux density B around the power via can be calculated as:

$$B(x) \approx \frac{\mu I}{2\pi x}, \tag{1}$$

where μ is the magnetic permeability, and x is the distance to the power via. Note that the return current flowing on the ground via equally contributes to the magnetic flux penetratin through the loop. So the total magnetic flux Φ is:

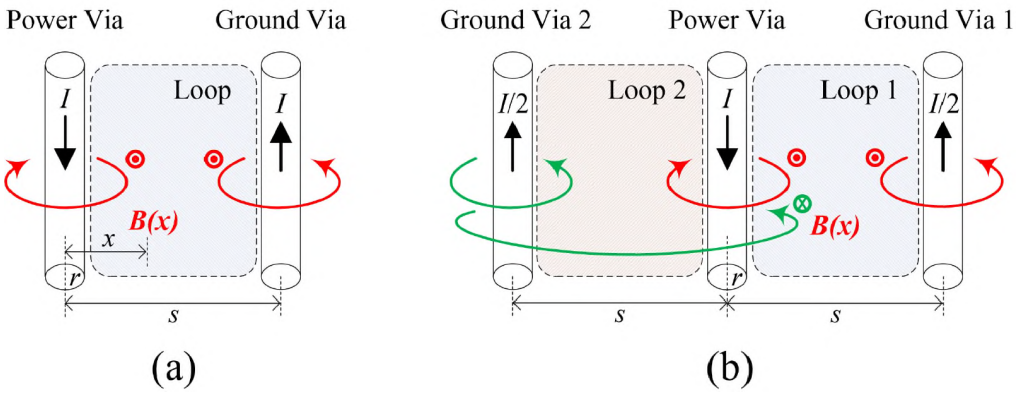


Figure 5. Magnetic flux though the loop formed by adjacent vias.

$$\Phi^{(a)} = 2\int_0^h \int_r^s B(x)dxdz = \frac{\mu Ih}{\pi} \ln\left(\frac{s}{r}\right), \tag{2}$$

The per-unit-length (PUL) inductance for this simple case is:

$$L_{\text{pul}}^{(a)} = \frac{\Phi^{(a)}}{Ih} = \frac{\mu}{\pi} \ln\left(\frac{s}{r}\right). \tag{3}$$

For a more complicated case, the power via may be surrounded by multiple ground vias, as shown in Figure 5 (b). In loop 1, the induced magnetic flux of ground via 2 has an opposite direction from that of ground via 1 and power via. It implies that the presence of ground via 2 reduces the total magnetic flux in loop 1. With the same distance s to the power via, the return current is evenly distributed on the two ground vias (I/2 on each ground via). The total magnetic flux in loop 1 can be calculated as:

$$\begin{aligned} \Phi_{\text{loop,1}}^{(b)} &= \frac{3}{2}\int_0^h \int_r^s B(x)dxdz - \frac{1}{2}\int_0^h \int_s^{2s} B(x)dxdz \\ &= \frac{\mu Ih}{2\pi}\left[\frac{3}{2}\ln\left(\frac{s}{r}\right) - \frac{1}{2}\ln(2)\right]. \end{aligned} \tag{4}$$

Symmetrically, the total magnetic flux in loop 2 is equal to the total magnetic flux in loop 1: $\Phi_{loop.2}^{(b)} = \Phi_{loop.1}^{(b)}$. Then, the PUL inductance for this case is determined by the magnetic flux of these two paralleled loops:

$$\begin{aligned} L_{\text{pul}}^{(b)} &= \frac{\Phi_{\text{loop,1}}^{(b)}}{\frac{1}{2}Ih} \,\Big\|\, \frac{\Phi_{\text{loop,2}}^{(b)}}{\frac{1}{2}Ih} \\ &= \frac{\mu}{2\pi}\left[\frac{3}{2}\ln\left(\frac{s}{r}\right) - \frac{1}{2}\ln(2)\right]. \end{aligned} \tag{5}$$

The derivations of (3) and (5) demonstrate the fundamental principles to calculate the PUL inductance based on the two simple cases. However, a real PCB structure may contain more complicated patterns. Therefore, a generalized equation for PUL inductance calculation needs to be developed based on an arbitrary via pattern.

Suppose a via pattern has N ground vias and the via radius is r, as illustrated in Figure 6. For each ground via i where i $\in$ [1, N], its distance to the power via is s_i. To maintain the law of current conservation, the total returning current I is distributed among all the ground vias. The ground via with longer distance to the power via shares less current. So a current coefficient c_i is defined to represent the portion of the current flowing on ground via i, where $\sum_{i=1}^{N} c_i = 1$. From (3), the impedance to the ground via is proportional to the logarithm of its distance ln(s). Therefore, the current coefficient c_i can be estimated based on the inverse logarithmic relationship of the distance as:

$$c_i = \frac{1}{\ln(s_i) \cdot \sum_{k=1}^{N} \frac{1}{\ln(s_k)}}. \tag{6}$$

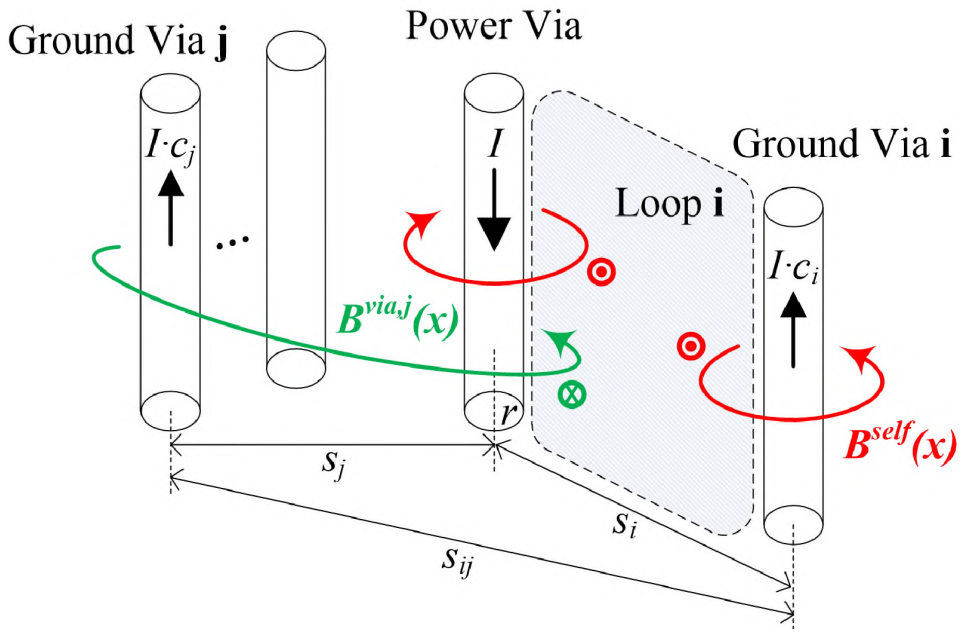


Figure 6. Illustration of the magnetic flux for an arbitrary via pattern.

Similar with (2), in the loop formed by ground via i and power via, the magnetic flux contributed by these two vias is:

$$\begin{aligned}\Phi_{\text{loop,i}}^{\text{self}} &= (1+c_i)\int_0^h\int_r^{s_i} B^{\text{self}}(x)dxdz \\ &= \frac{\mu I h}{2\pi}\left[(1+c_i)\ln\left(\frac{s_i}{r}\right)\right].\end{aligned} \tag{7}$$

The magnetic flux induced by other ground vias should also be considered. For a different ground via j where $j \in [1, N]$ and $j \neq i$, its distances to the power via and ground via i are s_j and s_{ij}, respectively. The current coefficient of ground via j is c_j. The magnetic flux, induced by ground via j and penetrates through the loop formed by ground via i and power via, is calculated as the integral of magnetic flux density from s_{ij} to s_j:

$$\begin{aligned}\Phi_{\text{loop,i}}^{\text{via,j}} &= c_j\int_0^h\int_{s_{ij}}^{s_j} B^{\text{via,j}}(x)dxdz \\ &= \frac{\mu I h}{2\pi}\left[c_j\ln\left(\frac{s_j}{s_{ij}}\right)\right].\end{aligned} \tag{8}$$

Note that the sign of $\Phi_{\text{loop,i}}^{\text{via,j}}$ is determined by the ratio of s_j and s_{ij}, which implies that other ground via's impact on the total magnetic flux is dependent on the relative positions of the vias.

Combining (7) and (8), the total magnetic flux in the loop formed by ground via i and power via is:

$$\begin{aligned}\Phi_{\text{loop,i}} &= \Phi_{\text{loop,i}}^{\text{self}} + \sum_{j=1,j\neq i}^{N}\Phi_{\text{loop,i}}^{\text{via,j}} \\ &= \frac{\mu I h}{2\pi}\left[(1+c_i)\ln\left(\frac{s_i}{r}\right) + \sum_{j=1,j\neq i}^{N} c_j\ln\left(\frac{s_j}{s_{ij}}\right)\right].\end{aligned} \tag{9}$$

Applying (9) to all the ground vias, the total magnetic flux in the N loops can be obtained, respectively. Following the same principle of (5), the PUL inductance for the generalized via pattern is calculated based on the magnetic flux of all the loops connected in parallel:

$$L_{\text{pul}} = 1 \Big/ \left(\sum_{i=1}^{N} \frac{c_i I h}{\Phi_{\text{loop,i}}} \right) = \frac{\left(\frac{\mu}{2\pi}\right)}{\sum_{i=1}^{N} \frac{c_i}{(1+c_i)\ln\left(\frac{s_i}{r}\right) + \sum_{j=1, j\neq i}^{N} c_j \ln\left(\frac{s_j}{s_{ij}}\right)}}. \tag{10}$$

Another parasitic element is the via resistance, which has a secondary effect on the PDN impedance mainly at dc and the resonant frequencies. Depending on the frequency f, the skin depth δ is calculated as:

$$L_{\text{pul}} = 1 \Big/ \left(\sum_{i=1}^{N} \frac{c_i I h}{\Phi_{\text{loop,i}}} \right) = \frac{\left(\frac{\mu}{2\pi}\right)}{\sum_{i=1}^{N} \frac{c_i}{(1+c_i)\ln\left(\frac{s_i}{r}\right) + \sum_{j=1, j\neq i}^{N} c_j \ln\left(\frac{s_j}{s_{ij}}\right)}}. \tag{11}$$

where ρ is the resistivity and μ is the permeability of the conductor material. For a standard-size via when the via radius $r \gg \delta$, the effective conduction area A_{eff} can be determined using a simplified equation: $A_{\text{eff}} = \pi[r^2 - (r-\delta)^2]$. However, the dimension of the micro-via used in mobile platform PCB is comparable with the skin depth within our frequency range of interest (300 kHz ~ 300 MHz). Hence, a more accurate method using the "truncated exponential decay" approach [23] is used to derive the modified skin depth δ' for the via resistance calculation:

$$\delta' = \delta(1 - e^{-\frac{r}{\delta}}). \tag{12}$$

The asymptotically correct formula for the effective area is:

$$A_{\text{eff}} = \pi[2r\delta' - \delta'^2] \cdot (1 + y), \tag{13}$$

where (1 + y) is a divisor correction coefficient based on a Modified Lorentzian function y. The fitted expression of y is also provided in [23]:

$$\begin{aligned} y &= \frac{0.19}{(1 + 0.27 \cdot [z^{1.83} - z^{-0.99}]^2)^{1.09}} \\ z &= 0.62\frac{r}{\delta}. \end{aligned} \tag{14}$$

Finally, the PUL resistance for a single via is calculated as:

$$R_{\text{pul}} = \frac{\rho}{A_{\text{eff}}}. \tag{15}$$

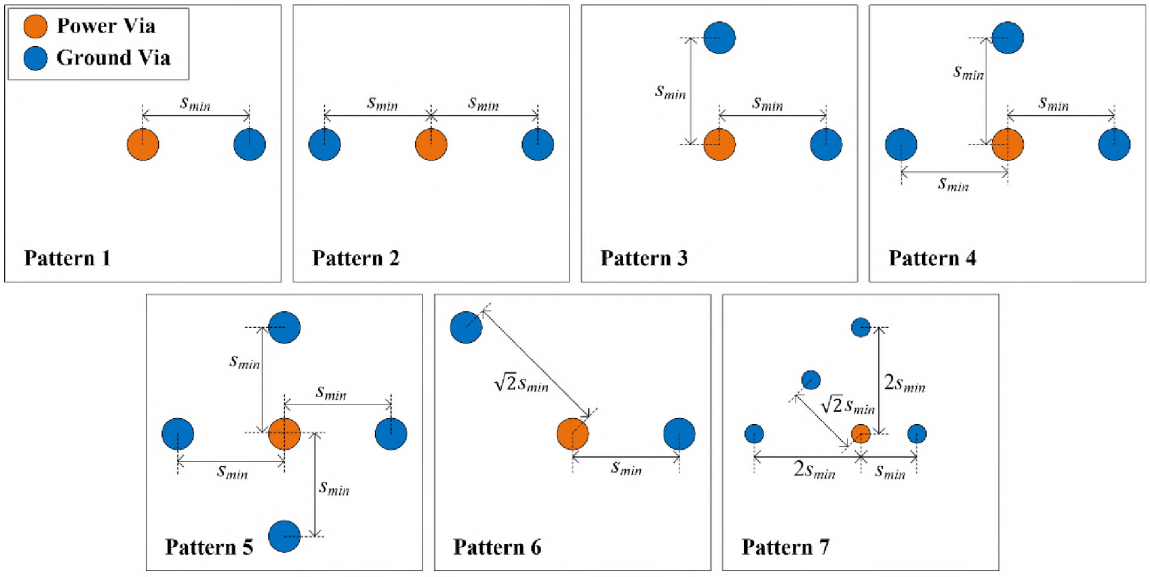


Figure 7. Arbitrary via patterns for validation.

2.3. SIMULATION STUDIES ON ACCURACY AND EDGE-EFFECT

The pattern-based analytical equation (10) can be applied to an arbitrary via pattern. Here a commercial RF simulation tool, ANSYS 2D Extractor, was used to validate this equation for various via patterns and distances. As illustrated in Figure 7, seven patterns were built in the simulation tool with different numbers and positions of the ground vias. The via diameter was 0.075 mm. The minimum via distance s_{min} was sweeping from 0.3 mm to 0.8 mm for all the patterns. These values were chosen based on the typical specification of the HDI PCB in mobile platforms. The simulated PUL via inductance, obtained using the ANSYS 2D Extractor, and the calculated PUL via inductance, obtained based on the proposed analytical equation, are compared in Figure 8. Good correlations are observed for all the cases where the largest difference between the calculated and simulated PUL inductances is 9.54 pH/mm (with a maximum discrepancy of 1.1%). It verifies the accuracy of our proposed analytical equation for an arbitrary via pattern. Equation (15) for the PUL via resistance is validated in Section 4.2.

Since the pattern is a 2-D structure, the vias are equivalently treated as relatively long wires during the calculation of the PUL parasitic elements. Therefore, the edge-effect, such as the fringing fields at the end of the vias or the proximity to the plane edges, may affect the accuracy of our method. To investigate the impact of the edge-effect, another 3-D electromagnetic field simulation tool, CST Studio, was used to simulate the via inductance of different lengths. “Pattern 1”, “Pattern 5”, and “Pattern 7” in Figure 7 were evaluated to check the smallest, median, and largest PUL inductance cases. The minimum via distance s min was fixed to 0.35 mm and the plane size was 2 mm by 2 mm. As shown in Figure 9, a port was added to the power via, the ground via(s) were shorted to provide a

return path for the injected current. The minimum via distance s min was fixed to 0.35 mm. The via length varied from 0.02 mm to 0.10 mm. The edge-effect causes additional parasitic PUL inductance when the via length is smaller than 0.04 mm. For a mobile platform PCB, the typical dielectric thickness between layers is 0.045 ~ 0.060 mm. In other words, the error introduced by the edge-effect is negligible in this application. The modeling of the edge-effect is beyond the scope of this article.

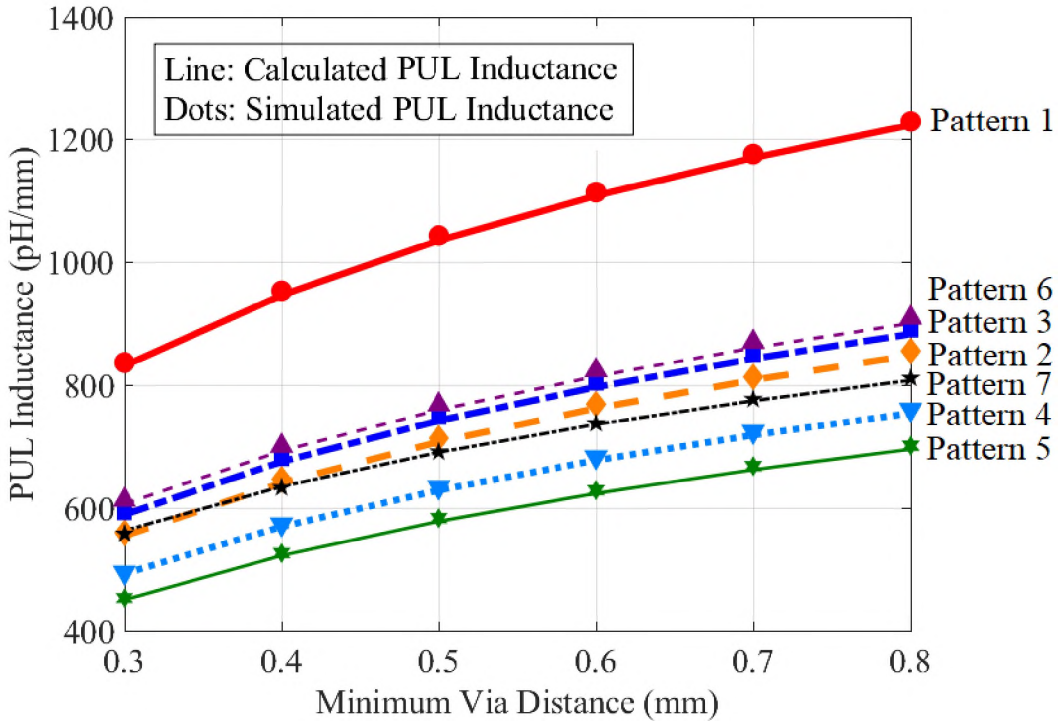


Figure 8. Comparison of via inductance for different patterns and distances.

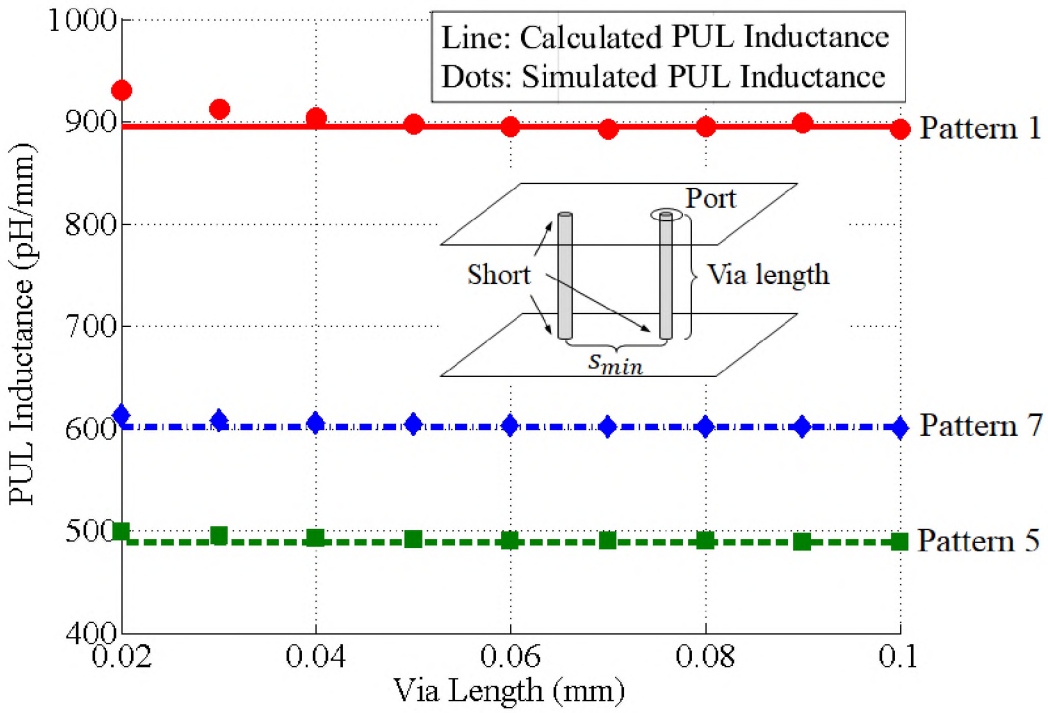


Figure 9. Simulation results of via inductance for different via lengths.

3. PDN MODELING METHODOLOGY

With the assistance of this pattern-based analytical method, a practical modeling methodology is proposed to calculate the PDN impedance of the entire PCB. The flow diagram is depicted in Figure 10. On the left side of this diagram, the "Via Pattern Database" indicates that the via patterns from the previous projects can be stored and adapted for future designs. It is not only useful to determine the impedance of a known PCB structure, but also helpful to improve the layout especially in the pre-design stage. The dashed arrow lines represent the interactions with this database. On the right side of this diagram, the main workflow is divided into four steps. The first three steps, including "(1) PCB division", "(2) pattern identification", and "(3) circuit reconstruction", construct

an equivalent circuit with one-to-one correspondences to the PCB physical geometry. Then, the PDN impedance can be obtained from the circuit simulations. If the target impedance is not satisfied for the initial design, an iteration process is conducted to further improve the impedance in the "(4) design optimization" step.

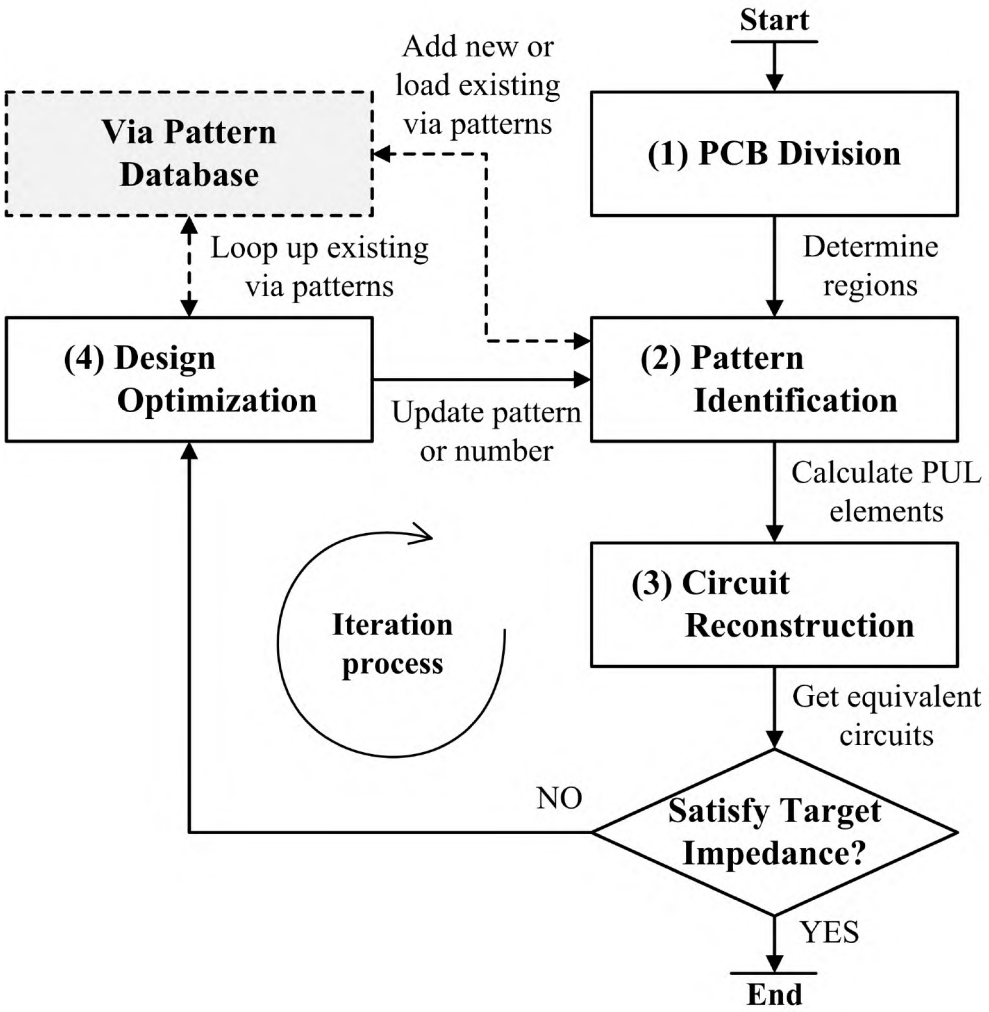


Figure 10. Flow diagram of the modeling methodology.

Following the modeling methodology, a real mobile phone PCB, illustrated in Figure 11, is investigated as an example. Among the total 12 layers, the 7th layer is the main power plane connecting all the decoupling capacitors and IC, and the 3rd layer is the sub power plane to unify the voltage under the IC. The ground planes are located on the 2nd, 4th, 6th, 9th, and 11th layers. The copper thickness is 0.023 mm for the top and bottom layers, and 0.018 mm for all the internal layers. There are 0402 package (22 μF, 10 μF) and 0201 package (2.2 μF) decoupling capacitors placed on both the top and bottom layers. All of the 0201 package capacitors are placed directly under the IC, while the other 0402 package capacitors are placed besides the IC due to the space limitation.

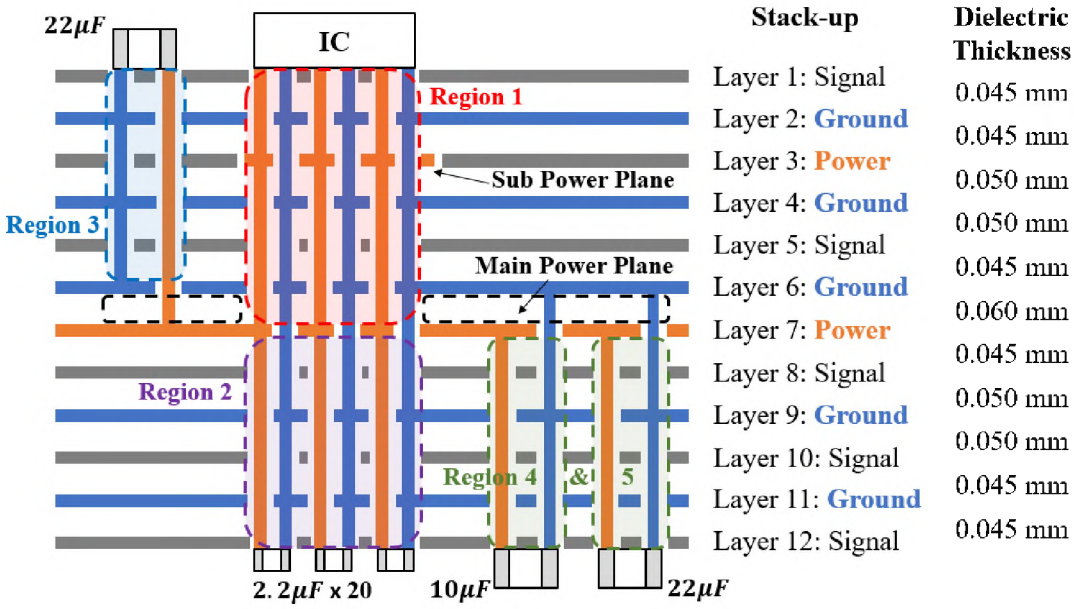


Figure 11. Physical geometry and region division of the mobile phone PCB.

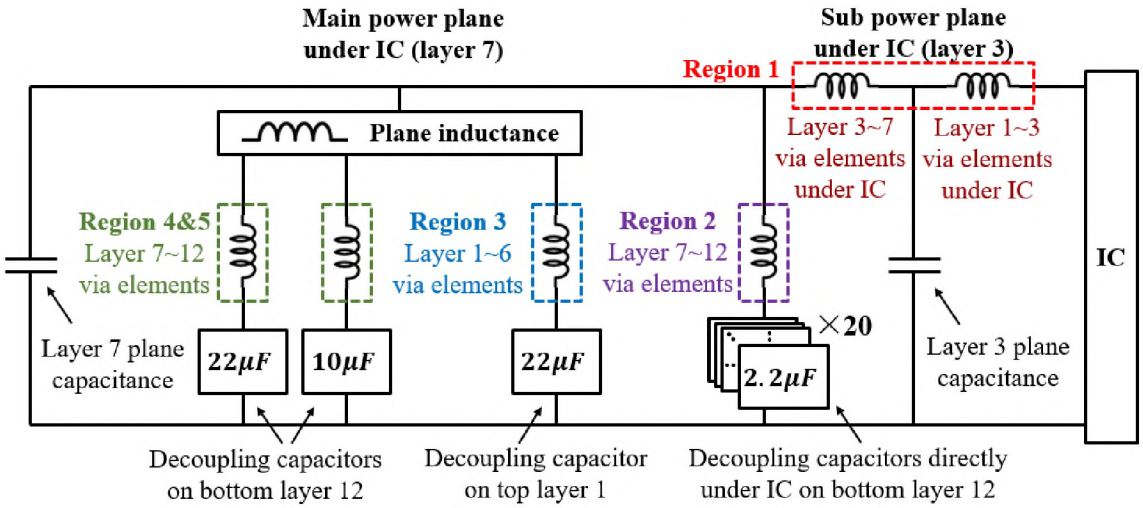


Figure 12. The equivalent circuit corresponding to the PCB under investigation.

3.1. PCB DIVISION

Seen at the input port of the load IC, the current in the PDN is always flowing along the power vias from the decoupling capacitors and returning along the nearby ground vias. By tracing the current flow path, the multilayered PCB structure can be divided vertically into different regions between the main power plane and the ground plane. For the target PCB in Figure 11, there are five regions associated with the physical geometry. “Region 1” and “Region 2” correspond to the vias directly under the IC from the top and bottom layers to the main power plane, respectively. “Region 2” also connects to the multiple 2.2 μF decoupling capacitors on the bottom layer. “Region 3”, “Region 4”, and “Region 5” correspond to the vias between the 0402 package decoupling capacitors and the main power plane. Since these capacitors are located besides the IC, we should include the plane inductance to reflect the current distribution on the main power plane. The mutual inductance among different regions are negligible because the distance between regions is

relatively larger than the distance from the power via to the nearby ground vias [24]. Within each region, the parasitic elements of the vias can be merged into the equivalent inductance and resistance. The equivalent circuit of the entire PCB structure is depicted in Figure 12.

3.2. PATTERN IDENTIFICATION

The pattern formulations for the IC and decoupling capacitor vias are introduced in Section 2. Accordingly, the patterns in "Region 1" are identified based on the IC pinout, and the patterns in other regions are identified based on the packages of the decoupling capacitors. Furthermore, an optimal pattern size needs to be selected for practical purposes. It is because a larger pattern includes more nearby ground vias, which leads to a more accurate result but also increases the complexity in pattern formulation. For the IC region shown in Figure 13, the pitch size s min is fixed to 0.35 mm and the radius of the effective pattern area r eff is investigated using 1, $\sqrt{2}$, 2, and $\sqrt{5}$ times s_{min}. When $r_{eff} = s_{min}$, only two ground vias are included in this pattern, but it yields a falsely high PUL via inductance of 635 μH/mm. By increasing r_{eff}, the PUL via inductance converges to 537 μH/mm. The optimal pattern size is achieved when $r_{eff} = 2s_{min}$ as it provides an accurate result with the simplest structure. This experimental-based conclusion can be verified using other via patterns. Therefore, it is suggested to include the ground vias whose relative distance is within two pitch sizes into the pattern.

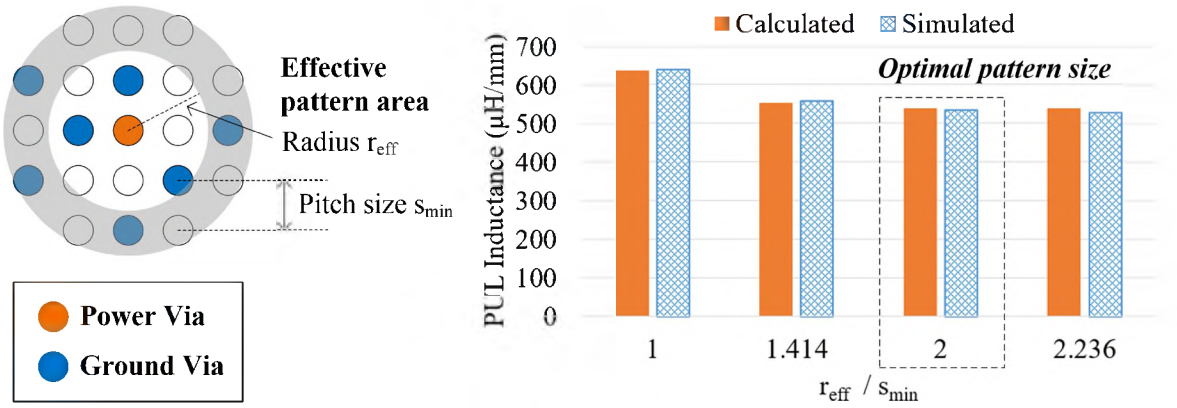


Figure 13. Selection of the optimal pattern size.

3.3. CIRCUIT RECONSTRUCTION

This step aims to determine all the components of the equivalent circuit in Figure 12. The PUL via inductance and resistance of the identified patterns can be calculated based on the analytical equations (10) and (15). Then, the inductance of a via segment is obtained by multiplying the PUL inductance by the effective length of this segment, and the resistance is obtained by multiplying the PUL resistance by the full segment length. Compared with the full length, the effective length excludes the layer thickness of the power and ground planes. It is because the inductance is related to the loop formed by the adjacent vias. The signal planes can also be ignored since they do not affect the impedance of the power nets. As illustrated in Figure 14, the inductance and resistance of multiple segments in the same region can be merged depending on their series or parallel relationship. As a result, one equivalent inductance and one resistance are generated to represent the parasitic elements for each region.

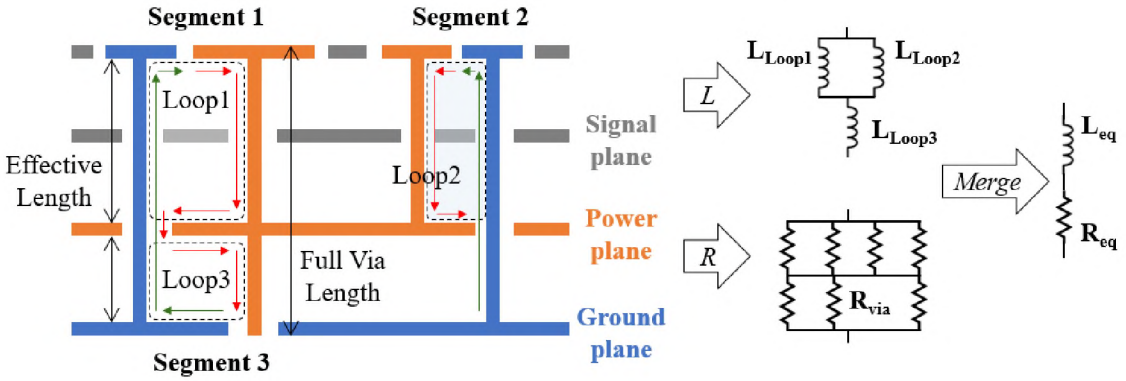


Figure 14. Calculation of the equivalent inductance and resistance in one region.

The plane capacitance is insignificant for the mobile phone PCB because of the limited layout space, so the simple parallel-plate capacitor equation is sufficient to estimate the plane capacitance:

$$C_{\text{plane}} = \frac{\varepsilon A}{d}, \tag{16}$$

where ε is the dielectric permittivity, A is the plane area, and d is the dielectric thickness between the plane pair. The total inductance between the main power plane pair ("Plane inductance" in Figure 12) is obtained based on the cavity model [15]–[18]. By merging the vias of the same region, the cavity model can be simplified by setting one port located at the center of each region instead of identifying the absolute positions for all the vias. At last, "Region 2", "Region 3", "Region 4", and "Region 5" connect to the decoupling capacitors on the top and bottom layers. For high accuracy, the SPICE model of the decoupling capacitor is employed in the circuit simulation since it includes both the parasitics, such as the equivalent series inductance/resistance (ESL/ESR) and the derating effects. Similar with the via inductance and resistance, the decoupling capacitors in the same region are in parallel and can be merged together.

3.4. DESIGN OPTIMIZATION

With the constructed equivalent circuit, the PDN impedance can be assessed by the circuit simulations. If the target impedance is not satisfied, an iteration process is conducted to further optimize the PDN design. The divided regions are helpful to identify the most critical component contributing to the total impedance. A common optimization method is to apply more decoupling capacitors, which can be easily implemented as increasing the number of the decoupling capacitor via pattern in our modeling methodology. Adding more ground vias is another feasible solution to reduce the parasitic via inductance, which is equivalent to changing the via pattern in design. The proposed pattern-based analytical equation is capable of predicting the PUL via inductance accurately, in order to provide quantitative guidance for the system designer. For instance, Figure 8 shows the PUL inductance with different via distances of the seven patterns in Figure 7. According to the calculated results, the designer is able to achieve lower impedance level with better utilization of the layout space for the new design. So our modeling methodology is especially useful in the pre-design stage when the PCB layout is not fully completed.

4. VALIDATION

The PDN impedance of the mobile phone PCB in Figure 11 was measured to validate our modeling methodology. The shunt-thru method was used to achieve the accurate mΩ impedance measurement [25], as depicted in Figure 15. By landing the two micro-probes (PacketMicro GR201504) between the IC's power and ground pads, the transmission coefficient S_{21} was measured by the vector network analyzer (Keysight

E5061B). Then, the impedance of the entire PCB structure can be derived from the measured S-parameter: $Z_{PDN} = 25 \cdot S_{21}(1 - S_{21})$. To avoid the mutual coupling between the micro-probes, the landing locations were separated at the opposite sides of the IC pinout. Full 2-port calibration and port extension were applied to move the reference planes to the micro-probe tips. Ferrite cores were attached to the test cable to eliminate the measurement error caused by the cable ground loop [26]. To include the derating effects of the decoupling capacitors, 0.75 V dc bias voltage was enabled in the vector network analyzer. The frequency range in this measurement was from 300 kHz to 300 MHz.

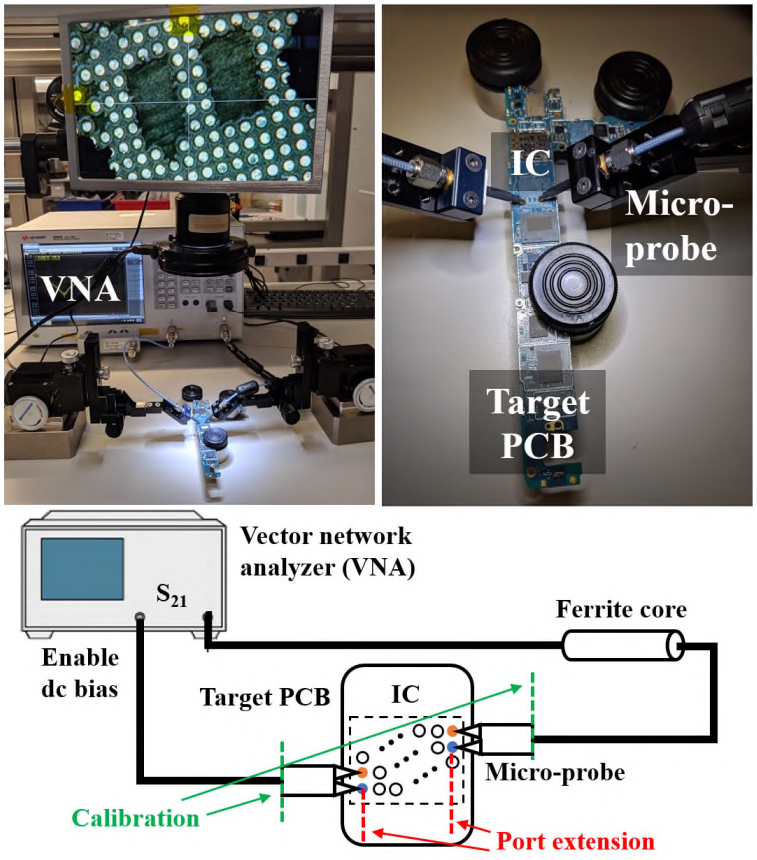


Figure 15. Photograph and diagram of the shunt-thru measurement setup.

The layout of this mobile phone PCB was also imported into a board-level electromagnetic field solver, Cadence Sigrity PowerSI. In addition to the total PDN impedance, the parasitic inductance and resistance of each region were simulated by manually setting the ports at different locations and layers. As a result, the accuracy of our modeling methodology can be validated by both whole structure and region-by-region comparisons.

4.1. WHOLE STRUCTURE COMPARISON

The impedance for the whole structure is contributed by all the components embedded in the PCB. However, different components have dominant effects at different frequencies. For example, capacitance usually dominates at a lower frequency and the via inductance is typically critical at a higher frequency. Therefore, it is desired to achieve good correlations with the simulations and measurements for the entire frequency range.

The calculated result based on our modeling methodology was using one lumped port grouping all the IC vias on the top layer. However, it is unrealistic to implement this lumped port in the measurement setup. As discussed above, the measured result was converted from the 2-port S-parameter, which resulted in lower IC via inductance and caused lower impedance at higher frequencies. So the calculated and measured results could not be compared directly. To solve this issue, two simulated results obtained using the Cadence Sigrity PowerSI were added with the lumped port and 2-port configurations, respectively. Then, the four types of results could be divided into two groups: the lumped port group including the calculated and simulated results; and the 2-port group including the simulated and measured results.

Two criteria are evaluated to validate our modeling method: the resonant frequencies and the magnitude of the PDN impedance. As shown in Figure 16, the impedance curves in the same configuration group agree well with each other. The three resonant frequencies, located at 1.5 MHz, 2.0 MHz, and 5.5 MHz, are all accurately captured with less than 100 KHz difference. The maximum variations of the impedance magnitude are within 0.26 mΩ and 0.33 mΩ for the lumped and 2-port configurations, respectively. Between the two groups, we can indirectly compare the calculated and measured results with respect to the difference of the two simulated impedance. The good correlations across the entire frequency range validates the accuracy of our modeling methodology for the whole PCB structure.

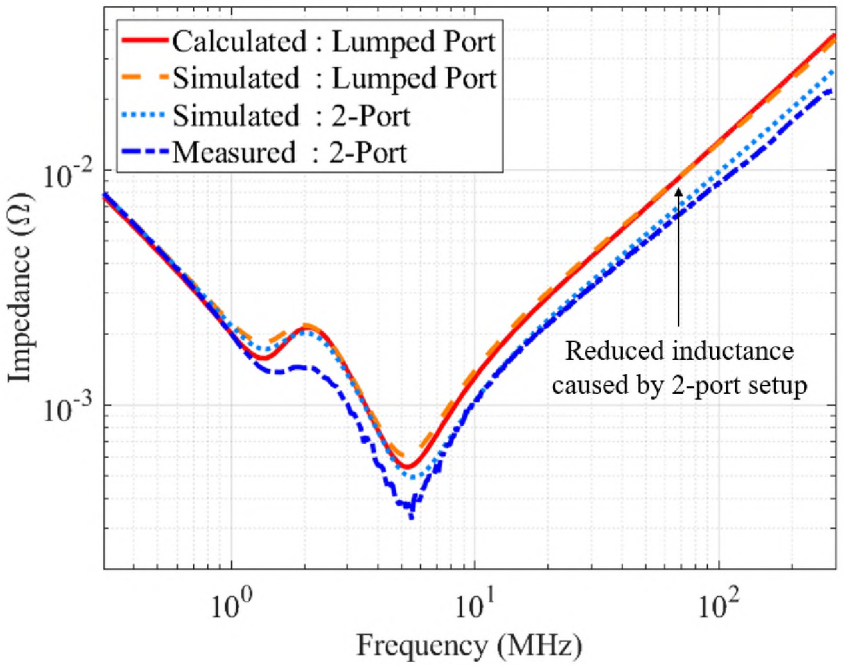


Figure 16. Comparison of the PDN impedance for the whole PCB structure.

Table 1. Region-by-region comparison of parasitic elements.

Location	Parasitic	Calculation	Simulation
Region 1 Layer 1∼3	Inductance	2.10 pH	2.39 pH
	Resistance	0.05 mΩ	0.06 mΩ
Region 1 Layer 3∼7	Inductance	4.81 pH	5.48 pH
	Resistance	0.14 mΩ	0.14 mΩ
Region 2 Layer 7∼12	Inductance	13.51 pH	12.93 pH
	Resistance	0.20 mΩ	0.19 mΩ
Region 3 Layer 1∼6	Inductance	289 pH	285 pH
	Resistance	2.95 mΩ	4.10 mΩ
Region 4 Layer 7∼12	Inductance	312 pH	312 pH
	Resistance	3.62 mΩ	4.00 mΩ
Region 5 Layer 7∼12	Inductance	242 pH	240 pH
	Resistance	3.62 mΩ	4.00 mΩ

4.2. REGION-BY-REGION-COMPARISON

Since the proposed modeling methodology is built on the basis of the divided regions, it is important to validate the equivalent inductance and resistance for each region. The calculated and simulated parasitic elements for different regions are compared in Table 1. "Region 1" is split into two parts because of the sub power plane on the layer 3. Other regions have only one set of equivalent inductance and resistance. The via resistance are obtained at the 6 MHz resonant frequency.

The error between the calculated and simulated parasitic inductance is within 12.2% for the IC vias and within 1.4% for the decoupling capacitor vias. The good agreement shows this methodology can not only estimate the via inductance accurately, but also identify the critical components contributing to the total PDN impedance. The calculated parasitic resistance generally correlate well with the simulated results (with a

discrepancy of 9.5%), except for "Region 3" (with a discrepancy of 28.0%). It is because there are multiple paralleled vias laid closely in the same pad of the decoupling capacitor in this region. Thus, the increased proximity effect causes higher ac resistance. However, the impedance curve is not significantly affected since the via resistance has a secondary impact mainly at dc and the resonant frequencies. So the current accuracy level for the resistance calculation is acceptable. The proximity effect modeling is not the focus of this article and will be discussed in future studies.

5. CONCLUSION

In this article, the limitations of the existing PDN modeling methods are discussed with the focus on mobile platform applications. To overcome these issues, a novel pattern-based analytical method is proposed for the impedance calculation. By utilizing the relative relationships between the adjacent vias, the localized via patterns are formulated based on the physical geometry. Then, the parasitic via inductance and resistance are analytically derived for arbitrary via patterns. It can be shown that our method has better flexibility to handle the complicated PCB structure in mobile platforms. In addition, a practical modeling methodology is developed to model and guide the PDN design. With the capability of accurate and layout-free impedance estimation, this methodology is especially useful for the pre-design stage to accelerate the development process. Finally, the proposed analytical equations and the modeling methodology have been extensively validated through the measurements and simulations on a real mobile phone PCB. Good agreements can be observed from both whole structure and region-by-region comparisons.

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II. TOPOLOGY-BASED ACCURATE MODELING OF CURRENT-MODE VOLTAGE REGULATOR MODULES FOR POWER DISTRIBUTION NETWORK DESIGN

ABSTRACT

Power distribution network (PDN) is essential in electronic systems to provide reliable power for load devices. Thus, modeling of PDNs in printed circuit board and package has been extensively studied in the past few decades. However, the voltage regulator module (VRM), which serves as the ultimate voltage source, was not thoroughly investigated. The conventional VRM model is either represented by a simple resistor-inductor equivalent circuit or implemented with simple assumptions. It lacks of accuracy for modern VRM devices. In this work, a generic behavior model, including both the power stage and control loops, is developed for the current-mode buck VRM. A novel method is also proposed to synthesize the continuous and discontinuous conduction modes for transient load responses. Through the measurement-based characterization, the model parameters are optimized to match with the actual design. Furthermore, this model can be applied to both the time-domain and frequency-domain circuit simulations to predict the voltage droop and output impedance, respectively. The accuracy of the model is validated using an evaluation board containing the single-phase and multiphase VRMs. It is demonstrated that the proposed model for VRM with control loops can be easily integrated into the PDN analysis and optimization.

1. INTRODUCTION

Power distribution network (PDN) is essential in electronic systems to provide reliable power for load devices [1]. The primary objective of the PDN design is to minimize the voltage fluctuations caused by the load current in order to maintain normal integrated circuit (IC) functions [2]. As depicted in Figure 1, a typical PDN consists of four main parts: voltage regulator module (VRM), printed circuit board (PCB)-level PDN, package-level PDN, and on-die PDN. When the transient current draws at the die bumps, a voltage droop may occur and affect the system's stability. The voltage droop in the time-domain and the PDN impedance in the frequency-domain are tightly related with each other, as shown in Figure 2. The high frequency response is mainly determined by the package/die parasitics (usually above 100 MHz) or the PCB design (usually 300 kHz ~ 100 MHz), and the low frequency response is typically dominated by the VRM (usually below 300 kHz). However, driven by ambitious user demands, modern ICs are dealing with more sophisticated scenarios while the voltage tolerance margin becomes progressively tighter [3]. To compensate for a large droop, the voltage sensing location is preferred to be closer to or even directly at the die bumps, so the voltage regulation (VR) control gains an increased open-loop bandwidth to react to faster transient events. This can introduce more coupling between the VR control and the PDN. An extreme case is the in-package integrated voltage regulator, where the control loop directly affects the first droop. Thus, influence of the VRM on the PDN design becomes increasingly more significant, especially in the high switching frequency and wide bandwidth applications.

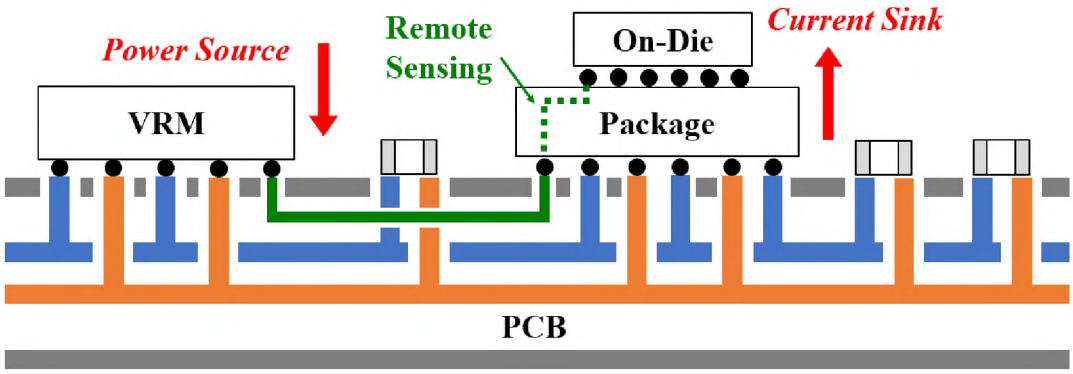


Figure 1. Main elements in the end-to-end PDN.

In the past few decades, the modeling of PDNs in PCB and package has been extensively studied. The fast transmission-line method (TLM) [4] and the cavity model method [5], [6] were successfully applied to the multilayered PCB. The chip-package hierarchical PDN structures were modeled by the partial-element equivalent circuit (PEEC) [7] and the decomposed segmentation method [8]. In addition, the full-wave electromagnetic modeling methods, such as the finite-difference time-domain (FDTD) [9], the finite-element method (FEM) [10], and the method-of-moments (MOM) [11], were also commonly used to simulate the PCB and package PDN impedance. For VRM modeling, conventionally the first-order linear resistor-inductor (RL) or the second-order 4-element RL circuits were fitted to match the VRM output impedance [12]. With the evolution in technologies, VRMs are integrated with the controller to effectively minimize voltage deviations caused by load transients [13]. As a result, discrete passive elements are incapable of representing the VRM's control loop responses. A behavior model including both the switching part and the feedback loop was proposed in [14]. However, the feedback loop was inaccurately simplified as a boost converter. Ahmadi et al. developed closed-loop

mathematical equations to calculate the output impedance of dc-dc switching converters [15]. But this approach was purely mathematical, and was not intuitive to provide insights to improve the VRM design. In [16], an encrypted device model provided by the IC vendor was employed for VRM transient simulations. Even though the simulation model was tuned to correlate with the actual performance, it was only applicable to a specific device from this vendor and the detailed implementations were not accessible due to the confidential concerns. In sum, despite the various PCB-level and package-level PDN modeling methods, there lacks an effective VRM model for PDN designs. Additionally, the higher the integration level of the VRM, the more complicated the internal design, which is mostly protected or encrypted by the IP-cores, will be. Thus, it is desired to develop a behavior model to bypass the IP-protection concerns.

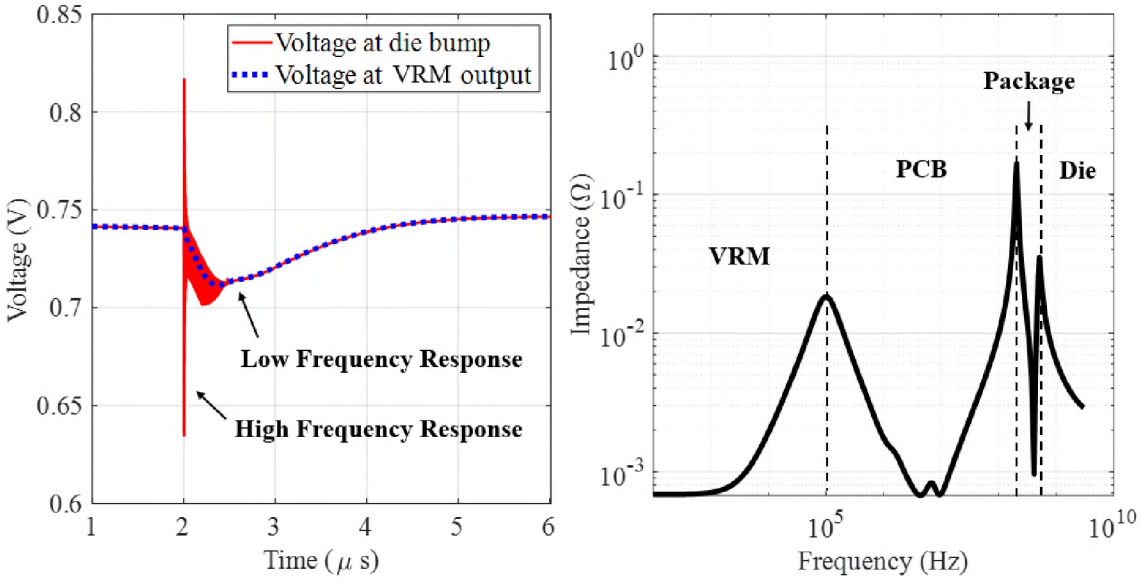


Figure 2. System-level PDN performance.

In this paper, a topology-based VRM model is proposed to address these challenges. By comparing different topologies in Section 2, this work mainly focuses on the widely used current-mode buck VRM. In Section 3, a generic behavior model based on the current mode topology is established including equivalent key components in the voltage control loop, the current control loop, and the power stage. Measurements are utilized in Section 4 to characterize the model parameters and also validate the proposed model using an evaluation board (EVB) which contains both single-phase and 3-phase VRMs. Section 5 concludes this paper.

2. VRM TOPOLOGY

VRM may refer to a wide range of chips and dc-dc converters with controllers. The step-down dc-dc converter for high-current rails that are especially sensitive to the transient voltage droop is studied herein because it is closely related to the PDN performance. Its power stage is essentially a buck converter. As depicted in Figure 3, the input voltage V_{in} is regulated by the high-side and low-side MOSFETs. The gate driver, which includes an oscillator, an RS flip flop, and a drive logic circuit, controls the alternating on-off states of the MOSFETs with the switching frequency f_{sw} and the duty cycle d. The switching node is connected to the output inductor L and the smoothing capacitor C_{out}, in order to provide the output voltage V_{out}. Depending on whether the inductor current i_L reaches zero during each switching cycle, the converter may operate in the continuous or discontinuous conduction mode (CCM or DCM). Since the CCM and DCM correspond to the heavy and light load conditions, respectively, it is crucial to model both modes to accurately predict

the transient load response. To minimize the voltage fluctuation caused by the IR drop and ac noise, the VRM typically integrates feedback control loops. Figure 4 demonstrates two types of the control topologies: the voltage-mode and the current-mode [17].

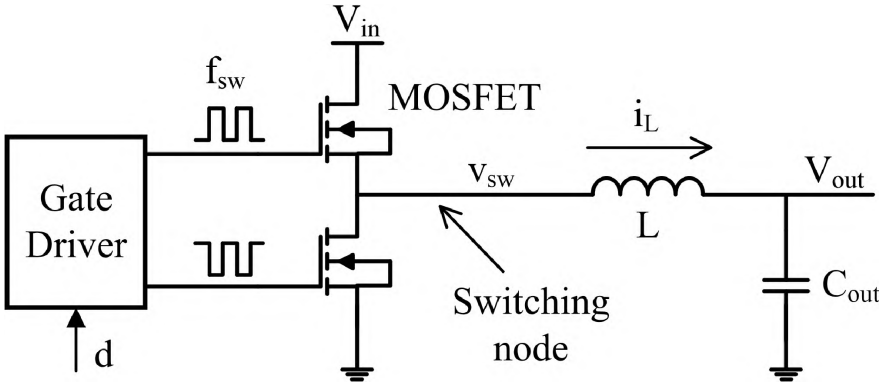
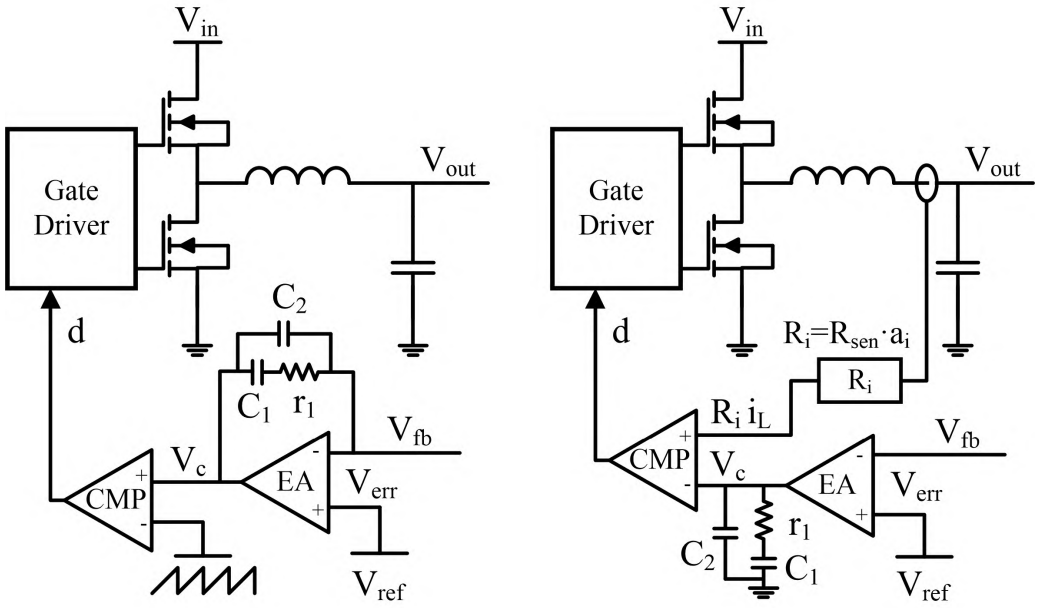


Figure 3. Diagram of an open-loop dc-dc buck converter.



(a) Voltage-Mode (b) Current-Mode

Figure 4. Typical feedback control topologies in VRM.

For the voltage-mode in Figure 4 (a), the feedback voltage V_{fb} can be sensed either at the output voltage node or remotely at the die bumps. Then, it is compared with an internal reference voltage V_{ref}, which is precise and stable over the temperature. The error voltage V_{err}, calculated by subtracting V_{fb} from V_{ref}, is further amplified by the error amplifier (EA) and the compensation circuits (r_1, C_1, and C_2). The compensated voltage V_c is then sent to the control input. The duty cycle d as the control variable can be determined based on the input level of V_c and a modulated saw-tooth signal. As a result, the power stage reacts to reduce V err as much as possible. However, the voltage-mode control has several notable drawbacks. First, the loop gain is limited and proportional to V_{in}. In addition, the changes in load must be sensed by V_{fb} in order to be corrected by the feedback loop, which results in a slow response. At last, it usually requires a complicated Type III compensation [17] and the CCM/DCM differences also add challenges for the compensation circuit.

To solve these drawbacks of the voltage-mode control, the current-mode control is developed and widely adopted in industrial applications. As shown in Figure 4 (b), the current-mode control introduces an additional feedback loop from i_L. The total current sensing gain is R_i, which is comprised of the sensing resistor R_{sen} and the current amplifier's gain a_i. The compensated voltage V_c from the voltage feedback loop is then compared with the voltage converted from i_L, and initiates the duty cycle d for the next switching period. When d > 50%, the slope compensation is also required for the current feedback loop to overcome the instability caused by the sub-harmonics oscillations [18]. The current-mode control can address the slow response issue of the voltage-mode control because i_L responds immediately to load changes. Furthermore, this system with a single-

pole roll-off of the control-to-output transfer function can be stabilized with a simpler Type II compensation circuit around the EA. The circuit also exhibits a higher gain bandwidth compared to the voltage-mode control [19]. In sum, the current-mode control is a superior approach for fast dynamic responses and is widely used in the modern VRM designs. However, this topology also possesses a larger complexity due to the dual feedback loops and slope compensation.

3. TOPOLOGY-BASED GENERIC BEHAVIOR MODEL

In this section, a topology-based generic behavior model is developed for the current-mode buck VRM. This model includes all the equivalent key components in the voltage control loop, the current control loop, and the power stage based on the topology shown in Figure 4 (b). A novel unified model is also proposed for the current control loop to handle both the CCM and DCM load conditions. At last, the implementation of this VRM behavior model is demonstrated in a circuit simulator, which is able to provide both the time-domain and frequency-domain simulation results.

3.1. VOLTAGE CONTROL LOOP

The voltage control loop is fed by the feedback voltage V_{fb}, as shown in Figure 5 (a). The error voltage V_{err} is obtained as:

$$V_{err} = V_{ref} - V_{fb}. \tag{1}$$

Since the EA is an equivalent voltage-controlled current source with the transconductance g_m, the current flowing into the compensation circuit is $i_c = g_m V_{err}$. It is convenient to model

the Type II compensation circuit using the s-domain analysis, because the compensated voltage V_c can be expressed as the multiplication of i_c and the EA output impedance:

$$\begin{aligned} V_c &= i_c \cdot \left[\frac{1}{sC_2} \parallel \left(r_1 + \frac{1}{sC_1} \right) \right] \\ &= g_m \cdot V_{err} \cdot \left[\frac{1}{sC_2} \parallel \left(r_1 + \frac{1}{sC_1} \right) \right], \end{aligned} \tag{2}$$

where r_1, C_1, and C_2 are the resistor and capacitors in this compensation circuit.

Choosing V_{err} as the input signal and V_c as the output, the transfer function of this system can be derived from (2):

$$\frac{V_c}{V_{err}} = \frac{g_m(sC_1r_1 + 1)}{s^2C_1C_2r_1 + s(C_1 + C_2)}. \tag{3}$$

Since C_1 is set to cancel the low-frequency pole of the current-mode topology and C_2 adds a high-frequency pole to filter out the high-frequency noises, the relationship $C_1 \gg C_2$ is generally satisfied in practical VRM designs. Therefore, (3) can be further simplified to:

$$\begin{aligned} \frac{V_c}{V_{err}} &\approx \frac{g_m(sC_1r_1 + 1)}{s^2C_1C_2r_1 + sC_1} \\ &= \frac{1}{sC_2r_1 + 1} \left(g_m r_1 + \frac{g_m}{C_1} \cdot \frac{1}{s} \right) \end{aligned} \tag{4}$$

The right-hand-side (RHS) of (4) contains a low-pass filter (LPF) and a proportional-integral (PI) control. The first term in the RHS represents the LPF with the cut-off frequency f_c:

$$f_c = \frac{C_2r_1}{2\pi}. \tag{5}$$

The second term in the RHS includes a proportional process with the coefficient k_p and a integral process with the coefficient k_i:

$$k_{\mathrm{p}} = g_{\mathrm{m}} r_1. \tag{6}$$

$$k_{\mathrm{i}} = \frac{g_{\mathrm{m}}}{C_1}. \tag{7}$$

In addition, the integrator has a dc gain limit k_{dc} in real devices, which can be modeled as:

$$k_{\mathrm{i}} \cdot \frac{1}{s} \approx \frac{k_{\mathrm{dc}}}{s \cdot k_{\mathrm{dc}}/k_{\mathrm{i}} + 1}. \tag{8}$$

Based on (4), the equivalent model of the voltage control loop is depicted in Figure 5 (b). The mapping relationships between the topology and the equivalent model are constructed by (5), (6), (7), and (8). Another parameter in the voltage control loop is the control delay t_d from the instant when V_{out} is sensed to the instant when V_c is updated, which is included in the model implementation procedure described later.

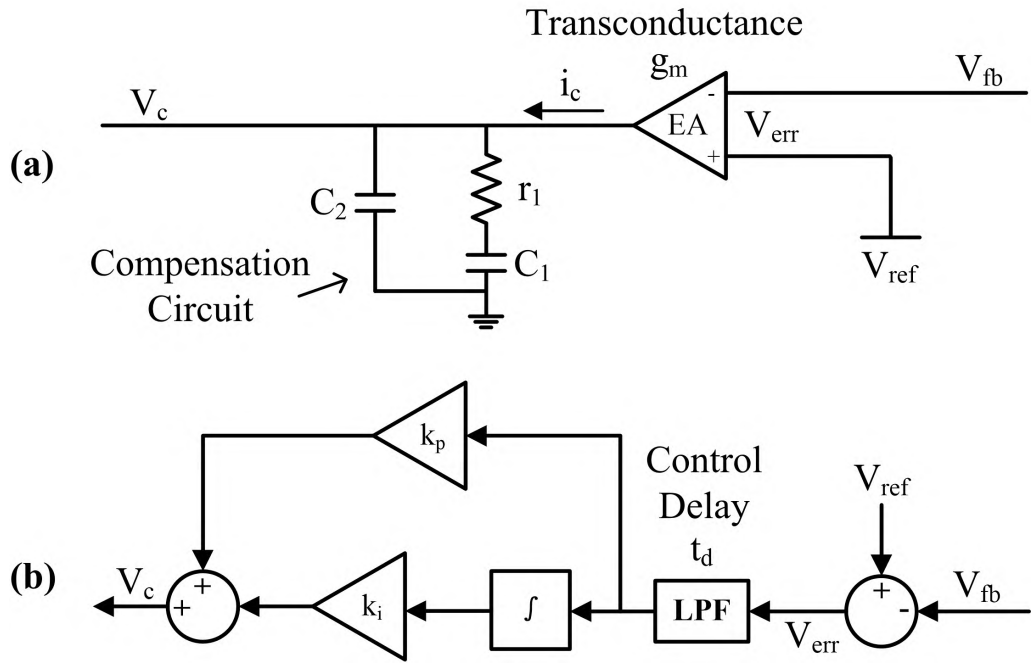


Figure 5. Modeling of the voltage control loop.

3.2. CURRENT CONTROL LOOP

Figure 6 illustrates the inductor current i_L under the CCM and DCM load conditions. Within each switching period $T_s = 1/f$, the averaged inductor current is denoted as $\widehat{i_L}$. The rising and falling slopes of i_L are denoted as S_r and S_f, respectively. Since the slopes are related to the charging and discharging behaviors of the output inductor, S_r and S_f are calculated as:

$$S_r = \frac{V_{in} - \widehat{i_L}(r_{on,H} + r_L) - V_{out}}{L}, \tag{9}$$

$$S_f = \frac{-\widehat{i_L}(r_{on,L} + r_L) - V_{out}}{L}, \tag{10}$$

where L and r_L are the inductance and equivalent series resistance (ESR) of the output inductor, $r_{on,H}$ and $r_{on,L}$ are the on-resistance of the high-side and low-side MOSFETs, respectively. With the slope compensation added to the compensated voltage, the peak inductor current $i_{L,peak}$ is calculated as:

$$i_{L,peak} = \frac{1}{R_i}(V_c - dV_{rp}), \tag{11}$$

where V_{rp} is the ramp voltage for the slope compensation.

For the CCM in Figure 6 (a), since i_L does not reach zero during each switching cycle, the derivative of $\widehat{i_L}$ between the adjacent cycles is determined as:

$$\frac{\partial}{\partial t}\widehat{i_L} = dS_r + (1-d)S_f. \tag{12}$$

Then, the averaged inductor current for the CCM is derived based on simple figure calculations:

$$\widehat{i_L} = i_{L,peak} - \frac{1}{2}dT_s\left(S_r - \frac{\partial}{\partial t}\widehat{i_L}\right). \tag{13}$$

Substitute (12) into (13) and move all the terms to the left-hand-side of the equation:

$$i_{\mathrm{L,peak}} - \widehat{i_{\mathrm{L}}} - \frac{1}{2}d(1-d)T_{\mathrm{s}}(S_{\mathrm{r}} - S_{\mathrm{f}}) = 0. \tag{14}$$

Define $\Delta S = S_r - S_f$, then combine (11) and (14), a quadratic equation with the independent variable d can be constructed as:

$$\frac{1}{2}T_{\mathrm{s}}\Delta S d^2 - \left(\frac{1}{2}T_{\mathrm{s}}\Delta S + \frac{V_{\mathrm{rp}}}{R_{\mathrm{i}}}\right)d + \left(\frac{V_{\mathrm{c}}}{R_{\mathrm{i}}} - \widehat{i_{\mathrm{L}}}\right) = 0. \tag{15}$$

Solve (15) to obtain d in the CCM. It should be noted that the range of the duty cycle is $1 \geqslant d \geqslant 0$, so the solution of $d > 1$ is dropped. Thus, the valid d can be expressed as:

$$d = \frac{1}{2} + \frac{V_{\mathrm{rp}}}{T_{\mathrm{s}}\Delta S R_{\mathrm{i}}} - \sqrt{\left(\frac{1}{2} + \frac{V_{\mathrm{rp}}}{T_{\mathrm{s}}\Delta S R_{\mathrm{i}}}\right)^2 - \frac{2}{T_{\mathrm{s}}\Delta S}\left(\frac{V_{\mathrm{c}}}{R_{\mathrm{i}}} - \widehat{i_{\mathrm{L}}}\right)} \tag{16}$$

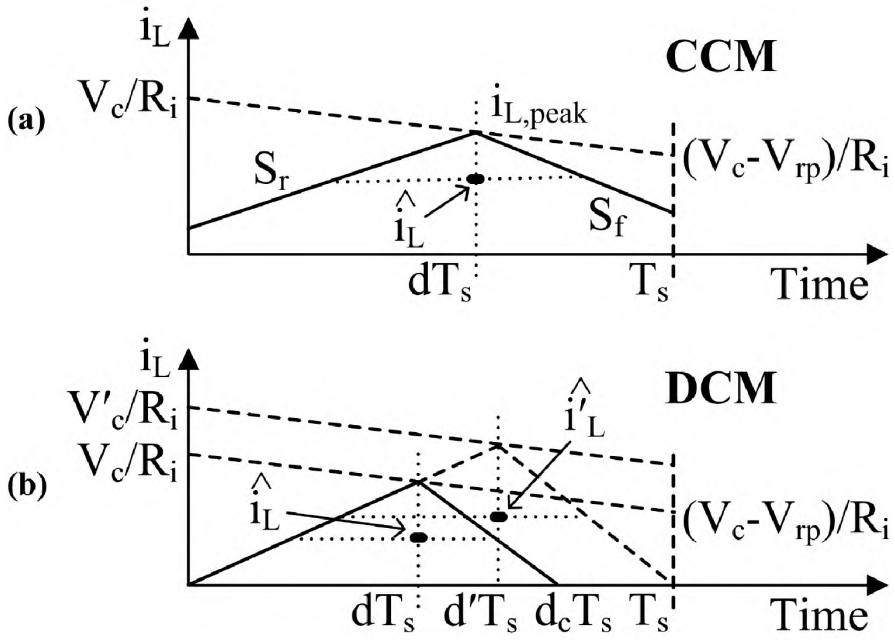


Figure 6. The inductor current in one switching period.

For the DCM in Figure 6 (b), i_L reaches zero within the switching cycle, so the derivative of $\hat{i}_L$ between the adjacent cycles is also zero. Suppose the ratio of the time period for $i_L > 0$ is d_c, the relationship between d and d_c is:

$$\frac{\partial}{\partial t}\hat{i}_L = dS_r + (d_c - d)S_f = 0 \tag{17}$$

Similarly, the averaged inductor current for the DCM is:

$$\hat{i}_L = \frac{1}{2}S_r d T_s d_c \tag{18}$$

Combine (17) and (18) to solve for the two unknown parameters d_c and d in the DCM:

$$d_c = \sqrt{\frac{-2\,\hat{i}_L \Delta S}{S_r S_f T_s}} \tag{19}$$

$$d = \sqrt{\frac{-2\,\hat{i}_L S_f}{S_r \Delta S T_s}} \tag{20}$$

It is clear that the current control loop is difficult to be implemented in circuit simulations, because the CCM and DCM use different equations, (16) and (20), to determine d for the power stage. To solve the problems, (19) is further expanded for any sensed $\hat{i}_L$ as:

$$d_c = \min\left\{\sqrt{\frac{-2\,\hat{i}_L \Delta S}{S_r S_f T_s}}, 1\right\}. \tag{21}$$

Then, d_c is utilized to transform the DCM i_L to the i_L of the special boundary case between the CCM and DCM. As shown in Figure 6 (b), the boundary case occurs when i i_L reaches zero exactly at T_s with the same slopes. The superscript (x') is introduced to the corresponding variables for the boundary case as:

$$V_c' = \frac{V_c}{d_c}. \tag{22}$$

$$\widehat{i_L'} = \frac{\widehat{i_L}}{d_c^2}. \tag{23}$$

Note that (16) is also applicable for the boundary case, so its duty cycle based on V_c' and $\widehat{i_L'}$ is:

$$d' = \frac{1}{2} + \frac{V_{rp}}{T_s \Delta S R_i} - \sqrt{\left(\frac{1}{2} + \frac{V_{rp}}{T_s \Delta S R_i}\right)^2 - \frac{2}{T_s \Delta S}\left(\frac{V_c'}{R_i} - \widehat{i_L'}\right)} \tag{24}$$

At last, the DCM duty cycle can be obtained by the reverse-transformation using (21) and (24) instead of (20) as:

$$d = d' d_c. \tag{25}$$

When the system works in the CCM, $d_c = 1$ and (25) provides the same result as (16). Therefore, a unified procedure is developed for the current control loop for different load conditions, which significantly simplifies the model implementation procedure.

3.3. POWER STAGE

As depicted in Figure 3, the control variable d from the feedback control loops is fed to the power stage to adjust the output. In this model, we mainly focus on the averaged behavior of the VRM to predict the low frequency response. Thus, the target variables are the averaged switching voltage $\widehat{v_{sw}}$ and the dc output voltage for the next cycle $V_{out,next}$.

The coefficient d_c is also applied here to unify the modeling of the CCM and DCM. Depending on the states of the MOSFETs and i_L, one switching cycle can be divided into three parts:

1) $(0 \sim d)T_s$. The high-side MOSFET is on and the low-side MOSFET is off. C_{out} is being charged by V_{in} (i_L increases).
2) $(d \sim d_c)T_s$. The high-side MOSFET is off and the low-side MOSFET is on. C_{out} is being discharged (i_L decreases).
3) $(d_c \sim 1)T_s$, which only occurs in the DCM ($d_c < 1$). The low-side MOSFET remains off and i_L already reaches zero. V_{sw} is equal to V_{out} during this period.

So the averaged switching voltage for the next cycle can be determined by combining all the three parts:

$$\widehat{v_{sw}} = d(V_{in} - r_{on,H}\widehat{i_L}) - (d_c - d)r_{on,L}\widehat{i_L} + (1 - d_c)V_{out}. \quad (26)$$

Since a dropout voltage, caused by the ESR of the inductor, exists between the switching and output nodes, the output voltage for the next cycle can be directly calculated as:

$$V_{out,next} = \widehat{v_{sw}} - r_L\widehat{i_L}. \quad (27)$$

3.4. MODEL IMPLEMENTATION

To simulate the voltage droop waveform in the time-domain and the PDN impedance in the frequency-domain, the proposed behavior model is implemented in a circuit simulator, Keysight Advanced Design System (ADS) [20].

The schematic of this model is illustrated in Figure 7, which clearly presents all the key components in the voltage control loop, the current control loop, and the power stage. The analytical equations can be implemented as circuit components using the Symbolically Defined Devices (SDD) of ADS. The "SDDnP" block indicates that this SDD component has "n" ports. For the voltage control loop, the output voltage is sensed by a voltage-

controlled voltage source (VCVS) with a specific time delay (t_d). Then, the LPF, the integrator, and the PI control are implemented by the SDD components ①, ②, and ③, respectively. For the current control loop, the inductor current is sensed by a current-controlled voltage source (CCVS). S_r, S_f, and $T_s\Delta S$ are calculated by the SDD component ④. The unified equations for the CCM and DCM, (21) and (24), are fulfilled by the SDD components ⑤ and ⑥. At last, the SDD component ⑦ represents (26) in the power stage, and (27) is directly executed by the circuit simulation for the next cycle $V_{out,next}$ (see Appendix for the detailed expressions of the SDD components).

By applying different simulation instances, the established circuit model can perform the transient and ac simulations. Therefore, it provides a straight-forward evaluation method in both the time-domain (TD) and frequency-domain (FD). This ADS based circuit simulation is introduced as an example to implement the proposed behavior model. Alternative implementation solutions may also be feasible based on other simulation tools.

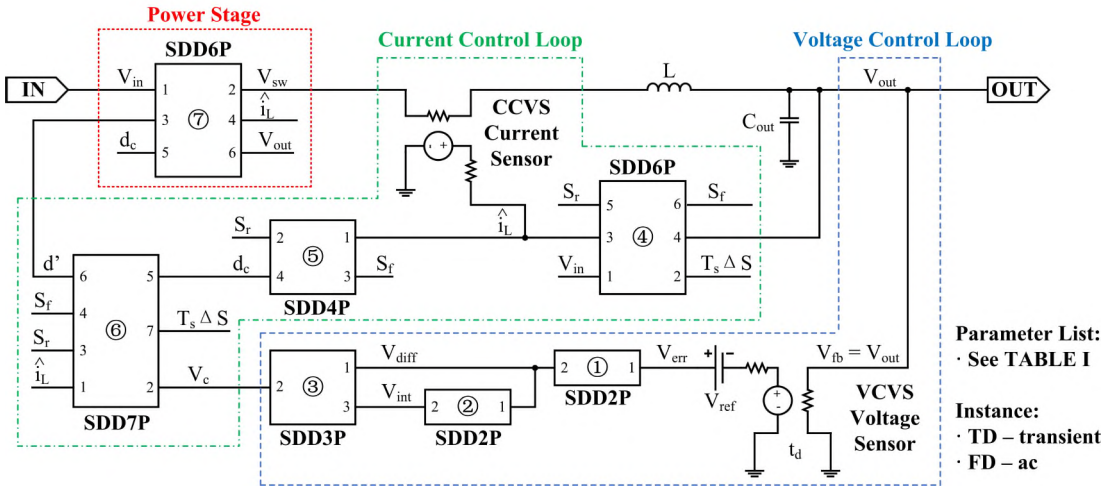


Figure 7. Schematic of the behavior model in the circuit simulator.

Table 1. VRM behavior model parameters.

Category	Parameter	Description
Fixed Parameters	V_{ref}	Internal reference voltage.
	f_s	Switching frequency.
	C_{out}	Output filtering capacitance.
	L, r_L	Output inductor and its ESR.
	$r_{on,H}$, $r_{on,L}$	On-resistance of the high-side and low-side MOSFETs.
Tuned Parameters	f_c	Cut-off frequency of the LPF.
	k_p, k_i, k_{dc}	PI control coefficients.
	t_d	Control delay.
	V_{rp}	Ramp voltage of the slope compensation.
	R_i	Current sensing gain.

4. CHARACTERIZATION AND VALIDATION

As discussed earlier, one of the biggest challenges in VRM modeling is the lack of knowledge for the actual design due to the IP-protection. With the assistance of the behavior model, the interior topology-level components are analyzed and implemented in the circuit simulator. Table 1 summaries the model parameters, which can be classified into two categories: the fixed and tuned parameters. The fixed parameters are accessible from the IC's datasheet, the PCB schematic, and other design files. The tuned parameters are related to the internal design of the VRM and not available at the system level. In this section, a measurement-based characterization is conducted on a power management IC (PMIC) EVB with the target VRMs to determine the tuned parameters. Using the same measurement setup, the behavior model with the finalized parameters is used to predict the voltage droops under different operating conditions. By comparing the simulated and

measured results, the proposed modeling method is validated for both single-phase and 3-phase VRMs.

4.1. MEASUREMENT SETUP

The measurement setup is depicted in Figure 8. The PMIC chip and its peripheral circuit components were already assembled on the PMIC EVB. The PMIC chip contained one single-phase and one 3-phase VRMs. Its input voltage V_{in}, ranging from 3.4 V to 4.2 V based on the typical battery voltage, was provided by the dc power supply (Keysight N6705B). The VRMs could be configured by the I2C commands, such as enabling the force-PWM mode, changing the desired output level, and setting the switching frequency. For the single-phase VRM, the output inductor was 0.47 μH with a 31 mΩ ESR, the effective output capacitance was 17 μF considering the derating effect. The output voltage was tunable from 0.7 V to 1.0 V and the switching frequency was 2.4 MHz. For the 3-phase VRM, the output inductor for each phase was 0.24 μH with a 18 mΩ ESR, the effective output capacitance for each phase was also 17 μF. The output voltage was fixed to 0.75 V and the switching frequency was 3.2 MHz. A custom-made slammer board was used to draw the step transient current at each VRM's output. The slammer boards were directly soldered on the PMIC EVB to minimize the connection impedance. In order to precisely control the amplitude and the slew rate of the load current, an external drive signal V drive was provided by the signal generator (Agilent 81150A). The maximum load current was 7 A with a minimum of 300 ns rising time. Both the output voltage and the current were monitored by an oscilloscope (Tektronix DPO5204B). There are several advantages in applying the time-domain measurements. First, the voltage droop in the time-

domain directly affects the stability of the system, so it is the most important criterion for characterizations and validations. Also, the measurement results are more accessible by using a less expensive instrument (i.e., an oscilloscope instead of a vector network analyzer). In addition, the output voltage waveform in the time-domain is helpful to determine proper initial values for the tuned parameters, which is further discussed in the "Parameter Optimization" section.

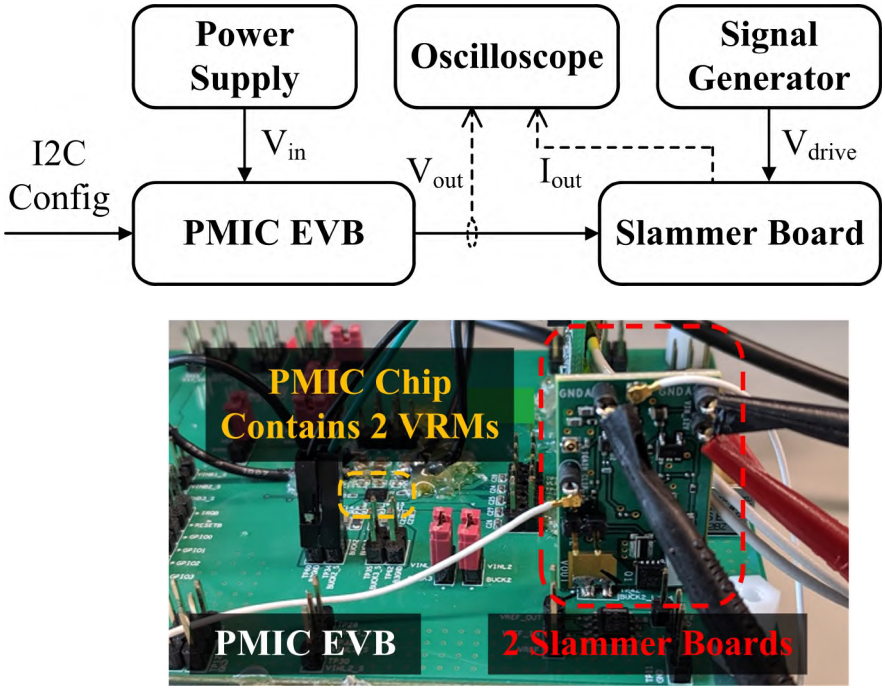


Figure 8. Diagram and photograph of the measurement setup.

4.2. PARAMETER OPTIMIZATION

The measurement-based characterization was conducted under the nominal operating condition. Using the single-phase VRM as an example, the input and output voltages were 3.8 V and 0.85 V, the amplitude of the load current was 2 A, and the rising

time was 1000 ns. The measured output voltage and load current waveforms are shown in Figure 9. The voltage droop in the time-domain is affected by all the model parameters. The goal of characterization is to achieve the same voltage droop waveform by optimizing the tuned parameters.

Conventionally, the trial-and-error method is used to test all the combinations of parameters within the ranges of interests. However, the 7 tuned parameters are coupled with each other, so this method is impractical and time-consuming. Therefore, a two-step procedure, including the initial step and the fine-tune step, is introduced to efficiently optimize the parameters.

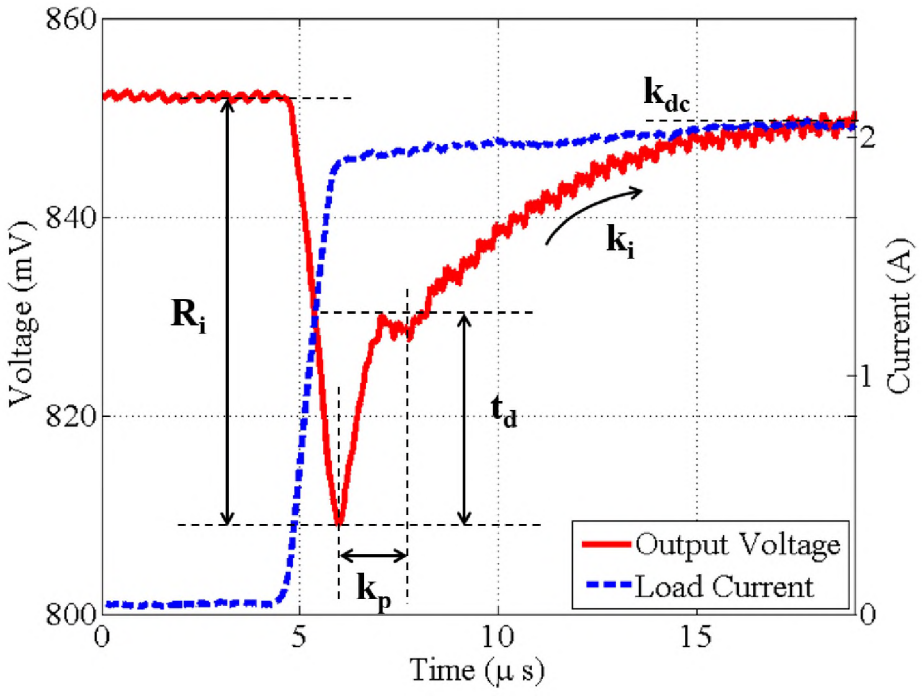


Figure 9. Measured voltage and current waveforms for characterization.

1) The initial step aims to set proper initial values for the tuned parameters, so the optimization in the next step can be expedited. Based on the characteristics of the control loops, the measured voltage waveform in the time-domain provides helpful information to determine the initial values, as illustrated in Figure 9. First, the voltage droop recovery (10 ~ 20 μs) is mainly dominated by the integrator of the voltage control loop, so k_i and k_{dc} are set based on the curvature and final level of the recovery part, respectively. Then, a ringing behavior can be observed after the first voltage droop (5 ~ 10 μs), which reflects the stability of the control loop. So for the remaining parameters of the voltage control loop, k_p mainly affects the ringing frequency and t_d can limit the ringing amplitude. After the initial values of the voltage control loop parameters are determined, R_i can be selected so that the the largest voltage droop (at 5 μs) can match with the measured result. At last, the other tuned parameters, f_c and V_{rp}, only have secondary effects on the voltage droop. It is suggested to set their initial values based on the general design guidelines. For example, f_c is set as two times of the switching frequency to filter out higher frequency noise. The typical compensating ramp slope is half of S_f [18], so the initial value of V_{rp} can be set as $-0.5S_fT_s$.
2) In the fine-tune step, the ADS built-in optimization tool is used to further adjust the parameters simultaneously based on the initial values. The goal is to minimize the error between the measured and simulated output voltage waveforms. The "Gradient" algorithm is chosen with maximum 200 iterations, while other optimization algorithms are also applicable. With the proper initial

value set for each tuned parameter, the optimization process can quickly converge and finalize the behavior model.

Following the same procedure, the measurement-based characterization is also conducted for the 3-phase VRM. Since the proposed model focuses on the averaged behavior of the VRM devices, the 3 output phases connected in parallel can be represented by one equivalent output inductor (1/3 of the inductance and ESR in one phase) and one equivalent capacitance (3 times of the capacitance in one phase). The optimized model parameters for both single-phase and 3-phase VRMs are listed in Table 2.

Table 2. Characterized single-phase and 3-phase VRM models.

Category	**Parameter**	**Single-Phase**	**3-Phase**
Fixed Parameters	V_{ref}	0.85 V	0.75 V
	f_{s}	2.4 MHz	3.2 MHz
	C_{out}	17 μF	51 μF
	L	0.47 μH	0.08 μH
	r_{L}	31 mΩ	20 mΩ
	$r_{\text{on,H}}$	60 mΩ	34 mΩ
	$r_{\text{on,L}}$	23 mΩ	13 mΩ
Tuned Parameters	f_{c}	6.0 MHz	6.7 MHz
	k_{p}	35	36
	k_{i}	$8.0e^6$	$18.6e^6$
	k_{dc}	980	775
	t_{d}	180 ns	288 ns
	V_{rp}	0.22 V	0.28 V
	R_{i}	0.70	0.74

4.3. MODEL VALIDATION

The novel method to unify the modeling of the CCM and DCM is firstly validated using the single-phase VRM model. Then, the simulated voltage droops from the finalized behavior models are compared with the measured results under various operating conditions for both single-phase and 3-phase VRMs.

The input voltage was 3.8 V and output voltage was configured to be 0.85 V on the single-phase VRM. By gradually increasing the load current from 0.05 A to 2 A, the operation mode of this VRM changed from the DCM to the CCM at the boundary current of 0.5 A. Figure 10 shows the simulated duty cycles for a 2 A step transient current load under the same configuration. The dash-dotted line, which represents d_c calculated based on (21), has a turning point at 5.32 µs. When the boundary case between the DCM ($d_c < 1$) and the CCM ($d_c = 1$) occurs, the corresponding averaged inductor current $\hat{i}_L$ is 0.5 A, which agrees with the measured boundary current. The duty cycle d, calculated based on (25), is depicted as the solid line. When $\hat{i}_L = 0.05$ A, d remains low at 0.08 for the DCM. As $\hat{i}_L$ increases to 2 A and the voltage droop occurs, d is then increased up to 0.58 by the feedback control loops. After the output voltage recovers to 0.85 V in the CCM, d is stabilized at 0.25, which matches with the ratio of the output and input voltages considering the additional power losses due to the MOSFET's on-resistance and the inductor's ESR. Thus, the proposed unified equations are proved to model the load transition between the CCM and DCM correctly.

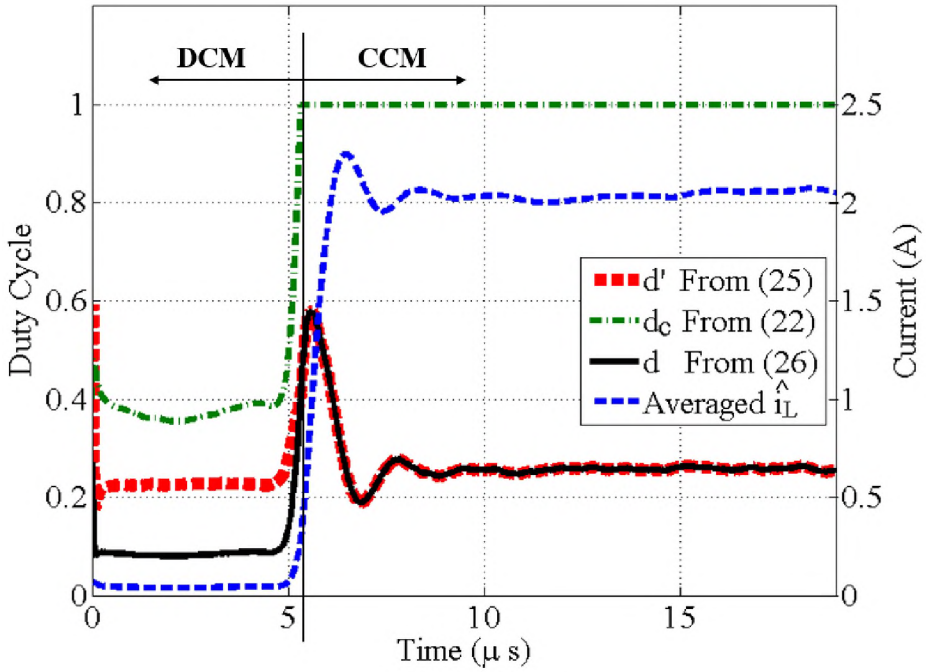


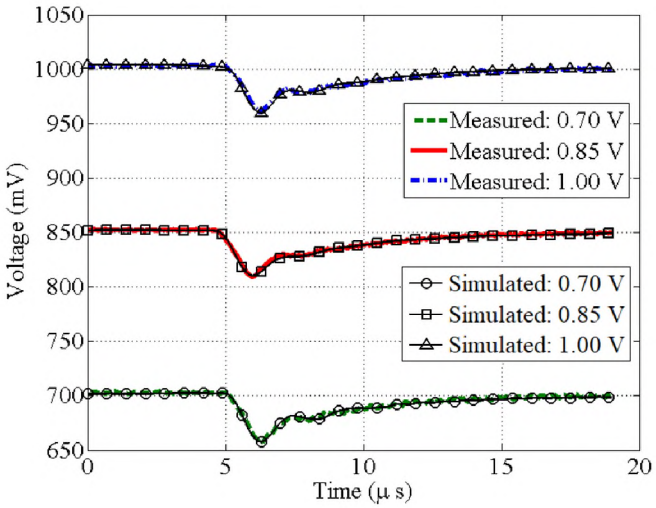
Figure 10. Validation of the unified equations for the CCM and DCM.

Figure 11 and Figure 12 show the comparisons between the simulated and measured voltage droop waveforms for single-phase and 3-phase VRMs, respectively. Different operating conditions, including the output voltage level (0.7 V ~ 1.0 V for the single-phase, fixed 0.75 V for the 3-phase), the load current amplitude (0.5 A ~ 2.0 A for the single-phase, 4 A ~ 7 A for the 3-phase), and the load current rising time (300 ns ~ 1000 ns), were investigated. It should be noted that the output voltage of the 3-phase VRM was fixed to 0.75 V, so we instead compared the voltage droops of different rising time at two load current amplitudes (5 A and 6 A). In addition, the voltage waveforms in Figure 11 (c), Figure 12 (b), and Figure 12 (c) are shifted by ±5 ns for better displaying purposes. The simulated and measured results have good correlations with each other for all the conditions. The maximum differences are within ±1.3 mV and ±1.9 mV for single-phase

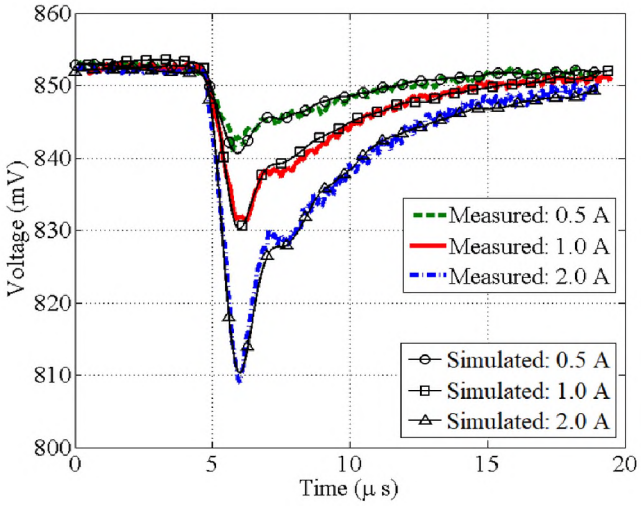
and 3-phase VRMs, respectively. It implies that the behavior model with the optimized parameters can accurately predict the voltage droop waveform in the time-domain.

The circuit model implemented in ADS (Figure 7) can also simulate the magnitude and phase of the PDN impedance with the ac instance. To validate the simulated frequency-domain result, the classic shunt-thru method was used to achieve accurate mΩ impedance measurements [21]. Two semi-rigid probes were mounted at the output power and ground pads of the single-phase VRM, the transmission coefficient S_{21} was measured by the vector network analyzer (Keysight E5061B) while the VRM was in the active state. Then, the PDN impedance was converted based on the measured S_{21} as: $Z_{PDN} = 25 \cdot S_{21} / (1 - S_{21})$. The frequency range in this measurement was from 50 Hz to 5 MHz. Full 2-port calibration was applied to move the reference planes to the connectors of the semi-rigid probes. Further port extension to the end probe tips was not required because the probe length was electrically short in regard to the target frequency range. The simulated and measured impedance are compared in Figure 13. Good agreements for both the magnitude and phase can be observed up to 1 MHz, so the results validate the accuracy of the proposed model within the desired frequency range. In addition, this model can be cascaded with the backend PCB and package circuits, which is useful to generate the end-to-end PDN impedance curve as illustrated in Figure 2 (b).

(a) Different output voltage levels.



(b) Different load current amplitudes.



(c) Different load current rising times.

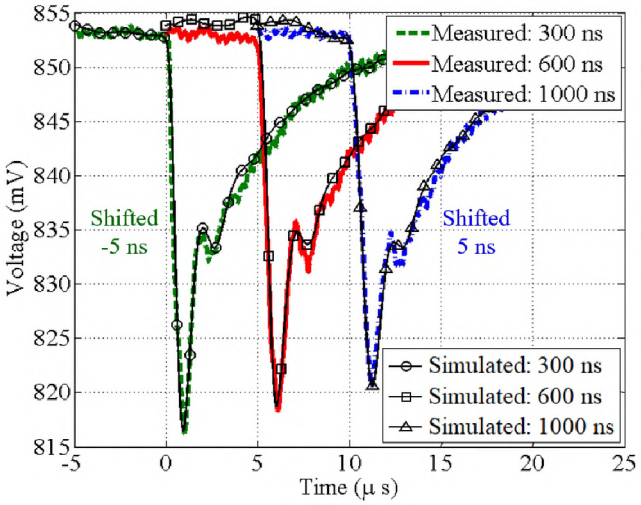
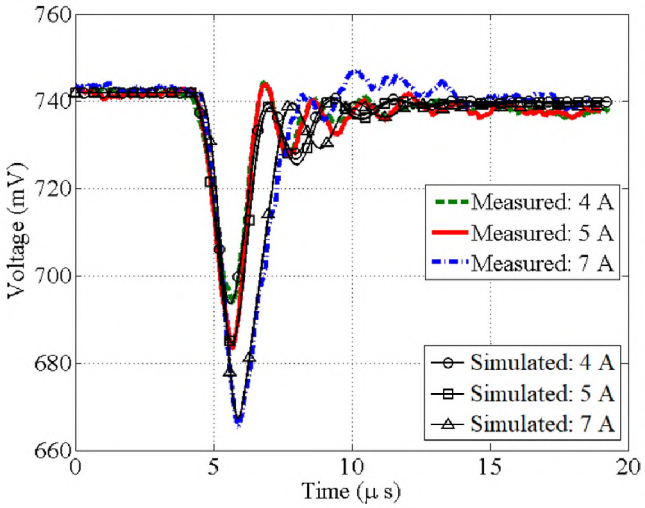
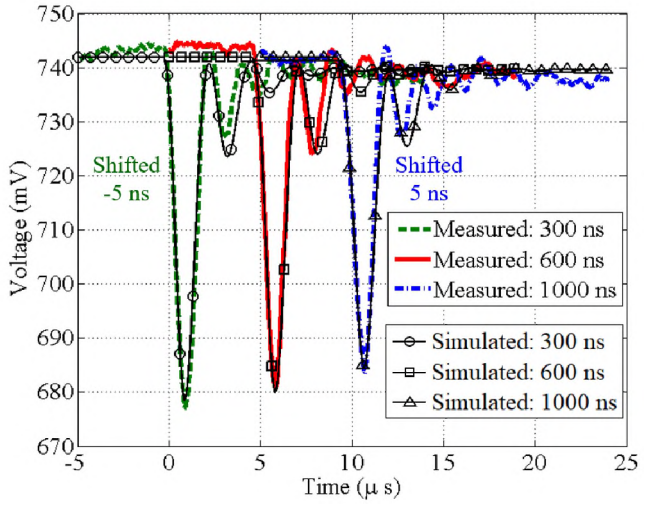


Figure 11. Comparison of voltage droop waveforms for single-phase VRM.

(a) Different load current amplitudes.



(b) Different rising times at 5 A current.



(c) Different rising times at 6 A current.

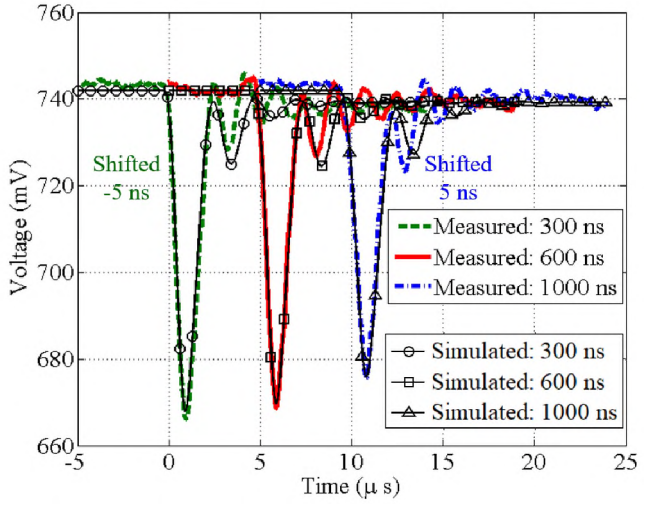
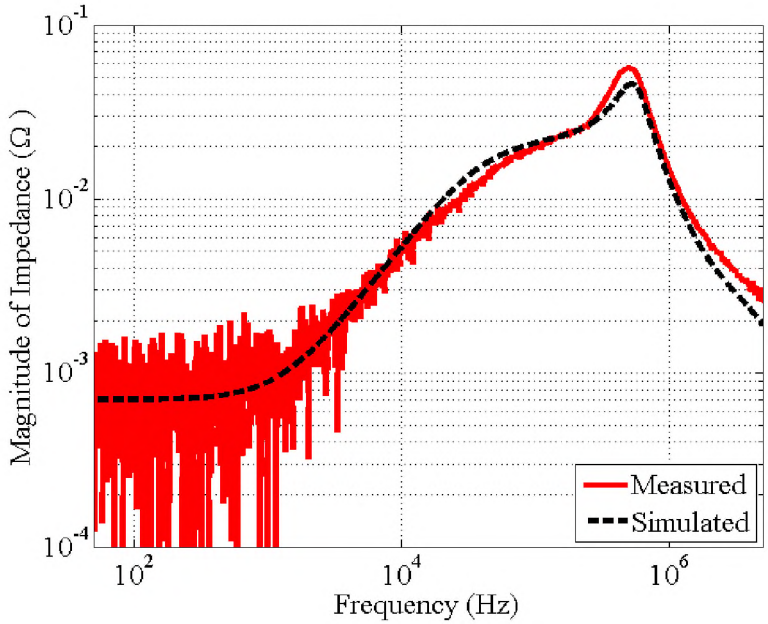


Figure 12. Comparison of voltage droop waveforms for 3-phase VRM.

(a) Magnitude.



(b) Phase.

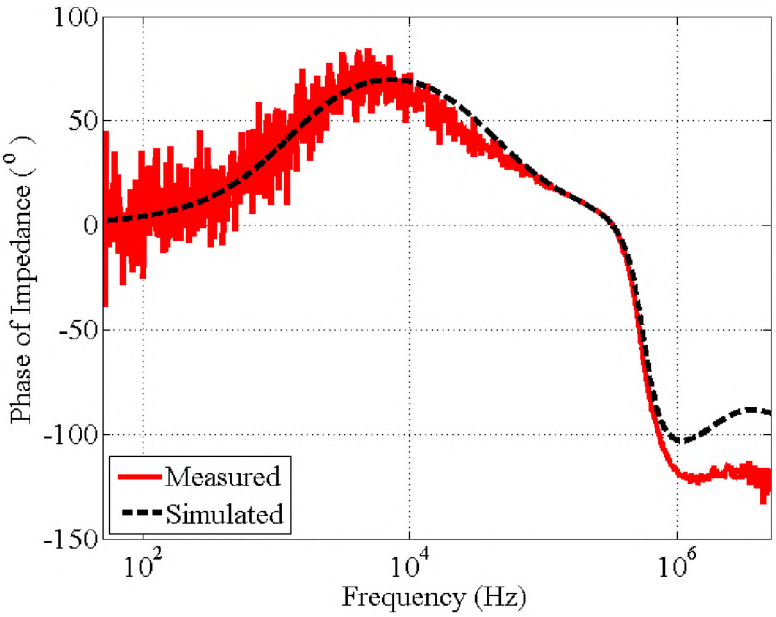


Figure 13. Comparison of simulated and measured impedance for single-phase VRM.

5. CONCLUSION

In this work, the topology and modeling challenges for the VRM are discussed. To overcome the challenges, a generic behavior model based on the current-mode topology is developed. This behavior model includes all the key components in the voltage control loop, the current control loop, and the power stage of an actual VRM device. A novel method is also proposed to unify the modeling of the CCM and DCM for different load conditions and simplify the implementation for circuit simulations. The model parameters are optimized based on the measurement-based characterization. Good accuracy of this model is observed by the comparisons between the simulated and measured results for both single-phase and 3-phase VRMs. The optimized VRM model can accurately predict the voltage droop waveforms in the time-domain and the PDN impedance in the frequency-domain under various operating conditions. Cascading the proposed VRM model with the PCB-level and package-level PDN models enables a combined PDN analysis, which is much needed for modern PDN designs.

APPENDIX

The analytical equations of the behavior model are implemented as the SDD components in Figure 7. In the expression of an "SDDnP" component, "v_i" represents the signal at port i (i = 1, 2, 3 ... n). The full expressions of all the SDD components are listed below.

- SDD component ① (SDD2P, LPF):

$$\mathrm{I}[1,0] = 0$$
$$\mathrm{F}[2,0] = \_v_2 - \_v_1$$
$$\mathrm{F}[2,1] = \_v_2/(2\pi f_\mathrm{c})$$

- SDD component ② (SDD2P, integrator):

$$\mathrm{I}[1,0] = 0$$
$$\mathrm{F}[2,0] = \_v_2/k_\mathrm{dc} - \_v_1$$
$$\mathrm{F}[2,1] = \_v_2/k_\mathrm{i}$$

- SDD component ③ (SDD3P, PI control):

$$\mathrm{I}[1,0] = \mathrm{I}[3,0] = 0$$
$$\mathrm{F}[2,0] = -\_v_2 + \min\{\max\{\_v_1 \cdot k_\mathrm{p} + \_v_3, -3\}, 3\}$$

- SDD component ④ (SDD6P, current feedback):

$$\mathrm{I}[1,0] = \mathrm{I}[3,0] = \mathrm{I}[4,0] = 0$$
$$\mathrm{F}[2,0] = -\_v_2 + 1/f_\mathrm{s} \cdot (\_v_1 + \_v_3 \cdot (r_\mathrm{on,L} - r_\mathrm{on,H}))/L$$
$$\mathrm{F}[5,0] = -\_v_5 + (\_v_1 - \_v_3 \cdot (r_\mathrm{on,H} + r_\mathrm{L}) - \_v_4)/L$$
$$\mathrm{F}[6,0] = -\_v_6 + (-\_v_3 \cdot (r_\mathrm{on,L} + r_\mathrm{L}) - \_v_4))/L$$

- SDD component ⑤ (SDD4P, dc calculation):

$$\mathrm{I}[1,0] = \mathrm{I}[2,0] = \mathrm{I}[3,0] = 0$$
$$\mathrm{F}[4,0] = -\_v_4 + \min\{\sqrt{2 \cdot \_v_1 \cdot (\_v_3 - \_v_2)/(\_v_3 \cdot \_v_2 \cdot f_\mathrm{s})}, 1\}$$

- SDD component ⑥ (SDD7P, duty cycle):

$$\mathrm{I}[1,0] = \mathrm{I}[2,0] = \mathrm{I}[3,0] = \mathrm{I}[4,0] = \mathrm{I}[5,0] = \mathrm{I}[7,0] = 0$$
$$\mathrm{F}[6,0] = -\_v_6 + \min\{\max\{0.5 + V_\mathrm{rp}/\_v_7/R_\mathrm{i} - \sqrt{(0.5 + V_\mathrm{rp}/\_v_7/R_\mathrm{i})^2 - 2/\_v_7(\_v_2/\_v_5/R_\mathrm{i} - \_v_1/\_v_5^2)}, 0\}, 1\}$$

- SDD component ⑦ (SDD6P, power stage):

$$\mathrm{I}[1,0] = \_v_3 \cdot \_v_5 \cdot \_v_4$$
$$\mathrm{F}[2,0] = -\_v_2 + \_v_3 \cdot \_v_5 \cdot (\_v_1 - \_v_4 \cdot r_\mathrm{on,H}) - (1 - \_v_3)\_v_4 \cdot \_v_5 \cdot r_\mathrm{on,L} + (1 - \_v_5) \cdot \max\{\_v_6, 0\}$$
$$\mathrm{I}[3,0] = \mathrm{I}[4,0] = \mathrm{I}[5,0] = \mathrm{I}[6,0] = 0$$

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III. ACCURATE RECTIFIER CHARACTERIZATION AND IMPROVED MODELING OF CONSTANT POWER LOAD WIRELESS POWER TRANSFER SYSTEMS

ABSTRACT

Wireless power transfer (WPT) is an emerging technology deployed for a wide range of applications. Various design challenges need to be addressed at both circuit and system levels. However, the conventional modeling methods either require impractical assumptions or only focus on the coil-to-coil part. This article presents a system-level model for WPT applications, including all the critical interior blocks, such as power amplifier, transmitter coil, receiver coil, matching networks, and rectifier. An accurate characterization method is proposed to obtain the rectifier impedance as a realistic load condition. Then, through frequency harmonic analysis, the power capabilities along the power flow path are analytically derived for both the fundamental and higher order harmonic components. The system efficiency and the power loss at each block can be accurately estimated. As a result, this model can not only optimize the system performance, but also help improve the thermal design for WPT products. With the assistance of this improved model, a practical design methodology is introduced to optimize the system parameters. An experimental prototype is built to validate the proposed model and the design methodology. Good correlations are observed between the calculations and experiments in both the time-domain and frequency-domain results.

1. INTRODUCTION

Wireless power transfer (WPT) is an emerging technology that brings great convenience toc harging a large variety of electronic devices. It has been widely deployed for domestic and industrial applications, including cell phones, home electronics, medical implants, and electric vehicles [1]–[4]. These applications usually have different requirements on power level, efficiency, physical size, and operating frequency. WPT standards, such as Qi from Wireless Power Consortium [5] and J2954 from the Society of Automotive Engineers [6], have been proposed to improve the interoperability and the safety protection of WPT applications.

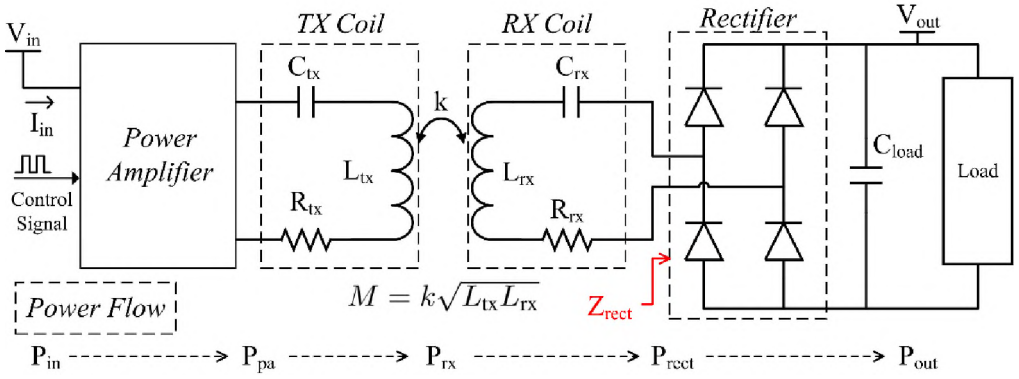


Figure 1. Typical WPT system with the SS topology.

In addition to the standards and regulations, it is crucial to minimize the power loss and improve the efficiency of WPT systems, since the dissipated heat of devices may cause potential safety issues and throttle the charging performance. There are three major challenges in designing a power efficient WPT system. First, it remains an unresolved question to achieve the optimal efficiency at the system level. As shown in Figure 1, a

typical WPT system is formed by multiple blocks, including the power amplifier, the magnetic coils, the matching networks, and the rectifier. It is worth noting that the optimal configuration of a single block may not correspond to the peak efficiency of the entire system. Second, the power loss of each block in a WPT system needs to be estimated accurately. Because of the increasing power levels, the thermal design becomes more important for the electronic products. An effective thermal design needs to account for not only the end-to-end total loss, but also the dissipated power at each block along the power flow path. Third, there are no practical methodologies to simultaneously optimize multiple system parameters, such as the coil matching capacitance, the operating frequency, and the input voltage level. The conventional trial-and-error method requires extensive measurements on a prototype system, which is time-consuming and expensive. These challenges limit the performance for a wide range of WPT applications, including the cell phones and electric vehicles [3]. To overcome these challenges, an accurate system-level model is desired to conduct the global optimization and loss estimation for all the blocks in a WPT system.

Over the past few decades, various studies have been carried out to investigate WPT designs at both coil and system levels [7]–[12]. Among these studies, a magnetic coil design methodology for the WPT system was presented in [7]. In addition to magnetic coils, matching networks and other system parameters are also critical to maximize efficiency. In [8] and [9], the power transfer capability was analyzed under different matching topologies for the coupled coils. However, the output load of the coils was assumed to be purely resistive, which is impractical because the nonlinear rectifier device may contribute reactance components to the load in real WPT systems. The effects of

rectifier input impedance were discussed in [10] and [11]. However, the authors in [10] only focused on the resonant condition and ignored the case when nonzero line impedance is present at the ac side of the rectifier. In addition, the rectifier impedance was obtained from PSPICE simulations, but the PSPICE model may be unavailable for many devices because of the lack of support or confidential concerns. In [11], an analytical model of the rectifier impedance was established for the positive half-cycles, but it neglected the nonlinearity caused by the line-commutation process. Zhang et al. presented analytical expressions of coil efficiency with both frequency and voltage tuning [12]. The derivations were based on the first harmonic approximation (FHA), which becomes inaccurate when the operation condition is not at the resonant frequency [13]. Other conditions from the existing WPT products also make FHA inaccurate, such as the low-voltage operation of the cell phone wireless charger, the low power charging mode that causes the loaded quality factor decreasing [14], and the frequency splitting and bifurcation phenomena due to high coupling coefficient [15].

This article aims to provide a comprehensive discussion on the system-level modeling for kilohertz WPT applications. The limitations of the existing models are investigated based on circuit-level simulations in Section 2. To overcome these issues, an accurate characterization method for the rectifier is proposed in Section 3. It provides a feasible solution to obtain the rectifier impedance, which is included as a realistic load condition for the improved WPT system model in Section 4. Using this model, a design methodology is introduced to determine the optimized parameters for a WPT system. Then, an experimental prototype is implemented to validate the proposed model and the design methodology in Section 5. Finally, Section 6 concludes this article.

2. TOPOLOGY AND PREINVESTIGATION

A typical WPT system (see Figure 1) consists of four blocks: 1) the power amplifier, to convert dc input voltage Vin and current Iin to ac power, which is commonly implemented by half-bridge or full-bridge topology; 2) the transmitter (TX) coil with self-inductance L_{tx} and matching capacitance C_{tx}; 3) the receiver (RX) coil with self-inductance L_{rx} and matching capacitance C_{rx}; and 4) the rectifier, to inversely regulate ac power to dc output voltage V_{out}.

In this article, the series-series (SS) matching topology is used. Other matching topology, such as parallel-series, series-parallel, and parallel-parallel, can be derived in a similar manner [8], [9]. For the remaining parameters in Figure 1, R_{tx} and R_{rx} are the equivalent series resistances (ESRs) of the coils and matching capacitors. k is the coupling coefficient of the coupled magnetic coils. Then, the mutual inductance can be expressed as $M = k\sqrt{L_{tx}L_{rx}}$. C_{load} is the smoothing capacitor at the rectifier's output. It is a common practice for WPT applications to add sufficiently large C_{load} to stabilize the output voltage, so the output voltage ripple can be neglected. Z_{rect} is the input impedance seen at the rectifier input port. Figure 1 also illustrates the power flow of a WPT system, including TX input power P_{in}, power amplifier output P_{pa}, transferred power to the RX side P_{rx}, rectifier input power P_{rect}, and RX output power P_{out}. The rated output power is typically specified as a requirement in the early design stage, and the output voltage is constant in WPT systems [16]–[18]. For the design purpose of efficiency optimization under the maximum output power, this article focuses on the constant power load (CPL) condition with fixed output voltage.

To investigate the limitations of assumptions used in the existing methods, a circuit model is built in an RF simulator, Keysight Advanced Design Systems, based on the WPT system with the SS topology. As some WPT models only focused on the coil-to-coil part, the system efficiency is compared with the coil-only efficiency to show the significance of other blocks in the system. Then, the inaccuracy of FHA is investigated by the comparison between the time-domain and frequency-domain results. Finally, by applying different load conditions to the RX coil's output, the simulations demonstrate that inaccurate estimation of the efficiency can be caused by the pure resistive load assumption. Therefore, it is important to model the WPT system with a realistic load impedance.

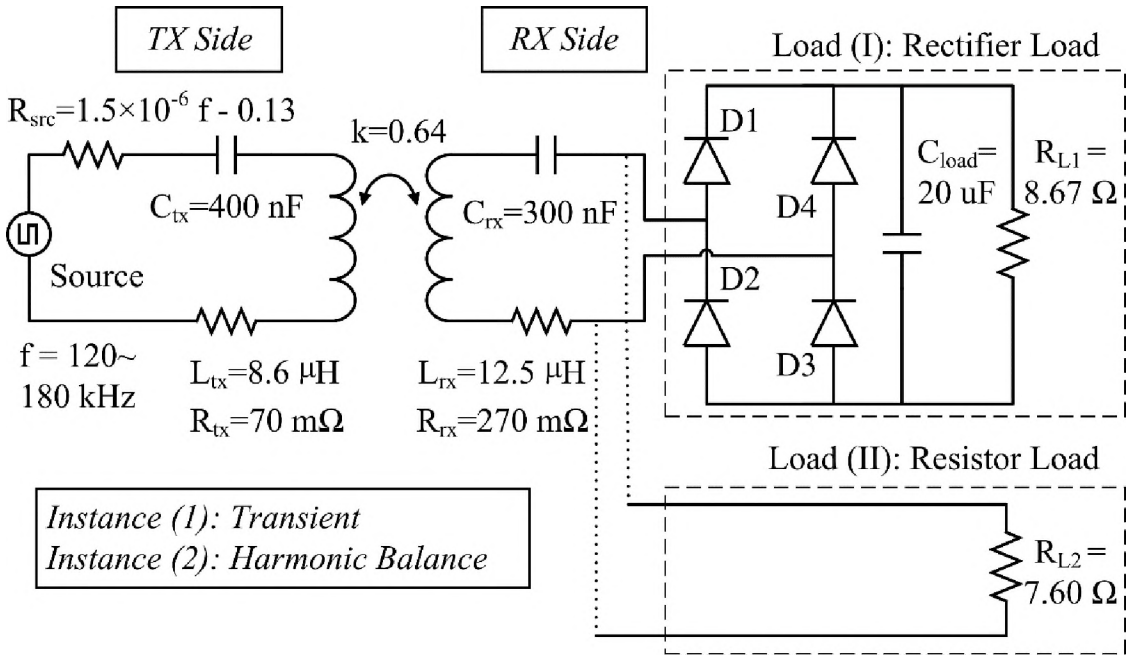


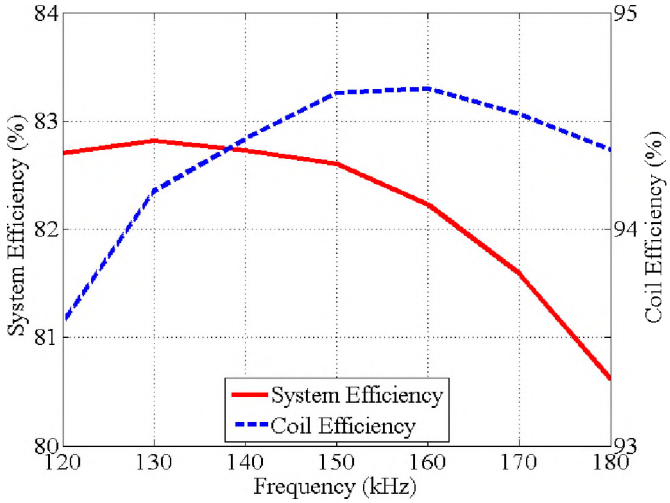
Figure 2. Diagram of the circuit model for preinvestigation.

The configuration of this circuit model is depicted in Figure 2. The value of each element is chosen based on a Qi-standard cell phone WPT system. This model can be simulated in both time and frequency domains by different simulation instances. On the TX side, the power amplifier is simplified to a trapezoidal-wave voltage source. The amplitude of this voltage source is between $-V_{in}$ and V_{in}; the operating frequency is f. A frequency-dependent equivalent resistor R_{src} is used to account for the power loss caused by the power amplifier. The function of R_{src} is determined by fitting the simulated power loss to the measured power loss of an existing power amplifier. Even though the equivalent resistor simplification cannot accurately model the loss of the power amplifier, it is sufficient to preinvestigate the limitations of the existing methods. A more rigorous modeling method is discussed in Section 4. On the RX side, the output power is fixed at 8 W. The CPL condition is satisfied by tuning V_{in} and f. Two load configurations are applied: (I) a full-bridge rectifier (D1-D4) with the load resistor R_{L1}; and (II) a pure resistor load R_{L2} directly connected to the RX matching network. To ensure similar output power levels for the two load configurations, $R_{L2}$is converted from R_{L1} based on the approximated effective resistance equation [14]:

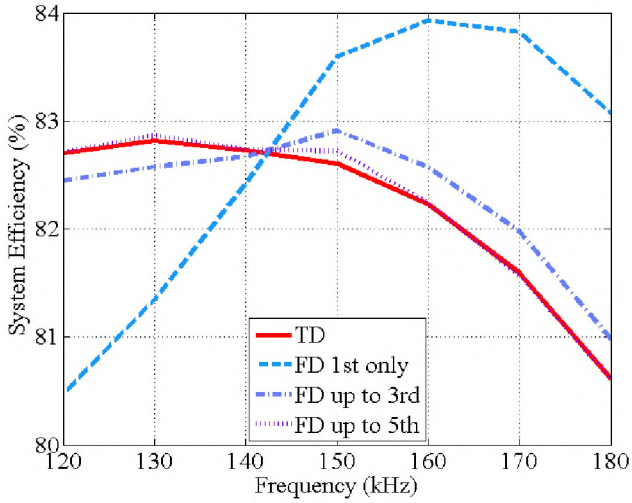
$$R_{L2} = \frac{8R_{L1}}{\pi^2}\left(1 + \frac{2V_{fw}}{V_{out}}\right), \tag{1}$$

where V_{fw} = 0.34 V is the forward voltage of the rectification diode, and V_{out} = 8.33 V is the rectifier output voltage.

(a) Comparison of system and coil-to-coil efficiencies.



(b) Comparison of efficiencies in time and frequency domains.



(c) Comparison of the system efficiencies under two load configurations.

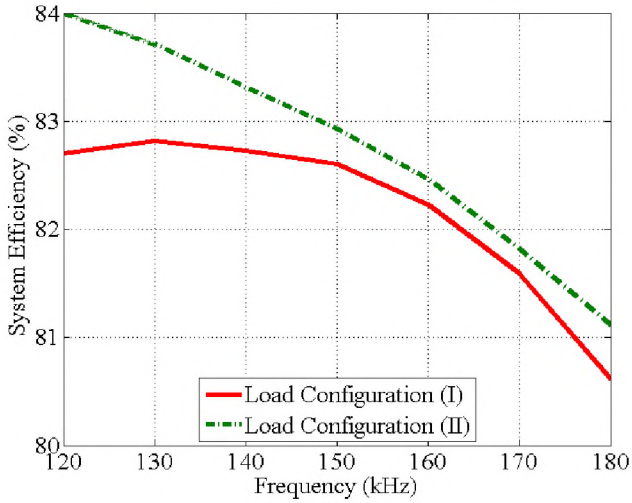


Figure 3. Simulation results of the circuit model.

2.1. INVESTIGATION OF SYSTEM AND COIL EFFICIENCY

Figure 3 (a) compared the system and coil efficiencies at different frequencies using load configuration (I). The system and coil efficiencies, η_{sys} and η_{coil}, were calculated as

$$\eta_{sys} = \frac{P_{out}}{P_{in}} \cdot 100\%, \tag{2}$$

$$\eta_{coil} = \frac{P_{rect}}{P_{pa}} \cdot 100\%, \tag{3}$$

where P_{in} and P_{out} are the input and output powers, respectively, and P_{pa} and P_{rect} are the power amplifier output and rectifier input powers, respectively.

Note that the peak system efficiency is achieved at a lower frequency compared with the peak coil efficiency. This implies that the TX and RX coil blocks are not the only factors determining the efficiency for a WPT system. Other blocks also have significant contributions; one important loss term related to frequency is the MOSFET switching loss of the power amplifier [19]. As the frequency increases from 120 to 180 kHz, the simulated loss of the power amplifier reaches up to 583 mW. In addition, the design of coil's matching network also affects the current flowing through all the blocks, which could affect the loss of the power amplifier and the rectifier. In the simulations and optimizations for real-world WPT applications, a system-level model is preferred over a coil-to-coil only model.

2.2. INVESTIGATION OF HARMONIC FREQUENCY

The simulated system efficiencies in the time and frequency domains, using the load configuration (I), were compared in Figure 3 (b). For the time-domain simulation, the steady-state voltage and current waveforms were directly multiplied in a unit time step to

calculate the input and output powers. The system efficiency in the time domain was obtained based on (2). For the frequency-domain simulation, with the dc output power fixed to 8 W, the input power carried by each frequency component was calculated individually by the magnitudes and phase difference of the simulated voltage and current. Then, the system efficiencies in the frequency domain were determined using the input power of the fundamental frequency only ("FD 1st only"), the input power including up to the third-order harmonics ("FD up to 3rd"), and the input power including up to the fifth-order harmonics ("FD up to 5th").

As shown in Figure 3 (b), only at the crossing point, the efficiency calculated by the fundamental frequency component can match with the time-domain efficiency. It is because the input power of higher order harmonics is zero due to the 90^{o} phase angle between the voltage and current, and only the fundamental frequency component carries the input power. With the increasing offset to this condition, the difference of the efficiencies using the fundamental frequency component and using the time-domain component becomes larger. It implies that FHA is not applicable, and higher order harmonic components should not be neglected. The inaccuracy of FHA is mainly due to two reasons. First, the voltage source of a real WPT system is not sinusoidal. Second, the nonlinearity of the rectifiers is not taken into consideration in FHA [20]. Therefore, a valid WPT model should have the capability to characterize the power distributed at both fundamental frequency and higher order harmonics. The waveform in a WPT system typically has a 50% duty cycle, so the power carried by even harmonics is negligible. For all practical purposes, the fundamental, third-order, and fifth-order harmonic components are the most critical terms in a WPT model.

2.3. INVESTIGATION OF RECTIFIER IMPEDANCE

The system efficiencies of two load configurations were compared in Figure 3 (c). Since the circuit of the load configuration (II) has no rectifier, to maintain the validity of this comparison, the output power in this case was estimated using an artificial full-bridge rectifier with a forward voltage V_{fw} of the rectification diode

$$P_{out}^{\text{Load (II)}} = P_{L2} \cdot \frac{V_{out}}{V_{out} + 2V_{fw}}, \tag{4}$$

where P_{L2} is the simulated power at R_{L2}, and V_{fw} and V_{out} are defined the same as (1). Then, the system efficiency can be calculated based on (2).

In load configuration (I), the simulated rectifier reactance varies from 0 to 1.34 Ω at different frequencies. The nonzero reactance at the RX side could affect the reflected impedance at the TX side and change the coil efficiency. With the absence of this rectifier reactance, in load configuration (II), the coil efficiency has less variation at different frequencies. As a result, the pure resistor load model gives a misleading estimation for the system efficiency and the optimal operation point. Therefore, a realistic load configuration is important to accurately model the efficiency in WPT systems. Both real and imaginary parts of the load impedance should be included in the model. It is also desirable to develop a practical characterization method for the provided rectifier diodes or ICs, in order to obtain the accurate impedance under various conditions.

3. ACCURATE RECTIFIER CHARACTERIZATION

The rectifier is a common nonlinear device in ac-dc power systems. The nonlinearity of the rectifier is mainly caused by the parasitic of the rectification diode [21] and the line-commutation process [22]. Figure 4 depicts the circuit model of a full-wave diode rectifier. The source voltage is denoted as v_s. At the dc output port of the rectifier, there are output voltage v_{dc} and output current i_{dc}. The dc component of i_{dc} is I_d. The load resistance and the smoothing capacitor are R_{load} and C_{load}, respectively. At the input port of the rectifier, there are ac voltage v_{ac} and ac current i_{ac}. The ac-side line impedance is defined as $Z_{line} = R_{line} + jX_{line}$. The line resistance R_{line} will cause the voltage drop from the source to the rectifier input. Since its value is determined by the ac resistance of the coils and the ESR of the matching capacitors, which is typically tens of milliohm, R_{line} can be neglected as a common practice. X_{line} is calculated by the line impedance of the RX side and the reflected impedance from the TX side as

$$X_{\text{line}} = \omega L_{\text{rx}} - \frac{1}{\omega C_{\text{rx}}} - \frac{(\omega M)^2}{\left(\omega L_{\text{tx}} - \frac{1}{\omega C_{\text{tx}}}\right)}, \tag{5}$$

where L_{tx} and L_{rx} are the TX and RX coil inductances, respectively, C_{tx} and C_{rx} are the TX and RX matching capacitances, respectively, M is the mutual inductance between two coils, and ω is the angular operating frequency. Depending on the coil inductance, matching network, and operating frequency, nonnegligible X_{line} may present at the input of the rectifier.

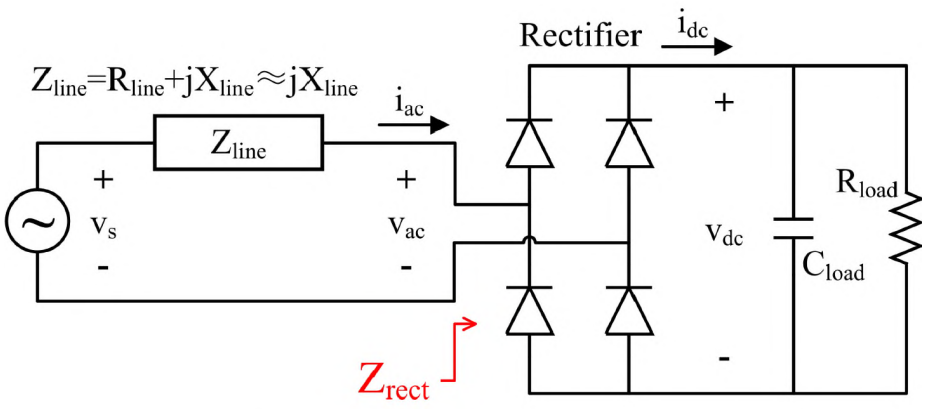


Figure 4. Circuit model of a full-wave diode rectifier.

Based on the small-signal analysis [22]–[25], the source voltage v_s consists of a sinusoidal wave v_1 and a small-signal perturbation Δv_p: $v_s = v_1 + \Delta v_p$. The amplitude of Δv_p is much smaller than that of v_1: $|v_1| = V_1, |\Delta v_p| = V_p$ with $V_p \ll V_1$. The rectifier impedance Z_{rect} can be expressed as follows (see the Appendix for the full derivation):

$$Z_{\text{rect}} = \frac{(\Delta v_p - \Delta S\ I_d\ Z_{\text{line}})\ (2Z_{\text{line}} + R_{\text{load}})}{2S\ \Delta S\ v_1 + S^2\ \Delta v_p - 3S^2\ \Delta S\ I_d\ Z_{\text{line}}}, \tag{6}$$

where S and ΔS are the nonlinear switching functions; S accounts for the line-commutation process and the parasitic of the rectification diode [22], and ΔS accounts for the change of nonlinearity caused by the input perturbation [24]. v_1 and v_p can be further expanded into the complex forms at the perturbation frequency with the amplitudes V_1 and V_p, respectively. The nonlinearity of perturbation ΔS is proportional to Δv_p with the same amplitude, so V_p is canceled. As a result, Z_{rect} is a function of the operating frequency, the input voltage amplitude V_1, the dc load current I_d, the load impedance R_{load}, and the input line impedance Z_{line}.

With the focus on the main nonlinear behaviors caused by the line-commutation process and the parasitic of the rectification diode ($S \neq 0, \Delta S = 0$), (6) can be simplified to (7). In addition, the line resistance R_{line} can be neglected as a common practice, so $Z_{line} = jX_{line}$

$$Z_{\text{rect}}|_{\Delta S=0} = \frac{2jX_{\text{line}} + R_{\text{load}}}{S^2}. \tag{7}$$

It implies that the rectifier impedance is mainly affected by X_{line} and load impedance R_{load}. With the CPL condition applied to the WPT systems, X_{line} becomes an effective criterion to characterize the rectifier impedance.

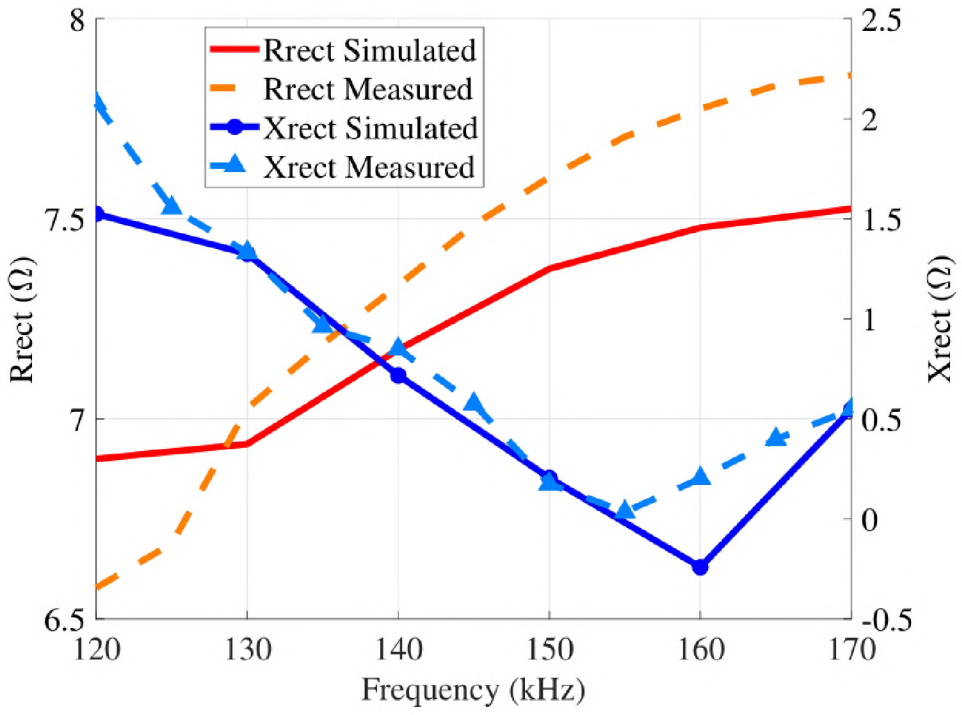


Figure 5. Comparison of simulated and measured rectifier impedance.

As discussed in [22], a standard sign function is used to represent the line-commutation process of the nonlinear switching function S. However, the analytical model described in this article is based on the assumption that no input line impedance is present at the ac side of the rectifier. It is not applicable to the kilohertz WPT system because X_{line} is commonly nonnegligible when the system is operating in an off-resonance condition. Another method to obtain the rectifier impedance is from the circuit simulation, where users need to correctly set all the parameters for the target device under simulation. Some electrical parameters, such as forward voltage drop (V_{fw}) and reverse break down voltage (B_v), are accessible from the datasheet. However, some physical parameters, such as junction grading coefficient (m), emission coefficient (N), saturation current (I_s), parasitic resistance (R_s), zero-bias junction capacitance (C_{jo}), and transit time (T_t), are either unavailable or require complicated calculations based on the figures in the datasheet. To investigate the accuracy of the circuit simulation for the rectifier impedance, a full-bridge rectifier using four Schottky diodes (SBR3U40P1) was simulated. In spite of the specified parameters, the unavailable parameters, including m, N, and T_t, were set using the recommended values from [26]. Other parameters, such as I_s, R_s, and C_{jo}, were calculated or extracted based on the typical characteristics and capacitance figures from the datasheet as $m = 0.333, N = 2, I_s = 1.8e-3\ A, R_s = 34\ m\Omega, C_{jo} = 80\ pF, T_t = 0\ ns, B_v = 40\ V$. The operating frequency varied from 120 to 170 kHz. The coil inductance, matching networks, and X_{line} were maintained the same for both simulation and measurement setups at each frequency. The comparison between the measured and simulated results is depicted in Figure 5, where only the fundamental frequency is considered. The rectifier impedance (Z_{rect}) is compared by its real and imaginary parts (R_{rect} and X_{rect}), respectively:

$$Z_{\text{rect}} = R_{\text{rect}} + jX_{\text{rect}}. \quad (8)$$

Large discrepancies are shown between the simulated and measured rectifier impedances. There are mainly two reasons for the inaccurate results. First, some parameters are not specified in the datasheet; setting recommended values based on user's experiences or extracting values from the figures will introduce errors. Second, the testing condition in the datasheet may not be the same as the operating condition in measurement. Thus, the parameters may change in a real WPT system. In sum, the analytical equation and circuit simulation are not capable of obtaining the rectifier impedance accurately.

In this article, a measurement-based characterization method is proposed for the rectifier. It provides the rectifier impedance and efficiency under the real operating condition. The characterization setup is illustrated in Figure 6. In practice, the load of the rectifier may consist of a dc-dc voltage regulator charging a battery. The dc-dc voltage regulator, such as buck or buck-boost converter, can be modeled as an equivalent resistor [27], [28]. Therefore, a resistive load R_{load} is used to represent a subcircuit feeding the actual physical electric load of the rectifier [29]. A differential voltage probe and a current probe are applied to the input port of the rectifier. The ac input voltage and current waveforms are measured by the oscilloscope in the time domain. Then, all stored data are processed by fast Fourier transformation (FFT) to provide the impedance in the frequency domain. There are several advantages in applying the time-domain measurements. First, the phase information is accessible by using a less expensive instrument (i.e., an oscilloscope instead of a vector network analyzer). Also, with the relatively high signal-to-noise ratio signals operating in the kilohertz frequency range, the phase information could be obtained without the down mixing method. In addition, the measurement time is

reduced, since a single-shot waveform in the time domain contains the complete information in the frequency range of interest (both fundamental and higher order harmonic components).

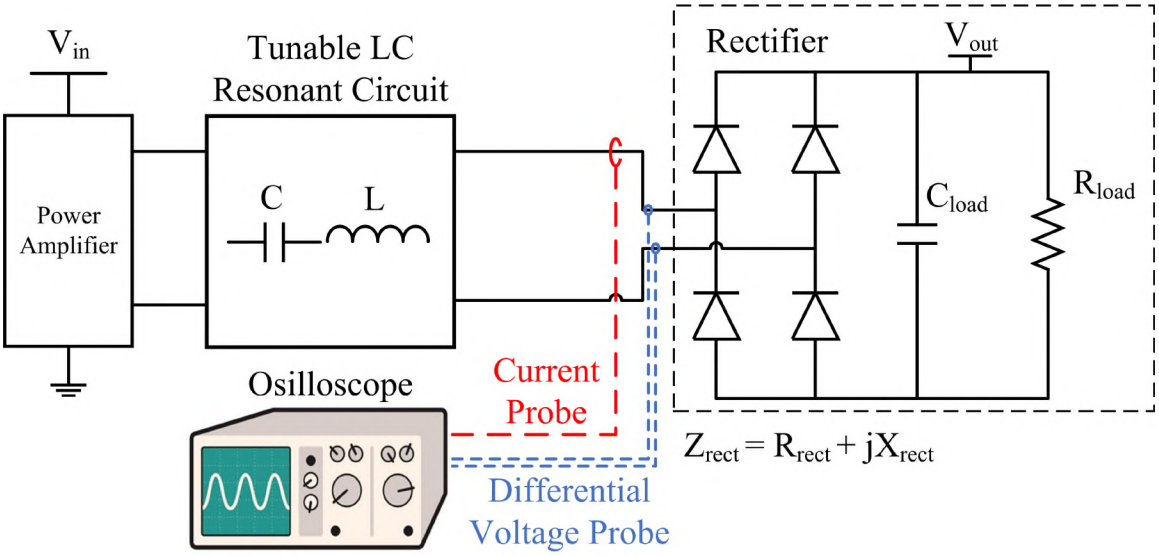


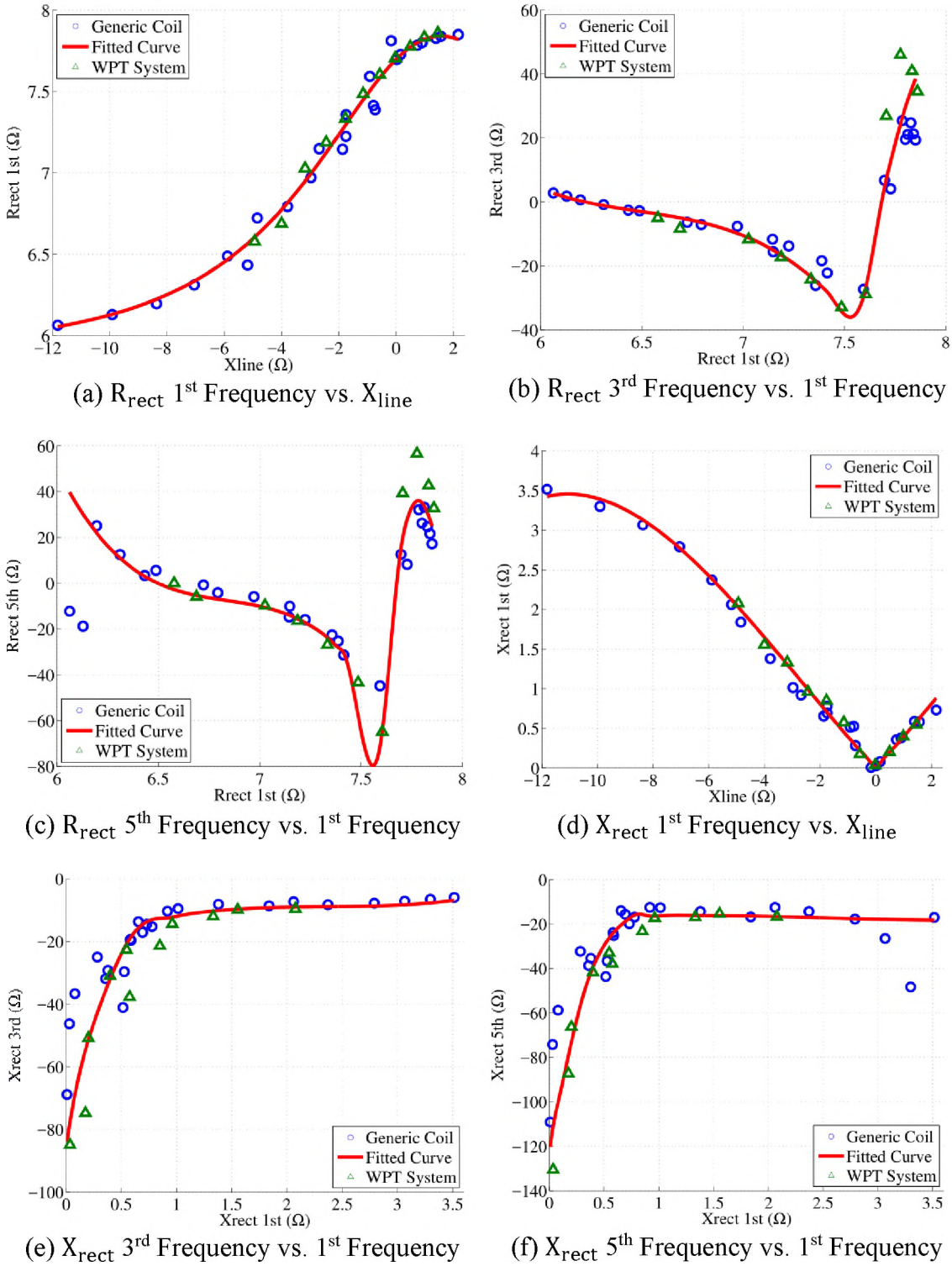
Figure 6. Measurement-based rectifier impedance characterization setup.

Table 1. Coil parameters for characterization and validation setups.

Coil Parameter	Generic Coil Module for Characterization	WPT System Coil for Validation
L_{tx}	7.90 μH	8.58 μH
L_{rx}	7.90 μH	12.52 μH
C_{tx}	400 nF	400 nF
C_{rx}	100, 200, 300, 400 nF	200 nF
k	0.58	0.63

The tunable LC resonant circuit is implemented to vary X_{line}. It is preferable to use a generic coil-to-coil module because of three main reasons. First, the line impedance X_{line} can be easily changed by the matching capacitance and the topology. Second, the scenario for characterization is close to the real WPT system, so it can achieve good coverage of the interested parameter range. Third, there is no additional hardware or cost. The parameters of the generic coil used in the rectifier characterization are described in Table 1. The line impedance X_{line} is tuned by varying the operating frequency and RX matching capacitance C_{rx}. The characterization results were validated by a real WPT system with a different set of coils.

In Figure 7, the real and imaginary parts of the rectifier impedance (R_{rect} and X_{rect}) are characterized separately. The part number of rectification diode is DIODES SBR3U40P1. $V_{out} = 8.3\ V, P_{out} = 8\ W, Z_{load} = 8.67\ \Omega$, operating frequency is 120 kHz $\sim$ 180 kHz. The circular dots are the characterization points using the generic coil module. The solid line is the fitted impedance curve based on the characterization points. The triangle dots are the measured rectifier impedance of a real WPT system. Both R_{rect} and X_{rect} at the fundamental frequency have strong correlation with X_{line} [see Figure 7 (a) and (d)]. Then, the impedance at the third- and fifth-order harmonics can be further predicted by R_{rect} and X_{rect} at the fundamental frequency [see Figure 7 (b), (c), (e), and (f)]. Thus, Z_{rect} can be accurately obtained in terms of its most critical frequency components for a WPT model.



(a) R_{rect} 1st Frequency vs. X_{line}

(b) R_{rect} 3rd Frequency vs. 1st Frequency

(c) R_{rect} 5th Frequency vs. 1st Frequency

(d) X_{rect} 1st Frequency vs. X_{line}

(e) X_{rect} 3rd Frequency vs. 1st Frequency

(f) X_{rect} 5th Frequency vs. 1st Frequency

Figure 7. Rectifier impedance characterization and validation results.

The rectifier efficiency (η_{rect}) is mainly affected by the forward voltage drop of the rectification diode, the output voltage of the rectifier, and the power level. This article focuses on the CPL WPT system, where the output power and voltage are fixed. The characterization is also conducted on a provided rectifier with the predetermined forward resistance property. So, η_{rect} is expected to be constant under different operation conditions. The measured η_{rect} in both characterization and validation setups was between 93.6% and 94.0%. For simplicity, the averaged value 93.8% was chosen as the characterized rectifier efficiency.

Currently, the characterization curves are fitted using polynomial and rational functions, which are sufficient for kilohertz WPT systems. However, certain discrepancies were observed at higher frequency harmonics [see Figure 7(c) and (f)]. It implied that more complicated fitting or data training techniques should be applied for the WPT system with higher operating frequency (megahertz or above). This part of work is beyond the scope of this article and will be discussed in future studies.

4. IMPROVED MODELING AND DESIGN METHODOLOGY

In this section, an improved WPT system model is demonstrated with the characterized rectifier impedance. This model is established based on the premise that all the blocks of a target WPT system are provided. Then, the coil parameters, the impedance and the efficiency of the rectifier, and the parasitic effects of the power amplifier can be obtained in advance (see Table 2: "Known Parameters"). The goal of this method is to optimize the matching network, input voltage, and operating frequency (see Table 2:

"Design Parameters"), in order to obtain 425 the peak system efficiency and accurate power loss of each block 426 (see Table 2: "Target Outputs"). A practical design methodology is introduced to optimize these system parameters.

Table 2. Categories of the WPT system model parameters.

Category	Parameter	Description
Known Parameters	$L_{\text{tx}}, L_{\text{rx}}, R_{\text{tx}}, R_{\text{rx}}, k$	Coil inductance and ac resistances, coupling coefficient
	$R_{\text{rect}}, X_{\text{rect}}, \eta_{\text{rect}}$	Rectifier impedance and efficiency
	$t_{\text{f}}, t_{\text{dead}}, V_{\text{d}}, R_{\text{on}}$	Power amplifier fall/dead times, MOSFET body-diode forward voltage and on-resistance
Design Parameters	V_{in}	TX dc input voltage
	$\omega = 2\pi f$	Operating frequency
	$C_{\text{tx}}, C_{\text{rx}}$	Capacitance of the TX and RX matching networks
Target Outputs	$P_{\text{in}}, P_{\text{pa}}, P_{\text{rx}}, P_{\text{rect}}$	Powers at the block interfaces
	η_{sys}	System efficiency

4.1. IMPROVED MODELING OF THE WPT SYSTEM

A typical WPT system is formulated in Figure 8. As discussed in Section 2, the power amplifier at the TX side can be simplified to a trapezoidal-wave voltage source. Since the rising/falling time of the input voltage waveform (typically tens of ns) is relatively small compared with the switching period (several μs for a kHz WPT system), the input source can be modeled as a square-wave with additional losses due to the transition edges. The original dc input voltage V_{in} then becomes the amplitude of this square-wave. R_s is related to the on-resistance R_{on} of the MOSFET in power amplifier. It

leads to the voltage drop along the power flow path and affects the back-end blocks. For a half-bridge power amplifier, $R_s = R_{on}$. For a full-bridge power amplifier, $R_s = 2R_{on}$. The rectifier impedance at the RX side is Z_{rect}, which is included in this model as a realistic load condition. The characterization method for Z rect and rectifier efficiency η_{rect} are introduced in Section 3.

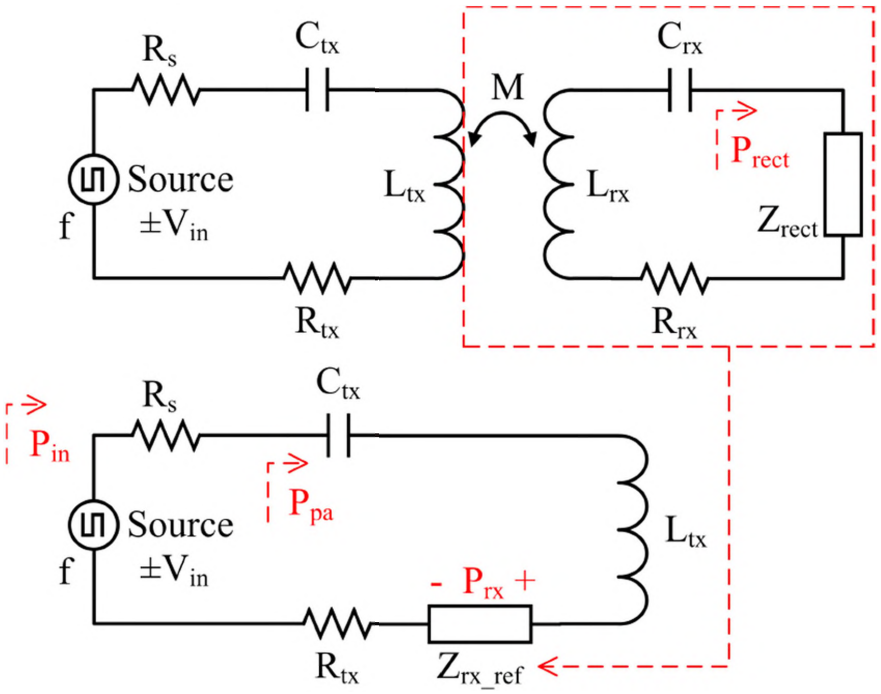


Figure 8. Formulation for the improved modeling of the WPT system.

Based on the standard mutual inductance coupling transfer model, the RX side circuits can be represented as a reflected impedance Z_{rx_ref} at the TX side

$$Z_{\text{rx\_ref}} = \frac{(\omega M)^2}{R_{\text{rx}} + j\omega L_{\text{rx}} + \dfrac{1}{j\omega C_{\text{rx}}} + Z_{\text{rect}}}. \tag{9}$$

Combining (8) and (9), Z_{rx_ref} can be represented as:

$$\begin{aligned} Z_{\text{rx\_ref}} &= \frac{(\omega M)^2}{(R_{\text{rx}} + R_{\text{rect}}) + j\left(\omega L_{\text{rx}} - \frac{1}{\omega C_{\text{rx}}} + X_{\text{rect}}\right)} \\ &= \left[\frac{(\omega M)^2 (R_{\text{rx}} + R_{\text{rect}})}{(R_{\text{rx}} + R_{\text{rect}})^2 + \left(\omega L_{\text{rx}} - \frac{1}{\omega C_{\text{rx}}} + X_{\text{rect}}\right)^2}\right] \\ &+ j\left[\frac{-(\omega M)^2 \left(\omega L_{\text{rx}} - \frac{1}{\omega C_{\text{rx}}} + X_{\text{rect}}\right)}{(R_{\text{rx}} + R_{\text{rect}})^2 + \left(\omega L_{\text{rx}} - \frac{1}{\omega C_{\text{rx}}} + X_{\text{rect}}\right)^2}\right] \\ &\triangleq R_{\text{rx\_ref}} + jX_{\text{rx\_ref}}, \end{aligned} \tag{10}$$

where R_{rx_ref} and X_{rx_ref} are the real and imaginary parts of the reflected impedance respectively.

Note that (10) is applicable to one single frequency. In order to take multiple harmonic frequencies into consideration, a superscript (n) is introduced into each notation to denote the index of the harmonic frequency. For example, the variables $X^{(1)}$, $X^{(3)}$, and $X^{(5)}$ are the fundamental, third order, and fifth order frequency harmonics, respectively. Then, R_{rx_ref} and X_{rx_ref} can be represented as

$$\begin{cases} R_{\text{rx\_ref}}^{(n)} = \dfrac{(n\omega_0 M)^2 \left(R_{\text{rx}}^{(n)} + R_{\text{rect}}^{(n)}\right)}{\left(R_{\text{rx}}^{(n)} + R_{\text{rect}}^{(n)}\right)^2 + \left(n\omega_0 L_{\text{rx}} - \dfrac{1}{n\omega_0 C_{\text{rx}}} + X_{\text{rect}}^{(n)}\right)^2} \\ X_{\text{rx\_ref}}^{(n)} = \dfrac{-(n\omega_0 M)^2 \left(n\omega_0 L_{\text{rx}} - \dfrac{1}{n\omega_0 C_{\text{rx}}} + X_{\text{rect}}^{(n)}\right)}{\left(R_{\text{rx}}^{(n)} + R_{\text{rect}}^{(n)}\right)^2 + \left(n\omega_0 L_{\text{rx}} - \dfrac{1}{n\omega_0 C_{\text{rx}}} + X_{\text{rect}}^{(n)}\right)^2}, \end{cases} \tag{11}$$

where ω_0 is the fundamental component of the operating frequency.

The total load impedance of the power amplifier at the TX side is denoted as Z_{pa}. Similar as the reflected impedance, Z_{pa} can be represented with the real and imaginary terms

$$Z_{\text{pa}}^{(n)} \triangleq R_{\text{pa}}^{(n)} + jX_{\text{pa}}^{(n)},$$

where

$$\begin{cases} R_{\text{pa}}^{(n)} = R_{\text{s}} + R_{\text{tx}}^{(n)} + R_{\text{rx\_ref}}^{(n)} \\ X_{\text{pa}}^{(n)} = n\omega_0 L_{\text{tx}} - \dfrac{1}{n\omega_0 C_{\text{tx}}} + X_{\text{rx\_ref}}^{(n)}. \end{cases} \tag{12}$$

As the input source is modeled as a square wave. The power losses related to the transition edges are calculated separately. Using the Fourier transform, the input source of a square wave can be divided into multiple sinusoidal harmonics, with the amplitude of each harmonic being

$$V_{\text{s}}^{(n)} = \frac{C}{\pi}\frac{V_{\text{in}}}{n}, \tag{13}$$

where C is a constant determined by the power amplifier's topology. For a half-bridge power amplifier, C = 2 as the switching voltage changes from 0 to V_{in}. For a full-bridge power amplifier, C = 4 as the switching voltage changes from $-V_{in}$ to V_{in}. With (13), the input power distributed on each harmonic component can be calculated as

$$\begin{aligned} P_{\text{in,cond}}^{(n)} &= \frac{1}{2}\left(V_{\text{s}}^{(n)}\right)^2 \frac{R_{\text{pa}}^{(n)}}{\left(R_{\text{pa}}^{(n)}\right)^2 + \left(X_{\text{pa}}^{(n)}\right)^2} \\ &= \frac{(CV_{\text{in}})^2}{2\pi^2 n^2} \frac{R_{\text{pa}}^{(n)}}{\left(R_{\text{pa}}^{(n)}\right)^2 + \left(X_{\text{pa}}^{(n)}\right)^2}, \end{aligned} \tag{14}$$

The time-domain input power is the sum of all the frequency harmonics

$$P_{\text{in,cond}} = \sum_{n=1}^{\infty} P_{\text{in.cond}}^{(n)} = \frac{(CV_{\text{in}})^2}{2\pi^2} \sum_{n=1}^{\infty} \left[\frac{1}{n^2} \cdot \frac{R_{\text{pa}}^{(n)}}{\left(R_{\text{pa}}^{(n)}\right)^2 + \left(X_{\text{pa}}^{(n)}\right)^2} \right], \tag{15}$$

where $R_{\text{pa}}^{(n)}$ and $X_{\text{pa}}^{(n)}$ are shown in (12). The full expansion of $P_{\text{in,cond}}$ is straightforward and will be omitted here.

Note that $P_{\text{in,cond}}$ only considers the conduction loss of the power amplifier. To model the total input power of the WPT system, the switching loss $P_{\text{loss,sw}}$ and the dead time loss $P_{\text{loss,dead}}$ of the power amplifier should also be included [30]

$$P_{\text{in}} = P_{\text{in,cond}} + P_{\text{loss,sw}} + P_{\text{loss,dead}}. \tag{16}$$

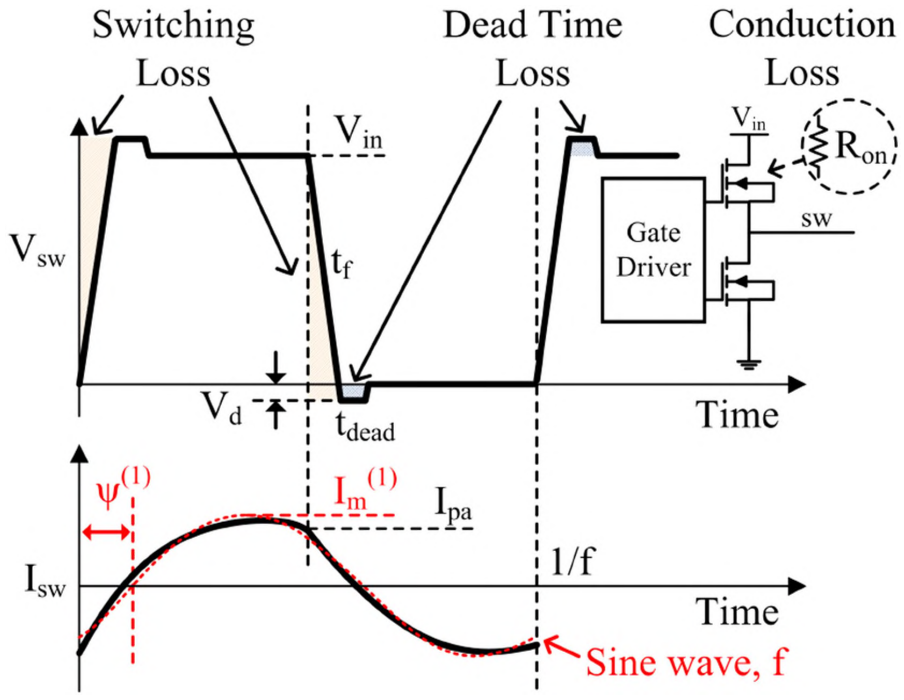


Figure 9. Time-domain voltage and current waveforms at the switching node.

The switching loss and the dead time loss occur at the MOSFET on-off transitions. For a zero-voltage-switched power amplifier, $P_{loss,sw}$ is mainly contributed by the turn-OFF switching losses of the high-side and low-side MOSFETs. And $P_{loss,dead}$ is caused by the current flowing through the body diodes during the excessive dead time after each transition. As shown in Figure 9, $P_{loss,sw}$ and $P_{loss,dead}$ for a half-bridge power amplifier (one pair of high-side and low-side MOSFETs) can be approximated using simple time-domain figure calculations. For a full-bridge power amplifier, $P_{loss,sw}$ and $P_{loss,dead}$ need to be doubled compared with the half-bridge power amplifier

$$P_{\text{loss,sw}} = \begin{cases} V_{\text{in}} I_{\text{pa}} t_{\text{f}} f, & \text{half-bridge power amplifier} \\ 2V_{\text{in}} I_{\text{pa}} t_{\text{f}} f, & \text{full-bridge power amplifier} \end{cases} \tag{17}$$

$$P_{\text{loss,dead}} = \begin{cases} 2V_{\text{d}} I_{\text{pa}} t_{\text{dead}} f, & \text{half-bridge power amplifier} \\ 4V_{\text{d}} I_{\text{pa}} t_{\text{dead}} f, & \text{full-bridge power amplifier} \end{cases} \tag{18}$$

where t_f is the falling time of the on-off transition. t_{dead} is the dead time after the rising/falling transitions. V_d is the forward voltage of the MOSFET body-diode. V_{in} and f are the design parameters: input voltage and operating frequency. I_{pa} is the switching node current I_{sw} at the on-off transition edge

$$I_{\text{pa}} = I_{\text{sw}}(t = t_{\text{on}\rightarrow\text{off}}). \tag{19}$$

I_{sw} is the composition of a sine wave with the operating frequency f and its higher order harmonics. The amplitude of each frequency component is denoted as $I_m^{(n)}$, which can be calculated as in [14]

$$I_{\text{m}}^{(n)} = V_{\text{s}}^{(n)} \frac{\cos \Psi^{(n)}}{R_{\text{pa}}^{(n)}} = \frac{CV_{\text{in}}}{\pi} \frac{\cos \Psi^{(n)}}{nR_{\text{pa}}^{(n)}}, \tag{20}$$

$$I_{\text{sw}}(t) = \sum_{n=1}^{\infty} I_{\text{m}}^{(n)} \sin(2n\pi ft - \Psi^{(n)}), \tag{21}$$

where $\Psi^{(n)} = \tan^{-1}\left(\mathrm{X}_{\mathrm{pa}}^{(\mathrm{n})}/\mathrm{R}_{\mathrm{pa}}^{(\mathrm{n})}\right)$ is the phase difference between voltage and current at the switching node.

Suppose that the MOSFET on-off transition occurs at time $\mathrm{t}_{\mathrm{on}\rightarrow\mathrm{off}} = 1/(2f)$. From (19)-(21), I_{pa} is calculated using the following formula:

$$\begin{aligned} I_{\text{pa}} &= \sum_{n=1}^{\infty} I_{\text{m}}^{(n)} \sin(n\pi - \Psi^{(n)}) \\ &= \frac{CV_{\text{in}}}{\pi} \sum_{n=1}^{\infty} \frac{V_{\text{s}}^{(n)} \cos\Psi^{(n)}}{nR_{\text{pa}}^{(n)}} \sin(n\pi - \Psi^{(n)}). \end{aligned} \tag{22}$$

Integrate I_{pa} into (17) and (18) to determine the $\mathrm{P}_{\mathrm{loss,sw}}$ and $\mathrm{P}_{\mathrm{loss,dead}}$, respectively. Finally, based on (16), the total input power of the WPT system P_{in} can be obtained.

The power flowing through the other blocks, such as the power amplifier, WPT coils, and rectifier, can be derived in a similar manner as

$$\begin{aligned} P_{\text{pa}} &= \sum_{n=1}^{\infty} P_{\text{pa}}^{(n)} = \sum_{n=1}^{\infty} \left(P_{\text{in,cond}}^{(n)} \frac{R_{\text{tx}}^{(n)} + R_{\text{rx\_ref}}^{(n)}}{R_{\text{pa}}^{(n)}} \right) \\ &= \frac{(CV_{\text{in}})^2}{2\pi^2} \sum_{n=1}^{\infty} \left[\frac{1}{n^2} \cdot \frac{R_{\text{tx}}^{(n)} + R_{\text{rx\_ref}}^{(n)}}{\left(R_{\text{pa}}^{(n)}\right)^2 + \left(X_{\text{pa}}^{(n)}\right)^2} \right], \end{aligned} \tag{23}$$

$$\begin{aligned} P_{\text{rx}} &= \sum_{n=1}^{\infty} P_{\text{rx}}^{(n)} = \sum_{n=1}^{\infty} \left(P_{\text{pa}}^{(n)} \frac{R_{\text{rx\_ref}}^{(n)}}{R_{\text{tx}}^{(n)} + R_{\text{rx\_ref}}^{(n)}} \right) \\ &= \frac{(CV_{\text{in}})^2}{2\pi^2} \sum_{n=1}^{\infty} \left[\frac{1}{n^2} \cdot \frac{R_{\text{rx\_ref}}^{(n)}}{\left(R_{\text{pa}}^{(n)}\right)^2 + \left(X_{\text{pa}}^{(n)}\right)^2} \right], \end{aligned} \tag{24}$$

$$P_{\text{rect}} = \sum_{n=1}^{\infty} P_{\text{rect}}^{(n)} = \sum_{n=1}^{\infty} \left(P_{\text{rx}}^{(n)} \frac{R_{\text{rect}}^{(n)}}{R_{\text{rx}}^{(n)} + R_{\text{rect}}^{(n)}} \right)$$
$$= \frac{(CV_{\text{in}})^2}{2\pi^2} \sum_{n=1}^{\infty} \left[\frac{1}{n^2} \frac{R_{\text{rx\_ref}}^{(n)}}{\left(R_{\text{pa}}^{(n)}\right)^2 + \left(X_{\text{pa}}^{(n)}\right)^2} \frac{R_{\text{rect}}^{(n)}}{R_{\text{rx}}^{(n)} + R_{\text{rect}}^{(n)}} \right] \tag{25}$$

The output power is a result of multiplying the rectifier input power by the characterized rectifier efficiency

$$P_{\text{out}} = \eta_{\text{rect}} P_{\text{rect}}. \tag{26}$$

The proposed WPT system model can accurately derive the power at each block by using the known and design parameters in Table 2. So, the power loss and system efficiency can be calculated by the two corresponding power values. For instance, the power loss on the TX coil and TX matching network is $(P_{pa} - P_{rx})$, the power loss on the RX coil and RX matching network is $(P_{rx} - P_{rect})$, and the system and coil efficiencies can be calculated based on (2) and (3) respectively. Therefore, this model is capable of conducting system-level optimization by tuning the design parameters analytically, instead of building a complete prototype and conducting massive measurements.

4.2. PRACTICAL DESIGN METHODOLOGY

One of the challenges in designing WPT systems is the lack of practical design methodologies. There are multiple parameters, such as the input voltage, the TX/RX coil matching capacitance, and the operating frequency, involved in determining the system efficiency. These parameters are coupled with each other, so it is unfeasible to tune them one by one. Conventionally, the trial-and-error method is used to conduct measurements

under all the combinations of parameters within the ranges of interests, which is time-consuming and costly. With the help of the improved WPT model, a novel design methodology is introduced to overcome these challenges.

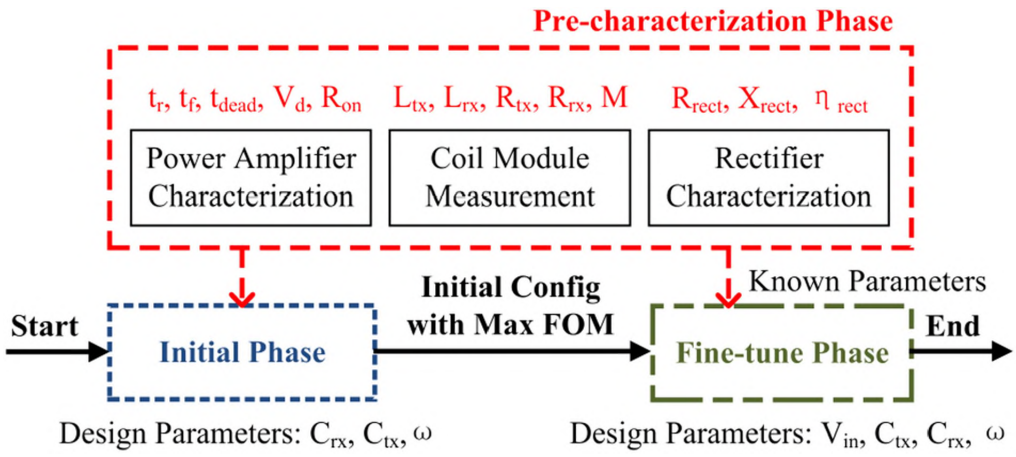


Figure 10. Flowchart of the design methodology.

The entire design process is divided into three phases: the *pre-characterization phase*, the *initial phase*, and the *fine-tune phase*. This design flow is shown in Figure 10.

1) The *pre-characterization phase* aims to obtain the "known parameters" (see Table 2) of the provided blocks, including the power amplifier, the coil module, and the rectifier. These parameters are accessible from the device's datasheet, oscilloscope, or impedance analyzer measurements, and the characterization method discussed in Section 3. The pre-characterized data can be collected into the lookup tables.

2) After the characterization on provided blocks, it is critical to set proper initial values for the design parameters. In the *initial phase*, the WPT model can be simplified by neglecting the switching and dead time losses of the power amplifier, and the higher order frequency harmonics. Then, the simplified system efficiency becomes

$$\eta_{\text{sys,initial}} = \eta_{\text{rect}} \frac{P_{\text{rect}}^{(1)}}{P_{\text{in,cond}}^{(1)}} = \eta_{\text{rect}} \frac{R_{\text{rect}}^{(1)}}{R_{\text{rx}}^{(1)} + R_{\text{rect}}^{(1)}} \frac{R_{\text{rx\_ref}}^{(1)}}{R_{\text{s}} + R_{\text{tx}}^{(1)} + R_{\text{rx\_ref}}^{(1)}}. \tag{27}$$

Note that η_{rect}, R_s, $R_{rx}^{(1)}$, and $R_{tx}^{(1)}$ are constants unrelated to the design parameters. Therefore, a figure of merit (FOM) is defined to find the initial values for the design parameters as

$$\text{FOM} = \frac{R_{\text{rect}}^{(1)}}{A + R_{\text{rect}}^{(1)}} \cdot \frac{R_{\text{rx\_ref}}^{(1)}}{B + R_{\text{rx\_ref}}^{(1)}}, \tag{28}$$

where $A = R_{rx}^{(1)}$ and $B = R_s + R_{rx}^{(1)}$ are both pre-determined constants. In this simplified condition, the goal is to maximize the FOM at the fundamental frequency. Based on (5) and (11), the FOM is determined by C_{rx}, C_{tx} , and ω. Other design parameters, such as V_{in}, are mainly set to provide sufficient power capability for the WPT system.

3) Finally, the full WPT model is included in the *fine-tune phase*. All the design parameters are tuned in fine steps based on the initial values. So, the optimizations can quickly converge to the actual optimal efficiency point.

5. EXPERIMENT AND VALIDATION

An experimental prototype was implemented to validate the proposed model. It was designed based on a real WPT system for cell phone products. In addition, the design methodology to optimize the system parameters is also validated using this prototype.

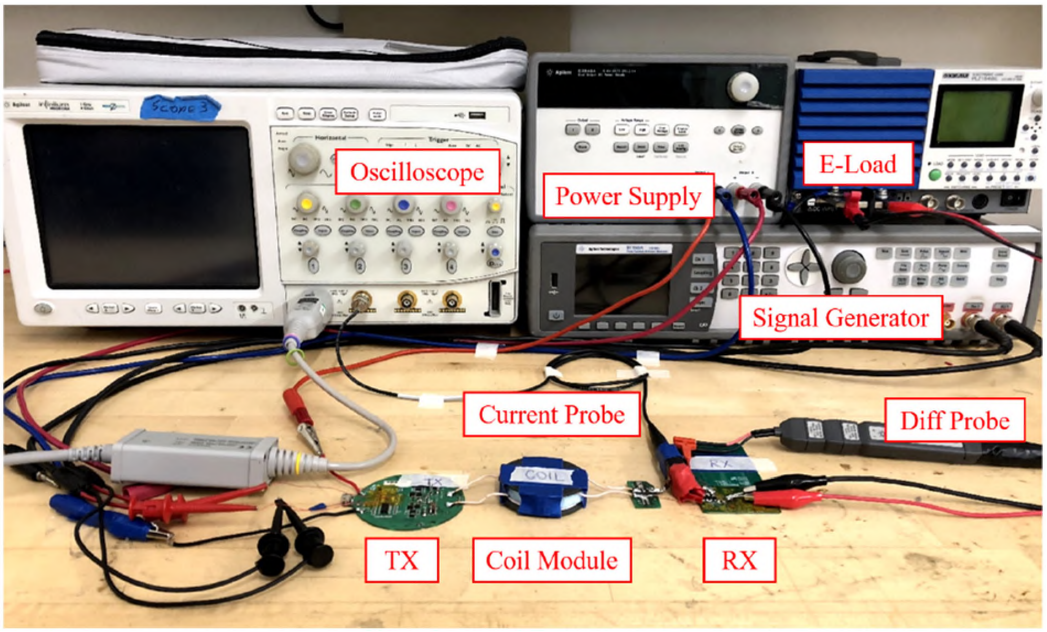


Figure 11. Photograph of the experimental prototype.

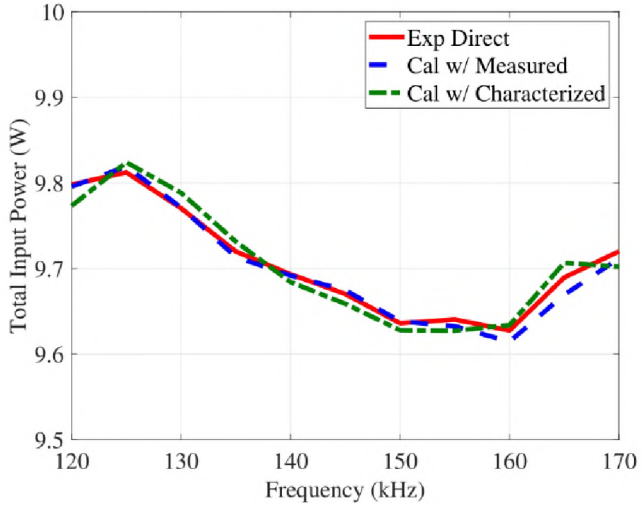
The experimental setup is depicted in Figure 11. The coil module consists of one TX coil and one RX coil. Two coils are aligned with each other by the center point and have 3-mm spacing in the vertical distance. The TX coil is built based on the standard A11 type from the Qi specification [5]. The RX coil is routed by 15-turn solid copper wires, and the physical dimensions are 38 mm × 32 mm. Both the TX and RX coils are assembled with magnetic ferrites. The matching capacitance is 400 nF for the TX coil and 200 nF for the RX coil. The detailed electrical specifications of this coil module are listed in Table 1 (WPT system coil for validation). On the TX printed circuit board (PCB) board, a full-bridge power amplifier is implemented by four N-channel MOSFET s (AON7544) and two gate drivers (NCP81151). The dc voltage for the TX board is provided by a dual-output power supply (Agilent E3648A). Since the proposed modeling method focuses on the power flow path of the WPT system, the experiment is also designed to remove the impact

of other nonpower-path circuits. Therefore, one output of the power supply is dedicated to the power flow path. The non-power-path devices, such as the gate driver, are powered separately by the other output. The gate drivers are controlled by two inverted channels from a signal generator (Agilent 81150A), where two square waves with the same frequency and 180^{o} out phase are generated. On the RX PCB board, a full-wave rectifier is implemented by four Schottky diodes (SBR3U40P1) and two 10 μF smoothing capacitors. The dc output is connected to an electrical load (KIKUSUI PLZ164WL), which operates in the 8.67 Ω constant-resistance mode. The RX output voltage is fixed to 8.33 V, and the rated output power is 8 W. The system efficiency of this experimental setup is calculated based on the dc powers measured at the input and output sides (P_{in}/P_{out}). The intermediate ac powers, such as the power amplifier output power (P_{pa}) and the rectifier input power (P_{rect}), are measured in the time domain by an oscilloscope (Agilent MSO8104A) with differential and current clamp probes.

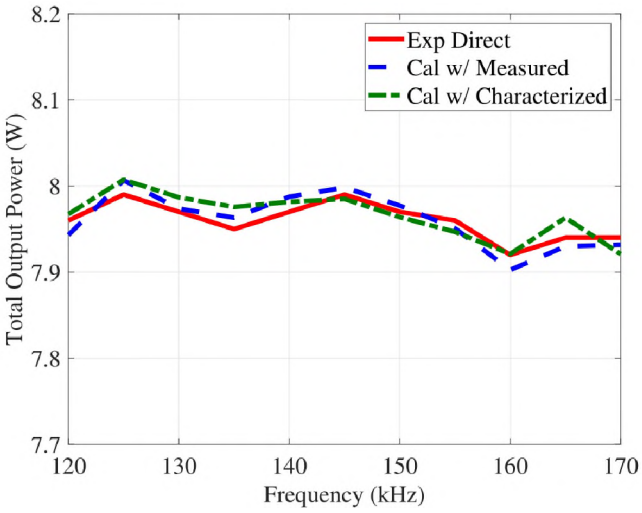
5.1. VALIDATION ON CHARACTERIZATION AND MODELING

In order to validate both the rectifier characterization method and the improved WPT model, three types of results have been compared: 1) the direct measured power and system efficiency from this experimental setup: "Exp Direct"; 2) the calculated result with measured rectifier impedance: "Cal w/Measured"; it validated this improved WPT model; and 3) the calculated result with characterized rectifier impedance: "Cal w/ Characterized"; by using the fitted rectifier impedance curve (the solid line in Figure 7), it validated the accuracy of this rectifier characterization method.

(a) Total input power.



(b) Total output power.



(c) System Efficiency.

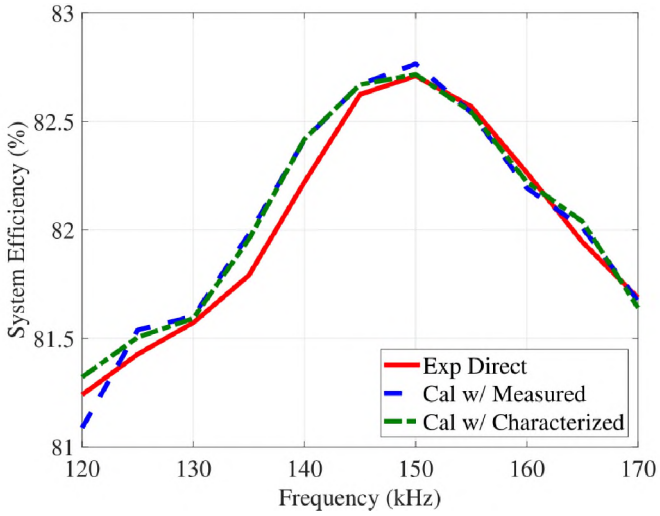


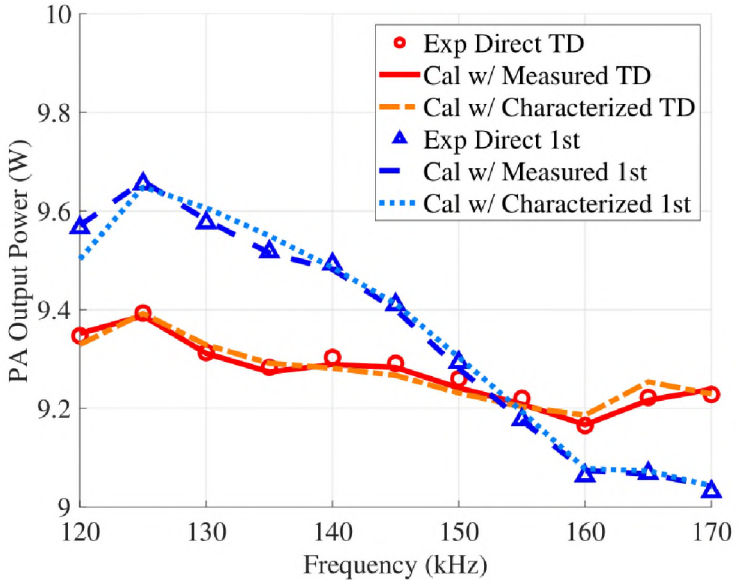
Figure 12. Comparison of dc power and efficiency.

The calculations, based on (16), (26), and (2), and the experiment results of input power P_{in}, output power P_{out}, and system efficiency η_{sys} versus the operating frequency are plotted in Figure 12. The rated output power is 8 W with less than 0.1 W variation in actual measurement, and the operating frequency varies from 120 to 170 kHz. The three types of results have good correlation with each other. The highest η_{sys} is achieved at 150 kHz, with the input voltage V_{in} = 8.52 V. The improved WPT model does not require any impractical assumptions used in the conventional modeling methods and can find the peak efficiency point across a wide frequency range.

Since this model is built on the basis of frequency harmonic analysis, it is important to validate the accuracy of the calculated power distributed on each frequency component. The comparison of intermediate ac powers, including P_{pa} and P_{rect}, is shown in Figure 13. For experiment, the time-domain result ("Exp TD") is obtained by multiplying the measured voltage and current directly, and the fundamental frequency result ("Exp 1st") is extracted from the FFT processed time-domain waveforms. For calculation, P_{pa} and P_{rect} distributed on each frequency component are calculated based on (23) and (25). The time-domain result ("Cal TD") includes the three most significant components: the fundamental, third-order, and fifth-order harmonics. The fundamental frequency result ("Cal 1st") only considers the fundamental component. The good agreement between experiment and calculation validates the improved model in both time and frequency domains. Additionally, it shows that this model can not only estimate the end-to-end system efficiency, but also provide the accurate power loss of each block in a WPT system. As a result, it provides more flexibility to set different loss thresholds for the critical blocks and

improve the thermal design. The configuration with the maximum FOM achieves the best system efficiency.

(a) Power amplifier output power P_{pa}.



(b) Rectifier input power P_{rect}.

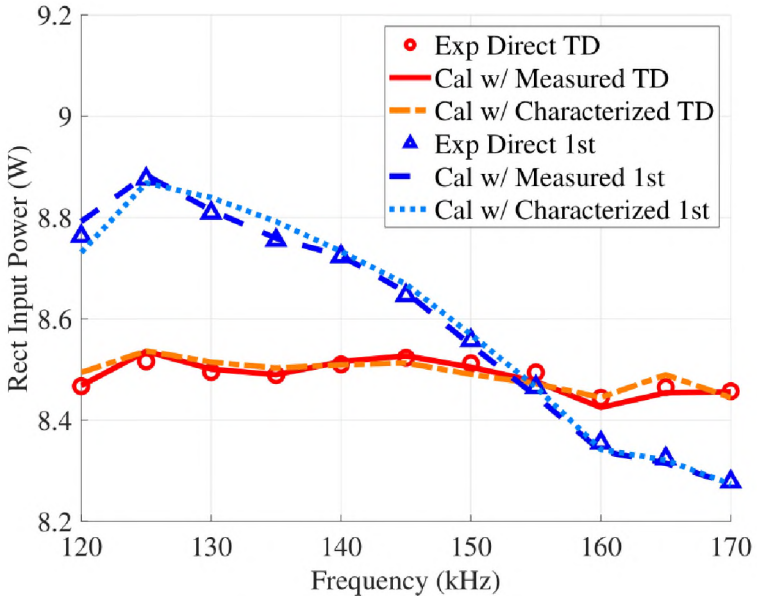


Figure 13. Comparison of intermediate ac powers.

5.2. VALIDATION ON DESIGN METHODOLOGY

The design methodology is validated using the same experimental prototype, so the *pre-characterization phase* has already been conducted. In the *initial phase*, three different configurations of the matching capacitance are investigated.

1) Config 1: C_{tx} = 400 nF and C_{rx} = 200 nF.

2) Config 2: C_{tx} = 400 nF and C_{rx} = 300 nF.

3) Config 3: C_{tx} = 300 nF and C_{rx} = 200 nF.

The FOM for each configuration is calculated based on (28) by sweeping the operating frequency from 120 to 170 kHz, as shown in Figure 14. The global maximum FOM is achieved with "Config 1" at around 150 kHz. To validate the effectiveness of the FOM, these configurations are intentionally kept the same in the *fine-tune phase*. Then, the other design parameters are tuned based on the initial values set by the local maximum FOM of each configuration. Figure 15 compares the system efficiencies from both calculations and experiments. The trend of system efficiency is very close to the predictions based on the FOM, which implies that the FOM can effectively determine the proper initial values for the design parameters. Note that the system efficiency is also affected by other blocks. Therefore, it is necessary to tune the design parameters in fine steps for the optimal system efficiency. The actual calculations in the *fine-tune phase* is from 135 to 165 kHz for all configurations, which is illustrated by the dashed line box in Figure 15. The final optimal configurations are: C_{tx} = 400 nF, C_{rx} = 200 nF, V_{in} = 8.52 V, and operating frequency at 150 kHz.

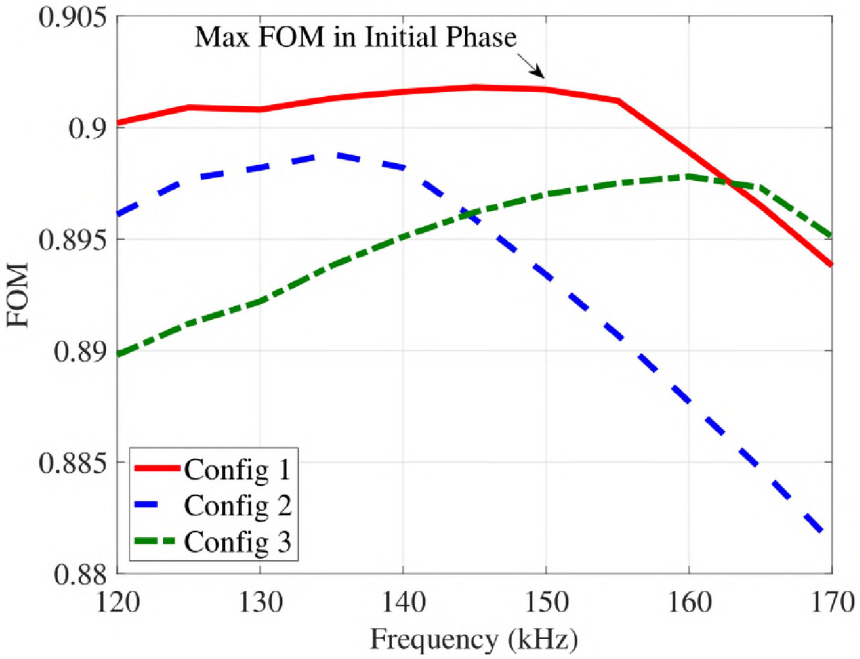


Figure 14. FOM calculation in the initial phase.

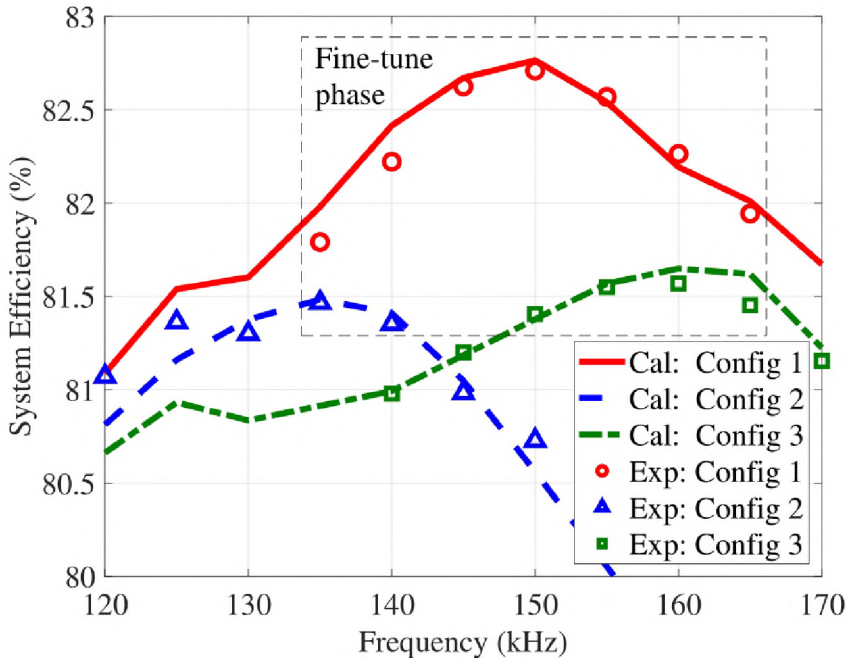


Figure 15. System efficiency comparison in the fine-tune phase.

6. CONCLUSION

In this article, the impractical assumptions of the existing WPT system modeling methods are investigated by circuit simulations. To avoid the pure resistance load assumption, an accurate rectifier characterization method is proposed to provide a realistic load condition. On the basis of the characterized rectifier impedance, a novel system-level WPT model is presented instead of only focusing on the coil-to-coil part. The improved model considers both the fundamental frequency and higher order harmonics, which can effectively eliminate the inaccuracy caused by FHA at off-resonance conditions. Good performance of the model is validated by experimental measurements in both time and frequency domains. The result shows that it can accurately estimate the system efficiency and power loss at each interior block. With the assistance of this model, a practical methodology is introduced to efficiently optimize the design parameters of a WPT system.

APPENDIX

Based on the small-signal analysis, the derivations of (6) is described in the following procedures. All variables are defined the same as Figure 4.

1) *Define the source voltage v_s with a perturbation*: Assume that the source voltage v_s consists of a sinusoidal wave v_1 and a small-signal perturbation Δv_p : $v_s = v_1 + \Delta v_p$, where $|v_1| = V_1$, $|\Delta v_p| = V_p$ with $V_p \ll V_1$.

2) *Calculate the output voltage* v_{dc}: Using the nonlinear switching functions S and ΔS defined in Section 3, the mapping relationship between the input and output sides of the rectifier can be expressed as

$$\begin{cases} v_{\mathrm{dc}} = (S + \Delta S) \cdot v_{\mathrm{ac}} \\ i_{\mathrm{ac}} = (S + \Delta S) \cdot i_{\mathrm{dc}} \end{cases} \tag{1}$$

The input voltage v_{ac} and output voltage v_{dc} are calculated by combining the source voltage v_s, the switching functions $(S + \Delta S)$, and the line impedance Z_{line} as

$$\begin{aligned} v_{\mathrm{ac}} &= v_{\mathrm{s}} - i_{\mathrm{ac}} \cdot Z_{\mathrm{line}} \\ &= (v_1 + \Delta v_{\mathrm{p}}) - (S + \Delta S) \cdot i_{\mathrm{dc}} \cdot Z_{\mathrm{line}} \end{aligned} \tag{2}$$

$$\begin{aligned} v_{\mathrm{dc}} &= (S + \Delta S) \cdot v_{\mathrm{ac}} \\ &= (S + \Delta S) \cdot [(v_1 + \Delta v_{\mathrm{p}}) - (S + \Delta S) \cdot i_{\mathrm{dc}} \cdot Z_{\mathrm{line}}] \\ &\approx S \cdot v_1 + \Delta S \cdot v_1 + S \cdot \Delta v_{\mathrm{p}} - \\ &\quad S^2 \cdot i_{\mathrm{dc}} \cdot Z_{\mathrm{line}} - 2S \cdot \Delta S \cdot i_{\mathrm{dc}} \cdot Z_{\mathrm{line}} \end{aligned} \tag{3}$$

Note that two terms $(\Delta S \cdot \Delta v_p)$ and $(\Delta S^2 \cdot i_{dc} \cdot Z_{line})$ are neglected because they involve the product of two small variation values ΔS and Δv_p.

The first term $(S \cdot v_1)$ is caused by the main wave. The second and third terms, $(\Delta S \cdot v_1)$ and $(S \cdot \Delta v_p)$, are related to the perturbation. The other terms are affected by the mutual effects of both signals, because the output current i_{dc} contains both main wave and perturbation components. In order to decouple the mutual effects, i_{dc} can be approximated to the dc component of the load current I_d. Then, the output voltage v_{dc} can be expressed by the main wave component $v_{dc,1}$ and the perturbation component Δv_{dc}

$$v_{\mathrm{dc}} = v_{\mathrm{dc},1} + \Delta v_{\mathrm{dc}}, \tag{4}$$

where

$$\begin{cases} v_{\mathrm{dc},1} \approx S \cdot v_1 - S^2 \cdot I_\mathrm{d} \cdot Z_\mathrm{line} \\ \Delta v_\mathrm{dc} \approx \Delta S \cdot v_1 + S \cdot \Delta v_\mathrm{p} - 2S \cdot \Delta S \cdot I_\mathrm{d} \cdot Z_\mathrm{line} \end{cases} \tag{5}$$

3) Calculate the output current i_{dc}: Similar with v_{dc}, the output current i_{dc} consists of the main wave component $i_{dc,1}$ and the perturbation component Δi_{dc}

$$i_\mathrm{dc} = i_{\mathrm{dc},1} + \Delta i_\mathrm{dc}. \tag{6}$$

The dc component of i_{dc} is denoted as I_d, which can be simply determined by the rated output power P_{out} and the load impedance R_{load}: $I_d = P_{out}/R_{load}$.

The ac components are calculated based on the Thevenin equivalent circuit representing the output side of the rectifier, as shown in Figure A.1. The voltage source of this equivalent circuit can be either $v_{dc,1}$ or Δv_{dc}. Correspondingly, the current is $i_{dc,1}$ or Δi_{dc}. The source impedance Z_{dc} is mapped from the ac-side line impedance Z_{line}. For the single-phase rectifier without overlap period, Z_{dc} approximately equals $2Z_{line}$ [24], [25]. Then, the ac components of the output current can be calculated as

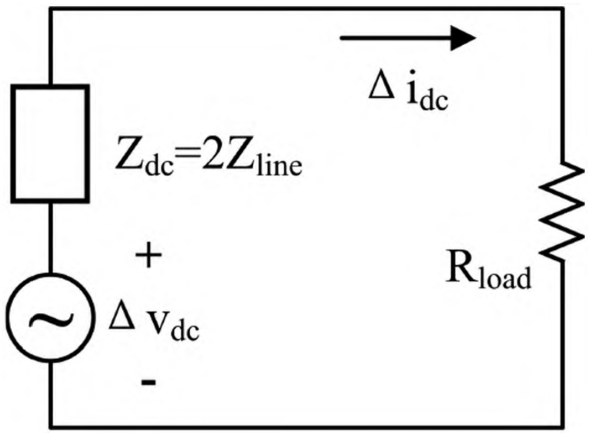


Figure A.1. Thevenin equivalent circuit for the output side of the rectifier.

$$i_{\mathrm{dc},1} = \frac{v_{\mathrm{dc},1}}{Z_{\mathrm{dc}} + R_{\mathrm{load}}} = \frac{S \cdot v_1 - S^2 \cdot I_{\mathrm{d}} \cdot Z_{\mathrm{line}}}{2Z_{\mathrm{line}} + R_{\mathrm{load}}}, \tag{7}$$

$$\Delta i_{\mathrm{dc}} = \frac{\Delta v_{\mathrm{dc}}}{Z_{\mathrm{dc}} + R_{\mathrm{load}}} = \frac{\Delta S v_1 + S\Delta v_{\mathrm{p}} - 2S\Delta S I_{\mathrm{d}} Z_{\mathrm{line}}}{2Z_{\mathrm{line}} + R_{\mathrm{load}}}. \tag{8}$$

4) *Map the output current to the ac-side input current* i_{ac}: Based on the mapping relationship, the ac-side input current i_{ac} can be calculated from the output current as

$$i_{\mathrm{ac}} = (S + \Delta S) \cdot i_{\mathrm{dc}} = (S + \Delta S) \cdot (i_{\mathrm{dc},1} + \Delta i_{\mathrm{dc}}) \tag{9}$$

To calculate the input impedance of the rectifier, only the perturbation component Δi ac is needed. So, Δi_{ac} is extracted from (37) and expressed as

$$\begin{aligned} \Delta i_{\mathrm{ac}} &= \Delta S \cdot i_{\mathrm{dc},1} + S \cdot \Delta i_{\mathrm{dc}} \\ &= \frac{2S\Delta S v_1 + S^2 \Delta v_{\mathrm{p}} - 3S^2 \Delta S I_{\mathrm{d}} Z_{\mathrm{line}}}{2Z_{\mathrm{line}} + R_{\mathrm{load}}} \end{aligned} \tag{10}$$

The perturbation component of the input voltage Δv_{ac} is:

$$\Delta v_{\mathrm{ac}} = \Delta v_p - \Delta S \cdot I_{\mathrm{d}} \cdot Z_{\mathrm{line}}. \tag{11}$$

Finally, the input impedance of the rectifier can be calculated by the ratio of perturbation voltage and current at the input side $\Delta v_{ac}/\Delta i_{ac}$, as shown in (6).

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SECTION

2. CONCLUSIONS

With the rapid developments of power electronic devices and technologies, there are serious design challenges in the modern electrical systems. The modeling techniques introduced in this dissertation provide powerful tools for the system designers. With the assistant of the measurement-based characterizations, analytical system-level models can be established to accurately predict the system performance for both the PDN and WPT systems. Based on the system-level models, practical methodologies are also proposed to accelerate the development process at the pre and post design stages.

In the first paper, a novel pattern-based analytical method is proposed for the impedance calculation. By utilizing the relative relationships between the adjacent vias, the localized via patterns are formulated based on the physical geometry. Then, the parasitic via inductance and resistance are analytically derived for arbitrary via patterns. In addition, a practical modeling methodology is developed to model and guide the PDN design. With the capability of accurate and layout-free impedance estimation, this methodology is especially useful for the pre-design stage to accelerate the development process. Finally, the proposed analytical equations and the modeling methodology have been extensively validated through the measurements and simulations on a real mobile phone PCB. Good agreements can be observed from both whole structure and region-by-region comparisons.

In the second paper, a generic behavior model based on the current-mode topology is developed. This behavior model includes all the key components in the voltage control

loop, the current control loop, and the power stage of VRM devices. A novel unifying method is also proposed for the transition between CCM and DCM, which significantly simplifies the circuit implementations. The model parameters are optimized through the measurement-based characterizations. Good accuracy of the proposed model can be validated using both single-phase and 3-phase VRMs. As a result, the voltage droop waveforms and the PDN impedance can be accurately predicted in the time-domain and frequency-domain, respectively. Cascading the proposed VRM model with the PCB-level and package-level PDN models enables a combined PDN analysis, which is much needed for modern PDN designs.

In the third paper, an accurate rectifier characterization method is proposed to provide a realistic load condition. On the basis of the characterized rectifier impedance, a novel system-level WPT model is presented instead of only focusing on the coil-to-coil part. The improved model considers both the fundamental frequency and higher order harmonics, which can effectively eliminate the inaccuracy caused by FHA at off-resonance conditions. Good performance of the model is validated by experimental measurements in both time and frequency domains. It shows that the system efficiency and power loss at each interior block can be accurately estimated. With the assistance of this model, a practical methodology is introduced to efficiently optimize the design parameters of a WPT system.

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