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A Discrete-Time Control Method for Fast Transient Voltage-Sag Compensation in DVR

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ABSTRACT This paper presents a discrete-time domain control scheme for balanced voltage sag compensation using a Dynamic Voltage Restorer (DVR), which is recognized to be an appropriate and economical power electronic device with which to ameliorate these disturbances. The proposed control method is implemented in the synchronous reference frame (SRF), with two nested regulators, one of which includes an integral action. This algorithm has some advantages with respect to other control algorithms, such as the fact that the proposed methodology permits all the closed-loop poles of the DVR system to be placed in the desired locations in order to define the dynamical behavior with a reduction in the number of the electrical magnitudes to be measured and without the need for state observers, as occurs in traditional control methods. What is more, the well-known inner current loop implemented in other control schemes, which is employed to attenuate the resonance of the plant, is unnecessary. Furthermore, the unbalanced voltage sag compensation can be achieved by adding a ''plug-in'' controller and following the same methodology presented for balanced voltage sags to design the controller. The good performance of the proposed control scheme is validated by means of simulation and experimental results carried out with a 5 kW DVR laboratory prototype. The discrete-time control method is also compared with two control schemes previously proposed in literature.

INDEX TERMS Discrete-time systems, dynamic voltage restorer, power quality, power system control, voltage sag.

I. INTRODUCTION

Power quality has emerged as a term of notable interest for researchers in recent years. This is principally owing to the increase in equipment connected to the electrical grid, which worsens power quality. The need for a power distribution grid whose voltage or current waveforms tend to be ideal is, therefore, an important issue that must be solved. The principal reasons for the worsening in voltages in the electrical grid are the presence of voltage sags, harmonics, imbalances and frequency deviations, which can be seen as the main disturbances that affect power distribution grids [1]. Other factors, such as the increase in the number of distributed generation systems, society's growing dependence on energy and the liberalization of the electricity market, have also lead to a deterioration in power quality [2].

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In order to deal with these disturbances and prevent their effects on sensitive loads connected to the electrical grid, several power electronic devices have been developed [3], [4]. Of these devices, DVR is a viable and effective solution for voltage-sag compensation [5], which can be viewed as the main cause of financial losses related to the electrical grid [6] and is considered as the largest disturbance in distribution systems [7].

This paper is focused on the topic of the design of the control algorithm for voltage-sag compensation in DVRs, according to [8], for which several previous control algorithms have been proposed, and for which a feedforward open loop control is the simplest solution. However, this solution has a poor transient response owing to the resonance introduced by the output filter, and might not produce zero tracking error owing to modeling errors. In order to overcome these problems, feedback or feedforward-feedback schemes, with different regulators in the feedback loop, have

been proposed to reduce the tracking error of the reference signal. The most widely used solution for the feedback loop is a proportional-integral (PI) regulator implemented in the SRF that achieves a zero tracking error for the fundamental component [9], [10]. This solution is denominated as a multi-loop scheme owing to the inclusion of an inner current-loop, which reduces the resonance of the filter. In this case, an extra sensor is required, as it is necessary to measure not only the output voltage, but also the current [11]. However, the resonance introduced by the output filter cannot be completely compensated owing to limitations of the design process with regard to the proportional current gain, such as the amplification of the capacitor current ripple. In order to speed up the transient response, some methods propose a forward loop [12], [13], but these solutions have to be treated carefully when the reference signal has step changes that may damage the DVR. These control schemes with PI controllers cannot completely compensate unbalanced voltage-sags owing to the additional component, which is twice the fundamental grid frequency, owing to the negative-sequence component. This signifies that, in order to solve the unbalanced compensation, some methods add an extra controller in the feedback loop to track this sinusoidal component. Other methods employ complex algorithms to separate the positive- and negative-sequence and apply the coordinate transformation in the SRF to both components separately [7], [14], or carry out the transformation in the stationary reference frame [15]. In [16], a state feedback strategy is proposed for balanced voltage-sag compensation and a repetitive controller is added to compensate voltage harmonics, as occurs in other methods [17]. In [18], an adaptive self-tuned-PI control scheme is presented in order to compensate voltage sags while compensating the DVR losses. Nevertheless, the results show a slow transient response of the load voltage. A control method based on a PID controller for a DVR transformerless topology can be found in [19], and a secondary controller with which to track the 100 Hz component is added for unbalanced voltage-sag compensation [20].

Other solutions for balanced and unbalanced voltage-sag compensation include a P + Resonant controller implemented in a stationary coordinate system $\alpha - \beta$ [21], [22]. These control schemes have a slow transient response and a noticeable overshoot. The addition of a Posicast regulator improves the overshoot [21], [23], as the resonance is reduced. A control method with a similar behavior to these is presented in [24], in which an H∞ controller provides a more robust performance for frequency deviations. In [25], a P + Resonant control scheme with two degrees of freedom is presented, which has a faster transient response when compared to other P + Resonant controllers. However, the control implies a great mathematical effort when the chosen poles of the closed-loop system have a multiplicity greater than 1, and the poles introduced by the implementation of the delay may modify the dynamic behavior of the system, as they are dependent on the sampling frequency. Finally, a non-linear method based on a generalized PI controller for a single-phase system is detailed in [26], but its transient response is considerably slower.

PI and P + Resonant regulators are, in keeping with the internal-mode principle (IMP), commonly employed in applications that demand zero tracking error when the reference is a step signal (reference voltage in the SRF) and a sinusoidal waveform (reference voltage in the $\alpha - \beta$ axes), respectively. These regulators are suitable for first-order systems owing to the fact that they include two design parameters in their transfer function. Nevertheless, in the case of a DVR, whose plant is modeled as a second-order transfer function or even as higher order transfer functions, the performance achieved can be very poor. The main reason for this is that these control schemes cannot entirely define the system behavior, as they do not have sufficient design parameters to be able to choose the position of all the closed-loop poles. The discrete-time control proposed can solve this problem when the fundamental component is tracked, because it contains the number of design parameters required to define completely the location of all the poles of the closed-loop system, although the zeros cannot be freely placed. For that reason, a control structure based on two nested regulators is used, which allows to choose all the poles of the closed-loop and minimizes the number of the zeros added to the closed-loop transfer function.

This paper presents a control method for voltage-sag compensation in a DVR. The control method for balanced compensation is based on the structure with two nested regulators presented in [25]. The proposed control is implemented in the discrete-time domain and allows the complete definition of the location of the poles of the closed-loop transfer function without the use of observers and a reduction in the number of signals to be measured. The unbalanced sag compensation is accomplished by including a resonant regulator in a ''plug-in'' structure, which is tailored following the same methodology explained for the design of the control scheme for balanced voltage sags. Although the methodology employed allows the control system to be designed using any reference frame, e.g., the stationary reference frame or a reference frame rotating at an arbitrary angular speed, the SRF has been chosen, since the algorithm can achieve zero-tracking error for the fundamental component by including a simple integral action. Moreover, the computational delay, which is related to the control implementation on a digital platform, is taken into account in order to obtain a successful behavior for the DVR. Unlike reference [25], the design of the control parameters can be tailored with no restrictions for the sampling frequency when the closed-loop poles are defined in the discrete-time domain. Furthermore, as the design of the controller is tailored in discrete time, all the parameters of the control system are obtained by simply inverting a matrix in order to solve a set of linear equations, even when the desired poles of the closed-loop system have a multiplicity greater than one. Thus, the mathematical effort in the design process is drastically reduced compared to the method presented in [25]. The control performance, for both types of sags, has a

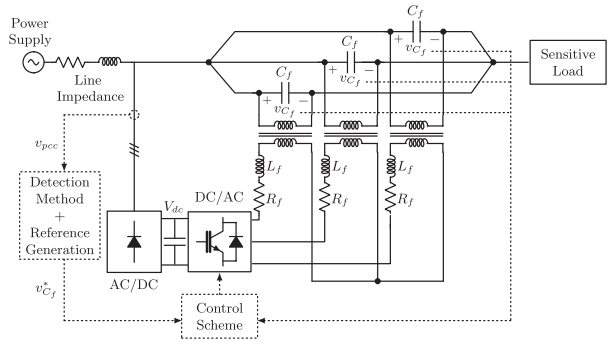

FIGURE 1. Typical configuration of a power system with a DVR.

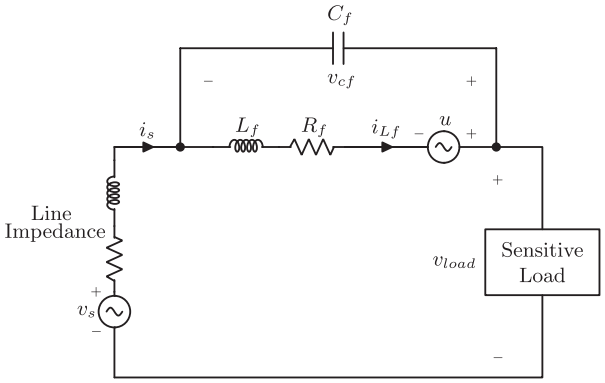

FIGURE 2. Single-phase equivalent circuit for the connection system of the DVR.

fast transient response and a zero steady-state error. The in-phase compensation strategy is employed for simulation and experimental results. Nevertheless, the design procedure of the algorithm allows the controller to be combined with other control strategies.

The remainder of this paper is organized as follows. The DVR model, the discrete-time control methodology for balanced voltage-sag, a solution for unbalanced voltage-sag compensation and the design procedures are presented in Section II. The simulations carried out in PSCAD/EMTDC and the experimental results obtained in a DVR laboratory prototype for the proposed control method are shown in Sections III and IV, respectively. Furthermore, in Section IV a comparison with other control methods is presented. Finally, Section V provides the overall conclusions of the paper.

II. PROPOSED DISCRETE-TIME CONTROL SCHEME

A. DVR MODEL

The well-known scheme of a power system in which a DVR is included to protect a sensitive load is shown in Fig. 1, although various different configurations have been proposed [27], including transformerless topologies [28]. The DVR is a series compensator that is usually composed of:

- An energy storage system or an alternative power source.
- A voltage source converter (VSC).
- An output filter.
- A coupling transformer.

The control design process starts with the model of the DVR. Taking into consideration that the VSC works at a sufficiently high switching frequency, the VSC can be evaluated as a linear amplifier. The DVR can consequently be modeled as an ideal voltage source connected in series with an LC filter, as shown in Fig. 2, in which the single-phase equivalent circuit of the connection system of the DVR is plotted. The three-phase state-space model of the DVR, i.e. in *abc* coordinates, can be expressed in the SRF as [29]:

$$\frac{d}{dt}\begin{bmatrix} v_{cfd} \\ v_{cfq} \\ i_{Lfd} \\ i_{Lfq} \end{bmatrix} = \mathbf{A_1}\begin{bmatrix} v_{cfd} \\ v_{cfq} \\ i_{Lfd} \\ i_{Lfq} \end{bmatrix} + \mathbf{B_1}\begin{bmatrix} i_{sd} \\ i_{sq} \\ u_d \\ u_q \end{bmatrix}, \tag{1}$$

with:

$$\mathbf{A_1} = \begin{bmatrix} 0 & \omega_1 & \frac{1}{C_f} & 0 \\ -\omega_1 & 0 & 0 & \frac{1}{C_f} \\ -\frac{1}{L_f} & 0 & -\frac{R_f}{L_f} & \omega_1 \\ 0 & -\frac{1}{L_f} & -\omega_1 & -\frac{R_f}{L_f} \end{bmatrix} \tag{2}$$

$$\mathbf{B_1} = \begin{bmatrix} -\frac{1}{C_f} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_f} & 0 & 0 \\ 0 & 0 & \frac{1}{L_f} & 0 \\ 0 & 0 & 0 & \frac{1}{L_f} \end{bmatrix} \tag{3}$$

where v_{cfd} and v_{cfq} are the variables to be controlled, which are the $d-q$ components of the capacitor voltage, i_{Lfd} and i_{Lfq} are the leakage inductance currents, i_{sd} and i_{sq} are the sensitive load currents, u_d and u_q are the output voltage of the VSC and, finally, ω_1 is the angular speed of the SRF ($\omega_1 = 100\pi$ rad/s) that coincides with the nominal frequency of the grid voltage. C_f is the capacitor of the output filter, L_f is the filter inductance plus the transformer leakage inductance and R_f models the transformer copper losses.

The state-space model in equation (1) shows that the input variables i_{sd} and i_{sq} can be considered as disturbances, whereas u_d and u_q are the variables used to control the capacitor voltages (v_{cfd} and v_{cfq}). The disturbances can be compensated, [24], with the feedforward term $\hat{P}_1^{-1}(s)$ by considering the following transfer functions for the model:

$$P_1(s) = \frac{1}{R_f + L_f s}, \quad P_2(s) = \frac{1}{C_f s} \tag{4}$$

This feedfoward action minimizes the effect of the current of the sensitive load on the capacitor voltage. The scheme for the DVR plant in *abc* coordinates with the transfer functions

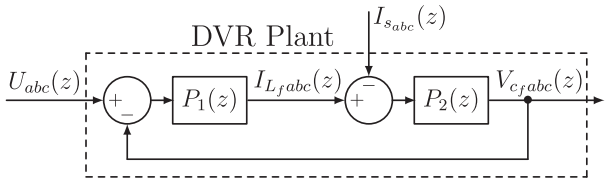

FIGURE 3. DVR plant in *abc* coordinates.

P_1 and P_2, the control inputs, the disturbances and the output variables, i.e., the capacitor voltages, is plotted in Fig. 3.

System (1) shows that variables v_{cfd} and v_{cfq} are coupled and changes in one of the voltages, therefore, affect the dynamics of the other component. Fortunately, the whole system can be decoupled using the following fictitious signals obtained from equation (1):

$$U_{cd}(s) = U_d(s) - (L_f s + R_f) I_{sd}(s) + W_{cd}(s) \quad (5)$$

$$U_{cq}(s) = U_q(s) - (L_f s + R_f) I_{sq}(s) + W_{cq}(s) \quad (6)$$

being:

$$W_{cd}(s) = \omega_1 L_f I_{Lfq}(s) + \omega_1 C_f (L_f s + R_f) V_{cfq}(s) \quad (7)$$

$$W_{cq}(s) = -\omega_1 L_f I_{Lfd}(s) - \omega_1 C_f (L_f s + R_f) V_{cfd}(s) \quad (8)$$

The resultant plant of the DVR can, for both components in the Laplace domain, then be written as the transfer function of a general second-order system:

$$G(s) = \frac{V_{cf}(s)}{U_c(s)} = \frac{\omega_n^2}{s^2 + s2\xi\omega_n + \omega_n^2} \quad (9)$$

where $U_c(s)$ is the fictitious control signal, the natural frequency is $\omega_n^2 = 1/(C_f L_f)$ and the damping ratio is obtained as $\xi = \frac{R_f}{2}\sqrt{\frac{C_f}{L_f}}$.

Finally, as the control will be implemented on a digital platform, the transfer function of the equivalent discrete-time model of the DVR, including the computational delay, can be expressed as a third-order system:

$$G(z) = \frac{1}{z} \cdot \frac{zb_3 + b_2}{z^2 + zb_1 + b_0} \quad (10)$$

where b_3, b_2, b_1 and b_0 are the coefficients calculated using a zero-order hold transformation in (9), [30].

B. DISCRETE-TIME CONTROL SCHEME METHODOLOGY

Equation (10) demonstrates that a simple PI controller does not contain sufficient parameters to be able to choose all the poles of the closed-loop system. The proposed discrete-time control scheme for the system plotted in Fig. 1 is based on a structure with two nested regulators implemented in the SRF, as shown in Fig. 4, in which one of them incorporates an integral action in order to ensure zero tracking error in steady-state. By using this structure, and if the transfer functions of both regulators are properly chosen, it is possible to obtain a denominator in which all the poles can be arbitrarily chosen, signifying that the dynamic behavior of the system can be defined by the designer.

In order to find the particular expressions for both controllers that ensure the balanced voltage-sag compensation, the control scheme must be able to compensate the DC component in the SRF and, therefore, $R_1(z)$ should have at least one pole at $+1$ in the z-plane.

According to Fig. 4, the closed-loop transfer function can be directly obtained as:

$$\begin{aligned} H(z) &= \frac{V_{cf}(z)}{V_{cf}^*(z)} = \frac{G(z)R_1(z)}{1 + G(z)(R_1(z) + R_2(z))} \\ &= \frac{G(z)n_{R_1}(z)}{d_{R_1}(z) + G(z)\left(n_{R_1}(z) + d_{R_1}(z)\frac{n_{R_2}(z)}{d_{R_2}(z)}\right)} \end{aligned} \quad (11)$$

where $n_{R_1}(z)$ and $n_{R_2}(z)$ are the numerators of the $R_1(z)$ and $R_2(z)$ controllers, respectively, $d_{R_1}(z)$ is the denominator of $R_1(z)$, and $V_{cf}^*(z)$ is the reference for the capacitor voltage $V_{cf}(z)$.

If the transfer functions $R_1(z)$ and $R_2(z)$ are defined as:

$$\begin{aligned} R_1(z) &= \frac{\lambda_0}{(z-1)(z+\sigma_0)(z+\sigma_1)} \\ R_2(z) &= \frac{z^2\lambda_3 + z\lambda_2 + \lambda_1}{(z+\sigma_0)(z+\sigma_1)} \end{aligned} \quad (12)$$

The characteristic polynomial of the closed-loop transfer function can be written as:

$$p(z) = z^6 + z^5\alpha_5 + z^4\alpha_4 + z^3\alpha_3 + z^2\alpha_2 + z\alpha_1 + \alpha_0 \quad (13)$$

It is worth mentioning that the number of design parameters in (12) is equal to the polynomial degree of (13). Taking into account that the term $(z + \sigma_0)(z + \sigma_1)$ can be rearranged as $(z^2 + z\gamma 1 + \gamma 0)$, the coefficients of equation (13) can be obtained according to the plant parameters and the parameters of both regulators:

$$\begin{aligned} \alpha_5 &= \gamma_1 + b_1 - 1 \\ \alpha_4 &= \lambda_3 b_3 + \gamma 1(b_1 - 1) + \gamma 0 + b_0 - b_1 \\ \alpha_3 &= \lambda_2 b_3 + \lambda_3(b_2 - b_3) + \gamma_1(b_0 - b_1) + \gamma_0(b_1 - 1) - b_0 \\ \alpha_2 &= \lambda_1 b_3 + \lambda_2(b_2 - b_3) - \lambda_3 b_2 - \gamma_1 b_0 + \gamma_0(b_0 - b_1) \\ \alpha_1 &= \lambda_0 b_3 + \lambda_1(b_2 - b_3) - \lambda_2 b_2 - \gamma_0 b_0 \\ \alpha_0 &= \lambda_0 b_2 - \lambda_1 b_2 \end{aligned} \quad (14)$$

If the characteristic polynomial is yielded with the desired poles for the closed-loop system, equation (13) can be written as:

$$p(z) = (z-p_1)(z-p_2)(z-p_3)(z-p_4)(z-p_5)(z-p_6) \quad (15)$$

where p_1, p_2, p_3, p_4, p_5 and p_6 are the desired poles of the closed-loop transfer function. The coefficients α_5, α_4, α_3, α_2, α_1 and α_0 can, therefore, be directly obtained by operating with equation (15). The design parameters of the controllers can alternatively be obtained using a matrix form as:

$$\mathbf{M_1 x_1} = \mathbf{N_1} \quad (16)$$

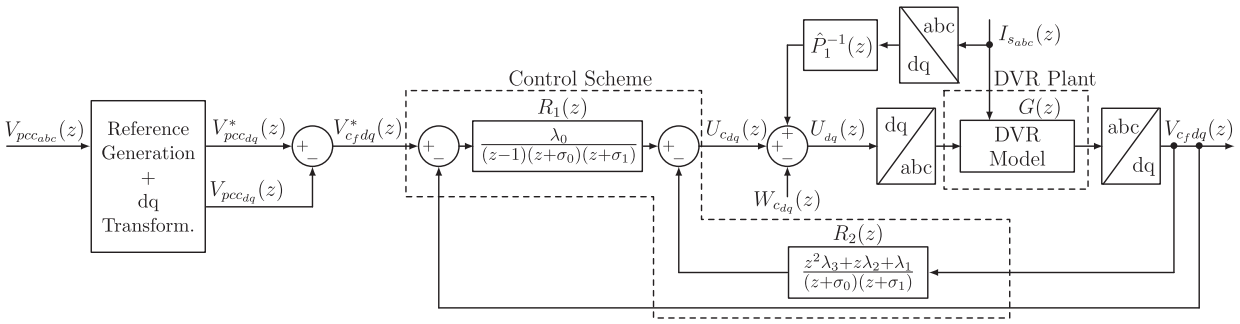

FIGURE 4. Proposed control scheme.

TABLE 1. Parameters of $R_1(z)$ and $R_2(z)$ controllers for the design example.

Parameter	Value
λ_0	0.0036
λ_1	−1.2937
λ_2	2.5656
λ_3	−1.5837
γ_0	0.8114
γ_1	−1.4290

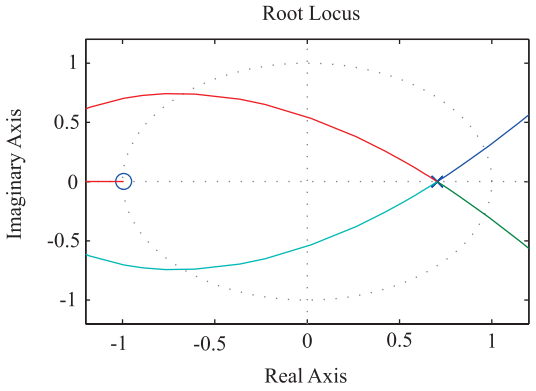

FIGURE 5. Root locus plot of the closed-loop system for the proposed control.

where $\mathbf{x_1} = [\lambda_0\ \lambda_1\ \lambda_2\ \lambda_3\ \gamma_0\ \gamma_1]^{\mathrm{T}}$, and $\mathbf{M_1} \in \Re^{6\times6}$ and $\mathbf{N_1} \in \Re^{6\times1}$. The elements of both matrices are defined as shown in equation (17).

Matrix $\mathbf{x_1}$, with the parameters of both regulators, can be calculated by inverting matrix $\mathbf{M_1}$, i.e., $\mathbf{x} = \mathbf{M_1}^{-1} \cdot \mathbf{N_1}$, if matrix $\mathbf{M_1}$ is full rank and square, even when the desired poles have a multiplicity greater than one.

The final step in the design methodology is to choose the location of the poles of the closed-loop transfer function that define the dynamic response of the system. The location of the poles can be directly chosen in the discrete domain or, alternatively, in the continuous domain, for an easy interpretation, and transformed into an equivalent discrete model.

This scheme, in fact, achieves $|H(z = 1)| = 1$ and $\angle H(z = 1) = 0°$ for $z = e^{j0T_s}$, which proves that the DC component is properly tracked. The methodology described enables the dynamical behavior of the system to be defined with the location of the closed-loop poles. It should be noted that the control scheme does not require state observers or estimators.

A design example in which the poles are chosen in $p_i = 0.704$ in the discrete-time domain, in which the multiplicity of the pole is equal to six ($m_{p_i} = 6$) and by considering a sampling period $T_s = 100\ \mu$s for the discretization, is now presented. It should be stressed that the equivalent poles in the continuous domain are located in $p_c = -3500$ rad/s (≈ -557 Hz), which provides a fast dynamic response. Table 1 shows the parameters of the $R_1(z)$ and $R_2(z)$ controllers obtained for the design example. Note that the parameters have reasonable values for the digital implementation.

The root locus of the closed-loop system for the control designed in the discrete-time domain is shown in Fig. 5.

The Bode diagram of the closed-loop system designed is shown in Fig. 6. The system response has the desired low-pass behavior with a unity gain for the DC component. Furthermore, the relative stability margins for the control system are calculated from the Bode diagram, obtaining a gain margin of 9.13 dB at the phase crossover frequency of $1.69 \cdot 10^3$ rad/s and a phase margin of 64.4° at the gain crossover frequency of 514 rad/s. These values fulfill the requirements for a satisfactory performance [31].

$$\mathbf{M_1} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & b_3 & (b_1 - 1) & 1 \\ 0 & 0 & b_3 & (b_2 - b_3) & (b_0 - b_1) & (b_1 - 1) \\ 0 & b_3 & (b_2 - b_3) & -b_2 & -b_0 & (b_0 - b_1) \\ b_3 & (b_2 - b_3) & -b_2 & 0 & 0 & -b_0 \\ b_2 & -b_2 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad \mathbf{N_1} = \begin{bmatrix} \alpha_5 - b_1 + 1 \\ \alpha_4 + b_1 - b_0 \\ \alpha_3 + b_0 \\ \alpha_2 \\ \alpha_1 \\ \alpha_0 \end{bmatrix} \tag{17}$$

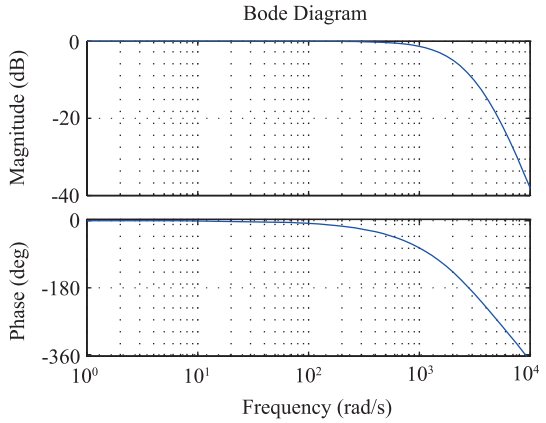

FIGURE 6. Bode diagram of the closed-loop system for the proposed control.

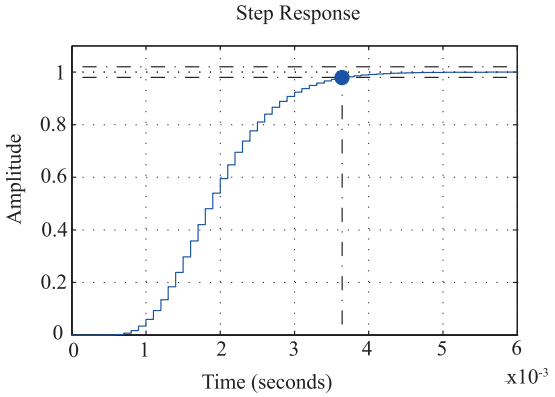

FIGURE 7. Step response of the closed-loop system for the proposed control.

Finally, the step response of the system for the example designed is shown in Fig. 7. As can be seen, this design provides a 2%-settling time of 3.64 ms without overshoot. This control scheme can consequently compensate balanced voltage-sags with zero steady-state error and fast time response.

C. DISCRETE-TIME CONTROL SCHEME FOR UNBALANCED VOLTAGE SAG COMPENSATION

In order to compensate imbalances, the control scheme must be defined to track the 100 Hz component in the SRF. A possible option is to employ a resonant controller, $R_W(z)$, in a "plug-in" structure as shown in Fig. 8. The design of this controller can be achieved by means of analytical or graphical methods. To support the methodology presented in this paper, the overall control for unbalanced voltage sag compensation is designed following the same procedure shown in Section II-B. In order to overcome the design of the control, the new transfer function $G_a(z)$ is defined as:

$$G_a(z) = \frac{G(z)R_1(z)}{1 + G(z)R_2(z)} \tag{18}$$

where the input of $G_a(z)$ is the output of the "plug-in" structure, $R'_W(z) = R_W(z) + 1$, which can be rearranged as a transfer function as:

$$R'_W(z) = \frac{z^2c_3 + zc_2 + c_1}{z^2 + zc_0 + 1} \tag{19}$$

In order to compensate the angular frequency at 100 Hz in the SRF, the parameter c_0 can, therefore, be calculated as $-2 \cdot \cos(2\omega_1 T_s)$. Furthermore, as the regulator $R'_W(z)$ adds two additional poles to the closed-loop system, the design parameters c_3, c_2 and c_1 will be used to completely define the location of all the poles of the resulting closed-loop system.

The closed-loop transfer function can be directly obtained, operating with equations (18) and (19), as:

$$H(z) = \frac{G(z)n_{R_1}(z)n_{R'_W}(z)}{d_{R_1}(z) + G(z)\left(n_{R_1}(z)n_{R'_W}(z) + d_{R'_W}(z)\frac{n_{R_2}(z)}{d_{R_2}(z)}\right)} \tag{20}$$

where $n_{R'_W}(z)$ and $d_{R'_W}(z)$ are the numerator and the denominator of $R'_W(z)$, respectively. Its characteristic polynomial is similar to the one presented in equation (13) but, in this case, with an order of eight. Following the methodology presented in Section II-B, the parameters of the characteristic polynomial can be calculated according to the plant and the regulators parameters as:

$$\begin{aligned}
\alpha_7 &= \gamma_1 + b_1 - 1 + c_0 \\
\alpha_6 &= \gamma_1(b_1 + c_0 - 1) + \gamma_0 + \lambda_3 b_3 + b_0 - b_1 \\
&\quad + c_0(b_1 - 1) + 1 \\
\alpha_5 &= \gamma_1(b_0 - b_1 + c_0(b_1 - 1) - 1) + \gamma_0(b_1 + c_0 - 1) \\
&\quad + \lambda_3(b_2 + b_3(c_0 - 1)) + \lambda_2 b_3 + b_1 - b_0 \\
&\quad + c_0(b_0 - b_1) - 1 \\
\alpha_4 &= \gamma_1((b_1 - b_0)(1 - c_0) - 1) \\
&\quad + \gamma_0(b_0 - b_1 + c_0(b_1 - 1) + 1) \\
&\quad + \lambda_3((b_3 - b_2)(1 - c_0)) + \lambda_2(b_2 + b_3(c_0 - 1)) \\
&\quad + \lambda_1 b_3 + b_0 - b_1 - c_0 b_0 \\
\alpha_3 &= \gamma_1(b_0(1 - c_0) - b_1) \\
&\quad + \gamma_0((b_1 - b_0)(1 - c_0) - 1) + \lambda_3(b_2(1 - c_0) - b_3) \\
&\quad + 0\lambda_2((b_3 - b_2)(1 - c_0)) + \lambda_1(b_2 + b_3(c_0 - 1)) \\
&\quad + c_3 b_3 \lambda_0 - b_0 \\
\alpha_2 &= -\gamma_1 b_0 + \gamma_0(b_0(1 - c_0) - b_1) - \lambda_3 b_2 \\
&\quad + \lambda_2(b_2(1 - c_0) - b_3) + \lambda_1((b_3 - b_2)(1 - c_0)) \\
&\quad + c_3 b_2 \lambda_0 + c_2 b_3 \lambda_0 \\
\alpha_1 &= -\gamma_0 b_0 - \lambda_2 b_2 + \lambda_1(b_2(1 - c_0) - b_3) + c_2 b_2 \lambda_0 \\
&\quad + c_1 b_3 \lambda_0 \\
\alpha_0 &= -\lambda_1 b_2 - c_1 b_2 \lambda_0
\end{aligned} \tag{21}$$

The parameteres α_7, α_6, α_5, α_4, α_3, α_2, α_1 and α_0 can, therefore, be obtained through the characteristic polynomial with the desired poles:

$$\begin{aligned}
p(z) &= (z - p_1)(z - p_2)(z - p_3)(z - p_4) \\
&\quad \cdot (z - p_5)(z - p_6)(z - p_7)(z - p_8) \\
&= z^7 + z^6\alpha_6 + z^5\alpha_5 + z^4\alpha_4 \\
&\quad + z^3\alpha_3 + z^2\alpha_2 + z\alpha_1 + \alpha_0
\end{aligned} \tag{22}$$

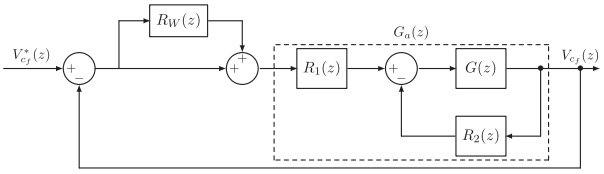

FIGURE 8. Scheme with the "plug-in" structure.

TABLE 2. Parameters of $R_1(z)$, $R_2(z)$ and $R'_W(z)$ controllers for the design example.

Parameter	Value
γ_1	-0.8465
γ_0	0.5154
λ_3	-0.2502
λ_2	0.7384
λ_1	-0.5711
c_3	0.0826
c_2	-0.1592
c_1	0.0770

where $p_1, p_2, p_3, p_4, p_5, p_6, p_7$ and p_8 are the desired poles of the closed-loop transfer function for unbalanced voltage sag compensation.

As there are nine design parameters and eight poles to be obtained, there is an extra degree of freedom and one of the design parameters can, therefore, be freely chosen. If the parameter λ_0 is considered equal to one, the design parameters of the controllers can be calculated using the matrix form $\mathbf{M_2 x_2} = \mathbf{N_2}$. The terms of matrices $\mathbf{M_2}$ and $\mathbf{N_2}$ can be extracted from equation (21), while the parameters matrix is $\mathbf{x_2} = [\gamma_1\ \gamma_0\ \lambda_3\ \lambda_2\ \lambda_1\ c_3\ c_2\ c_1]^{\mathrm{T}}$.

In order to continue with the design methodology, the poles are chosen at the same locations ($p_i = 0.704$) as in Section II-B:
in this case the multiplicity of the pole is equal to eight (m_{p_i}=8). With this new design, the transient response is slightly slower, obtaining a settling time of approximately 5.4 ms.

The resulting parameters of the regulators $R_1(z)$, $R_2(z)$ and $R'_W(z)$ are shown in Table 2, while the root locus of the closed-loop system for the control designed in the discrete-time domain is shown in Fig. 9.

D. IMPLEMENTATION OF THE DISCRETE-TIME CONTROL SCHEME

The control designed in Section II-C can be used for balanced and unbalanced voltage sag compensation. However as this control provides a transient response slower than that obtained in Section II-B, the "plug-in" controller $R_W(z)$ is only used when unbalanced voltage sags occur, which implies that a detection system for the negative sequence of the grid voltage is needed: When a voltage sag takes place, if a negative sequence is detected, the "plug-in" regulator $R_W(z)$ is connected. Otherwise, only the proposed control scheme with the controllers $R_1(z)$ and $R_2(z)$ for the DC component is used. Nevertheless, if a scenario is defined in which both types of voltage sags can occur, only the control scheme designed for unbalanced voltage sags should be used, as a sudden change between both control schemes might cause undesired transient responses and even instability.

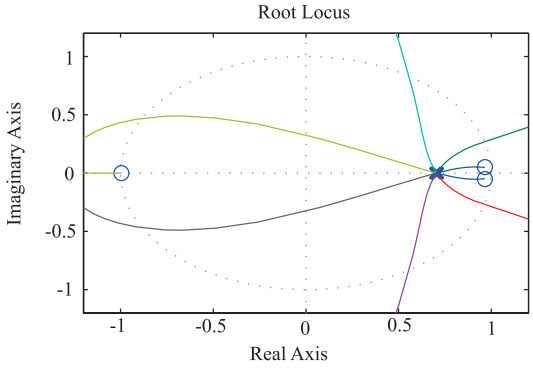

FIGURE 9. Root locus plot of the closed-loop system for the proposed control for unbalanced voltage sag compensation.

TABLE 3. Parameters of the system in PSCAD/EMTDC.

Electrical Grid	RMS line-to-line voltage: 400 V Frequency: 50 Hz
Coupling Transformer	Aparent power: $S = 20$ kVA Voltage windings: 400 V/400 V Winding resistance: $R = 0.95\ \Omega$ Leakage inductance: $L = 4.15$ mH No-load losses have been ignored
Output filter	Capacitor: $C_f = 8\ \mu$F Cutoff frequency: $f_c = 700$ Hz Inductance: $L_f = 6.48$ mH Series resistance: $R_L = 1.095\ \Omega$
Voltage-Source-Converter	DC-link voltage: $V_{dc} = 600$ V Switching frequency: 10000 Hz Three-phase converter
Sensitive Load	$R = 32\ \Omega$

With regard to the detection method, not only does it estimates the positive-sequence and negative-sequence components, but it also generates the reference signal required for the capacitor voltage $V^*_{cf}(z)$, as explained in [25], and is used to obtain the transformed variables in the SRF. Although different methods can be found in literature for this purpose [32], in this work, the detection of the voltage sags is carried out by employing the method proposed in [33], as it is robust to frequency deviations of the grid voltage.

III. SIMULATION RESULTS

In order to test the performance of the proposed control method for balanced voltage-sag compensation in a DVR, the scheme shown in Fig. 1 has been implemented in PSCAD/EMTDC. Table 3 shows the most relevant parameters used for simulations, whereas the sampling period and the location of the poles are the same as those defined in Section II-B. In addition, the rectifier AC/DC stage has been substituted with an ideal DC voltage source.

The performance of the DVR with the discrete-time control proposed has been tested for a balanced voltage-sag, in which the grid voltages decrease from their nominal val-

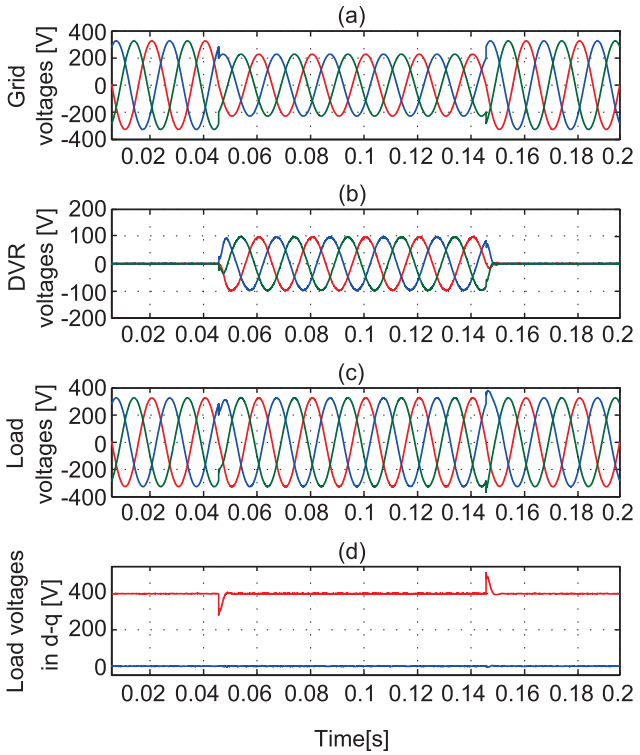

FIGURE 10. Simulation results for a balanced voltage sag with the proposed control: (a) Grid voltages, (b) voltages injected by the DVR, (c) load voltages, and (d) load voltages in $d-q$.

ues by 30%. The voltage-sag appears at $t = 0.05$ s and the voltages recover their nominal values at $t = 0.15$ s. Fig. 10(a) shows the line-to-neutral voltages at the PCC, Fig. 10(b) shows the voltages generated by the DVR, while the instantaneous load voltages and the load voltages in $d-q$ are shown in Figs. 10(c) and 10(d), respectively. As will be noted, the proposed discrete-time control compensates the balanced voltage-sag very quickly (in approximately 3.8 ms). Furthermore, there is no overshoot for the transient response and the errors are negligible for the steady-state. It should be noted that the voltages generated by the DVR do not have any peak when the voltage-sag starts and the control signals are not, therefore, critical.

IV. EXPERIMENTAL SETUP AND RESULTS

The discrete-time control scheme designed, along with the in-phase compensation strategy, were tested on a DVR laboratory test-rig. The prototype was constructed following the topology shown in Fig. 1. The PCC voltages are emulated with the ELGAR SW10500 programmable voltage supply (10.5 kVA). The series connection between the grid and the DVR is carried out using three single-phase transformers of 440 V/440 V and 4.4 kVA. The converter is the SKS 22FB6U + E1CIF + B6CI 13 V12 mounted by SEMIKRON. This power converter is composed of a rectifier stage and an inverter stage (a three-phase two-level voltage-source converter), both of which are connected to a common DC-link or DC bus with voltage V_{dc}. The LC output filter

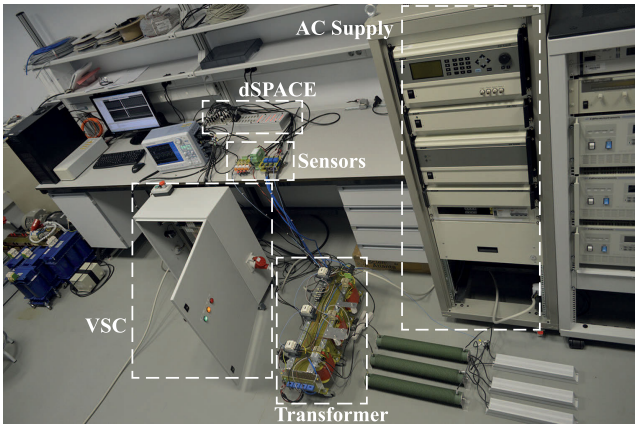

FIGURE 11. Experimental setup of the DVR prototype.

consists of an additional inductance of 2.33 mH with a resistance of 145 mΩ, connected between the inverter stage of the power electronic converter and the transformer, and a capacitor of 8 μF that is connected on the grid side. Note that the leakage inductance of the transformer, which is 4.15 mH with a resistance of 0.95 Ω, is considered to be part of the output filter. A resistive load of 32 Ω is used for experimental tests. The voltage measurements are taken with three LEM LV-25P voltage sensors and the current measurements are obtained with three LA55P current sensors. The control algorithm for the DVR has been carried out on the DS1103 real-time platform, with a sampling frequency of 10 kHz, i.e. the sampling period is 100 μs. The switching frequency is also 10 kHz and the location of the poles are the same as those defined in Sections II-B and II-C. All the derivative actions have been implemented in the real-time platform using the backward approximation in discrete time, $s \approx \frac{z-1}{zT_s}$, in order to obtain causal systems. A photograph of the DVR laboratory setup is shown in Fig. 11.

A. EXPERIMENTAL RESULTS WITH THE PROPOSED CONTROL SCHEME FOR BALANCED VOLTAGE SAGS

In the first test, the behavior of the control method designed for a balanced voltage-sag, in which the voltages at the PCC were reduced from their nominal values by 40%, was tested. The balanced sag was generated with a duration of 100 ms. Fig. 12(a) shows the grid voltages, the voltages injected by the DVR are shown in Fig. 12(b), whereas the instantaneous load voltages and the load voltages in $d-q$ are shown in Figs. 12(c) and 12(d), respectively. Finally, the currents through the resistive load are shown in Fig. 12(e). It is clear that when the sag appears, the DVR generates the necessary voltages with a very fast transient response of approximately 3.8 ms, without overshoot and with a steady-state error that can be ignored. A detail of the transient response is shown in Fig. 13.

Moreover, the performance of the control scheme for a balanced voltage sag was analysed when the sensitive load is an inductive-resistive load: in this case, a 20-mH inductance

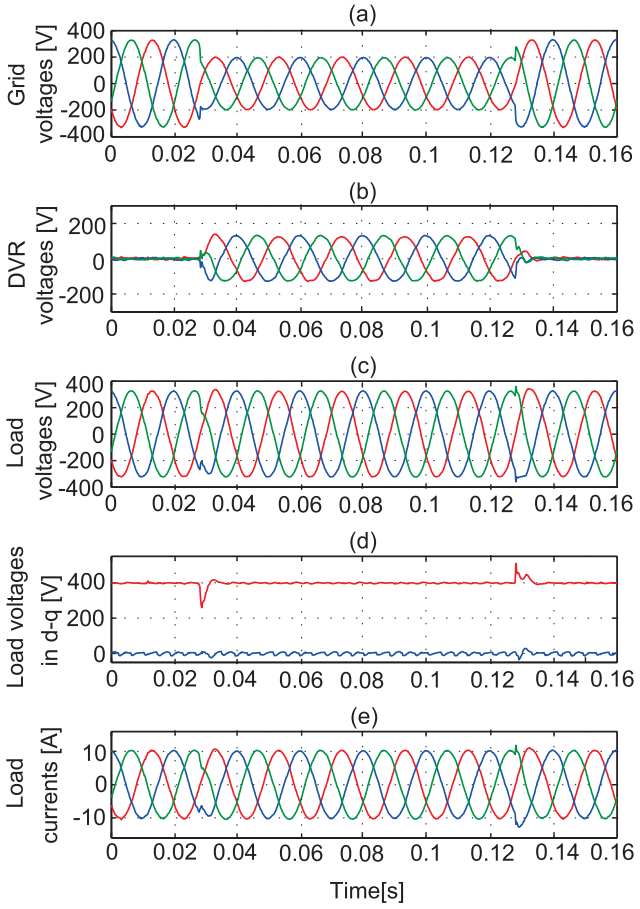

FIGURE 12. Experimental results for a balanced voltage sag with the proposed control: (a) Grid voltages, (b) voltages injected by the DVR, (c) load voltages, (d) load voltages in $d-q$, and (e) load currents.

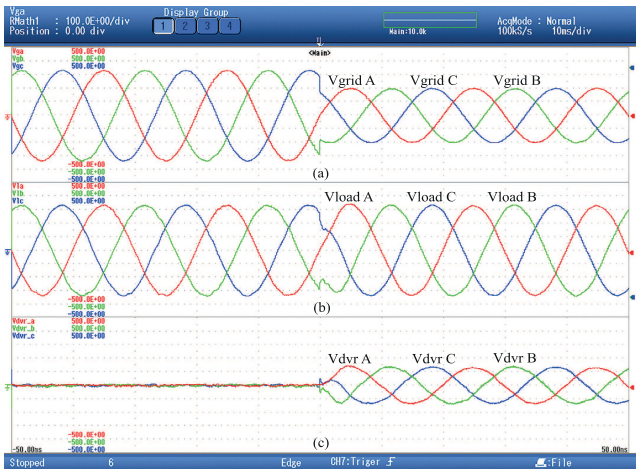

FIGURE 13. Startup transient for a 40% balanced voltage sag with the proposed control: (a) Grid voltages, (b) load voltages, and (c) voltages generated by the DVR.

is connected in series with the 32-Ω resistance. Fig. 14(a) shows the grid voltages, while the voltages generated by the DVR are shown in Fig. 14(b) and the instantaneous load voltages and the load voltages in d-q are shown in Figs. 14(c) and 14(d), respectively. Finally, the load currents are shown

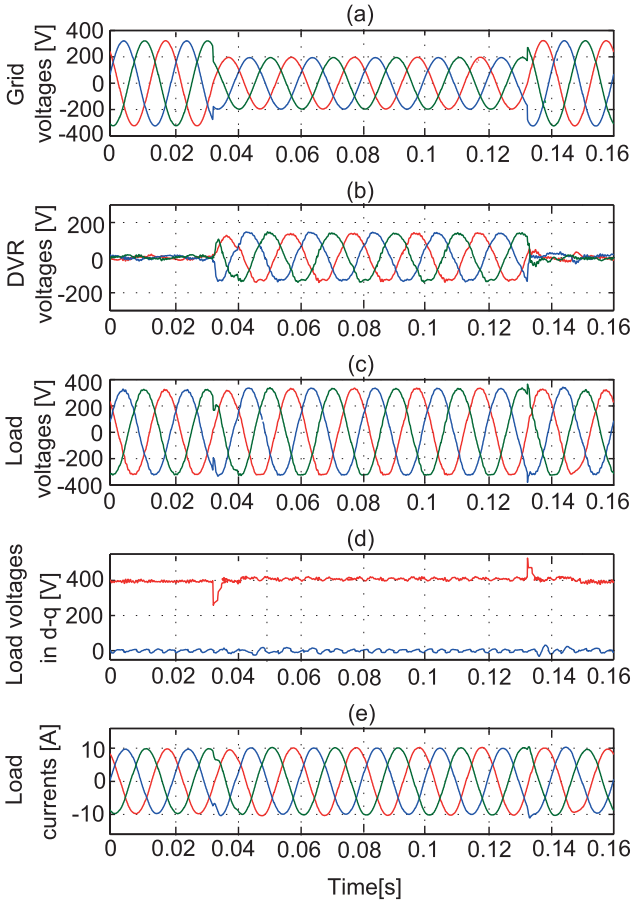

FIGURE 14. Experimental results for a balanced voltage sag with the proposed control in the SRF and an inductive-resistive load: (a) Grid voltages, (b) voltages injected by the DVR, (c) load voltages, (d) load voltages in $d-q$, and (e) load currents.

in Fig. 14(e). Furthermore, a detail of the time response for the inductive-resistive load case is shown in Fig. 15. As can be seen, the results are similar to those obtained in the case of a pure resistive load for a balanced voltage sag (see Figs. 12 and 13).

B. EXPERIMENTAL RESULTS WITH THE PROPOSED CONTROL SCHEME FOR UNBALANCED VOLTAGE SAGS

The performance when using this scheme for an unbalanced voltage sag was tested by means of an unbalanced voltage sag type B, in which one of the values of the voltage phases was reduced by 40% [34]. The grid voltages are shown in Fig. 16(a), the voltages injected by the DVR are shown in Fig. 16(b). Figs. 16(c) and 16(d) show the instantaneous load voltages and the load voltages in $d-q$, respectively, and the load currents are shown in Fig. 16(e). Furthermore, Fig. 17 shows the startup transient response when the unbalanced type-B voltage sag takes place. It should be noted that the unbalanced voltage sag can be perfectly compensated with this scheme.

The resulting time responses when applying an unbalanced type-E voltage sag, in which the values of two of the phases

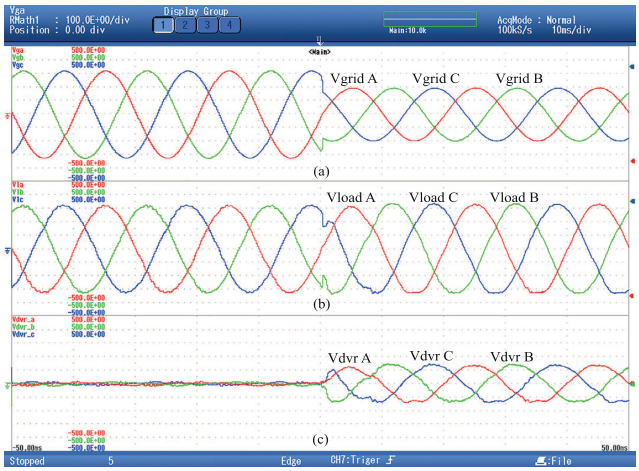

FIGURE 15. Startup transient for a 40% balanced voltage sag with the proposed control in the SRF and an inductive-resistive load: (a) Grid voltages, (b) load voltages, and (c) voltages injected by the DVR.

are reduced by 40%, for the inductive-resistive load are shown in Fig. 18. The grid voltages and the voltages provided by the DVR are shown in Figs. 18(a) and 18(b), respectively, while the instantaneous load voltages and the $d-q$ values are shown in Figs. 18(c) and 18(d), respectively, and the load currents are shown in Fig. 18(e). Furthermore, Fig. 19 shows the startup transient response for the inductive-resistive load. The control scheme and the DVR are able to compensate the unbalanced voltage sag with a similar performance to that of the case of the resistive load.

Finally, it should be noted that if the method used to obtain the transformed variables in the SRF is robust to frequency deviations of the grid voltage, the positive sequence of the voltage will be transformed into a DC component in the SRF, in spite of possible changes in that frequency. In the case of balanced voltage sags in which the voltage has only the positive sequence, this implies that the integral action of the proposed controller can compensate the voltage sag perfectly, even though the frequency of the grid voltage varies, which is an advantage with regard to the methods that employ resonant controllers in a stationary reference frame [21]–[23]. With regard to unbalanced voltage sags that contain both positive and negative sequences, the negative sequence is not completely compensated when the frequency undergoes deviations, as the ''plug-in'' structure is designed to track the component of the fixed frequency $2\omega_1$, but the positive sequence is again perfectly compensated owing to the integral action of the proposed controller.

C. COMPARISON WITH OTHER CONTROLLERS

An experimental comparison with other control methods for the resistive load has been carried out in this section. The first control scheme is presented in [22], [23] and uses a cascaded control structure with an inner loop with a proportional regulator for the current, and an outer loop that employs a P + Resonant controller for the regulation of the DVR voltage. The second solution chosen is based on the use of

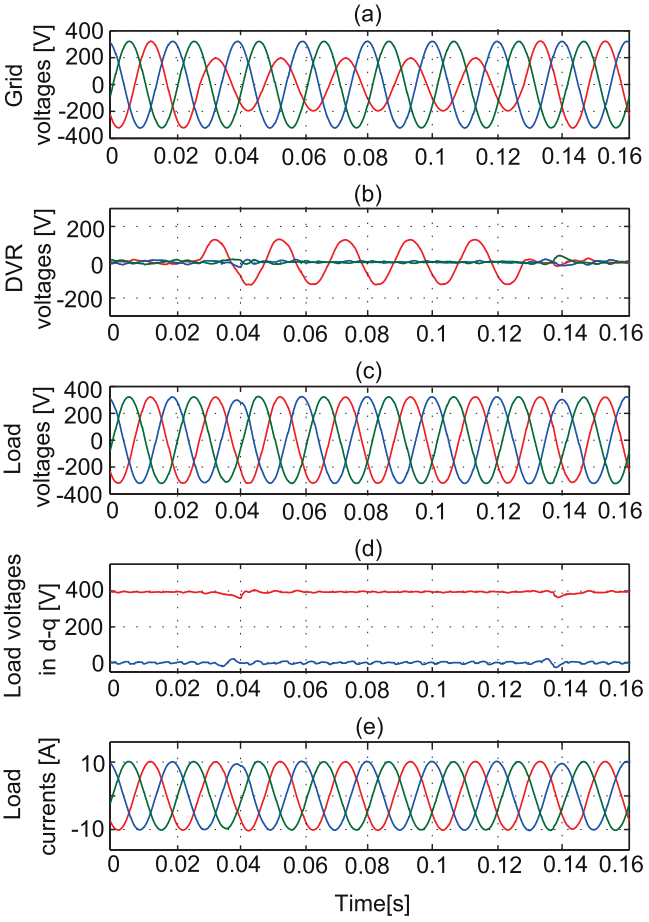

FIGURE 16. Experimental results for an unbalanced voltage sag, type B, with the proposed control plus a resonant controller: (a) Grid voltages, (b) voltages injected by the DVR, (c) load voltages, (d) load voltages in $d-q$, and (e) load currents.

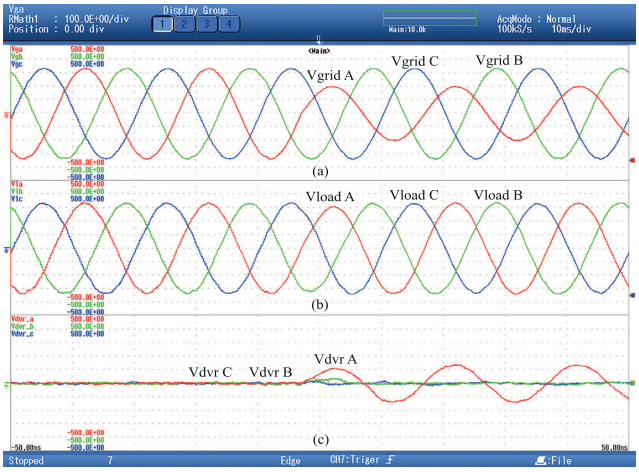

FIGURE 17. Startup transient for a 40% type B unbalanced voltage sag with the proposed control plus a resonant controller: (a) Grid voltages, (b) load voltages, and (c) voltages injected by the DVR.

a PID controller in the SRF and is presented in [19]. Both control proposals are considered to be traditional methods for voltage sag compensation. These controllers have been designed following the design procedures explained in [19],

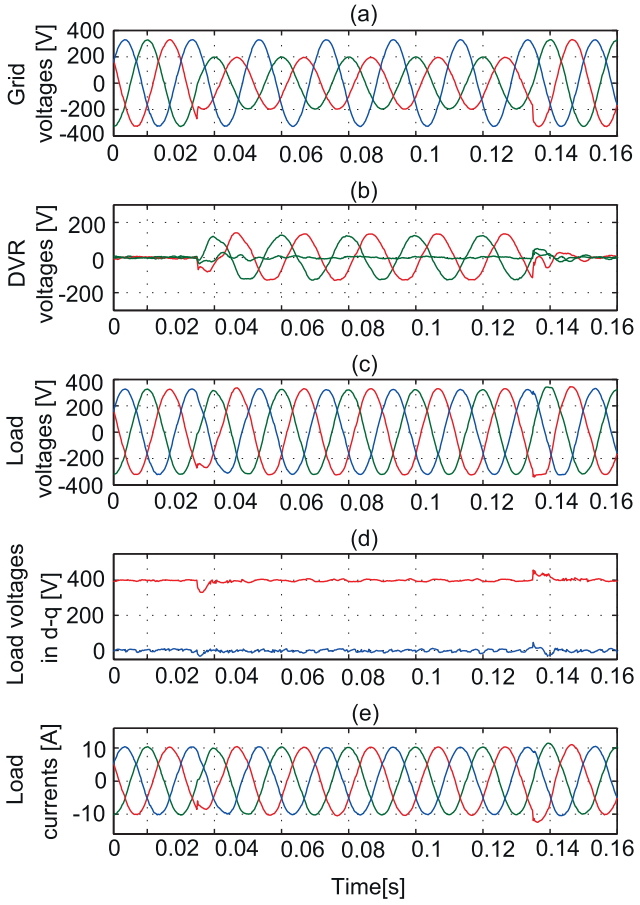

FIGURE 18. Experimental results for an unbalanced voltage sag, type E, with the proposed control plus a resonant controller and an inductive-resistive load: (a) Grid voltages, (b) voltages injected by the DVR, (c) load voltages, (d) load voltages in $d-q$, and (e) load currents.

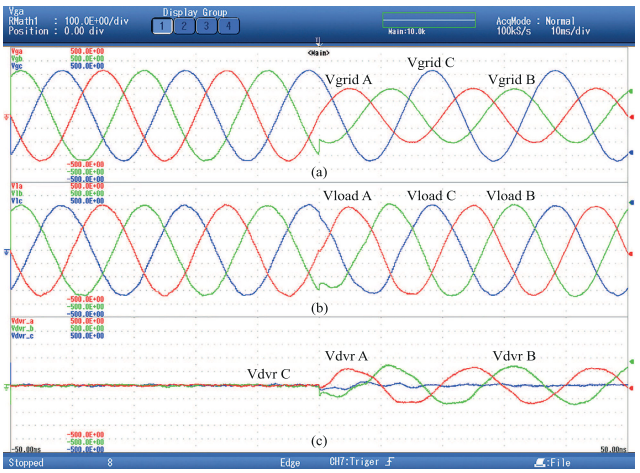

FIGURE 19. Startup transient for a 40% type E unbalanced voltage sag with the proposed control plus a resonant controller and an inductive-resistive load: (a) Grid voltages, (b) load voltages, and (c) voltages injected by the DVR.

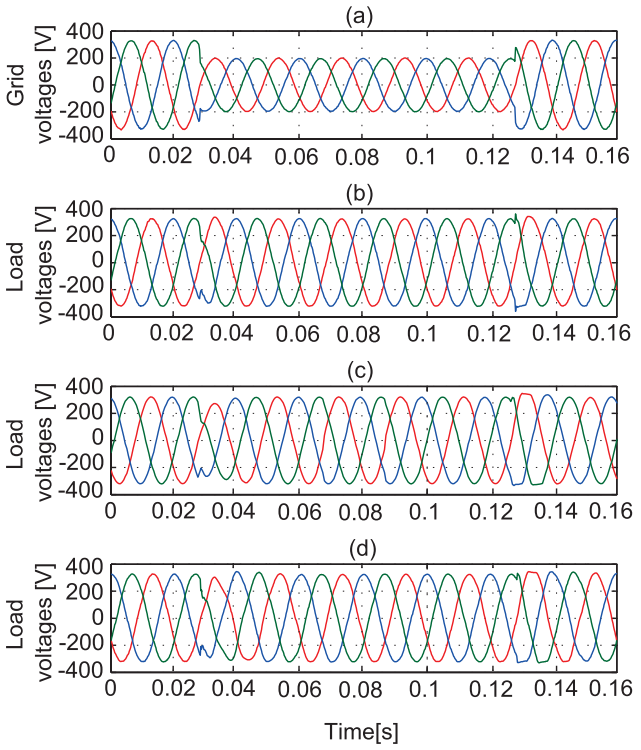

FIGURE 20. Experimental results for a balanced voltage sag with a resistive load: (a) Grid voltages, (b) load voltages with the proposed control, (c) load voltages with the P + Resonant controller, and (d) load voltages with the PID controller.

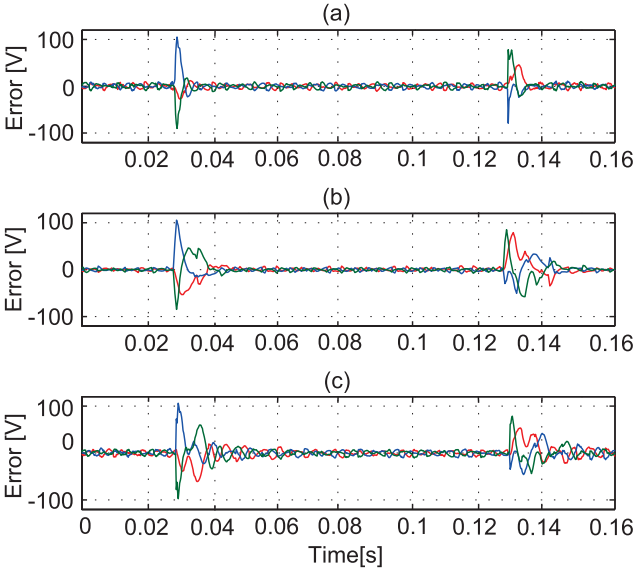

FIGURE 21. Errors in the instantaneous load voltages for a balanced voltage sag with a resistive load: (a) Proposed control, (b) P + Resonant controller, and (c) PID controller.

for the PID regulator-based scheme, and [22], [23] for the P + Resonant controller-based configuration.

The first scenario considers a balanced voltage sag. Fig. 20(a) shows the grid voltages, while Figs. 20(b), 20(c) and 20(d) show the load voltages for the proposed control, the P + Resonant control and the PID control, respectively. The errors in the instantaneous load voltages for the balanced voltage sag with the three control schemes are shown in Fig. 21. As can be seen, the proposed control achieves a

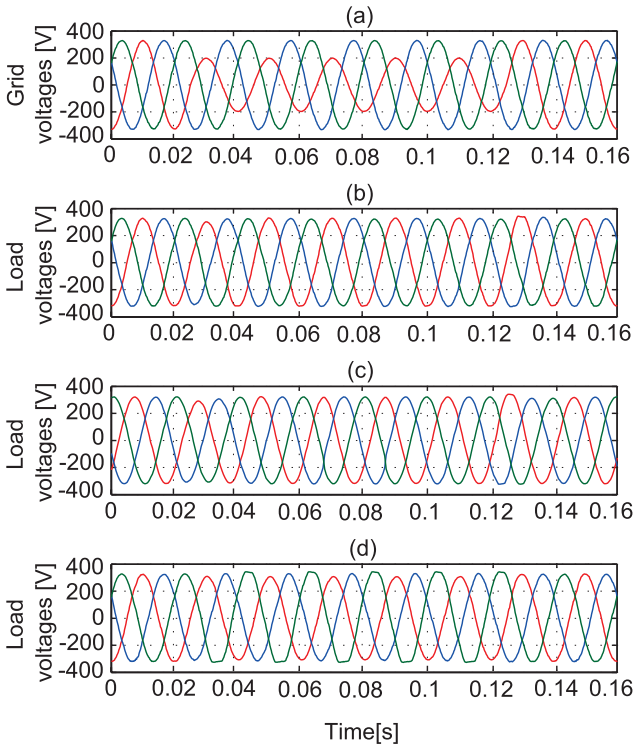

FIGURE 22. Experimental results for an unbalanced voltage sag, type B, with a resistive load: (a) Grid voltages, (b) load voltages with the proposed control, (c) load voltages with the P + Resonant controller, and (d) load voltages with the PID controller.

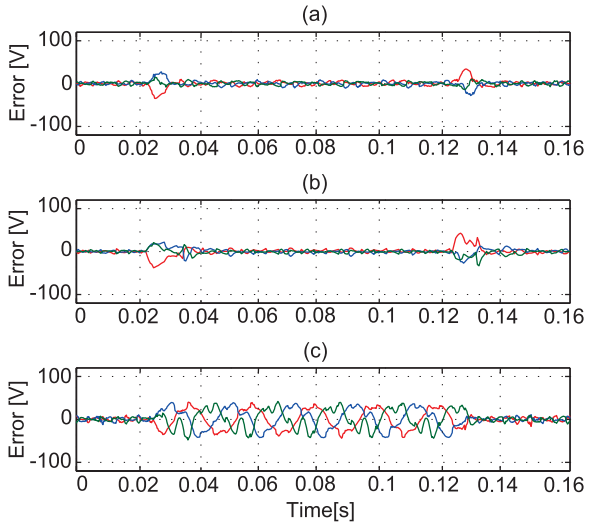

FIGURE 23. Errors in the instantaneous load voltages for an unbalanced voltage sag, type B, with a resistive load: (a) Proposed control, (b) P + Resonant controller, and (c) PID controller.

better performance than the other two schemes, providing a faster transient response and a similar steady-state error. In order to quantify the transient responses, the 2%-settling time has been calculated for the P + Resonant and PID control schemes. The 2%-settling time with the P + Resonant controller is 9.9 ms, whereas the settling time for the PID control scheme is 16.7 ms. These values are 6.1 ms and 12.9 ms slower than those obtained with the proposed control for a balanced voltage sag, i.e., 3.8 ms.

The second test takes an unbalanced type-B voltage sag into consideration. The grid voltages and the load voltages for the three control methods are shown in Fig. 22, while the instantaneous errors in the load voltages are shown in Fig. 23. The dynamic response of the proposed control method is still faster than that obtained with the P + Resonant controller (with a 2%-settling time of 5.4 ms for the proposed controller versus 9.9 ms for the P + Resonant controller), while the PID control method cannot compensate the unbalanced voltage sag, since it is not designed to compensate the 100 Hz component in the SRF.

In both cases the proposed control achieves a superior performance than the other two schemes because the dynamical behavior of the system can be completely defined with the control structure proposed through the two nested regulators.

V. CONCLUSION

This paper presents the design of a discrete-time control scheme for the compensation of balanced and unbalanced voltage sags in a DVR. The scheme is implemented in the SRF and is based on a structure with two nested regulators, in which one of them uses an integral action in order to achieve a zero-tracking error for the fundamental component in the case of balanced voltage sags. The proposed discrete-time control makes it possible to define the dynamical behavior of the system on the basis of selecting the closed-loop transfer function poles. The design methodology achieves the definition of the dynamical behavior with a reduction in the variables to be measured and without the need for state observers. Furthermore, this methodology is independent of the reference frame employed for the implementation of the control system, which makes the control algorithm suitable for use with several operation strategies, and not only with the in-phase compensation. In addition, other advantages of the proposed method are the considerable reduction in the mathematical effort when the multiplicity of the poles is greater than one and the independence of the location of the poles introduced by the implementation of the delay. A simulation with PSCAD/EMTDC corroborates the performance of the proposed control scheme. Furthermore, an extension of this control scheme, in which a resonant controller is added, is provided following the same design methodology for the overall control scheme. The experimental results show that the compensation of both balanced and unbalanced voltage sags is achieved. Moreover, the experimental results show that the performance of the control system when an inductive-resistive load is employed is similar to that obtained when using a pure resistive load. Finally, a comparison with a P + Resonant controller and a PID regulator has been carried out for both balanced and unbalanced voltage sags: The results obtained show a superior performance of the proposed control scheme, when compared to the other two alternatives, for both types of voltage sags.

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