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Highly Reliable and Repeatable Soldering Technique for Assembling Empty Substrate Integrated Waveguide Devices

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***Abstract*—In this paper a novel soldering technique that improves the fabrication process of Empty Substrate Integrated Waveguide (ESIW) devices is presented. Until now, in order to fabricate an ESIW device, the tin solder paste was distributed, before assembling, on the contact surface between layers, in order to ensure a good electrical contact. This process has a low degree of repeatability (random soldering thickness and distribution of tin) and reliability (significant number of non-working prototypes due to tin overflow). In this work, we propose the mechanization of a set of plated vias just next to the metallized walls of the ESIW in the central layer. Next, in the top and bottom covers that close this ESIW, additional plated vias are drilled in the same position, so that, when the device is assembled (using screws or rivets), metallized holes can be seen passing through the whole structure from top to bottom. These holes are then used as soldering vias that can guide the tin paste straight to the point where it is needed. When the paste is dried, soldered vias ensure a very good electrical contact between layers. Besides, the fluid tin fills any small gap that appears between layers, thus providing a very good electrical contact and mechanical union. This novel soldering technique has been validated with experimental results. Several prototypes of filters centered at 13 and 35 GHz have been fabricated, proving the repeatability and reliability of the proposed soldering technique.**

***Index Terms*—Empty Substrate Integrated Waveguide, ESIW, multilayer, fabrication.**

I. Introduction

Empty Substrate Integrated Waveguides [1]–[6] have recently attracted the attention of different researchers all over the world. The reason behind this growing interest is that this novel technology significantly reduces the losses exhibited by traditional Substrate Integrated Waveguide (SIW) circuits [7], preserving, at the same time, their most important benefits, that is, low cost, and the possibility of mass production.

Among all the different proposals of Empty SIWs [1]–[6], the Empty Substrate Integrated Waveguide (ESIW) [2] shows very interesting characteristics. ESIW is completely empty and, as a result, losses are more reduced. ESIW (like Dielectricless SIW of [6]) is closed using continuously metallized walls (not metallic vias). Therefore, it is indeed an actual rectangular waveguide, and the traditional analysis and design methods developed for rectangular waveguides can be directly transferred to ESIW. It can be manufactured using only standard Printed Circuit Board (PCB) manufacturing techniques (like Modified SIW [1] and Air-Filled SIW [3], [4]), so that it is a low cost solution with the possibility of mass production.

One of the most critical issues in the fabrication of these empty SIWs is to find a reliable fabrication technique to ensure a good electric contact between the different PCB layers of the waveguide. In ESIW [2], this good contact was ensured by distributing, before assembling, tin solder paste on the contact surface between each pair of layers. The soldering tin is distributed in both sides of the central layer and then in the bottom of top cover and in the top side of the bottom cover. Then, the final device is totally assembled and the tin is melted by putting the device into a reflow oven. In this way, it is very important that the tin solder paste does not fill the ESIW cavity. So, this is a tedious method and could lead to some device malfunctions if the tin enters the ESIW cavity. Although the process has produced acceptable results to provide the required proof-of-concept of the new technology, it provides a low degree of repeatability (random soldering thickness and distribution of tin) and reliability (significant number of non-working prototypes due to tin overflow). Therefore, in this paper, a novel soldering technique with a very high degree of repeatability and reliability is proposed, which means a very important step forward in the process of transferring this emerging technology from laboratory to industry, transforming this now emerging technology into a future solid alternative for the development of high-quality commercial applications.

This paper is structured as follows: in section II the novel soldering technique is explained. In section III we present the prototypes we have selected to test the new soldering approach. The measurement results of the fabricated prototypes are shown in section IV, and finally the conclusions are outlined in section V.

II. Novel soldering technique

As aforementioned, in this paper a novel reliable and repeatable soldering technique to assemble ESIW devices is proposed. In this technique, plated vias are drilled next to the metallized walls of the ESIW. In the top and bottom metallic covers of the waveguide, corresponding holes are also drilled, and, if necessary (if the covers are not metallic, but are PCB),

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metallized. When the layers are assembled, these metallized vias pass through the whole layer stack (see Fig. 1). From an electromagnetic point of view, these vias have no effect, since they are completely isolated from the waveguide as shown in Fig. 2. They are, in fact, only useful in the soldering stage when they allow the precise distribution of the tin solder paste. The prototype is assembled and fixed before distributing the soldering paste. Then, the soldering paste is forced to pass through the soldering vias, and the excess of paste is removed before soldering (see Fig. 3). When the paste is dried in a reflow oven, the tin ensures a very good contact between the different layers, and fills any possible gap in the structure.

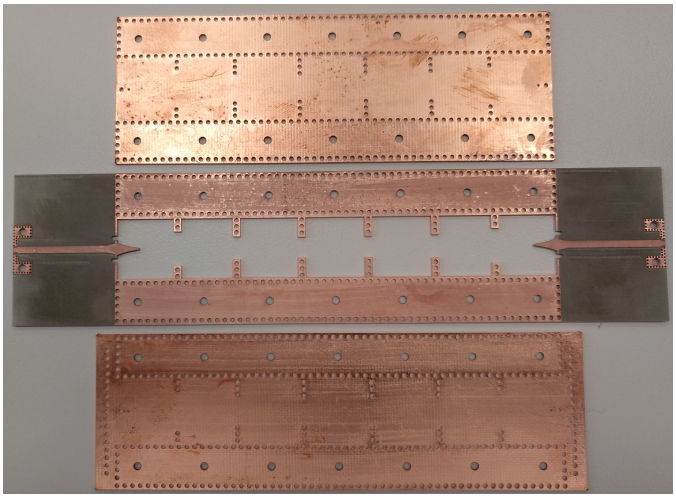

Fig. 1. ESIW filter at 13 GHz. Central layer and top and bottom covers before assembling. The soldering vias are repeated in the top and bottom covers so that, after assembling, metallized holes from top to bottom are formed.

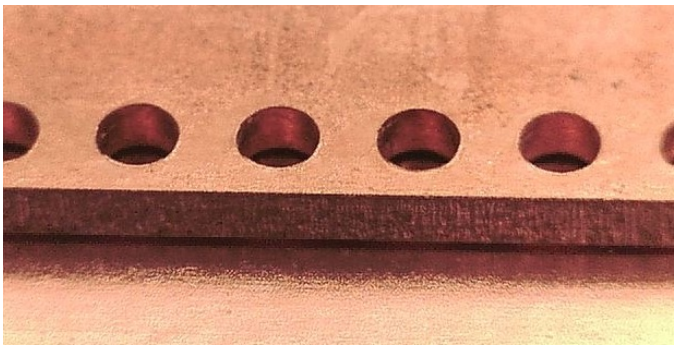

Fig. 2. Detail of soldering vias next to an ESIW metallized wall. The metallized wall isolates the soldering vias from the fields inside the waveguide, so that they are completely irrelevant from the electromagnetic point of view.

Finished prototypes provide excellent results, since the electrical contact is very good. They also show a very good mechanical resistance, because when tin fills the small gaps between layers, it provides a very good union between them. Moreover, with this soldering strategy, the prototypes are very reliable, since the probability that an undesired amount of tin flows inside the waveguide is very low. The tin solder paste is only located in the soldering vias thanks to this new technique. Designing the position of these soldering vias in the desired places of the device, the tin solder paste location is now

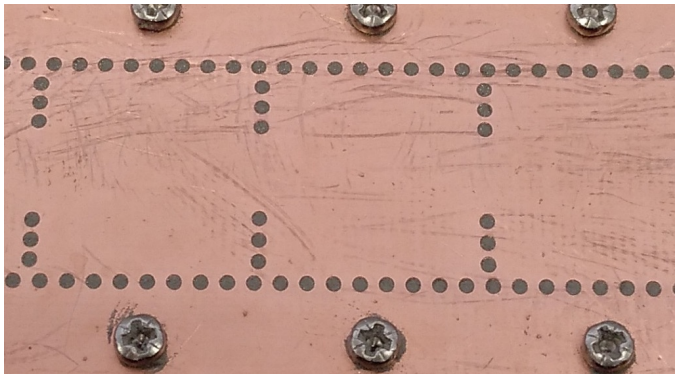

Fig. 3. Soldering vias filled with tin solder paste.

controlled.Besides, due to the fact that the assembling is done before soldering, the uncertainty introduced, in the previous method, by the unpredictable thickness of the soldering layers, is eliminated, and, consequently, results are highly repeatable. Then this new technique could be used for a series production of ESIW circuits. Table I summarize the advantages and disadvantages of soldering vias technique compared with tin solder deposition method.

TABLE I
ADVANTAGES AND DISADVANTAGES OF SOLDERING VIAS TECHNIQUE AND TIN SOLDER DISTRIBUTED BETWEEN LAYERS

Soldering vias technique	
Advantages	Good electrical contact between layers Repeatability (thickness of the soldering layers is eliminated) Reliability (tin that flows inside the waveguide is very low) Allow the precise distribution of the tin solder paste The excess of paste is removed before soldering The fluid tin fills any small gap that appears between layers
Disadvantages	Additional plated vias are drilled
Tin solder distributed between layers	
Advantages	Faster fabrication process, the soldering vias are not drilled Good electrical contact between layers
Disadvantages	Low degree of repeatability (random soldering thickness and distribution of tin) Low degree of reliability (tin overflow) Uncertainty introduced by the unpredictable thickness of the soldering layers

III. PROTOTYPES FOR TESTING

In order to test the novel soldering technique, two different prototypes, which operate at different frequency bands, have been fabricated. Since resonant devices are more sensitive to fabrication problems, bandpass filters have been selected in both cases to evaluate the soldering technique under the most disadvantageous possible conditions. In order to obtain enough information to confirm the reliability and repeatability of this novel soldering technique, several versions of each prototype have been fabricated.

The first prototype is a five-pole standard cavity-coupled Chebyshev H-plane filter, with 0.01 dB ripple in the passband, centered at 13 GHz, and with a 300 MHz bandwidth. The schematic layout of this ESIW filter is shown in Fig. 4, and its final dimensions can be seen in Table II.

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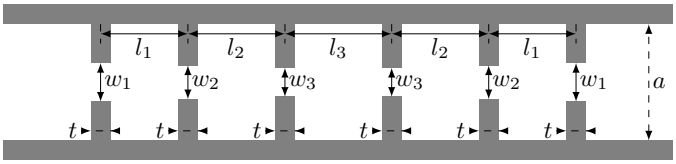

Fig. 4. Layout of the ESIW filters.

TABLE II
DIMENSIONS OF THE ESIW FILTER CENTERED AT 13 GHZ

Parameter	Value (mm)	Parameter	Value (mm)
t	2.0000	w_3	5.4318
a	15.7988	l_1	15.5838
w_1	8.9127	l_2	17.2861
w_2	5.9963	l_3	17.4756

This filter has been fabricated using Rogers 4003C substrate of height $h = 0.813$ mm, permittivity $\epsilon_r = 3.55$, and metal thickness $t = 27$ μm (considering both original and galvanic metallizations). The cover layers have been fabricated using FR-4 substrate of $h = 0.8$ mm height.

In order to feed this filter with planar lines, the transition of section III of [8] has been used. The simulated results for this filter, including the transitions to microstrip feeding lines, can be seen in Fig. 5.

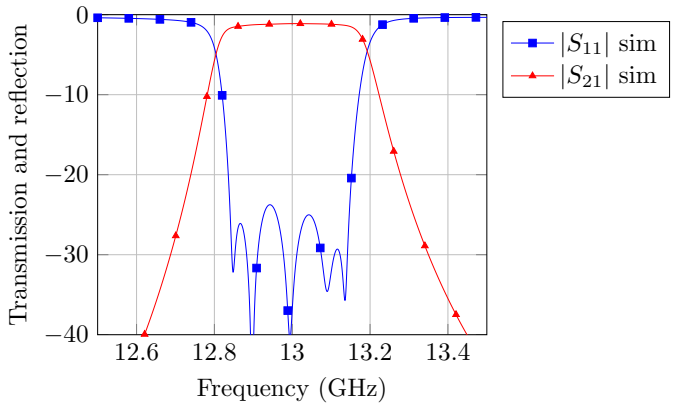

Fig. 5. Simulated results for the first prototype (filter at 13 GHz).

The simulated insertion loss of one of the feeding microstrip-to-ESIW transitions is 0.146 dB. Therefore, once the loss of both transitions have been discounted from simulations, the insertion loss of this filter is $IL = 0.828$ dB and, as a result, it shows an unloaded quality factor $Q_u = 1323$. In order to calculate this value, we have applied the following expression [9]:

$$Q_u = 4.343 \sum_{i=1}^{N} \frac{\Omega_C}{F_B \Delta L_{A0}} g_i \ \text{dB} \qquad (1)$$

where Ω_C is the normalized cut-off angular frequency of the lowpass filter prototype, g_i are its coefficients, N its order, F_B the fractional bandwidth of the passband filter, and ΔL_{A0} is equal to the insertion loss of the real passband filter minus the insertion loss of the ideal passband filter prototype at the central frequency. In this case, $\Omega_C = 1$, $g_1 = 0.7563$, $g_2 = 1.3049$, $g_3 = 1.5773$, $g_4 = g_2$, $g_5 = g_1$, $N = 5$, $F_B = 2.31\%$, and $\Delta L_{A0} = 0.828$ dB.

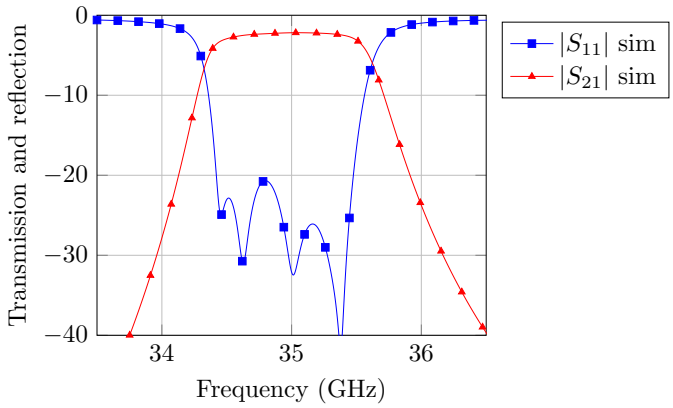

Fig. 6. Simulated results for the second prototype (filter at 35 GHz).

The second prototype is also a five-pole standard cavity-coupled Chebyshev H-plane filter. Therefore, the same schematic layout can be used for this second device (see Fig. 4). This Chebyshev filter shows a ripple of 0.01 dB, it is centered at 35 GHz, and provides 1 GHz bandwidth. Its final dimensions can be seen in Table III.

TABLE III
DIMENSIONS OF THE ESIW FILTER CENTERED AT 35 GHZ

Parameter	Value (mm)	Parameter	Value (mm)
t	2.0000	w_3	2.7650
a	7.1120	l_1	5.6749
w_1	4.0028	l_2	6.4056
w_2	2.9792	l_3	6.4981

The second prototype has been fabricated using also a Rogers 4003C substrate with the same metallization ($t = 27$ μm), but, in this case, of height $h = 0.305$ mm. The substrate employed to implement the covers is again FR-4, but, in this case, $h = 1$ mm.

In this case, in order to feed this filter with microstrip lines, we have used the first part of the transition of [10] (see Table I in section II). The simulated results, including again this microstrip-to-ESIW transition, can be seen in Fig. 6.

For this filter we have considered the effect of copper roughness. This effect is almost negligible at 13 GHz, and that is the reason why we have not considered this fact in the previous simulated results. In this case, though, we have measured, with a Mitutoyo SJ-410, the surface roughness of the FR-4 material we have used to build the covers, and we have inferred the equivalent conductivity of this rough copper at 35 GHz. Given that the root mean square (RMS) of the surface roughness of the material of the covers is equal to 0.42 μm, the conductivity of copper is reduced from $5.8 \cdot 10^7$ S/m to $2.0 \cdot 10^7$ S/m (see [11] for more information about this calculation). Then, we have simulated the prototype at 35 GHz using a metallic material with this reduced conductivity, instead of using the typical conductivity of copper. Using this copper with reduced conductivity, the insertion loss of a single microstrip-to-ESIW transition is 0.28

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dB, and the insertion loss of the filter (without transitions) is $IL = 1.63$ dB. Then, the unloaded quality factor of this filter is $Q_u = 543$. In order to calculate this value, we have applied, again, equation (1). In this case, since this second filter is of the same kind, order, and ripple as the filter of 13 GHz, the same Ω_C, g_i, and N must be used. On the other hand, for this filter, $F_B = 2.86\%$, and $\Delta L_{A0} = 1.63$ dB.

IV. Results

A. ESIW filter at 13 GHz

For the first test with the filter centered at 13 GHz, we have fabricated 4 prototypes using the novel soldering technique. We have also fabricated 4 filters using the former soldering technique (see section I), so that we could have a reference to compare the results of the new technique. Fig. 7 shows the complete set of fabricated filters.

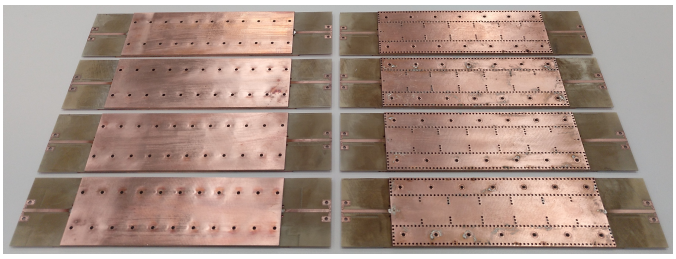

Fig. 7. Manufactured ESIW filters at 13 GHz, with soldering vias (right side) and without soldering vias (left side).

The fabricated prototypes have been measured with a vector network analyzer (VNA). K connectors have been used to attach the filter to the VNA, but they have been de-embedded from measurements using a custom microstrip calibration kit (see Fig. 8).

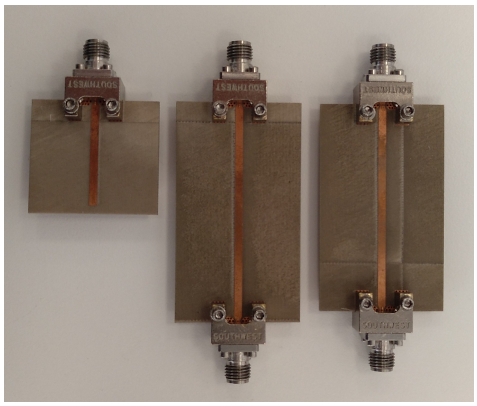

Fig. 8. Calibration kit used to de-embed connectors from measurements at Ku band.

Fig. 9 shows the mean of the measured prototypes, and, shaded in grey, it has been marked the region of minimum area which contains the response of all the measured prototypes, or, in other words, for a given parameter at a given frequency, the region in grey ranges from the minimum to the maximum measured value for this parameter.

It can be seen that all the manufactured filters with soldering vias work properly, so that we can say that the technique

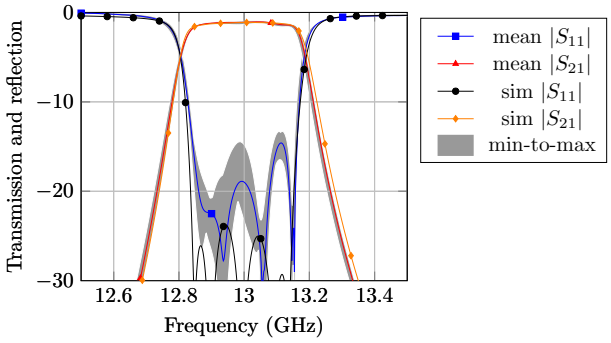

Fig. 9. Measured results of the fabricated ESIW filters 13 GHz with soldering vias. Mean values and maximum measured range of variation.

is highly reliable. Moreover, they provide a very stable response. It is so stable that the grey region, which graphically illustrates the variability of the measured responses, is almost indistinguishable for the S_{21} parameter. Only in the passband, and for S_{11}, there is a region where we can see a noticeable variability in the measured responses. This happens because return loss in the passband is the most sensitive parameter in a filter response. Anyhow, all the measured responses provide acceptable values of return loss. Therefore, we can also say that the soldering technique shows a high degree of repeatability.

Only one of the four prototypes assembled without soldering vias has provided acceptable results. However, even this prototype shows a notable drift in frequency and an important increase of insertion loss. The measured results for this filter are shown in Fig. 10

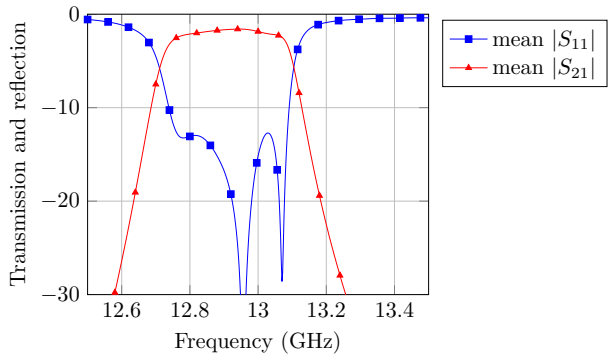

Fig. 10. Measured results of the only working prototype at 13 GHz manufactured without soldering vias.

To calculate the measured unloaded quality factor for these filters, we can use the same procedure we used before with simulations in section III. The only term that is different in the real case is the measured insertion loss at the central frequency. Each prototype presents a slight different value of insertion loss. Then, we have computed the mean quality factor for this set of identical filters, $\hat{Q}_u = 1402$, and the maximum and minimum quality factor achieved, $Q_{u,max} = 1676$, and $Q_{u,min} = 1043$. We can see that these values are very close to what was predicted by simulations. Therefore, we must conclude that the new soldering strategy provides an excellent

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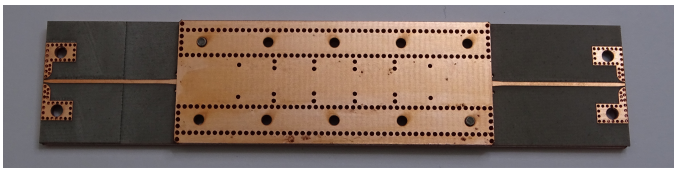
electric contact, very close to the ideal contact assumed in simulation. The high-performance exhibited by these prototypes, assembled with the novel soldering technique, becomes even more significant if their results are compared with the results provided by the only functional prototype assembled without soldering vias. The prototype fabricated using the former assembling approach shows an important drift in frequency (100 MHz), and a strong increase of insertion loss ($Q_u = 796$).

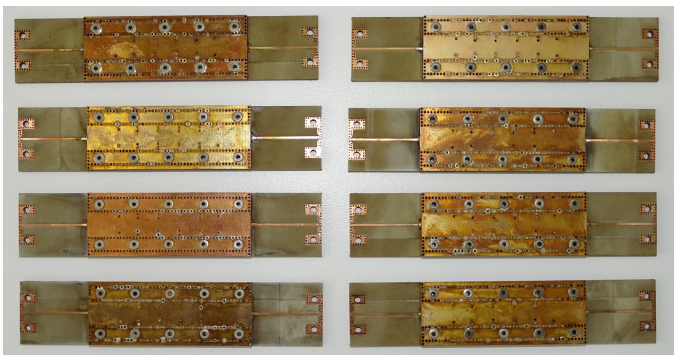
B. ESIW filter at 35 GHz

The filter at Ka band is the second test we have prepared for this novel soldering technique of ESIW devices. As frequency increases, the manufacturing defects affect more strongly the response of real devices, and this is the reason why we have decided to manufacture a set of prototypes centered at 35 GHz.

We have indeed manufactured 8 different prototypes of the second filter of section III. A detailed photograph of one of this prototypes can be seen in Fig. 11(a). A photograph of all the manufactured prototypes is shown in Fig. 11(b).



(a) Manufactured ESIW filter at 35 GHz before the tin application.



(b) Set of the 8 manufactured ESIW filter at 35 GHz.

Fig. 11. Manufactured ESIW filters.

As in the case of the Ku filters, these prototypes have been measured with the VNA, and, again, K coaxial connectors have been used to connect them to the VNA. In order to de-embed the connectors from measurements, another custom calibration kit has been fabricated (see Fig. 12). The mean response of all these prototypes has been calculated and represented in Fig. 13. As we did for the other set of prototypes, we have represented in grey, in this same figure, the region of minimum area that contains all the measured responses.

In this second, and more demanding test, all the fabricated prototypes provide acceptable results. The results are very similar, but, since the frequency is higher, one can observe more variability than in results at Ku band (compare grey areas of Fig. 9 and Fig. 13). We can conclude that, this new soldering technique is able to provide repeatable and reliable results also at Ka band.

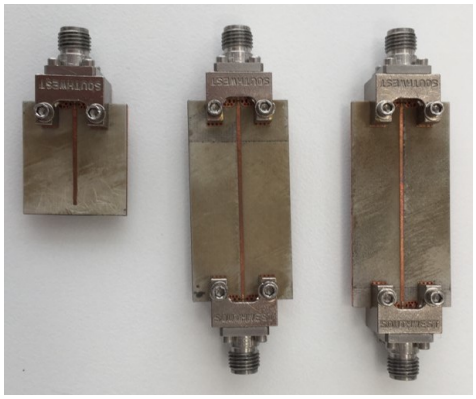


Fig. 12. Calibration kit used to de-embed connectors from measurements at Ka band.

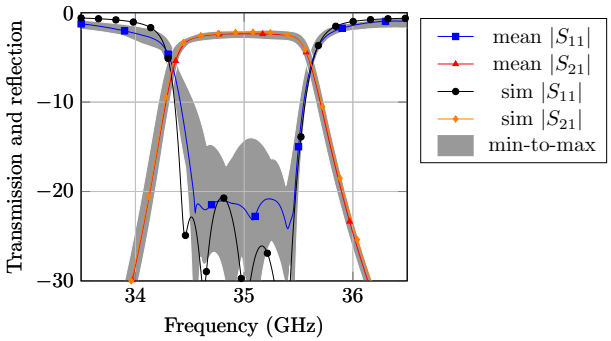


Fig. 13. Measured results of the fabricated ESIW filters at 35 GHz. Mean values and maximum measured range of variation.

For this set of filters we have calculated also the mean, maximum and minimum measured quality factor, $\hat{Q}_u = 500$, $Q_{u,max} = 604$, and $Q_{min} = 379$. In this case, we have obtained again measured quality factors that are very close to the value predicted by simulations. Therefore, we must conclude, also at Ka band, that this soldering technique is able to provide an excellent contact between covers and the central layer in ESIW devices. A very good electric contact is achieved.

V. Conclusion

A new fabrication technique to enhance the soldering process for ESIW devices has been presented in this paper. It is an easy and robust method to achieve very good contact and mechanical resistance between layers in a finished ESIW device. The soldering, with the new procedure presented in this paper, is achieved using metallized vias that pass through the whole layer stack. These soldering vias guide the tin paste straight to the point where it is needed. Therefore, in addition to better repeatability and reliability than with the former technique, less amount of tin is needed to obtain a good welded device.

In order to test the proposed soldering technique two sets of prototypes have been fabricated: a set of identical filters centered at 13 GHz, and a set of filters at 35 GHz. All the devices that have been fabricated with the novel soldering technique exhibit very good performance levels. Both results,

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at 13 and 35 GHz, show great stability and repeatability, thus confirming the desired repeatability and reliability of the developed soldering technique. In the case of the 13 GHz filters, an additional set of filters assembled with the former soldering technique have been fabricated. The comparison of the results of the former and novel soldering techniques demonstrates that the novel technique shows much superior performance. This novel fabrication technique can be seen as a very important step to transform ESIW technology into a good alternative to develop high quality devices in the industrial sector. Mass production is possible thanks to its great repeatability.

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