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Miniaturization of Power Divider and 90° Hybrid Directional Coupler for C-band Applications using Empty Substrate Integrated Coaxial Lines

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***Abstract*—This work presents the practical realization of a power divider and a 90° hybrid directional coupler in Empty Substrate Integrated Coaxial Line (ESICL) for C-band frequency applications. This new type of transmission line is very promising in terms of electric performance, bandwidth, integration with other planar circuits and manufacturing simplicity. The ESICL has been designed for obtaining a wide monomode bandwidth with a characteristic impedance of 50 ohms. Furthermore, an improvement of the efficient transition between the ESICL and the Grounded Coplanar Waveguide (GCPW), used as feeding line, has been also proposed. The passive devices built using this technology are reduced in mass and volume, keeping robustness and providing a well balanced power division, as well as reduced losses and high isolation in the whole operational bandwidth. Two prototypes have been manufactured and the experimental results are in good agreement with the simulated designs.**

***Index Terms*—C-band, empty substrate integrated coaxial line (ESICL), ESICL broadband transition, power divider, hybrid directional coupler.**

I. Introduction

THE practical development of passive devices operating at increasingly higher microwave frequencies is one of the current trends of RF communications industry. This interest responds to the use of these frequency bands to cope with the availability of bigger bandwidth that new communication applications demand [1], [2]. Nevertheless, this effort should not neglect the improvement of already existing passive devices operating at lower frequency bands in terms of efficiency, performance, volume or weight [3]. Otherwise, there is the risk to have high technology systems at higher frequencies, while using 20th century technology at the primitive microwave bands.

C-band, nominally compromising a frequency range between 4 GHz and 8 GHz, has been quite popular for satellite communications in the past, but is giving way to higher frequency bands for remote sensing, commercial or defense purposes in space communication systems [4], [5]. Nevertheless, C-band is still in use for several practical applications, specially those requiring high power, and is becoming widely used in nano- or pico-satellites [6], [7] for specific purposes. Furthermore, the availability of non assigned parts of the C-band spectrum has made it an ideal candidate for future 5G cellular communications [8].

C-band devices for high power applications are usually developed on waveguide technology, which is reliable and robust, but also expensive and difficult to integrate with other technologies. Moreover, when using waveguide technology, the lower the frequency, the bigger size of the device is, which leads to high volume and weight devices (as it usually happens with C-band applications). Cellular communications require an extensive infrastructure of base stations and RF links. This infrastructure is only affordable if the components of the communication systems are well integrated and inexpensive. Furthermore nano- or pico-satellites are small by definition, and their payload must be optimized in terms of volume and weight, but still the communication systems needs to be reliable and robust. Planar technologies, like microstrip, coplanar or stripline, provide small components and easy integration, but their electrical performance is not still enough (e.g. with regard to related insertion losses and high power handling).

This work proposes the use of a new Substrate Integrated Circuit (SIC) concept [9], i.e. the Empty Substrate Integrated Coaxial Line (ESICL) [10] for the development of passive microwave devices to operate at C-band frequencies. ESICL is seamless and can be easily integrated in planar circuits, throughout transitions with coplanar or microstip lines. Furthermore, it can be implemented with low-cost standard manufacturing procedures and it is rather tolerant to manufacturing defects. All of this makes ESICL an ideal candidate for mass production and fast prototyping. The resulting devices are of reduced weight and volume, but robust, whilst providing a reliable and efficient frequency response (with low insertion loss) in the operational bandwidth. Moreover ESICL presents wide mono-mode bandwidth, since the dominant mode is TEM and the frequency of the second upper mode can be optimized in the design process [11]. This promising technology could even be used in a reconfigurable scheme, since the coaxial line has two conductors, on which a DC bias voltage can be

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applied. For reconfiguration purposes lumped elements [12], [13] or anisotropic materials [14], [15] are used.

II. The Empty Substrate Integrated Coaxial Line

Over the past few years, the number of substrate integrated circuits and substrate integrated lines has not stopped growing. Since the first works on this field that introduce the idea of a Substrate Integrated Waveguide (SIW) [16], a significant effort has been invested on the development of new integrated waveguides, such as the Substrate Integrated Coaxial Line (SICL) [17].

On the one hand, SIW is a traditional rectangular waveguide manufactured on a Printed Circuit Board (PCB). It uses two side rows of metallic via holes, and the top and bottom metallic sheets of the dielectric substrate to obtain an equivalent rectangular waveguide with excellent propagation characteristics.

On the other hand, SICL is a coaxial line manufactured on a stack of two PCBs. In order to build the ground conductor it uses two side rows of metallic via holes in each layer, and the top of the up cover and the bottom of the down cover.

The aim of these technologies is to achieve a hybrid transmission line between traditional waveguides and planar transmission circuits, in other words, the goal is to get a new transmission line technology with the best possible electromagnetic characteristics, lower manufacturing costs, easy to integrate and allowing mass production. However, SIW and SICL technologies are made on dielectric substrates which implies an increase of related transmission losses. Therefore, empty versions of these two transmission media have been developed, ESIW [18] and ESICL [10].

ESICL is an empty squared coaxial line integrated in a stack of three layers of PCBs, plus two covers, as can be seen in Fig. 1. It is a non-dispersive transmission line with high monomode bandwidth and very low radiation and transmission losses. All these features make this technology specially promising for many RF and microwave applications.

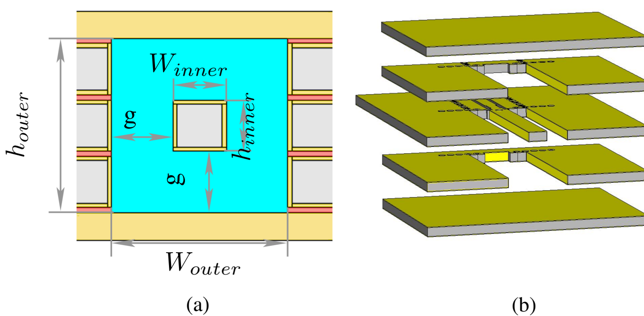

Fig. 1. (a) ESICL stack structure. Light gray is the dielectric substrate, blue is the empty gap, yellow is copper and orange is welding layer (if needed), (b) Detail of the multilayered structure.

The ESICL structure can be easily manufactured by commercial milling techniques used with planar lines (see Fig. 1 and Fig. 2). The layers, numbered from bottom to top, build the two conductors by cutting and stacking the substrates. Layers number 2 and 4 build the vertical separation between the inner and outer conductor, while the two side cuts of layers 2, 3 and 4 build the horizontal separation. The cost of manufacturing this structure is around 3 times the cost of manufacturing a conventional planar structure, since it has 3 layers to be processed. Plating of the side walls is the same galvanic metallizing process that it is used to metallize via holes of any PCB.

Furthermore, the design of different devices in this technology is specially easy, since the structure is simple and presents a pure TEM mode that enables the analysis and design based on classical transmission lines theory [19]. Moreover, this mode has surface electrical currents parallel to the propagation direction, this is the longitudinal axis direction. Therefore, the stack of layers does not cut the electrical current, and the assembling process does not need a welding stage.

A. Design of the ESICL

The main objective of this work is the practical development of two passive devices in ESICL technology: a power divider and a hybrid directional coupler. Therefore, it is important to have an ESICL with a specific characteristic impedance and monomode operation in a bandwidth as wide as possible.

For the TEM mode, the simple (and well-known) transmission line model can be applied for designing the characteristic impedance of both, the ESICL and the integrated devices built with this technology. Omitting the losses in the theoretical model, the problem of designing an ESICL with a specific characteristic impedance is reduced to the calculation of the structure capacitance, as can be seen next:

$$Z_0 = \sqrt{\frac{L}{C}} = \frac{1}{vC} = \frac{\sqrt{\mu\varepsilon}}{C} \quad (1)$$

In order to ease the evaluation of the requested line capacitance, the ESICL can be divided into 8 different sections (see Fig. 2). As a result, the total capacitance would be the sum of each portion [20]. Consequently, the characteristic impedance can be calculated as follows:

$$Z_0 = \frac{\sqrt{\mu\varepsilon}}{2\varepsilon[\frac{w+b}{g} + \frac{2}{\pi}(\log_{10}(\frac{1}{2}) + \frac{\pi}{2})]} \quad (2)$$

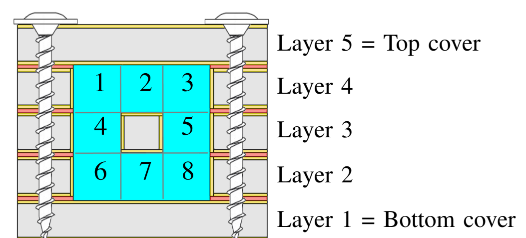

Fig. 2. ESICL is divided into 8 parts in order to calculate its capacitance. Light gray is the dielectric substrate, blue is the empty gap, yellow is copper and orange is welding layer (if needed).

This result is valid for obtaining the characteristic impedance of the TEM mode of an ESICL with the inner conductor centered in both vertical and horizontal dimensions, and homogeneously spaced from the outer conductor.

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It must be noticed that there is a wide combination of variables to achieve an ESICL with a specific value for the characteristic impedance. For this reason, the chosen dimensions must not only satisfy such a requirement, but also provide a wide monomode bandwidth. With this aim in mind, a modal study has been carried out through a commercial full-wave electromagnetic simulator, CST [1]. After performing this study, it is concluded that the more squared the ESICL cross section is, the broader the monomode operational bandwidth will be. As a result, the dimensions of the objective ESICL are shown in Table I. For comparison, a previous ESICL design in [10] has been included. As it can be seen, the dimensions of the variables are different, providing a more squared topology for the ESICL. This new design is also able to provide (keeping the same characteristic impedance value) a much wider bandwidth, as can be seen in Table II.

TABLE I
DIMENSIONS FOR THE ESICL.

Parameter	Designed ESICL (mm)	ESICL in [10] (mm)
W_{inner}	0.960	1.917
H_{inner}	0.584	0.933
W_{outer}	2.124	6.000
H_{outer}	1.748	2.733

TABLE II
CUTOFF FREQUENCIES OF THE ESICL MODES.

Mode	Cutoff Frequency of designed ESICL (GHz)	Cutoff Frequency of ESICL in [10] (GHz)
TEM mode	0	0
2nd mode (TE)	58.9	21.5
3th mode (TE)	61.9	39.1
4th mode (TE)	105.9	51.2

For implementing the designed ESICL, a Rogers 4003C ($\varepsilon_r = 3.38 \pm 0.05$) substrate has been chosen. The thickness of this substrate for layer 3 is 0.508 mm and 0.406 mm for layers 2 and 4. Moreover, these layers have their own copper shield, and during the manufacturing process they have been additionally metallized, resulting a final metallization of 40 μm on both sides.

B. Integration with Planar Technology

The overriding objective of SIC lines is to achieve a seamless integrated system with other popular planar technologies. For this purpose, a simple transition from a Grounded Coplanar Waveguide (GCPW) to ESICL has been designed.

Previous designs of this transition use a three stage model [10], but the present ESICL dimensions do not allow it due to mechanical weaknesses. Therefore, it has been decided to use a four stage transition model, as depicted in Fig. 3 and Fig. 4.

1) GCPW: as in the previous works, this is the first stage made of a simply GCPW located on the third layer (see Fig. 4).
2) SICL: the second stage is a typical SICL craved on two layers (third and fourth). The resulting line has also been named covered GCPW in some works, since it is a GCPW covered with a PCB substrate with a top metallic sheet. This transmission line is encapsulated with side metallic via holes, thus enclosing the GCPW within a metallic housing.
3) Housed strip line: the third stage is an encapsulated strip line built with the layers 2, 3 and 4 and the two covers of the stack. The layer number 3 (top view in Fig. 4) builds the active strip that connects the active conductors of the previous and next stage. In this layer, the ground conductor of the bottom side is erased in order to adapt

[1]CST Studio Suite, v2014.02

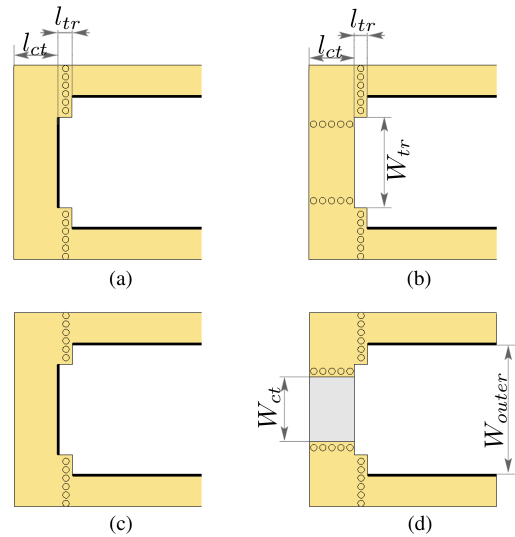

Fig. 3. GCPW to ESICL 4 stages transition: (a) Top view of layer 2, (b) Top view of layer 4, (c) Bottom view of layer 2, (d) Bottom view of layer 4. Light gray is the dielectric substrate, yellow is copper and solid black line are metallized walls.

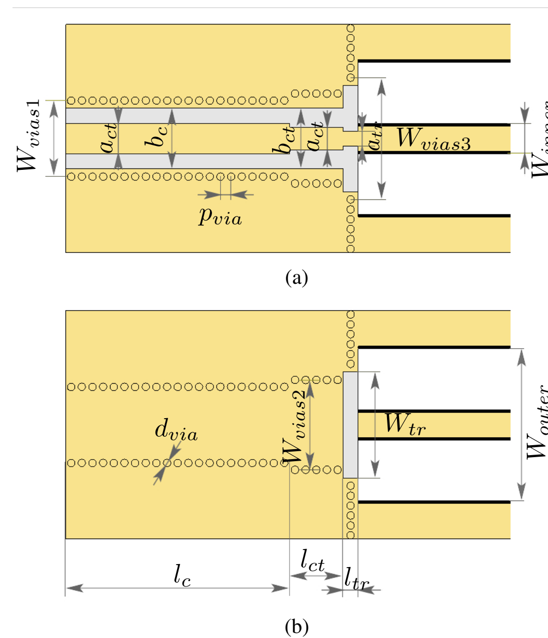

Fig. 4. GCPW to ESICL 4 stages transition: (a) Top view of layer 3, (b) Bottom view of layer 3. Light gray is the dielectric substrate, yellow is copper and solid black line are metallized walls.

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the SICL to the ESICL, see Fig. 4. In contrast to the previous three stages transition in [10], this new one does not have any cut in the layer 3, so that, its mechanical strength is increased. The additional mechanical strength this stage provides is required when the layer 3 of the line is very thin, as in this case. This strip is housed through the side rows of metallic via holes built on layers 2 to 4, see Fig. 3 and Fig. 4, and are covered by the metallic sheets of the layers 1 and 5. Layers 2 and 4 are empty to obtain a low effective dielectric permittivity, assuring to achieve an active strip as wide as possible.

4) ESICL: this is the final stage of the transition, which conforms the final objective line.

For implementing this four stage transition from a GCPW to the previously designed ESICL, the usual design steps have been followed. First of all, the GCPW, SICL and ESICL lines have been theoretically designed to get a characteristic impedance of 50 Ω. Next, these theoretical dimensions have been tuned with commercial software (CST) in order to achieve an impedance value as constant as possible over the selected bandwidth (from 0 to 20 GHz, the limiting monomode frequency for the GCPW line). Finally, the length and width of the housed strip line and the separation of the side via holes, have also been optimized in order to maximize the return loss of the total structure. The simulated and measured responses of the final back to back structure (Fig. 5) are depicted in Fig. 6, and the final optimized dimensions can be found in Table III. The cross section of this line and transition will no change for the design of any device working at any frequency up to 20 GHz, no matter of its operational bandwidth. This is an important enhancement in comparison to other transmission lines that need to be re-designed specifically for each operating frequency band.

The manufactured ESICL has a good response even with transitions. The connectors effect has been removed in both simulated and measured data.

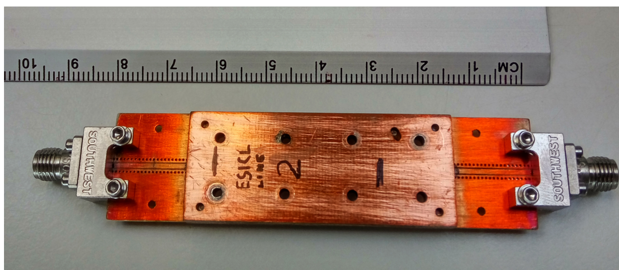

Fig. 5. Manufactured prototype of the back-to-back transition to ESICL.

Another issue to be considered is power handling. In a transmission line, it is traditionally addressed considering two different aspects: peak power and Continuous Wave (CW) power. For the first one, the breakdown value of electric field in the medium is normally used for the calculation of the peak power that the line can handle. The value of this field in dry air varies depending on the consulted sources from 10^6 V/m to $3{\cdot}10^6$ V/m. In average, for a C-band waveguide it gives theoretical values around 2,500 kW. The same calculation

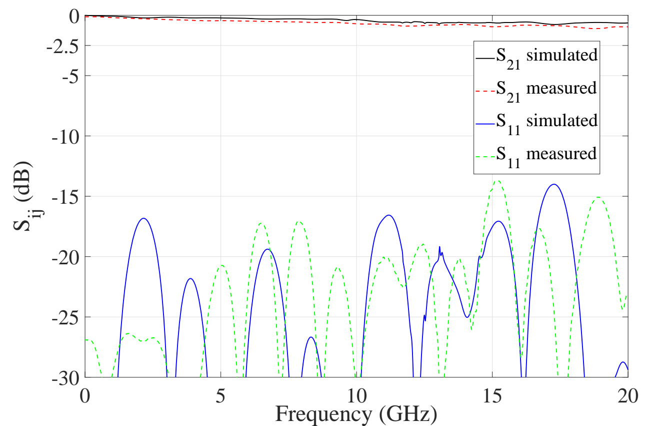

Fig. 6. Simulated and measured S parameters of the designed 4-stage transition between GCPW and ESICL.

TABLE III
DIMENSIONS FOR THE DESIGNED FOUR STAGE TRANSITION.

Parameter	Measure (mm)	Parameter	Measure (mm)
a_c	0.84	b_c	1.34
L_c	14.7	L_{ct}	3.5
a_{ct}	0.57	b_{ct}	1.34
W_{vias1}	2.34	W_{vias2}	3.24
W_{ct}	2.34	d_{via}	0.5
a_{tr}	0.92	W_{tr}	1.46
W_{vias3}	2.46	p_{via}	0.7
L_{tr}	1		

for the designed C-band ESICL gives values around 20 kW. Similar or even higher results can be obtained for microstrip or CPW depending on the type and height of employed dielectric substrate. Concerning CW power handling the results use to be empiric, and they depend very much of the shape and material of the waveguide. For C-band waveguides typical values are 10 kW to 15 kW. Obviously, the CW power handling of ESICL has not been studied so much up to now, but empty coaxial lines of similar sizes can handle up to 100 W, whilst microstrip lines can handle around 15 W of CW power [21].

As a proof of concept of ESICL technology, a power divider and a hybrid directional coupler operating at 5 GHz have been designed. Since the aim of this work is the miniaturization of C-band devices for high performance applications, these designs will enlighten the reduction in size and volume that this technology means in front of alternative waveguide solutions.

III. POWER DIVIDER

As already mentioned before, the first of the two manufactured prototypes is a power divider, based on a T-junction, operating at the working frequency of 5 GHz. This device consists of a passive, reciprocal and ideally loss-less network of 3 ports (with 50 Ω characteristic impedance) with a matched input port and two output ports (see Fig. 7), for which the input signal is equally distributed without introducing any phase shift [19]. The impedance matching in the input port is achieved by a $50/\sqrt{2}$ Ω characteristic impedance matching line with a length of $\lambda/4$ at the design frequency. When designing this device, the characteristic impedance is modelled

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by the width of the active strip of the ESICL, so it has been necessary to design a transition between the two lines of different characteristic impedance. This transition consists of a linear variation ($\alpha = 27°$ slope) from the strip width of the transmission line with a characteristic impedance of 50 Ω to the lines with a value of $50/\sqrt{2}$ Ω for the corresponding characteristic impedance, as can be seen in Fig. 7.

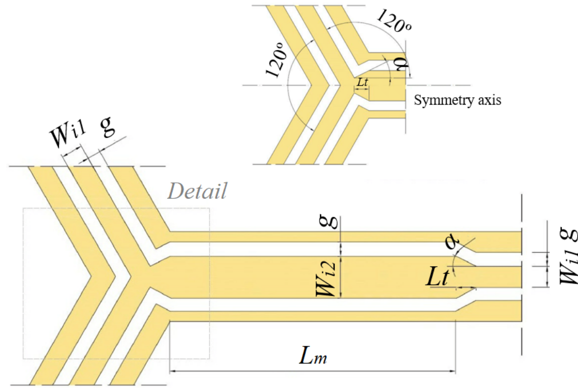

Fig. 7. Top view and detail of the layer 3 of the designed power divider.

Another aspect to take into account is the problem of reflection loss caused by the abrupt junction of the three arms of the classical T-junction device (90° between input and outputs). For this reason, it has been chosen to join the ports by forming an equilateral triangle, so that the arms have an angular separation of 120° and visually adopt a Y-shape, as can be seen in Fig. 7.

The most relevant factor in this design is the matching line, so its length has been optimized to get a good matching level at the frequency of 5 GHz. In this way, the aforementioned length becomes 12.57 mm, somewhat less than the 15 mm ($\lambda/4$) pointed by the theory. This is because the theoretical model assumes a non-gradual transition between lines of different characteristic impedance but, in practice, a gradual transition is required in order to optimize the design, so that the lengths of the transitions impact on the optimal value for the length of the matching line.

TABLE IV
DIMENSIONS OF THE POWER DIVIDER.

Parameter	Measure (mm)
W_{i1}	0.96
W_{i2}	1.88
g	0.60
L_m	12.57
L_t	0.925

In the manufacturing process, the same substrates and techniques used in the ESICL have been employed again. The final optimized dimensions of the structure are specified in Table IV. The assembling of the different layers has been made using screws, as can be seen in Fig. 8 (b) and, finally, three SMA connectors have been soldered to the entrance of the ports (see Fig. 8 (c)).

Once manufactured, the frequency response of the power divider has been measured using a previously calibrated vector

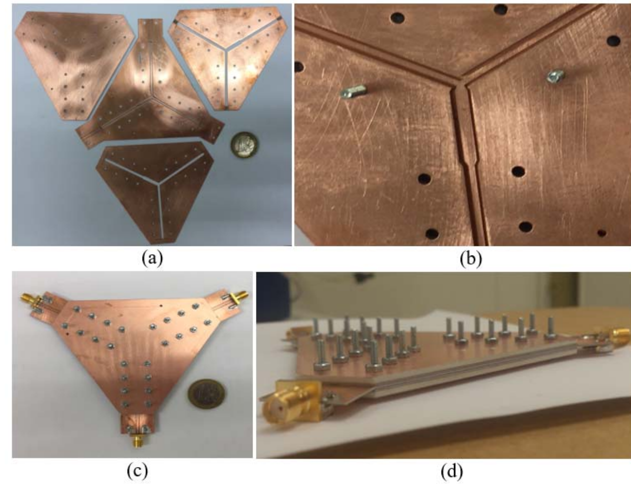

Fig. 8. (a) View of the power divider layers. (b) Top view of the assembled divider, layers 1 to 4. (c) Top view of the finally assembled device. (d) Detail of the layer stack thickness.

network analyzer. Fig. 9 shows the comparison of the measured parameters of the manufactured device with its simulated data. It is important to point out that the presence of both the transitions to the coplanar lines and the connectors have already been taken into account.

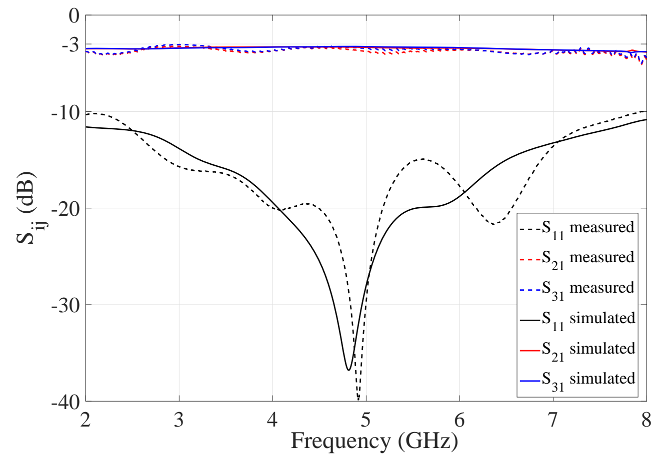

Fig. 9. Measured vs. simulated results of the most significant scattering parameters of the designed power divider.

As can be seen, the matching of the input port, as well as the power division, occur optimally. Indeed, after modelling the effect of the transitions and connectors, the electrical response is shifted to lower frequencies (4.8 GHz) in the simulation and, after measuring the device, it can be observed that finally, the matching appears at 4.92 GHz. In contrast, the relative bandwidth has been decreased from 65% to 54.8% for a return loss value greater than 15 dB. Moreover, there is an equitable power division between the output arms, since S_{21} and S_{31} are -3.4 dB ± 0.3 dB and -3.5 dB ± 0.5 dB respectively.

For high performance applications waveguide technology is commonly used, so this is the technology that must be taken into account for a fair comparison. Table V shows the results for an ESICL power divider and a typical commercial

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TABLE V
COMPARISON OF THE POWER DIVIDER.

Parameter	ESICL	Waveguide
Dimensions (mm^3)	40x29x4.8	95.3x127x88.9
Weight (g)	77.67	400
Bandwidth (return loss $>$ 15 dB) (%)	54.8	38
Insertion loss (dB)	0.3	0.09
Unbalance (dB)	$\pm$ 0.35	$\pm$ 0.25

device based on a waveguide T-junction (187 WG Tee-E of AINFO Inc.). Since the results of the waveguide power divider do not consider losses due to connectors or transitions to other technologies, for ESICL power divider the effect of the connectors (0.2 dB at 5 GHz) has also been removed in the included information about insertion loss. These results make the ESICL topology device versatile and suitable for applications that require small and light devices with a good electrical response (i.e. payloads of pico- and nano-satelllites).

IV. 90° HYBRID DIRECTIONAL COUPLER

The second manufactured prototype is a 90° hybrid directional coupler operating at the working frequency of 5 GHz. This 4 ports device (with 50 Ω characteristic impedance) is characterized by the equitable division of the signal that enters in a port (port 1 of the Fig. (10) in both the direct and the coupling arms (ports 3 and 4). On the other hand, the remaining port (port 2) is isolated. Additionally, there is a 90° phase shift between the two output signals of ports 3 and 4. One of the possible realizations of the device (and the chosen one) is the branch-line type, where its four arms have a length of $\lambda/4$, with the vertical arms having a characteristic impedance of 50 Ω and of $50/\sqrt{2}$ Ω for the horizontal ones [19].

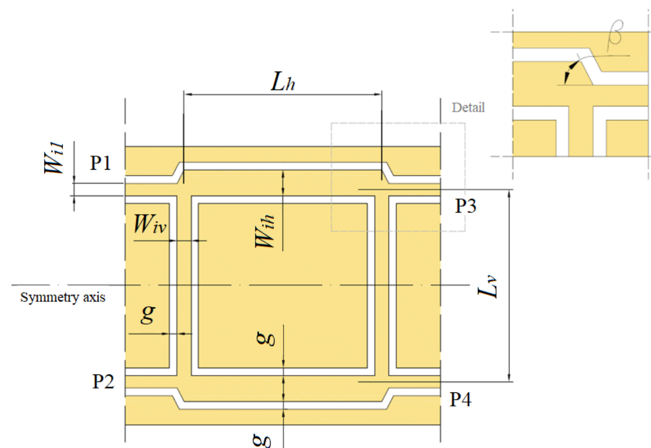


Fig. 10. Top view and detail of the layer 3 for the designed 90° hybrid.

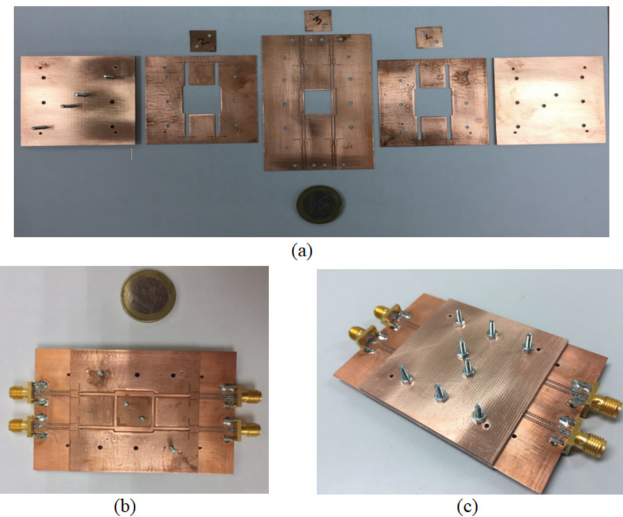
It is noteworthy, in this type of geometry, that the length of the four transitions is affected by half the width of the inner conductor of the vertical arms. Thus, the length of the transitions is invariant and has been designed as a linear variation of the width of the active strip, see Fig. 10. In this case these variations have a slope of $\beta = 62°$, see the detail in Fig. 10.

Once the device has been modelled, its dimensions have been optimized to achieve the desired response. This optimization has been carried out by the right selection of both the lengths of the arms and the widths of the inner strip, for example the optimal electrical response is achieved for a characteristic impedance of 48.26 Ω for the vertical branches (W_{iv}), 34 Ω for the horizontal branches (W_{ih}) and 50 Ω for the input or feeding lines (W_{i1}), where all related final dimensions are collected in Table VI.

TABLE VI
DIMENSIONS OF THE 90° HYBRID.

Parameter	Measure (mm)
W_{iv}	1.05
W_{ih}	1.98
W_{i1}	0.96
g	0.6
L_H	15.36
L_v	15.94

The major problem in the manufacture of this device is the loss of continuity between the inner square and the rest of the structure, as can be seen in Fig. 11 (a). This is solved by manufacturing it separately, assembling and fixing it with screws. Besides this, the same substrates and techniques employed with the ESICL and the power divider have been used in the manufacturing process of this device.



(a)

(b)

(c)

Fig. 11. (a) Exploded view of the 90° hybrid layers. (b) Top view of the final device, layers 1 to 4. (c) The final assembled device with connectors for measurements.

In Fig. 12 the simulated results are shown together with the measurements of the fabricated device. As can be seen, the scattering parameters of the manufactured device are the expected ones for a 90° hybrid operating at 5 GHz.

As in the case of the power divider, the matching of port 1 and the isolation of port 2, in the manufactured device, have been optimally shifted to the design frequency. In this case, the measured relative bandwidth is 22% for a return loss value higher than 15 dB. It should be noted that the relative increase in expected losses of the theoretical device affects positively in terms of bandwidth and matching. On the other hand, there is

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a power division of -3.7 dB ± 0.4 dB (S_{41}) and -3.5 dB ± 0.5 dB (S_{31}), including the effect of transitions and connectors.

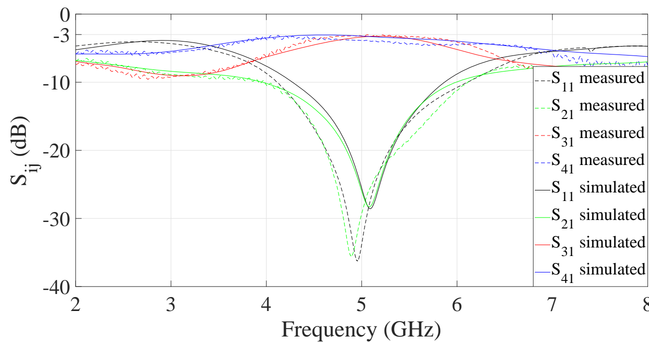

Fig. 12. Measured vs. simulated results of the most significant scattering parameters of the 90° hybrid.

Finally, in Fig. 13 the simulated versus measured phase shift is shown. It can be observed how the real one is well matched to the simulated one (even slightly improved), providing a value of 89.5° ± 1° for the considered bandwidth.

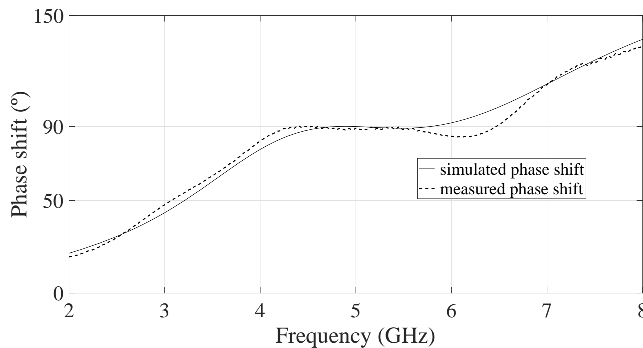

Fig. 13. Measured vs. simulated output phase shift.

TABLE VII
COMPARISON OF THE QUADRATURE HYBRID.

Parameter	ESICL	Waveguide	SICL
Dimensions (mm^3)	20x37x4.8	153x267x63.5	14x24x0.5
Weight (g)	48.28	900	(not reported)
Frequency (GHz)	5	5	5.5
Bandwidth (%)	22	14	16
Insertion loss (dB)	0.5	(not reported)	0.8
Unbalance (dB)	± 0.98	± 0.25	± 1

The comparison of the quadrature hybrid has been performed with two different devices with similar features: a commercial waveguide hybrid ('Z' Style combiner-divider Model No. 5228W of Advanced Technical Materials Inc.) and another one manufactured in SICL [22], as can be seen in Table VII. Since the data reported for these two devices do not consider the effect of transitions and connectors, the loss due to connectors in the measurement has been removed for the ESICL device. Please note that the bandwidth value for ESICL and SICL devices are for return loss values greater than 15 dB, and the value for the waveguide device is for values greater than 26 dB. The ESICL hybrid direct coupler is much lighter and smaller than the waveguide one, and just slightly bigger than the SICL device. Furthermore, the frequency response is in good comparison to other SIC technologies. In this way, ESICL technology demonstrates its viability for applications that require a trade-off between electrical performance, size and weight.

V. CONCLUSION

An efficient ESICL, in terms of monomode bandwith, and a well matched transition with a GCPW line have been designed and manufactured. Using this technology, two passive components, a power divider and a 90° hybrid directional coupler, have been designed and implemented. The results prove that such devices present an electrical response close to those equivalent in waveguide technology, but with reduced mass and volume. These characteristics make them good candidates for applications where small reduced devices, easy integration and inexpensive manufacturing whilst keeping a sufficient electrical performance are needed. These promising results lead to think on the potential use of the same technology for implementing more complex devices, such as multiplexers, diplexers and feeding networks for beam-forming phased arrays.

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