

# Realization and Optimization of Metal-Semiconductor Field-Effect Transistors and Integrated Circuits based on Amorphous Zinc Tin Oxide

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# Bibliographische Beschreibung

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*Realization and Optimization of Metal-Semiconductor Field-Effect Transistors and Integrated Circuits based on Amorphous Zinc Tin Oxide*

Universität Leipzig, Dissertation

163 Seiten, 118 Zitate, 71 Abbildungen, 6 Tabellen

## Referat:

Im ersten Teil der vorliegenden Arbeit werden die physikalischen Eigenschaften, insbesondere die elektrische Leitfähigkeit, von Zink-Zinn-Oxid Dünnschichten sowie darauf basierenden Schottky-Dioden in Abhängigkeit von der Kationenkomposition bestimmt. Zur Herstellung dieser Dünnschichten wurde ein Verfahren genutzt, welches die Herstellung von kontinuierlichen Kompositiongradienten im Rahmen eines gepulsten Laserabscheidungsprozesses bei Raumtemperatur ermöglicht. Erster Schwerpunkt der Diskussion ist die Abhängigkeit elektrischer Eigenschaften der Dünnschichten sowie die Diodeneigenschaften vom Kationenverhältnis. Des Weiteren wird die Langzeitstabilität der Schottky-Dioden und der Einfluss der Sauerstoffzufuhr während der Kontaktherstellung auf die Eigenschaften der Schottky-Dioden herausgestellt. Die Ergebnisse tiefenaufgelöster Röntgenphotoelektronenspektroskopie werden diskutiert und ein Mechanismus, welcher zu einer Verbesserung der Schottky-Dioden über die Zeit führt, wird vorgestellt.

Die Erkenntnisse über die optimale Kationenkomposition und den Einfluss des Sauerstoffs auf die Eigenschaften von Schottky-Dioden wurden genutzt, um Metall-Halbleiter-Feldeffekttransistoren herzustellen, welche im zweiten Teil der vorliegenden Arbeit beschrieben werden. In einem ersten Schritt wurden hierfür die Abscheidebedingungen in der Sputterkammer optimiert und eine neue Abscheiderezeptur für die Herstellung von Feldeffekttransistoren eingeführt. Auch hier finden alle Abscheidungen bei Raumtemperatur statt. Die Abscheidung mittels Sputtern wurde gewählt, da diese Abscheidemethode größere industrielle Relevanz als die gepulste Laserabscheidung hat. Metall-Halbleiter-Feldeffekttransistoren mit zwei verschiedenen Gate-Typen werden vorgestellt und jeweils der Einfluss der Kanalschichtdicke auf die Transistoreigenschaften untersucht. Der Einfluss des durch die Herstellung erzeugten Sauerstoffreservoirs in dem Schottky-Gate Kontakt auf die Eigenschaften der Feldeffekttransistoren wird ebenso gezeigt wie der Einfluss eines thermischen Ausheizprozesses auf die Schaltgeschwindigkeit der Feldeffekttransistoren. Außerdem werden einfache Inverter, welche auf zwei gleichartigen Feldeffekttransistoren basieren, vorgestellt. Ebenfalls werden Schottky-Dioden Feldeffekttransistoren Logik basierte Inverter vorgestellt und charakterisiert.

Abschließend werden Ringoszillatoren, aufgebaut aus mehreren in Reihe geschalteten Schottky-Dioden Feldeffekttransistoren Logik basierten Invertern vorgestellt. Der Einfluss der Kanalschichtdicke und der Gate-Geometrie auf die Oszillationsfrequenz wird diskutiert.

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# Abstract

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163 pages, 118 citation, 71 figures, 6 tables

## Abstract:

In the first part of the present work the physical properties, especially the electrical properties, of zinc tin oxide thin films as well as Schottky diodes based thereon are determined as a function of the cation composition. For film growth, a room temperature pulsed laser deposition process was used, which allows the realization of a continuous composition gradient within one sample. First focus of the discussion is the dependence of electrical properties of thin films as well as diode properties on the cation ratio. Furthermore, the long-term stability of the Schottky diodes and the influence of the oxygen supply during contact fabrication on the properties of the Schottky diodes are highlighted. The results of depth-resolved X-ray photoelectron spectroscopy measurements are discussed and a mechanism leading to an improvement of the Schottky diodes over time is elucidated.

The findings on the optimal cation composition and the influence of oxygen on the properties of Schottky diodes were used to produce metal-semiconductor field-effect transistors, which are described in the second part of this thesis. In a first step, the deposition conditions in the sputter chamber were optimized and a new deposition recipe for the fabrication of field effect transistors was developed. Here, too, all depositions take place at room temperature. Sputter deposition was chosen because this deposition method has greater industrial relevance than pulsed laser deposition. Metal-semiconductor field-effect-transistors with two different gate types are presented and the influence of the channel layer thickness on the transistor properties is investigated. The influence of the oxygen reservoir in the Schottky gate contact on the properties of the field-effect-transistors is shown as well as the influence of a thermal annealing process on the switching speed of the field-effect-transistors. In addition, simple inverters based on two identical field-effect-transistors are demonstrated. Also Schottky diode field-effect-transistor logic based inverters are presented and characterized.

Finally, ring oscillators consisting of several series-connected Schottky diode field-effect-transistor logic based inverters are presented. The influence of channel layer thickness and gate geometry on the oscillation frequency is discussed.

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## Zusammenfassung der Dissertation

*Realization and Optimization of Metal-Semiconductor Field-Effect Transistors and Integrated Circuits based on Amorphous Zinc Tin Oxide*

Der Fakultät für Physik und Geowissenschaften der Universität Leipzig  
eingereicht von

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angefertigt am

Felix-Bloch-Institut für Festkörperphysik Leipzig, Abteilung Halbleiterphysik

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Amorphous oxide semiconductors (AOSs) form a promising field of study in material research, driven by potential applications such as transparent and bendable electronic circuits. A prominent example, indium gallium zinc oxide, is nowadays already used in organic light emitting diode (OLED) displays as thin film transistors driving the individual pixel. Since indium is rare and has a high risk index [1], the investigation of alternative materials is of interest. A compound that comprises only naturally abundant elements, is zinc tin oxide (ZTO) [1]. As is typical for the group of AOSs, it exhibits a comparably high electrical conductivity and electron mobility even in the amorphous state [2-4]. The high potential of ZTO as pixel driver has been shown in 2006 by Görrn *et al.* using ZTO channels in metal-insulator-semiconductor field-effect transistors (MISFETs) as pixel drivers of OLEDs [5]. In literature, there are numerous reports on ZTO based MISFETs, which typically have the drawback of high voltage ranges required to switch the device from on to off. In 2017, Dang *et al.* presented the first ZTO based metal-semiconductor field-effect transistor (MESFET), which requires smaller voltages to switch the device [6]. However, an annealing of the ZTO channel was required to achieve a field-effect.

The aim of this work was the realization of MESFETs and integrated circuits based on amorphous ZTO deposited at room temperature. In the first part of this thesis the physical properties, especially the electrical properties, of ZTO thin films and of Schottky barrier diodes based on them are discussed in dependence on the cation ratio. A continuous composition spread approach for pulsed laser deposition (PLD) was used to achieve a large range of cation compositions within one deposition step [7]. A tuning of the free carrier density from  $3.9 \times 10^{19} \text{ cm}^{-3}$  for low zinc contents to  $0.5 \times 10^{17} \text{ cm}^{-3}$  for high zinc contents was achieved. An increase of the rectification ratio with increasing zinc content in the thin films was measured for the platinum oxide Schottky barrier diodes. A maximum current rectification ratio of  $2.7 \times 10^7$  was obtained for a zinc

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content of  $0.63 \text{ Zn}/(\text{Zn}+\text{Sn})$ . The increase of the rectification ratio with increasing zinc content is mainly due to a decrease of the reverse diode current, where the largest changes were observable for  $\text{Zn}/(\text{Zn}+\text{Sn}) < 0.5$ .

The long term stability of the Schottky barrier diodes was investigated. A decrease of the reverse diode current over time was observed, resulting in an increase of the rectification ratio. The forward current as well as the Schottky barrier height remained unaltered. It is known that oxygen plays a crucial role for the formation of Schottky barrier contacts to oxide semiconductors [8]. This leads to the hypothesis that oxygen diffuses from the noble metal oxide into the semiconductor. To investigate this, an experiment was conducted in which the extent of the oxygen reservoir in the Schottky barrier contact was varied. A higher oxygen reservoir led to higher rectification ratios in the as deposited state and a major improvement of the diodes over time. Using current-voltage measurements the time development of the improvement was investigated. Simultaneously, depth resolved X-ray photoelectron spectroscopy measurements were performed by Thorsten Schultz at the Humboldt Universität Berlin to study the spatial diffusion of oxygen. A diffusion of oxygen from the semiconductor into the metal contact was found as origin of the ohmic behavior of platinum/ZTO contacts. In contrast, a diffusion of oxygen from the metal oxide into the semiconductor was found to decrease the the reverse current of the platinum oxide/ZTO diodes.

These results were used as a basis for the fabrication of MESFETs. Room temperature sputtering was chosen as deposition technique because it has a higher industrial relevance than PLD. A new sputtering recipe was developed, which allows the reproducible fabrication of MESFETs. Two different gate contact types were investigated:  $\text{PtO}_x/\text{Pt}$  and intrinsic (*i*-)ZTO/ $\text{PtO}_x/\text{Pt}$  gate contacts. The advantage of the first are sub-threshold swings as low as  $109 \text{ mV dec}^{-1}$ , whereas the latter exhibit drain current on-to-off ratios as high as  $1 \times 10^7$ . An optimization of the devices was sought by a variation of the channel thickness. This was used to tune the threshold voltage. Simple inverters were investigated for both gate types. For the  $\text{PtO}_x/\text{Pt}$  gate contacts, a peak gain magnitude (*pgm*) as high as 263 was measured after a storage of the device for 145 days in ambient condition. Simple inverters based on MESFETs with *i*-ZTO/ $\text{PtO}_x/\text{Pt}$  gate contacts have *pgm* values as high as 385.

Schottky diode FET logic (SDFL) inverters were fabricated with *i*-ZTO/ $\text{PtO}_x/\text{Pt}$  gate contacts and a signal shift was achieved. Three stage ring oscillators based on SDFL inverters were characterized. A strong dependence of the oscillation frequency on the channel thickness and the gate geometry was observed. A maximum oscillation frequency of 555 kHz was obtained, which is comparable to values reported in literature for annealed ZTO channels [8,9].

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# Chapter 1

## Introduction

In recent years, the use of amorphous oxide semiconductors (AOSs) as an alternative to silicon based technologies for use in displays has gained in importance. In the field of displays, AOSs disclose the possibility to realize energy saving and faster displays for mobile phones and other technical applications. The currently most common displays are based on liquid crystals, which require back-lighting and switch comparatively slow. A promising alternative is the use of organic light emitting diodes (OLEDs), which are self-luminous and have higher switching speeds than displays based on liquid crystals. The control of OLEDs in displays is more efficiently done by using AOSs compared to amorphous silicon, as their electron mobility exceeds that of amorphous silicon [1]. Therefore, the outstanding advantages of AOSs based technologies are lower fabrication costs and performance, e.g. a faster switching of devices, compared to amorphous silicon electronics. In addition, large scale deposition at low temperatures is possible.

The high electron mobility of AOSs compared to amorphous silicon is due to the electronic structure of this material group. The conduction band minimum is predominantly formed by the large, spherical s orbitals of the metal cations [2,3]. This leads to an insensitivity against small variations in the bond angle, which are typical for amorphous materials. Electron mobilities 10 to 50 times higher than those of amorphous silicon were reported [1]. In addition, AOSs may be deposited at low or even room temperatures which allows the use of thermally unstable substrates, such as flexible plastic substrates [4]. As mentioned above, field-effect transistors (FETs) based on AOSs may be used to control OLED pixels in displays. As of today, amorphous [! (!)3]IGZO is used for this purpose [5,6]. However, a disadvantage of [! (!)3]IGZO is the use of rare and expensive indium [7]. An alternative, less studied material is amorphous [! (!)3]ZTO. It consists of naturally abundant and non-toxic elements only [7]. For room temperature deposited [! (!)3]ZTO, electron mobilities exceeding

$12\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$  [8] and optical band gaps around 2.8 eV have been reported [9]. In 2006, Görrn *et al.* demonstrated the use of  $\text{In}_2\text{O}_3/\text{ZTO}$  based FETs for the control of OLED pixels on a transparent substrate [10,11]. Up to now, most  $\text{In}_2\text{O}_3/\text{ZTO}$  based devices in literature are metal-insulator-semiconductor field-effect transistors (MISFETs), which have the disadvantage of large voltage ranges which are typically required to switch the devices from the on to the off state. Moreover, an annealing of the channel and/or a deposition at elevated temperatures are often required to improve the performance and stability of the devices [12,13]. The influence of the stoichiometry on the performance of devices and the stability against bias stress has been discussed [13].

Recently, the first  $\text{In}_2\text{O}_3/\text{MESFET}$  based on amorphous  $\text{In}_2\text{O}_3/\text{ZTO}$  has been demonstrated [14]. In comparison to MISFETs, a smaller voltage range is required to switch the device from on to off. However, a deposition at elevated temperatures and an annealing at more than  $400^\circ\text{C}$  is required to achieve a field-effect. This is incompatible with the use of bendable organic substrates, where the temperature must not exceed  $350^\circ\text{C}$  [1].

The goal of this work was the realization and characterization of metal-semiconductor field-effect transistors (MESFETs) and integrated circuits based on amorphous  $\text{In}_2\text{O}_3/\text{ZTO}$  deposited at room temperature. After a short summary of the theoretical descriptions of the devices that were investigated, a recapitulation of the deposition and characterization methods is given. The experimental part of this work is split into two parts. The first part concentrates on physical properties of  $\text{In}_2\text{O}_3/\text{ZTO}$  thin films and Schottky barrier diodes based thereon. The second part is dedicated to the fabrication of MESFETs and integrated circuits based on these MESFETs, using the results from the first part. In chapter 4, the dependence of the physical properties of amorphous  $\text{In}_2\text{O}_3/\text{ZTO}$  are investigated in dependence on the cation composition. To obtain a large range of cation compositions within one deposition process and at the same deposition parameters, a  $\text{In}_2\text{O}_3/\text{CCS}$  approach for  $\text{In}_2\text{O}_3/\text{PLD}$  was used for the deposition of thin films. Hall effect measurements were conducted to obtain their electrical properties and Schottky barrier diodes were investigated. A strong influence of the cation composition on the performance of platinum oxide Schottky barrier diodes was observed. Additionally, the performance of the Schottky barrier diodes could be further influenced by the oxygen content provided during the deposition of the metal oxide Schottky contacts.

The long term stability of the Schottky barrier diodes and in particular the crucial role of oxygen for the long term stability are discussed. With the help of depth resolved  $\text{In}_2\text{O}_3/\text{XPS}$  measurements, an explanation for the origin of the absent long term stability is sought.

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Based on the results discussed in the previous chapter, MESFETs and integrated circuits are reported in chapter 5. A deposition by sputtering was chosen, as this method is already used commercially and large scale depositions are possible. As for the deposition by [! (!)3]PLD, all thin films were fabricated at room temperature. An optimization of the deposition conditions as well as the proposal of a new sputtering recipe for the fabrication of FETs is presented. With this sputtering recipe the fabrication of MESFETs at room temperature is possible. An optimization of the gate contact was performed, using two different approaches for the realization of a functional platinum oxide gate contact. The first gate contact is without and the second with an additional intrinsic [! (!)3]ZTO layer [8] between the conductive channel and the gate contact. An investigation of the influence of the channel thickness is presented for both gate types. For the contacts without intrinsic [! (!)3]ZTO layer, the important role of oxygen for the formation of the rectifying gate contact is again investigated for the sputtered thin films. In addition, the switching speed of MESFETs is discussed. Using the second contact type, MESFETs and simple inverters based thereon as well as [! (!)3]SDFL inverters are reported. These devices represent the first step towards integrated circuits. An inverter chain as well as ring oscillators based on the [! (!)3]SDFL inverters are discussed. Further, a maximization of the oscillation frequency is sought by a variation of the channel thickness and contact geometry. Additionally, the results are compared to devices reported in literature based on amorphous [! (!)3]ZTO. In the last part of this thesis a summary of the presented results is given and an outlook on possible further investigations is presented.

**Annotation:** This work was prepared in the semiconductor physics group of the Felix-Bloch-Institut of the Universität Leipzig. Contributions by third parties are marked in the text and are by current or former members and students of the Universität Leipzig. The only exception is a contribution by Thorsten Schultz, who works at Humboldt Universität Berlin. References to publications with own contribution are marked with 'E'.



# Chapter 2

## Theoretical Descriptions

### 2.1 The Amorphous Semiconductor Zinc Tin Oxide

In this work, devices based on amorphous [! (!)3]ZTO are presented. Therefore, a short summary of the most important material properties and advances in research regarding this material system is given.

Amorphous [! (!)3]ZTO belongs to the group of amorphous oxide semiconductors (AOSs). This group contains oxides of heavy cations which have an electronic configuration of  $(n - 1)d^{10}ns^0$ ,  $n > 3$  [3]. Common to this material group is that the conduction band minimum is formed by the  $s$  orbitals of the metal cations. In the bound state of the metal oxides, these  $s$  orbitals are unoccupied. The  $s$  orbitals are extensive and spherical with a large spatial overlap, which renders them insensitive to variations of the bond angle, which are typical for amorphous oxide semiconductors. This leads to the comparably large conductivity and electron mobility of the AOS [2,3].

The most commonly used metal cations with this electronic configuration are indium, gallium, zinc and tin. Consisting of these elements, the well studied AOS [! (!)3]IGZO and [! (!)3]ITO are already used commercially [15-17]. The drawback of [! (!)3]IGZO and [! (!)3]ITO are that they contain the rare and expensive element indium [7]. An alternative consisting of readily available and cheaper components only is zinc tin oxide [7].

The high electron mobility can even be achieved for room temperature depositions [9]. In combination with the large optical band gap of [! (!)3]ZTO (2.8 eV reported in ([9])), this material is an interesting candidate for future transparent device applications on bendable, organic substrates.

Most studies on amorphous [! (!)3]ZTO concentrate on the use of the material as channel layer in transistors and integrated circuits. Numerous reports<sup>1</sup> deal with the optimization of crucial material properties of amorphous zinc tin oxide by employing a variety of different

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<sup>1</sup>Only a small overview over publications is given and no complete list of publications on amorphous [! (!)3]ZTO.

deposition methods among which are [! (!)3]PLD [8, 9, 18] [E1], sputter deposition [19, 20], solution processing [21, 22] and [! (!)3]CVD [14]. For [! (!)3]PLD and sputter deposited [! (!)3]ZTO, the possibility of tuning the electrical and optical properties by a variation of the deposition conditions has been reported [8, 9, 18, 20]. Electron mobilities as high as  $12.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  were achieved [8] as well as the possibility to tune the free carrier density over six orders of magnitude [9].

The investigation of the cation ratio of the ternary compound [! (!)3]ZTO with the aim to optimize the electrical and optical properties has received special attention. Therefore, studies on the influence of the cation ratio on the material properties and the device performance were conducted for deposition methods such as [! (!)3]PLD [9, 13] [E2], sputter deposition [23-27] and solution processing [21, 22, 28, 29].

The vast majority of publications concerning amorphous [! (!)3]ZTO concentrate on the investigation of zinc tin oxide for the use as channel material in metal-insulator-semiconductor field-effect transistors (MISFETs). The first [! (!)3]ZTO based MISFET was presented in 2005 by Chiang *et al.* [12]. Since then, numerous studies<sup>2</sup> on [! (!)3]ZTO based MISFET have followed [10, 11, 22, 29-33] and the first integrated circuits [21, 32, 34-36] were demonstrated. For all but the devices presented by Görrn *et al.* [10], a deposition at elevated temperatures (above 150°C) or an annealing step were required after the [! (!)3]ZTO channel deposition to achieve high quality FETs.

Complementary to the MISFET devices based on [! (!)3]ZTO, heterojunction and Schottky barrier diodes based on amorphous [! (!)3]ZTO were investigated with the aim to fabricate junction field-effect transistors (JFETs) and MESFETs. The first heterojunction and Schottky barrier diodes based on amorphous pulsed laser deposited [! (!)3]ZTO were reported by Schlupp *et al.* in 2014 and 2017, respectively [7, 37]. Rectification ratios as high as seven orders of magnitude were reported. Also in 2017, the first [! (!)3]MESFET based on amorphous [! (!)3]ZTO was presented by Dang *et al.* [14] using reactively sputtered silver oxide as Schottky barrier gate material. The ZTO was deposited by mist-chemical vapor deposition and drain current on-to-off ratios as high as five orders magnitude were achieved.

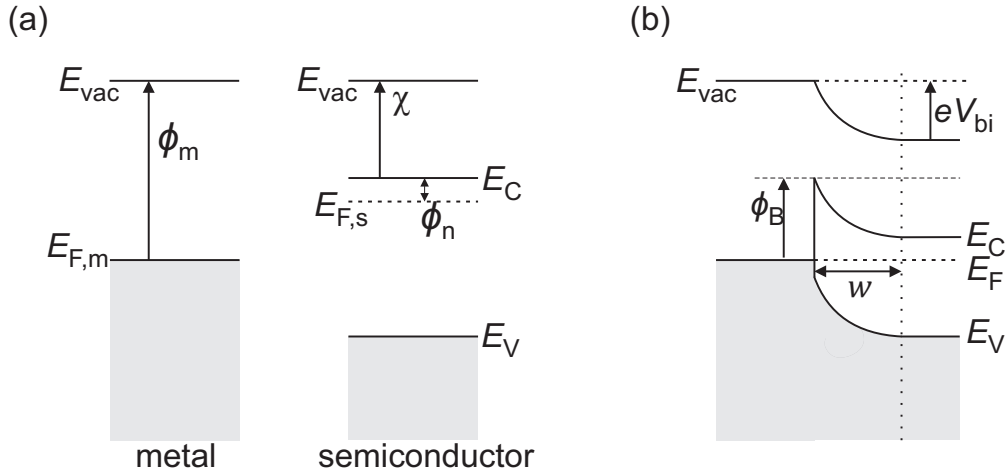
In this work, investigations on [! (!)3]ZTO thin films deposited by [! (!)3]PLD and sputter deposition as well as devices based on these thin films are discussed.

## 2.2 Schottky Barrier Diodes

Ohmic and rectifying contacts are required for almost all electronic devices. The most commonly used forms of rectifying contacts are based on *pn*-(hetero)junctions and metal-semiconductor contacts. In this chapter, a short summary on the theory of metal-semiconductor contacts is given, as all devices in this work will be based on this contact type. More detailed derivations can be found in [38, 39]. Metal-semiconductor contacts are also called Schottky

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<sup>2</sup>Only a small overview over studies on amorphous [! (!)3]ZTO based devices is given here.



**Figure 2.1:** Schematic drawing of a metal and a  $n$ -type semiconductor before (a) and after (b) they are brought in contact.

barrier contacts, or diodes, after a first model proposed for the description of these contacts by W. Schottky and N. Mott [40-42].

As a  $n$ -type semiconductor is used in this work, all discussions are given for this configuration. The descriptions for  $p$ -type semiconductors are analogous.

**Formation of a Barrier** In general, a metal and a semiconductor have different Fermi levels  $E_F$  and vacuum levels  $E_{vac}$ . In Figure 2.1 (a), these levels are shown for metal and semiconductor, for the case that they are not in contact. The distance between conduction band minimum and Fermi level in the semiconductor is denoted by  $\phi_n$  and  $\chi = E_{vac} - E_C$  denotes the electron affinity, where  $E_C$  is the conduction band minimum. If a metal with a work function  $\phi_m = E_{vac} - E_{F,m}$  is brought into contact with a  $n$ -type semiconductor with the electron affinity  $\chi$ , the Fermi levels of the two materials align. To achieve this, the bands in the semiconductor bend near the interface. If the work function of the metal is larger than the electron affinity of the  $n$ -type semiconductor, electrons flow from the conduction band of the semiconductor into the metal. The band bending continues until the Fermi levels have aligned. On the metal side electrons accumulate, while on the semiconductor side the ionized donors lead to a positive charge. This region is called space charge region or depletion region width  $w$ . The electrical field induced by the charge accumulation in the metal and the semiconductor inhibits the further diffusion of charges.

In Figure 2.1 (b), the case after the metal and semiconductor are brought in contact is shown. The barrier, which forms due to the aligning of the Fermi levels and the therefor necessary band bending, has a height of

$$\phi_B = \phi_m - \chi . \quad (2.1)$$

The potential difference, which arises on the semiconductor side, is called built-in potential  $V_{bi}$ , with

$$eV_{bi} = \phi_B - \phi_n , \quad (2.2)$$

where  $e$  is the elementary charge.

If an external voltage is applied between metal and semiconductor, the Fermi level in the semiconductor is shifted by  $eV$ . A negative voltage applied at the Schottky metal shifts the Fermi level in the semiconductor down, a positive voltage shifts it up. The application of a positive voltage is called forward regime. In this case, the applied voltage reduces the built-in potential. If the applied voltage is as large as  $V_{bi}$ , the bands are flat and electrons may flow freely from the semiconductor into the metal. For negative applied voltages, electrons flowing from metal to semiconductor see a constant barrier, whereas electrons flowing from semiconductor to metal see an increased barrier. As a negative voltage is applied at the metal, electrons flowing from metal to semiconductor dominate the current flow and the current stays constant in the reverse regime.

To describe the band diagram in dependence on the applied voltage, the Poisson equation

$$\frac{d^2\phi}{dx^2} = -\frac{1}{\epsilon_r\epsilon_0}\varrho(x) \quad (2.3)$$

has to be solved, where  $\epsilon_r$  and  $\epsilon_0$  are the relative dielectric constant and the vacuum permittivity, and  $\phi$  is the electric potential.  $\varrho$  is the carrier density. This equation has to be solved in the regime  $0 \leq x \leq w$ , where  $x$ -axis is perpendicular to the metal semiconductor interface. The interface is located at  $x = 0$ . In the abrupt approximation the carrier density is given as

$$\varrho = \begin{cases} eN_D & \text{for } 0 \leq x \leq w \\ 0 & \text{for } x > w \end{cases} . \quad (2.4)$$

With the boundary conditions  $\phi(x = 0) = -eV_{bi}$  and  $\phi(x = w) = 0$ , and the condition that  $\frac{d\phi}{dx}(w) = 0$ , the Poisson equation can be solved by integrating twice. For a constant doping  $N_D$ , the potential in dependence on the position is

$$\phi(x) = -\phi_B + \frac{e^2N_D}{\epsilon_r\epsilon_0} \left( wx - \frac{1}{2}x^2 \right) \quad (2.5)$$

with

$$w = \sqrt{\frac{2\epsilon_r\epsilon_0}{eN_D}(V_{bi} - V)} \quad (2.6)$$

as solution.  $V$  is, as described above, the externally applied voltage.

**Depletion Region Capacitance** The charge  $Q$  in the depletion region is

$$Q = A_0 \int_0^w \varrho dx = eN_D w A_0 , \quad (2.7)$$

where  $A_0$  is the contact area. Using the charge  $Q$ , the capacitance of the depletion region can be calculated as

$$C = \left| \frac{dQ}{dV} \right| = \frac{\epsilon_r \epsilon_0 A_0}{w} . \quad (2.8)$$

The metal surface is an equipotential surface, which leads to an image charge effect. An electron at a distance  $x$  from the equipotential surface interacts with it as though a positive charge is located at  $-x$ . An attractive image force  $F_{IF}$

$$F_{IF} = -\frac{e^2}{16\pi\epsilon_r\epsilon_0 x^2} \quad (2.9)$$

acts on the electron in the semiconductor. This reduces the barrier by  $\Delta\phi$

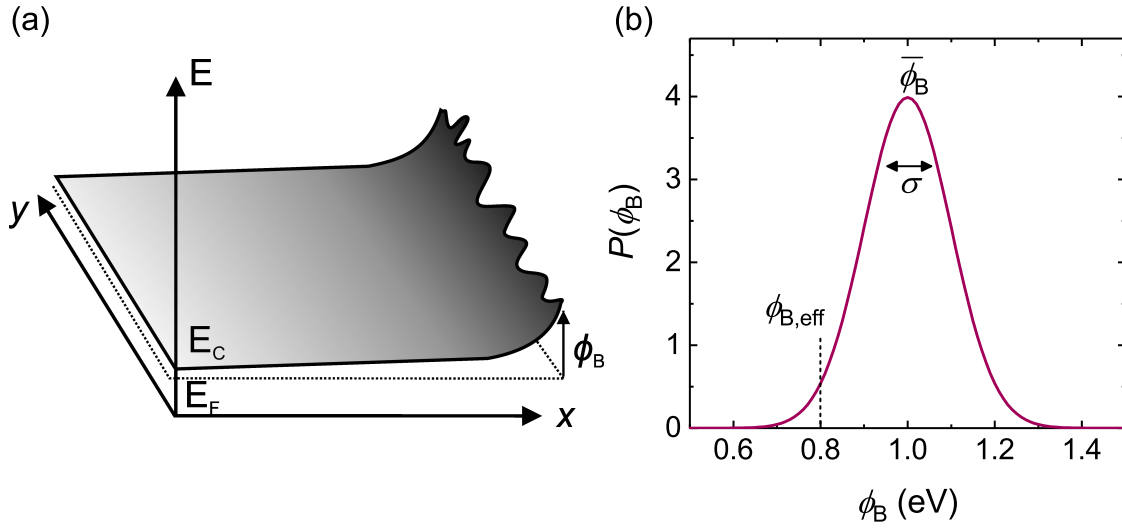
$$\Delta\phi = \frac{e^2}{2\pi\epsilon_r\epsilon_0} \sqrt{\frac{N_D w}{\pi}} . \quad (2.10)$$

Due to  $w$ , this equation depends on the external voltage  $V$ . This effect is called image force lowering or Schottky effect.

**Transport at the Barrier** Depending on the barrier height and the energy of the electrons, there exist different transport mechanism over and through the barrier [38]. Typically, one transport mechanism dominates. The transport can be limited by diffusion, which is due to a carrier concentration gradient within the depletion region. Another transport mechanism, where the electrons transport takes place over the barrier is thermionic emission, which is possible due to the energy distribution of the electrons. Even at low temperatures, single electrons have energies high enough to overcome the barrier. In (thermionic) field emission, the electrons tunnel through the barrier. To enable the tunneling of electrons through the barrier, the barrier has to be thin enough and electron energies have to be sufficiently high. Further transport mechanisms are recombination in the depletion layer and hole injection from the metal [38]. In the case of amorphous [! (!)3]ZTO, it is assumed that thermionic emission is the dominating transport mechanism [37] [E2]. It has to hold that the barrier height is larger than  $k_B T$  and the mobility of the electrons has to be large enough that the mean free path is large against the depletion region width. The equation for the current density for the case of thermionic emission was first presented by A. Bethe [43] and later on refined by E. Rhoderick and R. Williams [44]. The current density can be written as

$$j = j_s \exp\left(\frac{eV}{\eta k_B T}\right) \left[1 - \exp\left(-\frac{eV}{k_B T}\right)\right] , \quad (2.11)$$

where  $j_s$  is the saturation current density and  $V$  the external voltage applied at the contact.  $T$  denotes the temperature,  $k_B$  the Boltzmann constant and  $\eta$  the ideality factor. The saturation



**Figure 2.2:** Schematic drawing of a fluctuating barrier height (a) and distribution of the barrier height for  $\sigma = 0.1$  eV,  $\phi_{\text{mean}} = 1$  eV and  $\phi_{\text{eff}} \approx 0.8$  eV. Adopted from [45, 46].

current density can be calculated as

$$j_s = A^* T^2 \exp\left(-\frac{\phi_{B,0}}{k_B T}\right), \quad (2.12)$$

where  $\phi_{B,0}$  is the barrier height without an externally applied voltage and  $A^*$  is the Richardson constant, which can be calculated as

$$A^* = \frac{4\pi e m_{\text{eff}} k_B^2}{h^3}, \quad (2.13)$$

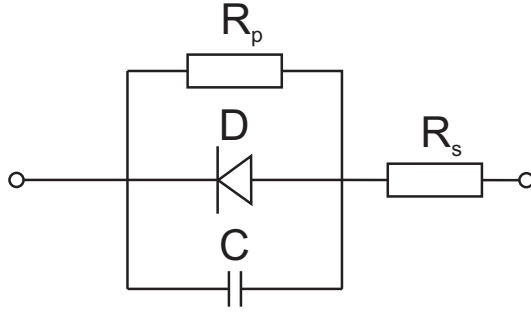
with the effective electron mass  $m_{\text{eff}}$ . The ideality factor  $\eta$  is a measure for the voltage dependence of the barrier height and is given by

$$\eta = 1 + \frac{1}{e} \frac{\partial \phi_B}{\partial V}. \quad (2.14)$$

As shown above, the image charge effect has a non-linear voltage dependence, which leads to an increase of the minimal achievable ideality factor from 1 to a slightly higher value (e.g.  $\eta = 1.02$  for crystalline  $\text{Ga}_2\text{O}_3$ ) [38].

**Non-Idealities in Real Diodes** In real, non-ideal diodes, fluctuations in the barrier height may arise due to e.g. a rough interface between metal and semiconductor or local fluctuations in the free carrier density. In Figure 2.2 (a) the barrier height fluctuations are schematically drawn in a direction parallel to the sample surface.

The Schottky contact can be regarded as several diodes connected in parallel, each with a different barrier height. This was, amongst others, discussed by Yearian *et al.* [47, 48]. J. Werner and H. Güttler [45] developed a model based on the assumption of a Gaussian barrier



**Figure 2.3:** Equivalent circuit of a real diode with capacitance  $C$ , parallel resistance  $R_p$ , series resistance  $R_s$  and ideal diode  $D$ .

height distribution by:

$$P(\phi_B) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(\bar{\phi}_B - \phi_B)^2}{2\sigma^2}\right), \quad (2.15)$$

where  $\bar{\phi}_B$  is the mean barrier height and  $\sigma$  the standard deviation of the barrier height distribution. An exemplary distribution is shown in Figure 2.2 (b). The total current density is calculated by a weighted integration of the currents for each barrier height:

$$j = \int P(\phi_B) j_\phi(\phi_B) d\phi_B. \quad (2.16)$$

For thermionic emission an analytic solution exists [45]. Therefore the barrier height in equation 2.12 is replaced by the effective barrier height  $\phi_{B,\text{eff}}$ . The effective barrier height is always smaller than the mean barrier height, as current paths with smaller barrier heights are preferred. The effective barrier height can be written as:

$$\phi_{B,\text{eff}} = \bar{\phi}_{B,0} - \frac{\sigma_0^2}{2k_B T}. \quad (2.17)$$

In general, the barrier parameters are voltage dependent.

Tung *et al.* [49] describe the current transport in Schottky diodes by thermionic emission with regions with smaller and larger barrier heights within the contact area. Regions with larger barrier heights have almost no contribution to the total current transport and are therefore disregarded [49]. Schmitsdorf *et al.* could show that a correlation exists between ideality factor and effective barrier height [50, 51]. For ideality factors that are nearly 1, a linear dependence exists. Using this correlation, the homogeneous barrier height can be evaluated by a linear extrapolation of the plot of the effective barrier height against the ideality factor down to the smallest possible ideality factor. The minimal ideality factor is 1 in the ideal case but in reality slightly higher due to image charge effects [38]. If large ideality factors are used for this extrapolation, the obtained homogeneous barrier height  $\phi_{B,\text{hom}}$  underestimates the real barrier height.

A second important reason for the non-ideal behaviors of real Schottky diodes are the influence of the resistance of the semiconductor and the metal over which part of the applied voltage  $V$  drops. These resistances are combined in the series resistance  $R_s$ . Furthermore, an ohmic surface or grain boundary conduction may exist for non ideal Schottky contacts, over which current flows. This is taken into account in the parallel resistance  $R_p$ . Additionally, the capacitance  $C$  of the depletion region has to be taken into account, which is done by an additional charging current  $I_C$ . A schematic circuit diagram of a real diode is shown in Figure 2.3.

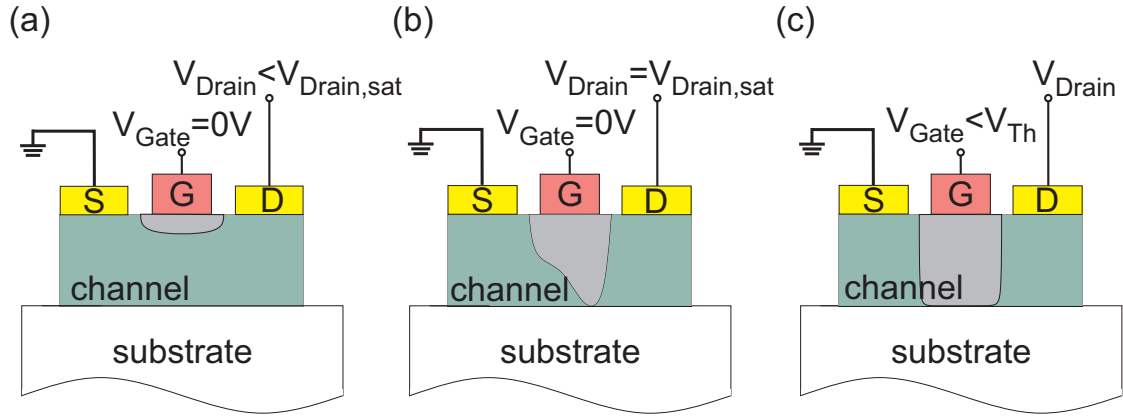
The equation for a current flow through a non-ideal diode with thermionic emission as dominating current transport can be written as:

$$I = A_0 A^* T^2 \exp\left(-\frac{\phi_{B,\text{eff}}}{k_B T}\right) \left[ \exp\left(e \frac{V - IR_s}{\eta k_B T}\right) - 1 \right] + \frac{V - IR_s}{R_p} + I_C . \quad (2.18)$$

**Ohmic Contacts** Ohmic contacts are characterized by a linear dependence of the current on the applied voltage. In the ideal case, they have a negligible contact resistance, which means that the voltage drop over the contact is small in comparison to the voltage drop over the semiconductor. Ohmic contacts can be realized by either a small work function of the metal compared to the electron affinity of the semiconductor ( $\phi_m < \chi$ ) or by such a high net doping (small depletion region width) that the current flow in the forward and the reverse regime is dominated by the series resistance. For the case of a high net doping density as origin of the ohmic contact, a tunneling current dominates the current flow. A high defect density within the semiconductor may also lead to the formation of an ohmic contact.

## 2.3 Field-Effect Transistors

A field-effect transistor consists of three contacts: a source, drain and gate contact. The current flow can be controlled by a current as is done in bipolar transistors or by a voltage as is done in field-effect transistors (FETs). In this work, field-effect transistors are investigated and all descriptions will therefore concentrate on this device type. The source and drain contact of FETs are ohmic, whereas the gate contact is a rectifying contact. If a Schottky barrier contact is used as gate contact, the device is called [! (!)3]MESFET. The field effect is achieved by a tuning of the depletion layer width by the voltage applied at the Schottky barrier contact. For  $pn$ -heterojunctions, it is called [! (!)3]JFET. The heterojunction leads to the formation of a depletion region and the working principle is similar as for MESFETs. If an insulator is brought between semiconductor and metal, the device is called [! (!)3]MISFET. A variation of the MISFET is the [! (!)3]MOSFET, where the insulator is realized by an oxide. The channel may be  $n$ - or  $p$ -type. FETs are unipolar devices, meaning they have only one majority carrier type. Most commonly used are MISFETs, which have the disadvantage that



**Figure 2.4:** Schematic side view of a FET and the varying extension of the depletion region in the channel for different applied voltages at the gate and drain contact.

part of the voltage drops over the gate insulator and therefore higher voltages are required for tuning of the current flow.

In this work investigations on MESFETs are discussed and therefore all descriptions will concentrate on this FET type.

**Working Principle** In the following descriptions, a  $n$ -type channel of thickness  $d$  shall be assumed and the gate contact shall be realized by a Schottky barrier contact. Source and drain contact are ohmic. In Figure 2.4 (a), a schematic side view of a FET is depicted. If no voltage is applied between source and drain ( $V_{\text{Drain}} = 0\text{V}$ ) and no voltage is applied at the gate ( $V_{\text{Gate}} = 0$ ), the transistor is in equilibrium. The depletion region below the gate contact is due to the Schottky metal-semiconductor contact.

If the source-drain voltage is continuously increased, while the gate contact is kept at  $0\text{V}$ , the current over the channel increases linearly. The depletion region expands due to the positive voltage applied at the drain contact, which leads to a reverse bias of the Schottky barrier contact. The voltage drops over the length of the channel and the depletion region deforms. When the depletion region reaches the substrate ( $w = d$ ) (compare Figure 2.4 (b)), the pinch-off is reached and the current through the channel saturates. The drain voltage at which the pinch-off occurs is called saturation voltage  $V_{\text{Drain,sat}}$ . If the drain voltage is further increased, the gate-drain diode is biased more negatively and at a certain point breakdown occurs, which leads to a strong increase of the source-drain current.

The source-drain current for a constant source-drain voltage can be tuned by the voltage applied at the gate. A reverse voltage at the gate leads to a decrease of the saturation current and a saturation at lower drain voltages. The reason for that is that by applying a negative bias at the gate contact, an extension of the depletion region can be achieved. For a certain applied gate voltage, called threshold voltage  $V_{\text{Th}}$ , the depletion region expands over the total channel thickness  $d$  (compare Figure 2.4 (c)).

The pinch-off voltage  $V_{\text{P}}$  is defined as the sum of the built-in and applied voltages at the

point, where the depletion region extents over the total channel thickness, as shown in Figure 2.4 (b).

**Static Calculations** If the gate length  $L$  is large compared to the channel thickness  $d$ , the depletion region width  $w$  can be calculated in dependence on the position  $x$  between source and drain using equation 2.6 and adding the voltage  $V(x)$ , which is caused by the voltage applied at the drain contact

$$w(x) = \sqrt{\frac{2\epsilon_r\epsilon_0}{eN_D} (V_{bi} - V_{Gate} + V(x))} . \quad (2.19)$$

This assumes the abrupt approximation, and a homogeneous doping. If  $w = d$ , it holds that  $V_{bi} - V_{Gate} + V_{Drain} = V_P$  and the pinch-off voltage can be written as

$$V_P = \frac{eN_D a^2}{2\epsilon_r\epsilon_0} . \quad (2.20)$$

In contrast, the threshold voltage  $V_{Th}$  is defined as the voltage that is required to be applied at the gate to deplete the channel for  $V_{Drain} > 0$  V.

Assuming current conservation, the current flowing from source to drain can be calculated by integrating the channel conductance along the channel width [38,52]. The current is then calculated as

$$I_{Drain} = I_P \left[ \frac{3V_{Drain}}{V_P} - 2 \left( \frac{V_{bi} - V_{Gate} + V_{Drain}}{V_P} \right)^{3/2} + 2 \left( \frac{V_{bi} - V_{Gate}}{V_P} \right)^{3/2} \right] . \quad (2.21)$$

With the current  $I_P$  is calculated as

$$I_P = \frac{e^2 \mu N_D^2 W a^3}{6L\epsilon_r\epsilon_0} , \quad (2.22)$$

where  $W$  is the gate width and  $\mu$  the electron mobility.  $I_P$  depends only on the material and geometrical properties and is therefore constant. In the case that  $V_{bi} - V_{Gate} + V_{Drain} \geq V_P$ , the drain current is independent of the drain voltage and is written as

$$I_{Drain} = I_P \left[ 1 - \frac{3(V_{bi} - V_{Gate})}{V_P} + 2 \left( \frac{V_{bi} - V_{Gate}}{V_P} \right)^{3/2} \right] . \quad (2.23)$$

If this equation is expanded around  $V_{Gate} = V_{Th}$ , equation 2.23 simplifies to

$$I_{Drain} \approx \frac{3I_P}{4V_P^2} (V_{Gate} - V_{Th})^2 . \quad (2.24)$$

The transistor may be either normally-on or normally-off. Normally-on transistors have a conductive channel and normally-off transistors have a non-conductive channel at 0 V gate voltage. A measure for normally-on or -off is the threshold voltage, which is  $V_{Th} < 0$  V or  $V_{Th} > 0$  V, respectively.

**Characteristic Parameters** The FETs in this work were characterized by three different current-voltage measurements: measuring (i) the gate-source and gate-drain diode characteristics, (ii) the transfer characteristic and (iii) the output characteristic. For (i) a variable voltage was applied at the gate contact and the resulting current flow was measured at the source and accordingly the drain contact. This measurement is important to verify the rectifying behavior of the gate contact, which is required to obtain a voltage tuning. The second measured characteristic is the transfer characteristic (ii), which is measured by connecting the source contact to ground and applying a constant positive voltage at the drain contact (typically 2 V in this work). The voltage at the gate contact is varied in a predefined voltage range and the resulting drain current and gate leakage current are measured. The drain current should, if a field-effect exists, be tunable by the voltage applied at the gate contact. The gate voltage is chosen in such a way that for small or negative voltages, the channel is depleted and no current flow is measured over the channel and for high positive voltages, the depletion region is completely dissipated and the saturation current flows. The transfer characteristics are used for the determination of the characteristic parameters of the transistor. A third measurement is the output characteristic (iii), in which the drain voltage is varied between 0 V and higher positive voltages for a constant gate voltage. This measurement is repeated for different gate voltages.

From the transfer characteristics different parameters of the transistor can be calculated. One parameter is the drain current on-to-off ratio, which is calculated as the maximum drain current divided by the minimum drain current during the transfer measurement

$$\text{on-to-off ratio} = \frac{\max(I_{\text{Drain}})}{\min(I_{\text{Drain}})} . \quad (2.25)$$

The sub-threshold swing  $S$  gives the minimum voltage that is required to switch the drain current by one decade

$$S = \min \left( \left[ \frac{d \log_{10}(I_{\text{Drain}})}{dV_{\text{Gate}}} \right]^{-1} \right) . \quad (2.26)$$

The theoretical minimum of the sub-threshold swing can be calculated by  $\ln(10) \frac{k_B T}{e}$ , which is  $\approx 60 \text{ mV dec}^{-1}$  at room temperature.

Using equation 2.24, the threshold voltage can be determined by a linear fit on the plot of  $\sqrt{I_{\text{Drain}}}$  in dependence on the gate voltage. Another important parameter is the maximal transconductance  $g_{\text{max}}$ , which is defined as the maximum of the derivative of the drain current with respect to the gate voltage:

$$g_{\text{max}} = \max \left( \frac{dI_{\text{Drain}}}{dV_{\text{Gate}}} \right) = \frac{e N_t d \mu_{\text{Ch}} W}{L} . \quad (2.27)$$

It has to be considered that non-idealities often lead to smaller values of  $g_{\text{max}}$  obtained from the characteristics [53] as compared to the values obtained by a calculation from the geometric and electrical parameters of the device. Using equation 2.27 and the net doping density  $N_t$ ,

the channel (field-effect) mobility  $\mu_{\text{Ch}}$  can be estimated for the investigated devices.

## 2.4 Inverter

An inverter is a simple logic element, which can switch between two states: e.g. on and off or 1 and 0. It can, in its simplest form be realized by a series connection of a switch  $S$  and a resistance  $R_L$  as shown in Figure 2.5 (a). If the switch is open, the operating voltage  $V_{\text{DD}}$  drops over the switch and  $V_{\text{out}} = V_{\text{DD}}$ . If the switch is closed, the ground potential is applied at the output and  $V_{\text{out}} = 0 \text{ V}$  is measured. The switch is typically controlled by an input voltage  $V_{\text{in}}$ .

In this work two identical FETs are used instead of a switch and a resistance. In the following, two different inverter designs are shortly explained: the simple inverter design and the [! ([!])3]SDFL inverter design.

A more detailed discussion on inverters can be found in [54].

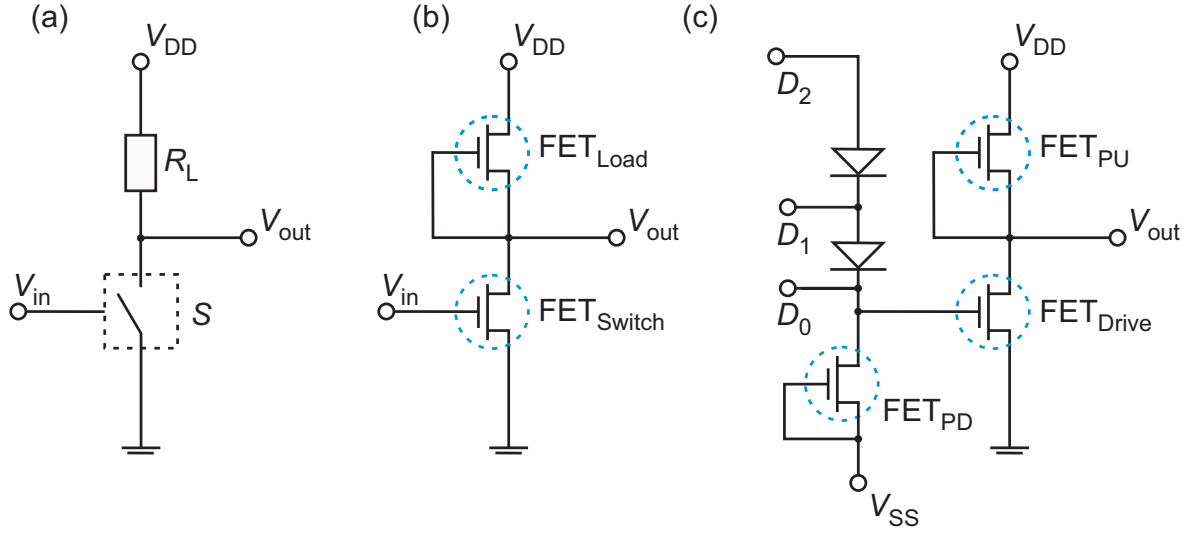
**Simple Inverter** The circuit diagram of a simple inverter is shown in Figure 2.5 (b). An input voltage is applied to the gate contact of the switch transistor  $\text{FET}_{\text{switch}}$ , whose source contact is connected to ground. The drain contact of the switch transistor is short-circuited with the source and gate contact of the load transistor  $\text{FET}_{\text{load}}$ . The output voltage is measured at this (combined) contact. Due to the shortening of the gate and source contact of the load transistor, this transistor always works at the same point. The operating voltage is supplied at the drain contact of the load transistor.

For a negative input voltage, the channel of the switch transistor is depleted and has a large resistance compared to the load transistor. The output voltage is therefore approximately the operating voltage  $V_{\text{out}} \approx V_{\text{DD}}$ .

In contrast, a positive input voltage at the switch transistor leads to a reduction and subsequent vanishing of the depletion region in this device. The switch transistor therefore has a lower resistance than the load transistor in this case, and the output voltage becomes, as for the closed switch, nearly zero  $V_{\text{out}} \approx 0$ .

The inverters investigated here switch between 0 V as low level and  $V_{\text{DD}}$  as high level, which is in contrast to a full inverter, where an exchange of two complementary voltage levels is achieved.

**Schottky Diode FET Logic Inverter** The basic working principle of this inverter type is the same as for the simple inverter. The difference lies in a pull down transistor  $\text{FET}_{\text{PD}}$  and a variable number of diodes (zero to two in this design), which are connected in front of the gate contact of the switch transistor of the simple inverter as shown in Figure 2.5 (c). The load transistor is now called pull-up transistor  $\text{FET}_{\text{PU}}$  and the switch transistor is called drive transistor  $\text{FET}_{\text{Drive}}$ .



**Figure 2.5:** Equivalent circuit of an inverter consisting of a switch and a resistance (a) and of two transistors (b). In (c) the equivalent circuit of an inverter in [! ([!3]SDFL design is shown.

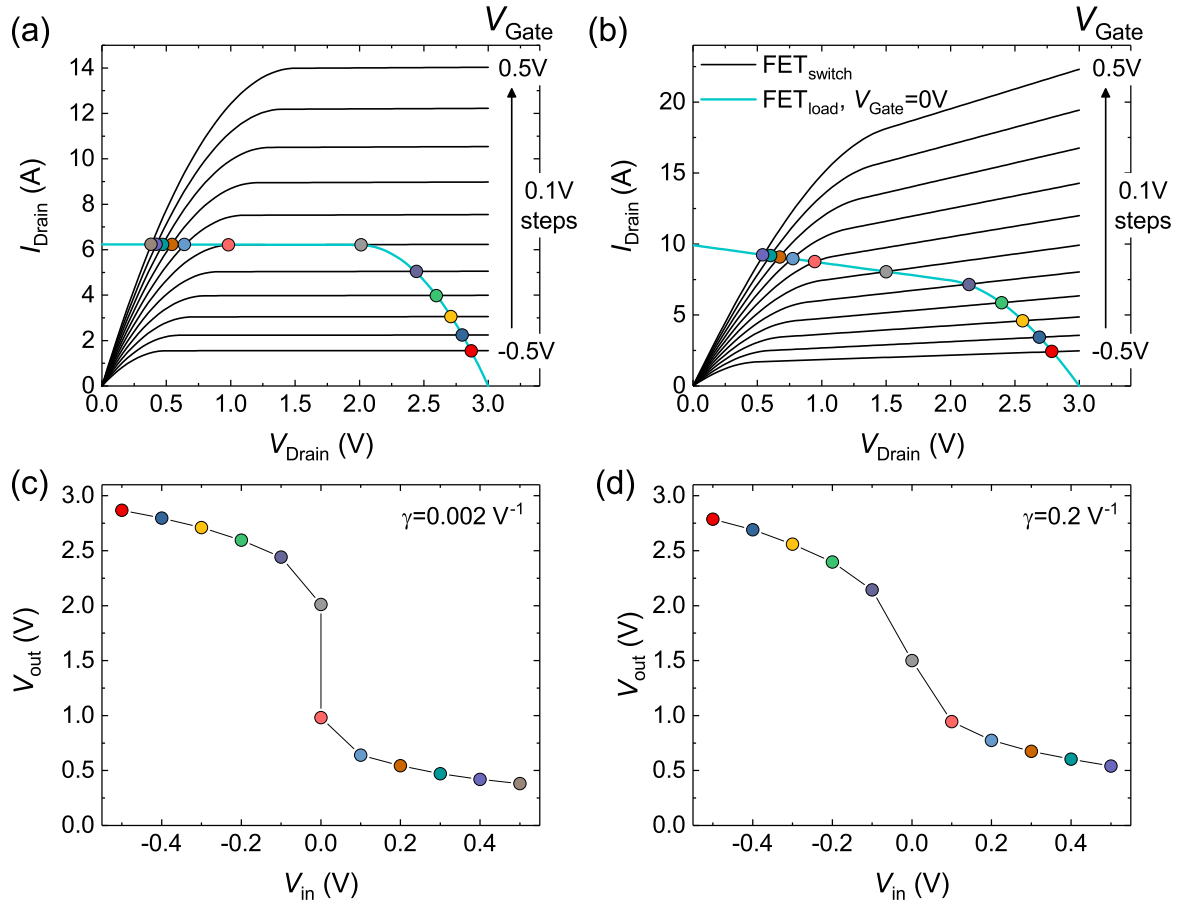
The input signal of the inverter is strongly influenced by the pull-down transistor, at which a negative constant voltage is applied. This voltage, called supply voltage  $V_{SS}$  is chosen in such a way that the pull-down transistor works in saturation. Typically a voltage of  $V_{SS} = -2\text{ V}$  is chosen. The gate length of the pull-down transistor is chosen in such a way, that it is  $1/2$  the gate length of the drive and pull-up transistor to ensure a smaller current flow and a smaller voltage drop over this transistor.

In the design used in this work, it is possible to chose between zero diodes  $D_0$ , one diode  $D_1$  and two diodes  $D_2$  as input port. In the case of one and two diodes, the pull down transistor works as current supply for the diodes. The combination of pull-down transistor and diodes is called level-shifter.

The level-shifter leads to a voltage shift  $V_{\text{shift}}$  of the gate voltage of the switch transistor  $V'_{\text{in}}$  by the voltage drop across the  $N$  diodes, which is  $V_x$  per diode. This can be formulated as  $V'_{\text{in}} = V_{\text{in}} - NV_x$ . As a result, the voltage transfer characteristic of the [! ([!3]SDFL inverter is shifted to positive input voltages for one and two diodes.

If this design is adopted in such a way that the level-shifter is connected behind the simple inverter, the design is called [! ([!3]FL. In this case, a  $y$ -axis voltage shift of the output voltage is achieved. This is used to ensure positive and negative input voltages of a subsequent inverter. A detailed description on this design, which was adopted from the GaAs-MESFET technology is given in reference [54,55].

**Voltage Transfer Characteristics of an Inverter** The voltage transfer characteristic of an inverter can be directly related to the output characteristic of the load and switch transistors. In this thesis, both FETs are identical and therefore their output characteristics



**Figure 2.6:** Simulation of output characteristics of a MESFET for (a)  $\gamma = 0.002 \text{ V}^{-1}$  and (b)  $\gamma = 0.2 \text{ V}^{-1}$  and the resulting voltage transfer characteristics, which are shown in (c) and (d).

are also assumed to be identical for simplicity<sup>3</sup>.

To construct the voltage transfer characteristic of a simple inverter, the output characteristics of the switch transistor are plotted. The output characteristic of the load transistor at  $V_{\text{Gate}} = 0 \text{ V}$  is mirrored on the  $x$ -axis in such a way, that it starts at  $V_{\text{DD}}$  (see Figure 2.6 (a,b)). Following Kirchhoff's law, the drain voltages and the operating voltage are connected by

$$V_{\text{out}} = V_{\text{Drain-Source,switch}} = V_{\text{DD}} - V_{\text{Drain-Source,load}} . \quad (2.28)$$

The intersections of both output characteristics, where both FETs carry the same current, give the working points of the inverter, marked by the dots in Figure 2.6 (a-d):

$$I_{\text{Drain,switch}}(V_{\text{in}}, V_{\text{Drain-Source,switch}}) = I_{\text{Drain,load}}(0, V_{\text{Drain-Source,load}}) , \quad (2.29)$$

if gate currents are neglected. As both transistors have the same resistance at  $V_{\text{Gate,switch}} = V_{\text{Gate,load}} = 0 \text{ V}$ , the switching point of the inverter is at  $V_{\text{in}} = 0 \text{ V}$  in the ideal case.

<sup>3</sup>However, a certain variance is always present in real devices.

**Table 2.1:** Fixed simulation parameters used during the simulation with the *Simulink* tool of *MATLAB*.

Parameter	$\Sigma$ $\text{S V}^{-1}$	$I_{\text{sat}}$ A	$T$ $^{\circ}\text{C}$	$R_{\text{ohmic}}$ $\Omega$	$C_j$ nF
	6.2	$5 \times 10^{-11}$	25	$1 \times 10^{-5}$	0.3

The output characteristics, and all further data in this section, were simulated using the *Simulink* tool by *MATLAB* in the layout of a simple inverter. Two JFETs with tunable transconductance  $\Sigma$ , saturation current  $I_{\text{sat}}$ , threshold voltage  $V_{\text{Th}}$ , saturation factor of the output characteristics  $\gamma$ , temperature  $T$ , ohmic contact resistance  $R_{\text{ohmic}}$  and junction capacitance  $C_j$  were used. All parameters that were kept fixed during the simulations are listed in Table 2.1. The equivalent circuit used for the simulation is depicted Figure A1 in the Appendix. For the modeling of inverters, it does not matter whether a JFET or MESFET is used as model block, as both devices are assumed to be unipolar and all characteristic properties of the FET could be adjusted within the program.

In the ideal case, the output characteristics exhibit a saturation of the drain current for  $V_{\text{Drain}} > V_{\text{Drain,sat}}$ . This case is shown in Figure 2.6 (a). The resulting voltage transfer characteristic of the inverter is infinitely steep in the transition regime and therefore ideal as shown in Figure 2.6 (c). If the drain current does not saturate, but rather exhibits a finite slope, the resulting voltage transfer characteristics become non-ideal. This effect is described by the parameter  $\gamma$  in the simulations, which can be obtained from a linear fit on the finite slope of the output characteristics for  $V_{\text{Drain}} > V_{\text{Drain,sat}}$ . The equation for the linear fit is

$$I_{\text{Drain,sat}} = a + bV_{\text{Drain}} , \quad (2.30)$$

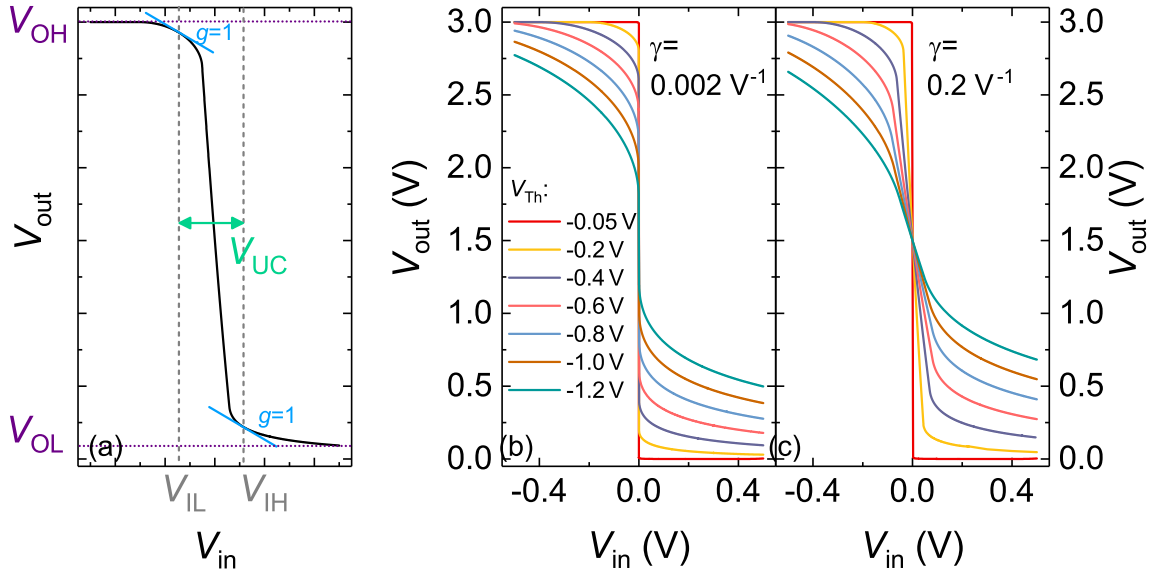
where  $a$  is the intercept with the  $y$ -axis and  $b$  the slope.  $I_{\text{Drain,sat}}$  has a finite slope in this case. The parameter  $\gamma$  is defined as one divided by the intercept with the  $x$ -axis and therefore  $\gamma = |-b/a| \text{ V}^{-1}$ . In Figure 2.6 (b), the output characteristics are depicted for  $\gamma = 0.2 \text{ V}^{-1}$ . The finite slope of the saturation current is very well visible. A voltage transfer characteristic for the case of a finite slope of the saturation current is shown in Figure 2.6 (d). If one compares the voltage transfer characteristics for  $\gamma = 0.002 \text{ V}^{-1}$  and  $\gamma = 0.2 \text{ V}^{-1}$ , the less steep increase of the voltage transfer characteristics for a larger  $\gamma$  is immediately visible.

In literature the value  $\gamma$  is typically replaced by the drain output resistance  $r_0$  [54]

$$r_0 = \frac{1}{\gamma I_{\text{Drain}}} . \quad (2.31)$$

The additional drain current is interpreted as current flowing through a drain output resistor  $r_0$ .

The influence of the transconductance parameter and the saturation current is visible in the logic off regime only and is not shown in this work. A non-ideality in these parameter leads to



**Figure 2.7:** Characteristic parameters of an inverter (a) and simulation of voltage transfer characteristics for different threshold voltages and a factor  $\gamma$  of  $0.002 \text{ V}^{-1}$  (b) and  $0.2 \text{ V}^{-1}$  (c).

gate lag currents and therefore an increase of the output voltage for positive input voltages. If the transconductance is smaller than a critical value, which is dependent on the geometry and the threshold voltage, it is no longer possible to achieve the operating voltage for negative input voltages.

Inverters are typically described by a number of parameters. The gain  $g$ , which is calculated as

$$g = -\frac{\partial V_{out}}{\partial V_{in}} \quad (2.32)$$

is used to determine the steepest point of the voltage transfer characteristic, i.e. the point with maximum gain. This point is called peak gain magnitude *pgm*. Additionally, the uncertainty level is determined as the difference in voltage for the two points where the gain is 1. The input and output voltage for which the point  $g = 1$  is reached are called input high voltage  $V_{IH}$  and input low voltage  $V_{IL}$  for the input voltage and output high voltage  $V_{OH}$  and output low voltage  $V_{OL}$  for the output voltage as depicted in Figure 2.7 (a). The uncertainty level  $V_{UC}$  is calculated as the difference of input high and low voltage  $V_{UC} = V_{IH} - V_{IL}$ . In the optimal case, the inverter switches between  $V_{DD}$  and  $0 \text{ V}$ . In this case, the logic swing is equal to the operating voltage. In the non-ideal case, the logic swing is smaller and calculated as  $V_{OH} - V_{OL}$ .

In Figure 2.7 (b,c), the voltage transfer characteristic for two different values of  $\gamma$  and a variation of the threshold voltage are simulated. A requirement of the simple inverter set-up is that the threshold voltage has to be close to zero or below for the inverters to work well. This can be seen very well in the simulated data. The more negative the threshold voltage becomes, the smaller the logic swing becomes. Additionally, it is visible that for the non

ideal case, where  $\gamma = 0.2 \text{ V}^{-1}$ , the slope of the voltage transfer characteristics increases with increasing threshold voltage.

For positive input voltages very close to 0 V, a voltage inversion is observed for the device. An increase of the threshold voltage to higher positive voltages leads to a lowering of the output high voltage and therefore of the logic swing. This is due to a high resistance of switch and load transistor in the regime  $V_{\text{in}} < 0 \text{ V}$ , which leads to a voltage drop over the switch transistor as well as over the load transistor. Additionally, the switching point of the inverter shifts to higher input voltages due to the higher threshold voltage of the transistors.

## 2.5 Inverter Chain and Ring Oscillator

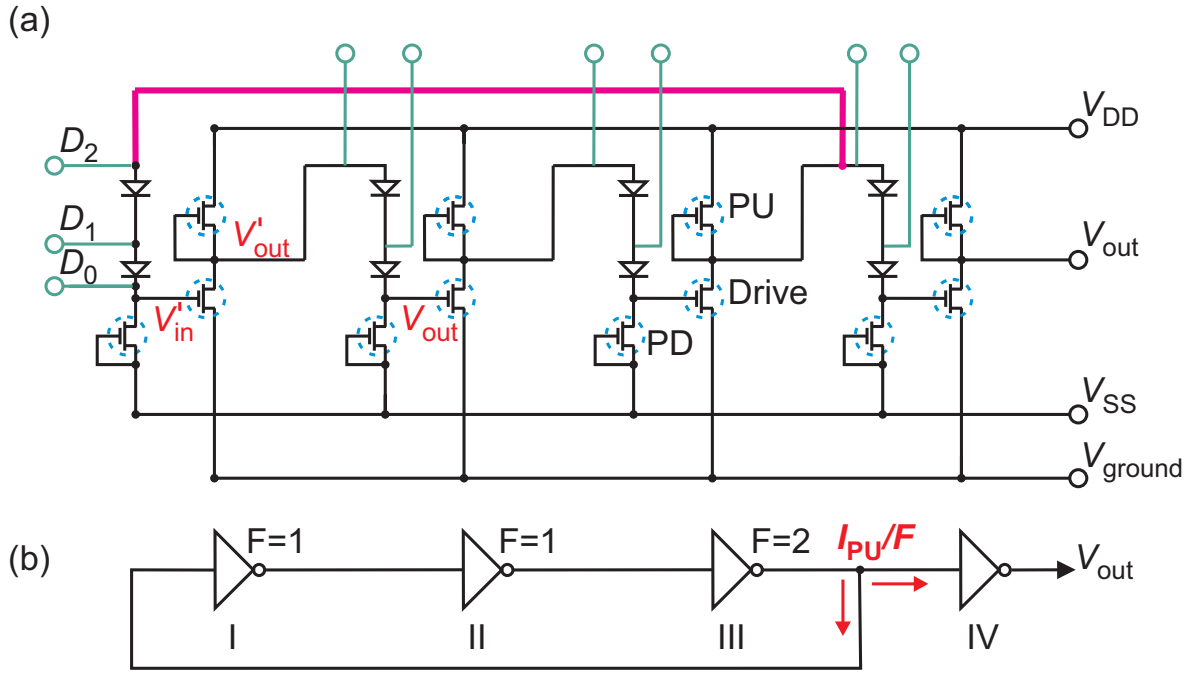
A further step towards integrated circuits is the series connection of inverters, which is called inverter chain or ring oscillator, depending if a shortening of the output of the last inverter with the input of the first inverter of the circuit is performed or not. An exemplary use of ring oscillators is as test structures for the propagation delay in logic elements [56, 57].

**Inverter Chain** In Figure 2.8 (a) an inverter chain is drawn. The pink line, which represents the connection of the circuit to a ring oscillator, has to be erased for the inverter chain. The green lines denote the possible measurement contacts. If the signal is measured between  $D_2$  and  $V_{\text{out}}$ , it is equal to the [! (!)3]SDFL design and a shift of the signal on the  $V_{\text{in}}$ -axis is achieved, whereas if the signal is measured between  $V_{\text{in}}$  and  $V_{\text{out}}$  the layout corresponds to a FET logic inverter and the signal is shifted on the  $V_{\text{out}}$ -axis. Therefore it is possible to shift the output signal of an inverter in such a way that negative output voltages are achieved and the next inverter can be driven.

Each inverter leads to an inversion of the signal of  $180^\circ$ . Thus the first inverter leads to the expected signal of high output for negative input voltages and low output for positive input voltages. If the signal is read-out after the second inverter, a low output signal is measured for negative input voltages and a high output level for positive input voltages, and so on. Therefore, an odd number of inverters leads to the same signal orientation as obtained for one inverter.

**Ring Oscillator** A ring oscillator is a cascading of an odd number of inverters, which are shortened in such a way, that the signal of the last inverters is fed into the first inverter. An additional inverter is used to read out the signal. A more detailed explanation on ring oscillators can be found in [58, 59]. The descriptions and derivations given in this chapter follow the argumentation by Klüpfel *et al.* [58].

Three conditions have to be fulfilled to enable the detection of an oscillation:  $V_{\text{SS}}$  has to be chosen in such a way that the pull down transistor works in saturation and acts as current supply,  $V_{\text{DD}}$  has to exceed the voltage shift of the level shifter and last but not least, a constant ground potential has to be applied to the circuit.

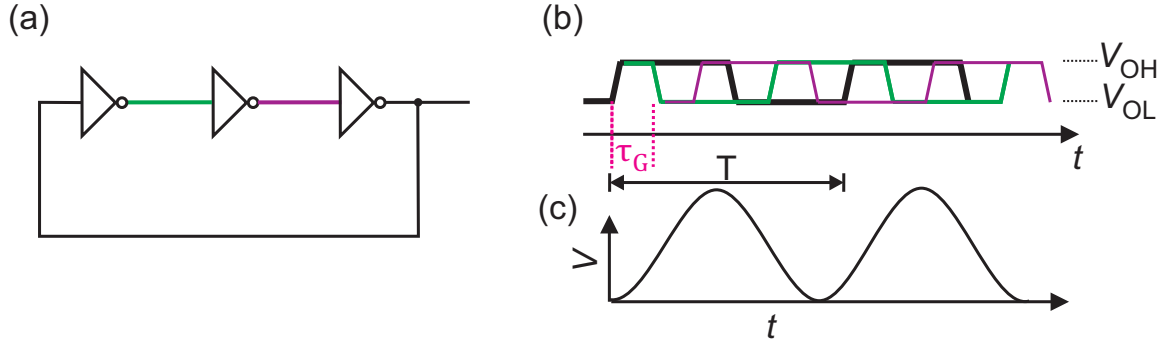


**Figure 2.8:** Schematic drawing of an (a) inverter chain (without the pink line) and a ring oscillator (with pink connection) and (b) schema of a ring oscillator with three stages and an out-coupling inverter stage. The pull-up FET is denoted by PU, the pull-down FET by PD and the driving FET by Drive.

A schematic drawing is shown in Figure 2.8 (a), where the pink line represents the shortening of the circuit to form a three stage ring oscillator. Another important parameter is the fan-out  $F$ , which denotes how many inverter stages have to be driven by any given inverter stage. For the first two inverter stages the fan-out is  $F = 1$ . For the third inverter stage it is  $F = 2$ , as the out-coupling as well as the inverter stage I have to be driven by this inverter. This is important as an inverter with  $F = 2$  has to supply the current to load the gate capacitance of two following devices in contrast to just one as is the case for  $F = 1$ . A more detailed description will follow below.

The signal oscillation in the circuit arises due to a propagation delay of the single inverter stages. The number of inverters therefore directly influences the oscillation frequency. A schematic drawing of the high and low levels of the inverter stages and the propagation delay for a three stage ring oscillator are shown in Figure 2.9 (a,b). At inverter stage I, the signal is original. At inverter stage II, it exhibits a delay  $\tau_G$  and the signal is inverted. A further delay is observed for inverter stage III, where the signal has the original orientation again and has a delay of  $2\tau_G$ . This signal is re-fed into inverter stage I, where - in combination with the original signal of inverter stage I - it causes an oscillation.

For GaAs based [! (!)3]SDFL ring oscillators, Helix *et al.* [59] derived a relation that enables the estimation of the gate delay  $\tau_G$  based on measurable quantities of the FETs and inverters



**Figure 2.9:** Three stage ring oscillator with signal paths marked in black, green and pink and (b) the high and low levels of each inverter stage with the time delay  $\tau_G$  depicted for the measurement time  $t$ . In (c) the resulting voltage oscillation is schematically drawn.

comprising the ring oscillator. This equation was formulated by Klüpfel *et al.* [58] to

$$\tau_G = \frac{C_G \Delta V F}{I_{PU}} , \quad (2.33)$$

where  $C_G$  is the gate capacitance, which can be determined by [! ([!])3]QSCV measurements.  $\Delta V$  is the logic swing of the inverter and  $F$  the fan-out. The pull-up current  $I_{PU}$  is the on-current of the pull-up transistor. The current available for recharging the next inverter gate is  $I_{PU}/F$ . The out-coupling inverter stage is used to prevent the load with an additional capacitance of the last inverter stage in the ring oscillator. The charge  $Q = C_G \Delta V$  required to switch the driving FET must be provided by the pull-up current of the previous inverter. If this additional out-coupling inverter stage is not used, the frequency can be determined by the time delay of each inverter step and is

$$f = \frac{1}{2N\tau_G} . \quad (2.34)$$

The oscillation frequency of an  $N$  stage ring oscillator with out-coupling inverter stage can be estimated by

$$f = \frac{1}{2(N+1)\tau_G^{F=1}} , \quad (2.35)$$

where  $(N+1)$  is due to  $N-1$  inverter stages with fan-out  $F=1$  and one inverter stage with  $F=2$ . The thus obtained oscillation frequency can be compared to the measured oscillation frequency. For [! ([!])3]CMOS based ring oscillators, typically, an operating voltage dependence is expected for the oscillation frequency of ring oscillators  $f \propto 1/V_{DD}$  [60].

For the layout used in this thesis, the gate voltage of the driving FET  $V_{\text{Gate;drive}}$  has a lower limit of  $V_{SS}$ , which is by definition the lowest voltage in the circuit. The upper limit of  $V_{\text{Gate;drive}}$  is given by the pull-up current of the previous inverter, which has to load the gate capacitance. This current flows through the two diodes of the level-shifter, which in turn cause a voltage drop of  $V_{\text{shift}}$ . If the level shifter diodes and gate diodes have identical dimensions, this leads to a maximum voltage drop across the gate diode of  $V_{\text{shift}}/3$ . And therefore the

expression  $\Delta V$  can be reformulated as

$$\Delta V = \frac{V_{\text{shift}}}{3} - V_{\text{SS}} , \quad (2.36)$$

which is independent of  $V_{\text{DD}}$  [58]. The oscillation frequency does therefore, in contrast to [! ([!)]3]CMOS ring oscillators, not change with a variation of  $V_{\text{DD}}$  exceeding the critical value [58, 60].

Another important factor is the power consumption  $P_{\text{DD}}$  of the ring oscillator. It is approximated as

$$P_{\text{DD}} = I_{\text{PU}} V_{\text{DD}} . \quad (2.37)$$

A low power consumption is desired, which can be achieved by either low pull-up current or low required operating voltages. The second is preferable, as low pull-down currents lead to an increase of the time delay and therefore a reduction of the oscillation frequency as can be seen in equation 5.4.

# Chapter 3

## Methods

### 3.1 Growth and Structuring Techniques

#### 3.1.1 Pulsed Laser Deposition

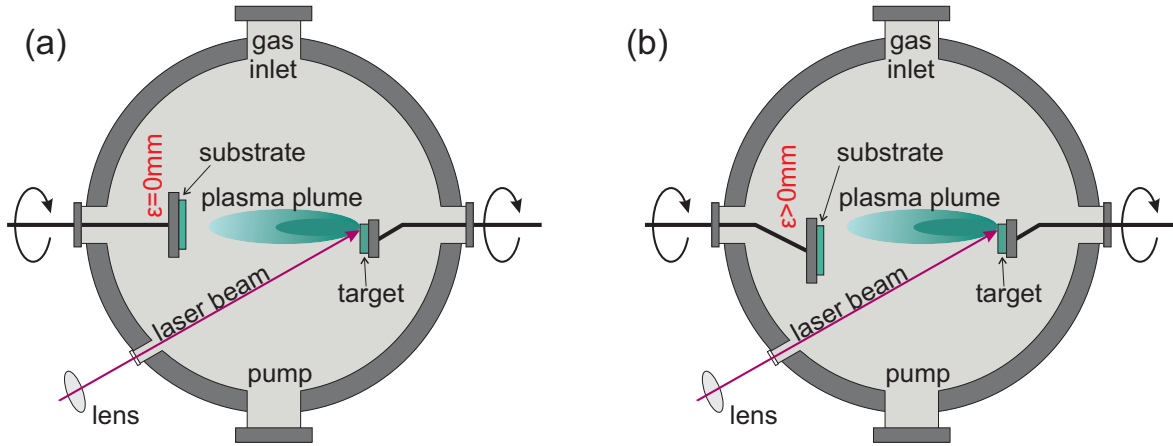
An advantageous method for the quick growth of thin films smaller than 8 inch is [! (!)3]PLD. The working principle of this method is the ablation of a target material by a laser inside a vacuum chamber, the ablated material in turn forms a plasma plume and subsequently condenses on a substrate, mounted opposite of the target. In this work, a ceramic target was ablated using a *LPX305* krypton-fluoride excimer laser by *Lambda Physik* with a wavelength of 248 nm. The laser has a pulse duration of 25 ns and an energy of 600 mJ. It is focused by a lens on a ceramic target, where the energy density is approximately  $2 \text{ J cm}^{-2}$ . The ablated material, consisting of atoms, ions and clusters, expands perpendicular to the target surface and absorbs part of the incoming laser light. This leads to an excitation of the ablated particles and atoms and thus the formation of a plasma plume. Subsequently, the ablated material nucleates on the substrate and forms the thin film. The chosen background gas and background pressure have a large influence on the extension of the plasma plume. In Figure 3.1, a schematic drawing of a PLD chamber is shown. The distance between target and substrate is 10 cm in the deposition chamber used in this work. The offset  $\epsilon$  between the center of the substrate and the target<sup>1</sup> can be varied by a shift of the substrate. For the deposition of single composition  $10 \times 10 \text{ mm}^2$  thin films, it was chosen as  $\epsilon = 10 \text{ mm}$ . The target as well as the substrate are rotated around their center during the deposition, as is shown schematically in Figure 3.1.

The targets used in this thesis were fabricated from ZnO and SnO<sub>2</sub> powders by *Alfa Aesar*. The powders have purities of 99.9978% (ZnO) and 99.9% (SnO<sub>2</sub>). Single composition targets were fabricated with a composition of 1 : 2 and 2 : 1 ZnO : SnO<sub>2</sub> by Gabriele Ramm<sup>2</sup>. For

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<sup>1</sup>Not the center of the target is aligned directly opposite the substrate center at  $\epsilon = 0 \text{ mm}$ , but the spot on the target where the laser impacts.

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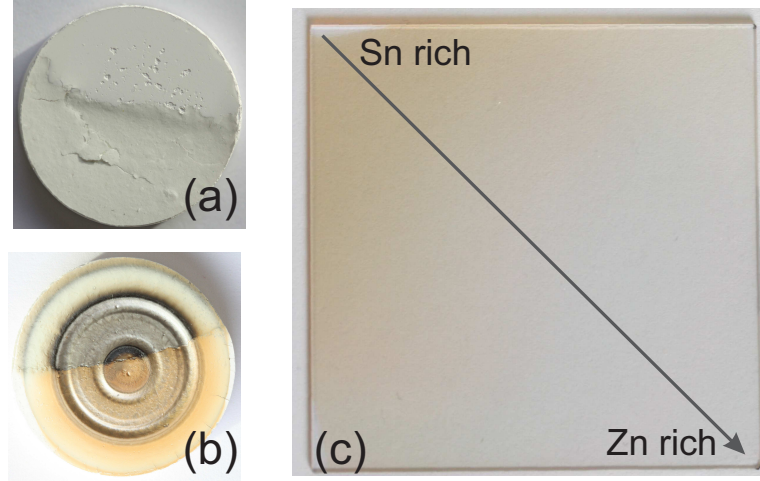
**Figure 3.1:** Schematic drawing of a [! (!)3]PLD chamber with an offset  $\epsilon$  between the target and the center of the substrate of 0 mm (a) and  $> 0$  mm (b).

this, the powders were mixed in the desired ratio, pressed into a pallet and subsequently annealed at  $1150^\circ\text{C}$  for 12 h. In this work, an amorphous thin film growth was desired and therefore all depositions were performed at room temperature. Oxygen with a pressure  $p_{\text{oxygen}} = 0.025 - 0.035\text{ mbar}$  was chosen as process gas. The pulse frequency and repetition rate were chosen between 5 and 15 Hz and 10 000 pulses, respectively. The thin film growth by [! (!)3]PLD was conducted by Peter Schlupp<sup>3</sup>.

## Continuous Composition Spread Approach for Pulsed Laser Deposition

An extension of the above described [! (!)3]PLD process is the [! (!)3]CCS approach. It enables the investigation of a large range of cation compositions of a ternary compound by one deposition step. It is therefore a time and energy saving method for a sampling of the influence of the cation composition of compounds on the thin film properties [61]. To achieve the composition gradient, a lateral offset  $\epsilon$  between target and substrate, a synchronized rotation of target and substrate and a segmented target are required. This is exemplary shown in Figure 3.1 (b). The offset was chosen as  $\epsilon = 24\text{ mm}$  for the deposition of  $50 \times 50\text{ mm}^2$  [! (!)3]CCS thin films. The pulse frequency has to be chosen sufficiently small to avoid the growth of stacked ZnO and SnO<sub>2</sub> layers. Calculations from the growth rate yielded that for a pulse frequency of 5 Hz less than one atomic layer is grown of each material per rotation. Previous reports suggested a thermal annealing of the thin films after the deposition to ensure an intermixing of the layers [62-65]. However, this was not desired for the growth of amorphous [! (!)3]ZTO thin films in this work, where a room temperature deposition was requisitioned. The low pulse frequency ensures a homogeneous thin film. A photograph of an exemplary resulting thin film is depicted in Figure 3.2 (c). The tin rich side has a brown tinge, whereas

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**Figure 3.2:** A segmented target after the fabrication (a) and after the [! (!)3]PLD process (b). A resulting continuous composition spread thin film is depicted in (c).

**Table 3.1:** Composition of the target segments S1 and S2 and resulting cation composition range of the thin films.

sample	S1	S2	film composition Zn/(Zn+Sn)
	at% ZnO/SnO <sub>2</sub>	at% ZnO/SnO <sub>2</sub>	
thin film I	40/60	5/95	0.12 – 0.29
thin film II	33/67	67/33	0.34 – 0.54
thin film III	47/53	76/24	0.46 – 0.57
thin film IV	60/40	95/5	0.56 – 0.72

the zinc rich side is transparent.

The fabrication of the segmented targets shall be discussed only briefly here, a detailed discussion of the fabrication of the required targets is given in [18, 66] [E1]. In previous experiments, where crystalline film growth was desired, the high temperature depositions of [! (!)3]CCS thin films was performed using a segmented target consisting of two individual target halves [61, 67-69]. However, for amorphous [! (!)3]ZTO this approach led to a high droplet density on the resulting thin films, which is likely due to a droplet ablation at the interface of the target halves. Therefore, experiments were performed to achieve the different target halves within one target (compare Figure 3.2 (a,b)). The most expedient method, regarding the thin film smoothness, was the fabrication of several targets with each covering a smaller cation composition range. Therefore four individual segmented targets were fabricated to cover the composition range from 0.12 to 0.72 Zn/(Zn+Sn). The target segment compositions and resulting thin film compositions are listed in table 3.1. All targets were annealed in ambient atmosphere for 12 h to 24 h at a temperature of 1150°C. The pulse frequency and repetition rate were chosen between 5 and 15 Hz and 50 000 pulses, respectively.

### 3.1.2 Sputtering Deposition

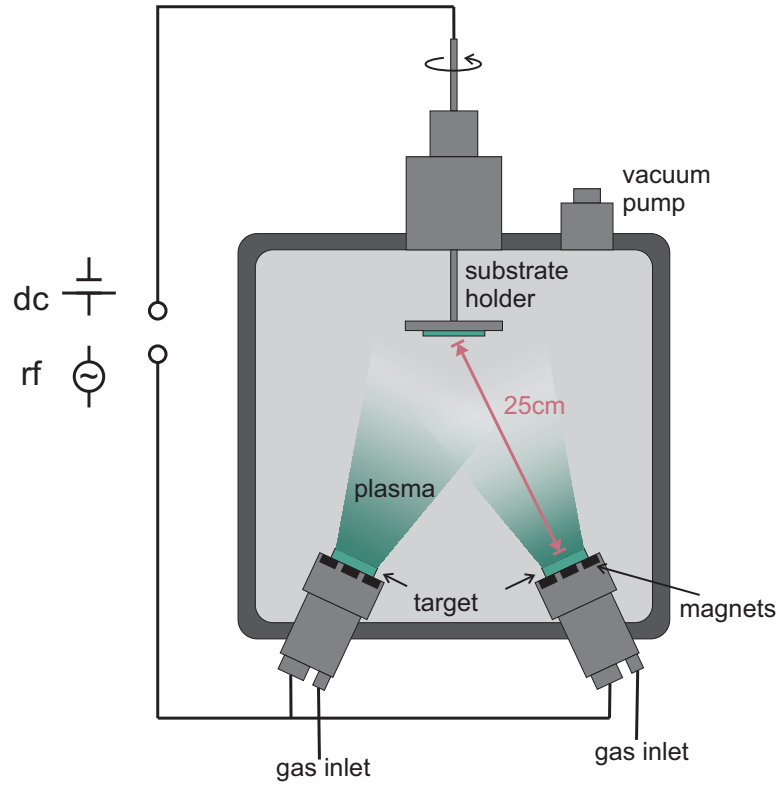
#### Direct Current-Sputtering

Sputtering deposition is a widely used technique for the fabrication of homogeneous and smooth thin films. It may, for example, be employed in roll-to-roll fabrication techniques for the fabrication of electrodes for flexible solar cells [70]. The general working principle of sputtering is based on the ablation of target material by the impact of highly energetic species, e.g. ionized atoms. Therefore, a vacuum chamber is filled with a process gas at a low pressure. Target and substrate are mounted on opposite sides of the chamber and a voltage is applied between them. For [! ([!])3]dc-sputtering, the metallic target forms the cathode and the substrate (holder) the anode and the applied voltage is constant. Due to random movement and collisions, inert gas atoms are ionized. Positively charged ions are accelerated towards the target. On the way towards the target they collide with other gas atoms and ionize them. The applied voltage between target and substrate leads - for small chamber pressures - to a glow discharge and the formation of a plasma. Once the ionized gas atoms hit the target, they lead to an ejection of target atoms and secondary electrons by bombardment. The secondary electrons contribute to a further ionization of the gas, whereas the ablated target atoms move perpendicularly away from the target surface and subsequently condensate on the substrate or lead to a re-sputtering of atoms from the substrate or the already grown thin film. The process may be performed in an inert or reactive gas atmosphere. In this work, argon was used as inert gas and oxygen or oxygen/argon gas mixtures were used for reactive sputtering. To increase the growth rate, the [! ([!])3]dc-sputtering process can be modified by placing magnets below the target. It is then called [! ([!])3]dc magnetron sputtering. The magnetic field forces the (secondary) electrons on a circular path above the target due to Lorentz force. This higher local electron density leads to a higher collision rate and therefore a higher ionization rate. This technique allows for smaller chamber pressures which in turn leads to less scattering of the target atoms on the background gas and therefore a higher growth rate. Sputtering at lower voltages is possible [71] and a circular ablation crater appears on the target, which is typical for magnetron sputtering.

The [! ([!])3]dc-sputtering may be used for metallic targets only and was used for the deposition of metals and, under an reactive atmosphere, metal oxides in this work. The target substrate distance is 4cm for the deposition chamber used here and a rotation of the substrate is possible.

#### Long-Throw rf Magnetron Sputtering

For ceramic targets, [! ([!])3]dc-sputtering is not possible, as the ion current leads to a charging of the insulating target. An alternative method, which allows for the sputtering of ceramic targets is [! ([!])3]rf-sputtering, where an alternating voltage is applied at the cathode. A typical frequency of 13.56 MHz is used. The alternating voltage prevents a charging of the



**Figure 3.3:** Schematic drawing of the sputtering chamber used for long-throw magnetron rf and dc-sputtering of thin films.

target because the heavy ions that would lead to charging are not able to follow this high frequency. This enables the sputtering of (semi-) insulating targets. Another advantage is the higher ionization rate due to the oscillation of electrons, which makes even lower process pressures possible. In this work, long-throw rf magnetron sputtering was used, which is characterized by a comparably large target substrate distance. This large distance prevents the heating of the substrate by the plasma, which is advantageous for the deposition of amorphous, room temperature deposited thin films [95]. Moreover, the small process pressures (typically  $10^{-3} - 10^{-2}$  mbar) lead to a smaller scattering rate and therefore an ideally perpendicular incoming of the target atoms on the substrate, which leads to a better homogeneity of the thin film layer thickness [94]. The large distance between target and substrate also leads to a thermalization or filtering out of highly energetic target particles. This leads to more homogeneous thin films with a smaller surface roughness. A disadvantage is the small growth rate of the deposited thin films compared to set-ups with smaller target substrate distances.

In this work, long-throw magnetron sputtering was used for the deposition of the ZTO thin films. A schematic image of the chamber by *Mantis Deposition* is shown in Figure 3.3. The target substrate distance is 25cm and the substrate holder is rotated during the deposition. The gas flow, chamber pressure and gas type can be varied (even continuously) in this chamber.

### 3.1.3 Photolithography

Photolithography is a well established method for the structuring of micro patterns on thin films. The samples are cleaned and coated over the entire surface in a spin coater with an [! (!)]UV sensitive photo-resist. A positive resist (AZ 1541H) and negative resist (AZ nLOF 2020) are used in this work. The positive photo-resist has to be annealed for 90 s at 90°C before the light exposure and the negative resist for 90 s at 110°C after the light exposure. A chromium mask with the desired pattern is aligned over the sample using a *MBJ3 Maskaligner* by *Carl Süss* and the uncovered photo-resist is exposed to [! (!)]UV-light for a predefined time. The photo-resist is changed by the [! (!)]UV-light in such a way that it becomes either resistant to (negative photo-resist) or removable by (positive photo-resist) a developer. The developers used are AZ351B and AZ 726 MIF for positive and negative resist, respectively. Afterward, the photo-resist is post-baked and the structure can be further processed by e.g. metal or thin film deposition or etching. Finally, the remaining photo-resist and the material deposited on top of it are removed by n-methyl-2-pyrrolidon and subsequently the sample is cleaned in acetone and isopropanol. Various small devices, such as field-effect transistors, Schottky diodes, and *pn*-diodes can be easily structured by this method. All samples were fabricated on Corning 1737 and Corning *Eagle XG* substrates. The Schottky diode FET logic inverter and ring oscillator samples were fabricated on  $10 \times 10 \text{ mm}^2$  quartz glass substrates.

## 3.2 Characterization Techniques

### 3.2.1 Hall Effect Measurements

Hall effect measurements in the van der Pauw geometry [72, 73] were used to determine the Hall coefficient  $R_H$  of the thin films. Subsequently, the free carrier density  $n$  and Hall mobility  $\mu$  were calculated from the Hall coefficient. The relationship between these quantities is

$$R_H = \mu \cdot \rho = \frac{1}{n \cdot e} . \quad (3.1)$$

The resistivity  $\rho$  of the thin films was determined by a four point measurement in the same measurement set-up. To determine the resistivity and Hall coefficient, four ohmic contacts were required on the sample corners. These were realized by [! (!)]dc-sputtered gold in this work. All Hall effect and resistivity measurements were conducted using a *Keithley 220* current source, a *Keithley 7001* switch with a *7065 Hall card*, and a *Keithley 200* multimeter. The magnet coils were operated using a *HP 6030A* power supply. The determination of the Hall coefficient was carried out under a magnetic field of  $B = 0.43 \text{ T}$ .

### 3.2.2 XRD and XRR Measurements

The X-ray amorphous structure of the thin films was confirmed by the absence of Bragg peaks in the [! (!)3]XRD patterns obtained by a *X'Pert Philips Analytical Materials Research Diffractometer*. Therefore,  $2\Theta - \omega$ -scans were performed. It utilizes a copper X-ray source with a  $K_\alpha$  line with a wavelength of  $1.5406 \text{ \AA}$  for the measurements. The [! (!)3]XRR measurements, used for the determination of the thin film thickness, were performed by Stefan Hohenberger<sup>4</sup> using a *Panalytical Pro MRD Diffraktometer*. The pattern obtained by [! (!)3]XRR also facilitate the calculation of the thin film density, surface and interface roughness.

### 3.2.3 Static and Dynamic Current-Voltage Measurements

Current-voltage measurements were conducted using an *Agilent 4155C Semiconductor Parameter Analyzer*. The samples were contacted by tungsten probes, which can be aligned in position and height, in a *Süss MicroTec PA200 PS waferprober*. The current was measured in a predefined voltage range, which can be tuned between  $-40 \text{ V}$  and  $40 \text{ V}$ . Currents between  $10^{-12}$  and  $0.1 \text{ A}$ <sup>5</sup> can be measured by the device. These devices were also used for [! (!)3]QSCV measurements. Automatic measurements were conducted using the *MATLAB* program *AutoWP*, written by Fabian Klüpfel. For temperature dependent measurements in a range of  $25^\circ\text{C}$  to  $150^\circ\text{C}$ , a *Unichiller* cooler was connected to the *Süss MicroTec PA200 PS waferprober*.

To determine the switching speed of the devices, gate lag measurements were performed. Therefor a self built tip by Fabian Klüpfel<sup>6</sup> was used [53, 74]. The modulations of the drain current were measured as an alternating current by the *Agilent 4155C Semiconductor Parameter Analyzer*. Gate voltage oscillations were supplied by a USB oscilloscope *Handyscope Hs3* by *TiePie* in a range from  $10 \text{ Hz}$  to  $20 \text{ MHz}$ . The measurement signals are processed by a program written by Fabian Klüpfel<sup>7</sup>. The upper detection limit of the self-built tip is at approximately  $1 \text{ MHz}$ .

Ring oscillators were measured using an active tip *Picoprobe* by *GGB Industries Inc.*, which is connected to a *Picoprobe* amplifier and the oscilloscope *Handyscope Hs3* by *TiePie*.

All measurements in this work were conducted without illumination (in the dark) unless otherwise stated.

### 3.2.4 Further Characterization Techniques

Optical images and information on the height profiles of sample surfaces were obtained by a laser scanning microscope. The instrument *Keyence VK-200K* unit combined with a *Keyence*

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<sup>5</sup>For voltages between  $20 \text{ V}$  and  $40 \text{ V}$  the maximal current is  $0.01 \text{ A}$ .

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<sup>7</sup>Universität Leipzig

*X210* microscope were used. With this confocal microscope a point wise scanning of the sample surface was possible. The device uses a laser with a wavelength of 408 nm and an outgoing power of 0.95 W. The reflected signal is detected by a photomultiplier.

Information on the transparency of thin films were obtained by transmission (and reflection) measurements, which were carried out by Ulrike Teschner<sup>8</sup>. A spectral range of 200 to 1200 nm and a aperture with 4 mm radius were used for the measurement with the *Spectrometer Lambda 19*. The thus obtained transmission data were also used for the calculation of the sample thickness for thicknesses > 500 nm.

Information on the cation composition were obtained by [! (!)3]EDX measurements performed by Jörg Lenzner<sup>9</sup> using a *Nova NanoLab 200* by *FEI Company*.

For thin film thicknesses of 200–500 nm, the thickness was obtained by a profilometer *Bruker Dektak XT*. It uses a diamond tip which is dragged over the sample with a predefined force and speed. This was only possible for samples, where a step between substrate and thin film (e.g. sample corners that are not coated during the deposition) exist.

AFM measurements were performed by Max Kneiß<sup>10</sup> on a *Park Systems XE150*.

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# Chapter 4

## Physical Properties of Amorphous Zinc Tin Oxide

The determination of the optimum composition for the most advantageous electrical and optical properties of ternary compounds is of great importance for the development of devices based on novel materials. The [! (!)3]CCS [! (!)3]PLD method offers a comparably quick and simple approach to acquire a wide range of cation ratios in one deposition step. This method is described in chapter 3.1.1, and is here employed for the deposition of amorphous [! (!)3]ZTO thin films. All [! (!)3]ZTO thin films, discussed in this chapter, were deposited at room temperature by Peter Schlupp<sup>1</sup>. In the first part of this chapter the influence of the cation composition of [! (!)3]ZTO thin films on the electrical, optical and structural properties for a wide cation composition range are presented and discussed. Other deposition conditions, such as the background gas and pressure, are kept constant in this work to investigate the influence of the cation composition on the thin film properties only. In previous reports, a tuning of the electrical and optical properties of pulsed laser deposited amorphous [! (!)3]ZTO thin films with fixed cation composition was done by a variation of the deposition conditions [8,9]. Based on the [! (!)3]ZTO thin films with varying cation composition, Schottky barrier diodes are fabricated and the long term stability as well as processes leading to the absence of a long term stability are discussed. The results presented here have been published in [E1-E4].

The results obtained from these investigations on the basic physical properties of [! (!)3]ZTO and of processes important for the formation of rectifying contacts, are later in this work used for the fabrication of devices and integrated circuits.

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## 4.1 Characterization of Pulsed Laser Deposited Zinc Tin Oxide Thin Films Having a Continuous Composition Spread

Based on the previously obtained results on continuous composition spread pulsed laser deposited  $[\text{Zn}]_3\text{ZTO}$  [E1] [66], four thin films were fabricated to cover a composition range of  $0.12\text{--}0.72 \text{ Zn}/(\text{Zn}+\text{Sn})$ . The thin films were deposited on  $50\times 50 \text{ mm}^2$  Corning 1737 glass substrates with a thickness of  $0.7 \text{ mm}$ . During the  $[\text{Zn}]_3\text{PLD}$  process an offset  $\epsilon = 24 \text{ mm}$  and a pulse frequency of  $5 \text{ Hz}$  were employed. Oxygen, with a pressure of  $p_{\text{oxygen}} = 0.03 \text{ mbar}$ , was chosen as process gas. The advantage in using four thin films to cover this wide composition range lies in a smaller composition gradient and therefore a more homogeneous composition on each sample piece, which is not necessarily given for larger composition gradients. Additionally, it was previously shown that thin films with a smaller composition gradient have a superior surface roughness [E1]. This is due to a reduced ablation of droplets from the interface of the segmented target for a smaller composition difference between the two target halves [E1]. In a first step the obtained thin films were investigated by  $[\text{Zn}]_3\text{EDX}$  by Jörg Lenzner<sup>2</sup> to obtain spatially resolved information on the cation composition. The thin films were subsequently sawed parallel to the composition gradient, which is along the diagonal<sup>3</sup> of the thin films, in  $5 \text{ mm}$  wide stripes. These stripes were then broken into  $5 \times 5 \text{ mm}^2$  pieces and characterized electrically by Hall effect measurements (see chapter 3.2.1) and optically by transmission measurements. The hereby obtained stripe of greatest length, which is that along the diagonal of the thin film, is called middle stripe in the following. All further stripes next to the middle stripe are henceforth called neighboring stripes. The composition ( $\text{Zn}/(\text{Zn}+\text{Sn})$ ) range, the layer thickness  $d$  at the thin film center, the resistivity  $\rho$  range and free carrier density  $n$  range for each thin film are listed in Table 4.1. The layer thickness was approximated from the constructive interferences in the transmission data (see Figure 4.4) and an estimated refractive index of  $1.90$ . Ellipsometry measurements on a  $[\text{Zn}]_3\text{ZTO}$  thin film deposited by  $[\text{Zn}]_3\text{PLD}$  using the  $[\text{Zn}]_3\text{CCS}$  approach yielded a refractive index of  $1.95$  and  $1.85$  for high and low zinc contents, respectively. The four thin films have compositions of  $0.12\text{--}0.29 \text{ Zn}/(\text{Zn}+\text{Sn})$  (thin film I),  $0.34\text{--}0.54 \text{ Zn}/(\text{Zn}+\text{Sn})$  (thin film II),  $0.46\text{--}0.57 \text{ Zn}/(\text{Zn}+\text{Sn})$  (thin film III) and  $0.56\text{--}0.72 \text{ Zn}/(\text{Zn}+\text{Sn})$  (thin film IV). There is an overlap in compositions for thin films II and III and thin films III and IV, which is later on used to compare the results between the different samples and to determine the reproducibility of the results. The cation composition of the stripes is depicted along the thin film diagonal in Figure 4.1. For the middle stripe of thin film I, a strong s-shape of the cation composition is visible, whereas it is less pronounced for the other thin films.

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<sup>3</sup>The composition gradient was chosen along the diagonal of the thin film to achieve the highest possible composition range for each thin film.

#### 4.1. Characterization of Pulsed Laser Deposited Zinc Tin Oxide Thin Films Having a Continuous Composition Spread

**Table 4.1:** Composition range, thin film thickness  $d$  range, resistivity  $\rho$  range and free carrier density  $n$  range of thin films I-IV. The compositions of the corresponding targets is listed in chapter 3.1.1.

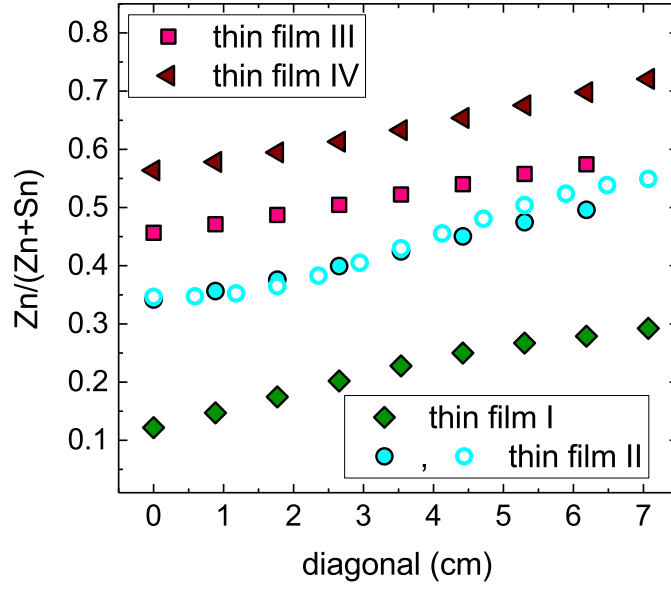
sample	film composition Zn/(Zn+Sn)	d $\mu\text{m}$	$\rho$ $\Omega\text{cm}$	$n$ $\text{cm}^{-3}$
thin film I	0.12 – 0.29	1.15	0.006 – 0.19	$(3.88 – 0.56) \times 10^{19}$
thin film II	0.34 – 0.54	0.86	1.1 – 16	$(8.72 – 0.50) \times 10^{17}$
thin film III	0.46 – 0.57	0.90	3.2 – 27	$(2.27 – 0.28) \times 10^{17}$
thin film IV	0.56 – 0.72	0.75	4.3 – 37	$(1.72 – 0.50) \times 10^{17}$

In the following the composition on each  $5 \times 5 \text{ mm}^2$  sample piece is assumed to be constant, which is acceptable due to the small maximum deviation from the mean composition of  $\pm 0.025 \text{ Zn}/(\text{Zn}+\text{Sn})$  per sample piece. All four thin films are approximately  $0.6 \mu\text{m}$  to  $1.2 \mu\text{m}$  thick, with a trend to smaller thin film thicknesses observable for higher zinc contents in the thin films. This is due to the smaller size and lighter mass of  $\text{ZnO}$  molecules and Zn atoms compared to  $\text{SnO}_2$  molecules and Sn atoms and the enhanced scattering of the lighter molecules and atoms on the background gas during the [! (!)3]PLD process. This leads to a reduced material input on the zinc rich side of the thin films. This effect is also visible if the target segment compositions are compared to the cation composition of the resulting thin films (see chapter 3.1.1) The tin rich side has a composition that is almost equal to the target segment composition, whereas the zinc rich side has a lower cation ratio than the one that was present in the target. For thin film I, the zinc rich target segment has a zinc oxide content of 40 at%, whereas the thin film has a maximum zinc content of 0.29  $\text{Zn}/(\text{Zn}+\text{Sn})$  only.

The cation compositions given in Table 4.1 correspond to the sample stripes used for the device fabrication. In Figure 4.2 (a) the resistivity of thin films I-IV is depicted as a function of the composition. For thin film I the middle stripe of the sample is shown, for thin film II the middle and a neighboring stripe are shown and for thin films III and IV only a neighboring stripe is shown. These sample pieces<sup>4</sup> were later used for the fabrication of devices. An overall increase of the resistivity with increasing zinc content is observable and the results of thin films I-III complement each other. In contrast, the resistivity of thin film IV is one order of magnitude lower than that of thin film II and III for the same film cation composition. For the fabrication of the segmented [! (!)3]PLD target used for the deposition of thin film IV, a  $\text{SnO}_2$  powder from a new charge was used. That the powder used for the target fabrication has a significant influence on the thin film properties was previously demonstrated for zinc oxide [75]. Therefore, not only the deposition conditions but also the target fabrication is of importance to achieve reproducible thin film properties.

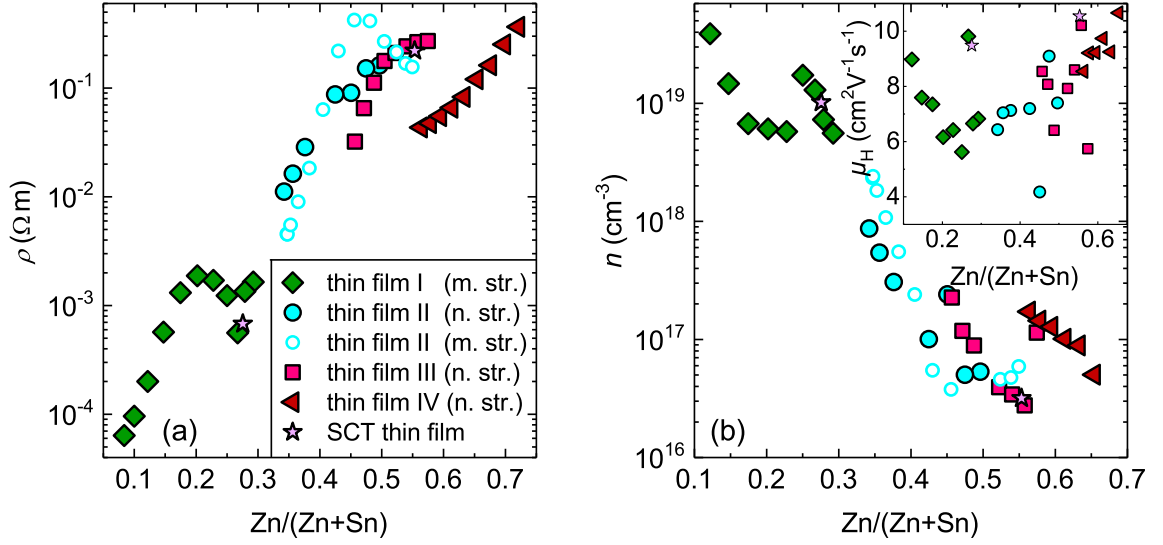
While the resistivity of the middle stripes of thin films III and IV, and the neighboring stripe

<sup>4</sup>except the middle stripe of thin film II



**Figure 4.1:** Composition over the diagonal of the four thin films determined by [! (!)3]EDX. For thin film I the neighboring stripe (full symbols) and middle stripe (open symbols) is shown.

of sample II exhibit a systematic increase of the resistivity with increasing zinc content in the thin films, a non systematic behavior is observed for thin film I (middle stripe) and the middle stripe of thin film II. For thin film I an increase of the resistivity up to a value of  $0.20 \text{ Zn}/(\text{Zn}+\text{Sn})$  is measured, before the resistivity drops by a factor of 3.4 and subsequently increases again. The middle stripe of thin film II exhibits a decrease of the resistivity by a factor of 2.6 for an increase of the zinc content from 0.46 to  $0.55 \text{ Zn}/(\text{Zn}+\text{Sn})$ . This non-systematic behavior of the resistivity may be explained by a position dependence of the energy of the incoming particles during the [! (!)3]PLD process. This leads to a superposition of the influence of the cation composition and the position on the sample on the electrical properties. This effect was discussed in detail in the PhD thesis of Peter Schlupp [18]. The resistivity in dependence on the position on the sample is shown in Figure 4.3 for the middle stripe of samples I-IV. Without a composition gradient, the thin film center has a higher resistivity than the outer edges. In the presence of a composition gradient this resistivity peak is shifted to the zinc rich side for the here investigated compound. This effect is strongest for the middle stripe of each sample and weaker for the outer stripes. For thin film I the middle stripe was used for the further fabrication of the diodes and is therefore depicted here, whereas for thin films II-IV neighboring stripes were used. The resistivity of the middle stripe of thin film II is depicted (compare Figure 4.2 (a)) to show that this effect appears not only for thin film I. For higher resistivities of the thin films as for example for thin film III and IV, this effect is less pronounced or not visible at all (see Figure 4.3). It may also be present but is probably dominated by the high resistivity of the thin films and therefore not discernible. The resistivity of the four thin films varied between  $3.4 \times 10^{-3} \Omega \text{ cm}$  and  $37 \Omega \text{ cm}$  for the

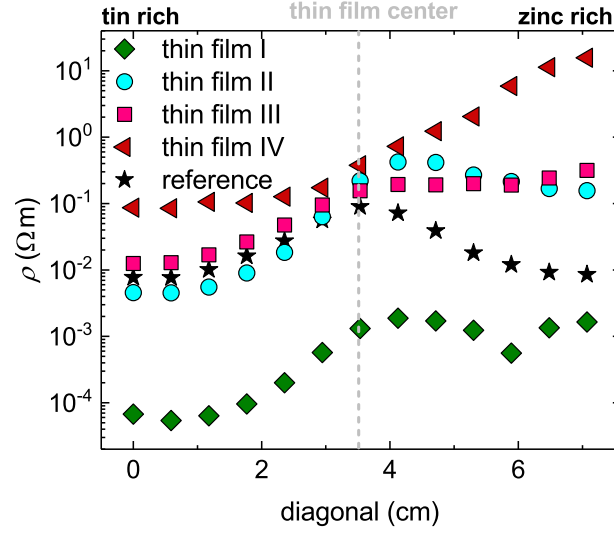


**Figure 4.2:** Resistivity (a), free carrier density (b) and Hall mobility (inset) determined by Hall effect measurements for thin films I-IV covering a composition range of 0.12 to 0.72  $\text{Zn}/(\text{Zn}+\text{Sn})$ . For two compositions, deposited from standard single composition targets (SCTs), the resistivity is plotted in (a). Middle stripes (m. str.) and neighboring stripes (n. str.) are denoted in the legend.

given composition range and  $p_{\text{oxygen}} = 0.03 \text{ mbar}$ . The lowest resistivity was measured for the lowest zinc content in the thin films and the highest resistivity for the highest zinc content. A tuning of the resistivity over four orders of magnitude was therefore achieved by a variation of the cation composition. Additionally, the resistivity of the thin films was compared to that of [! (!)]3SCT thin films deposited under the same background pressure during the [! (!)]3PLD but a different offset  $\epsilon = 10 \text{ mm}$  with two different compositions on  $10 \times 10 \text{ mm}^2$  Corning 1737 glass substrates. A high similarity between the results of the [! (!)]3CCS and SCT thin films is observed (compare Figure 4.2 (a)).

The results for the free carrier density  $n$ , shown in Figure 4.2 (b), coincide with the trend obtained for the resistivity. An overall decrease of the free carrier density with increasing zinc content was measured. The local extrema in the free carrier density for the middle stripes of thin films I and II may again be explained by position dependence of the energy of the incoming particles. The highest free carrier density of  $3.9 \times 10^{19} \text{ cm}^{-3}$  was obtained for  $\text{Zn}/(\text{Zn}+\text{Sn}) = 0.12$ , while the lowest free carrier density of  $2.8 \times 10^{16} \text{ cm}^{-3}$  was measured for  $\text{Zn}/(\text{Zn}+\text{Sn}) = 0.56$ . For  $\text{Zn}/(\text{Zn}+\text{Sn}) > 0.65$  the free carrier density and mobility could not be determined due to a Hall voltage within the noise level of the measurement device and a therefore inconclusive sign of the Hall coefficient during the measurement.

In literature, a tuning of the free carrier density and resistivity by a variation of the deposition pressure has been reported [8,9]. Free carrier density values of  $10^{12} \text{ cm}^{-3}$  to  $10^{19} \text{ cm}^{-3}$  and a tuning of the resistivity by seven orders of magnitude are reported for two different cation



**Figure 4.3:** Resistivity of thin films I-IV and a thin film deposited under the same deposition conditions as these thin films but from a single composition target (reference). The resistivity is depicted in dependence on the diagonal. The composition of the reference thin film is  $\approx 0.3 \text{ Zn}/(\text{Zn}+\text{Sn})$  and all thin films were deposited under  $p_{\text{oxygen}} = 0.03 \text{ mbar}$ .

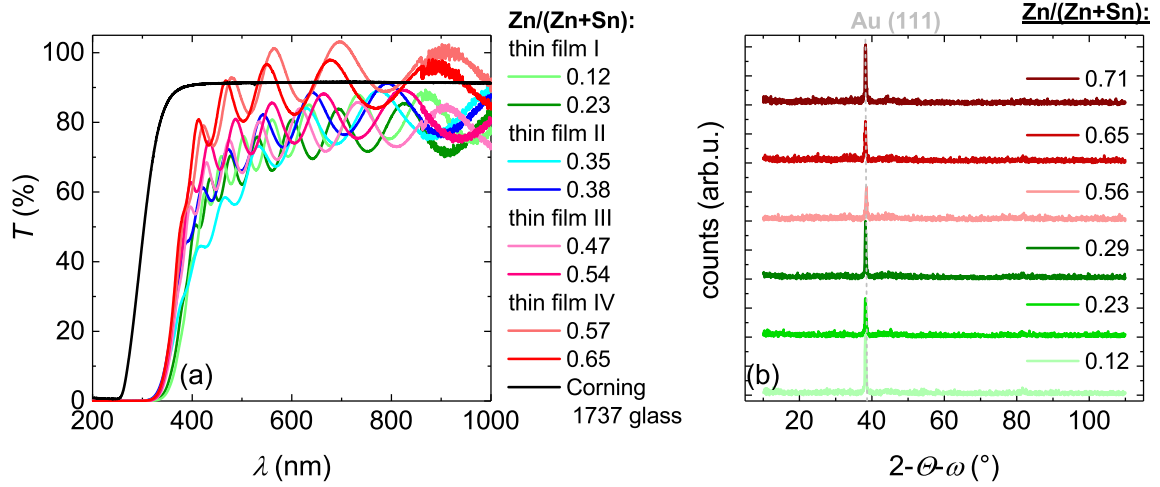
ratios of 0.33 and 0.67 Zn:Sn [9]. These results indicate that a further tuning of the free carrier density and resistivity of the here presented thin films is possible by a variation of the deposition pressure.

The Hall mobility of the four thin films exceeds  $4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  for all compositions. The maximum mobility of  $10.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  is obtained for  $0.65 \text{ Zn}/(\text{Zn}+\text{Sn})$ . These mobilities do not reach the reported highest value for pulsed laser deposited  $[\text{Zn}]_3\text{ZTO}$ , which is above  $12 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  [8]. Field-effect mobilities above  $20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  have been obtained by Chiang *et al.* [12].

The transmittance  $T$  of the combination of thin film and glass substrate for selected compositions is shown in Figure 4.4 (a). It was measured in a range from 200 nm to 1000 nm as described in chapter 3.2.4. The highest transmittance of the thin films<sup>5</sup> was obtained for high zinc contents, which cannot be explained by the band gap of ZnO and SnO<sub>2</sub>, which are 3.4 eV [E3] and 3.6 eV [76], respectively. Using these values, a comparable transmittance would be expected for high zinc and high tin contents. As discussed by Körner *et al.* for theoretical calculations on amorphous  $[\text{Zn}]_3\text{ZTO}$ , under-coordinated tin atoms may cause deep levels within the band gap and lead to a reduced transparency and increased conductivity [77]. This effect would be more pronounced for tin rich thin films and explains the reduced transmittance of the tin rich samples.

The absorption edge was previously determined for this composition range and has been published [E1]. There, the absorption edge was determined to be between 1.8 eV and 3.1 eV for low and high zinc contents in the thin film, respectively. By a variation of the deposition

<sup>5</sup>Mean transmittance in the visible range.



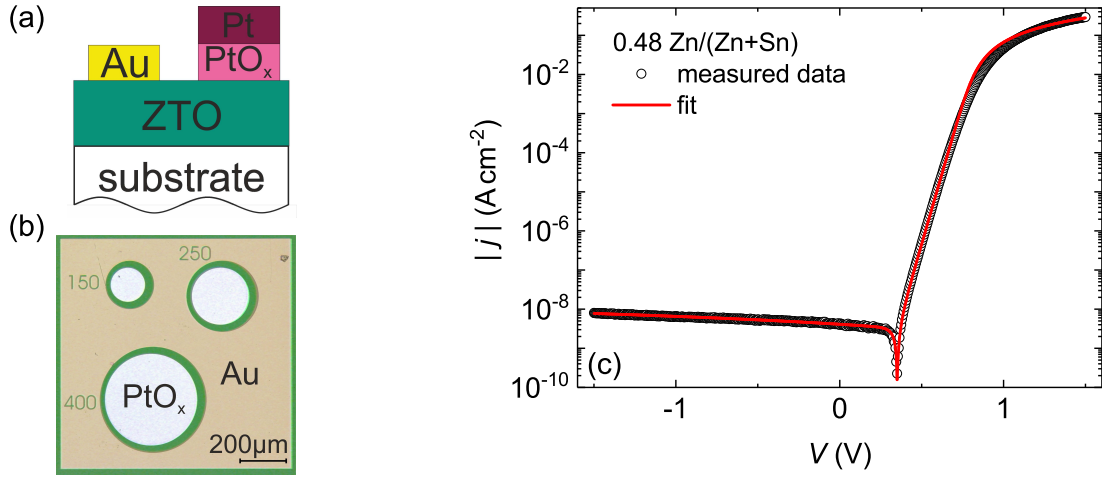
**Figure 4.4:** Transmittance (a) of the combined substrate/ZTO layers for selected compositions of the  $[\text{Zn}]_3\text{ZTO}$  as well as the transmittance of a Corning 1737 glass substrate.  $[\text{Zn}]_3\text{XRD}$  data (b) for selected compositions of thin films I and IV.

pressure the absorption edge of amorphous zinc tin oxide is tunable between 2 eV and 3.3 eV for 0.33  $\text{Zn}/(\text{Zn}+\text{Sn})$  [9, 78]. It has to be noted that all thin films have a transmittance above 60% for  $\lambda > 400$  nm and  $\text{Zn}/(\text{Zn}+\text{Sn}) > 0.5$ . For  $\text{Zn}/(\text{Zn}+\text{Sn}) < 0.5$ , the transparency in the visible light range is smaller. The rise of the transmittance in the regime of the constructive interferences above  $T = 100\%$  can be attributed to the detector error during the measurement. As comparison, the transparency of the Corning 1737 glass substrate is also plotted in Figure 4.4 (a). It is visible that for high zinc contents in the thin film, the transmittance of the combined system thin film and substrate is almost as good as that of the substrate alone. This high transmittance for  $\text{Zn}/(\text{Zn}+\text{Sn}) > 0.5$  renders the compound interesting for future transparent amorphous oxide semiconductor based devices.

As shown in Figure 4.4 (b), the thin films are x-ray amorphous in the given composition range. This is in good agreement with the results on a previously reported  $[\text{Zn}]_3\text{CCS}$   $[\text{Zn}]_3\text{ZTO}$  thin film with a concentration gradient of 0.08 to 0.72  $\text{Zn}/(\text{Zn}+\text{Sn})$  [E1], which also showed x-ray amorphous behavior. The peak visible in the  $[\text{Zn}]_3\text{XRD}$  pattern is attributed to the gold contacts on the corners of the samples, which were used for the Hall effect measurements.

## 4.2 Properties of Schottky Barrier Diodes in Dependence on the Cation Composition

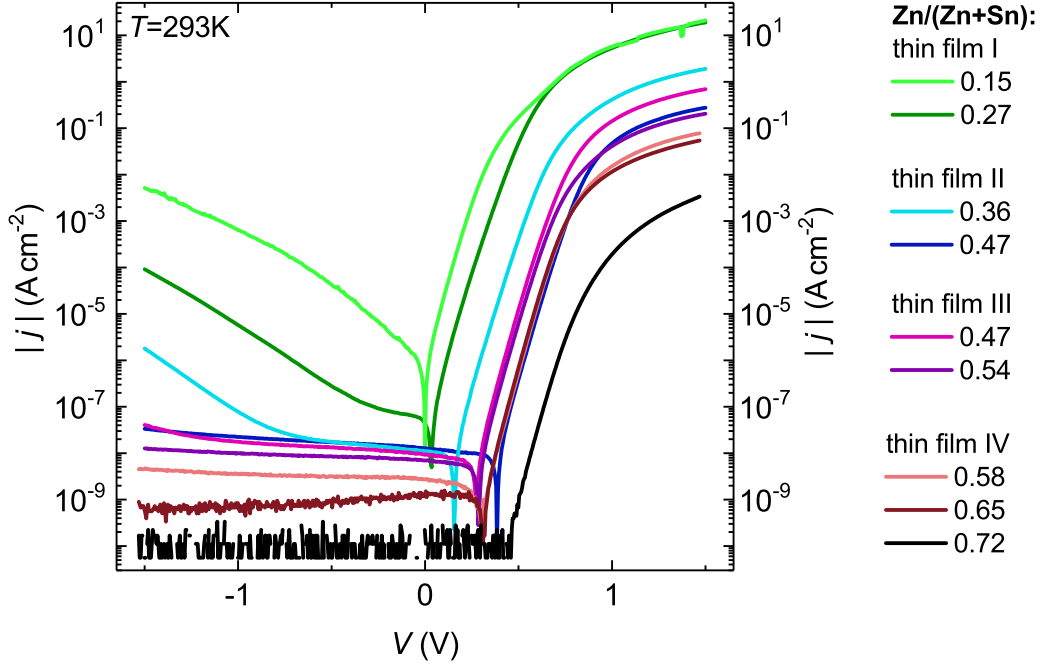
In a next step, Schottky barrier diodes were fabricated on the pre-characterized sample pieces. The contacts were defined by photolithography (chapter 3.1.3). For the formation of highly rectifying contacts, the work function of the metal forming the Schottky barrier contact as well as inherent properties of the semiconductor such as free carrier density and interface defect density are of importance. For many oxide semiconductors it is known that a metal oxide



**Figure 4.5:** Schematic graphic of the Schottky barrier contact (a) and image taken by a laser scanning microscope (b) for three diameters of the Schottky barrier diodes. The transparent [! (!)3]ZTO thin film appears green in this image. Exemplary current density-voltage characteristics (c) for the measured data (open symbols) and the fit by equation 2.18 (red line) for a composition of 0.48 Zn/(Zn+Sn) and a scan direction from positive to negative voltages.

or alternatively an oxygen plasma treatment of the semiconductor surface are required to achieve rectifying contacts [14, 79-92] [E4]. For amorphous [! (!)3]ZTO different metal oxides such as platinum oxide, gold oxide, silver oxide and palladium oxide have been investigated [37, 79, 80] [E2, E4]. Metallic platinum and gold are reported to form ohmic contacts without a previous oxygen plasma treatment of the [! (!)3]ZTO thin films [80] [E4]. The highest rectification ratios as well as the lowest ideality factors have so far been achieved for platinum oxide [18, 37], which will therefore be used as Schottky contact material in the following. The Schottky barrier contact is formed by platinum oxide capped with metallic platinum to ensure an equipotential surface during the measurements. The platinum oxide was dc-sputtered under a gas mixture of 50 sccm argon and 50 sccm oxygen for 15 s and the platinum capping was dc-sputtered under 100 sccm argon for 10 s for all samples on thin films I-IV. A schematic side view of the investigated structure is shown in Figure 4.5 (a). The Schottky barrier contacts are circular with a contact area of  $1.76 \times 10^{-8}$  to  $4.4 \times 10^{-7} \text{ m}^2$ , which corresponds to diameters of 150  $\mu\text{m}$  to 750  $\mu\text{m}$  as exemplary shown for three diameters in Figure 4.5 (b). The ohmic gold contact encloses the Schottky barrier contacts.

In Figure 4.6, exemplary current density-voltage characteristics for selected compositions of thin films I-IV are depicted. All characteristics were measured from positive to negative voltages. It has to be noted that the current density-voltage characteristics are influenced by the free carrier density as well as cation composition. The influence of the free carrier density on ZTO based Schottky barrier diodes is well known [18, 37]. However, the cation composition also plays an important role in such a wide composition range [13]. In the following discussions, the superposition of these two effects has to be kept in mind. However, to keep the discussions clear, the samples are referred to by their cation composition. The



**Figure 4.6:** Current density-voltage characteristics of Schottky barrier diodes on [! ([!)]3]ZTO for selected compositions of the pulsed laser deposited [! ([!)]3]ZTO thin films in a composition range from 0.12 to 0.72 Zn/(Zn+Sn).

free carrier density of the samples is given, where it is required for a better understanding of the device properties.

A decrease of the forward current at a forward voltage  $V_f$  of +1.5 V with increasing zinc content by four orders of magnitude is measured. This regime of the current density-voltage characteristics is dominated by the series resistance, which is directly related to the thin film resistance. Therefore, the increasing resistivity with increasing zinc content in the thin films limits the current flow over the semiconductor and with that the forward current of the diodes. The current at  $V_f = +1.5$  V decreases from a value of  $19 \text{ A cm}^{-2}$  to a value of  $3 \times 10^{-3} \text{ A cm}^{-2}$  for increasing zinc content and resistivity. The reverse current for a reverse voltage  $V_r < -0.5$  V scales exponentially with the voltage for  $\text{Zn}/(\text{Zn}+\text{Sn}) > 0.23$ . From the exponential voltage dependence of this leakage current, it was concluded that a tunneling current dominates the current density-voltage characteristics in this regime. The tunneling current contribution to the reverse current decreases with increasing zinc content and is smaller than the current contribution by thermionic emission for  $\text{Zn}/(\text{Zn}+\text{Sn}) > 0.38$ . This can be seen in the almost constant reverse current for compositions above 0.38 Zn/(Zn+Sn). The reverse current at  $V_r = -1.5$  V decreases by nine orders of magnitude for an increase of the zinc content from 0.12 to 0.72 Zn/(Zn+Sn). This decrease of the reverse tunneling current is due to a strong decrease of the net doping concentration with increasing zinc content, which leads to a wider depletion region and therefore a reduced tunneling probability. The width of the depletion region  $w$  is proportional to  $\sqrt{1/N_t}$  (compare chapter 2.2). The net doping

concentration is directly related to the free carrier density of the samples. For clarity, the free carrier density is used for all discussion of the tunneling current in the following.

For a composition of  $0.72 \text{ Zn}/(\text{Zn}+\text{Sn})$  a noise is observable for  $V < 0.5 \text{ V}$ , which is due to the current resolution of the measurement device *Agilent 4155C Semiconductor Parameter Analyzer*.

The zero crossing of the characteristics shifts to higher positive voltages with increasing zinc content for a voltage sweep direction from positive to negative voltages. The increase of the shift with increasing zinc content is due to overall smaller currents flowing for higher zinc contents. This zero crossing is due to a charging and discharging of interface trap states and the space charge region and is taken into account by an offset current  $I_C$  [93] during the modeling of the characteristics. This offset current is assumed to be bias-independent.

To determine the characteristic parameters of the Schottky barrier diodes investigated in this work, a *MATLAB* program by Daniel Splith<sup>6</sup> was used that employs equation 2.18 for thermionic emission:

$$I = A_0 A^* T^2 \exp\left(-\frac{\phi_{B,\text{eff}}}{k_B T}\right) \left[ \exp\left(e \frac{V - IR_s}{\eta k_B T}\right) - 1 \right] + \frac{V - IR_s}{R_p} + I_C . \quad (4.1)$$

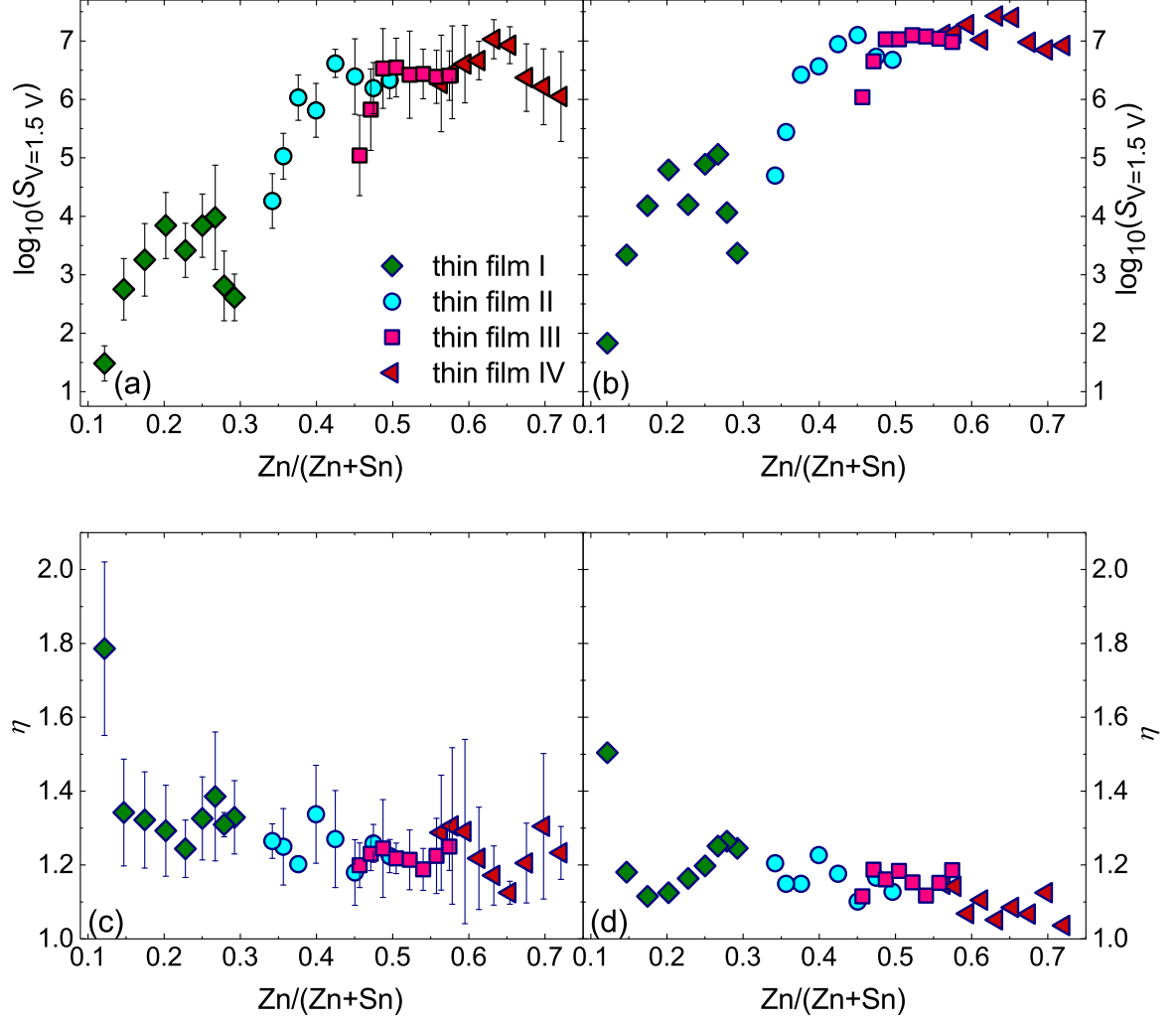
$A_0$  is the Schottky barrier contact size and  $A^*$  is the Richardson constant, which contains the effective electron mass  $m_{\text{eff}}$ . The effective electron mass of amorphous [! (!)3]ZTO is unknown and is approximated to be  $m_{\text{eff}} = 0.3m_0$  [18] in this work. This equation is valid even for the diodes having a high tunneling current contribution in the reverse direction, as the forward regime, which was modeled in the following, is dominated by the thermionic emission. This will be argued at a later point (see chapter 4.3). The fit was used to obtain information on the effective barrier height  $\phi_{B,\text{eff}}$  and the ideality factor  $\eta$ . The ideality factor describes the voltage dependence of the effective barrier height. For a composition of  $0.48 \text{ Zn}/(\text{Zn}+\text{Sn})$ , the current density-voltage characteristic and the corresponding fit are shown in Figure 4.5 (c). At the transition from the exponential regime of the characteristic to the series resistance dominated part of the characteristics in forward direction, the fit slightly overestimates the measured data. The non-ideal behavior of the characteristics in this regime is due to lateral current spreading as it is reported by Osvald [94].

For each sample piece, corresponding to a certain composition, 10 – 20 devices were measured to calculate the arithmetic mean of the rectification ratio and the ideality factor. The rectification ratio  $S_{V=1.5\text{V}}$  of the devices was calculated as the current density at  $+1.5 \text{ V}$  divided by the absolute current density at  $-1.5 \text{ V}$ . Its mean and the highest value for each composition are depicted in Figure 4.7 (a) and (b), respectively. The error bars denote the standard deviation of the logarithmic mean rectification (a) and the mean ideality factor (c). On the large scale, an increase of the rectification ratio with increasing zinc content is observed. For each individual thin film, but especially for thin film I, a plateau or even a dip to lower values is visible on the zinc rich side. For thin film I this dip appears at  $\text{Zn}/(\text{Zn}+\text{Sn}) > 0.27$  and cor-

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#### 4.2. Properties of Schottky Barrier Diodes in Dependence on the Cation Composition



**Figure 4.7:** Logarithmic mean (a) and logarithmic maximum (b) value for the rectification ratio and mean (c) and minimum (d) value of the ideality factor in dependence on the thin film cation composition.

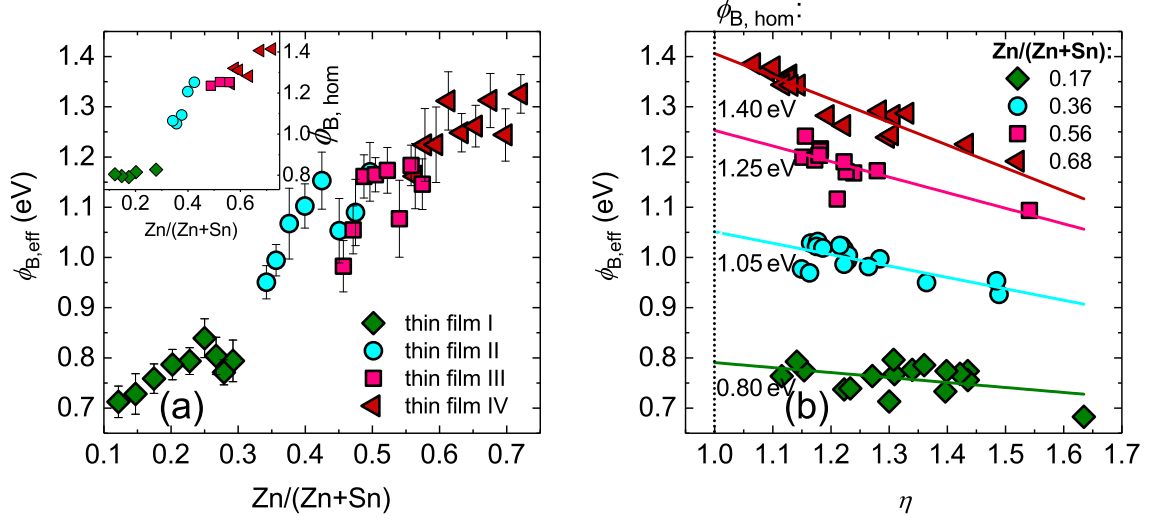
responds to the increase of the free carrier concentration previously described in this regime (see Figure 4.2 (b)). Similarly the plateau for thin films II and III can be attributed to a small change in the free carrier density for these regimes. A high thin film resistivity, which limits the forward current of thin film IV for high zinc contents, leads to a decrease of the rectification ratio for  $Zn/(Zn+Sn) > 0.65$ . The logarithm of the mean rectification ratio shows a large deviation for thin films I, III and IV, whereas the devices for each sample on thin film II are very homogeneous (compare Figure 4.7 (a)). The highest mean rectification ratio as well as the highest maximum rectification ratio are obtained for  $Zn/(Zn+Sn) = 0.63$  and  $n = 8.9 \times 10^{16} \text{ cm}^{-3}$  and are  $1.1 \times 10^7$  and  $2.7 \times 10^7$ , respectively. For thin film compositions above  $Zn/(Zn+Sn) > 0.48$ , the mean as well as the maximum rectification ratio is very similar. The standard deviation of the logarithmic rectification ratio is approximately 10% for all compositions. The smallest mean rectification ratio of 30 was obtained for 0.12  $Zn/(Zn+Sn)$

and a free carrier density of  $n = 3.9 \times 10^{19} \text{ cm}^{-3}$ . The rectification ratio is limited by the high reverse tunneling leakage current for low zinc contents and high free carrier densities of the thin films. In contrast, for high zinc contents and small free carrier densities it is limited by the series resistance of the thin films. An overall increase by five orders of magnitude is measured from the lowest to the highest mean rectification ratio.

At the compositional overlap between thin films III and IV ( $0.56 < \text{Zn}/(\text{Zn}+\text{Sn}) < 0.57$ ) a good agreement for the mean and maximum rectification ratio can be observed, even though the resistivity and free carrier density for these compositions on the two different thin films differ by approximately one order of magnitude. From the difference in the resistivity and free carrier density, a lower forward (and reverse) current would be expected for the sample on thin film IV and a higher reverse (and forward) current for the sample on thin film III. However, the measured current density-voltage characteristics are very similar for this composition. In contrast, for the compositional overlap between thin films II and III ( $0.46 < \text{Zn}/(\text{Zn}+\text{Sn}) < 0.54$ ), a huge difference (above one order of magnitude) in the rectification ratio is obtained for a composition of  $0.46 \text{ Zn}/(\text{Zn}+\text{Sn})$ . The free carrier density is with  $2.4 \times 10^{17} \text{ cm}^{-3}$  (thin film II) and  $2.3 \times 10^{17} \text{ cm}^{-3}$  (thin film III) nearly identical. However, the resistivity and Hall mobility of these two thin films differ significantly (compare Figure 4.2). The current density-voltage characteristics exhibit a higher forward current for the sample on thin film III compared to the sample on thin film II. For higher zinc contents, the mean and maximum rectification ratios for these two thin films are comparable.

The ideality factor  $\eta$ , obtained from a fit with equation 2.18 mirrors the behavior of the rectification ratio. An overall tendency of decreasing ideality factors with increasing zinc content was obtained (compare Figure 4.7 (c) and (d)). A minimum value of 1.04 was obtained from a fit of the characteristics for a composition of  $0.72 \text{ Zn}/(\text{Zn}+\text{Sn})$ . It is noteworthy that for compositions above  $\text{Zn}/(\text{Zn}+\text{Sn}) > 0.15$ , the mean and minimum ideality factors are below 1.5. A good agreement between the ideality factors for the overlap regime between thin films II and III and thin films III and IV is visible. The deviation from the mean ideality factor is large for thin films I, II and IV. This means that the exponential increase in the current density voltage characteristics is not very homogeneous for each composition. This may be due to interface defects. In contrast, the ideality factors on thin film III shows small deviations from the mean value. An overall deviation from the arithmetic mean of 10 – 20% is measured for all cation compositions.

In literature, a maximum rectification ratio of  $\approx 10^7$  is given for Schottky barrier diodes on room temperature deposited  $[\text{Al}]_3\text{ZTO}$  with a free carrier density of  $5 \times 10^{17} \text{ cm}^{-3}$  and a composition of  $0.3 \text{ Zn}/(\text{Zn}+\text{Sn})$  [37]. The contact is formed by  $\text{PtO}_x$  with a Pt capping, similarly to the devices presented here. For this composition a scaling of the rectification ratio with the free carrier density was reported [37]. A maximum rectification ratio was obtained for a free carrier density of  $\approx 5 \times 10^{17} \text{ cm}^{-3}$ , whereas higher and lower free carrier densities lead to reduced rectification ratios due to an increase of the reverse current (higher free carrier densities) or a decrease of the forward current (lower free carrier densities) [37]. For



**Figure 4.8:** Effective barrier height (a) and extrapolated homogeneous barrier height (inset) for compositions between 0.12 and 0.72 Zn/(Zn+Sn). Effective barrier height in dependence on the ideality factor (b) and estimation of the homogeneous barrier height for selected compositions.

palladium oxide, a rectification ratio of up to  $10^2$  with an ideality factor of 1.9 was reported by Son *et al.* [80]. The diode properties may be further tuned by a variation of the free carrier density to obtain information about the influence of the composition independent on the free carrier density and vice versa [37]. A further possibility to reduce the tunneling current is the use of a thin intrinsic  $\text{ZnO}$  layer between semiconducting ZTO and Schottky barrier contact [37]. This intrinsic  $\text{ZnO}$  layer mainly reduced the tunneling current for reverse voltages, however a slight reduction of the forward current is also observed. This method could be employed to further reduce the tunneling current for the devices presented here, especially for the thin films with high free carrier densities.

The fit with equation 2.18 was also used to determine the effective barrier height  $\phi_{B,eff}$  of the samples as shown in Figure 4.8 (a). An increase of the effective barrier height with increasing zinc content was determined. A minimum mean value of  $\bar{\phi}_{B,eff} = 0.71$  eV was obtained for 0.12 Zn/(Zn+Sn) and a maximum mean value of  $\bar{\phi}_{B,eff} = 1.33$  eV for 0.72 Zn/(Zn+Sn). As described in chapter 2.2, a plot of the effective barrier height as function of the ideality factor (see Figure 4.8 (b)) was used to estimate the homogeneous barrier height  $\phi_{B,hom}$ . Values between 0.8 eV and 1.4 eV were obtained in the given composition range. However, the homogeneous barrier height was only determined for compositions where a linear dependency between  $\phi_{B,eff}$  and  $\eta$  was observed.

The homogeneous barrier height is determined as the extrapolation of the linear regression of the barrier height over the ideality factor to an ideality factor of  $\eta = 1$ , which results in a minimal overestimation of the homogeneous barrier height. Due to image charge effects, which are not taken into account here, an ideality factor slightly above 1 would be more precise for the determination of the homogeneous barrier height (see chapter 2.2) [93]. Nonetheless, this

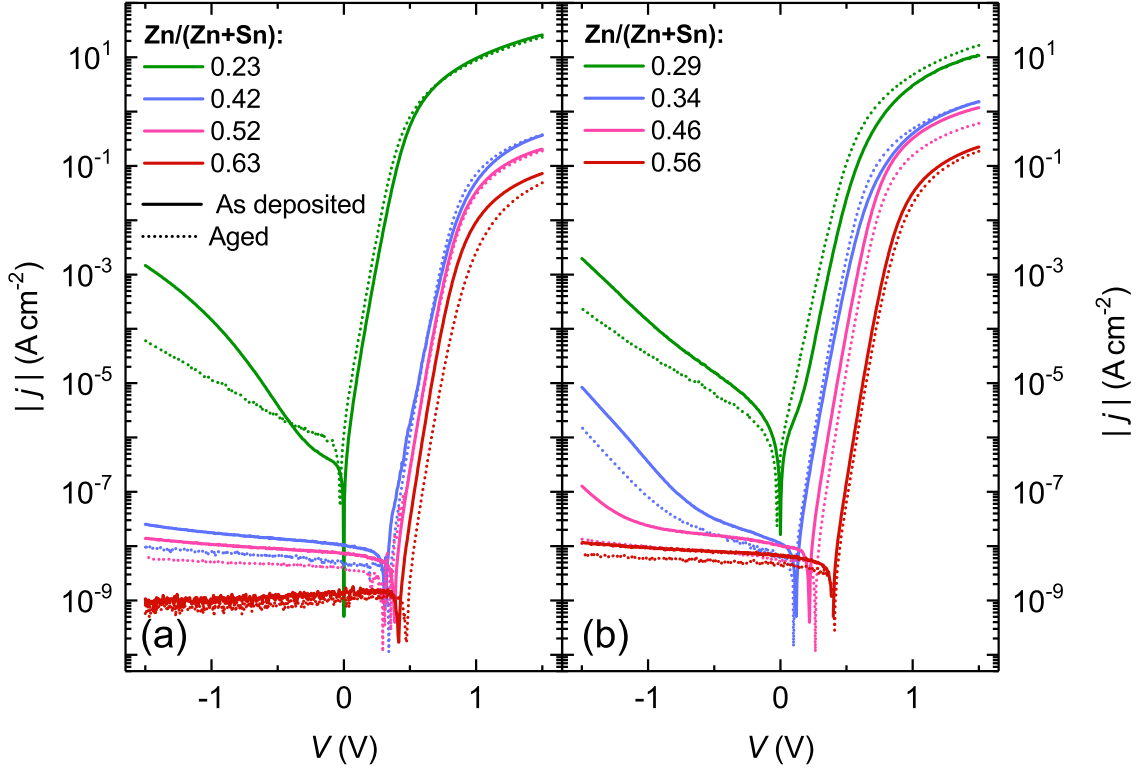
method allows a qualitative comparison of the barrier height of the Schottky barrier contacts. The values of the effective barrier height are in good agreement with a value of 0.8 eV given in literature for  $\text{PtO}_x/\text{ZTO}$  Schottky barrier contacts for a composition of  $\text{Zn}/(\text{Zn}+\text{Sn}) \approx 0.3$  reported by Schlupp *et al.* [37]. For palladium oxide Schottky barrier contacts on ZTO an effective barrier height of 0.4 – 0.5 eV was obtained by Son *et al.* [80].

### 4.3 Long Term Stability of Schottky Barrier Diodes

For future applications in complex devices, the long term stability of the  $[\text{Pt}/\text{ZTO}]$  based devices is crucial. To survey the long term stability, the Schottky barrier diodes were re-measured after 80–120 days. In the intermediate time, the samples were stored in a desiccator. Following this storage, current-voltage measurements were repeated. In Figure 4.9 the current density-voltage characteristics for selected compositions from the center and the border of each thin film are depicted. The previously measured characteristics and parameters are denoted as ‘*as deposited*’ and the re-measured characteristics and parameters as ‘*aged*’ in the following. Cation compositions from the sample center and the sample borders were chosen to appraise whether the long term stability depends on the position on the sample, e.g. the energy of the incoming particles during the  $[\text{Pt}/\text{ZTO}]$  PLD process. It is immediately visible that the forward current remains unaltered upon aging for all compositions, allowing the conclusion that the thin film resistivity of the bulk  $[\text{Pt}/\text{ZTO}]$  does not change during this time scale. In contrast, the reverse current at  $V_r = -1.5$  V changes drastically, whereat the largest decrease of the reverse current is observed for the highest reverse tunneling current in the as deposited state. This corresponds to the lowest zinc content ( $\text{Zn}/(\text{Zn}+\text{Sn}) = 0.12$ ) and highest free carrier density in the thin films. In contrast, for a composition of 0.63  $\text{Zn}/(\text{Zn}+\text{Sn})$ , no decrease of the reverse current upon aging is visible. In Figure 4.9 (b), for a composition of 0.34  $\text{Zn}/(\text{Zn}+\text{Sn})$ , a shift of the point where the tunneling current begins to dominate the reverse current is visible. For a composition of 0.46  $\text{Zn}/(\text{Zn}+\text{Sn})$ , no reverse tunneling leakage current was measured up to  $-1.5$  V in the aged characteristic, even though a tunneling current was detectable for  $V_r < -1$  V in the as deposited characteristic. Additionally, all characteristics become steeper in the forward regime, while the offset current  $I_C$  remained unaffected by the aging.

A detailed discussion of the processes leading to these changes in the current density-voltage characteristics will be given in chapter 4.5.

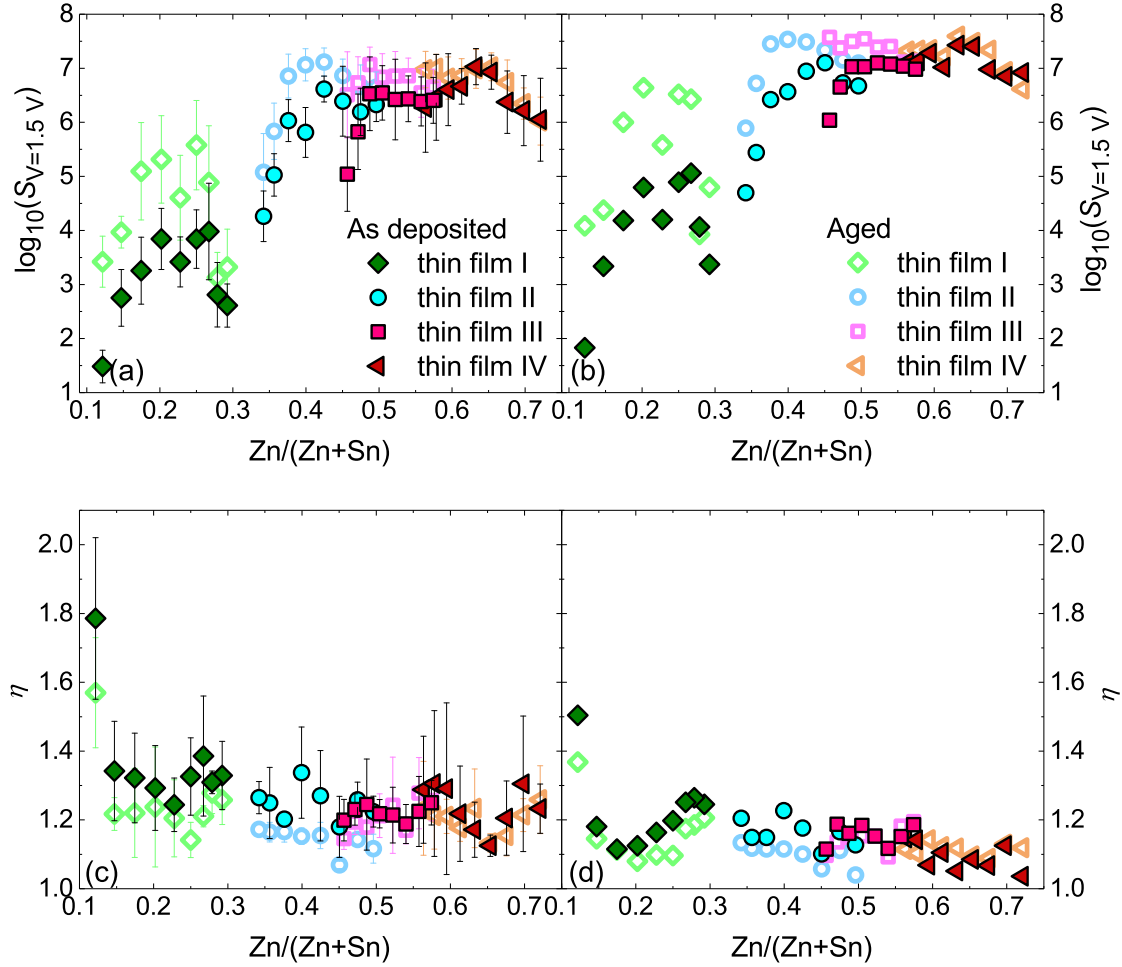
The decrease of the reverse current with simultaneously unaltered forward current leads to an increase of the rectification ratio for all compositions as shown in Figure 4.10 (a) and (b). The strongest increase of the rectification ratio is observed for thin films I and II, which have the highest free carrier density and therefore the highest reverse current in the as deposited state. The now highest values for the mean and maximum rectification ratio of  $1.3 \times 10^7$  and  $3.9 \times 10^7$  were measured for compositions of 0.42  $\text{Zn}/(\text{Zn}+\text{Sn})$  and 0.63  $\text{Zn}/(\text{Zn}+\text{Sn})$ , respectively. For the composition range from 0.12 to 0.25  $\text{Zn}/(\text{Zn}+\text{Sn})$ , the rectification ratio



**Figure 4.9:** Current density-voltage characteristics for selected compositions from the center (a) and border (b) of each thin film in the as deposited (solid line) and aged (dotted line) state.

increases by approximately two orders of magnitude during the storage. In contrast, for a composition of 0.72 Zn/(Zn+Sn), the mean rectification ratio does not increase upon aging. This is due to the already low reverse current in the as deposited state. The standard deviation from the logarithmic mean of the rectification ratio has shrunk for all thin films but thin film I, where it remained unchanged. The standard deviation from the logarithmic mean is below 5% for Zn/(Zn+Sn) > 0.36. For Zn/(Zn+Sn) > 0.38 the rectification ratio is very similar for all thin films and is above  $10^6$ . In the aged state, a lowest rectification ratio of  $1.3 \times 10^3$  is obtained for 0.28 Zn/(Zn+Sn).

The ideality factor slightly decreases for all compositions. A maximum decrease of the mean ideality factor of 0.2 is observed for thin films I and II. For thin films III and IV, which have low ideality factors in the as deposited state, only a small decrease of the mean ideality factor was measured. All four thin films show more homogeneous behavior in the aged state as can be seen from the smaller deviation from the mean rectification ratio and ideality factor. It is now below 4% for thin film II. For thin films I, III and IV it is between 10% and 20%. The minimum ideality factors remain similar to those of the as deposited thin films. These results underscore the negligible influence of the tunneling current contribution in the forward regime of the current density-voltage characteristics, as the ideality factor does not change



**Figure 4.10:** Logarithmic mean and the deviation from the logarithmic mean (error bars) (a) and logarithmic maximum (b) value for the rectification ratios for different compositions of the thin films. Further, the mean (and deviation from the mean, error bars) (c) and minimum (d) values for the ideality factor in dependence on the cation composition are shown. For all compositions the as deposited (full symbols) and aged (open symbols) values are depicted.

significantly, while the reverse tunneling current reduces drastically. Therefore, the use of the thermionic emission equation for the fit of the current density-voltage characteristics is justified.

The mean effective barrier height of the samples exhibits small changes below 0.1 eV. No systematic change with the composition was observed.

The marked improvement of the rectifying behavior of the diodes, especially of those with mediocre performance in the as deposited state, discloses that the potential of [! (!)3]ZTO based Schottky barrier diodes is even higher than assumed from the as deposited devices. The absolute change in the reverse current can be directly related to the free carrier density of the thin films. The same effect was previously observed for *pn*-heterojunction diodes based on [! (!)3]ZTO and was described in detail by Peter Schlupp [7, 18] [E2]. Additionally, an aging of field-effect transistor characteristics was already observed for [! (!)3]IGZO [95-97], where

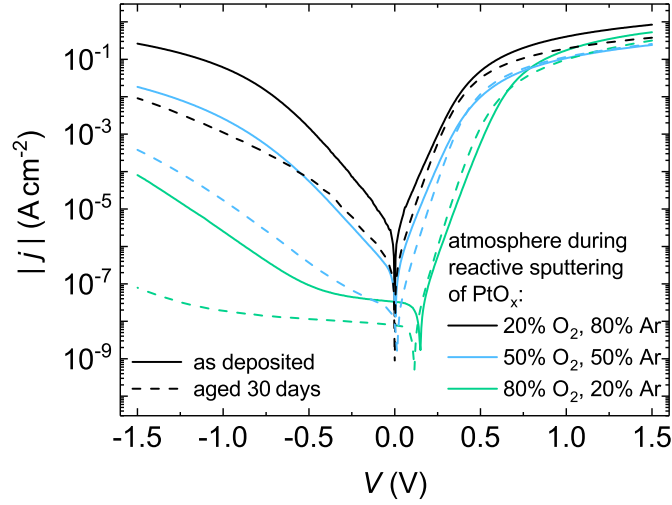
it was ascribed to an absorption and desorption of oxygen and hydrogen. However, for these devices the process was reversible after a storage in vacuum, which was not observed for the devices investigated here.

## 4.4 Important Role of Oxygen for the Formation of Highly Rectifying Contacts

As already discussed in section 4.2, a reactive sputter process or an oxygen plasma treatment are required to achieve highly rectifying contacts on many oxide semiconductors. In contrast, the deposition of high work function metals without additional oxygen leads to an ohmic or weakly rectifying contact [82,85,86,92]. For oxide semiconductors, such as indium oxide, zinc oxide, tin oxide and indium gallium zinc oxide, an influence of an oxygen deficiency on the surface band bending and therefore the surface conductivity was reported [79,85,87,88,91,92,98-101]. This effect can be prohibited or reduced by providing oxygen during the Schottky barrier contact metal deposition or by an oxygen plasma treatment [81,85,98]. For zinc oxide it was shown that the Schottky barrier height is pinned to about 0.75 eV independent of the used metal, if it is deposited non-reactively [82,102,103]. This can be ascribed to a high oxygen vacancy density at the interface [82,102,103], which can increase further by a chemical reaction of the Schottky barrier contact metal and the semiconductor [82]. The metal oxide may be deposited by reactive sputtering to prohibit this effect. However, during the deposition of the metal oxide a low kinetic energy of the particles should be ensured as not to induce additional defects [84,90,102]. The reactive dc-sputtering may induce the improved rectifying behavior of the diodes by several mechanisms: it may lead to a surface cleaning of the semiconductor during the metal oxide deposition, it may reduce the number of interface near oxygen vacancies and it likely inhibits the creation of additional oxygen vacancies.

The next aim was to understand the physical mechanism leading to improved device performance after aging. In a first step, the crucial role of oxygen in the platinum oxide Schottky barrier contacts for the aging was ascertained. For that purpose, two  $[\text{Pt}]_3\text{ZTO}$  thin films were deposited by  $[\text{Pt}]_3\text{PLD}$  from a single composition target on  $10 \times 10 \text{ mm}^2$  Corning 1737 glass substrates with an offset of  $\epsilon = 10 \text{ mm}$ . The thin films were deposited under an oxygen atmosphere of 0.035 mbar and have a thickness of about 300 nm as determined by a profilometer measurement, using a Bruker *DEKTAK XT*. The free carrier density was measured as  $5.5 \times 10^{17} \text{ cm}^{-3}$ , the mobility as  $\mu = 3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and the cation composition is approximately  $0.3 \text{ Zn}/(\text{Zn}+\text{Sn})$ . The two thin films are called A and B in the following.

Thin film A was divided in four equal  $5 \times 5 \text{ mm}^2$  pieces to investigate three different atmospheres during the reactive dc-sputtering of the platinum oxide. Namely, the platinum oxide was sputtered under 20/80 sccm oxygen/argon, under 50/50 sccm oxygen/argon and under 80/20 sccm oxygen/argon. The sputtering time was held constant at 15 s for all three configurations. The platinum oxide was capped with a metallic platinum layer sputtered under



**Figure 4.11:** Exemplary current density-voltage characteristics for three different atmospheres during the deposition of the platinum oxide Schottky barrier contacts. The as deposited (solid line) and aged for 30 days (dashed line) characteristics are depicted.

**Table 4.2:** Absolute value of the reverse current density at  $-1.5$  V and rectification ratio for the as deposited and aged state for three different atmospheres during the reactive sputtering of the platinum oxide Schottky barrier contacts. The values correspond to the current density-voltage characteristics shown in Figure 4.11.

atmosphere during PtO <sub>x</sub> deposition	$ j _{-1.5 \text{ V, as dep.}}$	$ j _{-1.5 \text{ V, 30 days}}$	$S_V, \text{ as dep.}$	$S_V, 30 \text{ days}$
oxygen/argon	A cm <sup>-2</sup>	A cm <sup>-2</sup>		
20/80 sccm	$2.6 \times 10^{-1}$	$9.1 \times 10^{-3}$	3	41
50/50 sccm	$1.8 \times 10^{-2}$	$3.8 \times 10^{-4}$	13	675
80/20 sccm	$7.8 \times 10^{-5}$	$7.9 \times 10^{-8}$	$6.6 \times 10^3$	$4.0 \times 10^6$

100 sccm argon for 10 s for all samples. The resulting current density-voltage characteristics are shown in Figure 4.11 for the as deposited and aged state. The forward current (at  $+1.5$  V) of the three samples is very similar for as deposited and aged characteristics. As described before, this can be attributed to the identical thin film on which the diodes were fabricated. A slightly smaller current density is observed at  $+1.5$  V for higher oxygen contents in the plasma during the sputtering.

The reverse current of the Schottky barrier diodes differs significantly for the three platinum oxide deposition conditions. A strong decrease of the reverse current is observable with increasing oxygen content in the plasma during the platinum oxide deposition (compare Figure 4.11. The current density at  $-1.5$  V and the rectification ratio in the as deposited and aged for 30 days state for the here investigated Schottky barrier diodes are summarized in Table 4.2. A decrease by about four orders of magnitude of the reverse current at  $-1.5$  V is observed for increasing oxygen content in the plasma during the reactive sputtering. A value of  $|j| =$

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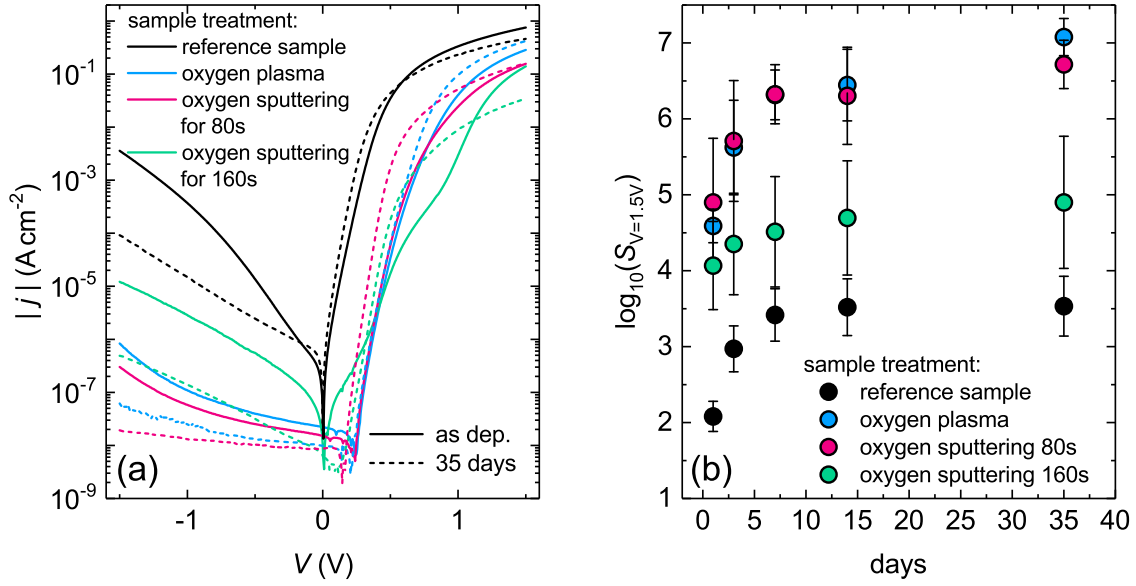
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$2.6 \times 10^{-1} \text{ A cm}^{-2}$  is obtained for a gas mixture of 20/80 sccm oxygen/argon and a value of  $7.8 \times 10^{-5} \text{ A cm}^{-2}$  for 80/20 sccm oxygen/argon. This is also reflected in the rectification ratio, which increases by three orders of magnitude for an increase of 20 sccm to 80 sccm oxygen in the plasma during the platinum oxide deposition. The reverse current of the current density-voltage characteristics exhibits, as already observed in chapter 4.2, an exponential voltage dependence.

After a storage time of 30 days, the Schottky barrier diodes were re-measured. For all three plasma compositions, a decrease of the reverse current was measured, as was already observed in the previous section. The decrease of the reverse current scales with the oxygen content in the plasma during the reactive sputtering. For an oxygen content of 20 sccm in the plasma, a decrease of the reverse current by 1.5 orders of magnitude is observed, whereas for 80 sccm oxygen, a decrease by three orders of magnitude is observed in the same time span. Due to the unchanged forward current at +1.5 V, the same tendency is seen in the rectification ratio (see Table 4.2). The lowest reverse current in the as deposited and aged state is observed for a platinum oxide deposition under 80/20 sccm oxygen/argon. This Schottky barrier diode also exhibits the highest rectification ratio of  $4.0 \times 10^6$  after 30 days. Furthermore, the shift of the onset of the reverse tunneling current shifts by about 0.5 V from  $-0.5 \text{ V}$  to  $-1 \text{ V}$ .

The decrease of the reverse current with increasing oxygen content in the plasma during the reactive platinum sputtering demonstrates the important role of oxygen for the formation of highly rectifying contacts. A similar study was performed on zinc oxide, where a decrease of the reverse current with increasing oxygen content in the plasma during the reactive sputtering of platinum, palladium and iridium was observed [89]. In this work, the strongest decrease of the reverse tunneling current was observed for the highest oxygen content in the plasma during the platinum oxide deposition. A reason for this might be the saturation of interface near oxygen vacancies during the reactive sputtering and a further diffusion of oxygen from the platinum oxide to the  $\text{Pt}/\text{ZTO}$  over time. A higher amount of oxygen in the plasma would lead to a more effective saturation of oxygen vacancies. Moreover, for higher oxygen contents, a higher amount of oxygen might be incorporated in the platinum oxide where it forms a reservoir. Consequently, the largest oxygen reservoir is formed for the highest oxygen content in the plasma during the sputtering and therefore these diodes show the strongest improvement over time.

A further step to investigate this effect was done by a comparison of the influence of different surface treatments of as deposited  $\text{Pt}/\text{ZTO}$  thin films on the properties of Schottky barrier diodes based thereon. Accordingly, the four  $5 \times 5 \text{ mm}^2$  pieces of sample B were prepared. On each piece a platinum oxide contact was sputtered under an atmosphere of 50/50 oxygen/argon for 15 s and capped with metallic platinum sputtered under 100 sccm argon for 10 s. This contact stack is denoted as  $\text{PtO}_x/\text{Pt}$ . Previous to the platinum oxide deposition, the Schottky contact area of the sample surfaces were treated differently. The first sample was exposed to an oxygen plasma treatment (OPT sample) with a power of 50 W for 60 s with the aim to saturate oxygen vacancies at the sample surface. The second sample



**Figure 4.12:** Mean current density-voltage characteristics (a) for four different contact configurations in the as deposited and aged state. Logarithm of the rectification ratio (b) for times between as deposited and 35 days storage.

was coated by a reactively sputtered platinum oxide layer that was deposited under 100 sccm oxygen for 80 s prior to the PtO<sub>x</sub>/Pt contact (OS-80 s sample). This was done to enlarge the oxygen reservoir and also to saturate oxygen vacancies at the surface of the [! (!)3]ZTO thin film. The same treatment but a sputtering time of 160 s was used for the third sample (OS-160 s sample). The fourth sample had a standard PtO<sub>x</sub>/Pt contact and is used as reference to the other three samples (reference sample).

In Figure 4.12, the mean current density-voltage characteristics for the four samples are depicted. The mean characteristics were obtained from all working contacts on each sample piece (approximately 10 contacts). A detailed look at the current in the forward regime at +1.5 V yields that the reference sample has a higher forward current compared to the OPT, the OS-80 s and the OS-160 s sample. This decrease in the forward current at +1.5 V is similar to what one observes if a thin intrinsic [! (!)3]ZTO layer is introduced between the [! (!)3]ZTO thin film and the platinum oxide [7, 18]. This indicates that if the provided amount of oxygen is high enough, a thin intrinsic [! (!)3]ZTO surface layer forms due to a saturation of oxygen vacancies. In the reverse regime at -1.5 V, the mean current density of the reference sample is  $|\bar{j}| = 3.3 \times 10^{-3} \text{ A cm}^{-2}$ . For the OPT and the OS-80 s sample, it is about four orders of magnitude lower and values of  $|\bar{j}| = 8.4 \times 10^{-7} \text{ A cm}^{-2}$  and  $|\bar{j}| = 2.6 \times 10^{-7} \text{ A cm}^{-2}$  are obtained. For these two methods, the characteristics are very similar in the as deposited state. The OS-160 s sample exhibits a higher mean reverse current of  $|\bar{j}| = 1.2 \times 10^{-5} \text{ A cm}^{-2}$  at -1.5 V and the forward regime of the Schottky barrier diode characteristics exhibits two barriers instead of one. This indicates that the barrier height is fluctuating, which also leads to the increased tunneling current in the reverse direction. In crystalline zinc oxide a similar

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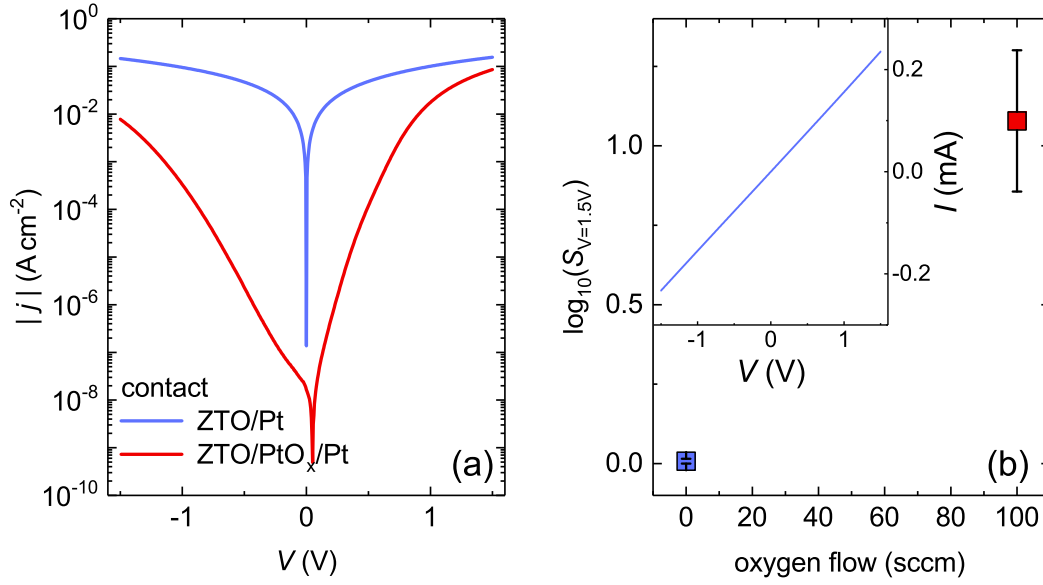
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effect was observed if the particle energy of the particles during the reactive sputtering was so high that they induced defects [84,90]. However, it is unlikely that this plays a role in these samples, as the OS-80s sample does not exhibit two barriers. The origin of the two barriers is therefore not understood in this case.

The mean rectification ratio increases from about 120 for the reference sample to  $3.9 \times 10^4$  and  $7.9 \times 10^4$  for the OPT and the OS-80s sample, respectively. The OS-160s sample has a rectification ratio of  $1.2 \times 10^4$ , which can be attributed to the high reverse current combined with the lower current density at +1.5 V. From the characteristics it can be concluded that an oxygen plasma treatment and oxygen sputtering for 80 s have similar effects on the rectifying behavior of ZTO/PtO<sub>x</sub> Schottky barrier diodes. In contrast, an oxygen sputtering for 160 s leads to inferior diode characteristics and a reduced rectification ratio compared to the OPT and OS-80s sample.

The Schottky barrier diodes were re-measured after predefined time spans to monitor the long term stability. The current density-voltage characteristics of the Schottky barrier diodes stored for 35 days are depicted in Figure 4.12 (a). The rectification ratios for each re-measurement are shown in Figure 4.12 (b). For the reference sample a decrease of the reverse current is observed, as expected from previous results. The further decrease of the reverse current of the OPT sample, even though a saturation of interface near oxygen vacancies was sought by the plasma treatment, can be explained by the deposition of platinum oxide on the pre-treated surface. This platinum oxide layer acts as an oxygen reservoir, which may allow for a further saturation of interface near oxygen vacancies over time. This permits the reverse conclusion that the oxygen plasma treatment did not achieve a total compensation of interface near oxygen vacancies or that oxygen diffuses further into the [Pt]/ZTO. The same is true for the OS-80 and OS-160s sample, which also exhibit a decrease of the reverse current after a storage time of 35 days. In the forward regime of the OS-160s sample, a uniform, exponential voltage dependence of the current is observed after this storage time. This indicates that the influence of the second barrier is no longer detectable and that defects, which may have been induced during the surface treatment, have healed out. Further, this sample exhibits a by one order of magnitude decreased forward current at +1.5 V after 35 days. This may be due to an enhancement of the formation of a thin intrinsic [Pt]/ZTO layer between [Pt]/ZTO thin film and metal oxide contact. It is not clear why this effect is seen for this surface treatment only. A high defect density in the as deposited state may promote the formation of an intrinsic [Pt]/ZTO layer of a higher thickness compared to the other surface treatment methods.

Son *et al.* have observed a similar behavior for bottom gate Schottky barrier diodes to amorphous solution processed ZTO. In their study, a palladium bottom contact was treated by an oxygen plasma to achieve a higher rectification ratio of the resulting Schottky barrier diodes [80]. They argue that a diffusion of oxygen from the palladium oxide into the [Pt]/ZTO leads to the improved rectifying behavior [80]. A similar effect appears to be responsible for the higher rectification of the PtO<sub>x</sub>/ZTO Schottky barrier diodes investigated in this work. The ensuing goal is to verify this hypothesis.

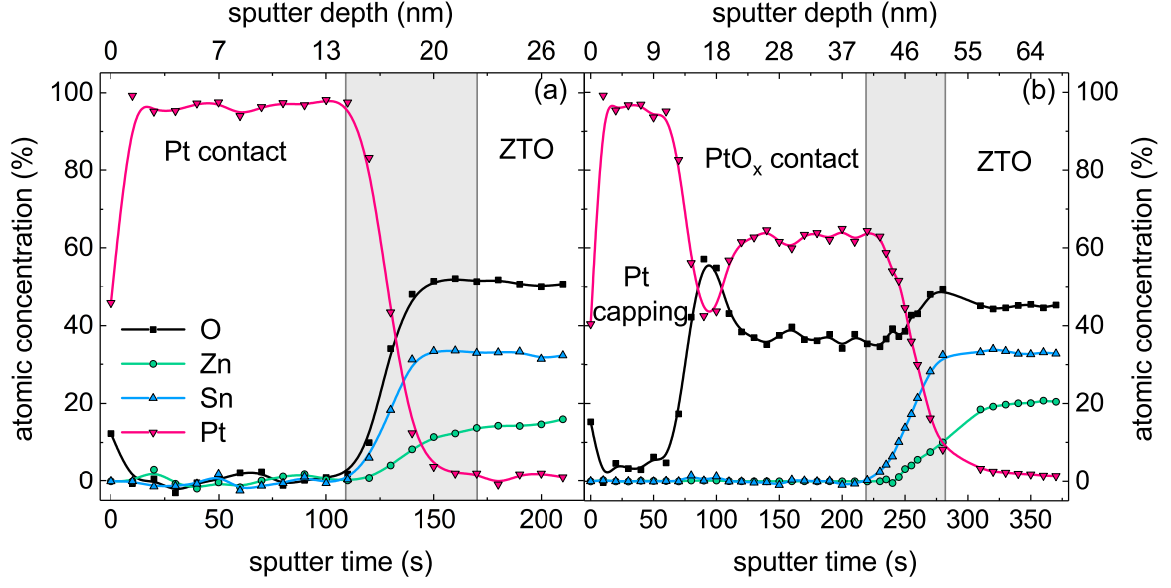


**Figure 4.13:** Current density-voltage characteristics (a) for a ZTO/Pt and a ZTO/PtO<sub>x</sub>/Pt contact and corresponding logarithmic rectification ratio (b). The inset in (b) shows a linear representation of the current-voltage characteristics of the ZTO/Pt contact.

## 4.5 Processes Governing the Long Term Stability

The next aim was to further gauge the influence of interface near oxygen vacancies on the rectifying behavior of ZTO based Schottky barrier diodes and to gain information on the processes leading to an improvement over time of the diodes. Therefore, five [! (!)3]ZTO thin films were deposited from a single composition target by [! (!)3]PLD. The thin films were deposited on 10 × 10 mm<sup>2</sup> Corning 1737 glass substrates with an oxygen background pressure of 0.025 and 0.035 mbar and an offset  $\epsilon = 24$  mm. With the profilometer Bruker *DEKTA XT*, the thin film thickness was measured as approximately 300 nm. Hall-effect measurements were employed to determine the free carrier density and the resistivity of the [! (!)3]ZTO thin films as  $3 \times 10^{17} \text{ cm}^{-3}$  and  $6.5 \Omega \text{ cm}$ , respectively. Compared to the results of thin films I-IV, the Hall mobility is comparably low with about  $3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ .

The [! (!)3]ZTO thin films were prepared for the investigation by [! (!)3]XPS and concurrent current-voltage measurements on Schottky barrier diodes [E4]. For the four [! (!)3]XPS samples, the metal (or alternatively the metal oxide) was deposited laminar on the whole sample, while the Schottky barrier contacts were structured by photolithography as described before. For the Schottky barrier diode investigations, one 10 × 10 mm<sup>2</sup> sample was divided into two pieces to ensure the highest possible comparability of the results. Two different contact compositions were chosen for the contact metal of the [! (!)3]XPS samples and the Schottky barrier diode samples. The first contact configuration was metallic platinum which was sputtered under 100 sccm argon for 20 s. This is denoted as ZTO/Pt contact in the following. The second contact composition was reactively sputtered platinum with a platinum



**Figure 4.14:** Depth resolved elemental composition of the ZTO/Pt (a) and ZTO/PtO<sub>x</sub>/Pt (b) contact. The gray area indicates the interface region.

capping, which is denoted as ZTO/PtO<sub>x</sub>/Pt contact. The platinum oxide contacts were sputtered under 100 sccm oxygen for 80 s and subsequently capped with a metallic platinum layer sputtered under 100 sccm argon for 20 s. The [! ([!)]XPS measurements were performed and analytically evaluated by Thorsten Schultz at the HU Berlin.

In Figure 4.13 (a), the current density-voltage characteristics for a ZTO/Pt contact and a ZTO/PtO<sub>x</sub>/Pt contact are depicted. A similar forward current density at +1.5 V is measured for the two samples. In this regime the current flow is limited by the thin film resistivity. As both contact compositions were fabricated on halves of the same sample, the thin film resistance is identical as expected. The reverse current at −1.5 V differs strongly for the two contact compositions. For the ZTO/Pt contact a value of  $|j| = 150 \text{ mA cm}^{-2}$  is measured, whereas it is as low as  $|j| = 8 \text{ mA cm}^{-2}$  for the ZTO/PtO<sub>x</sub>/Pt contact. As shown in the inset in Figure 4.13, the ZTO/Pt contact exhibits an ohmic behavior. The reverse current of the ZTO/PtO<sub>x</sub>/Pt contact exhibits an exponential voltage dependence. Mean rectification ratios, obtained at  $\pm 1.5 \text{ V}$ , are zero and one order of magnitude for the ZTO/Pt and ZTO/PtO<sub>x</sub>/Pt contact, respectively. The characteristics were fitted with equation 2.18, however only the Schottky diodes with reactively sputtered platinum could be fitted. An ideality factor of  $\eta = 1.6$  and an effective barrier height of  $\phi_{B,\text{eff}} = 0.9 \text{ eV}$  were obtained. Two samples with identical ZTO/Pt and ZTO/PtO<sub>x</sub>/Pt contacts deposited on the entire sample surface were investigated by [! ([!)]XPS by Thorsten Schultz<sup>7</sup>. The compositional depth profiles obtained from his measurements are depicted in Figure 4.14.

For the ZTO/Pt contact, the approximately 15 nm thick platinum contact is followed by

<sup>7</sup>Humbolt-Universität zu Berlin

an interface regime and subsequently the ZTO thin film. In the interface regime a strong decrease of the platinum signal and a simultaneous increase of the oxygen, zinc and tin signal are measured. In comparison, for the ZTO/PtO<sub>x</sub>/Pt contact, the platinum capping layer with a thickness of approximately 15 nm is followed by an about 20 nm thick PtO<sub>x</sub> contact. At the interface between PtO<sub>x</sub> and ZTO (gray area in Figure 4.14 (b)), an increase of the oxygen, zinc and tin content with a simultaneous decrease of the platinum content is visible.

In the depth profile of the ZTO/PtO<sub>x</sub>/Pt contact it appears as if a local maximum of the oxygen content is obtained at the interface. This was further investigated by a detailed examination of the binding energies. In Figure 4.15, the core level peaks with the corresponding fitting for the Pt 4*f*, the O 1*s* and the Sn 3*d*<sub>5/2</sub> core level are shown for the interface region of the ZTO/Pt and the ZTO/PtO<sub>x</sub>/Pt contact.

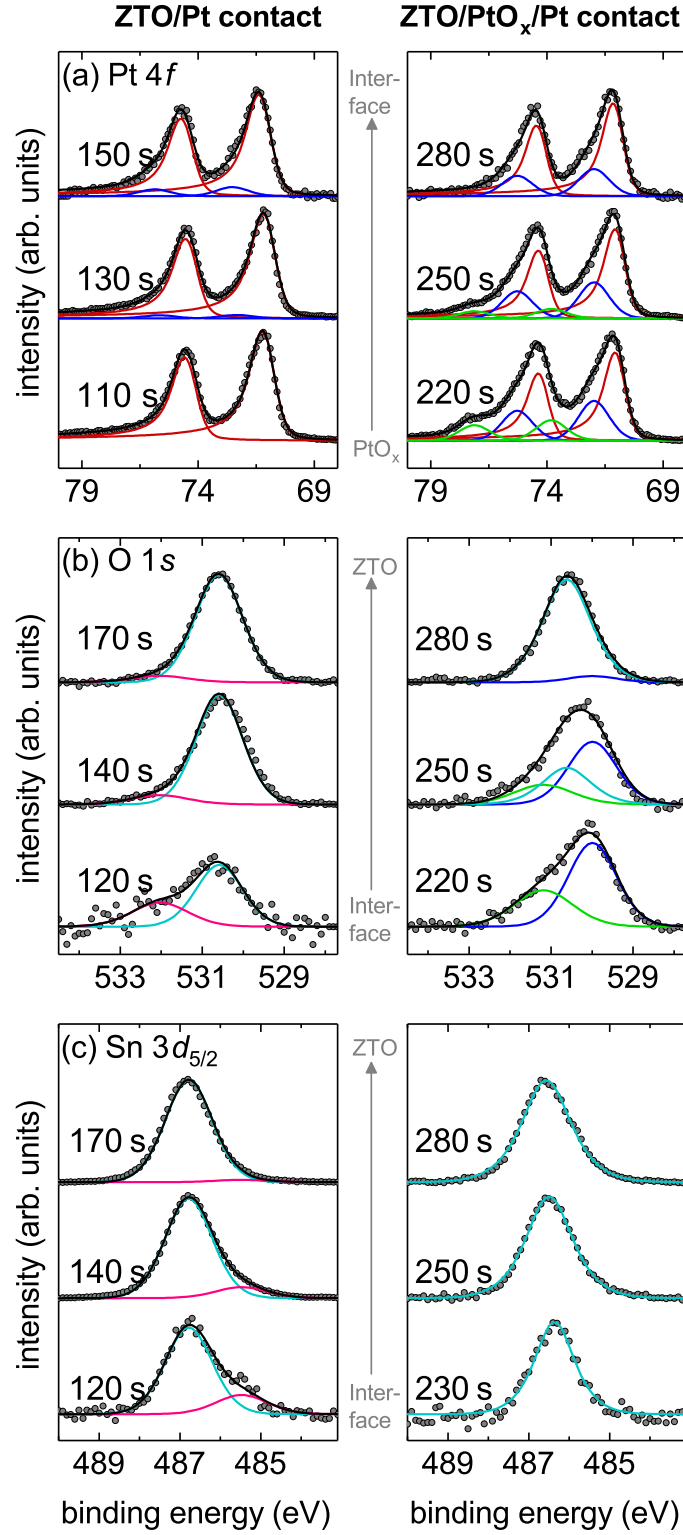
If one has a detailed look at the Pt 4*f* core levels of the ZTO/Pt contact, a doublet peak (red line) is observed in the platinum away from the interface. This can be attributed to metallic platinum. Going towards the interface, a small PtO contribution (blue line) becomes visible (compare Figure 4.15 (a)).

This indicates an oxidation of the metallic platinum contact at the interface or, in other words, a slight reduction of the [!] ([!])<sub>3</sub>ZTO by the metallic platinum. Going further from the interface towards the ZTO, the O 1*s* core level shows a decreasing shoulder, which can be allocated to oxygen vacancies (pink line) (compare Figure 4.15 (b)) [80]. The shoulder height is highest at the interface to the platinum contact and vanishes in the bulk [!] ([!])<sub>3</sub>ZTO. At the same time, the Sn 3*d*<sub>5/2</sub> core level (turquoise line) also has an additional shoulder with a lower binding energy at the interface (compare Figure 4.15 (c)). This can be attributed to tin atoms close to an oxygen vacancy [104].

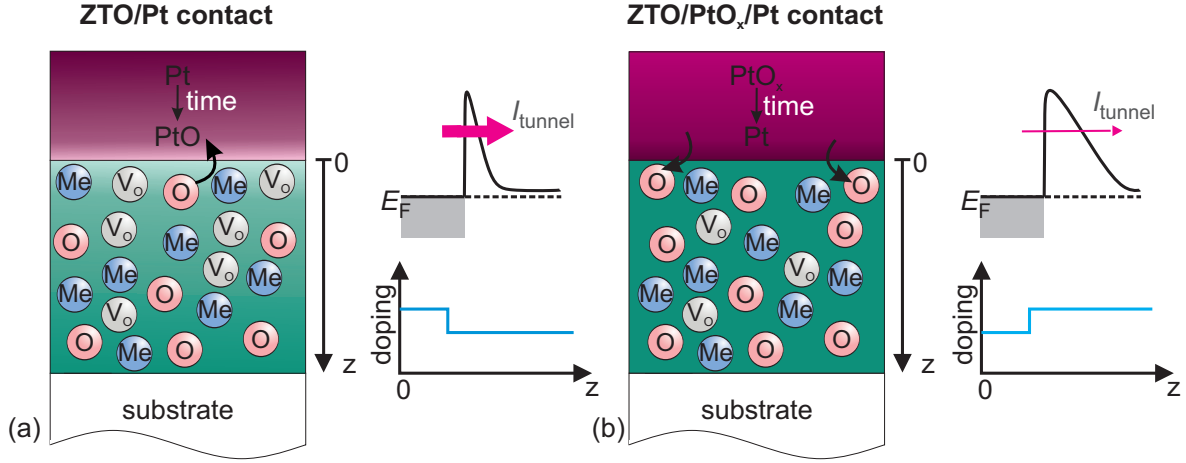
These results indicate that for the ZTO/Pt contact a diffusion of oxygen from the ZTO to the platinum takes place, as evidenced by the PtO peak and the peak ascribed to tin atoms in the vicinity of an oxygen vacancy in the interface region (compare Figure 4.15 (b),(c)). The increased oxygen vacancy density at the interface of the ZTO results in an increased free carrier density in this area. This leads to a reduced depletion region width, which allows for tunneling of electrons through the barrier.

With these insights, the ohmic behavior of the current density-voltage characteristics of the ZTO/Pt contact in Figure 4.13 can be explained. The reduced depletion region width due to a higher oxygen vacancy density allows for the tunneling of electrons through the barrier and therefore the formation of an ohmic contact between platinum and ZTO.

A schematic image of the diffusion of oxygen from the [!] ([!])<sub>3</sub>ZTO to the platinum is shown in Figure 4.16 (a). An oxygen atom diffusing from the [!] ([!])<sub>3</sub>ZTO into the platinum leaves an oxygen vacancy in its former place.



**Figure 4.15:** Core levels of the (a) Pt 4f, (b) O 1s and (c) Sn 3d<sub>5/2</sub> for the ZTO/Pt contact (left panel) and the ZTO/PtO<sub>x</sub>/Pt contact (right panel). The sputter times correspond to the interface region marked in gray in Figure 4.14. The Pt peak is fitted in red, the PtO peak in blue, the Pt(OH)<sub>4</sub> peak in green, the ZTO peak in turquoise and the oxygen vacancy in pink.



**Figure 4.16:** Schematic drawing of the oxygen diffusion and the resulting barrier height and approximated doping profile for (a) the ZTO/Pt and (b) the ZTO/PtO<sub>x</sub>/Pt contact.

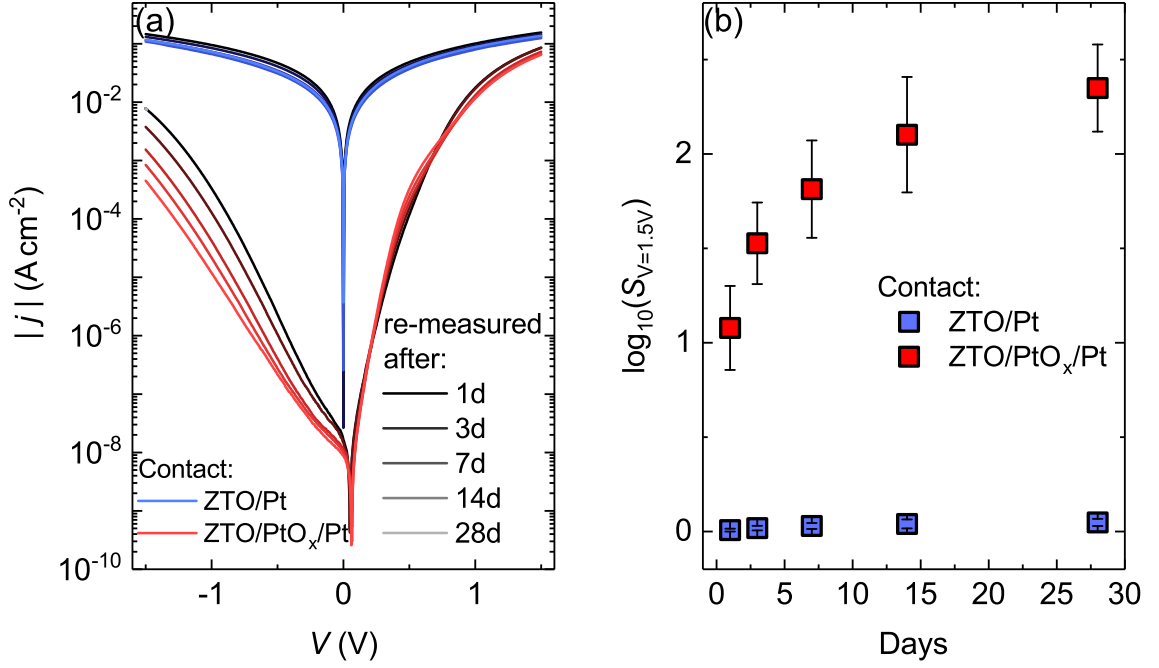
In contrast, for the ZTO/PtO<sub>x</sub>/Pt interface, no shoulder is visible in the Sn 3d<sub>5/2</sub> core level. Only one peak is detectable, which can be assigned to the bulk ZTO Sn 3d<sub>5/2</sub> level. For the O 1s core level, a contribution from an oxygen binding to platinum and to [! (!)3]ZTO is visible in the interface region. Going from the interface into the [! (!)3]ZTO thin film this contribution reduces, as expected, and only the peak for oxygen bound in the bulk [! (!)3]ZTO remains. The Pt 4f core level exhibits three peaks in the platinum oxide away from the interface. A doublet peak, which can be attributed to metallic platinum, a doublet pair of peaks with were assigned to PtO and a second pair of peaks, which come from Pt(OH)<sub>4</sub> [105]. Towards the interface, the small peak assigned to Pt(OH)<sub>4</sub> (green line), decreases and only the metallic platinum (red line) and PtO (blue line) peak remain. For the ZTO/PtO<sub>x</sub>/Pt contact, a diffusion of oxygen from the platinum oxide into the ZTO near the interface is detected (compare Figure 4.15 (b),(c)).

This leads to a saturation of oxygen vacancies in the ZTO and therefore reduces the free carrier density at the interface [106]. A lower free carrier density leads to a wider depletion region width and a reduced tunneling probability through the barrier. In the current density-voltage characteristics this is seen in the decreased reverse current of the ZTO/PtO<sub>x</sub>/Pt Schottky barrier diode as depicted in Figure 4.13. A similar effect was described for crystalline zinc oxide [89,102].

A schematic representation of this process is given in Figure 4.16 (b). A diffusion of oxygen from the platinum oxide near the interface into the [! (!)3]ZTO is observed, which saturates under-coordinated cations.

For bottom gate palladium oxide contacts to [! (!)3]ZTO, a reduction of the palladium oxide to metallic palladium after thermal annealing of the Schottky barrier diodes was observed by Son *et al.* [80].

As described in the previous sections, not only the oxygen content in the plasma during the reactive sputtering of the platinum contact is of importance for the formation of highly

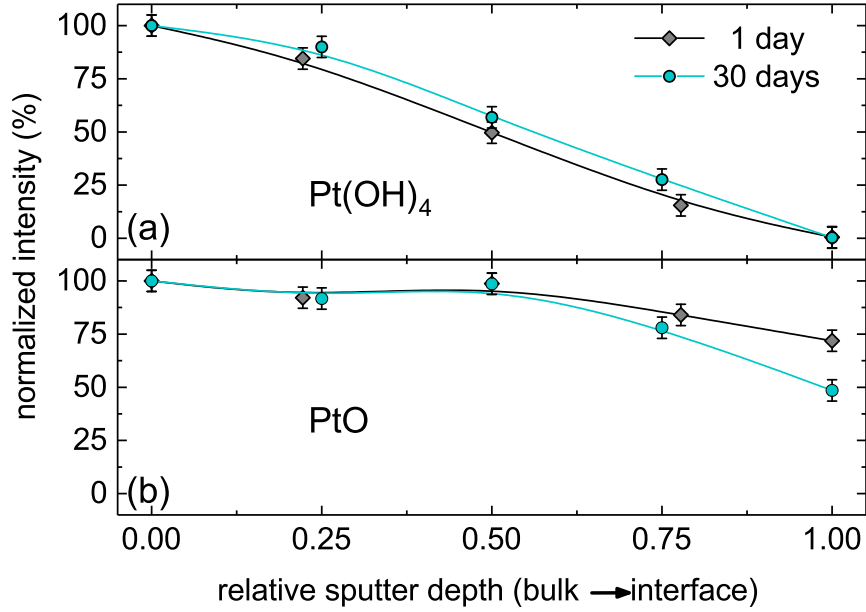


**Figure 4.17:** Current density-voltage characteristics (a) and mean rectification ratio (b) for a ZTO/Pt and a ZTO/PtO<sub>x</sub>/Pt Schottky barrier diode.

rectifying contacts, but also the storage time of the devices. Current-voltage measurements were repeated after 3, 7, 14 and 28 days on the ZTO/Pt and the ZTO/PtO<sub>x</sub>/Pt Schottky barrier diodes. In Figure 4.17 (a), the current density-voltage characteristics for both contact configurations are depicted. For the ZTO/Pt contact no change in either the forward or the reverse direction of the characteristics is observed. They remain unaltered upon a storage time of 28 days. The same result is obtained for the mean rectification ratio, which remains at zero orders of magnitude (compare Figure 4.17 (b)). The ZTO/Pt Schottky barrier diodes on this sample are very homogeneous as visible from the small standard deviation from the mean rectification.

In comparison, the ZTO/PtO<sub>x</sub>/Pt Schottky barrier diode exhibits the expected decrease of the reverse tunneling current over the 28 days. A decrease of the current density at  $-1.5$  V by more than one order of magnitude from  $|j| = 7.78 \text{ mA cm}^{-2}$  (1 day) to  $|j| = 0.45 \text{ mA cm}^{-2}$  (28 days) is measured. This leads to an increase of the mean rectification ratio up to a value of 223 after 28 days. The homogeneity of the ZTO/PtO<sub>x</sub>/Pt Schottky barrier diodes remains similar for the as deposited and aged devices. The effective barrier height is unaltered after 28 days, which means that the work function of the zinc tin oxide and platinum oxide do not change upon aging. The reverse tunneling current decreases because of a reduced tunneling probability due to an increased depletion region width. As discussed for the as deposited contacts, a reduced amount of oxygen vacancies at the interface may lead to a reduced free carrier density in the interface region and therefore to a wider depletion region width [E4].

In chapter 4.4 it was shown that diodes with the highest oxygen content in the plasma during



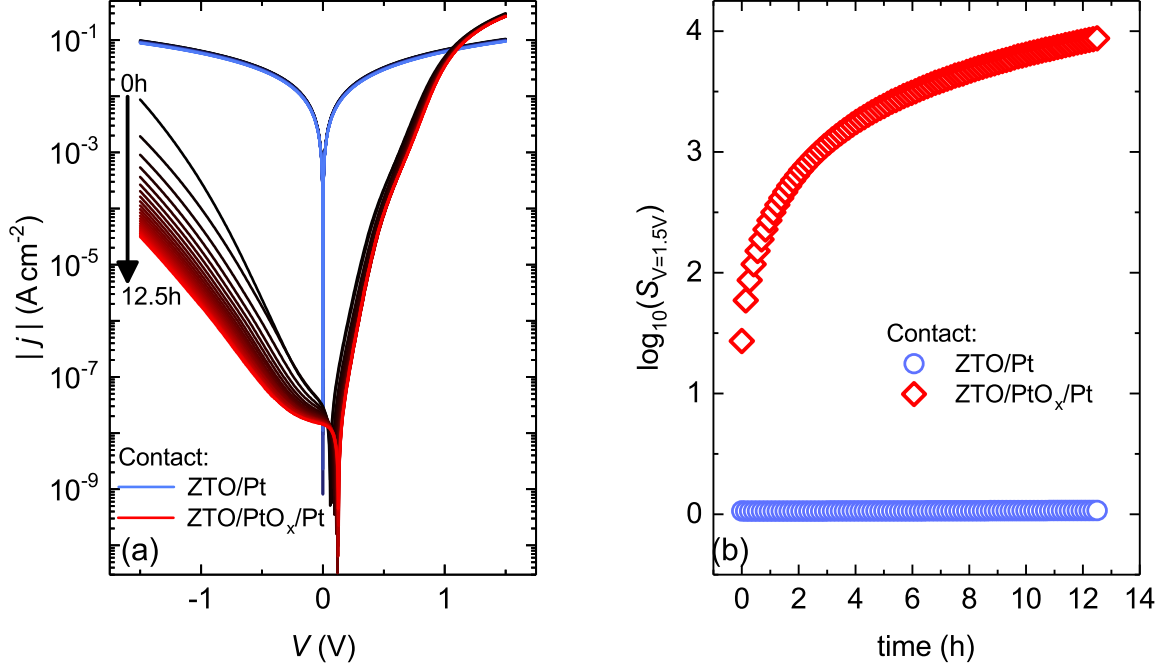
**Figure 4.18:** Change of the  $\text{Pt(OH)}_4$  (a) and  $\text{PtO}$  (b) contribution to the Pt 4f core level for an aged 1 day and aged 30 days ZTO/ $\text{PtO}_x$ /Pt contact.

the platinum oxide deposition exhibited the most pronounced improvement upon aging. This may be due to a further diffusion of oxygen from the platinum oxide into the  $[\text{ZTO}]$  near the interface. The vastly different rectifying behavior of the ZTO/Pt and ZTO/ $\text{PtO}_x$ /Pt Schottky barriers upon aging support this hypothesis.

To verify the hypothesis of an oxygen diffusion from the  $\text{PtO}_x$  into the ZTO, two identical samples with a ZTO/ $\text{PtO}_x$ /Pt contact were investigated by depth-resolved  $[\text{Pt}]$ XPS. The first sample was measured one day and the second sample 30 days after the contact deposition. In Figure 4.18, the relative change of the PtO and  $\text{Pt(OH)}_4$  contributions to the Pt 4f core level peak at the interface are depicted for both contact configurations. A similar decrease of the amount of  $\text{Pt(OH)}_4$  towards the  $\text{PtO}_x$ /ZTO interface is observable for the as deposited and the aged sample. As the  $\text{Pt(OH)}_4$  contribution to the Pt 4f core level peak can be detected in the  $\text{PtO}_x$  layer away from the interface, a diffusion of oxygen (and hydrogen) into the  $[\text{ZTO}]$  at the interface is likely. This process takes place in less than 24 hours, as this is the elapsed time between the contact deposition and the  $[\text{Pt}]$ XPS measurement on the first sample. It leads to the improved behavior of the ZTO/ $\text{PtO}_x$ /Pt compared to the ZTO/Pt Schottky barrier diodes.

The PtO contribution to the Pt 4f core level peak also decreases towards the ZTO interface. However, the reduction of the PtO seems to be a slower process, which explains the improvement of the ZTO/ $\text{PtO}_x$ /Pt Schottky barrier diode over time. It has to be expected that the improvement of the diodes continues until all interface near oxygen vacancies are saturated or the oxygen reservoir in the platinum oxide is depleted.

The next question was, whether this aging may be evoked and expedited in some way. Thus,



**Figure 4.19:** Selected current density-voltage characteristics (a) for a ZTO/Pt and a ZTO/PtO<sub>x</sub>/Pt Schottky barrier diode for a negative bias application of  $-1.5$  V for 0 up to 12.5 h. Change of the rectification ratio (b) with bias application time.

the aim in the following was to accelerate the diffusion of the oxygen into the ZTO. Therefore a negative voltage of  $-1.5$  V was applied for 500 s at the Schottky barrier contact between consecutive current-voltage measurements. The bias applications and measurements were repeated 90 times up to a total bias application time of 12.5 h. The current density-voltage characteristics for different times of the negative bias application to the ZTO/Pt and a ZTO/PtO<sub>x</sub>/Pt contact are depicted in Figure 4.19 (a). For the ZTO/Pt contact no change in the characteristics is visible, as was also the case for the aging. In contrast, for the ZTO/PtO<sub>x</sub>/Pt contact, a strong decrease of the reverse current at  $-1.5$  V is observable. It decreases from a value of  $8.5 \times 10^{-3}$  A cm<sup>-2</sup> before the bias application to a value of  $3.0 \times 10^{-5}$  A cm<sup>-2</sup> after 12.5 h of negative bias application. Similar as for the aging, the forward current at  $+1.5$  V remains unaltered. The rectification ratio of the ZTO/Pt contact is zero orders of magnitude for all bias application times. In contrast, the rectification ratio of the ZTO/PtO<sub>x</sub>/Pt Schottky barrier diode increases from a value of 27 to a value of  $8.7 \times 10^3$  after 12.5 h bias application.

The diodes were re-measured after the bias application and exhibited stable behavior after this treatment. However, it has to be expected that if the oxygen reservoir is large enough, this improvement of the diodes will continue. A longer total bias application time may be required to achieve a saturation of the device improvement in this case.

Dang *et al.* observed an improvement of transistors based on amorphous [! (!)3]ZTO by the application of a moderate thermal stress simultaneous to the bias application [14]. This

might also be used to improve the devices investigated here, as will be shown for [! (!)3]rf-magnetron sputtering deposited [! (!)3]ZTO thin films. The change of device properties with time of [! (!)3]ZTO based devices was shown for pulsed laser deposited, magnetron sputtered and mist-[! (!)3]CVD amorphous [! (!)3]ZTO thin films with a metal oxide or *p*-type amorphous oxide semiconductor contact [14, 18] [E4, E5].

These investigations show two several approaches can be used to achieve highly rectifying Schottky barrier diodes on amorphous [! (!)3]ZTO. A reactive sputtering in an atmosphere with high oxygen content or an oxygen plasma treatment of the [! (!)3]ZTO surface lead to good rectifying behavior in the as deposited state. To further improve this, the application of a negative bias at the Schottky barrier contact can be used as well as a storage of the devices in ambient atmosphere. Further, the additional use of thermal stress may lead to a faster improvement as demonstrated by Dang *et al.* [14].

## Chapter 5

# Demonstration and Characterization of Zinc Tin Oxide Based Devices

In the previous chapter, the basic physical properties of amorphous  $\text{Zn}_{1-x}\text{Sn}_x\text{O}$  thin films fabricated by PLD and rectifying contacts thereon were investigated. An advantage of this method is the possibility to quickly deposit<sup>1</sup> thin films using the CCS approach to survey over a large number of cation compositions within one sample [107, 108] [E1, E2]. However, the substrate size restriction of the deposition process limits the possibility of applications in industry.

The deposition of thin films by sputtering is an advantageous method for industrial and commercial uses. The deposition by sputtering in roll-to-roll fabrications has been proposed as an alternative to ink-jet fabrication as it is an easily scalable deposition technique [70, 109-111]. In this thesis, the sputtering deposition of  $\text{Zn}_{1-x}\text{Sn}_x\text{O}$  shall be used to investigate  $\text{Zn}_{1-x}\text{Sn}_x\text{O}$  based devices such as FETs and integrated circuits based on FETs and diodes. Sputtering is a widely used method for the deposition of  $\text{Zn}_{1-x}\text{Sn}_x\text{O}$  channels in MISFETs. The first MISFET having a sputtered  $\text{Zn}_{1-x}\text{Sn}_x\text{O}$  channel was presented by Chiang *et al.* in 2005 [12]. For this device, drain current on-to-off ratios  $I_{\text{ON}}/I_{\text{OFF}}$  as high as  $10^7$  have been achieved. A disadvantage of MISFETs is the large voltage range required to switch the device between on- and off-state, which is due to the substantial voltage drop over the insulator.

Previous works in this group, especially by Heiko Frenzel<sup>2</sup> on sputter deposited  $\text{Zn}_{1-x}\text{Sn}_x\text{O}$  yielded results on highly rectifying Schottky barrier diodes [20]. First attempts of Heiko Frenzel on implementing these Schottky diodes in field-effect transistors were not successful, as will be described in the beginning of chapter 5.1.

The aim of this work was the development and implementation of a sputtering recipe that enables the fabrication of  $\text{Zn}_{1-x}\text{Sn}_x\text{O}$  based FETs. The description of said process is followed by a short general description of the structural, electrical and optical properties of

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<sup>1</sup>Quickly compared to the deposition by long-throw sputtering, which is characterized by low growth rates.

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[! (!)3]ZTO. The main part of this chapter is about the properties of [! (!)3]ZTO based devices and integrated circuits and the optimization thereof, with regards to the gate contact and the channel thickness. In the last part of this chapter, inverter chains and ring oscillators are presented. The device dimensions are given in the chapters. Part of the results presented in this chapter have been published in [E5].

All thin films in this chapter were deposited from a ceramic  $\text{SnO}_2\text{--ZnO}$  sputtering target with a cation composition of  $\approx 0.5 \text{ Zn}/(\text{Zn}+\text{Sn})$ . This leads to thin films with optimal cation composition with regards to Schottky barrier diode rectification and ideality factor as discussed in chapter 4.

The standard substrates used in this chapter are *Eagle XG*  $10 \times 10 \text{ mm}^2$  glass substrates by Corning. Schottky diode FET logic inverter and ring oscillators were deposited on  $10 \times 10 \text{ mm}^2$  quartz glass substrates by Corning.

## 5.1 Implementation of a New Sputtering Recipe

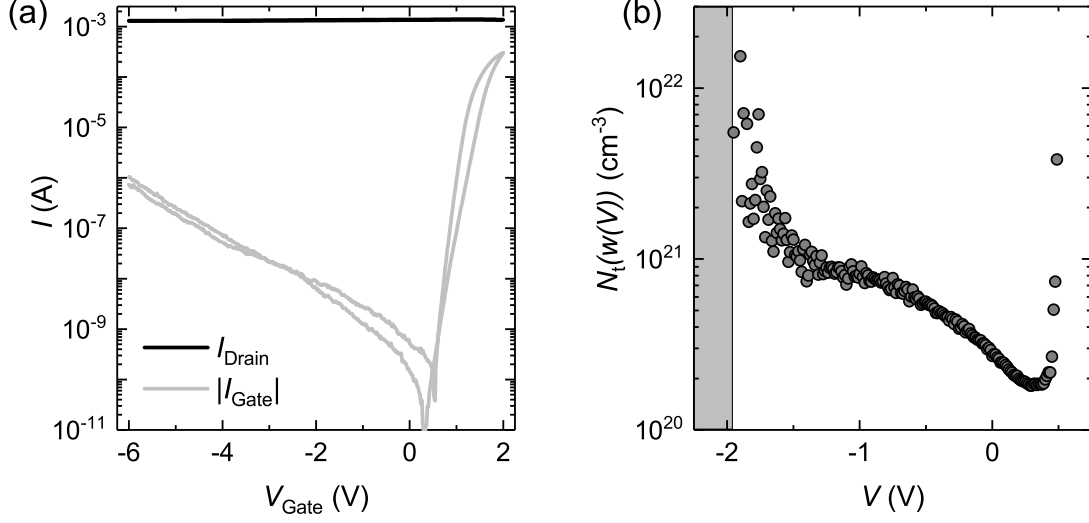
As mentioned above, previous works on amorphous [! (!)3]ZTO deposited by long-throw magnetron sputtering in this work group yielded well working Schottky barrier diodes based on amorphous [! (!)3]ZTO, but no field-effect was visible in MESFETs [20].

An exemplary transfer characteristic and the simultaneously measured gate leakage current are depicted in Figure 5.1 (a) for a MESFET on a [! (!)3]rf-sputtered [! (!)3]ZTO thin film. The drain voltage was chosen as  $V_{\text{Drain}} = 2 \text{ V}$ . A rectification of four orders of magnitude of the Schottky barrier diode is visible in the voltage range of  $-2 \text{ V}$  to  $2 \text{ V}$ , but no field-effect could be detected up to a gate voltage of  $-6 \text{ V}$ , after which it came to a breakthrough of the gate diode. Heiko Frenzel<sup>3</sup> performed capacitance-voltage measurements on a similar [! (!)3]ZTO thin film to gauge why a depletion of the channel could not be achieved. As shown in Figure 5.1 (b), he observed that the doping density  $N_t(w(V))$  strongly increases towards the substrate. The substrate is approached for negative applied voltages. This strong increase of the doping density towards the substrate effectively inhibits the depletion of the channel and therefore no field-effect is visible. The layer having a high doping density will be called highly conductive layer in the following. Heiko Frenzel performed numerous experiments on the influence of the choice of substrate on the capability to deplete the channel. Among other things, he experimented with a pulsed laser deposited and a sputtered intrinsic [! (!)3]ZTO layer below the conductive channel. None of these experiments yielded satisfactory results or a field-effect at all.

The goal of this thesis was to develop a sputtering recipe that inhibits the formation of a highly conductive [! (!)3]ZTO layer at or towards the substrate. A first step was the deposition of a  $p^+$ -doped oxide semiconductor below the [! (!)3]ZTO channel. The semiconducting oxides nickel oxide and zinc cobalt oxide were investigated for this. Both approaches did not succeed,

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**Figure 5.1:** Transfer characteristics and gate leakage current (a) of an approximately 15 nm thick [! (!)3]ZTO thin film and (b) the net doping density  $N_t(V) = N_D - N_A$  in dependence on the voltage applied at the Schottky contact. The gray area is a guide to the eye and illustrates where the substrate begins.

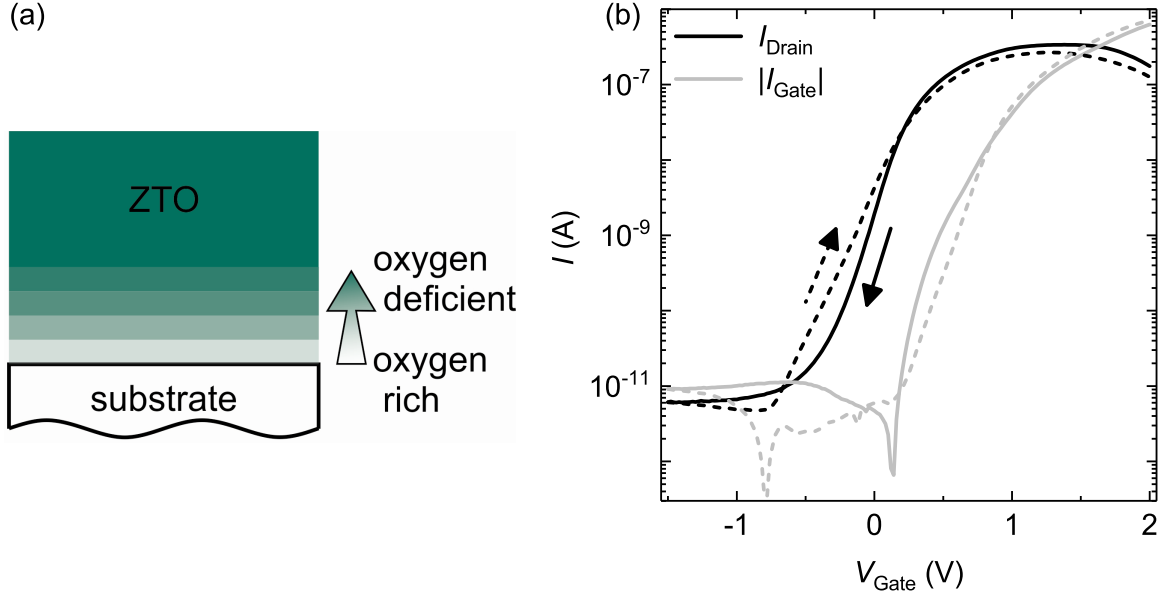
as droplets of the  $p$ -type oxides formed shunts through the [! (!)3]ZTO layer.

In previous experiments, it was found that sputtering of [! (!)3]ZTO thin films in a gas mixture of oxygen and argon leads to non-conductive thin films. The second approach was therefore the start of the sputtering process in an oxygen/argon gas mixture. Subsequently, the oxygen content in the plasma was step-wise reduced. With this process, a reproducible field-effect could be achieved. The quality of the field-effect strongly depends on the step-size. The deposition conditions resulting in the highest drain current on-to-off ratios are shortly described.

A start condition of 25/5 sccm oxygen/argon was chosen. Subsequently, the oxygen flow was decreased (and the argon flow simultaneously increased) by 1 sccm every 30 s until a pure argon atmosphere with a flow of 30 sccm was attained. This leads to a total sputtering time of 750 s and a resulting thickness of approximately 12 nm for the oxygen flow variation layer. Following this oxygen flow variation layer, a conductive channel was sputtered under 30 sccm argon flow for 330 s, which results in a thickness of  $\approx 10$  nm. In Figure 5.2 (a), a schematic drawing of the resulting [! (!)3]ZTO layer is depicted. The individual steps, where the composition of the sputtering gas is changed are depicted by different colors. The resulting transfer characteristics of a FET based on such a thin film is depicted in Figure 5.2 (b). A drain voltage of 2 V was applied during the measurement.

To describe these devices, the effective channel thickness  $d_{\text{eff}}$  is introduced. It is assumed that only the channel deposited under pure argon flow contributes to the current transport and therefore only the thickness of this layer is taken into account for the description of devices and calculations of e.g. the free carrier density.

Experiments yielded that even for very low oxygen contents in the atmosphere during the



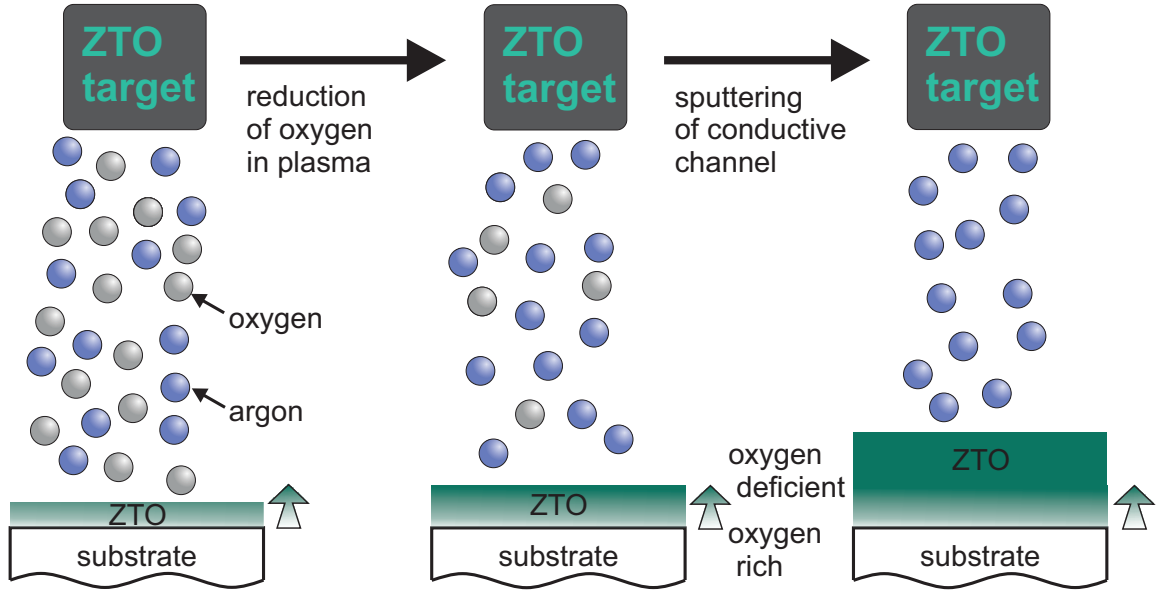
**Figure 5.2:** Schematic drawing (a) of a [! ([!)]3]ZTO channel layer with a step wise alteration of the gas composition during the sputtering process and the subsequent sputtering of the conductive channel in an oxygen deficient atmosphere. The transfer characteristic and gate leakage current (b) for a MESFET with platinum oxide gate contact based on such a channel with an effective channel thickness of  $\approx 10$  nm of the conductive layer and  $W/L = 430 \mu\text{m}/10 \mu\text{m}$ . A drain voltage of 2 V was applied during the measurement of the transfer characteristic.

sputtering the [! ([!)]3]ZTO thin films have high resistivities  $> 10^4 \Omega\text{m}$ . This validates the assumption of only the effective channel thickness contributing to the conduction.

Even though the FETs produced with this technique exhibit low off-currents below  $10^{-10}$  A, a small on-to-off ratio was achieved due to low forward currents of only  $4 \times 10^{-7}$  A, as can be seen in Figure 5.2 (b). An additional drawback is the variation of the flow rate by hand, which invariably leads to a non-optimal reproducibility. Therefore, an automation of this process was sought.

A further advancement of this deposition process was the use of an automatic program that continuously reduced the oxygen flow rate and allowed the programming of sputter times and flow rates. The automatic program by *Mantis Deposition Systems* is capable of driving one ramp at a time only, and therefore the sputtering conditions were adapted in such a way that the argon flow was kept constant at 30 sccm during the whole process. The oxygen flow rate could be varied continuously in this way. A schematic drawing of this process is shown in Figure 5.3. The start parameters are chosen as a gas mixture of 25/30 sccm oxygen/argon and the ramp is finished at 0/30 sccm oxygen/argon after a predefined time. Afterward, a conductive channel is sputtered for a defined time under pure argon flow atmosphere [E5].

As expected from the higher flow rate at the beginning of the process, the pressure decreases during the oxygen ramp, even though the pump valve is kept at constant position. This means that for an open pump valve a pressure of  $2.5 \times 10^{-3}$  mbar was measured at the beginning of



**Figure 5.3:** Schematic diagram of the process steps during the deposition of the [! (!)3]ZTO channel. The oxygen content is continuously reduced to a zero oxygen flow and subsequently, the conductive channel is sputtered in an argon flow atmosphere.

the ramp and a pressure of  $1.2 \times 10^{-3}$  mbar was reached at the end of the ramp.

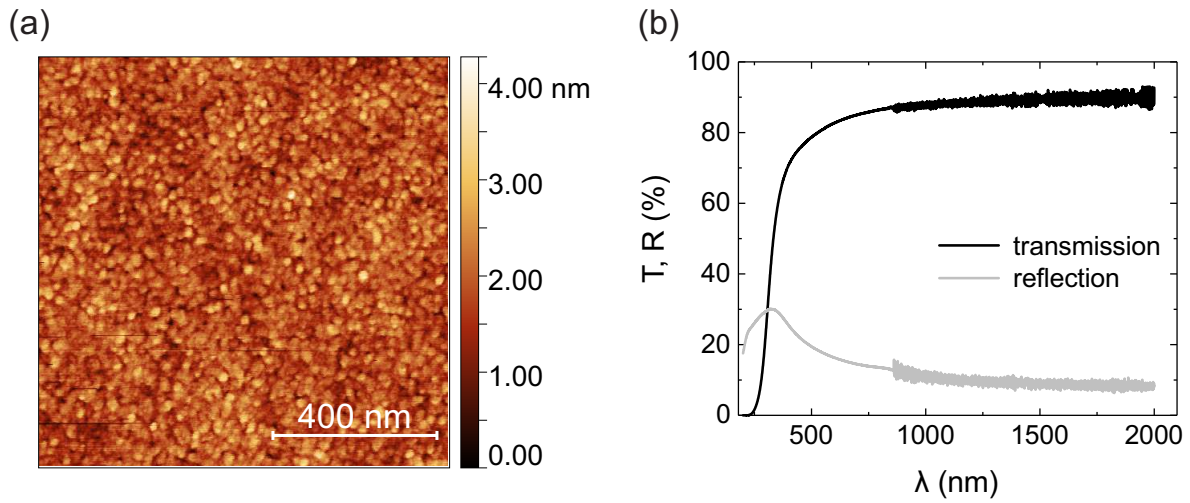
The results achieved with the automatized method were very similar to the results shown in Figure 5.2 (a) for the step wise process. The FETs are characterized by low off-currents but also low on-currents. Therefore, after establishing the new sputtering recipe, the goal was to optimize the [! (!)3]ZTO thin films with regards to the electron mobility and conductivity.

### 5.1.1 Characterization and Electrical Optimization of the Zinc Tin Oxide Thin Films

In a first step, a general characterization of the [! (!)3]ZTO thin films was performed. Their structural, optical and electrical properties were determined and are shortly presented. Moreover, an optimization of the conductivity and the electron mobility of the [! (!)3]ZTO thin films was conducted. The results in this section were obtained in cooperation with Lorenz Köhnlein in the scope of his *besondere Lernleistung* and Oliver Lahr<sup>4</sup> in the scope of his Master thesis. Until otherwise denoted, thin films for structural and electrical characterizations were deposited under argon atmosphere without oxygen flow variation layer.

For thin films deposited by long-throw magnetron sputtering, a small surface roughness of the thin films is expected, due to the large distance between sputtering target and substrate. Droplets are typically scattered on their way to the substrate. In Figure 5.4 (a) an [! (!)3]AFM scan of a  $1 \times 1 \mu\text{m}^2$  large section of a [! (!)3]ZTO thin film is shown. A small root mean square roughness of below 0.4 nm was measured and no droplets are observable.

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**Figure 5.4:** Topographic image (a) recorded by [! (!)3]AFM by Max Kneiß and transmittance and reflectance (b) of the substrate/thin film stack in a wavelength  $\lambda$  range from 200 nm to 2000 nm.

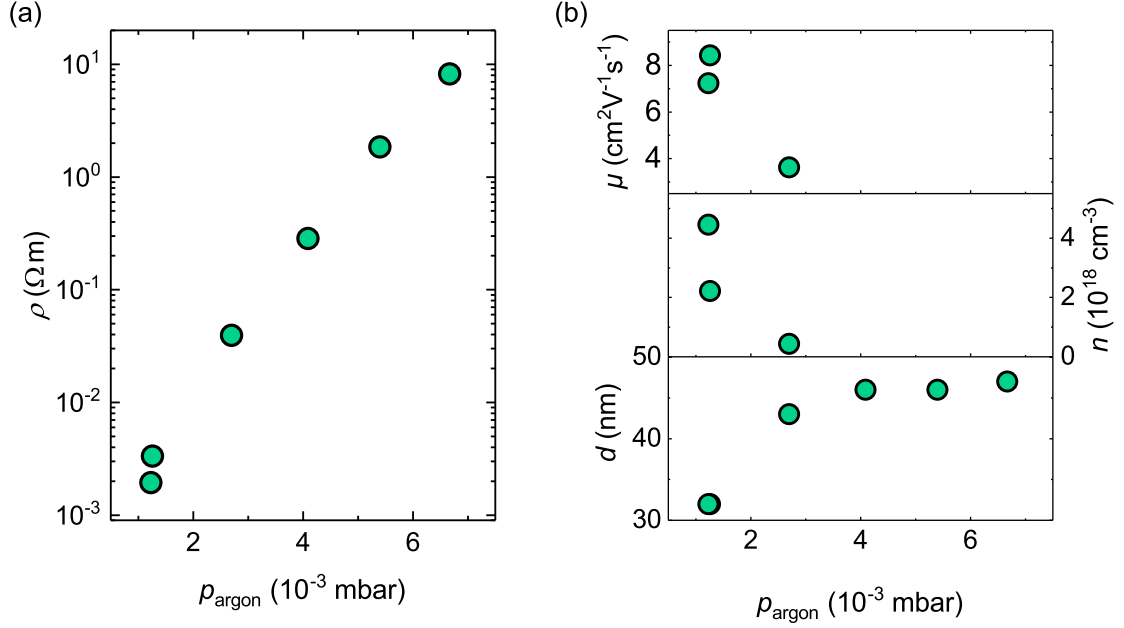
As can be seen in the scale on the right hand side, the peak to valley distance is below 4.3 nm. The absence of droplets on the thin films was confirmed by laser scanning microscopy measurements.

Additionally, the transmittance of the stack of glass substrate and a 30 nm thick thin film was recorded and is shown in Figure 5.4 (b). In the visible spectral range, the transmittance is above 80%. This enables the fabrication of transparent devices on basis of amorphous [! (!)3]ZTO.

From the absence of peaks in the [! (!)3]XRD pattern<sup>5</sup>, it was concluded that the samples are X-ray amorphous.

To gauge and modify the electrical properties of the [! (!)3]ZTO thin films, a series with samples deposited at different pressures was fabricated. The sputtering power and time were kept constant at 70 W and 1440 s. The sputtering atmosphere was chosen as a 30 sccm argon flow atmosphere and the pressure was regulated by the opening angle of the valve leading to the vacuum pump. This way, pressures between  $1.2 \times 10^{-3}$  mbar and  $6.7 \times 10^{-3}$  mbar were achievable. The obtained resistivity, free carrier density and electron mobility are shown in Figure 5.5 (a,b). By increasing the pressure, the resistivity of the thin films strongly increases by almost four orders of magnitude. Simultaneously, the free carrier density  $n$  and electron mobility  $\mu$  determined by Hall effect measurements, decrease. A maximum electron mobility of  $8.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  is obtained for the lowest pressure of  $1.2 \times 10^{-3}$  mbar. The resistivity varied from  $1.9 \times 10^{-3} \Omega \text{ m}$  for the lowest deposition pressure to  $18.2 \Omega \text{ m}$  for the highest deposition pressure. The free carrier density and electron mobility could be determined for pressures below  $p_{\text{argon}} \leq 2.7 \times 10^{-3}$  mbar only, as above this pressure the Hall constant exhibits an inconclusive sign, since the resolution limit of the measurement device was reached.

<sup>5</sup>XRD patterns are not shown here.



**Figure 5.5:** Dependence of the resistivity (a), electron Hall mobility, free carrier density and thin film thickness (b) on the deposition pressure.

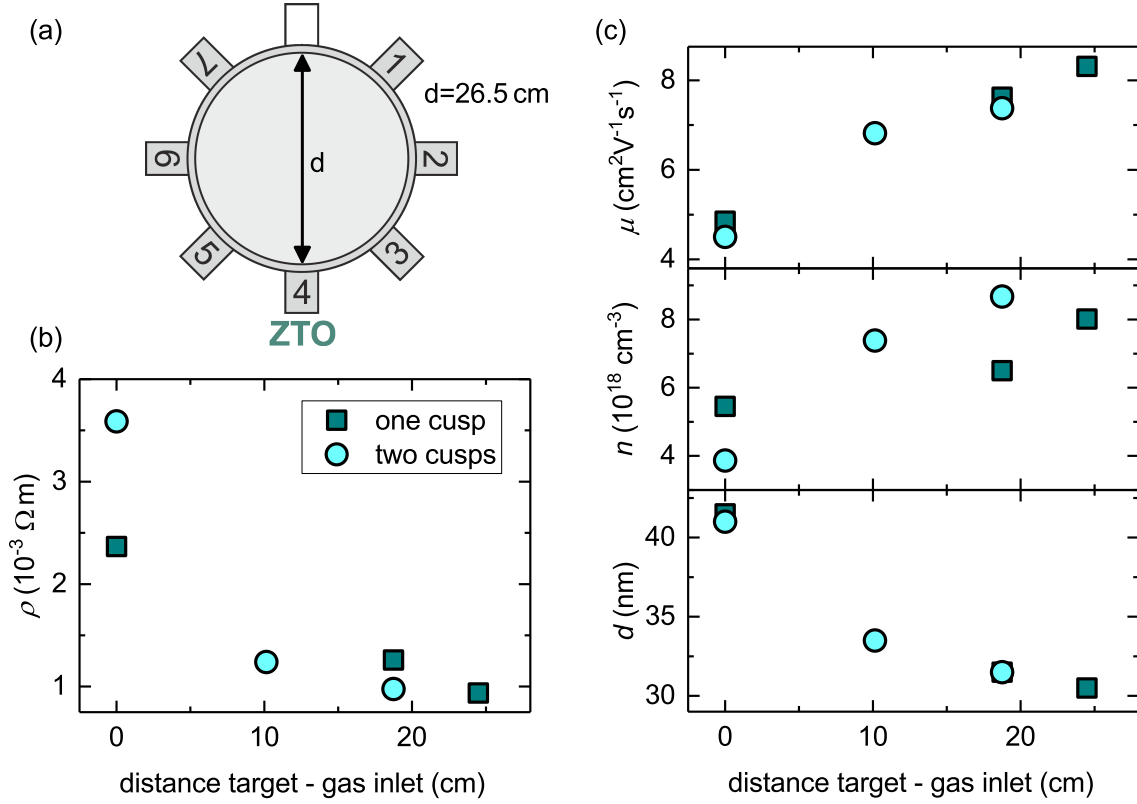
Lower chamber pressures can not be reached using this chamber without a decrease of the flow rate, which would lead to very small growth rates. A further increase of the sputter pressure would be possible by an increase of the flow rate, however, as the resistivity strongly increases with increasing chamber pressure.

The thin film thickness increases with increasing chamber pressure, as is expected from the higher ionization rate and therefore a higher amount of material ablated from the target. If the pressure were to be further increased, a decrease in the growth rate would be expected, as the ablated particles are increasingly scattered on the background gas. However, due to the high resistivity of the thin films, this pressure region is not of interest for this work. The [! (!)3]ZTO thin film thickness increases from 32 nm for a  $p_{\text{argon}} = 1.2 \times 10^{-3}$  mbar to 47 nm for  $p_{\text{argon}} = 6.7 \times 10^{-3}$  mbar. This means that for the thin film with the lowest resistivity and highest electron mobility a growth rate of  $1.3\text{ nm min}^{-1}$  is achieved.

For the deposition of these thin films, the gas inlet was chosen to be at the cusp<sup>6</sup> nearly opposite of the target to achieve a large distance between the target, where the plasma is ignited and the gas inlet in the chamber. A discussion of why this gas inlet is chosen is given below.

In a second step, the influence of the distance between sputter target and gas inlet was investigated. It was speculated that an increased distance between the gas inlet and the target, where the plasma is ignited, might lead to a more homogeneous gas distribution in the sputtering chamber. In contrast, if the gas inlet is chosen at the sputtering target, a locally higher pressure is expected, which might lead to an increase of the thin film roughness

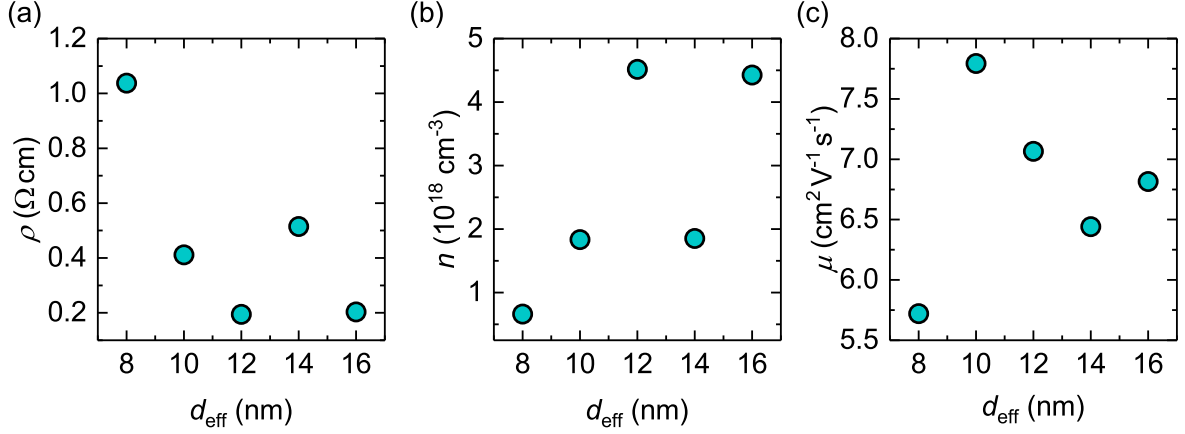
<sup>6</sup>'Cusp' denotes the target mount with gas inlet and water cooling in the following.



**Figure 5.6:** Schematic top view of the sputtering chamber with the position of cusps 1 to 7 (a). The resistivity (b) and Hall mobility, free carrier density and thin film thickness (c) in dependence of the distance between gas inlet and sputtering cusp. Data for the gas inlet at one cusp and two cusps is shown.

or a decrease of the electron mobility. The experiments were performed in cooperation with Lorenz Köhnlein.

A schematic drawing of the chamber with the target cusps, at which the gas inlets are originated, is depicted in Figure 5.6 (a). For the deposition, a flow rate of 30 sccm argon and a pressure of  $1.2 \times 10^{-3}$  mbar were chosen. The sputter time was fixed at 1440 s. To investigate the influence of the gas inlet on the electrical properties of the thin films, a series of thin films was deposited with different positions of the gas inlet relative to the sputtering target. Either one gas inlet or two were chosen. If more than one cusp was used, the cusp nearest to the sputtering target was used for the calculation of the distance. In Figure 5.6 (b), the resistivity in dependence on the distance of the gas inlet is shown. As the cusp opposite to the ZTO target cusp is not installed, a maximal distance of 24.5 cm was achieved between target and gas inlet. A clear increase of the resistivity is observed with decreasing distance. The highest electron mobility of  $8.3 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$  was achieved for the largest distance of 24.5 cm between sputtering target and gas inlet, as can be seen in Figure 5.6 (c). The lowest mobility is obtained if the gas inlet is at the sputtering target - independent of whether gas was additionally introduced at a further distanced cusp.



**Figure 5.7:** Resistivity (a), free carrier density (b) and electron mobility (c) in dependence on the effective thin film thickness for a [! (!)3]ZTO layer with underlying 11 nm thick oxygen variation layer.

A similar behavior, however less pronounced is observable for the free carrier density, which slightly increases with increasing distance between sputtering target and gas inlet. The thin film thickness decreases with increasing distance between the gas inlet and the sputtering cusp (compare Figure 5.6 (c)), which can be attributed to the increased local pressure at the target for a gas inlet at the sputtering target and therefore a higher ionization rate and thus a higher ablation rate at the target.

Structural investigation of the thin films by [! (!)3]AFM and [! (!)3]XRD yielded no significant influence of the distance between sputtering target and gas inlet on either the thin film roughness nor the amorphous structure.

These results were used for the deposition of the subsequent thin films. The gas inlet was chosen at the largest possible distance from the sputtering target and the lowest achievable pressure of  $1.2 \times 10^{-3}$  mbar was used for a flow rate of 30 sccm argon to achieve the highest electron mobility in the thin films.

In Figure 5.7 (a) the resistivity of thin films deposited with the new sputtering recipe in dependence of the effective layer thickness is depicted. The oxygen variation layer was deposited below the conductive channel with a ramp starting at 25/30 sccm oxygen/argon and was reduced to 0/30 sccm oxygen/argon in 720 s. This results in a thickness of the oxygen variation layer of 11 nm. This thickness is the standard thickness of the oxygen variation layer and was always used, unless otherwise denoted, in the following.

The resistivity decreases with increasing effective layer thickness, as expected. The thin films were not deposited in a systematic order to eliminate effects coming from the sputtering chamber. And in fact, it is visible that the resistivity does not show a systematic behavior for effective layer thicknesses between 12 nm and 16 nm. The increase of the resistivity for the sample with an effective thickness of 14 nm is likely due to the sputtering of a different oxide semiconductor before this process. The same behavior is visible in the free carrier density in Figure 5.7 (b). The mobility of the thin films is very similar for all effective thicknesses

(compare Figure 5.7 (c)).

These thin films will be used later on for a determination of the influence of the channel thickness on the performance of  $\text{In}_2\text{O}_3/\text{ZTO}$  based devices.

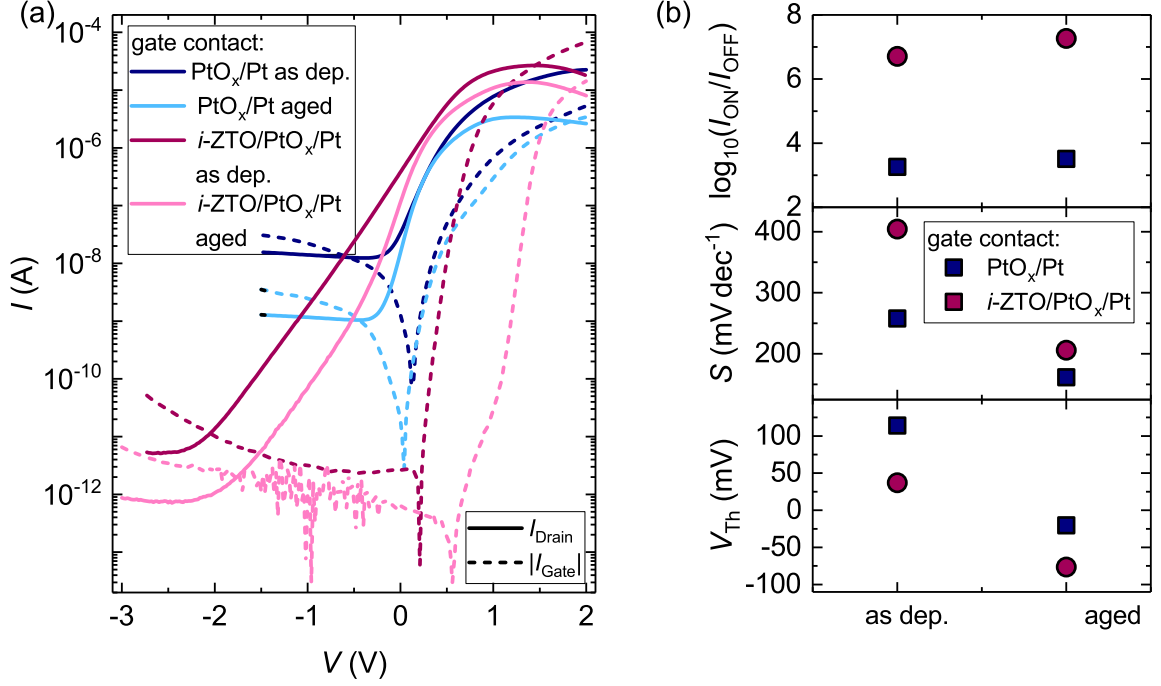
### 5.1.2 Optimization of the Gate Contact

The next aim was the optimization of the gate contact and the thin film thickness. In this chapter, a description of the gate contact optimization is given, which is crucial for the performance of the devices. As gate metal, platinum was chosen as a work by Schlupp *et al.* demonstrated that the most advantageous diode characteristics can be obtained for this metal [37]. As described in chapter 4, the reactively sputtered metal oxide has to be used to achieve a rectifying behavior.

A comparison of two different gate contact configurations was performed. Therefore, an identical channel with an effective thickness of 12 nm was used for the fabrication of  $\text{In}_2\text{O}_3/\text{ZTO}$  based MESFETs with different gate contacts. In Figure 5.8 (a), a comparison of the transfer characteristic of an as deposited and aged FET with two different gate contact types is depicted. One FET has a gate contact consisting of  $\text{PtO}_x/\text{Pt}$  deposited by  $\text{In}_2\text{O}_3$  dc-sputtering at a distance of 4 cm and the other a gate contact stack consisting of  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  deposited by long-throw sputtering. In explicit, two different deposition chambers were used for the contact fabrication. The advantage of the first is, that a reactive sputtering in a 100% oxygen atmosphere is possible and a high impact energy of the incoming target atoms can be achieved. This might lead to a surface cleaning during the contact deposition, but also induce a high number of defects at the interface. The second contact fabrication has the advantage of an additional intrinsic  $i\text{-ZTO}$  layer between the conductive channel and the gate contact. As was shown by Schlupp *et al.*, this layer significantly reduces the leakage current in the reverse regime of the diode [7,37]. For the here presented devices, the  $i\text{-ZTO}$  layer, which has a thickness of  $\approx 10$  nm, leads to a larger reverse voltage regime, in which the gate leakage current does not dominate the drain current of the FET. Additionally, the long distance between target and substrate leads to a reduced impact energy of the target atoms and may therefore lead to less induced defects at the interface of semiconductor and metal oxide.

Additionally, gate contact configuration with a  $\text{PtO}_x/\text{Pt}$  contact deposited by long-throw sputtering as well as an  $i\text{-ZTO}$  layer in combination with  $\text{PtO}_x/\text{Pt}$  deposited at a short distance of 4 cm were investigated. However, the performance of FETs with these gate contact configurations was low compared to the above described contact configurations. They were therefore not further investigated and only  $\text{PtO}_x/\text{Pt}$  (deposited at a distance of 4 cm) and  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  (deposited by long-throw sputtering) gate contacts are discussed here.

In Figure 5.8 (a), the transfer and gate characteristic are depicted for the two contact configurations. For both gate contact types, the forward current is dominated by the gate current. It is very similar for the  $\text{PtO}_x/\text{Pt}$  and  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  gate contact. In the off regime of the transistor, the characteristic is dominated by the leakage current over the gate, which signif-



**Figure 5.8:** Transfer characteristic and gate leakage current (a) of a  $i\text{-ZTO}$  based FET with  $\text{PtO}_x/\text{Pt}$  and  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  gate contact. Drain current on-to-off ratio, sub-threshold swing and threshold voltage for the as deposited and aged state of the two gate contact types. The effective channel thickness is 12 nm and  $W/L = 100 \mu\text{m}/10 \mu\text{m}$ . A drain voltage of 2 V was applied during the measurement of the transfer characteristics.

icantly differs for the two gate contact configurations. The transistor with  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  gate contact exhibits a three orders of magnitude lower off-current than the transistor with  $\text{PtO}_x/\text{Pt}$  gate contact. This leads to a higher drain current on-to-off ratio for the FET with  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  gate contact. However, the voltage span  $\Delta V_{\text{ON}}$  required to switch the FET from off to on is also larger for this gate configuration. For the  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  gate contact it is  $\approx 3.6$  V, whereas for the  $\text{PtO}_x/\text{Pt}$  gate contact it is  $\approx 2$  V.

The transfer characteristics were measured again after an aging time of  $\approx 270$  days. This re-measurement was performed since an improvement of Schottky barrier diodes was observed in the previous chapter 4.3. For the FETs shown here, a decrease of the off-current is observed, which can be attributed to the reduced reverse current of the gate diode and therefore the reduced leakage current. Moreover,  $\Delta V_{\text{ON}}$  reduces to  $\approx 1.5$  V for the  $\text{PtO}_x/\text{Pt}$  gate contact and remains unaltered for the  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  gate contact.

A direct comparison of the characteristic parameters of the FETs with the two different gate contact types is depicted in Figure 5.8 (b) for the as deposited and aged state. The main advantage of the  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  gate contact is the higher drain current on-to-off ratio of the device compared to a FET with  $\text{PtO}_x/\text{Pt}$  gate contact. The drain current on-to-off ratios are  $5.1 \times 10^6$  (aged:  $1.8 \times 10^7$ ) and  $1.8 \times 10^3$  (aged:  $3.5 \times 10^3$ ) for the  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  and  $\text{PtO}_x/\text{Pt}$  gate contact, respectively. However, especially in the as deposited state the sub-

threshold swing of the *i*-ZTO/PtO<sub>x</sub>/Pt gate contact is significantly higher than that of the PtO<sub>x</sub>/Pt gate contact. The difference in the sub-threshold swing for the two gate contact types decreases with aging, however even in the aged state, the FET with *i*-ZTO/PtO<sub>x</sub>/Pt gate contact exhibits a higher sub-threshold swing than the minimum value of 161 mV dec<sup>-1</sup> that was obtained for the FET with PtO<sub>x</sub>/Pt gate contact. Moreover, the absolute change in the sub-threshold swing upon aging is smaller for the PtO<sub>x</sub>/Pt gate contact.

The threshold voltage of both gate contact types shifts to negative values upon aging. As the threshold voltage can be easily influenced by the channel thickness, a comparison of the absolute values, which are very similar, is not performed here.

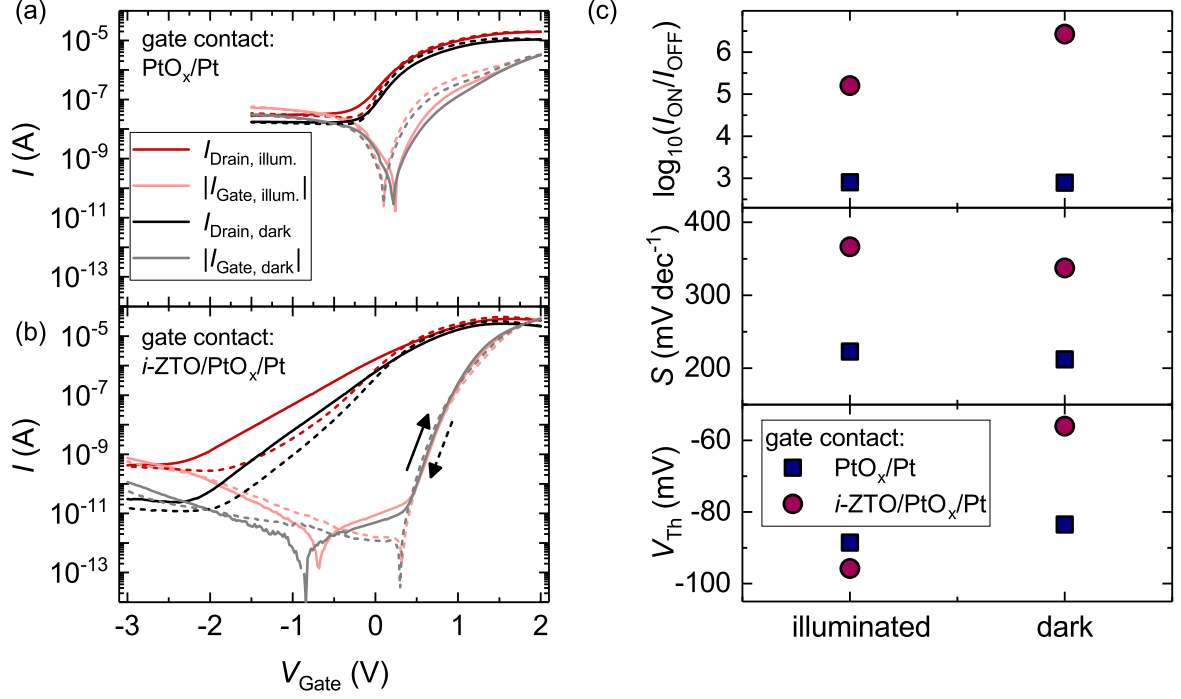
The diffusion of oxygen from the metal oxide contact into the semiconductor was discussed for PtO<sub>x</sub>/Pt contacts in chapter 4.5. It is most likely responsible for the improvement with aging of the transistor properties observed here. For the *i*-ZTO/PtO<sub>x</sub>/Pt contacts, the origin of the aging is not entirely clear. Three mechanisms are possible: (i) a diffusion of oxygen from the *i*-ZTO into the conductive [! (!)]ZTO channel, (ii) a diffusion of oxygen from the PtO<sub>x</sub> into the *i*-ZTO layer or (iii) a combination of both diffusion processes. An analysis by depth resolved [! (!)]XPS measurements could be used to determine the mechanism leading to the improvement. These measurements were not conducted within the framework of this thesis and are of interest for future investigations on [! (!)]ZTO based devices.

For the use of FETs in future integrated circuits for commercial use, the behavior of the transistors under illumination is of importance. In the ideal case, the devices should perform similar under illumination and in darkness, especially the device parameters like threshold voltage should remain the same.

To test the behavior of FETs with PtO<sub>x</sub>/Pt and *i*-ZTO/ PtO<sub>x</sub>/Pt gate contact, the transfer characteristics were measured under an illumination of 150 W of a halogen lamp. Afterward, the lamp was turned off and the samples were stored for 2 h in the dark before a subsequent measurement was performed. For both measurements a drain voltage of 2 V was applied.

In Figure 5.9 (a,b), the transfer characteristics for both gate types are depicted a measurement under illumination and in the dark. It is immediately visible that the transfer characteristics of the sample with PtO<sub>x</sub>/Pt gate contact do not change significantly between the measurement conditions under illumination and in the dark. The off current is measured as  $3.3 \times 10^{-8}$  A and  $1.7 \times 10^{-8}$  A for a measurement under illumination and in the dark, respectively. In contrast, the transfer characteristics of the sample with *i*-ZTO/ PtO<sub>x</sub>/Pt gate contact exhibit an increased off-current for the measurement under illumination. In this case it is  $5.2 \times 10^{-10}$  A, whereas it is as low as  $2.7 \times 10^{-11}$  A for the measurement in the dark. The increase of the off-current can be explained by the increase of the gate leakage current for the measurement under illumination.

To eliminate the smaller change in the off-current due to the generally higher current flowing for the PtO<sub>x</sub>/Pt gate contact, the measurement was repeated with a FET that has an off current of  $2.3 \times 10^{-10}$  A for a measurement in the dark. A measurement under illumination



**Figure 5.9:** Transfer characteristics recorded under illumination and in the dark for a [! ([!])3]ZTO based FET with (a) PtO<sub>x</sub>/Pt and (b)  $i$ -ZTO/PtO<sub>x</sub>/Pt gate contact. Characteristic parameters (c) of the two FETs obtained under illumination and in the dark. The effective channel thickness is 12 nm and  $W/L = 100\mu\text{m}/10\mu\text{m}$ . A drain voltage of 2 V was applied during the measurement of the transfer characteristics.

increased the off-current to a value of  $1.6 \times 10^{-9}$  A. It can therefore be concluded that the smaller change of the off current for the PtO<sub>x</sub>/Pt contact is due to the higher currents flowing for this gate contact type.

The origin of the light sensitivity of the [! ([!])3]ZTO based FETs was not further investigated here. A possible mechanism leading to the decrease of the off-current for a measurement condition in the dark might be the occupation of traps. This would also explain the reduced effect of the illumination on a FET with higher off current, as the contribution of the traps to the total current is negligible in this case.

In Figure 5.9 (c) the drain current on-to-off ratio, sub-threshold swing and threshold voltage for the two gate types is compared for the measurement conducted under illumination and in the dark. The [! ([!])3]ZTO based FET with PtO<sub>x</sub>/Pt gate contact does not exhibit a change in its characteristic parameters for the two measurement types. In contrast, the drain current on-to-off ratio of the FET with  $i$ -ZTO/PtO<sub>x</sub>/Pt gate contact decreases by one order of magnitude when measured under illumination. The change in the sub-threshold swing is very small and the threshold voltage shifts to more positive values for the measurement in the dark.

To eliminate charging effects of defects or interface trap states, the characteristics were also recorded with the starting point of the scan at positive rather than negative values. The

results are not shown here, as no difference was observable for the two different starting points of the voltage sweep scan.

A third measurement after a storage of 3 h and 15 h in the dark did not exhibit any change compared to the measurement after 2 h in the dark. Moreover, all FETs on both samples were recorded before the experiment on the influence of the illumination on the transfer characteristic. The characteristics recorded before the measurement under illumination are also equal to the measurement performed after a storage of the sample for 2 h in the dark.

In summary, it was shown that both gate contact types have their advantages and disadvantages. The gate contacts using an intrinsic  $i$ -ZTO layer exhibit much higher rectifications than the FETs without the  $i$ -ZTO layer. However, the sub-threshold swing and voltage required to switch the FET is lower for FETs with  $\text{PtO}_x/\text{Pt}$  gate contact.

The following chapter is split into descriptions on MESFETs with  $\text{PtO}_x/\text{Pt}$  gate contact and  $i$ -ZTO/ $\text{PtO}_x/\text{Pt}$  gate contact.

## 5.2 Devices with $\text{PtO}_x/\text{Pt}$ Gate Contact

The first part will concentrate on the description of  $i$ -ZTO based MESFET devices with a  $\text{PtO}_x/\text{Pt}$  gate contact. The influence of the effective channel thickness on the performance of MESFETs and simple inverters is discussed as well as the long term stability of both device types. Additionally, gate lag measurements to gauge the switching speed of the devices are presented.

### 5.2.1 Variation of the Channel Thickness

In the first part of this chapter, the deposition conditions were optimized with regard to the conductivity and electron mobility. The next goal was the determination of the optimum deposition time, and therefore channel thickness, to achieve transistors with high drain current rectification  $I_{\text{ON}}/I_{\text{OFF}}$ , low sub-threshold swings  $S$  and a threshold voltage  $V_{\text{Th}}$  close to zero. In the ideal case, a variation of the channel thickness does not influence the free carrier density of the thin films. However, as shown in Figure 5.7 (b), this is not true for the devices presented here. A variation of the effective channel thickness always leads to a change in the free carrier density. Therefore, the discussions here are an optimization of the combined system channel thickness and free carrier density. To clearly represent the results, the effective channel thickness is used to reference the individual samples.

The thin film thickness and electrical properties of the thin films were determined on planar thin films, which were deposited in the same sputtering process as the mesa for FETs. The thin films are the same as presented in Figure 5.7.

### ZTO/PtO<sub>x</sub>/Pt Gate Contact Transistors

In Figure 5.10 (a) exemplary transfer characteristics for effective channel thicknesses between 8 nm and 16 nm are depicted. The width to length ratio is  $W/L = 100 \mu\text{m}/10 \mu\text{m}$  and the transfer characteristics were measured with a drain voltage of 2 V. As described in chapter 5.1.2, the gate contact consists of platinum oxide sputtered under pure oxygen atmosphere for 80 s, which is capped by a metallic platinum layer.

An increase of the on-current with increasing effective channel thickness is observable. Simultaneously, the off-current of the FETs also increases. The on-current (off-current) increases from a value of about  $I_{\text{ON}} = 5.1 \times 10^{-8} \text{ A}$  ( $I_{\text{OFF}} = 9.7 \times 10^{-13} \text{ A}$ ) for  $d_{\text{eff}} = 8 \text{ nm}$  to a value of  $I_{\text{ON}} = 3.9 \times 10^{-5} \text{ A}$  ( $I_{\text{OFF}} = 3.8 \times 10^{-6} \text{ A}$ ) for  $d_{\text{eff}} = 16 \text{ nm}$ . For effective thicknesses of 8 nm and 10 nm the gate current is as high or higher than the drain current in the measured voltage range. This is most likely due to the high resistance of the thin film combined with a non-ideal rectifying behavior of the gate contact.

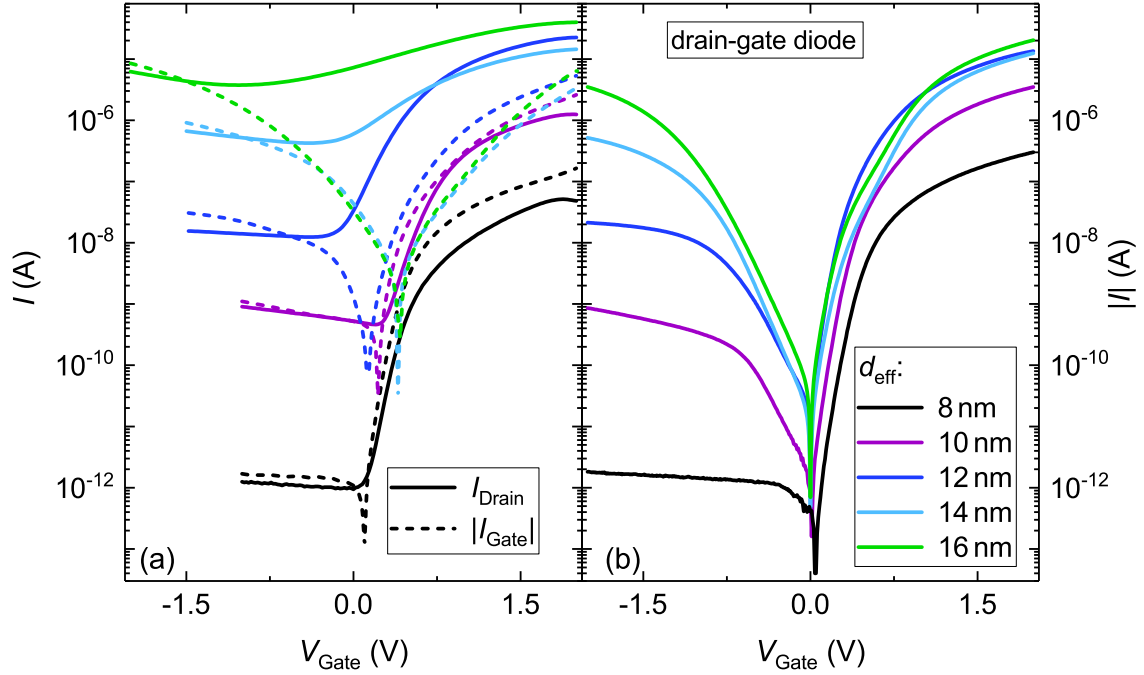
To gauge the quality of the gate contact, drain-gate diode characteristics were measured. The diode characteristics (see Figure 5.10 (b)) exhibits a similar increase of the forward and reverse current with increasing thin film thickness. For effective channel thicknesses  $d_{\text{eff}} \geq 10 \text{ nm}$ , an exponential increase of the reverse current is observed, which indicates that this current is a tunneling current. The diode characteristics were fitted with equation 2.18, using a *MATLAB* program written by Daniel Splith<sup>7</sup> and are listed, as well as the characteristic FET parameters, in Table 5.1. The effective barrier height and ideality factor were determined as 0.78 – 0.92 eV and 1.7 for all effective channel thicknesses, respectively, without a systematic change discernible. In contrast, the series resistance increases with decreasing effective channel thickness, as is also visible in the stronger influence of the series resistance in the forward regime of diodes with smaller effective channel thickness in Figure 5.10 (b).

The off-current of the transistors exhibits a stronger increase than the on-current with increasing effective channel thickness. This leads to a strong decrease of the drain current on-to-off ratio. In Table 5.1, the characteristic parameters of the depicted transfer characteristics of the drain-gate diode characteristics are listed.

A drop of  $I_{\text{ON}}/I_{\text{OFF}}$  from  $5.5 \times 10^4$  to 10 for an increase of the effective thickness from 8 nm to 16 nm is observed. This is mainly due to a strong increase of the gate leakage current in reverse direction. The maximal transconductance of the transistors increases due to the higher conductivity of the thin films and the sub-threshold swing also increases. The smallest value of the sub-threshold swing of  $109 \text{ mV dec}^{-1}$  is obtained for the smallest effective thickness of 8 nm. Values as small as these are desirable for FETs, as they indicate that only a small voltage regime is required for switching the devices. In this case 1.5 V are required to switch the device from on to off for the smallest effective channel thickness.

The threshold voltage of the devices shifts from positive values for  $d_{\text{eff}} \leq 12 \text{ nm}$  to negative values for  $d_{\text{eff}} > 12 \text{ nm}$ . Transistors with threshold voltages above 0 V are called normally-

<sup>7</sup>Universität Leipzig



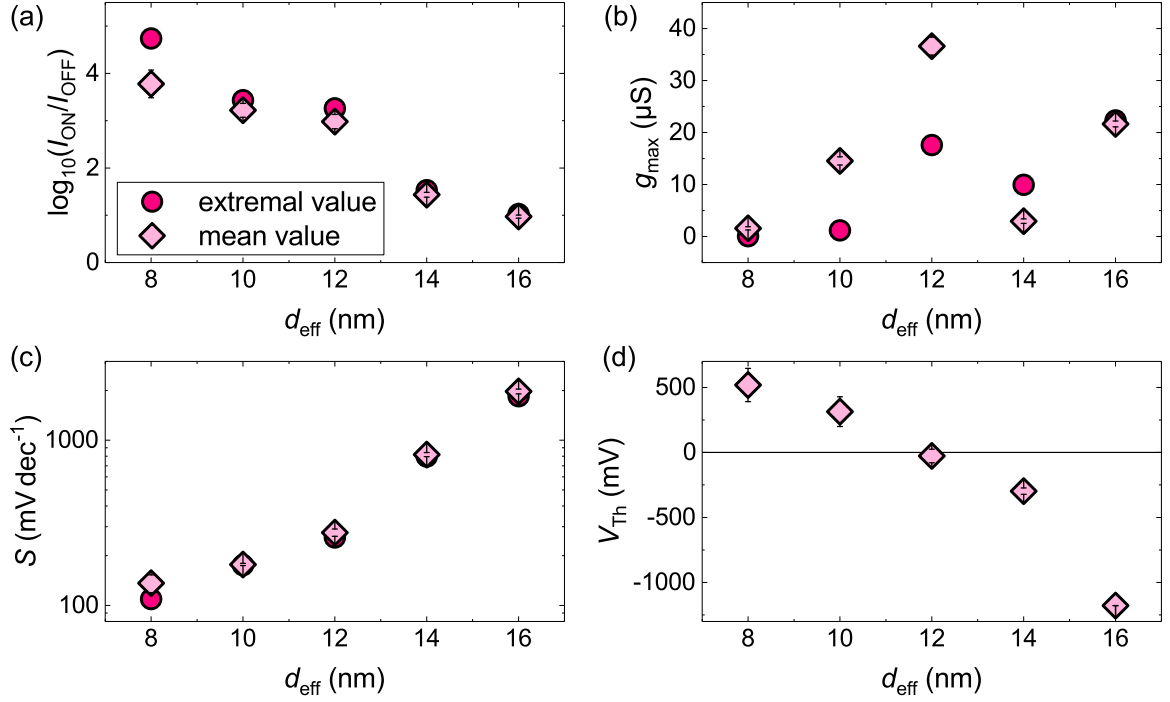
**Figure 5.10:** Exemplary transfer characteristics and gate leakage currents (a) and the corresponding drain-gate diode characteristics (b) for effective thin film thicknesses between 8 nm and 16 nm.

**Table 5.1:** Characteristic parameters of the MESFETs and diodes depicted in Figure 5.10 for effective channel thicknesses between 8 nm and 16 nm.

$d_{\text{eff}}$ nm	$I_{\text{ON}}/I_{\text{OFF}}$	$g_{\text{max}}$ $\mu\text{S}$	$S$ $\text{mV dec}^{-1}$	$V_{\text{Th}}$ mV	$R_s$ $\Omega$	$\phi_{\text{B,eff}}$ eV	$\eta$
8	$5.5 \times 10^4$	0.07	109	403	$5.1 \times 10^6$	0.92	1.7
10	$2.7 \times 10^3$	1.20	175	461	$4.5 \times 10^5$	0.86	1.7
12	$1.8 \times 10^3$	17.59	258	114	$1.2 \times 10^5$	0.79	1.6
14	34	9.94	798	-279	$1.3 \times 10^5$	0.81	1.8
16	10	22.34	1848	-1103	$8.1 \times 10^4$	0.78	1.8

off transistors, whereas transistors with threshold voltages below 0 V are called normally-on transistors.

For each effective channel thickness, 15 devices were measured. All FETs have a width to length ratio of  $W/L = 100 \mu\text{m}/10 \mu\text{m}$ . The mean and extremal values of the characteristic parameters of the transistors are shown in Figure 5.11 (a-d). The arithmetic mean values are depicted with the corresponding standard deviation. For the drain current on-to-off ratio, the arithmetic mean of the logarithmic drain current onto-off ratio is depicted. A very small deviation is visible for all effective channel thicknesses and parameters. The devices on each sample are therefore very similar. In Figure 5.11 (a), the above mentioned decrease of the drain current on-to-off ratio with increasing effective channel thickness is very well visible.



**Figure 5.11:** Mean (and extremal) values of the (a) logarithmic drain current on-to-off ratio (maximum), (b) maximal transconductance (maximum), (c) sub-threshold swing (minimum) and (d) mean threshold voltage in dependence on the effective channel thickness.

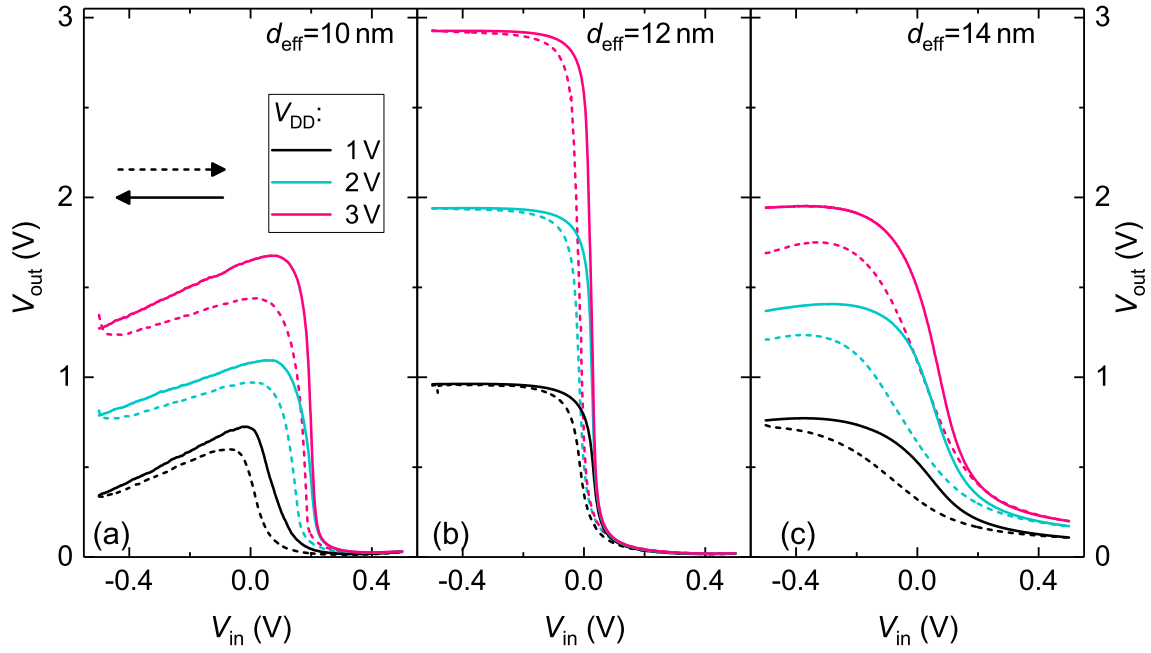
The maximum transconductance does not exhibit a systematic increase or decrease. It appears to mirror the behavior of the free carrier density as it is depicted in Figure 5.7 (b). The mean and minimum values of the sub-threshold swing are very similar. A strong increase from values close to  $100 \text{ mV dec}^{-1}$  for  $d_{\text{eff}} = 8 \text{ nm}$  to values above  $1000 \text{ mV dec}^{-1}$  for  $d_{\text{eff}} = 16 \text{ nm}$  is evident.

In Figure 5.11 (d), the threshold voltage is depicted in dependence on the effective channel thickness. A decrease of the threshold voltage from  $500 \text{ mV}$  to  $-1100 \text{ mV}$  is observed for an increase of the effective channel thickness from  $8 \text{ nm}$  to  $16 \text{ nm}$ . The black line in the graph is a guide to the eye and denotes a threshold voltage of  $0 \text{ V}$ . For integrated circuits, such as simple inverters with two identical FETs, this is the optimum threshold voltage. The MESFETs with an effective channel thickness of  $12 \text{ nm}$  exhibits a threshold voltage closest to zero.

Even though the free carrier density does not increase systematically with increasing effective channel thickness, the drain current on-to-off ratio, the sub-threshold swing and the threshold voltage exhibit a systematic decrease or increase with changing effective channel thickness.

### Simple Inverter

The devices presented above are integrated to simple inverters as described in chapter 2.4. Both FETs in this layout are identical and have dimensions of  $W/L = 100 \mu\text{m}/10 \mu\text{m}$ . The main requirement for this inverter layout is that  $V_{\text{Th}} \lesssim 0 \text{ V}$ , as discussed in chapter 2.4. Therefore, the best inverter characteristics are expected for  $d_{\text{eff}} = 12 \text{ nm}$ .

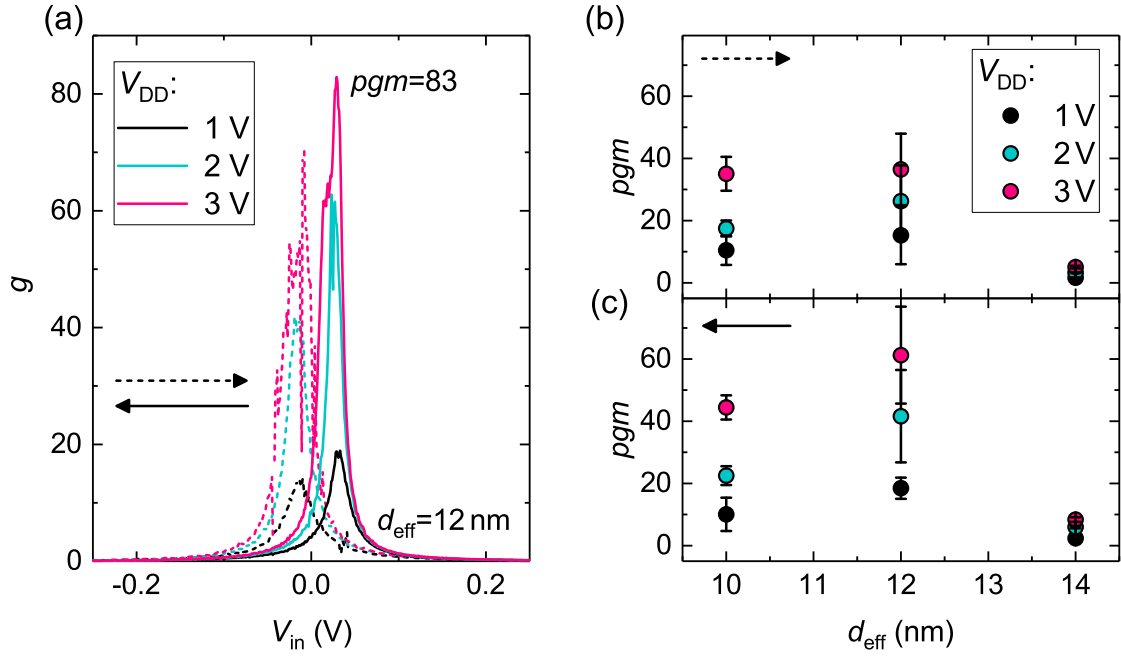


**Figure 5.12:** Voltage transfer characteristics of simple inverters based on MESFETs with effective channel thicknesses of (a) 10 nm, (b) 12 nm and (c) 14 nm for three different operating voltages between 1 V and 3 V.

In Figure 5.12 (a-c), the voltage transfer characteristics of inverters for an effective channel thickness of 10 nm, 12 nm and 14 nm are shown for three different operating voltages between 1 V and 3 V. As expected from the threshold voltage close to zero volt for the sample with an effective layer thickness of 12 nm, this inverter exhibits the largest logic swing of 2.87 V for an operating voltage of 3 V. In contrast, the logic swing for the samples with an effective channel thickness of 10 nm and 14 nm decreases to values of 1.44 V and 1.75 V, respectively. This reduced logic swing can be mainly attributed to a decrease of the output high voltage. The decrease of the output high voltage of the inverter is caused by a drop of the voltage over the switch transistor instead of a voltage drop over the load transistor for negative input voltages. This can be caused by a low transconductance of the FETs (compare Figure 5.11 (b)).

For all three effective channel thicknesses a hysteresis between voltage scan directions from negative to positive and positive to negative input voltage values is observed. This hysteresis is least distinct for  $d_{\text{eff}} = 12$  nm. A longer integration time leads to a reduced hysteresis, which implies that a charging and discharging of trap states leads to the hysteresis for the two voltage sweep directions.

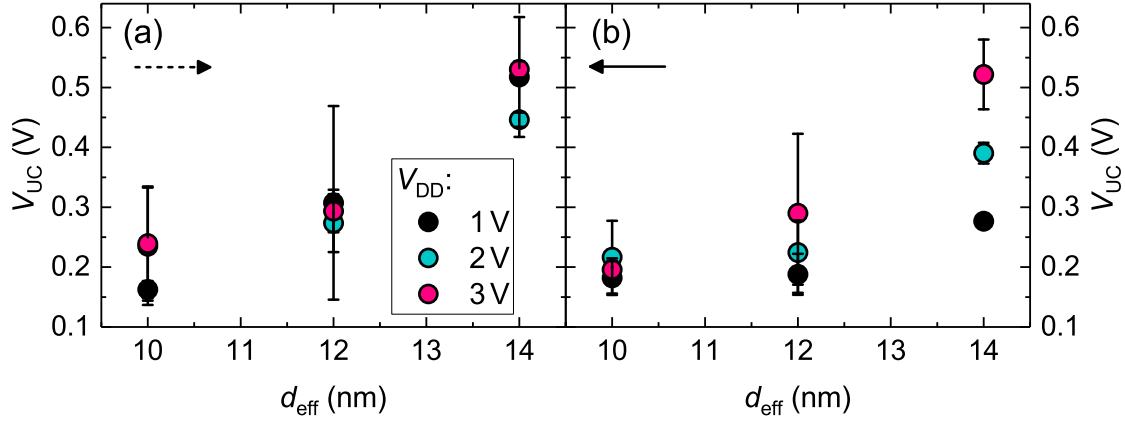
The voltage transfer characteristics were used to determine the characteristic parameters of the inverters, such as the gain and peak gain magnitude  $pgm$  and the uncertainty level. On each sample, so for each effective layer thickness, 12 inverters were measured. In Figure 5.13 (a) the gain, which is the negative derivative of output voltage with respect to input voltage,



**Figure 5.13:** (a) Gain of an inverter with an effective channel thickness of 12 nm for a scan direction from negative to positive and positive to negative voltages. Mean peak gain magnitude for inverters with effective channel thicknesses between 10 nm and 14 nm and different operating voltages for a scan direction (b) from negative to positive voltages and (c) positive to negative voltages. The error bars denote the standard deviations.

is depicted for both voltage scan directions for  $d_{eff} = 12$  nm. A  $pgm$  of 83 is achieved for an operating voltage of 3 V. However, as can be seen in Figure 5.13 (b,c), the  $pgm$  strongly differs for the two voltage scan directions and the operating voltages. Here, the arithmetic mean with the standard deviation is depicted. Typically, higher operating voltages lead to higher  $pgm$  values. For effective channel thicknesses of 10 nm and 14 nm, the  $pgm$  is very small even for an operating voltage of 3 V. Values around  $pgm = 40$  are obtained for  $d_{eff} = 10$  nm and  $V_{DD} = 3$  V. For an effective channel thickness of 12 nm, the devices exhibit very large deviations from the arithmetic mean value. The increase of the  $pgm$  with increasing operating voltage is observable for both voltage scan directions. However, for the voltage scan direction from positive to negative voltages, a higher  $pgm$  is achieved. This change in the  $pgm$  for the two voltage scan direction can be directly related to a hysteresis of the transfer characteristics. For the two voltage sweep direction, slightly different threshold voltages and saturation of the drain current  $\gamma$  of the corresponding FETs are measured. A more detailed analysis of the influence of the saturation of the drain current  $\gamma$  on the peak gain magnitude will be given below (see chapter 5.2.2).

A second important parameter that was extracted from the voltage transfer characteristics is the uncertainty level. It is depicted for the three different effective channel thicknesses and operating voltages in Figure 5.14 (a,b). A clear dependence of the uncertainty level on



**Figure 5.14:** Mean uncertainty levels for effective channel thicknesses between 10 nm and 14 nm and three different operating voltages for a scan direction (a) from negative to positive voltages and (b) positive to negative voltages. The error bars denote the standard deviations.

the effective channel thickness is observable for both voltage scan directions. With increasing effective channel thickness it increases. For  $d_{\text{eff}} = 12$  nm mean uncertainty levels below 300 mV are obtained for both scan directions and all operating voltages. In contrast, for  $d_{\text{eff}} = 14$  nm, values as high as 500 mV are determined.

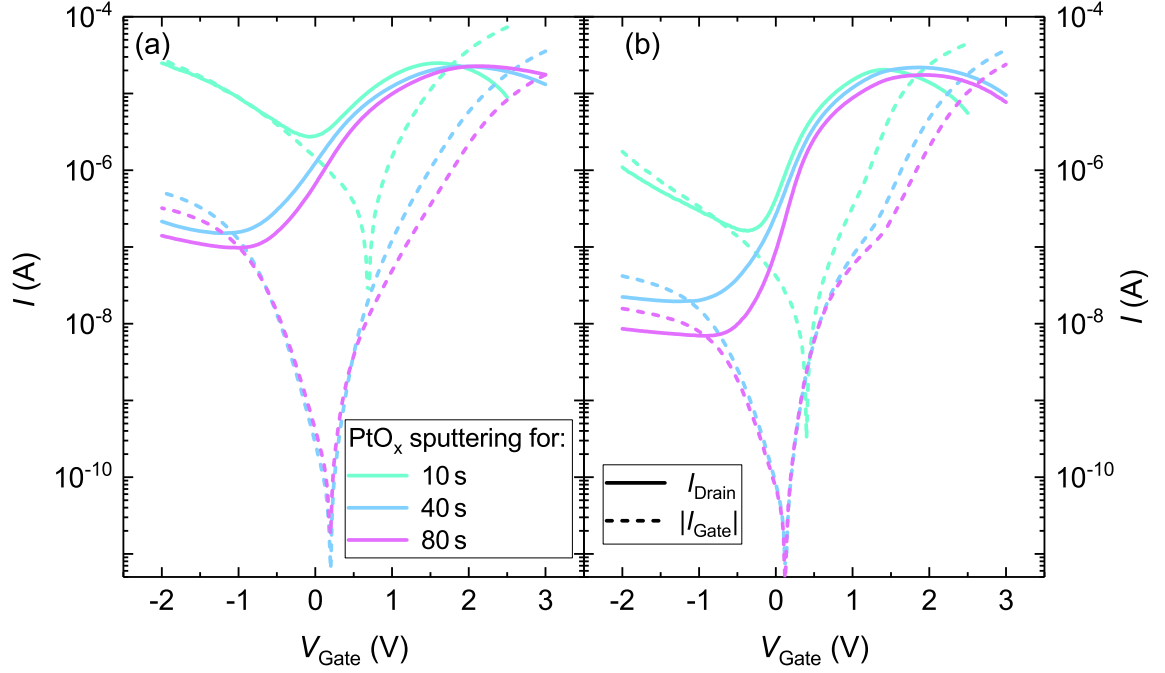
It is therefore possible to tune the drain current on-to-off ratio and the threshold voltage by a variation of the effective channel thickness. This way the optimum parameters, e.g. a threshold voltage close to zero volt, can be adjusted.

The highest peak gain magnitude and lowest uncertainty level were obtained for an effective channel thickness of 12 nm and 10 nm, respectively.

### 5.2.2 Influence of the Oxygen Reservoir on the Performance and Long Term Stability of Devices

In chapter 4.4, the important role of oxygen for the formation of rectifying contacts was discussed. The same processes that were discussed for pulsed laser deposited [! (!)3]ZTO, hold true for sputtered [! (!)3]ZTO thin films. The performance of Schottky barrier diodes can be greatly influenced by the amount of oxygen in the plasma during the sputtering of the Schottky barrier contact. The goal was to find the optimum time for the sputtering of the platinum gate contact under 100% oxygen atmosphere with regards to the performance of FETs and their long term stability.

Therefore, a series with different sputtering times of the  $\text{PtO}_x$  gate contact under 100% oxygen atmosphere was performed. The sputtering times were fixed at 10 s, 40 s and 80 s. Subsequently, the contact was capped with a platinum layer sputtered under pure argon atmosphere for 30 s. For both processes, the sputtering power was fixed at 30 W. Three identical [! (!)3]ZTO samples were used, which have an effective thickness of  $d_{\text{eff}} = 10$  nm, a resistivity of  $\rho = 0.2 \Omega \text{ cm}$  and a free carrier concentration of  $5.4 \times 10^{18} \text{ cm}^{-3}$ . The three



**Figure 5.15:** Transfer characteristics and gate leakage currents for the three different sputtering times of the  $\text{PtO}_x$  contact in the (a) as deposited and (b) aged for 145 days state. A drain voltage of 2 V was applied and the dimensions are  $d_{\text{eff}} = 10$  nm and  $W/L = 100 \mu\text{m}/10 \mu\text{m}$ .

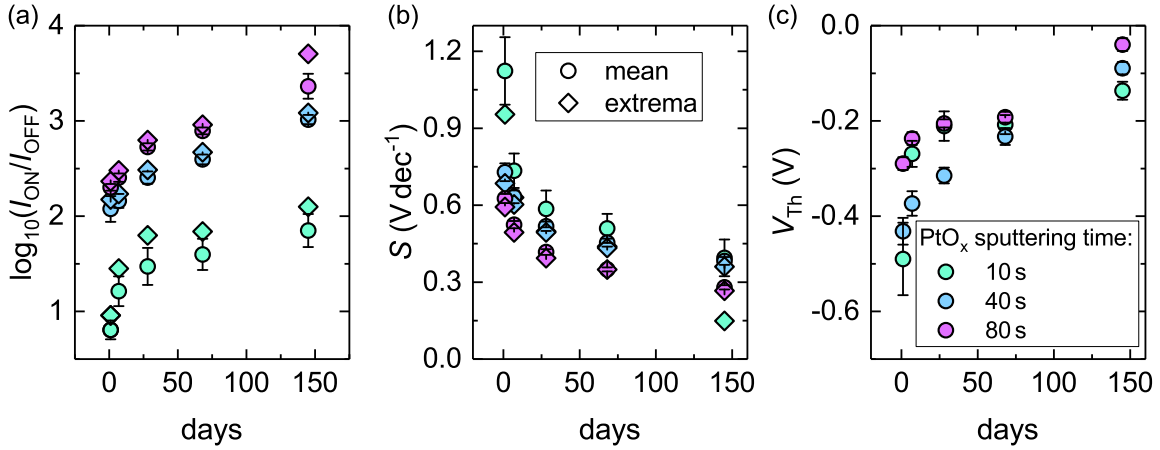
samples were measured in the as deposited state and then after the predefined times of 7, 28, 68 and 145 days.

In Figure 5.15 (a), the transfer characteristics and gate leakage currents measured directly after the device fabrication for the three different sputtering times are depicted. These characteristics are called 'as deposited' in the following. The on-current of all samples is very similar, as expected from the identical thin films used for the contact fabrication. The sample with a gate contact sputtered for 10 s under pure oxygen exhibits the highest off-current of  $2.8 \times 10^{-6}$  A. The high off-current is due to the high gate leakage current.

For  $\text{PtO}_x$  sputtering times of 40 s and 80 s under pure oxygen atmosphere, the reverse gate leakage current is reduced drastically. This leads to a significant drop of the off-current of the FETs. Values as low as  $1.5 \times 10^{-7}$  A and  $1.0 \times 10^{-7}$  A are achieved for sputtering times of 40 s and 80 s, respectively.

As expected, the off-current of the FETs further decreases with a longer storage time. In Figure 5.15 (b), the transfer characteristics and gate leakage currents after a storage time of 145 days are depicted. For all three sputtering times, a decrease of the off-current is observable, whereas the on-current remains unaltered. The off-current decreases by approximately one order of magnitude for the transistors with a  $\text{PtO}_x$  sputtering time of 10 s and 40 s and by almost 1.5 orders of magnitude for the FET with a  $\text{PtO}_x$  sputtering time of 80 s.

These results indicate that the larger oxygen reservoir for longer sputtering times of the platinum under pure oxygen atmosphere leads to a higher rectification of the gate contact

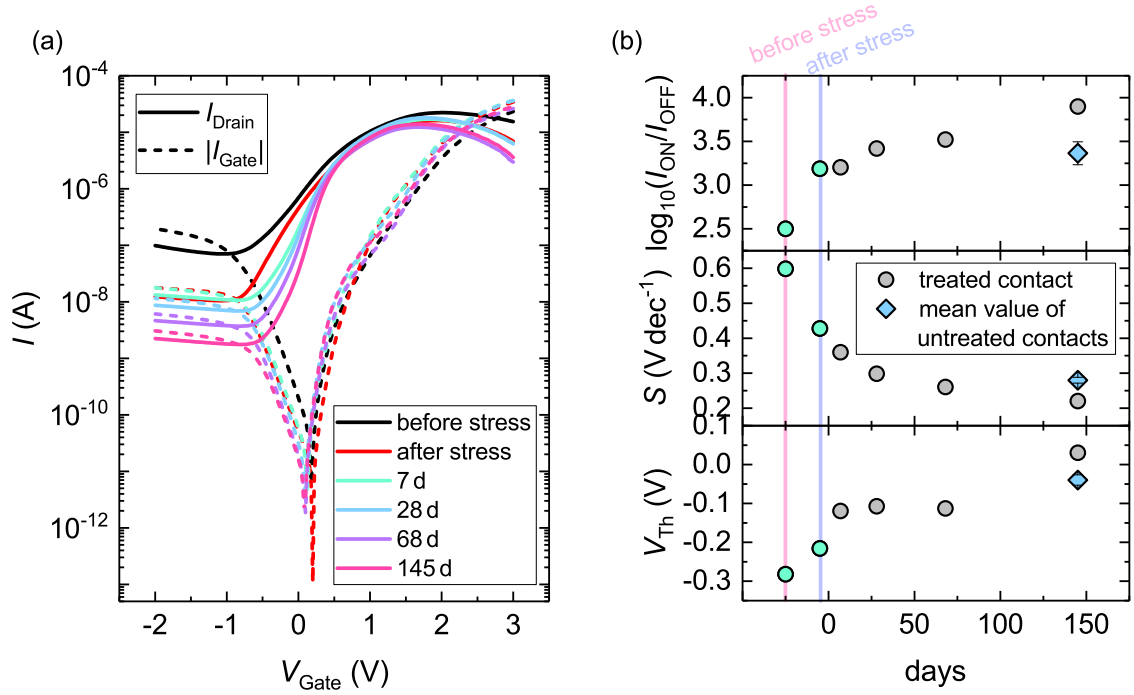


**Figure 5.16:** Arithmetic mean value (and extrema) of the (a) logarithmic drain current on-to-off ratio (maximum), (b) sub-threshold swing (minimum) and (c) threshold voltage in dependence on the storage time for the three different sputtering times of the PtO<sub>x</sub> contact under pure oxygen atmosphere. The standard deviation is extracted from the calculation of the arithmetic mean.

in the as deposited state. This might be due to the higher amount of Pt(OH)<sub>4</sub> in a larger reservoir, which diffuses very quickly. The larger oxygen reservoir due to the longer sputtering time under pure oxygen atmosphere is most likely the origin of the stronger improvement over time of the transistor with the PtO<sub>x</sub> gate contact sputtered for 80 s.

A more detailed look at the time resolved change of the characteristic parameters of the transistors is given in Figure 5.16. The mean over 15 contacts and the maximum logarithmic drain current on-to-off ratio and minimum sub-threshold swing values are depicted. Especially the drain current on-to-off ratio tends to saturate for the FET with a 10 s sputtered PtO<sub>x</sub> gate contact. This earlier saturation of this sample is expected, as it possesses the smallest oxygen reservoir. And even though the [! (!)3]ZTO thin films are identical for all three PtO<sub>x</sub> sputtering times, the sample with a gate contact sputtered for 80 s exhibits an 1.5 orders of magnitude higher drain current on-to-off ratio compared to the sample with a sputtering time of 10 s. This again stresses the important role that a large enough oxygen reservoir plays for the formation of these rectifying contacts. A drawback of the large oxygen reservoir is that the drain current on-to-off ratio does not saturate and the sample with a sputtering time of 80 s of the PtO<sub>x</sub> gate contact is not stable up to a storage time of 145 days. After 145 days, the maximum drain current on-to-off ratio has increased from an initial value of 232 to a value of  $5 \times 10^3$ .

The sub-threshold swing exhibits the expected decrease with increasing sputtering time of the PtO<sub>x</sub> contact and increasing storage time. After a storage time of 145 days, values below 350 mV dec<sup>-1</sup> are achieved for all three samples. The threshold voltage shifts to higher values upon storage. As for the sub-threshold swing, the sample with a gate contact sputtered under 100% oxygen atmosphere for 80 s exhibits the smallest change upon aging (compare Figure 5.16 (b,c)). This is likely due to the already superior performance of the FET in the as

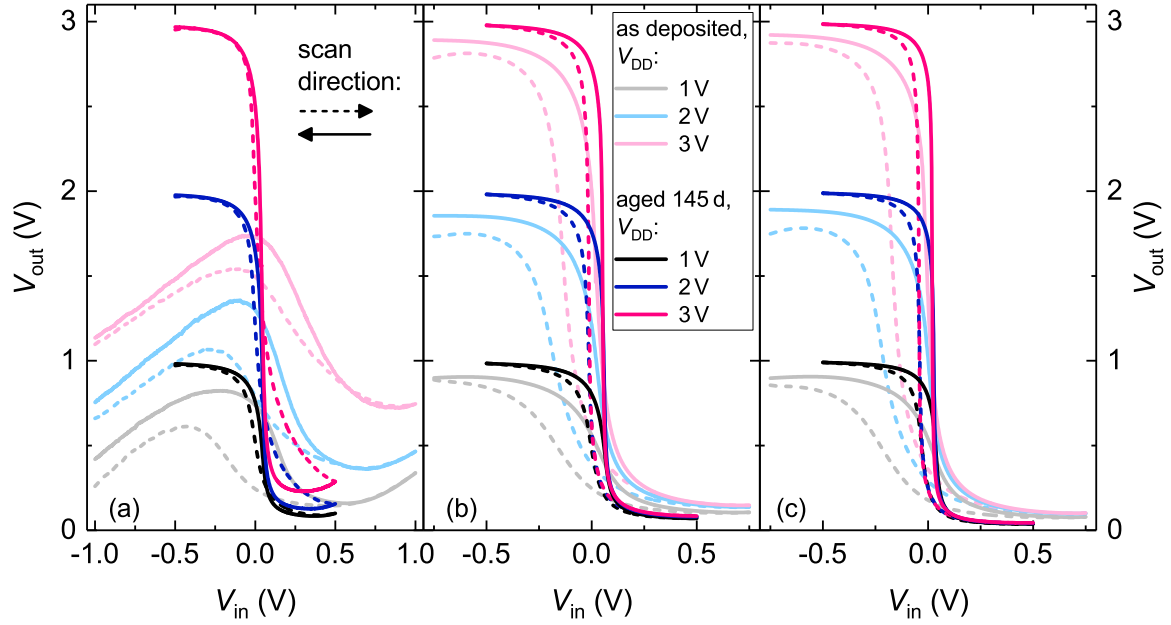


**Figure 5.17:** Transfer characteristics and gate leakage currents (a) for a FET with  $\text{PtO}_x$  gate contact sputtered under 100% oxygen atmosphere for 80 s and (b) the corresponding drain current on-to-off ratio, sub-threshold swing and threshold voltage. Further, the arithmetic mean values of the untreated contacts after a storage time of 145 days are depicted. The contact was stressed for 2.8 h at  $V_{\text{Gate}} = -1.5$  V. A drain voltage of 2 V was applied during the measurement of the transfer characteristics. The dimensions are  $d_{\text{eff}} = 10$  nm and  $W/L = 100 \mu\text{m}/10 \mu\text{m}$ .

deposited state compared to the two lower sputtering times.

For the potential use of  $[\text{!}(\text{!})3]\text{ZTO}$  in commercial devices, the change of the characteristic FETs parameters over time is problematic. A common technique in industry is the annealing (e.g. by thermal or voltage stress) of devices. In this work, the use of a voltage stress was chosen to purposefully elicit the change in the transfer characteristics of the transistor. Therefore, the sample with a  $\text{PtO}_x$  gate contact sputtered under 100% oxygen atmosphere for 80 s was used for the application of a voltage stress, as this sample exhibits the most promising characteristic parameters of the transistors.

The experiment was conducted by measuring the transfer characteristics of a FET in the as deposited state and then applying a negative bias of  $-1.5$  V at the gate contact for 1000 s. Subsequently, the transfer characteristics were recorded again and the next bias application cycle was started. This was repeated 10 times until a total bias application time of 2.8 h was reached. In Figure 5.17 (a), the transfer characteristics before the bias application, directly afterward and then after storage times between 7 days and 145 days of one FET are depicted. A strong decrease of the off-current during the bias application is visible. The subsequent change in the transfer characteristics is small, compared to the initial change induced by the bias application. However, a further decrease of the off-current is still visible.



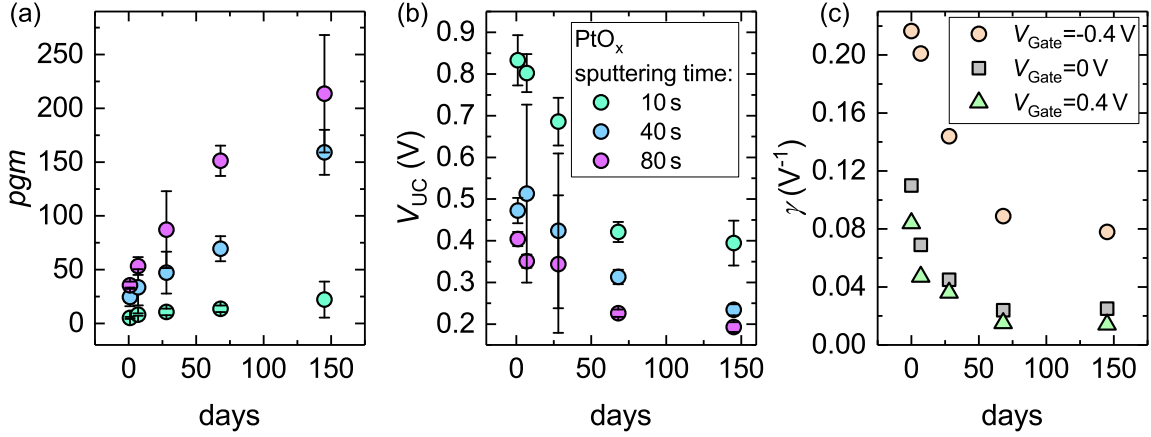
**Figure 5.18:** Voltage transfer characteristics in the as deposited and aged state for sputtering times of the  $\text{PtO}_x$  gate contact under 100% oxygen atmosphere of (a) 10 s, (b) 40 s and (c) 80 s.

The drain current on-to-off ratio was increased by almost one order of magnitude by the bias application, as is shown in Figure 5.17 (b). After 28 days it is one order of magnitude higher than in the initial state and higher than the mean drain current on-to-off ratio of the non-treated contacts after 145 days. Even though, a further increase of the drain current on-to-off ratio is observed up to 145 days storage time. In other words: a bias treatment for approximately 3 h can elicit the same aging effect as a storage of the samples in ambient condition for 145 days.

A longer bias treatment time could likely reduce the aging after the bias application. Dang *et al.* investigated the use of thermal stress additional to the application of a bias stress [14]. The results are promising and a pure thermal treatment of the MESFETs could also induce an accelerated aging.

The sub-threshold swing decreases upon bias application and further decreases upon storage. A minimum value of  $220 \text{ mV dec}^{-1}$  is reached after 145 days. This value is very similar to the arithmetic mean value of the untreated FETs after the same storage time (compare Figure 5.17 (b)). The threshold voltage exhibits the expected shift to positive values. Here, also no saturation is visible in the investigated time span. A longer bias application time might lead to a better saturation of the drain current on-to-off ratio as well as the threshold voltage.

Additionally to the FETs, simple inverters were investigated using the three sputtering times



**Figure 5.19:** Mean peak gain magnitude (a) and uncertainty level (b) for a voltage sweep direction from positive to negative voltages and an operating voltage of 3 V in dependence on the aging time. (c) For a sputtering time of 80 s of the  $\text{PtO}_x$  gate contact, the time evolution of  $\gamma$  determined from the output characteristics for three different gate voltages is depicted.

under pure oxygen atmosphere for the  $\text{PtO}_x$  gate contact. The voltage transfer characteristics for the three contact types are depicted in Figure 5.18 in the as deposited and aged state. For a sputtering time of 10 s (compare Figure 5.18 (a)), the strong influence of the threshold voltage on the logic swing is visible. The mean threshold voltage (compare Figure 5.16 (c)) increases from a value of  $-0.5$  V in the as deposited state to a value of  $\approx -0.1$  V after 145 days. This leads to an increase of the logic swing from 0.8 V to 2.6 V for an operating voltage of 3 V in the same time span. Moreover, the voltage transfer characteristics become much steeper for all three operating voltages.

For sputtering times of the  $\text{PtO}_x$  gate contact of 40 s and 80 s, the change in the logic swing is much less pronounced (compare Figure 5.18 (b,c)). For an operating voltage of 3 V a logic swing of 2.7 V and 2.8 V is reached for sputtering times of 40 s and 80 s, respectively, after an aging for 145 days.

Further, the hysteresis of the voltage transfer characteristics significantly reduces for all three contact configurations. This is directly related to a reduction of the hysteresis in the transfer characteristics. The origin of the hysteresis might be the charging and discharging of interface trap states, which are reduced in density due to the aging. A longer integration time leads to a further reduction of the hysteresis, which supports the hypothesis of trap states as origin of the hysteresis.

As can be expected from the steeper characteristics after the aging, the peak gain magnitude increases with increasing aging time. In Figure 5.19 (a) the arithmetic mean of the  $pgm$  is depicted for an operating voltage of  $V_{DD} = 3$  V. The error bars denote the standard deviation. To increase the lucidity, only the values obtained for a voltage sweep direction from positive to negative voltages are depicted. For all three sputtering times of the  $\text{PtO}_x$  gate contact, an increase of the  $pgm$  with increasing aging time is observed. However, the change is most pronounced for sputtering times of 40 s and 80 s. For a sputtering time of 40 s a mean and

maximum  $pgm$  of 22 and 70, respectively, are measured after 145 days aging and  $V_{DD} = 3\text{ V}$ . The highest mean and maximum values of the  $pgm$  are obtained for a  $PtO_x$  gate contact sputtering time of 80 s and an aging time of 145 days. A mean value of 213 and a maximum value of 263 were measured.

The uncertainty level, which is depicted in Figure 5.19 (b), decreases with increasing aging time for all three gate contact sputtering times. For a sputtering time of 80 s, the change is least pronounced. The mean uncertainty level for  $V_{DD} = 3\text{ V}$  is reduced from 0.4 V to below 0.2 V. In contrast, for a sputtering time of 10 s it decreases from 0.85 V to 0.4 V.

As described in chapter 2.4, the peak gain magnitude of an inverter can be directly related to the factor  $\gamma$ , which describes the non-ideal, linear increase of the FETs' output characteristics in the saturation regime. In theory,  $\gamma$  is treated like an additional output resistance, which should be equal for all applied gate voltages [54]. In this case,  $\gamma$  changes with the applied gate voltage.

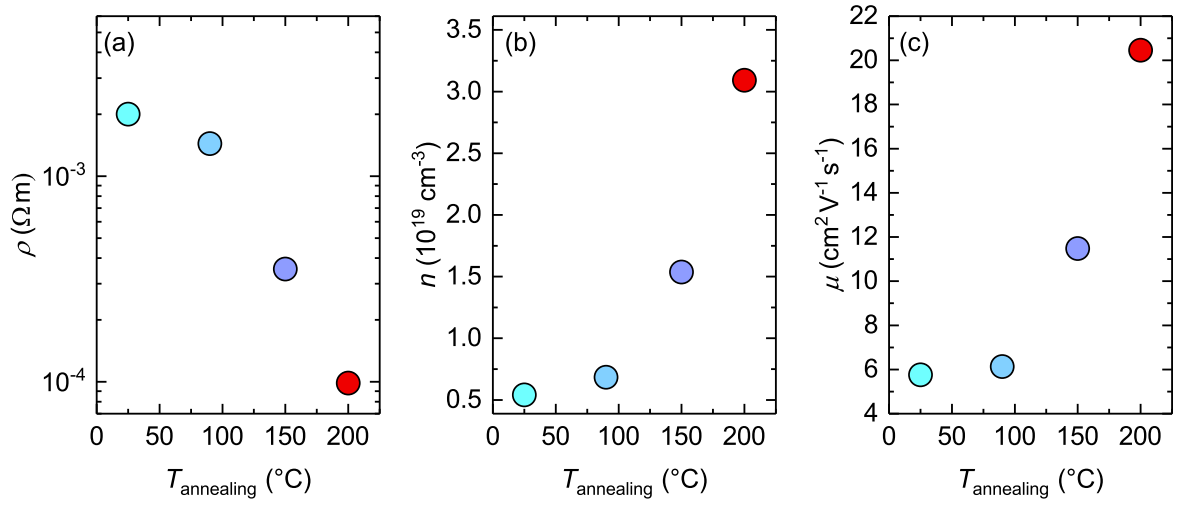
For a  $PtO_x$  gate contact sputtering time of 80 s, the factor  $\gamma$  is depicted in Figure 5.19 (c) for gate voltages of  $V_{Gate} = -0.4\text{ V}$ ,  $V_{Gate} = 0\text{ V}$  and  $V_{Gate} = 0.4\text{ V}$  with increasing aging time. A strong decrease of  $\gamma$  with increasing aging time is observed, which directly explains the strong increase of the  $pgm$  over time.  $\gamma$  drops from a value of approximately  $0.1\text{ V}^{-1}$  in the as deposited state to a value of  $0.02\text{ V}^{-1}$  after 145 days of aging for  $V_{Gate} \geq 0\text{ V}$ . For  $V_{Gate} = -0.4\text{ V}$ , it drops from a value of  $\approx 0.2\text{ V}^{-1}$  to a value of  $0.08\text{ V}^{-1}$ . Only for this gate voltage  $\gamma$  exhibits a continued change after 68 days of aging.

As mentioned above,  $\gamma$  is independent of the applied gate voltage in the ideal case. This is not observed in the transistor investigated here. For negative applied gate voltages, where the transistor is almost off,  $\gamma$  is significantly larger than for zero volt or positive gate voltages. This means that the non-ideal increase of the output characteristics is larger in the case that the transistor is almost off ( $V_{Gate} = -0.4\text{ V}$ ). For an almost open channel, the output characteristics become more ideal and  $\gamma$  is smaller.

If one were to use the model of an output resistor, this would translate to a large output resistance for small  $\gamma$  values and a small output resistance for large  $\gamma$  values.

A reason for this change with changing applied voltage might be the inhomogeneous doping profile of the channel. The oxygen variation layer below the conductive channel is assumed to not influence the behavior of the FETs, however for very small currents flowing in the nearly off regime, it might play a role.

Additionally, a second doping profile is introduced by the diffusion of oxygen from the gate contact into the  $[Zn_{1-x}Sn_x]ZTO$  channel. It is assumed that with longer aging times oxygen diffuses deeper into the  $[Zn_{1-x}Sn_x]ZTO$  channel and therefore the value  $\gamma$  decreases and converges for all applied gate voltages.



**Figure 5.20:** Resistivity (a), free carrier density (b) and electron mobility (c) in dependence on the annealing temperature. The sample depicted at 25°C denotes the as deposited [! (!)3]ZTO thin film.

### 5.2.3 Tuning of the Electron Mobility

As described before, the goal is the use of [! (!)3]ZTO based devices in integrated circuits. For many of these devices, the switching speed of the FETs is of importance. The aim in this chapter was therefore to achieve an increase of the electron mobility and therewith conductivity of the channel. An increase of the conductivity is also of importance if the [! (!)3]ZTO based FETs are used to drive OLEDs, which require a certain power supply to function.

Most [! (!)3]ZTO based devices reported in literature are either deposited at elevated temperatures or thermally annealed after the deposition to achieve well working FETs. Dang *et al.* report that the drain current on-to-off ratio of their MESFETs increases by two orders of magnitude by annealing the [! (!)3]ZTO channel at 525°C instead of 450°C [14].

In this work a softer thermal annealing at lower temperatures was performed, which would still be suitable if organic, thermally unstable substrates were used. The thermal annealing temperatures were chosen as 90°C, 150°C and 200°C. For comparison, a room temperature deposited sample was fabricated equivalently to the thermally annealed samples.

To acquire the electrical properties of the thin films, planar [! (!)3]ZTO thin films were thermally annealed in the same process as the [! (!)3]ZTO channels. The thermal annealing was conducted under normal atmosphere in an oven for 1 h. In Figure 5.20, the electrical properties of the as deposited and the thermally annealed samples are shown. The resistivity decreases with increasing annealing temperature by one order of magnitude. In the as deposited state it is  $2 \times 10^{-3} \Omega \text{m}$ , whereas it is as low as  $1 \times 10^{-4} \Omega \text{m}$  for an annealing at 200°C (compare Figure 5.20 (a)). The free carrier density and electron mobility, both determined by Hall effect measurements, increase with increasing annealing temperature. A strong change

in the free carrier density is observed for annealing temperatures above 90°C. The free carrier density increases up to a value of  $3.1 \times 10^{19} \text{ cm}^{-3}$  for an annealing at 200°C. The net doping density was approximated by performing [! (!)3]QSCV measurements on the FETs. The net doping density was approximated as  $\approx 2 - 4 \times 10^{19} \text{ cm}^{-3}$  for all thermal annealing temperatures. Therefore, the free carrier density and the net doping density converge with increasing annealing temperatures.

The gate capacitance at  $V_{\text{Gate}} = 0 \text{ V}$  was determined as 15 – 16 pF for all thermal annealing temperatures.

In Figure 5.20 (c), the electron mobility determined by Hall effect measurements is depicted in dependence on the annealing temperature. It exhibits a strong increase with increasing annealing temperature. For an annealing at 200°C, a value of  $20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  was measured. This value is more than three times as high as that of the as deposited sample.

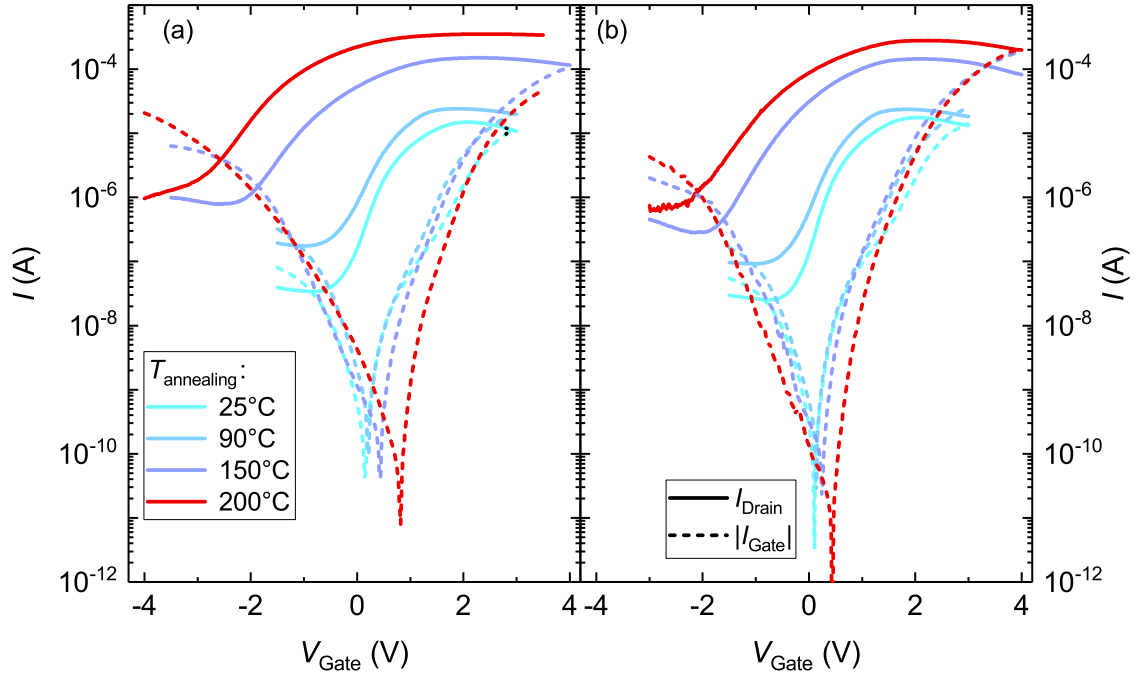
The resistivity, free carrier density and electron mobility do not change significantly for an annealing at 90°C compared to the as deposited samples. This is noteworthy, as during the device fabrication, the samples are treated shortly at 90°C during the device patterning (see chapter 3.1.3).

On all samples [! (!)3]XRD measurements were performed, which yielded that the thin films are X-ray amorphous.

In summary, thermal annealing at temperatures between 150°C and 200°C leads to a strong decrease of the thin film resistivity and an increase of the electron mobility as well as the free carrier density.

To rule out that higher thermal annealing temperatures lead to a further increase of the electron mobility, a thermal annealing at 250°C was conducted. It leads to an increase of the thin film resistivity and a decrease of the electron mobility, while the thin films were still X-ray amorphous. The results for this thermal annealing temperature are not shown here.

[! (!)3]ZTO channels, which were annealed simultaneously with the planar thin films, were used to fabricate MESFETs. The gate consists of platinum oxide, which was sputtered for 80 s under pure oxygen atmosphere, capped with a metallic platinum layer. In Figure 5.21 (a) the as deposited transfer characteristics and gate leakage currents for the different annealing temperatures are depicted. To increase the lucidity of the results, only the voltage sweep direction from positive to negative voltages is depicted. Due to the decrease of the thin film resistivity, the on-current of the transistors increases with increasing annealing temperature. For the as deposited sample an on-current of  $1.5 \times 10^{-5} \text{ A}$  is measured. The sample annealed at 200°C exhibits an on-current as high as  $3.4 \times 10^{-4} \text{ A}$ . In addition, an increase of the off-current and a shift of the off-state of the transistors to more negative voltages is observed. The samples were stored in ambient atmosphere for 28 days after the measurement and then re-measured. The corresponding transfer characteristics are shown in Figure 5.21 (b). As expected, the on-current is unaltered by the aging, whereas the off-current decreases slightly for all annealing temperatures. This leads to a shift of the off-state to more positive voltages. For the aged samples, the voltage required to turn the transistor from off to on is  $\Delta V_{\text{ON}} = 2.7 \text{ V}$  for the as



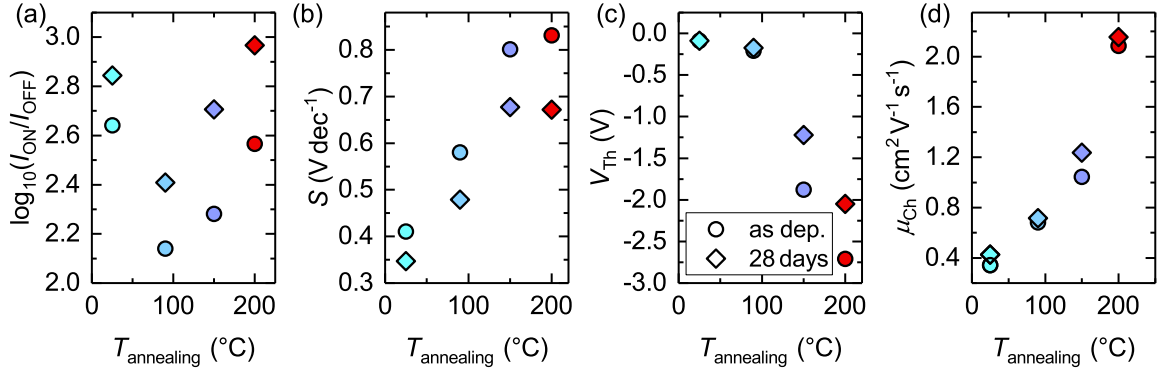
**Figure 5.21:** Transfer characteristics and gate leakage currents of samples annealed at different temperatures in the (a) as deposited and (b) (28 days) aged state. The non-annealed sample is denoted by 25°C. The effective channel thickness is 10 nm and  $W/L = 100\text{ }\mu\text{m}/10\text{ }\mu\text{m}$ . A drain voltage of 2 V was applied during the measurement of the transfer characteristics.

deposited and  $\Delta V_{\text{ON}} = 4.6\text{ V}$  for the sample annealed at 200°C after an aging of 28 days.

The gate characteristics are very similar for all thermal annealing temperatures. The change of the off-current is mainly due to an increase of the threshold voltage due to the higher free carrier densities for higher thermal annealing temperatures.

Using a *MATLAB* program written by Daniel Splith<sup>8</sup>, the characteristic parameters of the MESFETs were extracted from the transfer characteristics. In Figure 5.22 (a) the drain current on-to-off ratio is depicted for the as deposited and aged devices in dependence on the annealing temperature. For all thermal annealing temperatures an increase of the drain current on-to-off ratio is visible. After the aging, the highest drain current on-to-off ratio is measured for an annealing at 200°C, for which it is almost three orders of magnitude. However, the sub-threshold swing and threshold voltage for an annealing at 200°C are as large as  $0.7\text{ V dec}^{-1}$  and almost  $-2\text{ V}$ , respectively. The sub-threshold swing and threshold voltage are depicted in Figure 5.22 (b,c) in dependence on the thermal annealing temperature. An overall increase of the sub-threshold swing is measured with increasing annealing temperature. The aging leads, as expected, to a decrease of the sub-threshold swing for all annealing temperatures. The change is most pronounced for the highest annealing temperatures, as these characteristics exhibit the highest sub-threshold swings in the as deposited state. The threshold voltage shifts to negative values with increasing annealing temperature. For the

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**Figure 5.22:** Drain current on-to-off ratio (a), sub-threshold swing (b), threshold voltage (c) and channel mobility (d) in dependence on the thermal annealing temperature.

non-annealed sample and the sample annealed at 90°C, the threshold voltage is close to zero volt and does not change significantly upon aging. In contrast, for the samples annealed at 150°C and 200°C, the threshold voltage is as large as  $-2 \text{ V}$  and almost  $-3 \text{ V}$ , respectively, in the as deposited state. After an aging of 28 days it shifts to more positive values by almost  $1 \text{ V}$  for both annealing temperatures.

Using the maximal transconductance and the net doping density  $N_t$  of the samples, which was determined by [! ([!)]3]QSCV measurements, the channel mobility  $\mu_{\text{Ch}}$  can be calculated by

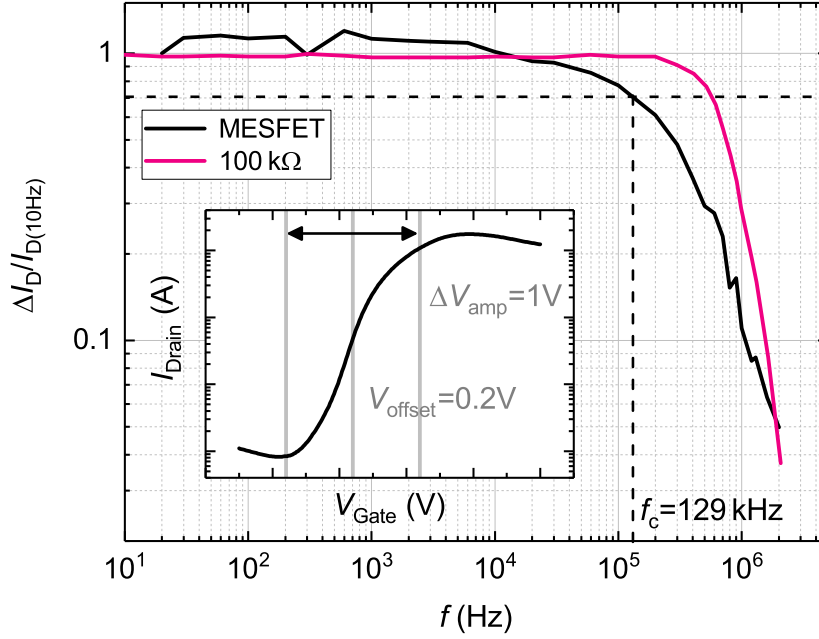
$$\mu_{\text{Ch}} = \frac{g_{\text{max}}}{\frac{W}{L} \cdot N_t \cdot d_{\text{eff}} \cdot e} . \quad (5.1)$$

The calculated channel mobilities for the different annealing temperatures are depicted in Figure 5.22 (d). As already observed for the electron mobility determined by Hall effect measurements, the channel mobility increases with increasing annealing temperature. For the as deposited sample a channel mobility of  $0.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  was determined, whereas it is as high as  $2.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  for the sample annealed at 200°C. It has to be noted that these values are a factor ten lower than those obtained by Hall effect measurements.

It is therefore possible to achieve an increase of the channel mobility as well as the on-current by a thermal annealing of the [! ([!)]3]ZTO channels. The drain current on-to-off ratio is very similar for the as deposited sample and the sample annealed at 200°C. However, the tradeoff are higher sub-threshold swings and threshold voltages compared to the as deposited thin films and an additional processing step is required.

## 5.2.4 Frequency Dependent Switching of Transistors

As mentioned above, the switching speed of FETs between the on- and off- state is of great interest for the use in integrated circuits and especially for high frequency applications in the MHz range. To gauge the switching speed of the previously described devices, gate lag measurements were conducted. These allow the assessment of the signal lag induced by

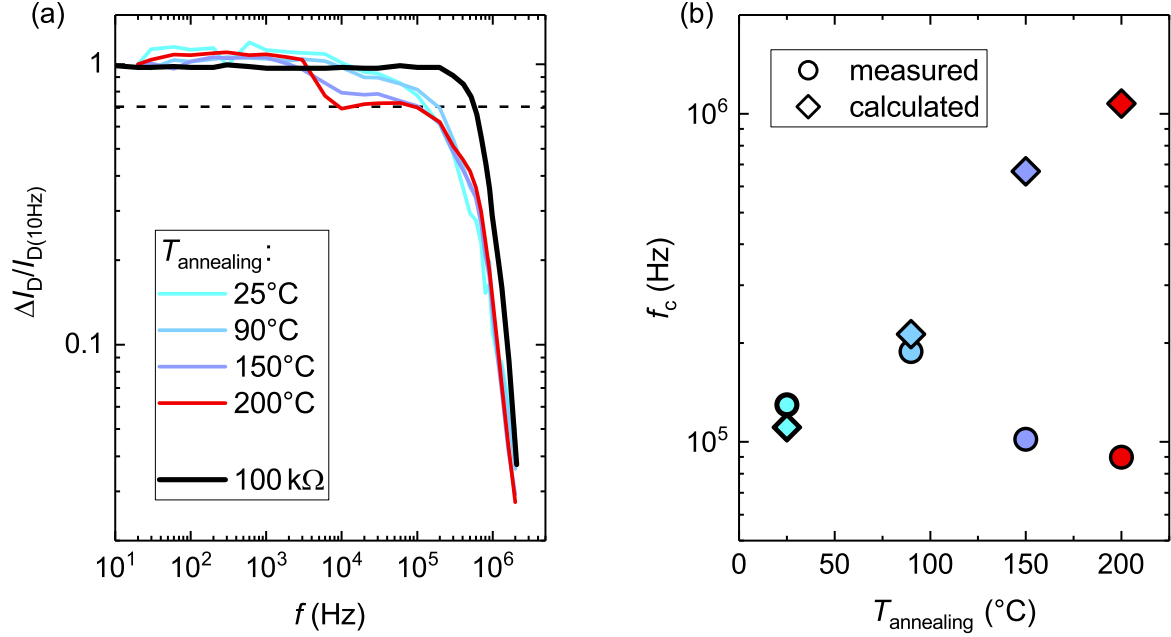


**Figure 5.23:** Frequency dependence of the drain current amplitude of a transistor for an amplitude of 1 V and an offset of 0.2 V, as well as the reference line obtained from a 100 k $\Omega$  resistance. The inlay depicts the transfer characteristic with the corresponding voltage offset and amplitude chosen for the measurement.

the gate contact. The measurement is conducted by applying an oscillating voltage signal with fixed amplitude  $V_{\text{amp}}$  and offset  $V_{\text{offset}}$  and a varying frequency at the gate contact. Simultaneously, a drain voltage of 2 V is applied. The applied frequency can be varied between 10 Hz to 2 MHz. The resulting modulations of the drain current are measured as an alternating current. The signal is read out over a 220  $\Omega$  resistance, which is in series to the drain contact. The signal is detected with a signal amplifier designed and built by Fabian Klüpfel<sup>9</sup>. The alternating gate voltage was supplied by a USB oscilloscope *Handyscope Hs3* by *TiePie*, which was also used for the detection of the amplified oscillations of the drain current [74, 112].

In Figure 5.23, the frequency dependence of the drain current amplitude of a MESFET is depicted. The device corresponds to the FET described in the previous section as non-annealed sample. The offset was chosen as 0.2 V and the signal was varied sinusoidal with an amplitude of 1 V. With these settings, the signal is varied between the nearly on- and nearly off-state of the transistor, as can be seen from the transfer characteristic in the inset in Figure 5.23. In the main plot, the normalized drain current amplitude is depicted on the  $y$ -axis. It is normalized to the drain current amplitude measured at 10 Hz. Up to a frequency of 10 kHz, the transistor fully switches between the nearly on- and nearly-off state. For higher frequencies, a decrease of the amplitude is detectable. The cut-off frequency  $f_c$ , which is

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**Figure 5.24:** (a) Frequency dependence of the drain current amplitude of transistors with as deposited and annealed [! (!)3]ZTO channel. (b) Measured and theoretically calculated cut-off frequency in dependence on the thermal annealing temperature. The transistor has dimensions of  $W = 100 \mu\text{m}$  and  $L = 10 \mu\text{m}$ .

defined as the point where the drain current amplitude signal has dropped to  $\frac{1}{\sqrt{2}}$  of its initial value, is determined as  $f_c = 129 \text{ kHz}$ . As can be seen from the frequency-dependent signal of the  $100 \text{ k}\Omega$  resistor, the cut-off of the measurement set-up is reached at a frequency of  $1 \text{ MHz}$ . The ohmic resistance of  $100 \text{ k}\Omega$  is used as a constant frequency independent amplitude is expected for this frequency range and device.

Size and Ng have formulated an equation with which the cut-off frequency of a FET can be estimated [39] as

$$f_c = \frac{g_{\max}}{2\pi C_G}, \quad (5.2)$$

where  $C_G$  is the gate capacitance, which can be estimated from [! (!)3]QSCV measurements. The equation yields that a high maximal transconductance or a lower gate capacitance lead to higher cut-off frequencies.

Therefore, the thermally annealed samples, described in the previous section are compared to the as deposited sample, as a thermal annealing leads to an increase of the maximal transconductance. It should therefore lead to an increase of the cut-off frequency. In Figure 5.24 (a) the dependence of the drain current amplitude for the as deposited sample is compared to that of thermally annealed samples.

The samples annealed at  $150^\circ\text{C}$  and  $200^\circ\text{C}$  exhibit a strong drop of the drain current amplitude at a frequency of about  $10 \text{ kHz}$ , whereas the signal of the as deposited and annealed at  $90^\circ\text{C}$

sample remain high until the cut-off frequency is reached.

The cut-off frequency for all annealing temperatures was determined from the measurement and calculated using equation 5.2. The corresponding values are depicted in Figure 5.24 (b). For the as deposited sample and the sample annealed at 90°C, the measured and calculated cut-off frequency are very similar. The highest cut-off frequency is obtained for the channel annealed at 90°C, for which it is  $f_c = 188$  kHz. Contrary to expectations, the measured cut-off frequency for annealing temperatures of 150°C and 200°C is lower than that for annealing temperatures  $T_{\text{annealing}} \leq 90^\circ\text{C}$ . Due to the increased maximal transconductance of these samples, the calculated value is much higher and a theoretical cut-off frequency of 1.1 MHz can be achieved for the sample annealed at 200°C.

The origin of the large deviation between measured and calculated cut-off frequency and the strong drop of the drain current amplitude at about 10 kHz for annealing temperatures  $T_{\text{annealing}} \geq 150^\circ\text{C}$  is unknown. A reason might be the formation of trap states, however further investigations are needed to gauge this effect. A possible way to investigate these trap states would be by capacitance-voltage measurements, but a requirement would be channels with larger effective thickness to obtain a higher depth resolution of the capacitance-voltage measurements.

## 5.3 Devices with $i$ -ZTO/PtO<sub>x</sub>/Pt Gate Contact

In the second part of this chapter, devices with  $i$ -ZTO/PtO<sub>x</sub>/Pt gate contacts are introduced. As described at the beginning of this chapter, the advantage of this gate contact type is the significantly higher drain-current on-to-off ratio. An investigation of the influence of the channel thickness on the performance of MESFETs for different gate geometries is discussed. Based on these results, simple and [! ([!3]SDFL inverters are presented. And last an inverter chain, as well as ring oscillators are presented.

The results on [! ([!3]SDFL inverters, inverter chains and ring oscillators were obtained in cooperation with Oliver Lahr<sup>10</sup> in the scope of his Master thesis.

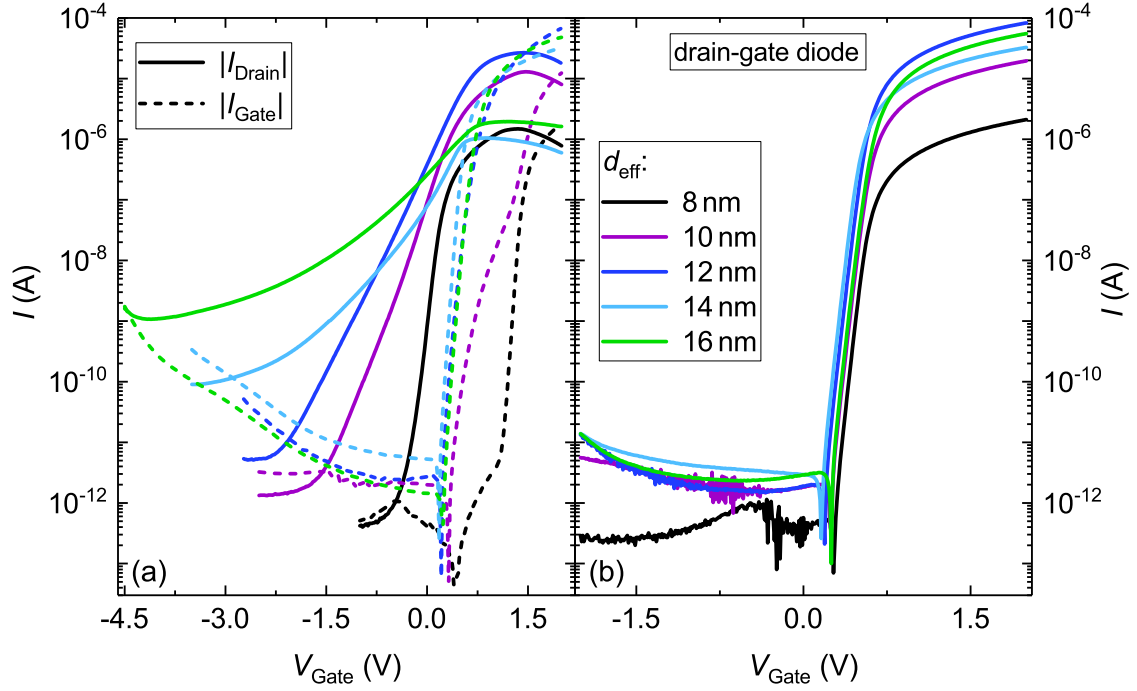
### 5.3.1 Transistors with Varying Channel Thickness

As already demonstrated in chapter 5.2, the channel thickness has a large influence on the performance of field-effect transistors. The goal in this chapter was to optimize the devices to achieve high drain current on-to-off ratios, low sub-threshold swings and threshold voltages close to zero volt. The channel thickness as well as the device geometry are varied to achieve this.

The used channel layers are identical to the thin films used in chapter 5.2 for the investigation of the influence of the channel thickness on the device properties.

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**Figure 5.25:** Exemplary transfer characteristics and gate leakage currents (a) and the corresponding drain-gate diode characteristics (b) for effective thin film thicknesses between 8 nm and 16 nm. A drain voltage of 2 V was applied during the measurement of the transfer characteristic and the geometry of the devices is  $W/L = 100 \mu\text{m}/10 \mu\text{m}$ .

In Figure 5.25 (a,b), the transfer characteristics with the corresponding gate leakage currents and the drain-gate diode characteristics for different effective channel thicknesses are depicted. Only the voltage sweep direction from positive to negative voltages is depicted. The drain-gate diodes show an increase of the series resistance with decreasing effective channel thickness. It is notable that the reverse current is below  $2 \times 10^{-11}$  A up to a reverse voltage of  $-2$  V for all channel thicknesses. For  $V_{\text{Gate}} \leq 1.5$  V, no tunneling current is visible. This low reverse current is due to the intrinsic *i*-ZTO layer, which acts as tunneling barrier [7].

The on-current of the transfer characteristics is limited by the gate current. Especially for the largest effective channel thicknesses of  $d_{\text{eff}} = 14$  nm and  $d_{\text{eff}} = 16$  nm, this effect is visible. The highest on-current of  $I_{\text{ON}} = 2.3 \times 10^{-5}$  A was measured for the device with an effective channel thickness of 12 nm.

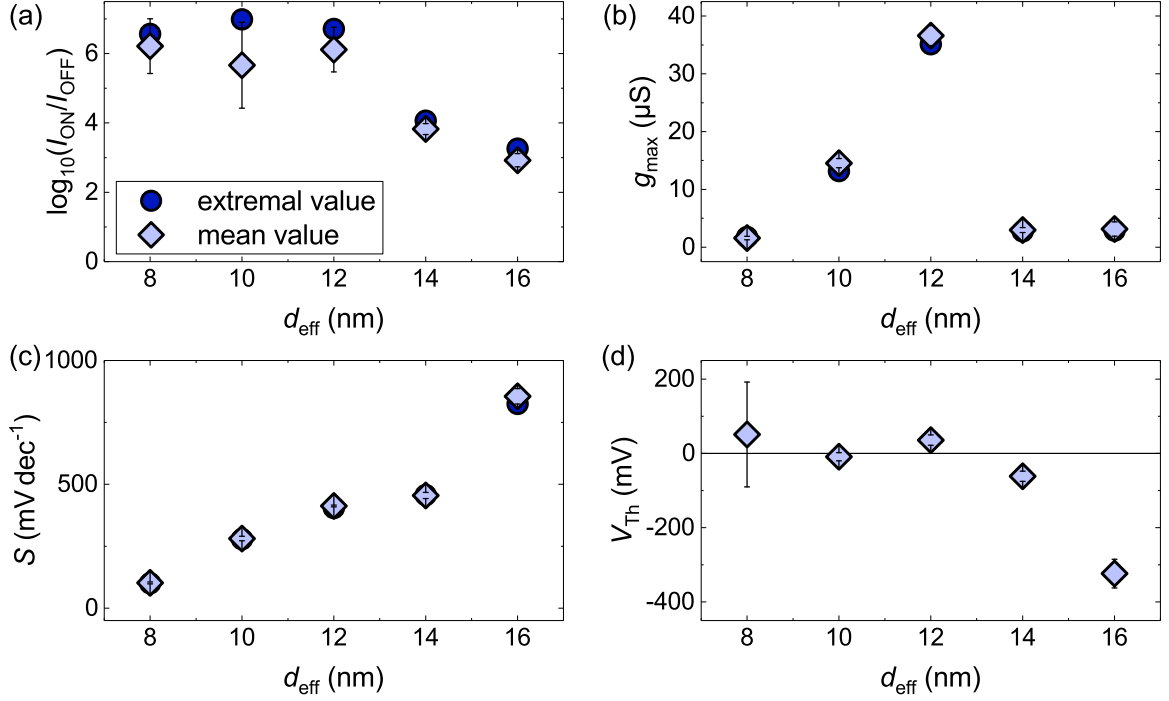
The off-current exhibits a systematic increase with increasing effective channel thickness. The lowest off-current of  $5 \times 10^{-13}$  A is measured for  $d_{\text{eff}} = 8$  nm. It increases by four orders of magnitude up to a value of  $1.1 \times 10^{-9}$  for  $d_{\text{eff}} = 16$  nm.

In contrast to the devices with  $\text{PtO}_x/\text{Pt}$  gate contact, the gate current in the transition region of the FETs is always lower than the drain current for the *i*-ZTO/ $\text{PtO}_x$ /Pt gate contact independent of the effective channel thickness.

The characteristic parameters of the transistors depicted in Figure 5.25 are listed in Table 5.2. The highest drain current on-to-off ratio of  $9.7 \times 10^6$  is obtained for an effective channel

**Table 5.2:** Drain current on-to-off ratio, maximal transconductance, sub-threshold swing, threshold voltage of the FETs depicted in Figure 5.25. In addition, the series resistance, effective barrier height and ideality factor of the drain-gate diodes are listed.

$d_{\text{eff}}$ nm	$I_{\text{ON}}/I_{\text{OFF}}$	$g_{\text{max}}$ $\mu\text{S}$	$S$ $\text{mV dec}^{-1}$	$V_{\text{Th}}$ mV	$R_s$ $\Omega$	$\phi_{\text{B,eff}}$ eV	$\eta$
8	$3.7 \times 10^6$	1.75	100	37	$6.4 \times 10^5$	1.2	1.05
10	$9.7 \times 10^6$	13.17	279	-22	$6.7 \times 10^4$	1.1	1.10
12	$5.1 \times 10^6$	35.13	404	37	$1.6 \times 10^4$	1.0	1.05
14	$1.2 \times 10^4$	2.73	457	-56	$4.3 \times 10^4$	1.0	1.05
16	$1.8 \times 10^3$	2.86	825	-314	$2.4 \times 10^4$	1.1	1.05

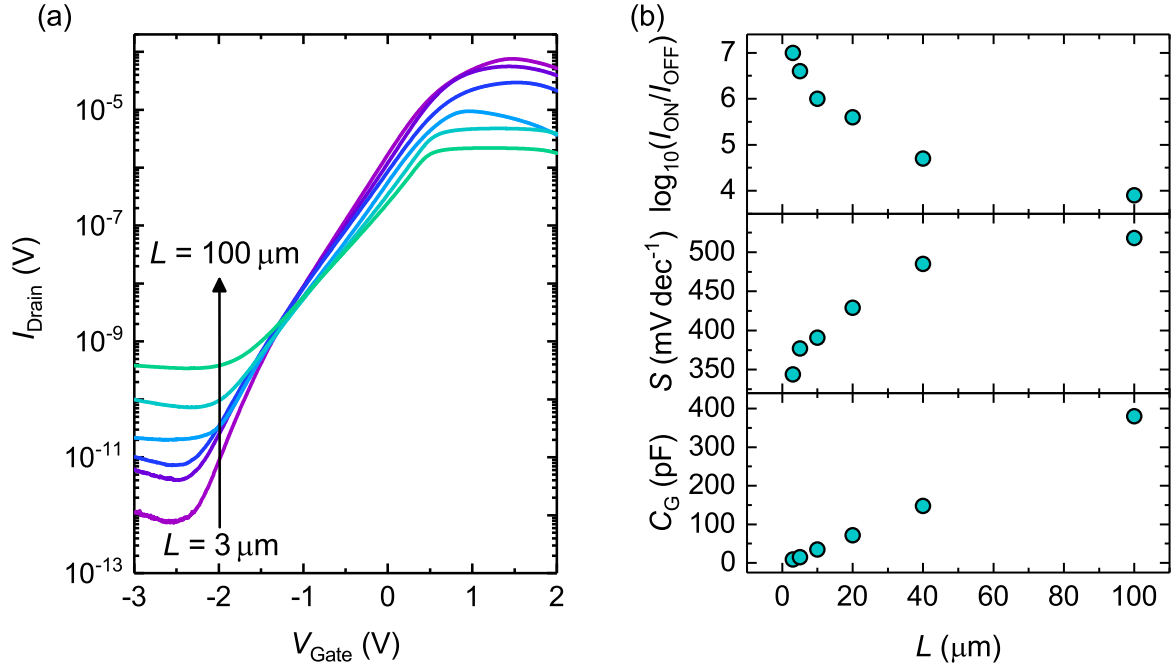


**Figure 5.26:** Mean (and extremal) values of the (a) logarithmic drain current on-to-off ratio (maximum), (b) maximal transconductance (maximum), (c) sub-threshold swing (minimum) and (d) threshold voltage in dependence on the effective channel thickness.

thickness of 10 nm. The lowest sub-threshold swing of  $100 \text{ mV dec}^{-1}$  is obtained for  $d_{\text{eff}} = 8 \text{ nm}$ . For this device only a voltage of  $\Delta V_{\text{ON}} = 2.1 \text{ V}$  is required to switch the device from off to on.

The threshold voltage is very close to zero volt for effective channel thicknesses between 8 nm and 14 nm. Only the sample with  $d_{\text{eff}} = 16 \text{ nm}$  has a threshold voltage as low as  $-0.3 \text{ V}$ . The sub-threshold swing of this sample is as high as  $0.8 \text{ V dec}^{-1}$ .

In addition, the series resistance obtained from the drain-gate voltage is listed. It increases with decreasing effective channel thickness. The ideality factor and effective barrier height were also determined and values of 1.05 and  $1.0 - 1.2 \text{ eV}$ , were obtained for all effective



**Figure 5.27:** Transfer characteristics (a) for varying gate length  $L$  and constant gate width  $W = 200 \mu\text{m}$ . The effective channel thickness is 10 nm and a drain voltage of 2 V was applied during the measurement of the transfer characteristics. (b) Logarithmic drain current on-to-off ratio, sub-threshold swing and gate capacitance in dependence on the gate length.

thicknesses, respectively (compare Table 5.2). No dependence of these parameters on the effective channel thickness was observed.

In Figure 5.26 (a-d), the arithmetic mean and extremal values of 15 transistors for each effective channel thickness are depicted. The sub-threshold swing is the only parameter that exhibits a monotonous dependence on the effective channel thickness. With increasing channel thickness, the sub-threshold swing also increases. In contrast, the drain current on-to-off ratio as well as the threshold voltage remain almost constant for effective thicknesses between 8 nm and 12 nm and then decrease. The standard deviations of all determined parameters are very small for all effective channel thicknesses.

For the threshold voltage, a guide to the eye is depicted at  $V_{\text{Th}} = 0 \text{ V}$ . For  $d_{\text{eff}} \leq 14 \text{ nm}$ , the threshold voltage is close to zero volt. The maximal transconductance does not exhibit a clear dependence on the effective channel thickness. A maximum value of  $35 \mu\text{S}$  is obtained for  $d_{\text{eff}} = 12 \text{ nm}$ . The origin of the smaller maximal transconductance for smaller effective channel thicknesses can be found in the higher resistance of these thin films. In contrast, for higher effective channel thicknesses it is limited by the gate leakage current.

A second important point is the geometry of the gate contact. For a channel thickness of  $d_{\text{eff}} = 10 \text{ nm}$  the transfer characteristics for gate lengths between  $2 \mu\text{m}$  and  $100 \mu\text{m}$  are depicted in Figure 5.27 (a). The gate width is kept constant at  $W = 200 \mu\text{m}$ . A strong increase of the on-current is visible for decreasing gate length. This is due to the increasing

$W/L$ -ratio, which - as expected - leads to a higher current flow through the channel. The on-current increases from a value of  $2.2 \times 10^{-6}$  A for  $L = 100 \mu\text{m}$  to a value of  $7.6 \times 10^{-5}$  A for  $L = 3 \mu\text{m}$ . In contrast, the off-current decreases with decreasing gate length. A decrease by three orders of magnitude is observable for a decrease of the gate length from  $100 \mu\text{m}$  to  $3 \mu\text{m}$ .

This leads to a strong increase of the drain current on-to-off ratio with decreasing gate length, as can be seen in Figure 5.27 (b). A maximum value of  $1 \times 10^7$  is obtained for  $L = 3 \mu\text{m}$ . The sub-threshold swing is minimal for the smallest gate length and increases with increasing gate length. However, the voltage required to turn the device from off to on decreases with increasing gate length. For a gate length of  $3 \mu\text{m}$  it is as high as  $\Delta V_{\text{ON}} = 3.6$  V, whereas it is as low as  $\Delta V_{\text{ON}} = 2.2$  V for a gate length of  $100 \mu\text{m}$ .

The threshold voltage is not depicted, as it is constant between  $-0.1$  V to  $-0.2$  V for all gate lengths.

For the use of the MESFETs in fast switching integrated circuits, the gate capacitance is important. It is therefore depicted for different gate lengths in Figure 5.27 (b).

The gate capacitance was determined by [! ([!3]QSCV measurements and using equation 2.8. A linear correlation between gate capacitance and gate length is expected:

$$C_G \propto \frac{A_0}{w} = \frac{WL}{w} . \quad (5.3)$$

This linear relation is very well visible in the here depicted data. A smaller gate length leads to a smaller gate capacitance for constant gate width.

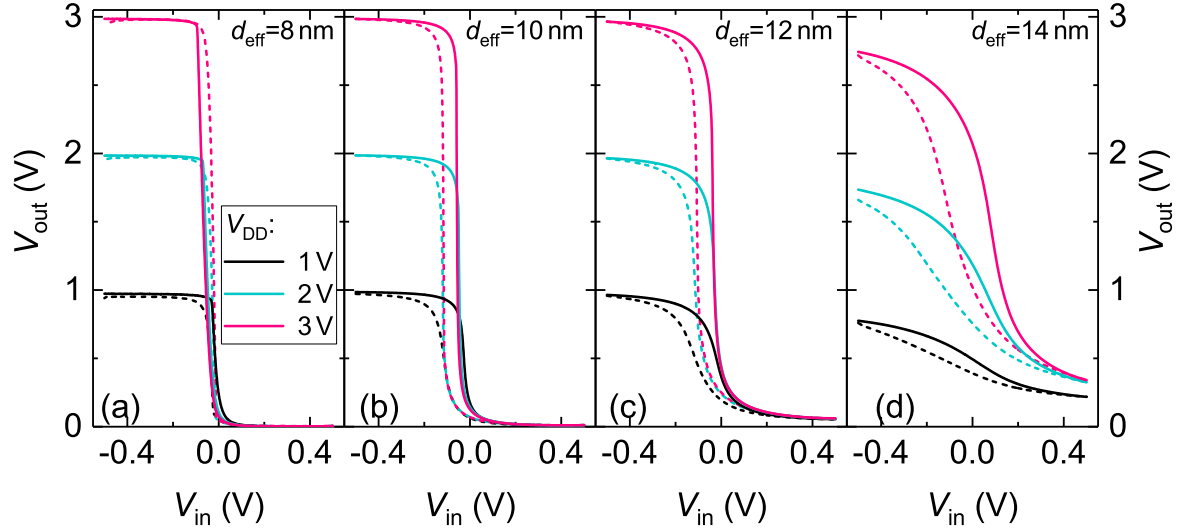
It is therefore possible to achieve a further optimization of the devices by a reduction of the gate length.

At this point it is of note that the gate capacitance does not change with the effective channel thickness for the devices presented here.

### 5.3.2 Simple Inverter

The MESFETs were connected to form simple inverters to determine the properties of a simple integrated circuit in dependence on the effective channel thickness. As the threshold voltage for all effective thin film thicknesses between 8 nm and 14 nm is  $\approx 0$  V, these effective channel thicknesses could be used to fabricate simple inverters.

The two MESFETs that built up the inverter have dimensions of  $W = 100 \mu\text{m}$  and  $L = 10 \mu\text{m}$ . In Figure 5.28, the voltage transfer characteristics for the different effective channel thicknesses are depicted for both voltage sweep directions. The operating voltage was chosen between 1 V and 3 V. The logic swing of the devices is 2.9 V ( $d_{\text{eff}} = 8$  nm), 2.8 V ( $d_{\text{eff}} = 10$  nm), 2.6 V ( $d_{\text{eff}} = 12$  nm) and 2.1 V ( $d_{\text{eff}} = 14$  nm) for an operating voltage of 3 V. The decrease of the logic swing of the sample with  $d_{\text{eff}} = 14$  nm can be attributed to the threshold voltage  $V_{\text{Th}} < 0$  V.



**Figure 5.28:** Voltage transfer characteristics of simple inverters based on MESFETs with effective channel thicknesses of (a) 8 nm, (b) 10 nm, (c) 12 nm and (d) 14 nm for three different operating voltages between 1 V and 3 V.

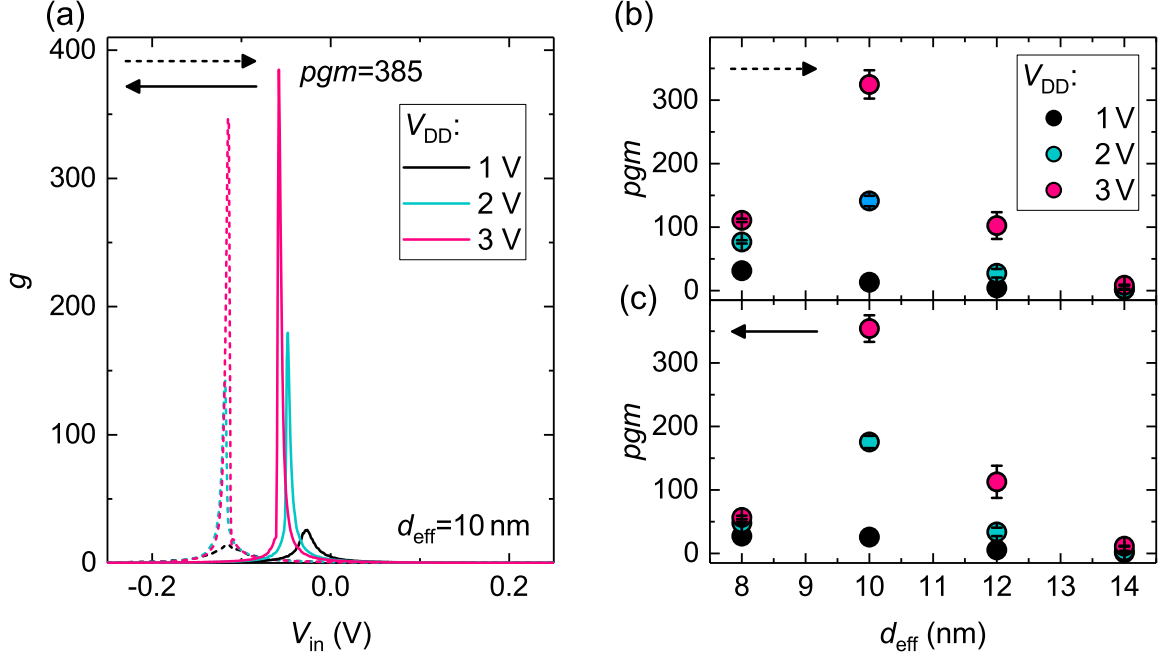
For all effective channel thicknesses a hysteresis is visible between the two voltage sweep directions, which increases with increasing effective channel thickness. This hysteresis can, as before, be attributed to the charging and discharging of interface trap states.

The characteristic parameters of the inverters were extracted from the voltage transfer characteristics and are depicted in Figure 5.29. The gain, which is exemplary shown for  $d_{\text{eff}} = 10$  nm, has a maximum value of  $\text{pgm} = 385$  for a voltage sweep direction from positive to negative voltages and an operating voltage of 3 V. In the opposite voltage scan direction a  $\text{pgm}$  of 350 is measured for the same operating voltage.

In Figure 5.29 (b,c) the arithmetic mean  $\text{pgm}$  for the two different voltage sweep directions is shown. The arithmetic mean was calculated using the values of 12 devices. A clear dependence of the  $\text{pgm}$  on the used operating voltage is visible. For higher operating voltages, higher peak gain magnitudes are obtained. The peak gain magnitude is highest for effective channel thicknesses of 10 nm. A maximum peak gain magnitude of 384 was measured for this sample. For effective channel thicknesses of 8 nm and 12 nm, maximum peak gain magnitudes of 113 and 160 were measured, respectively, for an operating voltage of 3 V. Compared to the simple, as deposited inverters presented in chapter 5.2, these  $\text{pgm}$  values are high. A maximum  $\text{pgm}$  of 83 was achieved for the sample with  $d_{\text{eff}} = 12$  nm and a  $\text{PtO}_x/\text{Pt}$  gate contact.

The inverters are very homogeneous in their performance, as can be seen from the small standard deviations.

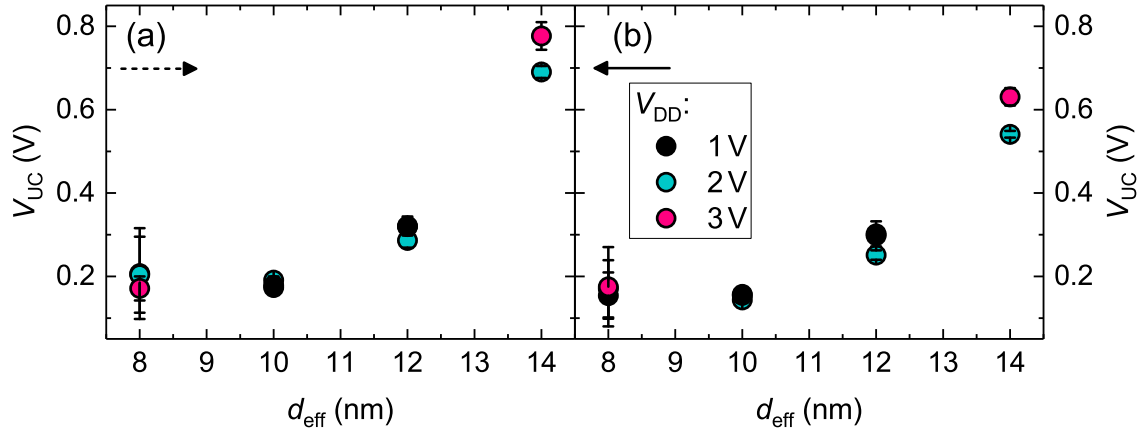
In Figure 5.30 (a,b) the arithmetic mean of the uncertainty level is depicted. An increase of the mean uncertainty level with increasing effective channel thickness is visible for both voltage scan directions. For all samples and operating voltages the uncertainty level is smaller for a voltage scan direction from positive to negative voltages. The deviation from the mean value



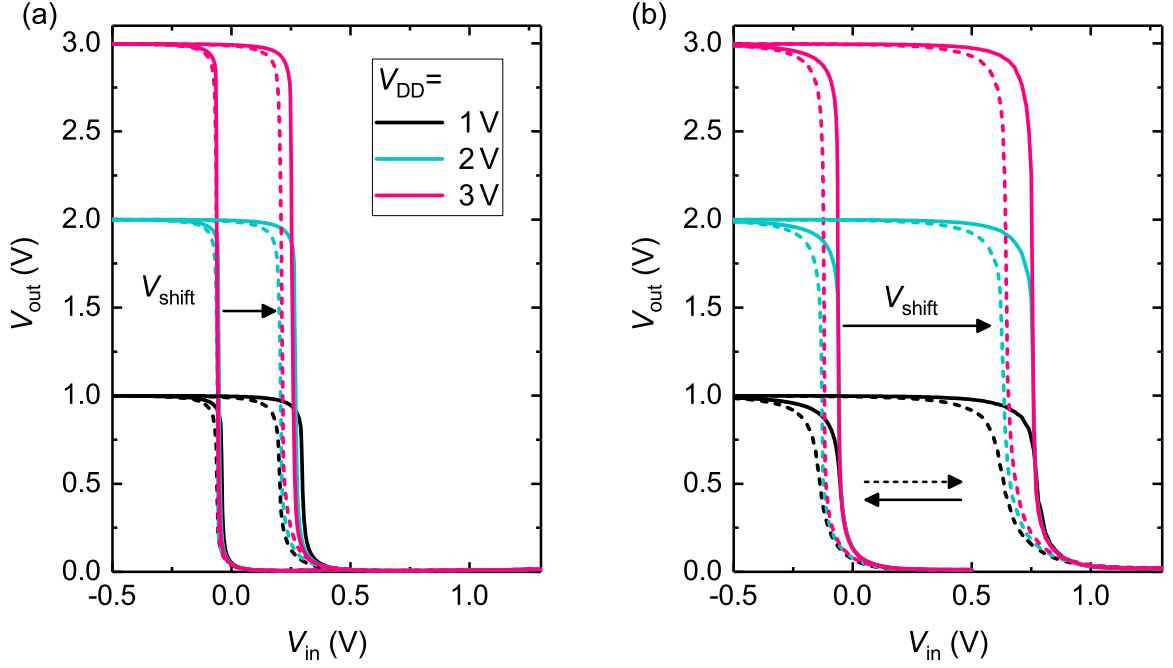
**Figure 5.29:** Gain of an inverter with  $d_{eff} = 10$  nm for both voltage sweep directions. The arithmetic means of the peak gain magnitude for effective channel thicknesses between 8 nm and 14 nm is depicted for a voltage sweep direction from negative to positive voltages (b) and positive to negative voltages (c). The error bars denote the standard deviation.

is largest for  $d_{eff} = 8$  nm, whereas it is negligible for all other effective channel thicknesses. For  $d_{eff} \leq 10$  nm, the uncertainty level is below 0.2 V for all operating voltages. For  $d_{eff} = 14$  nm, values as high as 0.8 V are obtained.

From the small deviations from the mean value of the  $pgm$  and uncertainty level it can be concluded that the devices on each sample are very homogeneous.



**Figure 5.30:** Mean uncertainty level in dependence on the effective channel thickness for operating voltages between 1 V and 3 V for a voltage sweep direction from (a) negative to positive voltages and (b) positive to negative voltages. The error bars denote the standard deviation.



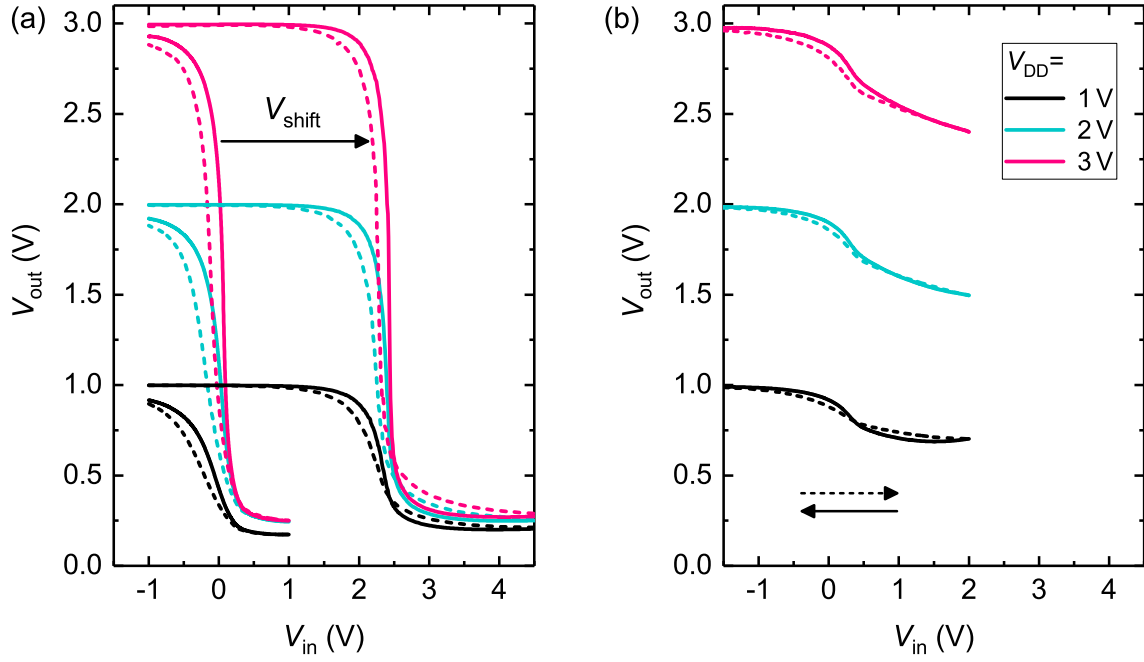
**Figure 5.31:** Voltage transfer characteristics for [! (!)3]SDFL inverters without and with level shifter for an effective channel thickness of (a) 8 nm and (b) 10 nm. Operating voltages between 1 V and 3 V were applied.

### 5.3.3 SDFL Inverter

For Schottky diode FET logic inverters, a drive and a pull-up transistor are requisite. In addition, as described in chapter 2.4, a level shifter is required, which consists of diodes and a pull-down transistor. The [! (!)3]SDFL inverters discussed in this chapter consist of two identical MESFETs with dimensions of  $W = 185 \mu\text{m}$  and  $L = 20 \mu\text{m}$ , which act as drive and pull-up transistor. The pull-down transistor has dimensions of  $W = 52.5 \mu\text{m}$  and  $L = 20 \mu\text{m}$  and the length and width of the rectangular Schottky barrier diodes is  $35 \times 100 \mu\text{m}^2$ . The performance of the [! (!)3]SDFL inverters was investigated in dependence on the effective channel thickness. Hence, samples identical to the thin films described above were used with effective channel thicknesses of 8 nm, 10 nm, 12 nm and 16 nm. The channel thickness for the FETs and Schottky barrier diodes within one sample is identical and was deposited within one sputtering process.

The difference of this inverter layout compared to the simple inverter layout is, as described in chapter 2.4, the additional use of two Schottky diodes and a pull-down transistor, which are connected at the input of the actual inverter. A constant supply voltage of  $V_{SS} = -2 \text{ V}$  is applied at the pull-down transistor. The input signal is either given in such a way that no diode (no level shifter) or two diodes (level shifter) are connected before the actual inverter.

In Figure 5.31 and Figure 5.32, the voltage transfer characteristics for different effective channel thicknesses are depicted without and with level shift for three different operating voltages.



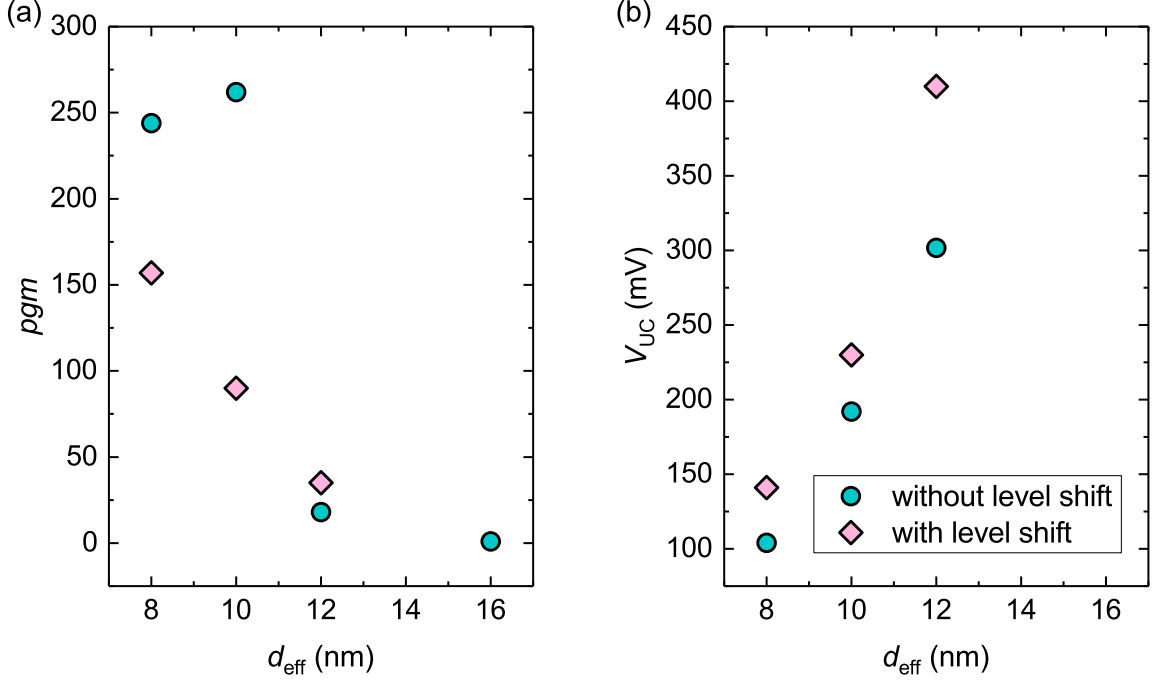
**Figure 5.32:** Voltage transfer characteristics for [! ([!3]SDFL inverters without and with level shifter for an effective channel thickness of (a) 12 nm and (b) 16 nm. Operating voltages between 1 V and 3 V are applied.

The voltage shift over the level shifter is denoted by  $V_{\text{shift}}$ . It increases with increasing effective channel thickness. No voltage inverting behavior was observed for an inverter with  $d_{\text{eff}} = 16$  nm measured with level shifter. The voltage shift is  $V_{\text{shift}} = 0.3$  V ( $d_{\text{eff}} = 8$  nm),  $V_{\text{shift}} = 0.8$  V ( $d_{\text{eff}} = 10$  nm) and  $V_{\text{shift}} = 2.4$  V ( $d_{\text{eff}} = 12$  nm) for an operating voltage of 3 V and a voltage sweep direction from positive to negative voltages.

The increase of the voltage shift with increasing effective channel thickness is due to a higher voltage drop over the level shifter diodes. With increasing effective channel thickness, the drive, pull-up and pull-down transistor are in a progressively higher on-state for gate voltages  $V_{\text{Gate}} \geq 0$  V. This leads to a lower resistance of the pull-down transistor and therewith a higher voltage drop over the level shifting diodes.

The logic swing of the inverters decreases with increasing effective channel thickness, as expected from the results presented for the simple inverters. For an operating voltage of 3 V it decreases from a value of 2.98 V for  $d_{\text{eff}} = 8$  nm to a value of 0.55 V for  $d_{\text{eff}} = 16$  nm. The use of a level shifter does not lead to a change in the logic swing compared to the measurement without level shifter.

Similar to the results for simple inverters in chapter 5.3.2 the peak gain magnitude is highest for  $d_{\text{eff}} = 10$  nm (measured without level shifter). For an operating voltage of 3 V, a maximum value of  $pgm = 262$  is measured. In Figure 5.33 (a), the  $pgm$  is depicted in dependence on the effective channel thickness for  $V_{\text{DD}} = 3$  V. The values for the inverters without and with level shifter are presented there. For  $d_{\text{eff}} \leq 10$  nm, the  $pgm$  is higher for the measurement



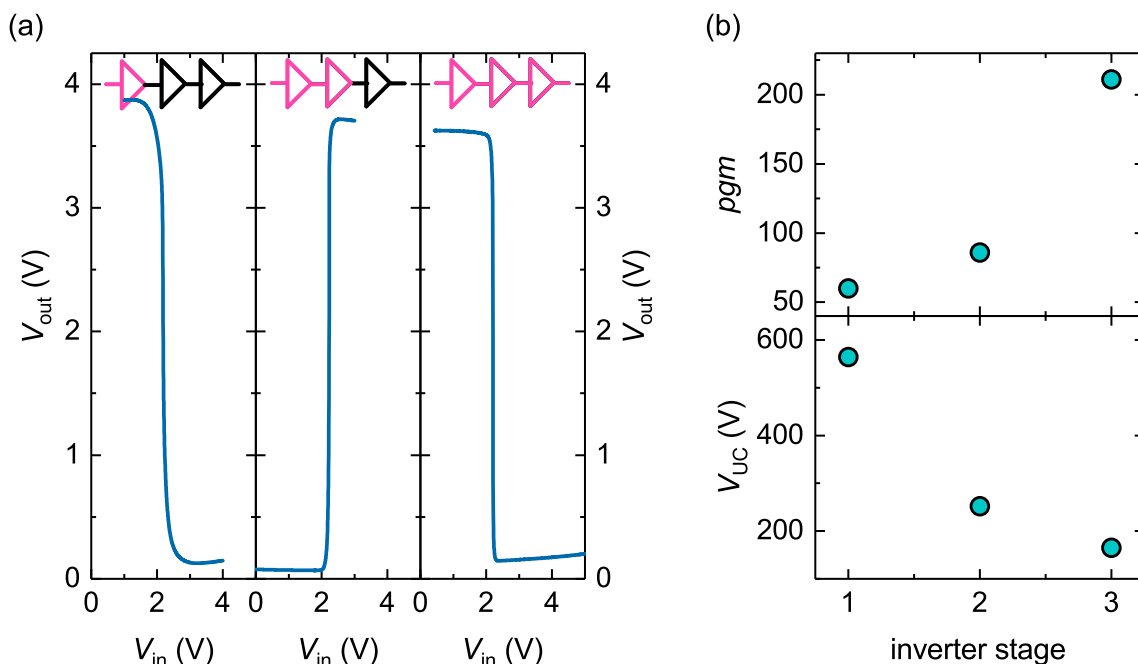
**Figure 5.33:** Peak gain magnitude (a) and uncertainty level (b) for [! ([!])3]SDFL inverters without and with level shifter for an operating voltage of 3 V and a voltage sweep direction from positive to negative voltages.

without level shifter. For  $d_{\text{eff}} = 12$  nm, the  $pgm$  of the inverter without and with level shifter is very similar.

In addition, the uncertainty level for an operating voltage of 3 V is depicted in Figure 5.33 (b). For an effective channel thickness of 16 nm it could not be determined, as the  $pgm$  was 1. An increase of the uncertainty level with increasing effective channel thickness is visible. Moreover, the uncertainty level increases if the measurement is performed with level shifter. A minimum value of  $V_{UC} = 100$  mV is obtained for  $d_{\text{eff}} = 8$  nm without level shift. With level shifter a value of  $V_{UC} = 140$  mV is measured for this effective channel thickness. With increasing effective channel thickness, the difference in the uncertainty level without and with level shifter increases.

### 5.3.4 Inverter Chain

The next step towards achieving a ring oscillator is the series connection of several [! ([!])3]SDFL inverters to obtain an inverter chain. In Figure 5.34 (a), the voltage transfer characteristics for one, two and three inverter stages of an inverter chain are depicted. The effective channel thickness of the thin film is 10 nm. An operating voltage of 5 V was applied. This higher voltage was chosen, as for the measurement of ring oscillators, operating voltages that exceed the voltage shift introduced by the level shifter are required. A more detailed discussion of this is given in the next chapter 5.3.5. The logic swing is below 4 V for all combinations. In



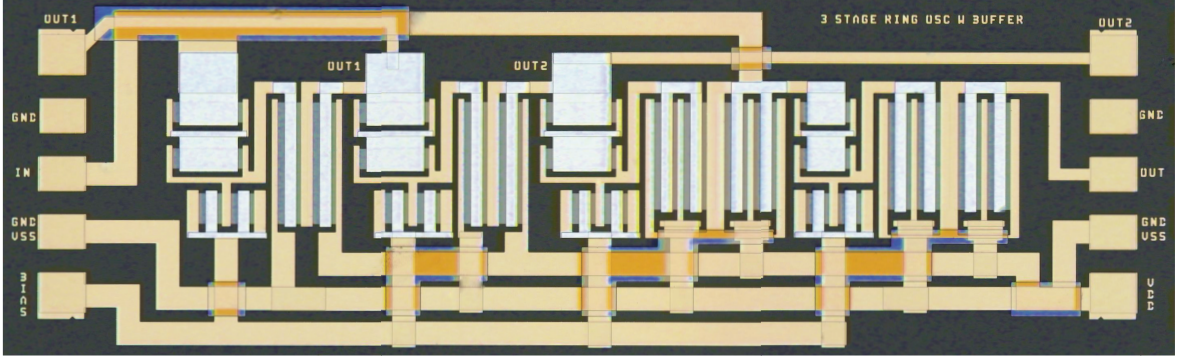
**Figure 5.34:** Voltage transfer characteristic of three stages of an inverter chain (a) and peak gain magnitude and uncertainty level (b) in dependence on the number of inverter stages measured. An operating voltage of 5 V was applied.

the first case, the input signal is applied at the first inverter stage and the output signal is recorded directly behind this stage. The shift of the switching point of the characteristic is due to the level shift before the actual inverter. If the input signal is fed into the first inverter stage, but the output signal is measured after the second inverter stage, an inverse signal with regards to the output voltage is observed. For low input voltages a low output voltage is measured and analogous for high input voltages. In addition, the signal becomes steeper.

If the output signal is read out after the third inverter stage, the voltage transfer characteristic has the same orientation as the original signal after one inverter stage. However, the logic swing has decreased due to voltage drops over the level shifter and non-idealities in the circuit.

The increase of the steepness of the voltage transfer characteristics is also visible in the peak gain magnitude and uncertainty level, which are depicted in Figure 5.34 (b). The peak gain magnitude increases from a value of 60 for one inverter stage to a value of 210 for three inverter stages. Simultaneously, the uncertainty drastically decreases with the increasing number of inverter stages. For one inverter stage, a value of  $V_{UC} \approx 600$  mV is measured, whereas it is as low as  $V_{UC} < 200$  mV for three inverter stages.

This is of great interest for the fabrication of ring oscillators, as it means that the uncertainty level of the individual inverters has to be below a critical value only, but does not have to approach 0 mV, for the ring oscillator to operate. The critical value of the uncertainty level is determined by clearly distinguishable on- and off-states of the inverter.



**Figure 5.35:** Photographic image of a three stage ring oscillator taken by Oliver Lahr.

### 5.3.5 Ring Oscillators

In a last step, three stage ring oscillators were measured for different effective channel thicknesses. As explained in chapter 2.5, a ring oscillator is built by connecting the output signal port of the last inverter stage of an odd number of inverter stages to the input signal port of the first inverter stage. The gate width of the pull-down FET is  $W = 66 \mu\text{m}$ . For the pull-up and drive FET the gate width is  $W = 200 \mu\text{m}$ . The gate length is varied between  $5 \mu\text{m}$  and  $10 \mu\text{m}$ .

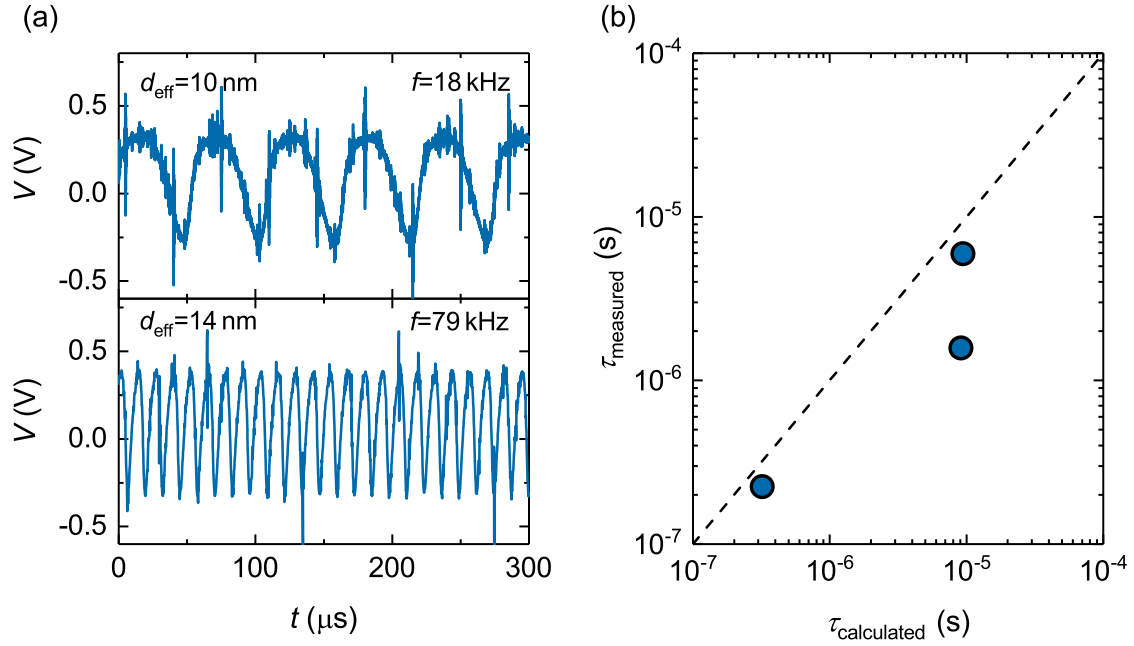
To measure the oscillations, a constant supply voltage of  $V_{\text{SS}} = -2 \text{ V}$  and a ground potential of  $V_{\text{Ground}} = 0 \text{ V}$  are applied. The operating voltage  $V_{\text{DD}}$  is varied during the measurement to record the oscillation frequency for different operating voltages.

In Figure 5.35, a photographic image of a ring oscillator is depicted. It is visible that the last inverter stage as well as the out-coupling inverter have a two-finger gate structure. The two-finger design leads to an increase of the pull-up current of the last inverter stage, as the current supplied by this inverter stage has to charge and discharge two following gate capacitance instead of one. By increasing the number of gate fingers per transistor, the on-current of the transistor can be increased. The same can be achieved by an increase of the  $W/L$ -ratio, however that is more space consumptive and therefore not desired for this layout.

In Figure 5.36 (a), the time evolution of the voltage signal is depicted for an effective channel thickness of  $d_{\text{eff}} = 10 \text{ nm}$  and  $d_{\text{eff}} = 14 \text{ nm}$ . A higher oscillation frequency for a greater value of  $d_{\text{eff}}$  was observed. The gate length is constant at  $10 \mu\text{m}$  for both ring oscillators and an operating voltage of  $9 \text{ V}$  was applied, as explained below. Only effective channel thicknesses of  $10 \text{ nm}$  and  $14 \text{ nm}$  are discussed here, as for all other effective channel thicknesses, the devices are faulty after the lithography process. Most often, wires have become displaced or the connection has been interrupted. This is due to the very small size of the structures in combination with a high number of processing steps required to fabricate a ring oscillator.

The time delay of an inverter stage can be approximated by (see chapter 2.5):

$$\tau_{\text{G}} = \frac{C_{\text{G}} \Delta V F}{I_{\text{PU}}} . \quad (5.4)$$



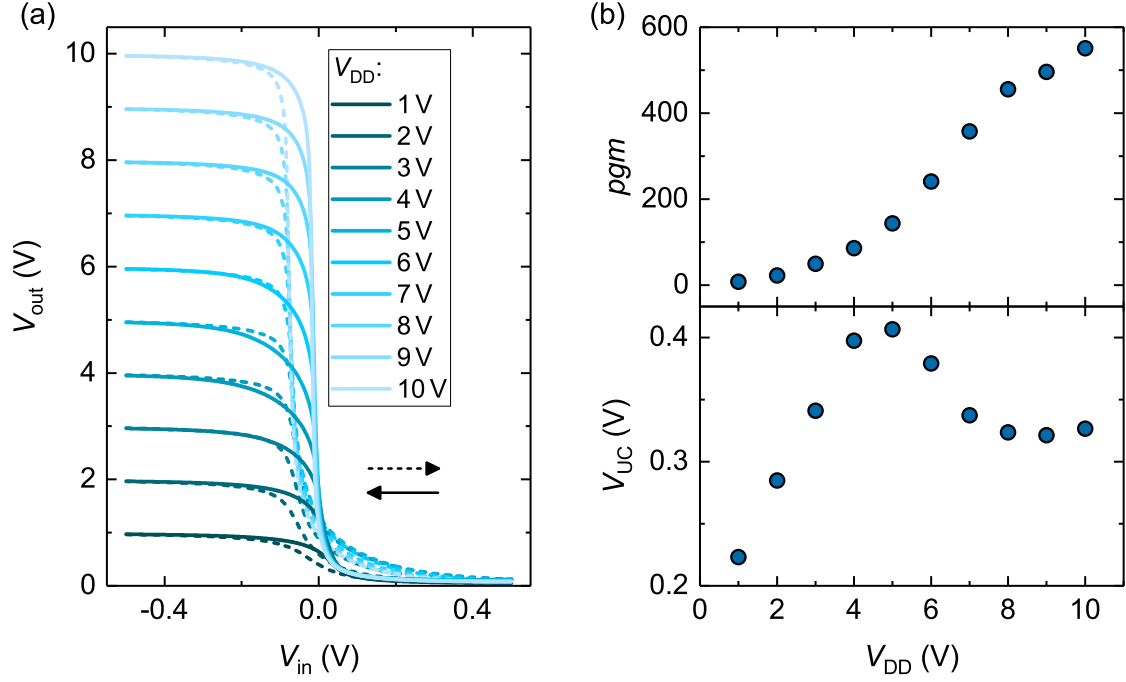
**Figure 5.36:** (a) Time evolution of the voltage signal of two ring oscillators based on thin films of different effective channel thickness  $d_{\text{eff}}$  as labeled. Both devices have a gate length of  $10\ \mu\text{m}$  and their voltage signals were obtained at  $V_{\text{DD}} = 9\ \text{V}$ . (b) The measured time delay is depicted in dependence on the calculated time delay.

The oscillation frequency of an inverter is  $f \propto \tau^{-1}$ . Using equation 5.4, it can be concluded that the time delay of a ring oscillator  $\tau_{\text{G}}$  can be reduced by either an increase of the pull-up current or a reduction of the gate capacitance of the MESFETs.

The higher oscillation frequency of  $f = 79\ \text{kHz}$  for  $d_{\text{eff}} = 14\ \text{nm}$  can be explained by the higher current flowing over the pull-up transistor, which allows a faster charging and discharging of the following gate capacitance. However, a disadvantage of the increase of the effective channel thickness is the increased signal shift by the level shifter due to a higher voltage drop over the level shifter. This leads to a higher power consumption of the device. The power consumption for an  $d_{\text{eff}} = 10\ \text{nm}$  can be approximated by equation 2.37 as  $P_{\text{DD}} \approx 4.5 \times 10^{-6}\ \text{W}$ . In contrast, for  $d_{\text{eff}} = 14\ \text{nm}$  it is as high as  $P_{\text{DD}} \approx 2.7 \times 10^{-5}\ \text{W}$ , each calculated for  $V_{\text{DD}} = 9\ \text{V}$ .

From the oscillation frequency  $f$ , the measured time delay  $\tau_{\text{G}}$  can be calculated. In addition, the theoretical time delay can be calculated using equation 5.4. The measured time delay  $\tau_{\text{measured}}$  is depicted in dependence on the theoretically calculated time delay  $\tau_{\text{calculated}}$  in Figure 5.36 (b). The dashed line is a guide to the eye and illustrates where the measured and calculated values are equal. A good agreement between measured and calculated values is observed.

To verify that the inverters do not degenerate for an applied operating voltage of  $9\ \text{V}$ , measurements on inverters up to a voltage of  $10\ \text{V}$  were performed. The results for an effective channel thickness of  $12\ \text{nm}$  are shown in Figure 5.37. The peak gain magnitude of the inverter

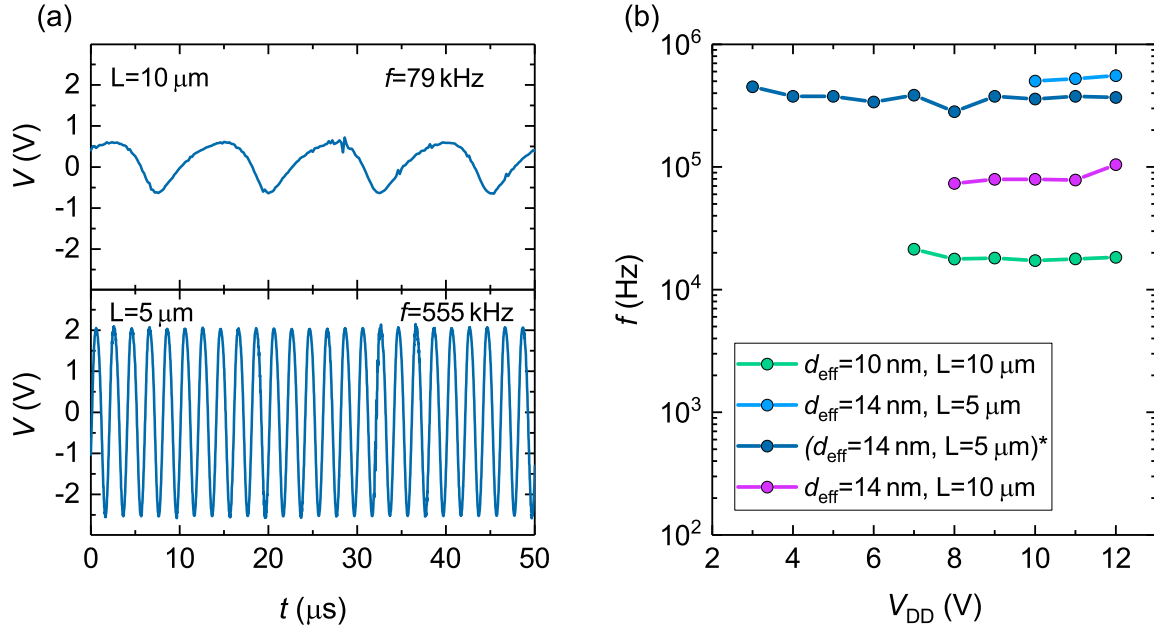


**Figure 5.37:** (a) Voltage transfer characteristics of a simple inverter for both voltage scan directions up to  $V_{DD} = 10$  V and (b) peak gain magnitude and uncertainty level in dependence on the operating voltage. The effective channel thickness is 10 nm.

increases with increasing operating voltage, whereas the uncertainty level remains approximately constant. A maximum value of  $pgm = 550$  was measured for an operating voltage of 10 V.

After an application of  $V_{DD} = 10$  V, the voltage transfer characteristics were again recorded at an operating voltage of 1 V to 3 V and no change to the original measurement was discernible. The devices are therefore stable up to operating voltages of at least 10 V. Further experiments suggest that even operating voltages up to 15 V do not lead to a degeneration of the devices. A second possibility to increase the oscillation frequency of a ring oscillator is by reducing the gate capacitance or i.e. the gate length. As stated before, the effective channel thickness does not influence the gate capacitance. Using equation 5.4, it can be formulated that  $f \propto \tau_G^{-1} \propto I_{PU}/C_G$ . The pull-up current scales with  $L^{-1}$  (compare Figure 5.27 (a)) and as has been formulated before, the gate capacitance is  $C_G \propto WL/w$  (compare Figure 5.27 (b)). Hence, the relation between oscillation frequency and gate length becomes  $f \propto L^{-2}$ . A decrease of the gate length should therefore lead to a strong increase of the oscillation frequency. In Figure 5.38 (a), a comparison of the oscillation for two different gate length at a constant effective channel thickness of 14 nm are depicted. A maximum oscillation frequency of 555 kHz can be measured, which is more than seven times higher than the oscillation frequency of a ring oscillator on the same sample but with a gate length of  $L = 10$   $\mu$ m.

A comparison of the oscillation frequencies for different effective channel thicknesses and gate length is depicted in dependence on the operating voltage in Figure 5.38 (b). The



**Figure 5.38:** (a) Time evolution of the voltage signal of two ring oscillators having  $d_{\text{eff}} = 14 \text{ nm}$  and measured at  $V_{\text{DD}} = 10 \text{ V}$ . (b) Comparison of the oscillation frequency in dependence on the operating voltage for ring oscillators with different gate length and effective channel thickness. The sample with brackets and star is the same as the sample above, but with an improved electrical contact between conducting wire and metallic capping of the gate contact and after an aging of  $\approx 270$  days.

oscillations of the as deposited devices start at operating voltages of  $7 \text{ V}$  to  $10 \text{ V}$ . A general requirement for oscillations to begin is that the supplied operating voltage is larger than the voltage shift introduced by the level shifter. However, the devices presented here exhibit much higher starting values for the oscillations than just the expected voltage shift. For the devices presented here, there exists no additional pad that connects the conducting wire to the platinum capping of the gate contact. A voltage drop is therefore expected at the connection between conducting wire and gate contact capping. Even though, an oscillation frequency of  $555 \text{ kHz}$  was obtained for an effective channel thickness of  $14 \text{ nm}$  and a gate length of  $5 \mu\text{m}$ . This device was remeasured after  $\approx 270$  days and after adding a gold pad, which connects the conducting wire and the metallic capping of the gate contact. With pad the oscillations start at an operating voltage of  $3 \text{ V}$ , which corresponds to the voltage shift introduced by the level shifter. The oscillation frequency has slightly reduced to a value of  $369 \text{ kHz}$ , which is likely due to the aging of the sample.

No dependence of the oscillation frequency on the operating voltage is visible, as is expected for this design [58].

A further increase of this frequency is possible by an increase of the channel thickness or a further decrease of the gate length. A gate length of  $3 \mu\text{m}$  is possible with the mask used in this work, however this is at the resolution limit of the used lithography set-up and the

fabrication of such a ring oscillator did not succeed in the scope of this work.

## 5.4 Comparison to Literature

Numerous publications exist on amorphous [! ([!])3]ZTO based MISFETs. The first was presented in 2005 by Chiang *et al.* [12] and up to now more than 45 publications exist on [! ([!])3]ZTO based MISFETs. In contrast, the first MESFET having a [! ([!])3]ZTO channel was presented in 2017 by Dang *et al.* [14]. The MESFET comprises an  $\text{AgO}_x/\text{Ag}$  gate contact and exhibits drain current on-to-off ratios as high as  $1.1 \times 10^5$  after an annealing of the channel at  $525^\circ\text{C}$ . For [! ([!])3]RT deposited devices, which have seen a maximum temperature of  $90^\circ\text{C}$  during the photolithography, maximum drain current on-to-off ratios of  $5.5 \times 10^4$  and  $9.7 \times 10^6$  were presented for a  $\text{PtO}_x/\text{Pt}$  and  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  gate contact, respectively, in this work. The drain current on-to-off ratio can be further increased by the use of a different MESFET design, i.e. a different  $W/L$ -ratio, as has been published in [E5]. Drain current on-to-off ratios as high as  $1.8 \times 10^6$  have been achieved for  $\text{PtO}_x/\text{Pt}$  gate contacts [E5]. The devices presented in this work achieve lower sub-threshold swings than the MESFET reported in literature [14]. Few descriptions on inverters using [! ([!])3]ZTO as channel layer are reported in literature, and all reported inverters are based on [! ([!])3]ZTO MISFETs [21,32,34-36]. A maximum peak gain magnitude of 23 for  $V_{\text{DD}} = 15\text{ V}$  has been achieved by Tsai *et al.* [36]. All other reported devices have peak gain magnitudes below 20 and uncertainty levels above 1 V. Further, high operating voltages are required due to the voltage drop over the insulator. The devices presented here exhibit  $pgm$  as high as 263 and 385 for operating voltages of 3 V and  $\text{PtO}_x/\text{Pt}$  and  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  gate contact, respectively. Uncertainty levels below 0.4 V have been achieved for both gate contact configurations. These values far exceed the values reported in literature up to now.

Kim *et al.* presented a seven stage ring oscillator in 2011, which is based on a [! ([!])3]ZTO-MISFET [! ([!])3]TFT-ring oscillator design [35]. They report oscillation frequencies as high as 800 kHz at  $V_{\text{DD}} = 60\text{ V}$ . In 2014, [! ([!])3]CMOS five stage ring oscillators based on a [! ([!])3]ZTO MISFET and transistors based on carbon nano-tubes was presented, which reaches oscillation frequencies as high as 714 kHz at  $V_{\text{DD}} = 8\text{ V}$  [113]. However, an annealing of the [! ([!])3]ZTO channel at  $500^\circ\text{C}$  was required for this circuit.

In comparison, the devices presented here exhibit oscillation frequencies as high as 555 kHz at  $V_{\text{DD}} = 10\text{ V}$  for a [! ([!])3]RT deposition and  $90^\circ\text{C}$  being the highest temperature in the fabrication process.

The results presented in this chapter illustrate the high potential of [! ([!])3]ZTO based devices for the use in integrated circuits. With a further tuning of the thin film properties and the geometry of the ring oscillator layout, especially a reduction of the gate length, a further increase of the oscillation frequency can be achieved. The fabrication of ring oscillators with  $\text{PtO}_x/\text{Pt}$  gate contact is also of interest, as the gate capacitance for these contacts was smaller than that of  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  gate contacts.



# Chapter 6

## Summary and Outlook

**Summary** MESFETs and integrated circuits based on amorphous  $\text{In}_{0.5}\text{Zn}_{0.5}\text{ZTO}$  were presented in this work. In a first step, the electrical properties of  $\text{In}_{0.5}\text{Zn}_{0.5}\text{ZTO}$  thin films and the characteristics of Schottky barrier diodes were discussed in dependence on the cation ratio. To achieve a large range of cation ratios within one fabrication step, a  $\text{In}_{0.5}\text{Zn}_{0.5}\text{CCS}$  method for  $\text{In}_{0.5}\text{Zn}_{0.5}\text{PLD}$  was used. All depositions were conducted at room temperature in oxygen atmosphere. An increase of the resistivity and decrease of the free carrier density were found for an increase of the zinc content in the thin films. Subsequently, platinum oxide Schottky barrier diodes were prepared on the pre-characterized thin films. It was shown that the rectification ratio of the Schottky barrier diodes increased from 30 up to  $1.1 \times 10^7$  with increasing zinc content in the samples. However, the largest change of the rectification ratio in dependence on the cation composition was observed for zinc contents below 50%. The effective barrier height increased from 0.71 eV to 1.33 eV with increasing zinc content in the thin films. The change in the ideality factor was less pronounced but an overall tendency to smaller ideality factors was observed with increasing zinc content.

The devices were re-measured after a storage in ambient conditions for 80 – 120 days to investigate the long term stability of the Schottky barrier diodes. It was found that a storage of the samples leads to an increase of the rectification ratio, caused by a decreased leakage current. After the storage, the rectification ratio and ideality factor were very similar for all zinc contents higher than  $\approx 40\%$  in the thin films. Rectification ratios about  $10^7$  and minimal ideality factors below 1.2 were obtained. A hypothesis to explain the improvement over time was that oxygen diffuses from the  $\text{PtO}_x$  contact into the  $\text{In}_{0.5}\text{Zn}_{0.5}\text{ZTO}$ . To further investigate this, a series with different oxygen contents in the plasma during the sputtering of the platinum oxide Schottky contact was performed. Higher oxygen contents in the plasma during the sputtering led to higher rectification ratios and a stronger increase of the rectification ratio over time. The same could be achieved if the  $\text{In}_{0.5}\text{Zn}_{0.5}\text{ZTO}$  sample was treated with an oxygen plasma prior to the platinum oxide deposition. It was speculated that the diffusion of oxygen might be the cause of the vast improvement of diodes for higher oxygen contents in the plasma during the reactive sputtering of platinum and of the improvement over time.

To investigate this, depth resolved  $\text{Pt } 4f$  XPS measurements were performed at the Humboldt Universität Berlin. A comparison of a  $\text{Pt } 4f$ /ZTO sample with metallic platinum and one with platinum oxide was performed. In addition, a sample with platinum oxide contact was stored and then measured after a pre-defined time. A diffusion of oxygen from the semiconductor towards the metal was observed for metallic platinum. This is in accordance with the current-voltage measurements on diodes with metallic platinum as Schottky contact metal, which exhibit an ohmic behavior. A diffusion of oxygen from the semiconductor to the metal leads to an increased number of oxygen vacancies and with that free carriers in the semiconductor. This significantly reduces the depletion region width and enables a tunneling of electrons through the Schottky barrier. For platinum oxide contacts, a diffusion of oxygen from the metal oxide into the semiconductor was observed, which reduces the number of interface near oxygen vacancies and leads to an increase of the depletion region width. This effect is enhanced over time. Comparative current-voltage measurements on diodes demonstrated the improvement of the devices over time. The same effect could be evoked and accelerated by the application of a negative voltage at the Schottky barrier contact.

The results obtained from these studies on  $\text{Pt } 4f$ /ZTO were then used for the fabrication of devices. Sputtering was chosen as deposition method as it has a higher relevance for potential industrial and commercial uses. In a first step, the sputtering conditions for the  $\text{Pt } 4f$ /ZTO channel layer were optimized and a new recipe was developed that allows the reproducible fabrication of FETs. A  $\text{Pt } 4f$ /ZTO layer with vertical oxygen gradient, fabricated under oxygen rich conditions at the beginning and oxygen poor conditions at the end, was deposited prior to the conductive channel. With this additional layer, a depletion of the channel is possible. The cation composition of the thin films was chosen as  $\approx 50\%$  zinc content in the thin films, as this composition was determined as optimal in the previous chapter. Two different contact layouts of the Schottky barrier gate contact were investigated: (i)  $\text{PtO}_x/\text{Pt}$  and (ii) intrinsic  $i$ -ZTO/ $\text{PtO}_x/\text{Pt}$ . A comparison of the two gate contact types yielded that both have advantages and disadvantages. Therefore, both contact types were further investigated.

First, the properties of MESFETs using a  $\text{PtO}_x/\text{Pt}$  gate contact were discussed. A channel thickness variation yielded a monotonous dependence of the drain current on-to-off ratio, sub-threshold swing and threshold voltage on the effective channel thickness. A maximum drain current on-to-off ratio of about four orders of magnitude was obtained for the smallest effective channel thickness. The sub-threshold swing increased with increasing effective channel thickness. Simultaneously, a shift of the threshold voltage from positive to negative values was observed. The same samples were used to fabricate simple inverters and the highest gain (83) and smallest uncertainty level ( $< 300 \text{ mV}$ ) were obtained for an effective channel thickness of  $12 \text{ nm}$ . Using the results from the previous chapter, an investigation of the size of the oxygen reservoir, introduced during the sputtering process of the gate contact, on the properties of MESFETs and simple inverters was performed. A higher drain current on-to-off ratio and stronger improvement over time of the MESFETs was observed for the largest oxygen reser-

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voir. The change in the characteristics could also be elicited by the application of a negative bias, which can therefore be used to accelerate the improvement over time. In contrast, the smallest oxygen reservoir led to a saturation of the improvement over time after 28 days. For larger oxygen reservoirs, no saturation was observed up to 145 days.

The voltage transfer characteristics of the inverters also improved over time, which is mainly due to a shift of the threshold voltage of the MESFETs towards  $\approx 0$  V. Further, the non-ideal, linear increase of the drain current in the saturation regime of the output characteristics of one inverter were tracked over time and a more ideal saturation of the drain current, i.e. a decreasing slope in the saturation regime, over time was observed. This leads to an increase of the peak gain magnitude of the simple inverter to a value of 263. To increase the channel mobility and in the ideal case the switching speed of the MESFETs, a soft thermal annealing was conducted. Annealing temperatures of  $\leq 200^\circ\text{C}$  were chosen, which are compatible with organic substrates [1]. A strong increase of the Hall mobility as well as the channel mobility was measured, however the cut-off frequency did not improve. In contrast, for a thermal annealing at temperatures of  $150^\circ\text{C}$  and higher, a decrease of the cut-off frequency was observed. The origin of this decrease is unknown as of yet. A highest cut-off frequency of 188 kHz was obtained.

In a second step, devices having a  $i\text{-ZTO}/\text{PtO}_x/\text{Pt}$  gate contact were investigated. A channel thickness variation yielded the highest drain current on-to-off ratio of almost seven orders of magnitude for an effective channel thickness of 10 nm. The sub-threshold swing increased with increasing effective channel thickness. For an effective channel thickness of 10 nm, it was demonstrated that the gate geometry, i.e. the ratio between gate width and gate length, strongly influences the characteristic parameters of a MESFET. An increase of the drain current on-to-off ratio was found for the decrease of the gate length at constant gate width. Simple inverters and Schottky diode FET logic inverters were fabricated based on these channels and high peak gain magnitudes above 380 were measured. Using the [! ([!])3]SDFL design a shift of the voltage transfer characteristics could be achieved.

The peak gain magnitude of the inverters exceeds the current state-of-the-art devices based on [! ([!])3]ZTO in literature by more than a factor 10 [36].

An inverter chain, consisting of three [! ([!])3]SDFL inverters with  $i\text{-ZTO}/\text{PtO}-x/\text{Pt}$  gate contact connected in series was demonstrated. Subsequently, ring oscillators with varying channel thickness and gate length were measured. A strong dependence of the oscillation frequency of the ring oscillators on the effective channel thickness was observed. Thicker channels lead to higher frequencies as the pull-up current, required to charge and discharge the gate capacitance of the next inverter stage, increases. A further increase of the oscillation frequency could be achieved by a reduction of the gate length, which increased the pull-up current as well as reduced the gate capacitance. The highest oscillation frequency of 555 kHz was measured for an effective channel thickness of 14 nm and a gate length of 5  $\mu\text{m}$ .

**Outlook** This work demonstrated the high potential of  $\text{In}_2\text{ZnO}_3$  as channel material for FETs in integrated circuits. In addition, the high drain current on-to-off ratios enable the use of  $\text{In}_2\text{ZnO}_3$  based MESFETs as pixel drivers for OLEDs. An increase of the on current, which is required to drive the OLED can be achieved by a soft thermal annealing of the  $\text{In}_2\text{ZnO}_3$  channel. However, the reduction of the switching speed of MESFETs, i.e. the reduction of the cut-off frequency for higher annealing temperatures should be an issue in further investigations. The investigation by capacitance voltage measurements or thermal admittance spectroscopy of these thin films could be of use to understand the physical mechanism leading to the reduction in the switching speed of the MESFETs.

An investigation of  $\text{In}_2\text{ZnO}_3$  based MESFETs on flexible substrates and their stability against tensile and compressive strain has to be investigated for the use in bendable displays. As the gate capacitance of the  $i\text{-ZnO}/\text{PtO}_x/\text{Pt}$  gate contacts is higher than that of the  $\text{PtO}_x/\text{Pt}$  gate contacts, an increase of the oscillation frequency of ring oscillators to achieve frequencies in the MHz range could be achieved by a change of the gate contact material. Here, a reduction of the capacitance leads to higher oscillation frequencies. Also other gate contact materials such as silver oxide or  $p$ -type oxide semiconductors, e.g. zinc cobalt oxide or nickel oxide, have to be further investigated as alternatives to platinum oxide. A further increase of the oscillation frequency could be achieved by a reduction of the gate length, which would require a different lithography set-up than the one used in this work.

# Abbreviations

<b>AFM</b>	atomic force microscope
<b>AOS</b>	amorphous oxide semiconductor
<b>CCS</b>	continuous composition spread
<b>CVD</b>	chemical vapor deposition
<b>CMOS</b>	complementary metal-oxide semiconductor
<b>dc</b>	direct current
<b>EDX</b>	energy dispersive X-ray spectroscopy
<b>FET</b>	field-effect transistor
<b>FL</b>	FET logic
<b>IGZO</b>	indium gallium zinc oxide
<b>ITO</b>	indium tin oxide
<b>JFET</b>	junction field-effect transistor
<b>MESFET</b>	metal-semiconductor field-effect transistor
<b>MISFET</b>	metal-insulator-semiconductor field-effect transistor
<b>MOSFET</b>	metal-oxide-semiconductor field-effect transistor
<b>OPT</b>	oxygen plasma treatment
<b>OLED</b>	organic light emitting diode
<b>PLD</b>	pulsed laser deposition
<b>QSCV</b>	quasi static capacitance voltage
<b>rf</b>	radio frequency
<b>RT</b>	room temperature
<b>SCT</b>	single composition target

**SDFL** Schottky diode FET logic

**TFT** thin film transistor

**UV** ultra violet

**XRD** X-ray diffraction

**XRR** X-ray reflectivity

**XPS** X-ray photoelectron spectroscopy

**ZTO** zinc tin oxide

# List of Symbols

$A_0$	contact area
$A^*$	Richardson constant
$C$	capacitance
$d$	layer/channel thickness
$d_{\text{eff}}$	effective channel thickness
$\eta$	ideality factor
$e$	elementary charge
$\epsilon_r$	relative dielectric constant
$\epsilon_0$	vacuum permittivity
$E_C$	conduction band minimum
$E_F$	Fermi level
$E_{F,m}$	metal Fermi level
$E_{F,s}$	semiconductor Fermi level
$E_{\text{vac}}$	vacuum level
$E_V$	valence band maximum
$F$	fan out
$F_{\text{IF}}$	image force
$f$	frequency
$f_c$	cut-off frequency
$g$	gain
$g_{\text{max}}$	maximal transconductance
$\gamma$	saturation factor of the output characteristics

$h$	Planck constant
$I$	current
$I_C$	charging current
$I_{PU}$	pull-up current
$j$	current density
$j_s$	saturation current density
$k_B$	Boltzmann constant
$L$	gate length
$\lambda$	wavelength
$m_{\text{eff}}$	effective electron mass
$\mu$	mobility
$\mu_{\text{Ch}}$	channel mobility
$n$	free carrier density
$N$	integer number
$N_D$	doping density
$N_t$	net doping density density
$\phi$	electric potential
$\phi_B$	barrier height
$\overline{\phi}_{B,0}$	mean barrier height at $V = 0$ V
$\overline{\phi}_B$	mean barrier height
$\phi_{B,\text{eff}}$	effective barrier height
$\phi_m$	metal work function
$\phi_n$	distance of conduction band to Fermi level
$p_{\text{oxygen}}$	oxygen partial pressure
$p_{\text{argon}}$	argon partial pressure
$P(\phi_B)$	barrier height distribution
$P_{\text{DD}}$	power consumption
$Q$	charge
$r_0$	output resistance

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$\varrho$	carrier density
$\rho$	resistivity
$R_p$	parallel resistance
$R_s$	series resistance
$\sigma$	standard deviation of the barrier height distribution
$S$	sub-threshold swing
$t$	time
$\tau_G$	gate delay
$T$	temperature
$V$	voltage
$V_{bi}$	built-in potential/voltage
$V_{DD}$	operating voltage
$V_{Drain}$ and $I_{Drain}$	drain voltage and drain current
$V_{Gate}$ and $I_{Gate}$	gate voltage and gate current
$V_{Ground}$	ground voltage
$V_{in}$	input voltage
$V_{IH}$ and $V_{OH}$	input high and output high voltage
$V_{IL}$ and $V_{OL}$	input low and output low voltage
$V_{out}$	output voltage
$V_P$ and $I_P$	pinch-off voltage and pinch-off current
$V_{shift}$	voltage shift
$V_{Source}$	source voltage
$V_{Th}$	threshold voltage
$V_{UC}$	uncertainty level
$w$	depletion region width
$W$	gate width
$\mathcal{X}$	electron affinity



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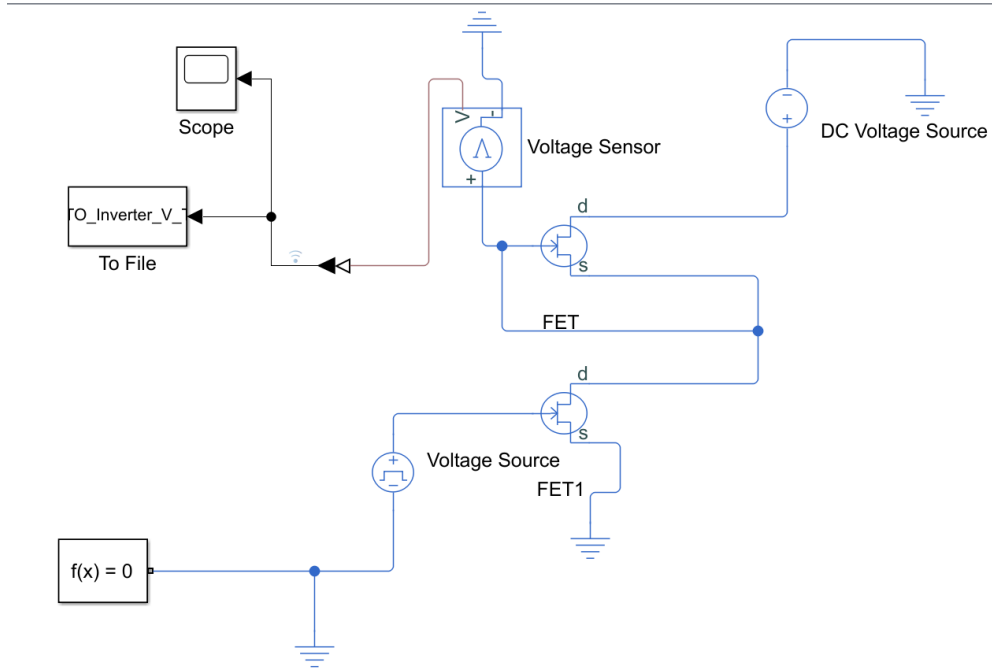
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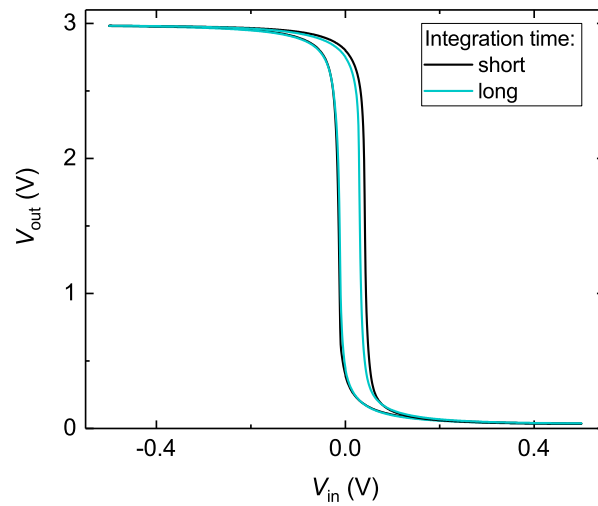


# Appendix

## Appendix - Additional Figures



**Figure A1:** Equivalent circuit of a simple inverter designed with *Simulink* (*MATLAB*) used for the simulation of voltage transfer characteristics. Two identical JFETs with tunable electrical properties were used for the simulation.



**Figure A2:** Voltage transfer characteristics of an inverter with  $\text{PtO}_x/\text{Pt}$  gate contact and an effective thickness of 12 nm for an operating voltage of 3 V. Short integration time is 0.64 ms and long integration time 320 ms. A decrease of the hysteresis with longer integration time is visible.

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"Realization and Optimization of Metal-Semiconductor Field-Effect Transistors and  
Integrated Circuits based on Amorphous Zinc Tin Oxide"

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