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Design of a Low Offset, Low Noise Amplifier for Neural Recording Applications

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The design of a capacitive feedback based neural recording amplifier is presented. The prime design requirements in case of neural amplifiers includes low noise, high gain, high CMRR, low power, low area and low offset voltage. However, there is an inherent trade-off between noise-power and area-offset in the design process which needs to be addressed. A Recycling Folded Cascode based Operational Transconductance Amplifier (RFC-OTA) topology is employed to realize the amplifier as it offers better gain and offset voltage as compared to other topologies. The sizing of the transistors has been done with the primary objective of low random offset voltage while meeting other design criteria within the specified range subject to all inherent trade-offs. Simulations have been done in Cadence Virtuoso using SCL 180 nm technology and comparative analysis with other reported designs reveals that the proposed RFC-OTA based neural amplifier design achieves a low random offset voltage of 1.4 mV with a low input noise of 1.38 µV as compared to most of the reported design.

Keywords: Neural Amplifier, Recycling Folded Cascode, Low Random Offset Voltage, High Gain, Area-Offset trade-off, Capacitive Feedback

Introduction

Neural Amplifiers are high gain bio-potential amplifiers used for amplifying weak neural signals.[1,2] Being battery-operated and implantable, low area and low power are major design requirements.[3] Furthermore, to minimize noise due to both electronics and external sources, a very low input noise and high CMRR is desirable.[1–5] However, an inherent trade-off exists between low noise and low power.[4] Apart from these, the need of low offset voltage is also desired as it impacts the accuracy and precision.[6] Random offset voltage arises due to random mismatch in device parameters[7] and can be improved at the cost of higher area.

Numerous works have been reported in design of neural recording amplifiers. However, most of the reported works[2–4,8–12] fail to meet the low noise and low power criteria along with high gain because of the various trade-off between design specifications. They also do not take into account the need of a low offset voltage. The proposed work aims at designing a neural recording amplifier to overcome such limitations by determining optimal sizing of MOS transistors for minimum random offset voltage subject to all design specifications as constraints using swarm intelligence based meta-heuristic algorithms[13] due to their easy search mechanism and ability to find global optimum, which is a major contribution of the proposed work. To realize the amplifier, a RFC OTA is employed as it offers better gain, offset voltage, input noise[14] in comparison to a basic folded cascode. Simulations, investigation of temperature variation and comparative analysis with state of art design reveals significant improvement in input noise and random offset voltage with a value of 1.38 µV and 1.452 mV respectively.

Proposed Neural Amplifier design

The proposed design consists of a capacitive feedback neural recording amplifier comprising of an input dc blocking capacitor, C_{in} and feedback capacitor, C_f which mainly control the mid-band gain as defined by ($-C_{in}/C_f$) as shown in Fig. 1. There are two diode connected pseudo resistors, M_{b1} and M_{b2} in the feedback network which together with the capacitors, defines the transfer function of the system, *H(s)* as given by Eq. (1).

$$H(s) = \frac{v_{out}(s)}{v_{in}(s)} = -\frac{C_{in}}{C_f} \cdot \frac{sR_P C_L}{1+sR_P C_L} \quad \ldots (1)$$

Where C_L is the load capacitance and R_p realizes the contribution of C_L, M_{b1} and M_{b2}.

A capacitive feedback amplifier is preferred over an open loop one as it offers lower input noise and can also be easily reproduced without large tuning.[11] The OTA stage (G_m) which controls the gain is realized using a RFC OTA as shown in Fig. 1. It is an improved

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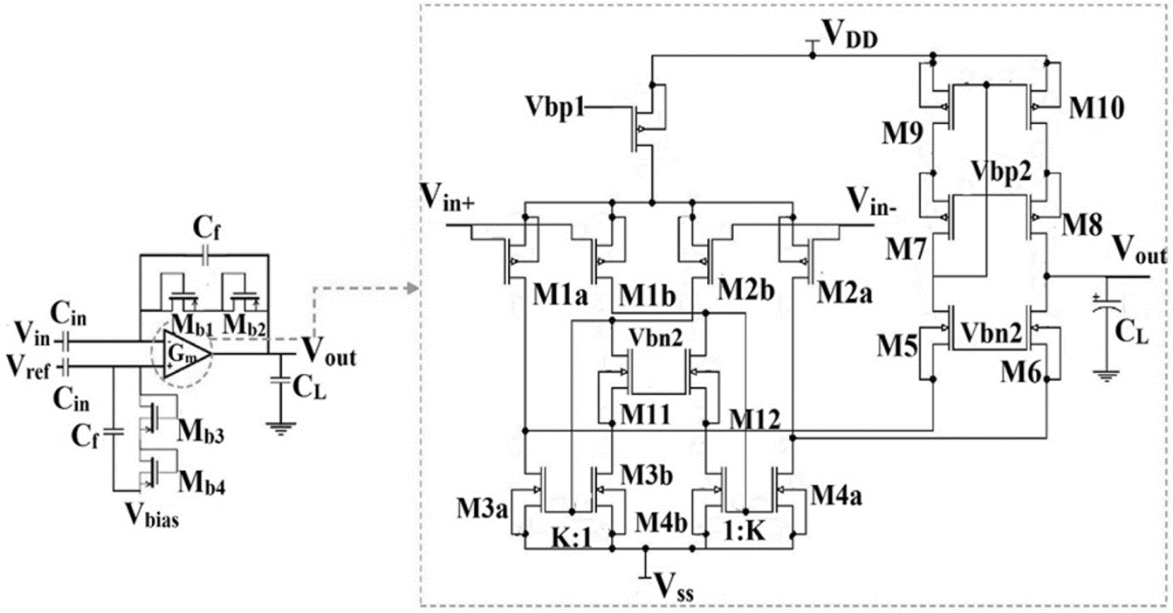

Fig. 1 — Proposed Neural Amplifier along with Recycling Folded Cascode OTA used to realize the G_m block

variant of conventional folded cascode OTA and offers large improvement in gain, input noise, offset voltage etc. under same power and area budget.[14] It is achieved by reusing the idle currents and devices. As seen from Fig. 1, the input differential pair M1 and M2 is split in the ratio of half each in M1a, M1b, M2a and M2b, while the current sinks M3 and M4 are split in the ratio of K:1 where K is the recycling factor. M7 to M10 represents the cascode current mirror load. Furthermore, to improve the systematic offset voltage, two new transistors M11 and M12 are incorporated in the design which maintains the drain potentials for better matching.[14] The modelling of the proposed amplifier is performed and the small signal gain (A_v) and input referred thermal noise spectral density ($S_n(f)$) is given by Eq. (2) and Eq. (3) respectively.

$$A_v = g_{m1a}(1+K)g_{m6}r_{06}(r_{02a}||r_{04a})||g_{m6}r_{08}r_{010} \quad \ldots (2)$$

$$S_n(f) = \frac{16KT}{3g_{m1a}}\left[\frac{(1+K^2)}{(1+K)} + \frac{g_{m3a}}{g_{m1a}} + \frac{g_{m9}}{(1+K)g_{m1a}}\right] \quad \ldots (3)$$

Where g_{mx} is the transconductance of transistor Mx and r_{ox} is the output resistance of transistor Mx.

The mismatch analysis is further performed and the contribution of the various drain current mismatches of the transistors at the output is divided by the input transconductance to achieve the random offset voltage ($V_{OS,RFC}$) of the proposed RFC-OTA as shown in Eq. (4).

$$V_{OS,\ RFC} = 2\frac{A_{VTH,P}^2}{W_{1a}L_{1a}(1+K)}\left[\frac{(1+K)^2}{1+K} + \frac{3\mu_N A_{VTH,N}^2}{\mu_P A_{VTH,P}^2}\left(\frac{L_{1a}}{L_{3a}}\right)^2 + \frac{2}{(1+K)}\left(\frac{L_{1a}}{L_9}\right)^2\right] \quad \ldots (4)$$

Where $A_{VTH,P}$ and $A_{VTH,N}$ are constants for area matching for PMOS and NMOS respectively.

The sizing of the MOS transistors and the values of other design parameters have been determined by formulating the random offset voltage shown in Eq. (4) as an objective function and using the modelling of other design parameters such as gain and input noise defined by Eq. (2) and Eq. (3) respectively, other specifications such as CMRR, power dissipation, slew rate and also area defined by $\sum_{k=0}^{12} W_k L_k$ as design constraints and solving the objective function for minimum random offset voltage using swarm intelligence based algorithms[13] due to the reasons mentioned previously. The use of such meta-heuristics has also become prominent due to existence of trade-offs among the various design specifications which makes the manual sizing of the transistors a computationally inefficient approach. One such example of trade-off would be the opposite dependency of $S_n(f)$ and V_{OS} on L_9 as seen from Eq. (3) and Eq. (4) respectively. Thus, to minimize both $S_n(f)$ and V_{OS}, an optimum L_9 has to be determined, which becomes difficult to be addressed manually without compromising on one of them and thus to achieve

optimum values of both these design specifications the use of meta-heuristics comes into play. The algorithm used to optimize the random offset voltage here is an improved hybrid swarm intelligence-based algorithm namely the Hybrid Whale Particle Swarm Optimization (HWPSO).[13] It is basically a hybrid variant of two popular swarm intelligence algorithms namely the Whale Optimization Algorithm (WOA) and the Particle Swarm Optimization (PSO). The flowchart of the approach is shown in Fig. 2. The design parameters obtained are shown in Table 1. For the input and feedback capacitors MIM capacitors are

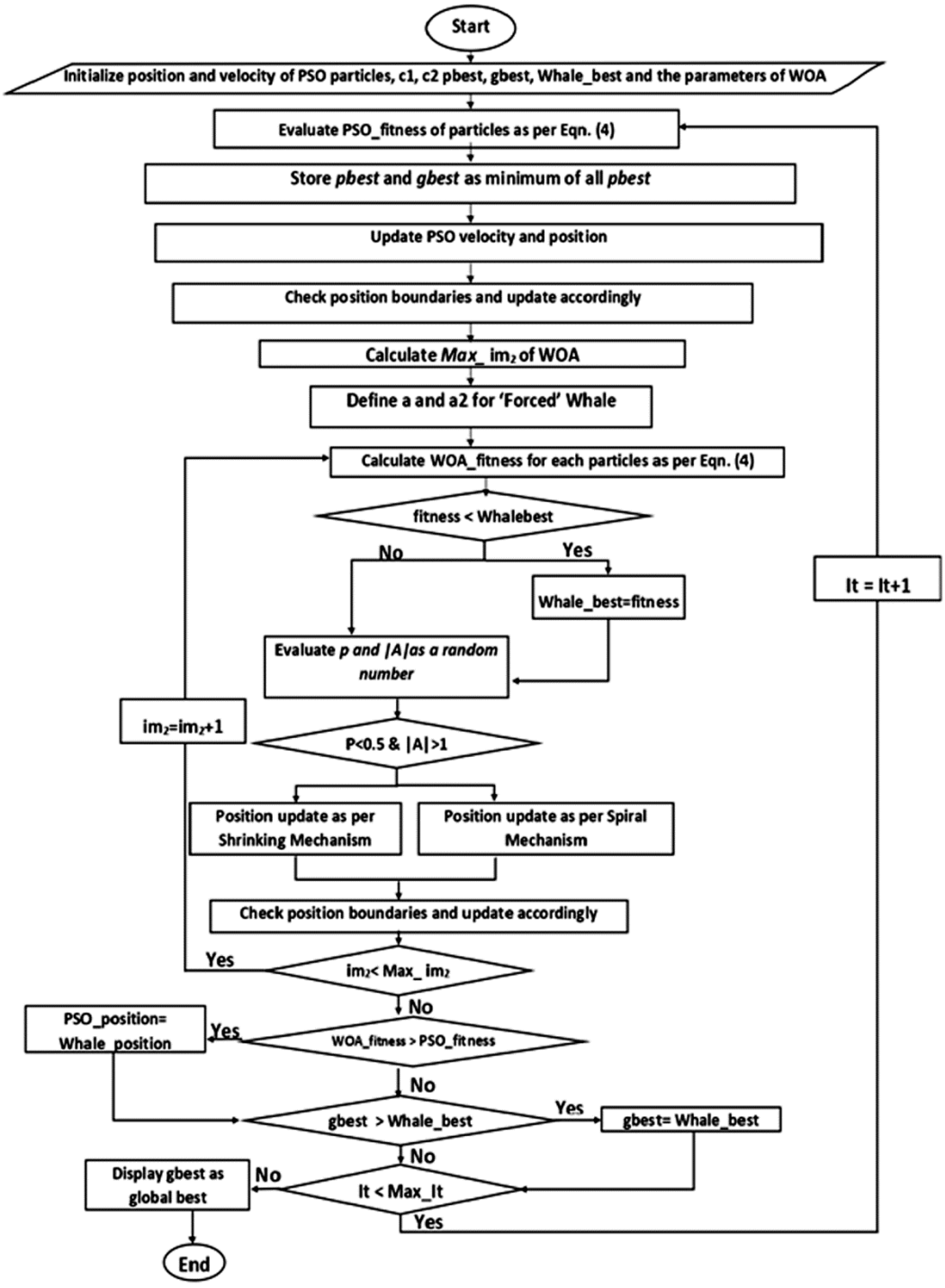

Fig. 2 — Flowchart of HWPSO algorithm for optimizing random offset voltage

used as they have higher density and lower parasitic effects.[11] The mid-band gain of the neural amplifier is mainly controlled using the C_{in} and C_f ratio and has to meet the desired specification also as it is lower than the dc gain of the OTA defined by Eq. (2). Thus, to maximize the mid-band gain, the C_{in} has to be higher while C_f has to be lower. However, the size of the capacitors also impacts the area of the amplifier which also needs to be lower. Additionally, there is also a limit imposed on the value of the capacitors as imposed by the technology bound constraints. So, keeping in view all these trade-offs, the values of the MIM capacitors have been optimized as shown in Table 1.

Table 1 — Optimaldesign parameters of proposed neural amplifier used

Design Parameter	Values
I_{bias} (µA)	2
W_{1a}/L_1	30/30
W_{1b}/L_1	30/30
W_{2b}/L_2	30/30
W_{2b}/L_2	30/30
W_{3a}/L_3	21/21
W_{3b}/L_3	7/21
W_{4a}/L_4	21/21
W_{4b}/L_4	7/21
W_5/L_5	28/28
$W6/L_6$	28/28
W_7/L_7	50/40.49
W_8/L_8	50/40.49
W_9/L_9	50/40.49
W_{10}/L_{10}	50/40.49
W_{11}/L_{11}	14/14
W_{12}/L_{12}	14/14
W_0/L_0	40/40
C_{in} (pF)	12
C_f (fF)	100

Simulation Results and Analysis

The performance of the proposed design is validated by designing a capacitive feedback neural amplifier in Cadence Virtuoso using SCL 180 nm technology. Simulations have been performed and comparison with other reported designs are done. The results are illustrated in Table 2 and Fig. 3 and Fig. 4. The AC analysis for gain plot of the proposed RFC-OTA based neural amplifier is shown in Fig. 3 from where it is seen that the mid-band gain of the proposed neural amplifier is found to be 50.5 dB with an input capacitor of 12 pF and feedback capacitor of 100 fF which rolls of at -20 dB/decade. The OTA open loop gain is equal to approximately 70 dB contributed mainly by the M1a, M6 and M8 in accordance to Eq. (2). The use of feedback capacitors decreases the open loop gain to 50 dB as per ratio governed by Eq. (1). The input referred noise of the

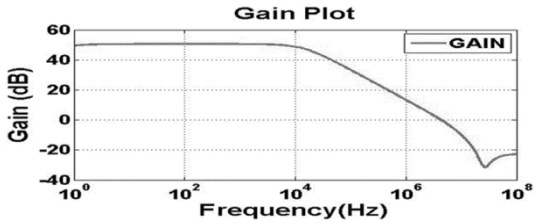

Fig. 3 — AC analysis plot for mid-band gain of proposed neural amplifier

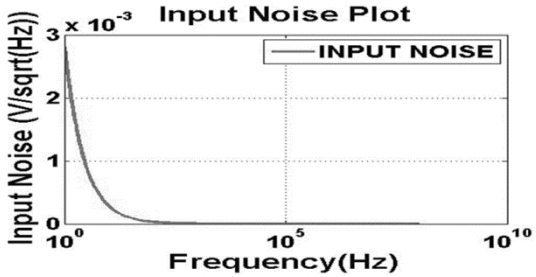

Fig. 4 — Noise analysis plot for input noise of proposed neural amplifier

Table 2 — Comparative analysis between proposed design and other reported works

Work	Technology (µm)	Gain (dB)	CMRR (dB)	Power dissipation (µW)	Input Noise (µV)	Bandwidth (KHz)	Random Offset Voltage (mV)
Wattanipanitch *et al.*[3]	0.5	40.85	66	*NR	3.06	5.3	*NR
Chaturvedi *et al.*[4]	0.13	37	*NR	1.5	5.5	7	*NR
Amaya *et al.*[2]	0.13	46	85	1.92	3.8	7.3	*NR
Feng *et al.*[8]	0.5	58.4	154.4	*NR	21.06	10.2	*NR
Ng *et al.*[9]	0.065	52.1	>80	3.28	4.13	8.2	*NR
Kim *et al.*[10]	0.18	54.5	*NR	62.5**	10.2**	5.8	*NR
Laskar *et al.*[11]	0.18	61.52	104.52	3.345	3.3	13.4	7.2
Proposed Neural Amplifier	0.18	50.5	124.07	4.68	1.38	13.1	1.452

*NR= Not Reported; **including the ADC

proposed design is illustrated in Fig. 4, which is very low and equal to 1.38 µV. As seen from Fig. 4, the flicker noise is dominant at lower frequency ranges and it decreases as the frequency increase. The flat frequency response following the corner frequency indicates that thermal noise is dominant which is mostly contributed by M1a, M3 and M9 as indicated by Eq. (3). Table 2 further indicates that the proposed design reports a lower input referred noise as compared to the other reported designs. The use of RFC-OTA architecture plays a significant role in this as none of the reported designs mentioned has utilized it to realize a neural amplifier. The sizing of the MOS transistors was further done by formulating the input noise as a design constraint for low random offset which also resulted in such a low value. This is evident from Eq. (4) which shows that to achieve a low random offset voltage, a lower g_{m1a} is required which also results in a low input noise as shown in Eq. (3). To achieve the random offset voltage, Monte Carlo analysis is performed and the standard deviation of the sample values is noted for a variation in process parameters which is found to be equal to 1.452 mV. This is better than the high swing cascode current mirror load based folded cascode OTA used to realize a neural amplifier as reported by Laskar *et al*.[11] indicated by Table 2. However, a small increase in power dissipation is reported as compared to other designs. This is due to the inherent noise-power trade-off and higher I_{bias} required for minimum design specifications to be met.

In order to test the robustness and reliability of the amplifier's performance, the Monte Carlo analysis is performed for a variation in temperature from room temperature i.e. 27°C to 60°C, by considering a sample size of 50 each. The results are shown in Table 3 and Fig. 5, from which it is evident that value of mean gain as well as mean input noise is very low with a value of around 50.4 dB and 1.38µV respectively with a very low standard deviation of around 600 mdB and 16.42 fV for a wide variation of temperature from 27°C to 60°C.

Table 3 — Performance of the proposed design for variation in temperature

Parameter	27ºC		40ºC		60ºC	
	Mean	SD	Mean	SD	Mean	SD
Gain (dB)	50.48	642m	50.45	339m	50.42	109.4m
Input Referred Noise (V)	1.384µ	16.24f	1.384µ	16.24f	1.384µ	16.24f

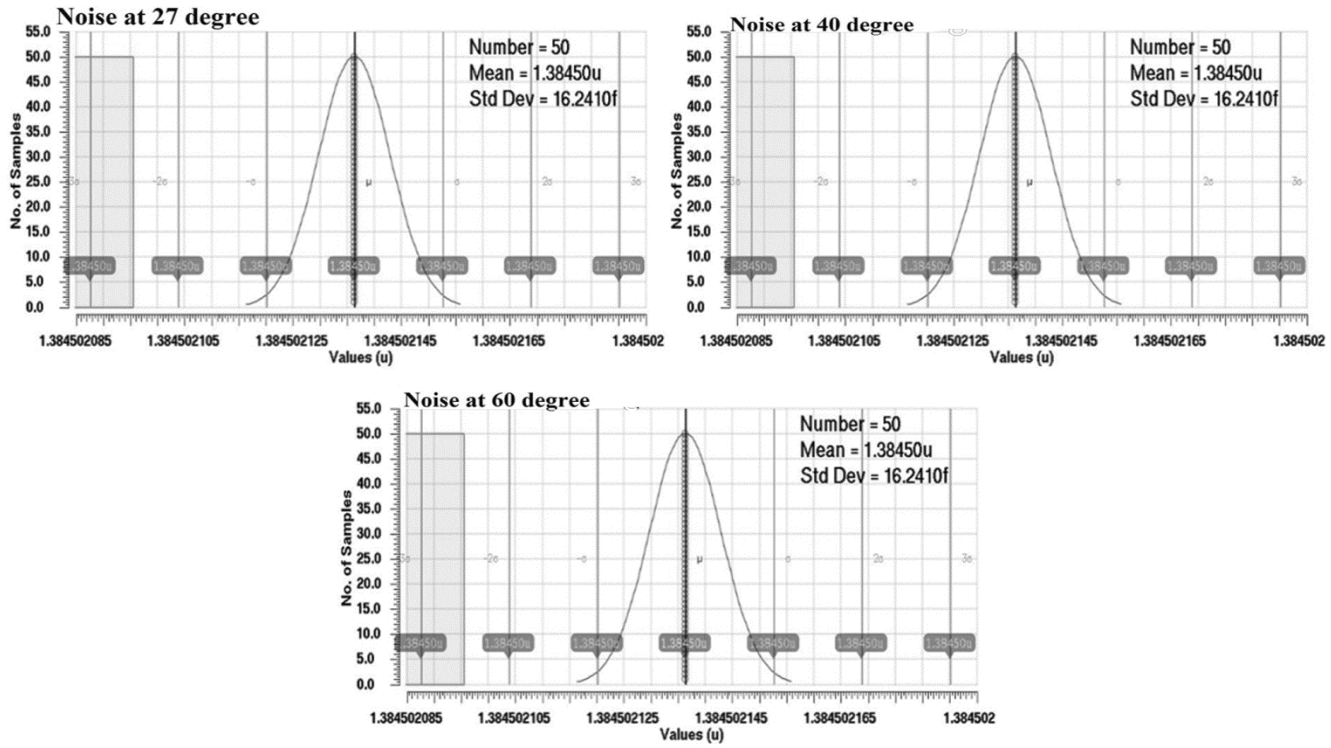

Fig. 5 — Monte Carlo Analysis of Input Noise for variation in temperature from 27°C to 60°C

Conclusions

A low random offset, low noise neural amplifier design using capacitive feedback topology is reported. The proposed design utilizes the RFC-OTA to realize the amplifier. The modelling of the amplifier is done and the sizing of MOS transistors are performed considering a low random offset voltage as the design objective and all other design specifications such as gain, noise, power, CMRR, bandwidth, slew rate as design constraints which are to be met within the desired range. Simulations, Monte Carlo analysis for temperature variation have been performed and comparison with other reported designs illustrated a significant improvement in input noise and random offset voltage with a low standard deviation, while all other design specifications are within the required ranges for use in neural recording systems. The proposed design can be extended to include a programmable gain amplifier and ADC to design a complete neural recording system, which is a future enhancement to the proposed work.

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