A Logic Gate Model based on Neuronal Molecular Communication Engineering

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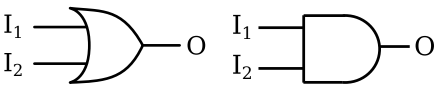
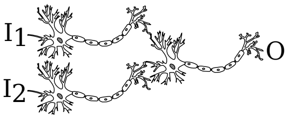
***Abstract*—The field of Neuroengineering aims to investigate ways to proposed synthetic and controllable Boolean computing inside the brain using neuronal cells based on the existing neuronal computation abilities of the Brain. In this work, we propose the design of AND and OR logic gates using a multicellular Boolean logic operation by engineering the molecular communications of neurons and we evaluate their performance when passing data along as isolated units. The results show higher accuracy values of gate operation for mid-level inter-spike intervals when stimulated with spike trains revealing the role of the frequency of firing and how this impacts on neuronal logic gating.**

***Index Terms*—molecular communication, neuronal network, logic gates, Boolean algebra**



(a) OR gate. (b) AND gate.



(c) Neuronal logic gate.

Logic Gates

I_1	I_2	OR	AND
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

(d) Truth table.

Fig. 1. Logic gates and their truth tables.

I. INTRODUCTION

Recent studies have investigated the computation abilities of the brain following findings that its internal structure might be composed of reliable Boolean building blocks similar to the ones found at the core of today's transistors [1]. A question remains as to how synthetic and controllable engineering of neuronal logic gates can impact on future precision medicine technologies for neurodegenerative diseases.

Neuronal cells send and receive information through the firing of action potentials (AP), i.e. spikes, and depending on the task that is being performed by the brain, a neuron can speed up or slow down its firing rate. This exchange of information through electrochemical signalling between neurons is known as neuro-spike communication and is one of the models of molecular communication proposed in the literature [2]. In this work, we propose the design of logic gates using a multicellular Boolean logic operation by engineering the molecular communications of neurons, based on the neuro-spike signal propagation.

Our objective is to present an analysis from the perspective of molecular communications on the logical Boolean operations of neuronal cells by controlling information processing at a tissue level, for potential reconfiguration of neural circuits or the development of non-surgical neural interfaces, in relation to stimulation frequencies of the input neurons, as illustrated in Fig. 1. The variations in the frequency of stimulation may represent interference in the neuro-spike propagation that could cause loss of information. The performance of the gates is measured in terms of accuracy between the expected output, given with known inputs, and the actual output.

II. NEURONAL DIGITAL LOGIC GATES

The neuron spiking threshold value not only controls the firing rate of a neuron but also plays a role in how it processes information. A neuron follows the *all-or-none* principle to fire a spike. Stereotypically, an AP is initiated only when the membrane potential, $V(\cdot)$, in the cell reaches a certain level, i.e. threshold, th. According to Platkiewicz and Brette [3], the threshold in brain cells depends on several parameters such as stimulus (x), type of cells (α), synaptic conductances ($gSyn$) and properties of ionic channels (E). We use this phenomenon of the neurons to design logic gates and it is defined as

$$AP = \begin{cases} 1, & \text{if } V(x, \alpha, gSyn, E) > th \quad (1) \\ 0, & \text{otherwise} \quad (2) \end{cases}$$

In order to build a single logic gate, three neurons are used, two of them operating as the inputs and the other one as the output, and the synaptic connections between them are made with regards to their respective connection

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probabilities. The stimulation may be due to spikes from other neighbouring neurons or can be artificially stimulated using miniature implantables *Wireless Optogenetics Nanonetwork Devices (WiOptND)* [4].

In this work, we use a simple OOK modulation, where a spike is considered as a bit "1" and its absence as a bit "0" in a time slot with τ ms. Both inputs, I_1 and I_2, are stimulated with spike trains with different inter-spike intervals (ISI). The models of neurons were kept in their default configuration except for the threshold for spike initiation that was set to a very low value of -60 mV for both gate types.

For this paper, we present the design of two logic gate types, an OR and an AND gate. Five OR and three AND gates were built for this study with different types of cells but all of them follow the structure/connection depicted in Fig. 1(c) and their behaviour is described by their respective truth tables as shown in Fig. 1(d).

By knowing the type of the gate and the two input spike trains, it is possible to obtain the expected output, $E[Y]$, and then calculate the accuracy of the gate by comparing $E[Y]$ with the actual output, Y. The accuracy, $A(E[Y];Y)$, is then defined as the ratio of correct classifications to the total number of samples classified, thus

$$A(E[Y];Y) = \frac{P_{1,1} + P_{0,0}}{P_{0,0} + P_{0,1} + P_{1,0} + P_{1,1}}, \qquad (3)$$

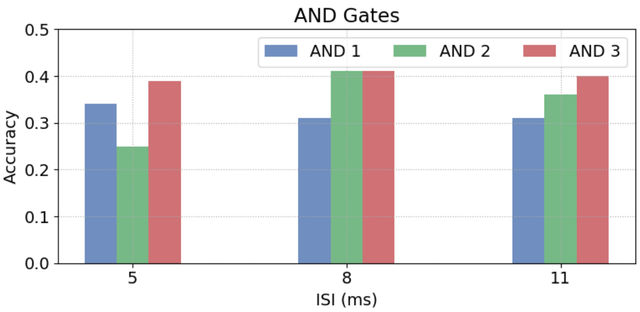
where $P_{Y,E[Y]}$ is the probability of Y given $E[Y]$, where $Y \& E[Y] \in \{0,1\}$.

III. RESULTS AND DISCUSSION

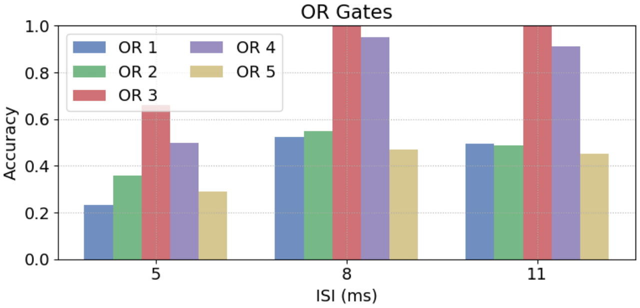
In this section, the simulations performed with the models of neurons downloaded from the *Digital Reconstruction of Neocortical Microcircuitry* [5] using the *NEURON Simulator* [6] are presented. The models are arranged as isolated cells connected to each other as shown in Fig. 1(c) and do not represent activities as part of a larger network. The type of cells include *Descending Axon (DAC)*, *Horizontal Axon (HAC)*, *Small Axon (SAC)*, *Martinotti (MC)*, *Bitufted (BTC)*, *Double Bouquet (DBC)*, *Bipolar (BP)*, *Large Basket (LBC)*, *Nest Basket (NBC)* and *Small Basket (SBC)*.

In Fig. 2(a), it is possible to verify that different ISI's do not represent drastic changes in the accuracy of the AND gate, where the average accuracy is around 0.353. On the other hand for the gate OR (Fig. 2(b)), we observe an increase of the accuracy with the ISI between $5 - 11$ ms from 0.232 to 1.

In general, Fig. 2 shows that for all gates, an ISI of 8 ms returns the highest values of accuracy and that the higher the frequency of firing, the worse the performance of the gates will be. At the same time, higher ISI's can decrease the accuracy considering that to evoke a spike in the output, the potential summation should increase towards the threshold in a faster pace than the rate with which the cell goes back to its resting potential. We highlight this importance to consider that changes in the parameters of the models may lead to a change of the gate's accuracy.



(a) Accuracy for AND gates.



(b) Accuracy for OR gates.

Fig. 2. Accuracy for the AND and OR gates with different ISI's. AND gates: (1) MC, NBC and HAC, (2) SBC, MC and SBC, (3) MC, MC and DAC. OR gates: (1) DAC, SAC and LBC, (2) DBC, BTC and BP, (3) DAC, HAC and MC, (4) MC, NBC and DAC, (5) DBC, DBC and BP.

IV. CONCLUSIONS

In this paper, we designed OR and AND logic gates using the engineering of neuronal molecular communication systems. Our results show how the frequency of firing affects the accuracy of the neuronal digital logic gates, where a mid-level ISI demonstrates to be the most appropriate for high accuracy. For future work, we intend to conduct analysis on logic circuits composed by several gates with a generalised approach to fine-tune the system constructed within a cellular tissue .

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