AIP Journal of Applied Physics

Advanced performance and scalability of Si nanowire field-effect transistors analyzed using noise spectroscopy and gamma radiation techniques

J. Li, S. A. Vitusevich, M. V. Petrychuk, S. Pud, A. Offenhäusser, and B. A. Danilchenko

Citation: Journal of Applied Physics **114**, 203704 (2013); doi: 10.1063/1.4833567
View online: http://dx.doi.org/10.1063/1.4833567
View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/114/20?ver=pdfcov
Published by the AIP Publishing

Advanced performance and scalability of Si nanowire field-effect transistors analyzed using noise spectroscopy and gamma radiation techniques

J. Li,[1] S. A. Vitusevich,[1,a)] M. V. Petrychuk,[2] S. Pud,[1] A. Offenhäusser,[1] and B. A. Danilchenko[3]
[1]*Peter Grünberg Institute, Forschungszentrum Jülich, 52425 Jülich, Germany*
[2]*Radiophysics Faculty, Shevchenko National University, Kiev, Ukraine*
[3]*Institute of Physics, NASU, Kiev, Ukraine*

(Received 23 September 2013; accepted 11 November 2013; published online 27 November 2013)

High-quality Si nanowire field effect transistors (FETs) were fabricated using thermal nanoimprint and chemical wet etching technologies. FET structures of different lengths demonstrate high carrier mobility with values of about 750 cm^2/Vs and low volume densities of active traps in the dielectric layers of $5 \times 10^{17}\,cm^{-3}\,eV^{-1}$. We investigated the transport properties of these n-type channel structures using low-frequency noise spectroscopy before and after gamma radiation treatment. Before gamma irradiation, FET structures with lengths of less than 4 μm exhibited noise from contact regions with $1/(L^2)$ dependence for the relative 1/f noise. After gamma radiation, the spectra reflected the priority of channel noise with 1/L dependence for all samples. The transport characteristics show that the fabricated nanowire FETs improved scalability, decreased parameter scattering, and increased stability after treatment. The results demonstrate that these nanowire FETs are promising for nanoelectronic and biosensor applications due to the cost-efficient technology and advanced performance of FETs with improved stability and reliability. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4833567]

I. INTRODUCTION

Si nanowires (NWs) are the object of increased attention because along with nanoscaling they provide a number of new features in electronic transport.[1] Novel test structures fabricated on the basis of Si NWs are the ultimate building blocks for future nanoelectronics[2] and biological sensor applications.[3] These structures have to be stable in operation. However, a great many factors influence their reliability and stability, particularly the fabrication technology of nanowire-based structures.

The fabrication technologies of Si NWs can be divided into two categories: "bottom-up" and "top-down." The bottom-up approach[4] relies on the growth of Si NWs, which suffers from the limitations of complex chip integration. The top-down approach[5] is more compatible with standard complementary metal-oxide-semiconductor (CMOS) processes and usually involves electron beam lithography and dry etching technologies. Top-down methods are currently attracting growing interest due to their unique advantages, such as high controllability, good reproducibility, and compatibility with state-of-the-art CMOS processing. These factors are very important for the fabrication of biosensors. However, almost all of the top-down processes use the reactive-ion etching (RIE) technique, which results in imperfections at the edges of nanostructures with a relatively low signal-to-noise ratio. Nanoimprint lithography (NIL) is a promising method for fabricating nanowire structures because of its low cost, high resolution, and high throughput. Anisotropic wet etching in tetramethylammonium hydroxide (TMAH) produces a smooth surface and improved performance of the structures.[6]

However, despite progress in the technology and the ability to fabricate nanosize structures with identical geometry, structures of a similar size show rather large scattering in their electrical characteristics. This is primarily caused by traps and imperfections, by the utilization of very thin dielectric layers, and captures by these defect charges, which lead to a shift in the threshold voltage and change the transistor characteristics over time as these traps are charged. The values of voltages applied to the transistor also affect the processes in the channel of silicon transistor and the exchange processes with the traps.[7] Noise spectroscopy is one of the most powerful methods for studying device performance and the reliability of structures with nanoscale dimensions, which is directly related to the type and number of traps in the structures. In this respect, the data obtained from noise spectra allows to analyze the performance of the structure, to identify the main traps determining transport properties, and to predict the stability and reliability of the structures. Thus, noise properties directly reflect the performance of fabrication technology.

In this work, the top-down method was used to fabricate high-performance Si NW-FET structures for biosensor applications applying cost-efficient thermal NIL in combination with anisotropic wet etching in TMAH. We investigated n-type channel Si NW-FET structures of different lengths. This enabled us to analyze different transport regimes, including regimes with and without the influence of contact contribution to channel transport, by studying the noise properties of the FET structures. In addition, the use of low doses of gamma radiation treatment yielded an improvement in the

a)On leave from the Institute of Semiconductor Physics, NASU, Kiev, Ukraine. Author to whom correspondence should be addressed. Electronic mail: s.vitusevich@fz-juelich.de.

structure parameters, such as reduced leakage current in the dielectric layers, reduced scattering in the transport characteristics, and a reduced Lorentzian noise component in the spectra of FET structures.

II. EXPERIMENTAL

We designed and fabricated Si NW structures with a width of 250 nm and different lengths (L = 2 μm, 3 μm, 4 μm, 6 μm, 8 μm, 10 μm, 12 μm, 14 μm, 16 μm, 18 μm, 20 μm, 22 μm) to investigate the effect of nanostructure scalability on device performance. The silicon-on-insulator (SOI) wafers were purchased from SOITEC, France. The thicknesses of the buried oxide (BOX) and of the top Si layer (Si⟨100⟩, boron-doped 14–22 Ω cm) were 145 nm and 70 nm, respectively. First, a dry thermal SiO_2 layer was grown. The final thicknesses obtained were 50 nm for the active Si layer and 37 nm for the SiO_2 layer, which is used as the mask layer during chemical etching. The nanowire structures were then transferred from the mold to the SOI wafers by thermal nanoimprinting (Nanonex NX2000, USA) with a main step of 550 PSI, 160 °C, 6 min. After imprinting, RIE was used to etch the residual resist layer and to etch off the SiO_2 layer between the contact lines and nanowire structures. These structures were then transferred to the active Si layer by anisotropic wet etching with TMAH (25%, 90 °C). Before this wet etching, 1% hydrofluoric acid (HF) etching for 20 s was necessary to remove the residual SiO_2. Due to the large etch rate difference between Si and SiO_2, the Si was etched off in the regions that were not covered by oxide. Under the oxide mask, the wet etching process slowed down when it reached the ⟨111⟩ surface of the Si layer. Further etching slowly reduced the width of the wires under the oxide mask. To maintain the surface quality of the Si NWs after TMAH etching, the oxide mask was removed by wet etching, and the Si NWs were then protected by an 8 nm silicon oxide formed by dry oxidation. Optical lithography was used to define a protection layer to protect the nanowires during ion implantation. Arsenic ions ($5 \times 10^{14}/cm^2$) were implanted on the conducting lines of the sensors with an energy of 7 keV and subsequently annealed at 950 °C for 30 s in nitrogen atmosphere to activate the arsenic ions and thus reduce serial resistance and improve the electrical performance of the devices. After annealing, the oxide layer was etched by 1% HF, and a new dry oxidation layer was grown again. Afterwards, 100 nm PECVD oxide was deposited as passivation. The back gate areas and the bond pads were then defined using optical lithography and wet chemical etching. Finally, metallization was performed using aluminum deposition and a lift-off process. The conductivity of the samples was modified by applying a voltage to the substrate used as the gate electrode. To tune the characteristics of the FETs, they were exposed to small doses of gamma irradiation using a standard isotope ^{60}Co source with a flux of 1 Gy/s and an energy of 1.2 MeV, using an accumulated dose of 10^4 Gy.

The electrical properties of the back-gated nanowire FETs were characterized by I-V measurements and low-frequency noise spectroscopy. A low-noise noise measurement setup developed in-house enabled us to study the peculiarities of noise spectra in the frequency range from 1 Hz to 100 kHz in order to extract the characteristic parameters of the structures as a function of channel length.

III. RESULTS AND DISCUSSION

A. Characterization of Si NW FETs before gamma radiation treatment

Fig. 1(a) shows a schematic of a Si NW FET with source and drain regions on the surface of a SiO_2/Si substrate. The inset in Fig. 1(a) shows a high-resolution transmission electron micrograph of a Si NW with a width of 250 nm while Fig. 1(b) shows a scanning electron micrograph of a Si NW-FET device and the amplified channel.

The electrical properties of the back-gated nanowire FETs were studied using I-V characteristics and low-frequency noise spectra measurements at room temperature. A low-noise measurement setup was developed in-house based on an amplifier with a low level of intrinsic input-related thermal noise of 2×10^{-18} V^2 Hz^{-1}. This enabled the peculiarities of the noise spectra to be studied in the frequency range from 1 Hz to 100 kHz and the characteristic parameters of the structures to be extracted as a function of channel length.

B. Current-voltage characteristics of fabricated NW FETs

The I-V characteristics for one of the Si NW devices with a length of 8 μm and width of 250 nm are shown in Fig. 2. The drain current I_D versus drain-source voltage V_{DS}

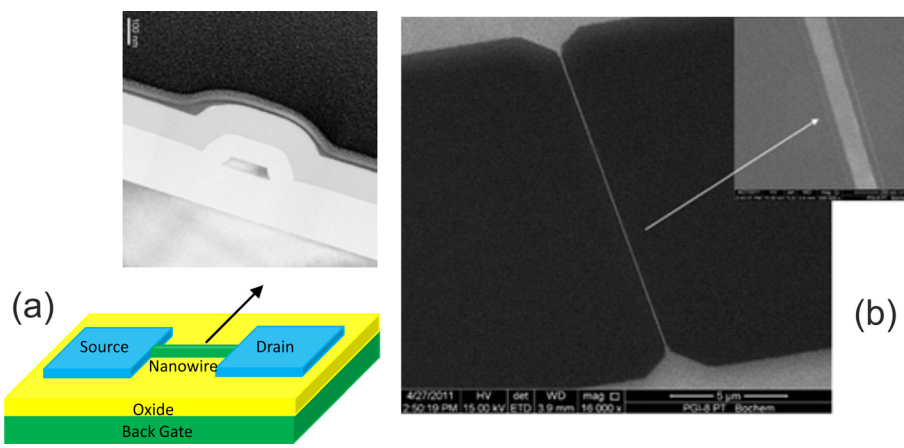

FIG. 1. (a) Schematic of a Si NW FET showing a NW with source and drain regions on the surface of a SiO_2/Si substrate. Inset: high-resolution transmission electron micrograph of cross-section of a Si NW with a width of 250 nm. The scale bar is 100 nm; (b) scanning electron micrograph of a fabricated silicon nanowire. The scale bar is 5 μm. Inset: enlarged image of the NW with a width of 250 nm.

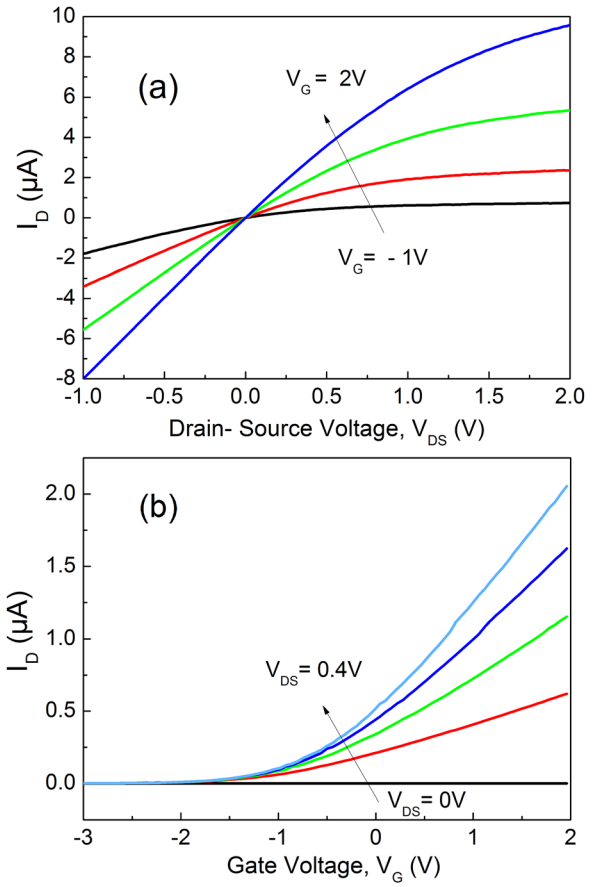

FIG. 2. (a) Typical output I_D-V_{DS} characteristics of the Si NW FET with a width of 250 nm and length of 2 μm measured at different gate voltages V_G in the range from −1 V to 2 V with a step of 1 V. The arrow indicates the increasing value of the back-gate voltage; (b) transfer characteristics of the FET, measured at increasing drain voltage V_{DS} in the range from 0 V to 0.4 V with a step of 0.1 V.

characteristics were measured at various gate voltages V_G (Fig. 2(a)). These output characteristics demonstrate that the drain current increases with positive drain-source voltage and can be effectively controlled by the gate voltage. The transfer characteristics of the Si NW device are shown in Fig. 2(b). For a given V_{DS}, the I_D shows a considerable increase with positive gate voltages V_G. This indicates an n-channel behavior of the transistor. A characteristic feature of these samples is a slow drift (*decrease*) in the drain current when drain-source voltage is applied over a long time of about 2 h. The transfer characteristics registered in the short-time regime (5 min after voltage application) and after a longer period (2 h) differ. In the second case, the measurements were performed after the establishment of the quasi-steady state. The value of the threshold voltage V_T was determined as −1.26 V.

The transfer characteristics, measured for Si NW FETs with different lengths, are shown in Fig. 3. The measurements were performed at a low drain voltage (V_{DS} = 100 mV). The transfer characteristics demonstrate good scalability depending on the nanowire length for different NW FETs. The transition from the linear I_{DS} (V_G) to a sublinear dependence, at $V_G > 1.5$ V, was typical for all samples. Such a behavior in the case of MOSFET devices is well studied and explained

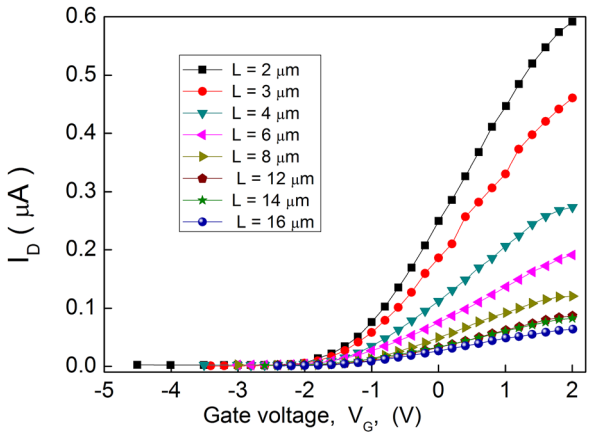

FIG. 3. Transfer characteristics measured at V_{DS} = 100 mV for Si NW sample with width W = 250 nm and different lengths L scaling in the range of 2 μm–16 μm.

by series resistance and mobility degradation.[8–10] It should be noted that the above-described dependences were measured at an applied drain-source voltage after 2–3 h, i.e., when the stable state was reached in the structures. Measurement results in the high-speed regime (measuring time: a few seconds) demonstrated no transition to a sublinear dependence. These data demonstrate that at V_{DS} = 100 mV and at gate voltages larger than 1.5 V, slow traps are charged slowly in the dielectric layer by negative charges, which leads to a shift in the threshold voltage and results in a reduced concentration of free electrons in the channel.

Fig. 4(a) shows the total resistance as a function of channel length, obtained at different gate overdrive voltages, V_G–V_T. The extracted contact resistances of the samples using the transmission line model (TLM) are shown in Fig. 4(b). We can clearly see that the contact resistance decreases as the gate bias increases. This decrease in contact resistance can be explained by the small voltage drop over the contact regions and potential profile change due to applied gate voltage.[11] Such a behavior has been taken into account for analysis of experimental data.

There was almost no registered change in the threshold voltage, which was estimated to be −1.26 V as a function of the length of the sample down to L = 4 μm. A sharp decrease was observed for samples with lengths of L = 3 μm and L = 2 μm. This effect in samples with short channels can be explained by contact phenomena at the interface between the ion implantation feedline region doped by As atoms and the sides of the nanowire channel of unintentionally doped silicon.

The results demonstrate that the contact resistance is lower than the total resistance, and we can neglect the contact effect of the drain and source on the channel conductivity for samples with lengths above 4 μm.

For MOSFET devices, field-effect mobility can be extracted from transfer characteristics using the following relation:[12]

$$\mu_{FE} = \frac{L^2 g_m}{C_{ox} V_{DS}}, \quad (1)$$

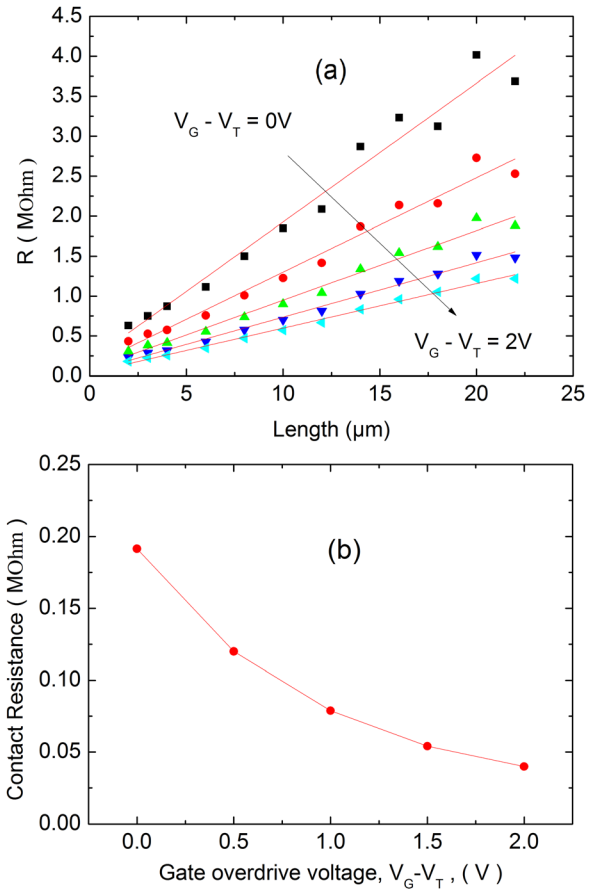

FIG. 4. (a) Total resistance of Si nanowire FET devices as a function of channel length, measured at low drain voltage $V_{DS} = 100$ mV and different gate overdrive voltages, V_G–V_T (V): 0, 0.5, 1, 1.5, 2. (b) Contact resistance extracted from TLM structures of different lengths. These data demonstrate nonlinear dependence on gate overdrive voltage.

where L is the gate length (cm), g_m is the transconductance (S), C_{ox} is the gate capacitance per unit area, which was calculated using $C_{ox} = \varepsilon_r \varepsilon_0 / d$, W is the width of the channel, V_{DS} is the drain-source voltage, ε_r is the dielectric constant of SiO_2, and d is the thickness of buried oxide layer. It follows from data shown in Fig. 5 that our nanowire devices exhibit a much higher mobility than the values usually reported in the literature about 180 cm^2/Vs.[13] This is due to a higher degree of confinement and the high quality of the nanowire fabrication process, which produces a smooth surface.

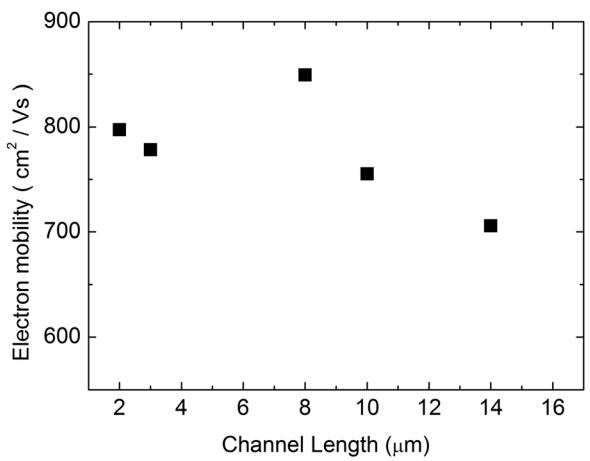

FIG. 5. Electron mobility (μ_{FE}) extracted for Si nanowire FET devices with different channel lengths.

C. Noise spectra of fabricated NW FETs

Noise measurements of NW FET samples of different lengths showed that the spectra mostly demonstrated $1/f$ behavior. A study of input referred gate noise behavior as a function of gate voltage showed that the main source of noise is the exchange process between the carriers and traps in the dielectric layer[14] as it will be shown below. This process can be described by the McWhorter model.[15] The input-referred noise spectral density is usually used to analyze the noise properties of the structures. Such equivalent input noise voltage was determined as a function of the gate in accordance with the following expression:

$$S_U = \frac{S_I}{g_m^2}, \tag{2}$$

where S_I is the current channel noise, and g_m is the transistor transconductance, which can be determined from the slope of the transfer characteristic of the transistor using the following expression:

$$g_m = \left. \frac{dI_D}{dV_G} \right|_{V_{DS}=const.} \tag{3}$$

The transconductance dependences on gate voltage are shown in Fig. 6.

In some cases, well-resolved Lorentzian noise components were registered in the spectra above the flicker noise. These components were observed in the spectra of short samples at high gate voltages. Typical families of spectra measured for samples with a length of 2 μm are shown in Fig. 7.

In the noise spectra measured for samples of short lengths (L = 2–4 μm), Lorentzian noise components were also

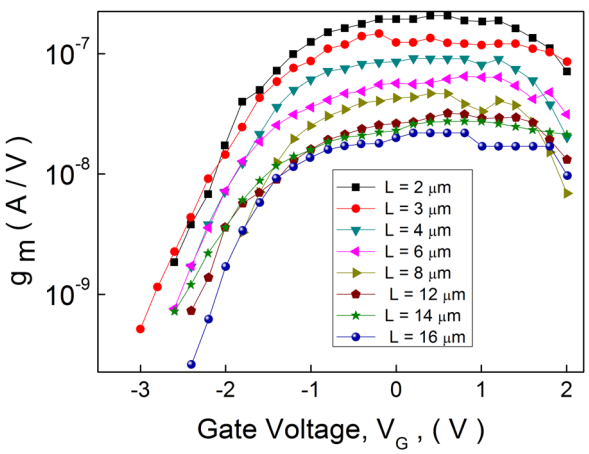

FIG. 6. Transconductance of Si NW FETs with a width of 250 nm and different lengths as a function of gate voltage V_G, measured at low drain voltage $V_{DS} = 100$ mV.

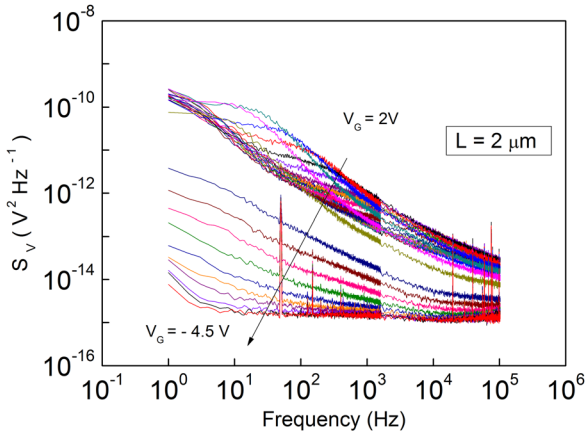

FIG. 7. Measured noise spectral density for a Si NW FET sample of length $L = 2\,\mu m$ at gate voltages from 2 V to −4.5 V.

resolved (Fig. 8(a)). The plateau of generation-recombination (GR) current noise S_I as a function of I shows I^{-3} power law dependence (Fig. 8(b)) at small values of current. Such a behavior cannot be explained by GR originating from the series resistance.[16] These GR components corresponding to random telegraph signal (RTS) noise can be related to the channel of the FET.

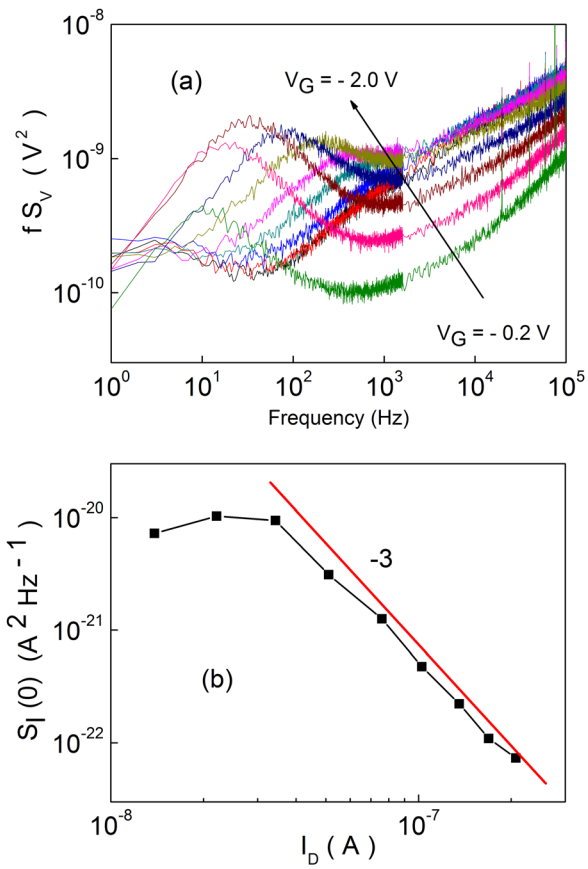

FIG. 8. (a) Normalized noise spectral density for the Si NW FET sample with length $L = 2\,\mu m$ measured at different gate voltages in the range from −0.2 V to −2.0 V with a step of 0.2 V. (b) The plateau of GR current noise S_I (data taken from Fig. 8(a)) as a function of drain current I_D at 10 Hz frequency.

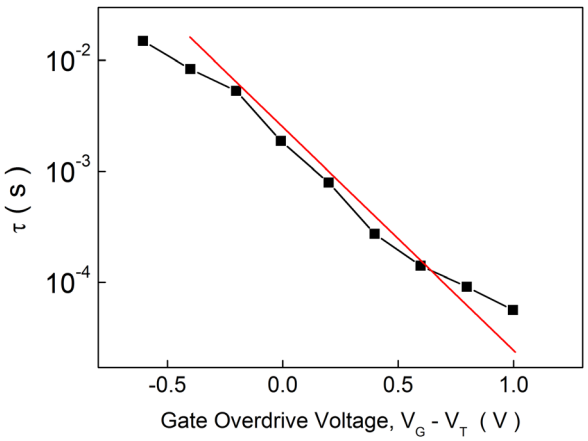

FIG. 9. Capture time constant extracted from measured spectra (Fig. 8) for the Si NW FET sample of length $L = 2\,\mu m$ at different gate overdrive voltages, V_G–V_T, from −0.6 V to 1.0 V.

An analysis of RTS noise spectra for the sample length was $L = 2\,\mu m$ allowed us to obtain the dependence of the time constant on the overdrive gate voltage (Fig. 9).

The dependence of the time constant on the gate voltage is exponential. This relationship can be represented as

$$\tau \sim \exp[-\alpha(V_G - V_T)], \tag{4}$$

where $\alpha = 4.6$.

Such a dependence reflects the characteristic time constant of carrier capture. The reason that the time constant decreases with an increasing gate voltage is the increase in free carrier concentration in the channel, i.e., the time of capture decreases with increasing concentration.

D. Analysis of flicker-noise component

The noise level was set to 1/f noise at the frequency $f = 1$ Hz. Dependence of this parameter on the gate voltage, measured at drain-source voltage $V_{DS} = 100$ mV, is shown in Fig. 10: $1/f$ noise at $f = 1$ Hz.

These dependences are typical of MOSFET structures. A weak dependence was observed in the accumulation regime at high voltages and a sharp decrease in the subthreshold regime.

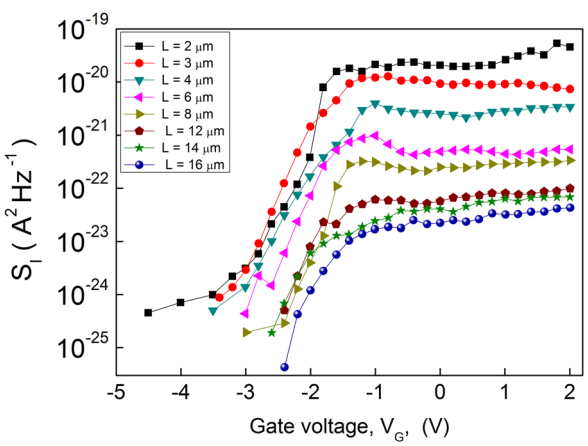

FIG. 10. Measured noise spectral density of flicker noise $1/f$ at $f = 1$ Hz as a function of gate voltage V_G at $V_{DS} = 100$ mV.

Peaks were observed at times at voltages close to the threshold V_{Th}. Further analysis was performed using equivalent gate voltage noise (Fig. 11).

The dependence of 1/f noise at the frequency of f = 1 Hz was plotted as a function of the gate voltage and used to obtain the input-related noise spectral density S_U as a function of V_G, as shown in Fig. 11.

S_U behavior was similar for all samples: a relative independence of gate voltage between $-1\,V < V_G < 1.5\,V$. A weak dependence was observed in the inversion regime at high voltages $V_G > 1.5\,V$. This increase can be explained by changes of g_m as a function of time due change of trap charging state before reaching the equilibrium conditions. At negative values of V_G, the growth of the S_U at $V_G < -1\,V$ can be explained as follows. With increasing of absolute value of gate voltage an accumulation layer forms near the bottom of the interface layer. This layer screens the channel from the influence of gate voltage (and from voltage fluctuations), which leads to a slower change in the drain current with gate voltage in this area (Fig. 11). Therefore, the noise in the subthreshold regime is no longer determined by the states in the bottom interface, but rather by the states in the upper interface between the passivation dielectric layer and the channel. In this case, the charge fluctuations in the dielectric layer transform in the channel with a transconductance defined by the upper dielectric layer.

In addition, the presence of accumulation layer in the channel can result in a number of processes. The first process involves the formation of two p-n junctions connected in series: the forward-biased source/accumulation channel and the reverse-biased junction formed by the accumulated channel drain. This leads to a current associated with recombination (forward-biased junction) and generation (reverse-biased junction). Generation-recombination processes of this type are reflected in the spectra in addition to the 1/f noise of the Lorentzian noise component, particularly in the samples of short length (Fig. 7). The current increase at large negative V_G is also associated with this phenomenon. The second process is caused by the presence of a dielectric interface on the top channel, which can lead to the "floating base" effect,[17] which also results in additional noise with a characteristic frequency determined by internal capacitances.

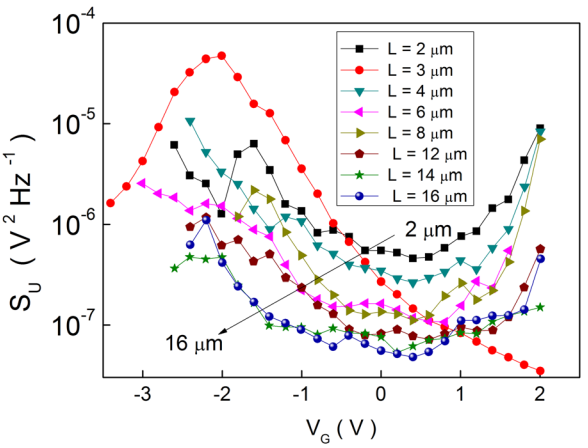

FIG. 11. The input-referred noise spectral density S_U as a function of gate voltage V_G, obtained for Si NW FETs of different lengths.

At moderate voltages independent of back-gate voltage V_G, the plateau (Fig. 11) corresponds to the flicker noise associated with a bottom dielectric layer. It should be noted that the noise level in this region differs (by about one order of magnitude) for samples of different lengths. However, this difference is much smaller than the difference of three orders of magnitude in the S_I values (Fig. 10). The data in Fig. 11 shows that S_U has weak dependence on V_G in voltage range from −1 to 1 V. This confirms the applicability of the McWhorter model[20] with

$$S_U(f) = \frac{kTq^2\lambda N_{ot}(E_F)}{fWLC_0^2} \sim \frac{1}{WL}, \tag{5}$$

where $N_{ot}(E_F)$ is the trap density in the dielectric layer, $C_0 = \varepsilon_{ox}/t_{ox}$ is the gate insulator capacitance per unit area, ε_{ox} is the permittivity of the dielectric layer, t_{ox} is the oxide thickness, $\lambda = \sqrt{\hbar^2/2m_z^*\phi_B} = 10^{-8}$ (cm) is the tunneling distance, T is the temperature, k is the Boltzmann constant, q is the electron charge, φ_B is the potential barrier between the channel and the gate dielectric, $\hbar$ is the reduced Plank's constant, m_z* is an effective mass of the carriers, and W is the width of the sample.

The experimental results obtained (Fig. 12) demonstrate that S_U is reciprocally dependent on length 1/L at $V_G = 0$.

Using Eq. (5), we can determine the volume trap density of active sites in the lower dielectric layer, substituting $\varepsilon_{ox} = 3.9$ ε_0 and $t_{ox} = 145$ nm, $S_U = 10^{-7}$, $L = 10\,\mu$m, $W = 0.25\,\mu$m: N_{ot} is about $5 \times 10^{17}\,cm^{-3}\,eV^{-1}$. This value is not as high as that obtained for top-quality bulk Si material.[18]

E. Estimation of the Hooge parameter

In order to compare the noise level of our devices with noise values reported in the literature, we estimated the Hooge parameters using following equation:[19]

$$S_I = \frac{\alpha_H I_D^2}{fN}, \tag{6}$$

where N is the number of carriers and α_H is Hooge's constant, which is used to quantitatively assess and compare the noise performance of our devices.

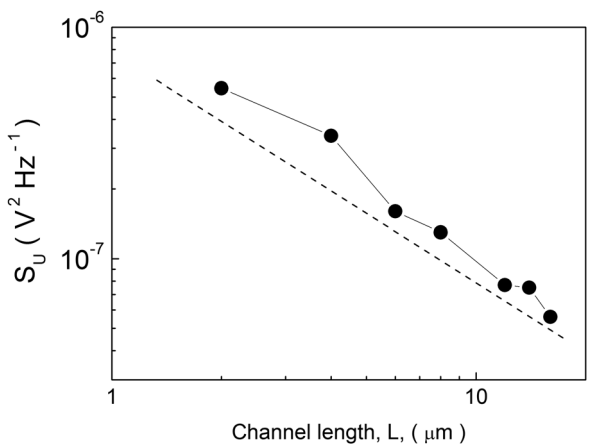

FIG. 12. The input-referred noise spectral density S_U as a function of L at $V_G = 0$. Dashed line shows 1/L dependence.

The total number of carriers, N, in the working point with the maximum of the transconductance using the following equation:

$$N = \frac{I_D L^2}{qV_{DS}\mu}. \quad (7)$$

The average Hooge parameter (Fig. 13) for the devices was below 2×10^{-4} for Si NW fabricated using developed nanoimprint technology. This value is much lower than the values reported in the literature for silicon nanostructures,[20] demonstrating the improved technology and performance of Si NW FETs.

F. Comparison of electric properties of Si NW FETs before and after gamma radiation treatment

Typical output characteristics of Si NW FETs measured before and after gamma radiation treatment with a dose of 10^4 Gy are shown in Fig. 14. The measurements were performed in a linear regime at $V_{DS} = 100$ mV for samples with a uniform width of 250 nm and different lengths.

It should be noted that subthreshold current is strongly reduced after the treatment by an average of about one order of magnitude. Before gamma irradiation, V_T was -1.26 V (except for samples of length 8 μm and 12 μm). After irradiation, the threshold voltage shifted to a positive value of 0.295 V. In addition, increasing negative gate biases in unexposed to gamma radiation samples results in a sharp increase in current, while irradiated samples showed a decrease. Thus, the subthreshold current behaved differently in the irradiated and non-irradiated samples. At the same time, the scattering of characteristics reduced after treatment while the reproducibility of electric parameters improved. Further analysis of NW FET transport properties before and after gamma radiation treatment was performed using the results of the noise study. Fig. 15 shows the normalized measured 1/f noise obtained at a frequency of 1 Hz. It should be emphasized that there are specific differences in the noise characteristics: in the irradiated samples at a subthreshold voltage, noise is relatively weakly dependent on the gate voltage, and the non-irradiated characteristics demonstrate a sharp peak at $V_G - V_T = -0.5$ V, followed by a sharp decrease at large negative biases.

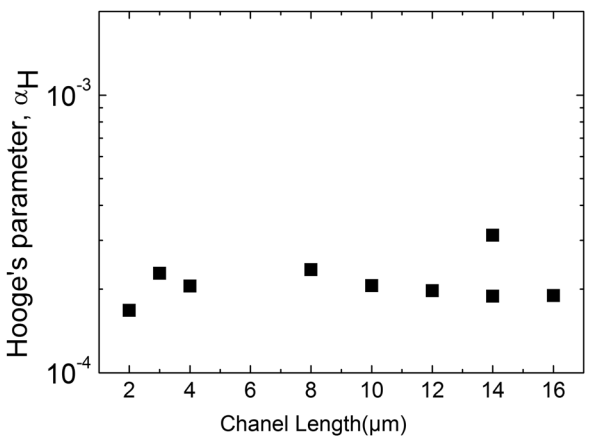

FIG. 13. Hooge parameters for Si NW FET structures of different lengths.

In spite of the relatively long lengths of the channels from 2 μm to 22 μm, as shown in Fig. 16, we found that the normalized current noise spectral density decreases as a function of $1/(L^2)$ in the samples with lengths of less than 4 μm. Such dependence is characteristic of the contact contribution to the noise properties. At the same time, in relatively long samples, the behavior changed to a 1/L dependence, demonstrating the priority of channel noise. The latter dependence was also registered for samples with short lengths after gamma irradiation, reflecting improved scaling of the sample characteristics as a function of length. Increased stability of the structures and decreased scattering in the structure characteristics were also observed. The effect of gamma radiation can be explained by relaxation processes in the structure and a decrease in the strain[21,22] in the contact regions of the FETs.

Thus in the case of short samples in the strong inversion, noise related to near-contact regions was mainly observed while noise related to the channel phenomena was registered in the case of long samples before and after irradiation. After gamma radiation treatment, the contact contribution became negligible compared to an increased channel noise, and the noise results for short-channel samples also showed channel-related properties.

A more detailed analysis of noise spectra for samples with lengths of 2 μm, measured before gamma radiation treatment

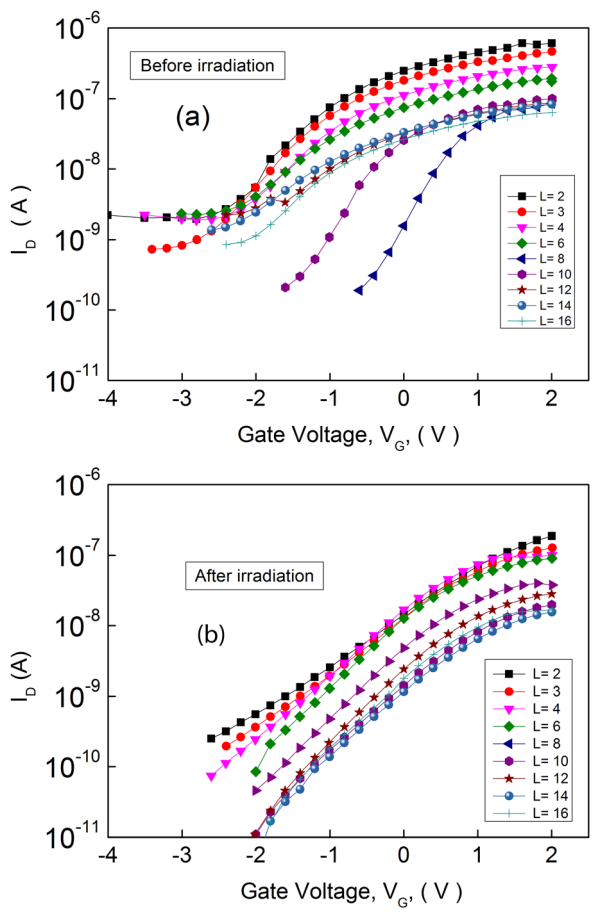

FIG. 14. Output characteristics of Si NW FETs (a) before and (b) after gamma radiation treatment measured at $V_{DS} = 100$ mV for samples of different lengths in the range from 2 μm to 16 μm.

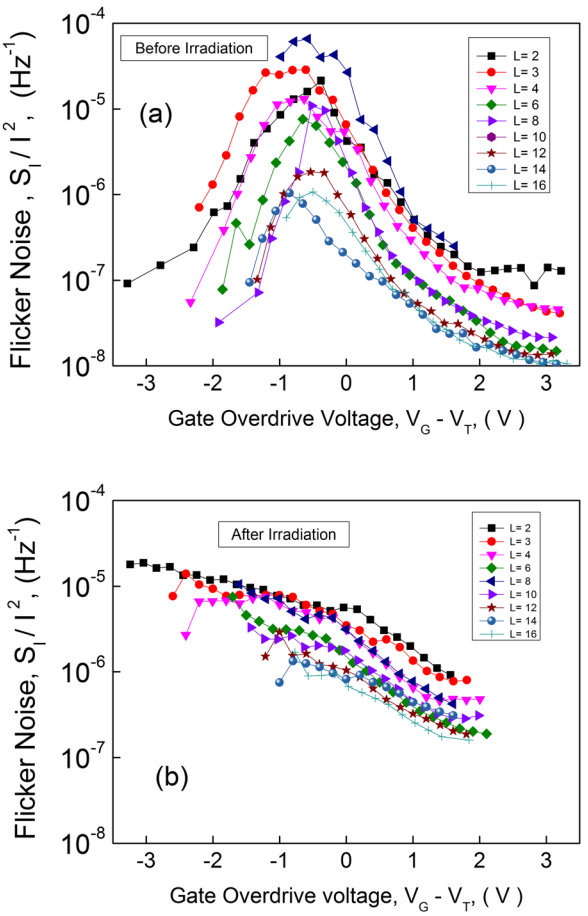

FIG. 15. 1/*f* noise at a frequency of 1 Hz measured (a) before and (b) after gamma radiation treatment as a function of overdrive gate voltage V_G–V_T.

at large negative gate voltages, revealed Lorentzian component with a slope near −2 (Fig. 17) noise. It should be emphasized that Lorentzian component disappears after the gamma radiation treatment.

The slope of the noise spectra in the low frequency region is close to 2, indicating the GR nature of this noise. The value of the time constant of the GR process is beyond the range investigated ($\tau > 1/2\ \pi f_0 = 1/2\pi \cdot 1\,\text{Hz} = 0.16\,\text{s}$). The

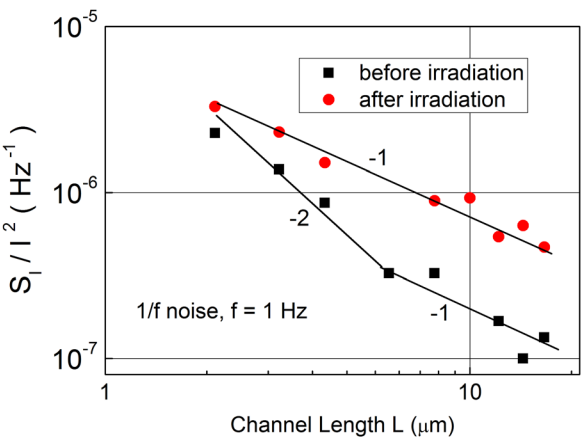

FIG. 16. Normalized current noise spectral density of the flicker noise component versus sample length, measured at drain-source voltage $V_{DS} = 100\,\text{mV}$ and gate overdrive voltage V_G–$V_T = 0.5\,\text{V}$.

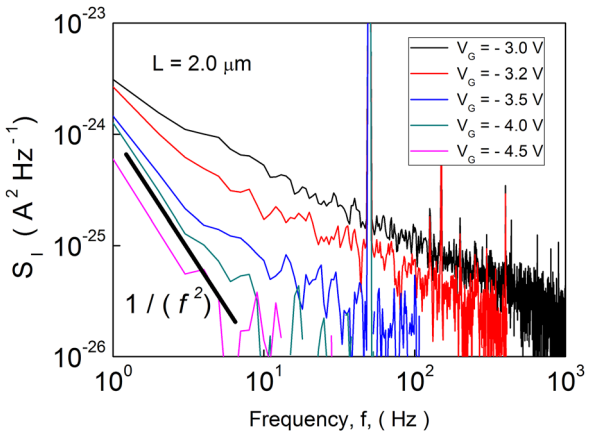

FIG. 17. Current noise spectral density of Si NW sample of length $L = 2\,\mu\text{m}$, measured at large negative gate biases V_G: −3.0 V, −3.2 V, −3.5 V, −4.0 V, −4.5 V.

slope of the spectra of other samples with short channels measured at large biases showed a similar tendency to increase at low frequencies, but the increase was less pronounced.

At the same time, the subthreshold current of non-irradiated samples increases (Fig. 14(a)) at large negative gate voltages. This current is accompanied by a low-frequency GR noise with a time constant of $\tau > 0.16\,\text{s}$. Noise S_I at a frequency of at least $f = 1\,\text{Hz}$ decreases with an increasing negative bias V_G. The reason for the low-frequency noise behavior of sub threshold current is difficult to identify. Kink effects[17] cannot be responsible for the noise: the non-linear kink effect is impossible because of the low voltage V_{DS}; the linear kink effect is also impossible because of the large thickness of the back-gate (in this case—buried) oxide. Furthermore, the tunneling of charges through the top oxide of the valence band is also impossible because the field is practically zero. The behavior in the subthreshold region can be explained by processes taking place at negative voltages[23–26] in MOSFET structures. At these biases, the Si layer is partially depleted, and majority carriers (holes) accumulate near the buried oxide layer. This results in an increase in the forward current through the source/Si-layer junction. This current generates shot noise with a spectrum limited to a frequency determined by the nature of the capacitive impedance of the p-n junction. The capacity of this impedance is determined by the state of interface between the Si/SiO_2 buried oxide layer. This interface state was investigated with proton irradiation in Ref. 25. It was shown that irradiation reduces the level of GR noise components in n-MOSFET, but in p-MOSFETs, the influence is the opposite, i.e., the GR noise increases.

In our work, we found that under the influence of a low dose of gamma radiation treatment, the GR noise component in the subthreshold current (at a large negative bias on the gate, in the regime of the accumulation of holes) was not registered after treatment despite a lower flicker noise level. This agrees with the trends described in Ref. 25 for n-MOSFETs of relatively large areas.

The origin of the capacitive impedance of the p-n junction is discussed in Refs. 23–25. In Ref. 23, it is suggested

that front-back gate coupling effects can be explained by considering the increased body-source leakage currents and, hence, the body-source conductance induced by the accumulation. In Ref. 24, it is proposed that the additional source of floating-body-related excess Lorentzian noise is shot and thermal noise in the body charge, filtered by the *RC* impedance of the source-body junction. The possible origin of the body-charge fluctuations and related shot and thermal noise are discussed. In Ref. 26, the back-gate-induced noise overshoot revealed in partially depleted SOI n-MOSFETs and p-MOSFETs. It is assumed that the accumulating back-gate voltage induces the p^{++}-n^{--} junction near the back interface, and its leakage current increases conductance.

The results of our investigation of the effect of gamma irradiation on subthreshold current and associated GR noise, registered before treatment, allow us to associate the capacitive component with the slow centers at the interface between the Si/SiO_2 buried oxide layer. The fact that GR noise can be removed after irradiation confirms participation of slow traps, which may change their charge state under the influence of radiation. There is also a change in the threshold voltage, and its variance is reduced in the array of samples. The subthreshold current is also reduced (Fig. 14). In addition, the normalized input-referred noise spectral density also demonstrates the influence of the change in the charge state of slow traps at the interface (compare Fig. 18(a) and Fig. 18(b)) and after the gamma radiation reflects behavior that is more typical of high-quality MOSFETs with noise that is almost independent of gate voltage.

The spectra measured for short-length samples also reveal Lorentzian-type noise components in addition to the 1/f noise component (Fig. 19). An analysis of fluctuation behavior as a function of time showed that the Lorentzian noise components correspond to the RTS-type noise, i.e., the noise is associated with fluctuations related to a single center. Measurement results for the RTS noise component for short-length samples demonstrated that there is a significant contribution of this kind of noise before irradiation (Fig. 19), but that after exposure, the level of the RTS noise component significantly reduces, and the characteristic frequency decreases from 1.6 kHz to 40 Hz. At the same time, the slope drain-gate characteristics reduce slightly with back-gate voltages, as shown above. This can be explained by the shift of the conductive channel to the upper interface and the reduced influence of the back-gate voltage on the channel. In this case, the electron density at the lower interface decreases as does the probability of the GR process, manifested in the form of RTS noise, leading to a shift in the spectrum of RTS to low frequencies. Since the bottom interface no longer exhibits high current density, the noise level decreases.

The shift in the maximum frequency of Lorentzian RTS after irradiation (Fig. 19, red curve) can be explained by changes in the charge state of the center from the positively charged (attracting) state to neutral, or from neutral to a negatively charged (repulsive) state. This results in a decrease in carrier concentration for exchange processes between the channel and dielectric layer. In turn, this causes a decrease in the probability of the carrier being captured and, consequently, an increase in the time constant, which determines the position of the maximum frequency in the noise spectrum.

The reduction in the amplitude of RTS noise in the irradiated sample can be explained as follows. RTS noise modulates, i.e., charge fluctuations of a single center modulate the conductivity of the channel with high density. These regions arise because of the inhomogeneity of the semiconductor characteristics in the channel area.

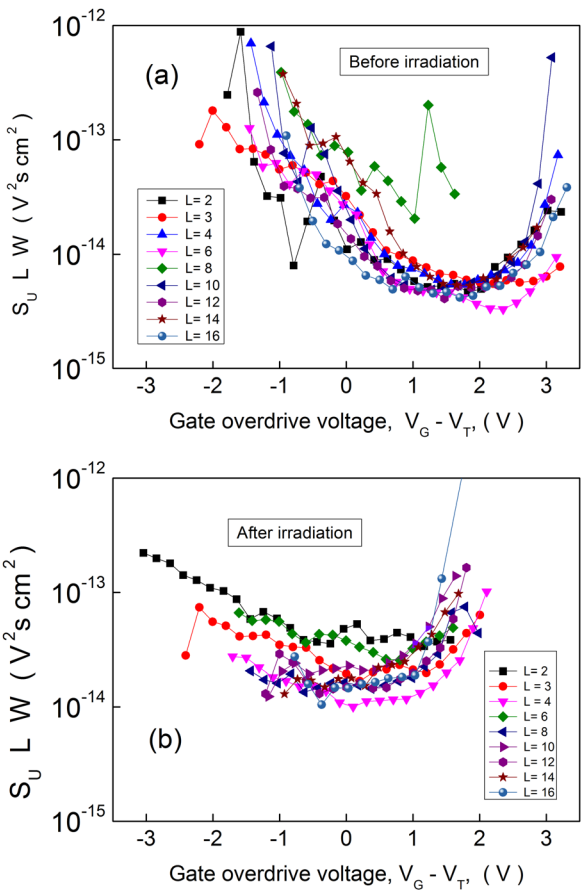

FIG. 18. The normalized input-referred noise spectral density S_U as a function of gate overdrive voltage V_G–V_T (a) before and (b) after gamma radiation treatment with a dose of 10^4 Gy.

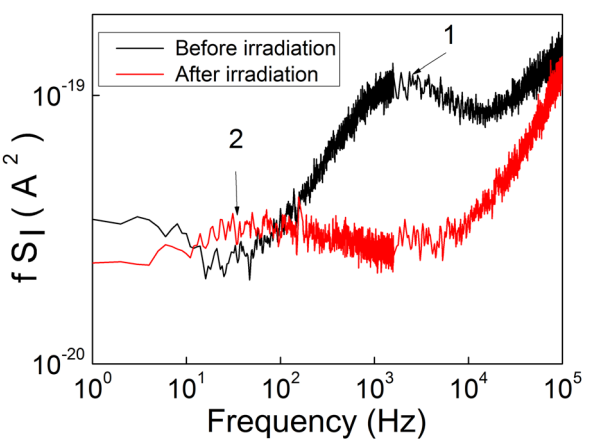

FIG. 19. Normalized current-noise spectral density measured in the strong inversion for a Si NW-FET sample with a width W = 250 nm and length L = 2 μm (1) before and (2) after gamma radiation treatment.

Irradiation removes mechanical stress in the contact region, which also reduces 1/f noise and RTS noise levels. The fact that the RTS noise was only observed in short-channel devices confirms the near-contact origin of the observed RTS fluctuations.

In the subthreshold regime, the slope of the drain current-gate voltage characteristic reduces twice, which represents a reduced influence on the conduction channel of the bottom gate bias. Such changes in the conditions at the lower interface influence the subthreshold current, which after exposure practically disappears. The shift in the threshold voltage to positive values of gate voltage indicates an increase in negative charge at the interface. At the same time, it is known that γ-irradiation leads to an increase in the concentration of positive charge due to the difference in nobilities of electrons and holes. This contradiction may be explained by percolation transport before gamma radiation treatment due to non-uniform potential redistribution along the SOI wafer. Radiation stimulated a more uniform redistribution of the potential. This resulted in a change from a negative to a positive threshold voltage and reduced scattering in device characteristics.

IV. CONCLUSIONS

In this paper, we verified the high quality of nanowire FETs fabricated by TMAH wet etching and thermal nanoimprint technology. This fabrication method is a promising low-cost and CMOS-compatible method. The results of electrical measurements show that we can neglect the contact effect for samples with lengths greater than 4 μm. The characteristic time constants corresponding to the capture of the carriers were determined by analysing RTS noise spectra components. Trap density, estimated from flicker noise, was found to be about $5 \times 10^{17}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$, which is of the order of magnitude of good-quality bulk silicon material. The improved technology and TMAH chemical etching produced samples with a high mobility and low noise level. Such devices can be employed as chemical or biological sensors with a higher sensitivity to the object being tested due to a high level of uniformity and performance. The results demonstrate that the irradiation results in increased stability and reliability of the structure parameters. Normalized current noise spectral density decreased as a function of 1/L in the samples of all lengths after gamma radiation treatment, demonstrating the priority of channel noise. An analysis of the RTS noise component, registered for samples of short length before gamma treatment, was reduced after this treatment, confirming the results obtained.

ACKNOWLEDGMENTS

J. Li would like to acknowledge support from the China Scholarship Council. S. Pud greatly appreciates the research grant from the German Academic Exchange Service (DAAD). The authors are grateful to the anonymous referees for their constructive criticism.

[1]R. B. Salazar, S. R. Mehrotra, G. Klimeck, N. Singh, and J. Appenzeller, Nano Lett. **12**, 5571 (2012).
[2]R. Rurali, Rev. Mod. Phys. **82**, 427 (2010).
[3]B. P. Timko, T. Cohen-Karni, Q. Qing, B. Z. Tian, and C. M. Lieber, IEEE Trans. Nanotechnol. **9**, 269 (2010).
[4]G. F. Zheng, W. Lu, S. Jin, and C. M. Lieber, Adv. Mater. **16**, 1890 (2004).
[5]S. M. Koo, A. Fujiwara, J. P. Han, E. M. Vogel, C. A. Richter, and J. E. Bonevich, Nano Lett. **4**, 2197 (2004).
[6]E. Stern, J. F. Klemic, D. A. Routenberg, P. N. Wyrembak, D. B. Turner-Evans, A. D. Hamilton, D. A. LaVan, T. M. Fahmy, and M. A. Reed, Nature **445**, 519 (2007).
[7]S. Pud, J. Li, M. Petrychuk, S. Feste, S. Vitusevich, B. Danilchenko, A. Offenhaeusser, and S. Mantl, J. Appl. Phys. **113**, 124503 (2013).
[8]J. Woo and B. Cheng, J. Phys. IV, France **6**, C3–43 (1996).
[9]A. G. Sabnis and J. T. Clemens, Electron Devices Meet. **25**, 18 (1979).
[10]L. K. J. Vandamme, Fluct. Noise Lett. **7**, L321 (2007).
[11]X. S. Li and L. K. J. Vandamme, Solid State Electron. **35**, 1471 (1992).
[12]Y. Huang, X. F. Duan, Y. Cui, and C. M. Lieber, Nano Lett. **2**, 101 (2002).
[13]N. K. Rajan, D. A. Routenberg, J. Chen, and M. A. Reed, IEEE Electron Device Lett. **31**, 615 (2010).
[14]L. K. J. Vandamme, X. S. Li, and D. Rigaud, IEEE Trans. Electron Devices **41**, 1936 (1994).
[15]A. L. McWhorter, "1/f noise and germanium surface properties," in *Semiconductor Surface Physics*, edited by R. H. Kingston (University of Pennsylvania, Philadelphia, PA, 1957).
[16]E. P. Vandamme and L. K. J. Vandamme, Microelectron. Reliab. **36**, 1107 (1996).
[17]G. G. Shahidi, IBM J. Res. Dev. **46**, 121 (2002).
[18]J. Jomaah, M. Fadlallah, and G. Ghibaudo, in *Advances in Innovative Materials and Applications*, edited by M. Soueidan, M. Roumie, and P. Masri (Trans. Tech. Pubn., 2011), Vol. 324, p. 441.
[19]L. K. J. Vandamme and F. N. Hooge, IEEE Trans. Electron. Devices **55**, 3070 (2008).
[20]K. Heo, E. Cho, J. E. Yang, M. H. Kim, M. Lee, B. Y. Lee, S. G. Kwon, M. S. Lee, M. H. Jo, H. J. Choi, T. Hyeon, and S. Hong, Nano Lett. **8**, 4523 (2008).
[21]J. S. Milne, A. C. H. Rowe, S. Arscott, and C. Renner, Phys. Rev. Lett. **105**, 226802 (2010).
[22]P. E. Allain, X. Le Roux, F. Parrain, and A. Bosseboeuf, J. Micromech. Microeng. **23**, 015014 (2013).
[23]N. Lukyanchikova, N. Garbar, A. Smolanka, M. Lokshin, E. Simoen, and C. Claeys, J. Appl. Phys. **98**, 114506 (2005).
[24]N. Lukyanchikova, N. Garbar, A. Smolanka, E. Simoen, and C. Claeys, IEEE Electron Device Lett. **25**, 433 (2004).
[25]E. Simoen, A. Mercha, J. M. Rafi, C. Claeys, N. B. Lukyanchikova, A. M. Smolanka, and N. Garbar, J. Appl. Phys. **95**, 4084 (2004).
[26]N. Lukyanchikova, N. Garbar, A. Smolanka, E. Simoen, and C. Claeys, in *Science and Technology of Semiconductor-On-Insulator Structures and Devices Operating in a Harsh Environment*, edited by D. Flandre, A. Nazarov, and P. F. Hemment (Springer, Netherlands, 2005), Vol. 185, p. 255.