CMOS - Top down

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Strained Silicon

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From Silicon Nanostructures to Double Gate MOSFETs

INTRODUCTION

For the last 15 years, the advancement of powerful computers has been facilitated by the extreme downscaling of the dimensions of microelectronic devices. In particular the most important device, the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), was reduced in size from a few µm in the mid-80s to 130 nm in 2002. According to the International Technology Roadmap for Semiconductors (ITRS) [1], this downscaling will continue for the next 12 years and will require devices with typical dimensions of a few tens of nm. In these extremely small MOSFETs, physical limitations will induce parasitic phenomena. These so called Short Channel Effects (SCE) are one of the most challenging problems the semiconductor industry has to face. Down to the 130 nm node the SCE were dealt with by improving the lateral MOSFET layout [2]. Uniform doping levels were replaced by more elaborate doping profiles and layer thicknesses were reduced to a few nm. Below the 50-nm node, however, new concepts with completely different layouts need to be developed.

APPROACH

One of the most promising candidates for downscaling is the double-gate MOSFET. While in a normal MOSFET the conducting channel is formed on the surface of a thick silicon layer, in a double-gate MOSFET this silicon layer is only 5 to 20 nm thick. The potential of this layer is controlled by two gates on either side of the thin silicon layer (Fig. 1a-c). Biasing the two gates in parallel induces inversion channels on both sides of the layer until they overlap. Consequently, the whole silicon layer is inverted. This improves the shape of the electric field between the gates, so that the field penetration from drain to source is effectively screened. This eliminates one of the SCE. Therefore the double-gate MOSFET has recently attracted increasing atten-

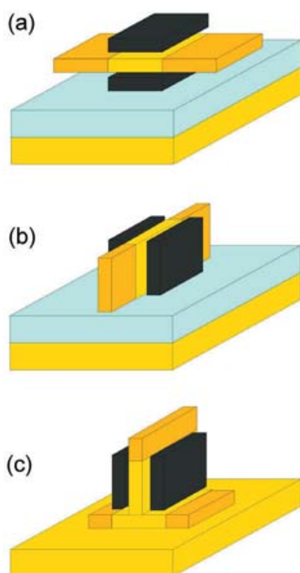


Fig. 1
Double-gate MOSFET layouts:
(a) Planar Double-Gate,
(b) FinFET and
(c) Vertical Double-Gate.

tion. Three basic double gate configurations have been proposed. In the first, the silicon channel layer and current flow are parallel to the wafer surface (Fig. 1a). However, it is technologically challenging, to implement identical gates on top and beneath the channel layer. In the second concept the silicon channel layer is perpendicular to the surface, but the current still flows in parallel to the wafer (Fig. 1b). This so-called FinFET is fabricated from Silicon on Insulator (SOI) substrates and requires two sub-50 nm lithography steps: one for the patterning of the channel layer, and the other for the definition of the gate length. In the third layout (Fig. 1c), which is the topic of this article, the channel layer is perpendicular to the substrate, but the current also flows perpendicular to the surface. The “heart” of the transistor consists of a 20 nm wide and 300 nm high silicon ridge. The doping profile (npn for n-channel and pnp for p-channel transistors) is adjusted by ion implantation. It defines the channel length. This necessitates only one sub-50 nm lithography step, which simplifies the process flow. First results of a preliminary layout were published in Ref. 3.

RESULTS

Nano-patterning

The device processing commences with the most challenging step, the nano-patterning of 20 nm wide silicon ridges with an aspect ratio of 25. Since even advanced optical lithography presently is not capable of providing these fine lines, electron beam lithography is used to define these small patterns. We use a new electron beam negative tone resist, HSQ. This is well known as a flowable oxide for intermetalic dielectrics in multilevel metalizations. HSQ is an inorganic polymer based on a Si-

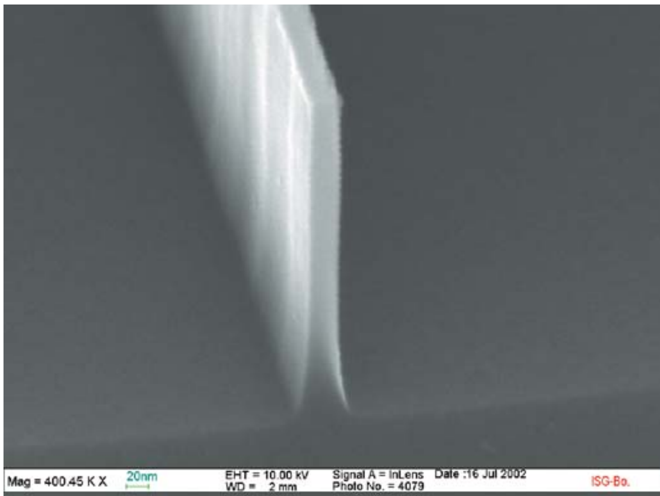
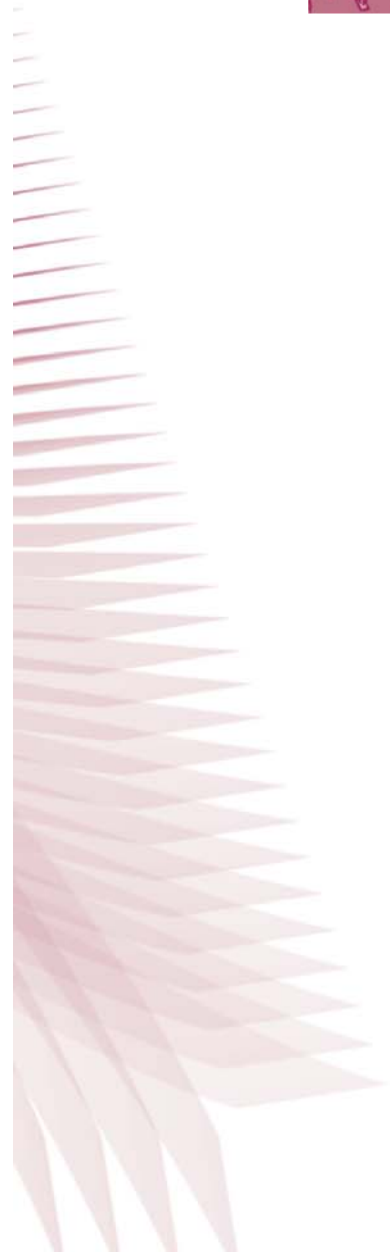


Fig. 2
A 330 nm high and 25 nm wide silicon ridge produced by electron beam lithography and reactive ion etching.

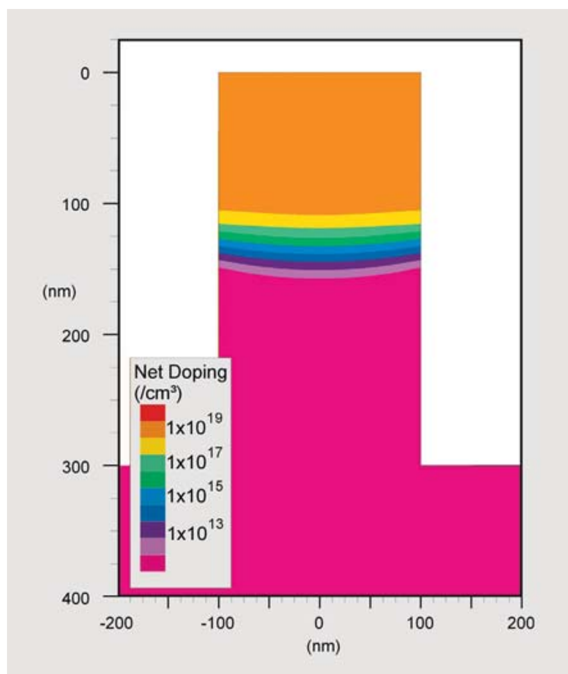


matrix. The e-beam irradiation converts the HSQ to SiO_x and the unexposed HSQ can be removed in standard DUV-resist developers. Resist lines of 23 nm width and 100 nm height are obtained.
After defining the patterns they have to be transferred to the silicon using Reactive Ion Etching (RIE). Immediately before RIE the resist is baked at 450°C for 1 hour to increase etching resistance. The pattern transfer is done by inductively coupled plasma reactive ion etching in a 2-step process. In the first step an HBr plasma removes the native oxide on the wafer surface, in the second step a mixture of HBr and O_2 is used to increase the selectivity between resist and silicon. The remaining resist is removed by immersion in hydrofluoric acid. Figure 2 shows a silicon ridge 25 nm wide and 330 nm high.

Ion implantation

For doping of the source and drain regions ion implantation is necessary. However, the application of ion implantation to nanoscale targets has not yet been studied in detail. It is known from planar targets, that the resulting final dopant profile after implantation and annealing is strongly affected by transient enhanced diffusion (TED), which is governed by the increased point defect concentration introduced by implantation.

Fig. 3
Simulation of the doping profile in a nanopillar after annealing.



Additionally, the agglomeration of these point defects leads to the formation of extended defects. It has been established that the surface is a sink for point defects and significant evidence has been adduced to suggest that TED and extended defect evolution are influenced by surface proximity. As the lateral dimensions of implanted structures decrease, the availability of free surfaces increases, facilitating the enhanced annihilation of point defects at the surface. Consequently, the diffusion of dopants and the behaviour of extended defects are expected to differ significantly from that in bulk materials.

Simulations of boron implants into silicon nanostructures followed by annealing were carried out using SSUPREM4 to predict the diffusion behaviour in infinitely long nano-ridges, 300 nm high and 25 to 200 nm wide. For smaller structures a reduced diffusion is predicted. A typical doping profile is illustrated in Fig. 3. The simulations predict a lateral non-uniformity of the diffusion front. The boron at the center of the ridge diffuses more rapidly than in the surface regions. Preliminary measurements using scanning spreading resistance microscopy show evidence of the latter behavior.

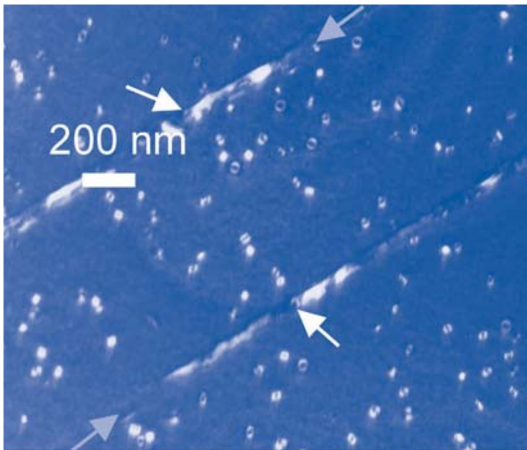


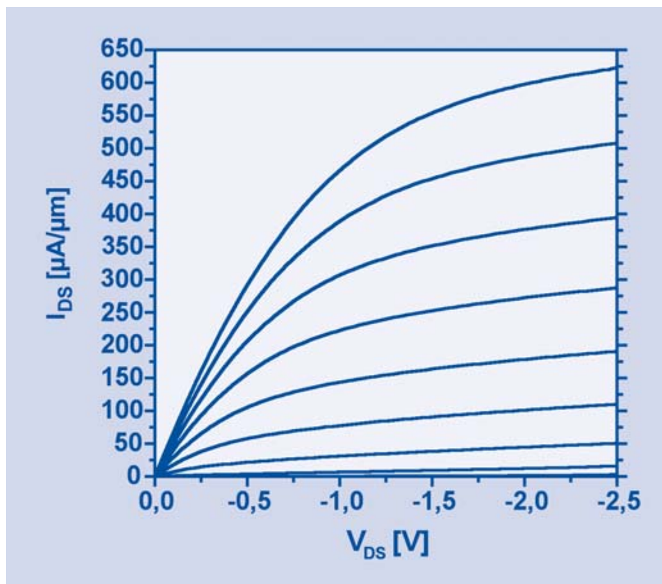
Fig. 4
Plan view TEM of 40 nm Si nano-ridges. The ridges are indicated by the grey arrows and several dislocation loops within the ridges are highlighted by the white arrows.

We performed plan-view transmission electron microscopy analysis on 40 nm nano-ridges. These were amorphised using Si implants and recrystallized using annealing. Despite the reduced dimensions, extended defects are still observed in the nanostructures with dimensions similar to those in bulk Si (Fig. 4).

Devices

After the undoped substrates have been patterned into nano-ridges as described above, the source and drain doping is adjusted by ion implantation. For this purpose the sidewalls of the ridges are protected by a 15 nm oxide spacer, which is removed after annealing out the implantation damage. Here an optimized thermal treatment is crucial. Otherwise the dopants will diffuse from the spacer into the ridge and eliminate the channel. The gate oxide is grown by low temperature wet oxidation to reduce the thermal budget, and hence the diffusion at the source and drain junctions. The gate stack is completed by deposition of in situ doped polysilicon. This polysilicon is patterned and etched back to obtain a spacer at the sidewall of the ridges, which ends 100 nm below the top of the ridge. The deposition of a 700 nm thick oxide and the planarization of the structure facilitates the formation of the contact directly at the top of the ridge. On the planarized sample a lithography step defines the top contact holes. Using RIE, a certain amount of oxide can be removed to open the top of the ridge. After defining the other contact areas

Fig. 5
Transistor characteristics obtained with a 50 nm gate length vertical double gate design, shown in Fig. 1c.



and performing an additional contact implantation, a NiSi-salicide process is carried out to obtain ohmic contacts. Finally, aluminum is evaporated for contact formation. Excellent transistor characteristics are shown in Fig. 5 for a 50 nm gate lenght p-channel device. Its maximum transconductance, which is a measure for the switching speed, reaches 480mS/mm.

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Self-Assembly Silicide Nanopatterning and Advanced MOSFET Devices

INTRODUCTION

Metallic silicides are widely used as contacts and local interconnects in silicon microelectronic devices due to their excellent material properties and their high process stability. In particular $CoSi_2$ has emerged as a leading choice for these purposes since it maintains its properties even after scaling down to nanometer dimensions. Furthermore it can be grown epitaxially on silicon, providing almost atomically abrupt interfaces and highly uniform layers. These advantages make epitaxial $CoSi_2$-nanostructures highly attractive for use in advanced nanoelectronic devices. In recent years, silicide growth and self-assembly patterning of epitaxial $CoSi_2$ has been studied and used in Jülich for the fabrication of nanometric MOSFET devices. The limited resolution of optical lithography and the lack of suitable dry etching processes for $CoSi_2$ make the self-assembly patterning a promising alternative for the generation of silicide nanostructures. These nanostructures are very interesting for studying nanoheterostructures and nanomaterials.

APPROACH

When $CoSi_2$ on a Si substrate is exposed to an oxidizing ambient, the formation of SiO_2 is energetically more favorable than the formation of cobalt oxides. The excess metal will then diffuse through the silicide layer and react with the substrate material, forming new $CoSi_2$. This self passivating behavior is a key feature of metal silicides and is well understood. Based on this we have developed a self assembly technique for patterning of epitaxial $CoSi_2$ by local oxidation of silicides (LOCOSI). The oxidation process, as mentioned above, forms SiO_2 on top of the silicide layer, driving it into the silicon substrate. Surprisingly, high quality single-crystalline epitaxial $CoSi_2$ layers can be pus-

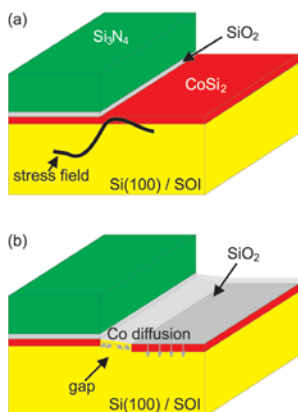
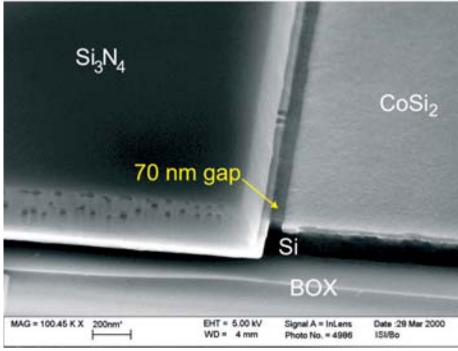


Fig. 1
Schematic drawing of the patterning structure (a) before oxidation and (b) after oxidation.

hed into the substrate without degradation – even into a depth, which exceeds their thickness several times. Our patterning technique uses a local mechanical stress field to modify the diffusion processes during the oxidation of the silicide layer to generate the nanostructures. It is schematically shown in Fig. 1. First, a single crystalline $CoSi_2$-layer of a thickness typically between 20 and 30 nm is grown by molecular beam epitaxy and an additional annealing step. This process is called molecular beam allotaxy (MBA). It is highly reproducible and yields very homogenous layers on both conventional and silicon-on-insulator (SOI) substrates. Then an oxidation mask consisting of SiO_2 and Si_3N_4 is deposited by plasma enhanced chemical vapor deposition (PECVD), which is patterned using conventional optical lithography and dry etching. This masking technique is similar to that of the well known LOCOS-process (local oxidation of silicon) which induces a strain field along its edges in the underlying layers due to the intrinsic stress of the nitride (Fig. 1a). Subsequent rapid thermal oxidation (RTO) leads to a separation of the silicide layer near the edge of the mask. This is caused by the stress induced anisotropic diffusion of the Co atoms during the oxidation process (Fig. 1b). Combined with selective etching processes, this technique is also capable of producing narrow silicide nanowires. The silicide nanostructures form excellent Schottky contacts on moderately doped silicon and can be used for the fabrication of ultra-short-channel MOSFET devices.

RESULTS

Nanogaps and nanowires: The process described above produces homogenous separations (nanogaps) with dimensions down to 40 nm in silicide layers on both conventional and SOI substrates. A scanning electron microscopy (SEM) micrograph of a typical structure is shown in Fig. 2a. A cross-sectional transmission



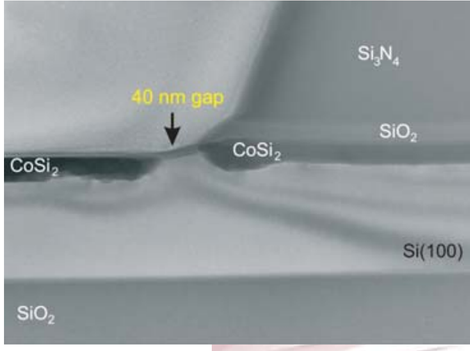
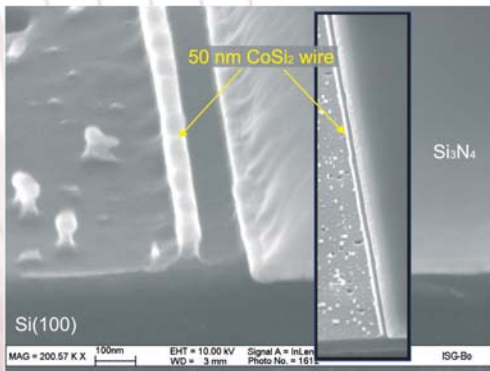


Fig. 2
(a) SEM image of a 70 nm wide gap and (b) TEM micrograph of a 40 nm wide gap.

electron microscopy (TEM) image of the structure is shown in Fig. 2 b. At the edges of the separated silicide layers one can cleary observe the formation of <111> facets. These facets are energetically favorable because of their low interface energy and are responsible for the astonishingly high uniformity of the structure. Additional etching steps enable the fabrication of nanowires as displayed in the microscopy images in Fig. 3. Figure 3a shows SEM micrographs of a 50 nm wide silicide wire. The silicion was etched back by RIE using the wire as an etching mask. The resulting silicide/silicon-ridge structure may be applied in vertical devices with a self aligned silicide contact on top. A 50 nm wire on SOI is also shown in cross-section in the TEM micrograph in Fig 3b. One can see the formation of the <111> facets leading to a triangular shape of the wires. It is possible to contact these wires with a simple masking step during fabrication which is essential for measuring transport properties, currently under investigation.

Schottky barrier MOSFETs: As an application of the nanogaps, we have fabricated Schottky barrier MOSFETs on SOI with channel lengths of 70 nm. Schottky barrier MOSFETs avoid implanted p-n-areas and the concomitant problems with activation and diffusion of dopant atoms which are hard to control on nanometer scale. Therefore the p-n-diodes forming source and drain in con-



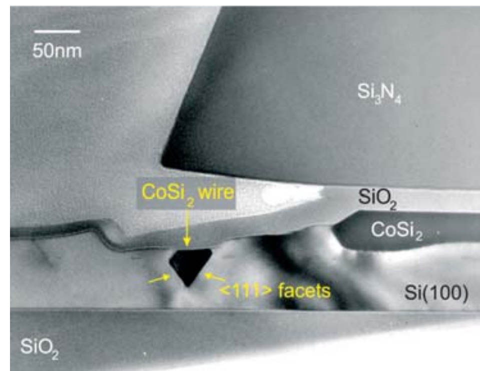
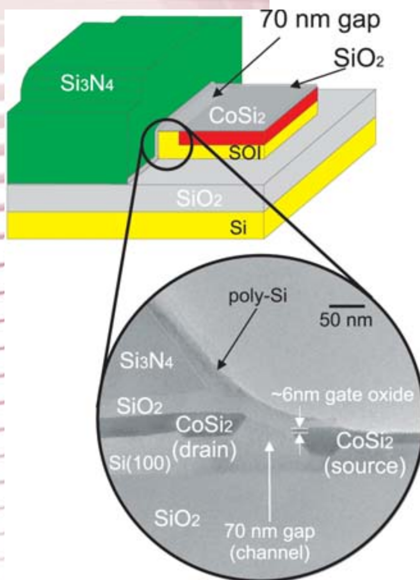


Fig. 3

(a) SEM images of a 50 nm $CoSi_2$ wire. The silicon was etched back using the wire as an etching mask.

(b) XTEM micrograph of a 50 nm wide $CoSi_2$ wire on SOI. The formation of the <111> facets are responsible for the triangular shape of the wire.



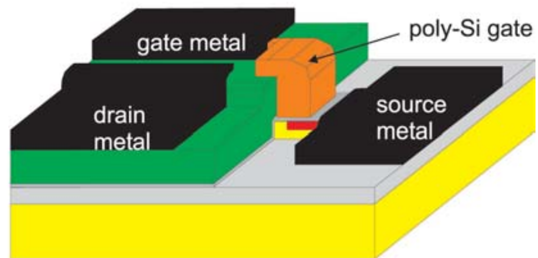


Fig. 4:

(a) Schematic drawing and XTEM micrograph of the SBMOSFET-structure after the nanopatterning step.

(b) Schematic drawing of the device.

ventional MOSFETs are replaced by Schottky-Diodes which work in a similar way. Fig 4(a) shows schematically the fabrication process of our transistor after the nanopatterning step and a TEM micrograph of a device test structure. The two separated silicide layers act as source and drain. The oxide formed on top of the gap during the oxidation is used as the gate dielectric. A poly-Si gate is attached to the structure and the contacts are metallized for measurements. A schematic view of the basic device structure is shown in Fig 4 b. The transistor can be driven as both p-channel and n-channel device. Fig. 5 demonstrates the ambipolar operation modes (band schemes in the insets) and their respective I-V-curves of our device. In the off-state the carriers are blocked by the Schottky barrier. An applied gate-voltage

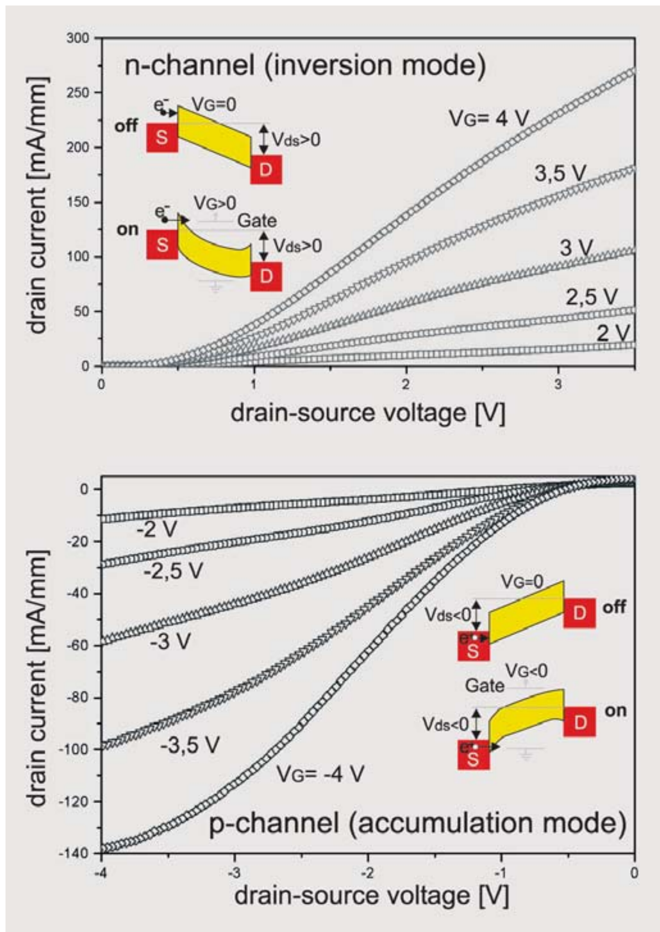


Fig. 5:
I-V charakteristics of the inversion and the accumulation mode of a 70 nm Schottky barrier MOSFET. The insets show schematically the band diagrams of the transistor in the on and off state

modifies the Schottky barrier width so that electrons (or holes) can tunnel through the barrier and the transistor is turned on. Although the concept of SB-MOSFETs dates back to 1968, they have recently received renewed attention due to their potential application in nanoelectronics. They are interesting from the device point of view and improve our fundamental understanding of Schottky barriers on the nanometer scale.

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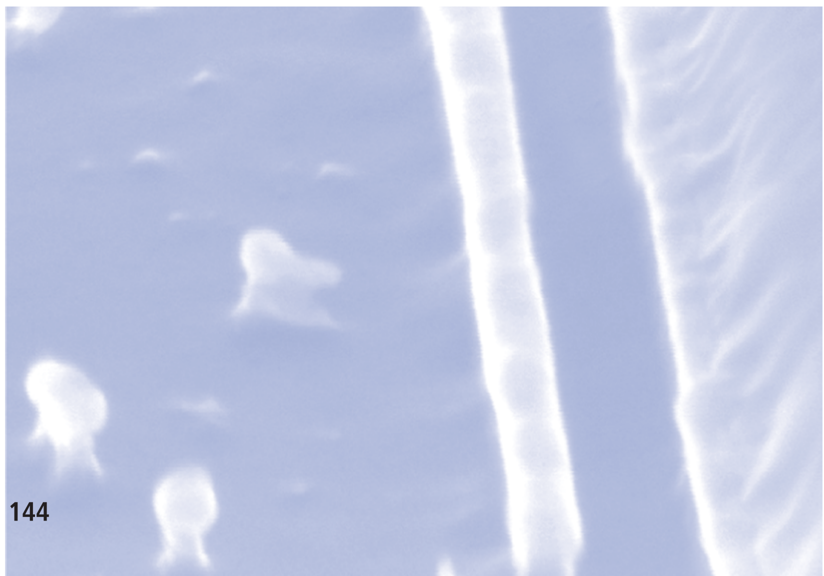


Towards Strained Silicon: Strain Relaxed Ultrathin SiGe Buffer Layers Produced by He^+ Ion Implantation

INTRODUCTION

Strained silicon layers provide a strongly increased carrier mobility, compared to unstrained silicon crystals. This leads to much faster transistors without the need to further shrink the lateral dimensions of the devices. In fact, strained Si can be regarded as a new high mobility group IV semiconductor which will lead to a new generation of high speed strained Si and Si/SiGe devices with superior electronic performance. In the very near future strained Si will be used in the silicon mainstream technology [1]. Strained Si is of great advantage for Si MOSFETs, modulation doped field effect transistors (MODFETs) and resonant tunneling diodes (RTDs). A key issue for the successful application of strained Si is the fabrication of high quality thin strain relaxed (SR) SiGe buffer layers on Si or SOI (Silicon On Insulator) wafers. The buffer layers serve as virtual substrates for the growth of strained silicon. These SR SiGe buffer layers have a slightly (approx. 1%) larger lattice constant than silicon and allow the pseudomorphic growth of a thin, biaxially strained Si layer. We have shown that high quality thin SR SiGe buffer layers can be produced using He^+ ion implantation and annealing. All other methods for the fabrication of SR SiGe buffer layers, as the growth of thick graded buffer layers, SIMOX or oxidation methods, have their specific drawbacks, which are overcome by our new processing scheme.

APPROACH

Following a Jülich invention, we produce ultrathin SR SiGe layers (≈100nm) using He ion implantation and subsequent annealing at a moderate temperature (750-900°C) to relax the strain of a pseudomorphic SiGe layer grown on Si or on SOI [2,3]. Ion

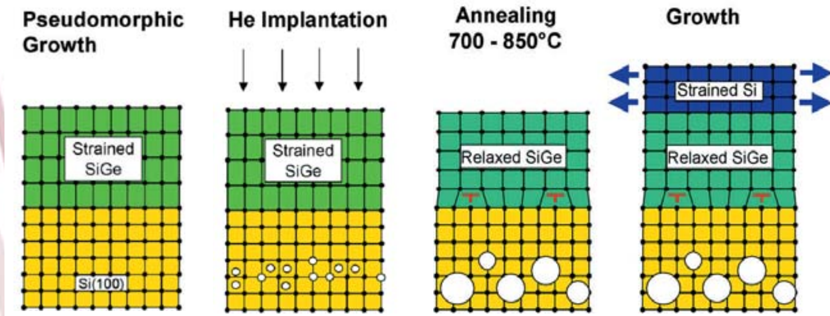
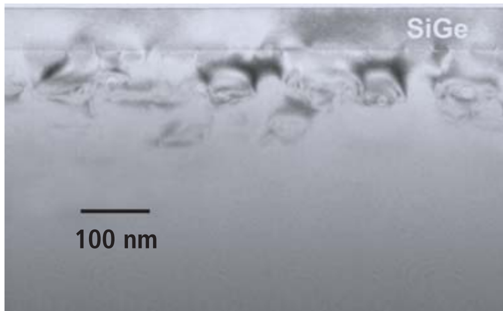


Fig.1
Main steps of the new process:
(a) First, a fully strained SiGe layer is epitaxially grown on a Si(100) substrate.
(b) He ions are implanted through the SiGe layer into the substrate in order to form a defect region below the interface.
(c) Bubbles form during annealing at temperatures between 750-900 °C, which punch out dislocation loops. The dislocation loops move to the interface and form strain relieving misfit dislocations.
(d) A thin Si layer grown pseudomorphically onto the SR SiGe layer is under tensile, biaxial strain.

implantation is a well established technique in semiconductor research and industry. Note, that about 20 different implantations are required to fabricate a modern Si chip. The pseudomorphic SiGe layers are grown either by Molecular Beam Epitaxy (MBE) or by Chemical Vapour Deposition (CVD) in collaborations with the DaimlerChrysler Research Center, Ulm and with IMEC, Leuven, Belgium. The process is fully CMOS compatible. Its main steps are shown in Fig. 1. First, a pseudomorphic SiGe layer is grown on Si(100). Then He ions are implanted, using our ion implanter, which complies to industrial standards. The He ions come to rest 50 to 200 nm below the SiGe/Si interface. Annealing at around 900°C leads to the desired strain relaxation of the layer. During annealing the implanted He forms highly pressurized bubbles in the silicon which punch out dislocation loops. These dislocation loops move to the Si/SiGe interface and form misfit dislocations, which provide the desired strain relaxation. Subsequently, strained silicon is obtained by growing a thin, pseudomorphic Si layer on top of the SR SiGe layer. The strained Si is then under tensile, biaxial strain.

RESULTS

We have studied the strain relaxation of SiGe layers with Ge concentrations of up to 33 at. % and a thickness between 50 and 120 nm grown on Si and SOI wafers, using different ion implantation and annealing conditions [3]. Fig. 2 shows a cross sectional transmission electron micrograph (XTEM) of a $Si_{.73}Ge_{.27}$ layer implanted with 13 keV He^{+} ions at a dose of $1.5x10^{16}$ cm^{-2} after thermal annealing at 850 ^{o}C for 600 seconds.
A bubble layer approximately 70 nm below the interface is surrounded by dislocation loops which extend to the interface. Strain contrast at the interface indicates the formation of misfit dislocations. The SiGe layer appears to be free of threading dislocations. An AFM image of this sample (Fig. 3) shows the very smooth surface of the SiGe layer with an rms roughness of only 0.32 nm. This flat surface is an enormous advantage compared to alternative approaches where polishing is needed before the Si overgrowth step or a wafer bonding process. The amount of strain relaxation was measured by ion channeling angular yield scans along a (100) plane through the [100] sample normal and



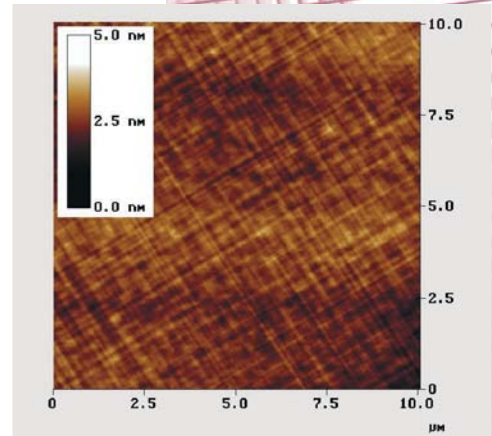


Fig. 2
XTEM micrograph of a 75 nm thick $Si_{.73}Ge_{.27}$ layer on Si(100) after 13 keV He implantation and annealing at 850°C for 600s. Many misfit dislocations are visible at the SiGe/Si interface but no threading dislocations were found in the cross-section of the SiGe layer. He bubbles and dislocations appear in the Si substrate.

Fig. 3.
AFM of a relaxed SiGe layer showing the small rms roughness of 0.32 nm. The excellent surface smoothness allows overgrowth without additional polishing.

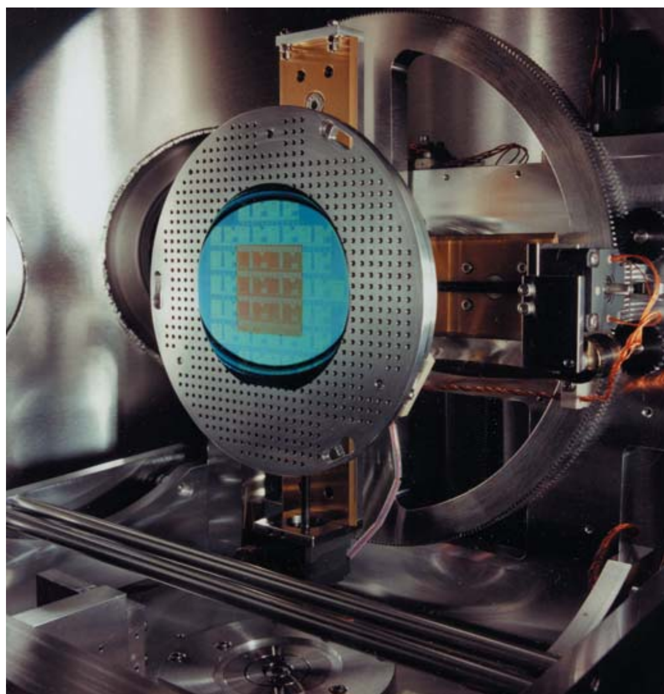


Fig. 4
View of the unique 5-axes goniometer installed at the Jülich Tandetron accelerator where strain measurements in SiGe layers are performed.

an inclined [110] direction. In a cubic crystal, the angle between the [100] and [110] directions amounts to 45°. Tetragonal strain in the SiGe layer leads to a shift in the angular scans. This shift can be measured with a high precision 5-axes goniometer, as installed at the Jülich Tandetron (Fig. 4), and converted directly into the strain data. Fig. 5 shows the influence of an 18 keV He implantation with a dose of $2x10^{16}$ cm^{-2} on the relaxation of a 100 nm $Si_{.695}Ge_{.305}$ layer after annealing at 750 °C for 600 seconds. The 'as grown' sample shows an angular deviation of –0.59° from 45° indicating full pseudomorphic strain. The unimplanted and annealed sample shows a strain relaxation R_{rel} of only 7%, while the implanted and annealed sample shows an R_{rel}–value of 66%. Our process also can be applied successfully to SiGe layers on SOI substrates. Fig. 6 shows an XTEM micrograph of an MBE grown 88 nm $Si_{.67}Ge_{.33}$ layer on SOI implanted with a dose of 1.0 x 10^{16} cm^{-2} after annealing at 850 °C for 600s. The degree of relaxation R_{rel} was 64%. Surprisingly, no bubbles appeared in the Si layer at this low dose. Recently, we have demonstrated that MODFETs produced on such buffer layers

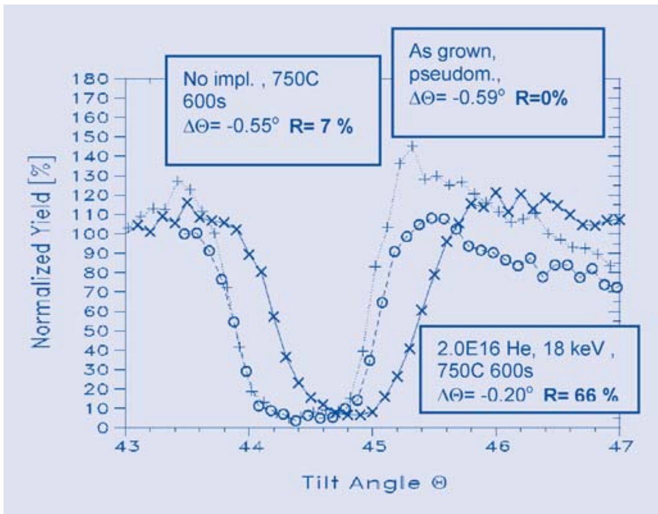


Fig. 5
Channeling angular yield scans demonstrating the influence of an 18keV He implantation with a dose of $2.0x10^{16}$ cm^{-2} on the relaxation of a 100nm $Si_{695}Ge_{.305}$ layer after annealing at 750°C for 600s. The 'as grown' sample shows an angular deviation of -0.59° from 45° confirming full pseudomorphic strain. The unimplanted and annealed sample shows only a R_{rel} of 7%, while the implanted and annealed samples shows R_{rel} of 66%. This implies that unimplanted areas keep their strain during the annealing.

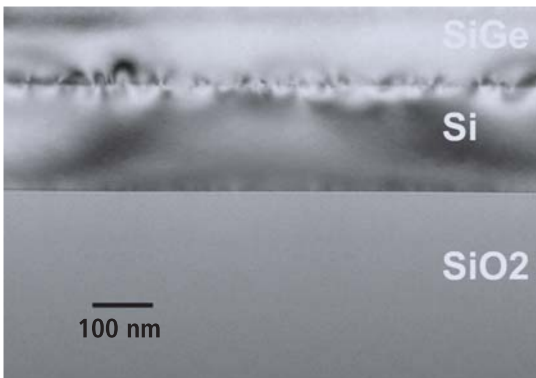


Fig. 6
XTEM micrograph of a strain relaxed SiGe layer with a Ge concentration of 33 at.% on SOI implanted with 13 keV He ions and a dose of $1.0x10^{16}$ cm^{-2}. Due to the low dose, no bubbles are visible in the about 100nm thick Si layer. The SiGe layer appears to be free of threading dislocations in the XTEM image. The degree of relaxation is 64% .

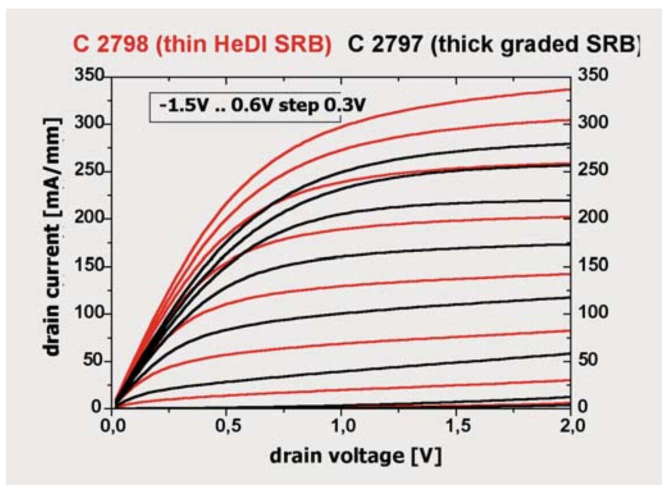


Fig. 7
Drain current vs. drain voltage for different gate voltages. Black curves are measured from transistors grown on a thick, graded SR buffer layer, red curves are from a transistor grown on a He implanted SR SiGe buffer layer exhibiting even higher saturation currents.

show the same RF response (f_{max} =95 GHz , f_t = 53 GHz) and higher drive currents as devices processed on thick, graded buffers [4]. The I-V characteristics of the devices are shown in Fig. 7.

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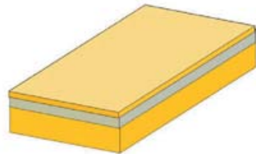
Ultrafast Silicon-based Photodetectors

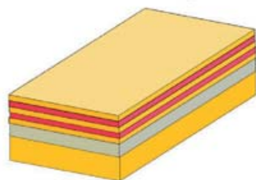
INTRODUCTION

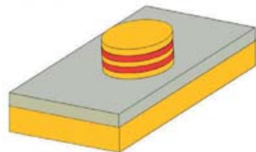
Optocommunication relies on fast detectors. We have developed a complete series of detectors for visible and near-infrared (IR) frequencies, which are all based on silicon technology. They are compatible with CMOS processing. The photosensitive layer consists of pure Si for the operation at wavelengths shorter 1.1 µm and SiGe quantum wells or Ge for the wavelengths up to 1.5 µm. In order to provide an ultrafast electrical response, the photogenerated carriers from the semiconductor have to reach the high conductivity metallic electrodes after a very short drift path. This is best achieved in a plate capacitor structure with a submicrometer thin layer of a semiconductor sandwiched between two metallic electrodes, forming Schottky contacts between both metals and the semiconductor. Therefore our devices consist of a thin photosensitive layer of less than 400 nm thickness grown epitaxially on a metallic $CoSi_2$ bottom electrode and capped by a semitransparent top Cr contact. This design provides a high carrier mobility in the crystalline semiconductor and an average carrier drift path of only 200 nm to the electrodes, leading to record measured electrical signals of pulse widths from 1.3 to 12 ps (full width at half maximum, FWHM). The development of these detectors has been part of an EU program to demonstrate different key optoelectronic components, which are all completely silicon- based.

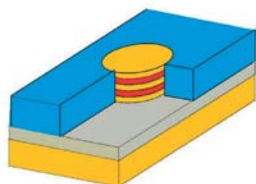
APPROACH

Most of the diodes are manufactured in our institute using an epitaxial „silicon-on-metal" heterostructure, see Fig.1. The buried $CoSi_2$ layer has been fabricated by implantation of Co ions and a subsequent annealing step. The resulting metallic $CoSi2_2$ is epitaxially aligned to the Si wafer. On the $CoSi_2$, the photodetecting layer of Si or SiGe is grown in our molecular beam epitaxy (MBE) setup. For patterning, standard UV lithography and reactive ion etching has been used. The finished devices contain an array of 60 detectors of different geometrical dimen-









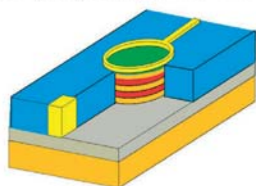


Fig.1
Fabrication steps

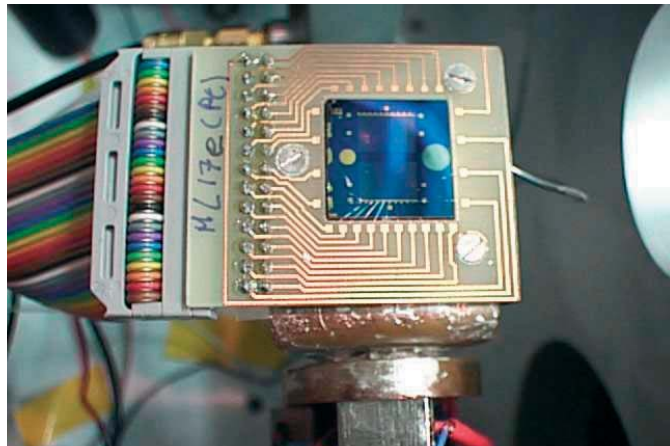


Fig 2
Mounted chip, containing 60 individual detectors

sions on one chip [1]. This chip is mounted onto a chip carrier and bonded with Au wires. Figure 2 shows a finished detector array mounted onto the cold finger of a cryostat, which permits measurements of the electrical properties down to 4 K.
The SiGe quantum wells of the strained layer superlattice samples consist of 10 periods with a nominal thickness of 12 nm for Si and 5 nm for SiGe. They were grown at 600 °C. The desired Ge concentration was up to 50% Ge within the SiGe layers. The stack is sandwiched between two Si buffer layers. The SiGe superlattice is shown in a cross-section micrograph, Fig. 3.

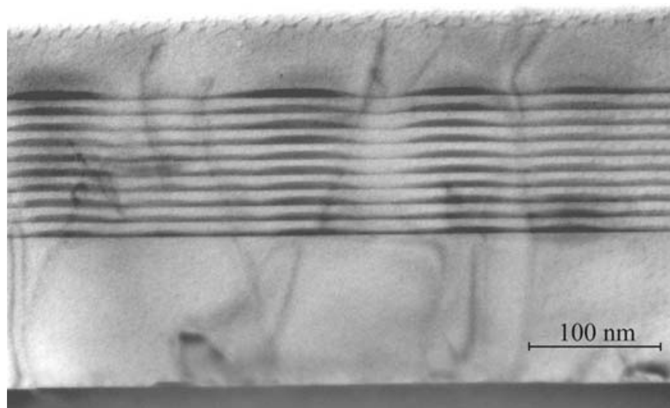


Fig 3
Cross-section micrograph of SiGe undulating layers

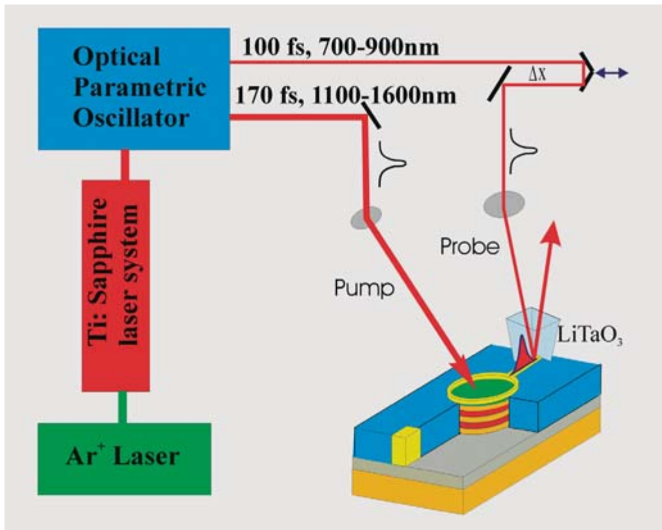
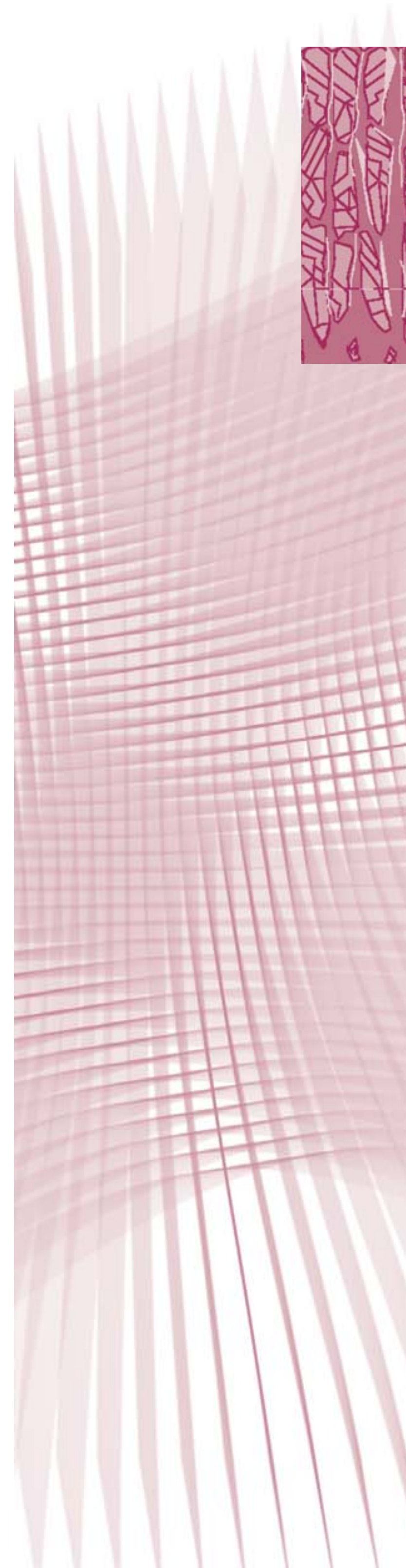


Fig 4
Femtosecond optical characterization setup



It is observed, that the elastic strain in the superlattice leads to an alignment of the Ge-rich volumes, forming undulating layers of self-ordered quantum wells [2].
The temporal response of the devices is measured by an optical femtosecond laser system. The pump-probe geometry is outlined in Fig. 4. For wavelengths of 700-900 nm, a Ti-sapphire laser provides pump and probe pulses of 100 fs full FWHM. The pump light excites carriers in the detector, generating the electrical pulses. The electrical pulses propagate along a microstrip line and pass through an electrooptical sampling crystal. In this crystal, the electrical field of the pulse can be measured optically with the help of a probe pulse, which is delayed by an adjustable amount with respect to the pump pulse. This optical femtosecond pump-and-probe setup provides a better time resolution for ultrafast electrical processes than any other technique. For the IR regime from 1100 nm to 1600 nm, a synchronous optical parametric oscillator is added into the pump beam path. Using nonlinear processes, it is able to emit photons of longer wavelength.

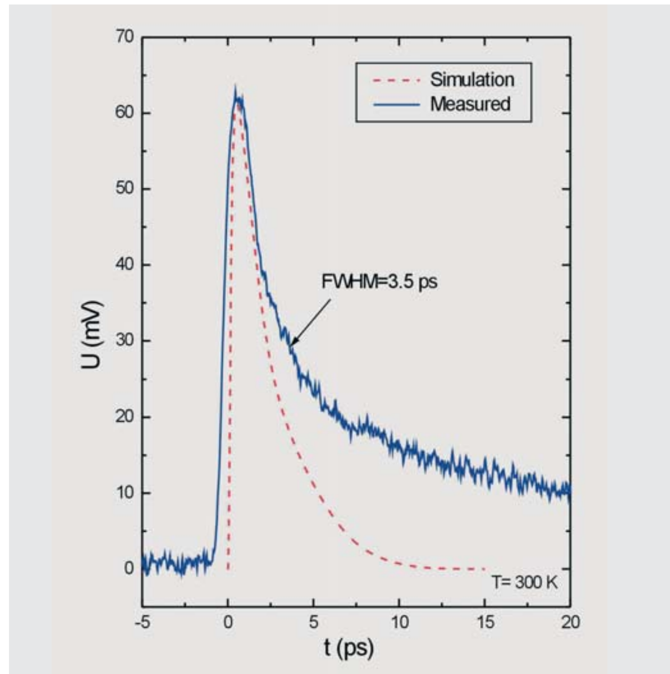


Fig 5
Electrical response from a Si MSM detector

RESULTS

Fig. 5 shows the fast electrical response of a pure Si detector of 360 nm thickness for an optical excitation at a wavelength of 800 nm. We measured an electrical pulse of 3.5 ps FWHM [1]. The applied voltage of 4 V corresponds to 10V/µm and leads to carrier saturation velocities. Higher voltages do not improve the response speed. At the wavelength of $\lambda = 1250$ nm the Si becomes transparent, but hot carriers are still excited across the Schottky barrier into the Si by the internal photo effect, generating even faster pulses, although with a significantly lower quantum efficiency. A record response speed of 1.3 ps FWHM was measured under these conditions, Fig.6 [1].

The quantum efficiency is increased to 5%, if the SiGe superlattice with 39% Ge system is used [2]. The band structure is shown in Fig.7. For a pump wavelength of 1300 nm we observed pulses of 16 ps FWHM. Increasing the Ge concentration to 45%, the superlattice becomes photosensitive at 1550 nm as well. Thinner cap layers together with a superlattice of 340 nm thickness resulted in a pulse response of 9.4 ps at 1550 nm, while providing an acceptable quantum efficiency of 1%, see Fig.8. These

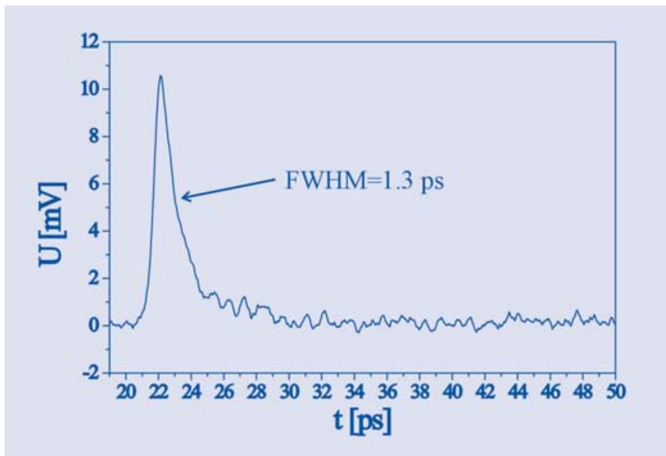


Fig 6
Electrical response from the internal photoeffect at the Schottky barrier of a Si MSM detector

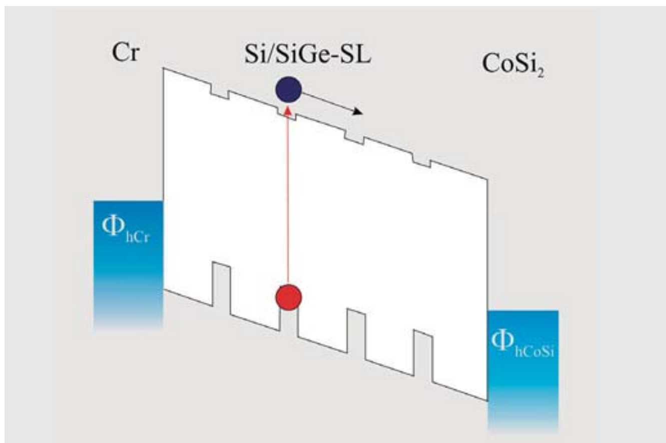


Fig 7
Band structure of the SiGe quantum well detector

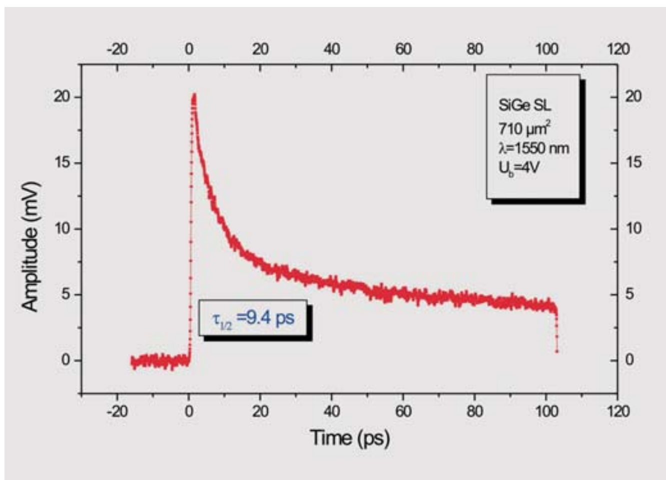


Fig 8
Electrical response from the SiGe quantum well detector

are the fastest pulses ever achieved from SiGe IR detectors. A further increase of the response efficiency is achieved by changing to pure Ge. These devices provided external quantum efficiencies of 13% at 1320 nm and 7.5% at 1550 nm [3]. In this case, the epitaxy was more complex and a different detector design with finger electrodes had to be adopted.

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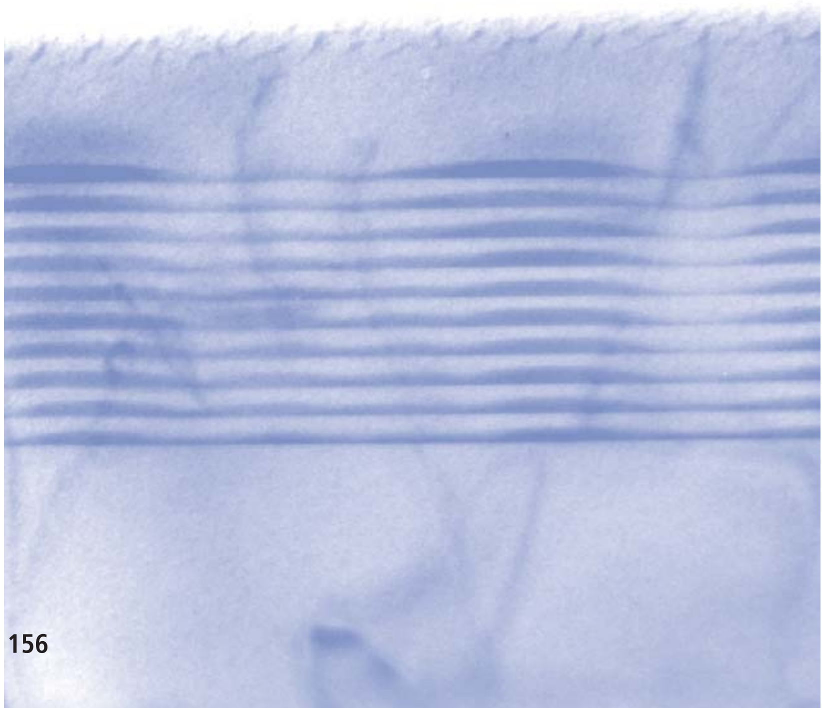

Microcrystalline Silicon Thin Films for Large Area Optoelectronics

INTRODUCTION

Large area thin films of silicon are important for flat panel displays and solar cells. These Si films have to be fabricated by deposition techniques. It is a challenge to optimize the electrical properties while maintaining the necessary low deposition temperatures in order to make the process compatible with low cost glass or plastic substrates. The key material parameters are the nano- and microcrystalline structure of the deposited film and its defect density. We use plasma-enhanced chemical vapour deposition (PECVD) or hot-wire chemical vapor deposition (HWCVD) to fabricate hydrogenated microcrystalline silicon (μc-Si:H) in a large area compatible process. This material is more stable against defect creation under device operation compared to amorphous silicon. Pixel switching by thin film transistors (TFT) in LCD displays benefits from the improved stability in the gate threshold voltage. Already microcrystalline silicon thin film solar cells with record efficiencies of up to 9.4 percent were prepared on a laboratory scale in Jülich [4]. This process was recently scaled up to modules of an area of 30 x 30 cm^2.
Improving the material's properties to device requirements is based on a detailed knowledge of its nanostructure and its electro-optical characteristics.

APPROACH

μc-Si:H films grown by PECVD and hot-wire CVD films were studied in dependence on the key deposition parameters, especially the gas phase dilution of silane in hydrogen. The principal set-up of a glow-discharge PECVD and the hot-wire CVD is shown in Fig. 1. Direct structural investigations by transmission electron microscopy (TEM) were used to study the nucleation on different substrates and the growth in dependence on the PECVD and HWCVD deposition parameters. Short range order was probed by Raman spectroscopy.

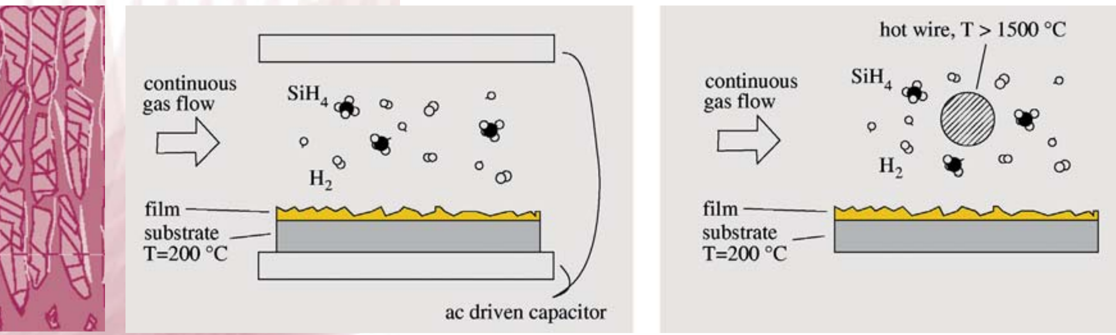

Fig. 1
Plasma enhanced (left) and hot-wire assisted (right) gas phase decomposition of SiH_4 diluted in H_2 employed for the codensation of a hydrogenated silicon film on a substrate at low temperature.

IV-characteristics of solar cells were used to investigate the relation between the structure of the material and it's suitability for device integration.

RESULTS

Nucleation of mc-Si:H

Depending on the substrate, the nucleation of microcrystallites either starts right from the beginning of the deposition or after an initial growth of an amorphous network.
Fig. 2 a and b show cross-section TEM images of 30 nm thin layers grown by PECVD on glass substrates and on a-Si:H substrate under identical conditions. The grain sizes typically remain smaller than a few 10 nm because of the low surface mobility of the film precursors SiH_n at 200 °C. A delayed nucleation of crystallites, represented by bright regions, can be seen on top of the a-Si:H substrate in Fig. 2b. Raman spectra are used to estimate the volume fractions of the amorphous and the crystalline network within the films. The amorphous network gives rise to a broad band TO-Phonon excitation around 480 cm^{-1}, whereas crystalline silicon exhibits a sharp symmetry related TO mode at 520 cm^{-1}. Raman spectra taken from films of different thickness are displayed in Fig. 2. In the case of the a-Si:H substrate, the broad band excitation around 480 cm^{-1} and therefore the amorphous volume fraction dominates up to more than 50 nm of film thik-

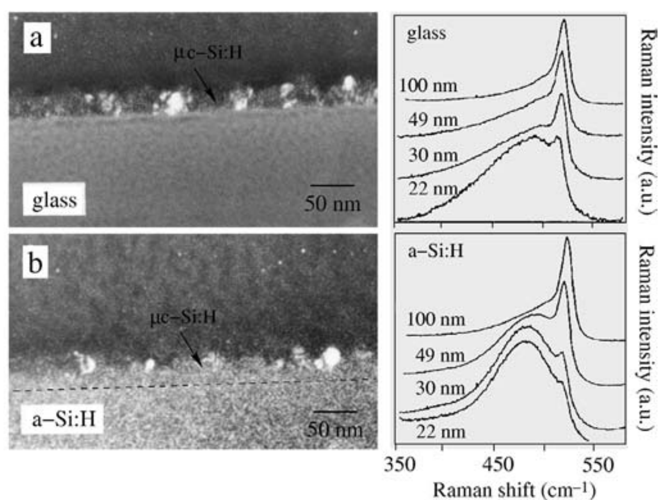

Fig. 2
TEM dark-field images and Raman spectra of several 10 nm thin μc-Si:H layers grown on (a) borosilicate glass and (b) amorphous silicon.

kness. Conclusively, nearly instantaneous nucleation of crystallites is found on glass substrates for the same deposition conditions for that the nucleation is delayed on a-Si:H.
Very high frequency PECVD at plasma excitation frequencies larger than 13.56 MHz and a high hydrogen dilution was shown to be benefical for the crystallization on substrates like a-Si:H [1]. It is advantageous for device fabrication, that the deposition parameters can be adapted to the substrate in order to avoid amorphous channels of poor stability and low doping efficiency in TFTs.

Volume structure of thin μc-Si:H films

Thicker μc-Si:H layers are needed for the efficient optical absorption of red and near infrared light in solar cells. The relative amount of amorphous and crystalline network usually becomes constant at a thickness exceeding approximately 1 mm. The detailed composition then depends mainly on the composition of the process gases. A close relation between the composition and the structural characteristics was found by TEM imaging of numerous PECVD grown films. A schematic representation of these findings is given in Fig. 3 together with cross-sectional TEM images. High crystallinity at strong hydrogen dilution

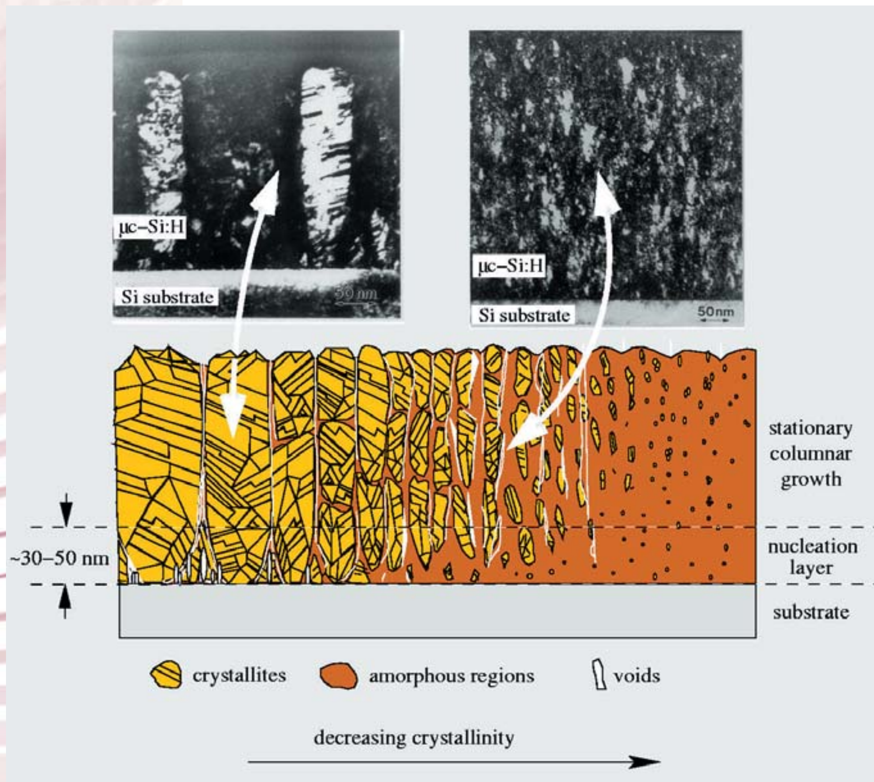

Fig. 3
Schematic representation of the characteristic structural features of µc-Si:H films.

(< 2% SiH_4 in H_2) and high discharge power in PECVD is linked to strong columnar growth of highly twinned grains and porous nucleation layers. A transition to purely amorphous growth is mediated by lowering the hydrogen dilution (typically 10 % SiH_4 in H_2). Upon decreasing crystallinity, more compact films are formed with smaller grain sizes and increased grain boundary volume fraction until finally the amorphous phase appears [2].

Tailored µc-Si:H for solar cell applications

For the preparation of pin thin film solar cells, appropriate conditions were derived from the studies on the nucleation layers in order to prepare thin microcrystalline doped layers with a thickness of less than 30 nm. Amorphous layers are undesirable due

to their non-transparency for blue light and due to a high density of electrically active defects. Moreover, all microcrystalline pin solar cell performance measured by their IV characteristics in dependence on the i-layer deposition parameters shows an efficiency maximum related to a rather small grained material with increased grain boundary fraction for PECVD and for the hot-wire grown material [3,4].
Thus, tailored µc-Si:H differs from poly-Si, where in general the performance increases with grain size. Here, it is primarily the compact material and enhanced grain boundary passivation that enables a higher collection efficiency.

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