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Schottky barrier height enhancement on n-$In_{0.53}Ga_{0.47}As$

P. Kordoš,[a] M. Marso, R. Meyer, and H. Lüth
Institut für Schicht- und Ionentechnik, Forschungszentrum Jülich, W-5170 Jülich, Germany

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Schottky barrier height enhancement on n-InGaAs is studied on structures with thin surface layers of different compositions. Counter-doped p^+-InGaAs layers, as well as layers of n- and p-InP, n-GaAs, and n-InGaP of different thicknesses and dopant densities, respectively, were used to enhance the barrier. Titanium was used as a barrier metal to prepare Schottky diodes of different areas and the barrier height is analyzed by current-voltage measurements. It is observed that the barrier height enhancement by p^+-InGaAs layers increases with the layer thickness and dopant density, respectively, and effective barrier heights up to 0.63–0.68 eV, i.e., higher values than previously reported, have been measured. The barrier height enhancement by counter-doped p^+-InGaAs layers on n-InGaAs can be described by the two-carrier model. Schottky diodes with extremely low reverse current densities have been prepared, $J_R(1\ \text{V}) = 4.5\times10^{-6}\ \text{A/cm}^2$. It is shown that lattice-matched InP surface layers can be used as an alternative to enhance the barrier height on n-InGaAs. The barrier height increases with the layer thickness up to $\phi_B=0.53$–0.55 eV, i.e., up to values previously reported as barrier heights on thick n-InP. Additional barrier enhancement can be achieved by counter doping of the InP surface layer and barrier heights of 0.66 eV have been obtained by p-InP surface layers on n-InGaAs. On structures with barrier-enhanced n-GaAs layers, a remarkable decrease of the reverse current density is observed if the layer thickness is reduced to the critical layer thickness, but the barrier height is very low due to the small n-GaAs thickness. For structures with slightly lattice-mismatched n-InGaP layers ($x_{\text{GaP}}=0.11$) measured barrier heights are similar to those for n-InP enhancement layers of the same thicknesses.

I. INTRODUCTION

Schottky barrier control is an important tool to study the properties of metal-semiconductor interfaces, as well as to optimize the preparation of barrier diodes and gates of field-effect transistors (FET). The Schottky barrier height can be modified by a thin interfacial layer (semiconducting or insulating), which is intentionally incorporated between an active layer of the semiconductor and the barrier metal. In device physics the barrier-enhancement procedure is important for application mainly on one of the most used materials for preparing novel electronic devices on III-V semiconductors, on the ternary solid solution $In_{0.53}Ga_{0.47}As$ (referred to only as InGaAs in the following). By deposition of metals such as Au, Al, Ti, or Nb, the Schottky barrier height on n-InGaAs is low, $\phi_B\simeq0.2$ eV.[1–3] This is in agreement with observed barrier heights of about 0.55 eV on p-type InGaAs,[4,5] since $\phi_B(n)+\phi_B(p)$ amounts to the gap energy $E_g=0.75$ eV. On the other hand, unfortunately, barriers with 0.2 eV are not sufficient for good device operation. For this reason many attempts have been made to enhance the Schottky barrier on n-InGaAs.[6–20] A relatively convenient procedure is the preparation of thin counter-doped p^+-InGaAs surface layers on top of n-InGaAs.[6–8] Another approach consists of the preparation of an interfacial oxidelike layer between the n-InGaAs and the barrier metal.[9–11] Effective barrier heights in the range from 0.38 to 0.54 eV are reported by utilizing these methods. Higher-band-gap materials such as lattice-matched InP[12] and InAlAs,[13] and lattice-mismatched GaAs (Refs. 14 and 15) and AlGaAs (Refs. 16 and 17) were used to enhance the Schottky barrier on n-InGaAs FETs and metal-semiconductor-metal (MSM) photodetectors, but unfortunately no data about the barrier heights are reported. Lattice-mismatched surface layers of InGaP were also used to enhance the barrier. The effective barrier height is $\phi_B=0.4$ eV if the mole fraction of GaP in InGaP is $x=0.49$,[18] and $\phi_B=0.48$–0.50 eV if $x=0.25$.[19] In most of the reported results concerning barrier enhancement on n-InGaAs, the prepared Schottky diodes unfortunately exhibit nonideal behavior (ideality factor n and reverse current densities J_R are relatively high). Nearly ideal quasi-Schottky diodes or n-InGaAs ($n=1.1$, $J_R=10^{-4}$ A/cm^2) with effective barrier heights enhanced by counter-doped layers up to 0.6 eV are described in our recent communication.[20]

The present paper reports a detailed study of Schottky barrier enhancement on n-type InGaAs. In order to investigate the enhancement conditions at the metal-InGaAs interface we have grown thin surface interlayers of different compositions. Counter-doped p^+-InGaAs layers, as well as lattice-mismatched n- and p-type InP, lattice-mismatched n-GaAs and n-InGaP layers, with different thicknesses and dopant densities, respectively, were grown by low-pressure metal-organic vapor-phase epitaxy (MOVPE). The electrical behavior of the prepared quasi-Schottky diodes is analyzed by means of current-voltage (I-V) measurements at room temperature, as well as by I-V measurements at different temperatures (I-T). The

[a]Permanent address: Institute of Electrical Engineering, Slovak Academy of Sciences, CS-84239 Bratislava, Czechoslovakia.

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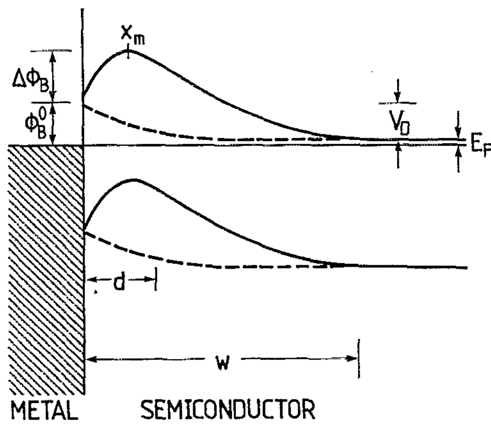

FIG. 1. Energy-band diagram of a metal n-type semiconductor contact with a counter-doped surface layer.

Schottky barrier height ϕ_B, together with the ideality factor n, series resistance R_s, and reverse current density J_R (1 V) are used as characteristic measures of the prepared devices.

II. SCHOTTKY BARRIER ENHANCEMENT

A. Enhancement by counter-doped surface layers

The idea to modify the Schottky barrier height on semiconductors by band bending due to space charge in a thin surface layer has been known for a long time. In 1974 Shannon showed that the Ni-silicon barriers can be enhanced[21] (or reduced[22]) using counter-doped (or isotype highly doped) ion-implanted layers by an amount in the range of 0–0.25 eV. This method was later applied to other semiconductors, e.g., to CdS,[23] GaAs,[24–26] InP,[27] and InGaAs.[6–8,20] On n-GaAs with the unmodified Schottky barrier height of $\phi_B^0=0.8$ eV reduced or enhanced barriers $\phi_B=\phi_B^0+\Delta\phi_B$ in the range from 0.49 to 1.24 eV were achieved.[24] On n-InGaAs actually only enhanced barriers are needed since the preparation of ohmic contacts is not difficult.[28]

There are three different theoretical approaches to Schottky barrier enhancement by counter-doped surface layers, all based on the solution of the Poisson's equation under zero-bias conditions, but using different approximations. The best-known model of Lubberts *et al.*,[23] later specified by other authors,[29–33] is based on the depletion approximation in highly doped surface layers. The increase of the Schottky barrier on n-type semiconductors (Fig. 1) with dopant density N_D by a p-type surface layer with dopant density N_A and thickness d, respectively, is described in simplified form[34] as

$$\Delta\phi_B=(q/2\epsilon_s)N_A d^2, \qquad (1)$$

where q is the elementary charge and $\epsilon_s=\epsilon_r\epsilon_0$ is the dielectric constant of the semiconductor. Equation (1) is valid if $N_A \gg N_D$ and $N_A d \gg N_D(w-d)$, where w is the depletion region thickness. These conditions are mostly fulfilled for experiments of Schottky barrier enhancement. However, from Eq. (1) it follows that barrier heights exceeding the band-gap energy should easily be obtained, e.g., with $N_A=1\times10^{18}$ cm^{-3} and $d>30$ nm the barrier enhancement will be $\Delta\phi_B>0.65$ eV and then the barrier height $\phi_B=\phi_B^0+\Delta\phi_B$ on n-InGaAs will be higher than 0.85 eV. On the other hand, such extremely high barrier enhancement by counter-doped surface layers was experimentally not confirmed.

Roy and Daw[35] have analyzed the barrier enhancement considering the presence of an inversion space-charge layer at the p/n interface, i.e., the existence of holes in the region $x>d$ was included. According to this assumption, the Schottky barrier enhancement can be described by Eq. (1) with the difference that instead of the thickness d only the effective thickness $(d-x_m)$ must be used, where x_m is the distance from the p/n interface toward the surface where the energy-band maximum is located (Fig. 1). An analytical expression for x_m can unfortunately not be given, since one has to solve two coupled equations. However, qualitatively one might infer that owing to the accumulated charge in the inversion layer the energy maximum x_m shifts further from the p/n interface toward the surface with increasing p^+-layer thickness. This is different from the depletion-layer model, where the energy maximum shifts with increasing p^+-layer thickness in the opposite direction and is located very close to the p/n interface (therefore x_m is neglected in this case). If one uses the effective thickness $(d-x_m)$, a saturation of the barrier height with increasing layer thickness or dopant density is predicted, but still unrealistically high barrier heights are obtained. According to the inversion-layer model, enhanced barriers should vary with bias since x_m is field dependent and the ideality factor n should increase with the p^+-layer thickness.[35]

Schwartz and Gualtieri[36] have solved Poissson's equation numerically including both electron and hole carriers in metal-p^+-n Schottky structures on InP, GaAs, and InGaAs. From their "two-carrier" model it follows that at low dopant densities or thicknesses of a p^+-layer the barrier enhancement can be expressed by Eq. (1), but at higher values of N_A or d the effective barrier height will saturate at the band-gap energy of the semiconductor, i.e., $\phi_B \simeq E_g$. The dependence of the barrier enhancement on the p^+-layer dopant density according to the two-carrier model in comparison with depletion and inversion models (as given in Ref. 36 for the case of n-InP) is shown in Fig. 2.

Unfortunately, no published data exist with respect to an experimental verification of described models of Schottky barrier enhancement. Mostly, only one dopant density or one thickness of the surface layer was used in the experiments on InGaAs. Chen *et al.*[6] and Kim and coworkers[7] have used the MBE technique to grow thin highly doped p^+-layers on n-InGaAs. In the former work, Be-doped layers with $N_A=8\times10^{18}$ cm^{-3} and $d=8$ nm were grown and quasi-Schottky diodes with an effective barrier height of 0.47 eV were prepared. In the latter work, the barrier height of 0.52 eV was obtained on samples with $N_A=1\times10^{18}$ cm^{-3} and $d=30$ nm. Recently, we have reported quasi-Schottky diodes on n-InGaAs with p^+-layer

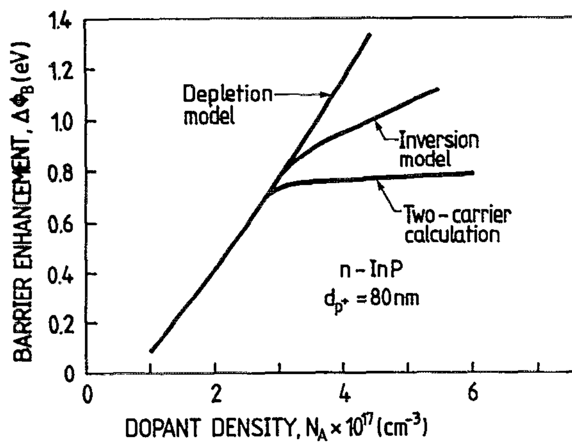

FIG. 2. Barrier height enhancement on n-InP by a p^+-InP surface layer according to the depletion model, the inversion model, and the two-carrier calculation, as given in Ref. 36.

parameters similar to Kim and co-workers' investigations ($N_A=1.5\times10^{18}$ cm^{-3}, $d=30$ nm) and with the barrier height of 0.6 eV.[20] Our structures differed from Kim and co-workers' in that we have grown an n^+-InGaAs layer between the n^+-InP substrate and n-InGaAs active layer to avoid the possible rectification at the InGaAs/InP interface. Eglash *et al.*[24,25] have prepared a series of quasi-Schottky diodes on n-GaAs with enhanced barriers by p^+ layers of different thicknesses up to 36 nm. They report good agreement between experimental values of enhanced barrier heights and theoretical ones calculated by the inversion model, but for a given dopant density $N_A=1\times10^{18}$ cm^{-3} the p^+-layer thicknesses are in the range where the barrier enhancement $\Delta\phi_B$ has the same values for all described models. Actually, Schwartz and co-workers[27,36] were not able to compare experimentally obtained enhanced barriers on n-InP with their model because of small p^+ thicknesses produced by Zn diffusion.

B. Enhancement by surface layers of different composition

A well-known method to enhance the Schottky barrier height is by an insulating interfacial layer. The dependence of the Schottky barrier enhancement on the thickness of an insulating surface layer was described on the basis of a tunneling model.[37] The barrier height according to this model is proportional to the layer thickness d, i.e.,

$$\phi_B=\phi_B^0+Dd, \tag{2}$$

where D is a material constant, depending on the electron effective mass in the semiconductor (in n-InGaAs D is about 1×10^6 V/cm). Morgan and Frey[9] have used a 10-nm-thick SiO_x layer to enhance the barrier height on n-InGaAs up to $\phi_B=0.49$ eV. Similarly, Chan *et al.*[10] and Licata *et al.*[38] have used a Cd-based organic complex as a thin dielectric layer on n-InGaAs; they could obtain enhanced barriers with $\phi_B=0.52$ eV. All these values are lower than those predicted by the tunneling model. However, the application of dielectric interlayers to high-speed devices[39] might be accompanied by interface-state formation and by possible degradation of the device performance.

A modification of the Schottky barrier height is also possible by heteroepitaxial growth of a thin semiconducting surface layer of different band gap on top of the n-InGaAs. The effective barrier height will be increased owing to the band-gap discontinuity if an isotype layer of higher E_g is used and/or by band bending produced by counter doping in this heterolayer. The barrier height enhancement by higher-band-gap layers was first reported by Yang *et al.*[40] On n-GaAs they have used undoped lattice-matched liquid-phase epitaxy (LPE) and molecular-beam epitaxy (MBE) -grown n-AlGaAs layers of different compositions and with thicknesses up to 70 nm; effective barrier heights up to 1.19 eV were obtained. Even if by LPE growth thin AlGaAs layers can be grown, e.g., under isothermal conditions,[41] such layers exhibit a compositional grading in the growth direction. Recently, barriers on GaAs enhanced by counter-doped Si layers (i.e., by lower-band-gap surface layers) were reported.[42]

The theoretical description of Schottky barrier enhancement by surface heterolayers is more complicated than that by simple counter-doped homolayers. Barrier enhancement depends not only on the thickness and dopant density of the surface layer, but also on the band-gap discontinuity at the heterointerface. Additionally, if a lattice-mismatched surface layer is used, the critical thickness for pseudomorphic growth[43,44] should be considered. Yang *et al.*[40] assumed that the Fermi level remains pinned at about $\frac{2}{3}$ of the direct band-gap energy of AlGaAs, i.e., for $x<0.45$,

$$\phi_B=\phi_B^0+\Delta\phi_B=\tfrac{2}{3}E_g^\Gamma, \tag{3a}$$

and for $x>0.45$,

$$\phi_B=\phi_B^0+\Delta\phi_B=E_g^X-\tfrac{1}{3}E_g^\Gamma, \tag{3b}$$

where E_g^Γ and E_g^X are the direct and indirect band-gap energies of AlGaAs, respectively. However, in this assumption, the experimentally observed dependence of the barrier height on the AlGaAs thickness and doping density were not taken into account. On the other hand, some doubts about the Fermi-level pinning were recently published,[45] which might modify the picture.

One might expect that the barrier height on n-InGaAs enhanced by higher-band-gap surface layers should be proportional to the conduction-band discontinuity ΔE_c at the heterointerface,

$$\phi_B=\phi_B^0+\Delta E_c. \tag{4}$$

Unfortunately, there is a wide spread in the published values of ΔE_c at the InP/InGaAs interface ranging from 0.24 to 0.36 eV.[46] There is also the question of how the thickness of a heterolayer will influence the barrier enhancement. Eizenberg *et al.*[47] have analyzed the metal-AlGaAs barriers prepared on n-GaAs and they have obtained a good correlation between the barrier height and the conduction-band discontinuity at the GaAs/AlGaAs inter-

barrier metal

BARRIER ENHANCED LAYER

n-InGaAs	<2×10^{15} cm^{-3}	2 μm
n$^+$-InGaAs	3×10^{18} cm^{-3}	200 nm
n$^+$-InP	3×10^{18} cm^{-3}	300 nm
n$^+$-InP substrate	3×10^{18} cm^{-3}	

FIG. 3. Basic structure of InGaAs quasi-Schottky diodes used in the experiments.

face for different AlGaAs compositions; but, this has only been observed on structures with a AlGaAs thickness of $d=500$ nm.

Not enough data are available to evaluate published results of the barrier enhancement by higher-band-gap surface layers and, in some cases, layers with thicknesses exceeding the critical layer thickness for pseudomorphic growth were used.

III. EXPERIMENTAL PROCEDURES

A. Structure preparation

Multilayered structures with barrier-enhanced surface layers were grown on (100)-oriented n^+-InP substrates by conventional low-pressure MOVPE equipment using growth conditions that provide high-quality InGaAs layers.[48] Basic structures consisted of the following layers (Fig. 3): On an n^+-InP substrate at first an n^+-InP buffer layer was grown (3×10^{-18} cm^{-3}, 300 nm), then an n^+-InGaAs layer (3×10^{18} cm^{-3}, 200 nm) to avoid possible rectification at the n^+-InP/n-InGaAs interface, followed by an active n-InGaAs layer ($<2\times10^{15}$ cm^{-3}, 2 μm) and finally by a barrier-enhanced layer of different composition. To study the barrier enhancement by counter-doped surface layers, zinc-doped p^+-InGaAs was used (about the low Zn diffusion in InGaAs see bellow) with different doping levels, $N_A=(1.5\text{–}8)\times10^{18}$ cm^{-3}, and different thicknesses, $d=8\text{–}80$ nm, respectively. Additional lattice-matched layers of n-InP (2×10^{15} cm^{-3}, 8, 30, and 60 nm) and p^+-InP (2×10^{18} cm^{-3}, 30 nm), as well as lattice-mismatched undoped n-InGaP with a mole fraction of GaP ($x=0.11$) were grown. The thickness of the InGaP layers was 8 nm, which should be below the critical layer thickness for given lattice mismatch. In order to study the influence of the layer thickness on the barrier enhancement, we have also grown one structure with an extended surface region, a structure with a 60-nm-thick InP/InGaP multiquantum well (10 periods of 3 nm InP and 3 nm InGaP). Finally, highly lattice-mismatched undoped n-GaAs layers with different thicknesses in the range from 2 to 100 nm were also grown on top of the n-InGaAs. The quality of the thin surface layers was evaluated by scanning electron microscopy and x-ray diffractometry.

B. Zinc diffusion in InGaAs

It is known that zinc is a rapidly diffusing element in III-V materials. Impurity-induced disordering effects that may occur at heterointerfaces during the acceptor diffusion[49] can therefore negatively affect the properties of the prepared samples with p^+-InGaAs surface layer, mainly when very thin and highly doped layers are needed for the effective barrier enhancement in device applications. However, unintentional diffusion of acceptors during the growth should be 2–3 orders of magnitude slower than the intentional doping of InP by indiffusion.[50] Recently, Wielsch, Ambrée, and Gruska have studied the diffusion of Zn in InGaAs from the gas phase,[51] as well as across the InGaAs/InP and InP/InGaAs interfaces.[52] They have observed that the diffusion from the p-InP top layer into the n-InGaAs has no measurable influence on the stability of the interface. Unfortunately, there are not published data about the solid diffusion from p-InGaAs into n-InGaAs, but we might assume a similar behavior. In order to control this assumption, we have annealed part of the prepared structure with a p^+-InGaAs layer (1.5×10^{18} cm^{-3}, 8 nm) at 640 °C for 15 s (the T-t profile was the same as that of the 8-nm-thick p^+ layers). A sample with this thickness was chosen since variations of the barrier enhancement due to eventual broadening of the p^+ region respond sensitively just in this region, as will be shown later. By comparison of the Schottky diode parameters obtained on annealed and unannealed structures, we have not observed differences in the evaluated values of n, ϕ_B, and J_R. This is also in agreement with simple estimation using data of the diffusion coefficient of Zn in InGaAs from the gaseous phase.[51] Assuming at least 100 times slower diffusion from the solid source, the calculated diffusion depth of Zn during the growth of 8-nm-thick p^+ layer will be only $x_j=0.4$ nm, i.e., less than the accuracy of the thickness determination.

C. Schottky diode characterization

The quasi-Schottky diodes were prepared by electron-beam evaporation of a barrier metal, followed by standard optical lithography and mesa etching procedures. Titanium was used in experiments reported here and evaporation was done on a room-temperature surface. For comparison platinum and aluminum were also used on some structures, but in contrast to the result on InAlAs (Ref. 53) we have not observed differences in the barrier height. Using a lift-off technique Schottky diodes with five different areas (squares with a side length of 10, 25, 50, 100, and 250 μm) were fabricated on all-prepared layer structures. After rapid thermal annealing for 10 s at a temperature of 320 °C (the usual sintering procedure for ohmic contacts) no degradation of the diode parameters was observed. Current-voltage characteristics at stabilized temperatures in the range from 10 to 100 °C were then measured by supplying a voltage to the diode with a programmable voltage source and measuring the current through the diode with an elec-

trometer in the range from 10^{-12} to 10^{-2} A. Measurements at increased, as well as decreased, temperatures in the whole temperature range were still made, but no difference between these two procedures were observed. All measurements were automated with a PC/AT microcomputer.

Schottky barrier diodes on low-doped n-InGaAs exhibit current transport over a potential barrier which can be described by the thermionic-emission equation[34]

$$J=J_s\{\exp[q(V-IR_s)/nkT]-1\}, \quad (5)$$

where the saturation current density J_s (current density extrapolated to zero bias) can be expressed as

$$J_s=A^*T^2\exp(-q\phi_B/kT). \quad (6)$$

Equations (5) and (6) can be used to evaluate the Schottky barrier height $\phi_B^{I\text{-}V}$. Here V is the bias voltage, I the total current, R_S the series resistance, and A^* the effective Richardson constant ($A^+=5.04$ A/cm^2 K^2 in n-InGaAs).[3] The ideality factor n should be equal to one according to thermionic emission theory and if remarkable deviations occur then other mechanisms are responsible for the current transport, e.g., tunneling through the barrier, recombination in the space-charge region, etc.[34]; but, this is not the case for our structures as will be shown in the following section.

Another approach to determine the Schottky barrier height used in this study is based on the thermal activation energy method,[34] i.e., by measurement of I-V characteristics at different temperatures and using a plot of $\ln(J_s/T^2)$ as a function of the reciprocal temperature. The barrier height $\phi_B^{I\text{-}T}$ is obtained from the slope of this dependence according to Eq. (6).

In most prepared devices, the current values of different diodes on the same structure were found to scale with their area resulting in area-independent values of current density. For the evaluation of our data we have numerically fitted the measured I-V characteristics in order to determine the ideality factor n, series resistance R_s, and barrier height ϕ_B.

IV. RESULTS AND DISCUSSIONS

A. Schottky barrier enhancement by p^+-InGaAs surface layers

A series of quasi-Schottky diodes on n-InGaAs with counter-doped p^+-InGaAs surface layers was prepared with the aim to study the influence of the surface layer thickness on the barrier enhancement. The thickness of the p^+ layers was therefore varied in the range from 8 to 80 nm at constant dopant density, $N_A=1.5\times10^{18}$ cm^{-3}. Typical room-temperature I-V characteristics of prepared quasi-Schottky diodes on n-InGaAs with different p^+ layer thicknesses are presented in Fig. 4. Schottky barrier heights $\phi_B^{I\text{-}V}$, together with other characteristic parameters of the prepared diodes, are summarized in Table I (presented data are mean values of our measurements on samples with different contact areas). From I-T measurements somewhat higher barrier heights $\phi_B^{I\text{-}T}$ were obtained, but

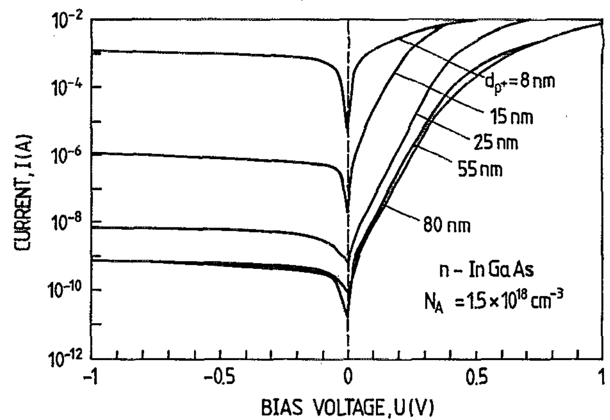

FIG. 4. I-V characteristics of n-InGaAs quasi-Schottky diodes with p^+-InGaAs surface layers of different thicknesses.

with a similar dependence on the p^+-layer thickness. Schottky diodes with a p^+-layer thickness of only 8 nm exhibit high leakage currents and the barrier height is low, $\phi_B=0.26$ eV. However, this is in agreement with the expected barrier enhancement according to Eq. (1). The reverse current decreases remarkably as the p^+-layer thickness increases and on samples with p^+-layer thicknesses of 55 and 80 nm reverse current densities are only J_R (1 V)$=3\times10^{-5}$ A/cm^2. All I-V characteristics of diodes with a p^+-layer thicknesses $d>15$ nm exhibit a linear portion in a $\log(I)$-U plot at least in four orders of current. The ideality factor n is near unity with expected slow increase with the p^+-layer thickness, $n=1.08$ at $d=15$ nm and 1.26 at 80 nm. The quasi-Schottky diodes with p^+-layer thicknesses between 35 and 80 nm exhibit barrier heights in the range 0.61–0.63 eV, i.e., they reach higher values than reported until now on n-InGaAs. Enhanced Schottky barriers are dependent on electric field and that might be a disadvantage for device applications of such structures. From our measurements it follows that this effect is more apparent for higher barrier heights, but the maximal decrease of the barrier from zero to $U_R=2$ V is only about 10%.

TABLE I. Characteristic parameters of the quasi-Schottky diodes on n-InGaAs with counter-doped p^+-InGaAs surface layers of different thicknesses and dopant densities.

d (nm)	$N_A\times10^{-18}$ (cm^{-3})	J_R (1 V)$\times10^3$ (A/cm^2)	n	ϕ_B (eV)
8	1.5	1000	···	0.26
15	1.5	3	1.08	0.47
20	1.5	0.8	1.12	0.56
25	1.5	0.5	1.08	0.59
35	1.5	0.1	1.16	0.61
55	1.5	0.03	1.20	0.63
80	1.5	0.03	1.26	0.63
30	1.5	0.2	1.14	0.60
30	4	0.03	1.17	0.63
30	8	0.006	1.12	0.66
60	8	0.0045	1.15	0.68

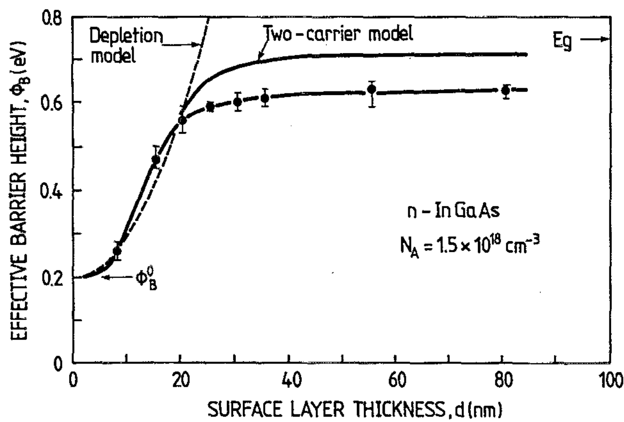

FIG. 5. Schottky barrier height on n-InGaAs as a function of the thickness of the p^+-InGaAs surface layer.

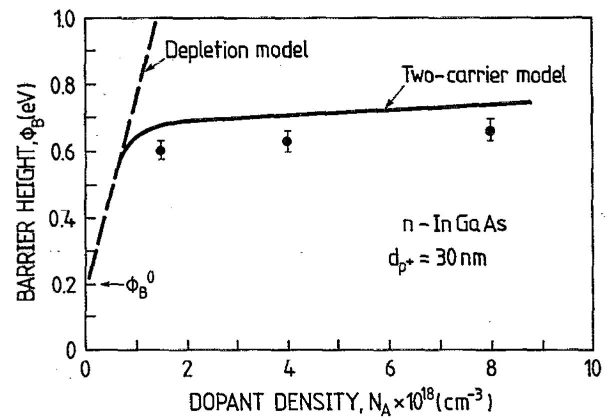

FIG. 6. Schottky barrier height on n-InGaAs as a function of the dopant density of the p^+-InGaAs surface layer.

In Fig. 5 the dependence of the effective barrier height on the p^+-layer thickness, as determined by our experiments, is compared with theoretical dependencies according to the depletion and two-carrier models ($N_A=1.5\times10^{18}$ cm^{-3}). At lower thicknesses, $d<20$ nm, the barrier enhancement depends on thickness almost quadratically, $\Delta\phi_B\simeq d^2$. At a p^+-layer thickness of 20 nm, our experimentally determined dependence of ϕ_B vs d starts to deviate remarkably from the depletion calculation using Eq. (1). On the other hand, it is in agreement with the two-carrier model, since the barrier height should begin to deviate from the depletion model at the certain "critical" barrier height $\phi_B^*=CE_g$, where C is a material constant, $C\simeq0.8$ in n-InGaAs.[36] From our experimental data it follows that $C=0.75$. With further increase of the p^+-layer thickness the barrier enhancement becomes saturated and the Schottky barrier height reaches a value of about 0.63 eV. As follows from Fig. 5, our results are qualitatively in good agreement with the two-carrier model.[36] From detailed analysis[54] of Eglash *et al.*'s[24] results concerning the barrier enhancement on n-GaAs by counter-doped p^+-GaAs layers with different thicknesses a tendency of barrier height saturation for $d>30$ nm can also be found. This can be expected because the measured barrier height of 1.12 eV for a 36.1-nm-thick p^+-layer is higher than $\phi_B^*=CE_g=1.06$ eV if $C=0.75$.

In order to study the effect of the dopant density of the counter-doped p^+ layer on the Schottky barrier enhancement we have prepared diodes on n-InGaAs with three different acceptor densities in enhancement layers, $N_A=1.3$, 4, and 8×10^{18} cm^{-3}. The p^+-layer thickness was 30 nm in all these structures, i.e., thickness in the saturated region of the ϕ_B vs d dependence was chosen. Characteristic parameters of these quasi-Schottky diodes on n-InGaAs are given in Table I. Extremely low reverse current density, $J_R(1\text{ V})=5.8\times10^{-6}$ A/cm^2, an ideality factor $n=1.12$, and an effective Schottky barrier height of 0.66 eV were achieved on structures with the p^+-layer doped to $N_A=8\times10^{18}$ cm^{-3}. Theoretical dependencies of the $\phi_B=f(N_A)$ according to the depletion and the two-carrier models together with our experimental values of the effective barrier height are shown in Fig. 6. In spite of only three data points we can imagine the correlation of the experiment with the two-carrier model. If the p^+-layer thickness is greater than 30 nm, only a small increase of the barrier height occurs at the same dopant density $N_A=8\times10^{18}$ cm^{-3}, as might be expected. Barrier heights of 0.68 eV were measured on structures with 60-nm-thick p^+ layers (Table I).

B. Schottky barrier enhancement by heteroepitaxial growth of an InP, GaAs, or InGaP layers

In view of the technological processes involved in preparation of barrier-enhanced highly doped p^+-layers, some arguments can be found against the use of an acceptor in the surface layer, e.g., memory effects in the growth equipment might influence the ability to reproducibly grow pure and uncompensated layers. The heteroepitaxial growth of an undoped material with higher band gap is a good alternative for this purpose. In the case of InGaAs, there are several different appropriate choices of materials. InP is the simplest candidate due to its lattice matching to InGaAs. According to Eqs. (3) and (4), higher-band-gap materials will be preferred, therefore InAlAs lattice matched to InGaAs ($E_g=1.45$ eV at $x_{\text{InAs}}=0.52$) is another possibility for barrier enhancement. Schottky barrier heights of $\phi_B=0.56$–0.72 eV were measured on diodes prepared directly on n-InAlAs,[55] in comparison with $\phi_B=0.48$–0.55 eV measured on n-InP.[56] However, air oxidation of Al-rich materials together with the presence of deep traps at the InAlAs/InGaAs interface[57] might be an obstacle for device preparation. Lattice-mismatched surface layers are the next category of materials for Schottky barrier enhancement. In the past, GaAs barrier-enhanced layers were grown on top of InGaAs,[14,15] but due to the high lattice mismatch between these two materials ($\Delta a/a=3.7\%$) it might be difficult to prepare Schottky diodes with reasonable parameter from such structures. InGaP might be a good compromise because one can adjust both the bandgap and the lattice mismatch by changing the composition.

TABLE II. Characteristic parameters of quasi-Schottky diodes on n-InGaAs with InP and InGaP ($x_{GaP}=0.11$) surface layers.

Surface layer	d (nm)	J_R (1 V)$\times 10^3$ (A/cm^2)	n	ϕ_B^{I-V} (eV)	ϕ_B^{I-T} (eV)
n-InP	8	80	1.04	0.42	0.38
n-InP	30	8	1.12	0.48	0.49
n-InP	60	1	1.22	0.53	0.55
p-InP	30	0.03	···	0.66	···
n-InGaP	8	90	1.08	0.40	0.40
n-InGaP	60[a]	3	1.26	0.50	0.51

[a]Multiple quantum well of 10 periods of 3 nm InP and 3 nm InGaP.

However, one would have to consider the conditions of pseudomorphic growth.

Characteristic parameters of prepared quasi-Schottky diodes on n-InGaAs with barrier-enhanced undoped n-InP surface layers are summarized in Table II. Typical I-T characteristics of these diodes with n-InP layer thicknesses of 8, 30, and 60 nm are shown in Fig. 7. Measured Schottky barrier heights ϕ_B^{I-V} and ϕ_B^{I-T} are in good agreement. We observed that the barrier enhancement for the n-InP as a function of layer thickness is similar to the enhancement by counter-doped p^+-InGaAs layers and leads to barrier heights of 0.53–0.55 eV (Fig. 8). Higher barriers, as suggested by Eq. (2) for insulating enhancement layers, cannot be obtained although the n-InP layer is undoped and nearly intrinsic. Measured barrier heights can only roughly be compared with expected values using Eq. (4), due to a wide spread in published values of the conduction-band discontinuity at the InP/InGaAs interface. Considering $\Delta E_c=0.24$–0.36 eV,[46] the enhanced barrier height should be in the range between 0.44 and 0.56 eV. On the other hand, we can assume that with the increase of the n-InP layer thickness the barrier height should approach values measured directly on "thick"

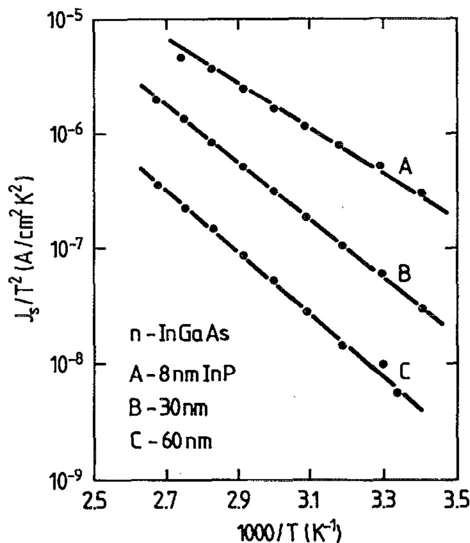

FIG. 7. I-T characteristics of n-InGaAs quasi-Schottky diodes with n-InP surface layers of different thicknesses.

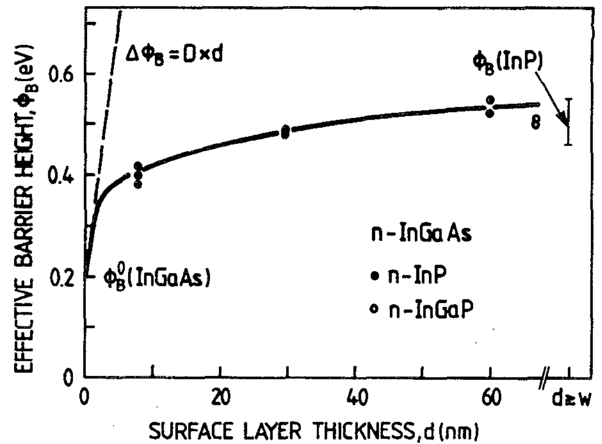

FIG. 8. Schottky barrier height on n-InGaAs as a function of the thickness of the n-InP and n-InGaAs ($x_{GaP}=0.11$) layers.

n-InP. In this case our barrier heights of 0.53–0.55 eV are in agreement with barrier heights of $\phi_B=0.48$–0.55 eV reported on n-InP.[56]

More efficient barrier enhancement on n-InGaAs should be obtained by p-type InP surface layers, since the barrier height will be enhanced simultaneously by conduction-band discontinuity at the InP/InGaAs interface and by band bending in the counter-doped p^+-layer. We have observed this additional barrier enhancement on structures with 30-nm thick p^+-InP surface layers. Instead of using undoped n-InP, a p^+-InP surface layer with a dopant density $N_A=2\times 10^{18}$ cm^{-3} was used and the effective barrier height was increased from 0.48 to 0.66 eV (Table II). However, if we compare this result with the barrier height of 0.60 eV measured on samples with a p^+-InGaAs enhancement layer of similar thickness and dopant density, respectively, one would expect a higher barrier-height enhancement with a p^+-InP layer due to the simultaneous contributions from the conduction-band discontinuity and the band bending.

Another series of prepared quasi-Schottky diodes on n-InGaAs was with undoped n-GaAs surface layers of different thicknesses in the range from 2 to 300 nm. In published works dealing with GaAs as a barrier-enhancement layer on n-InGaAs Schottky diodes[14,15,58] only reverse currents of prepared diodes are given, without data about the barrier height. The n-GaAs thickness was in the range from 58 to 300 nm. Only Chakrabarti *et al.*[59] have reported forward current properties with an ideality factor $n>2$ on structures with an extremely thick n-GaAs layer, $d=1$ μm. On structures with n-GaAs thicknesses of 10, 50, 100, and 300 nm we have obtained similar results with decreased reverse current densities with increased layer thicknesses, e.g., $J_R(1\text{ V})=10^2$ A/cm^2 for $d=10$ nm and 5×10^{-4} A/cm^2 for 300 nm. A good correlation is found between the reverse current densities and GaAs layer thicknesses using data from our experiments as well as from recent literature as is shown in Fig. 9 (dashed line). At the interface of a relaxed GaAs layer grown on an InGaAs layer a high number of edge dislocations and threading dislocations are

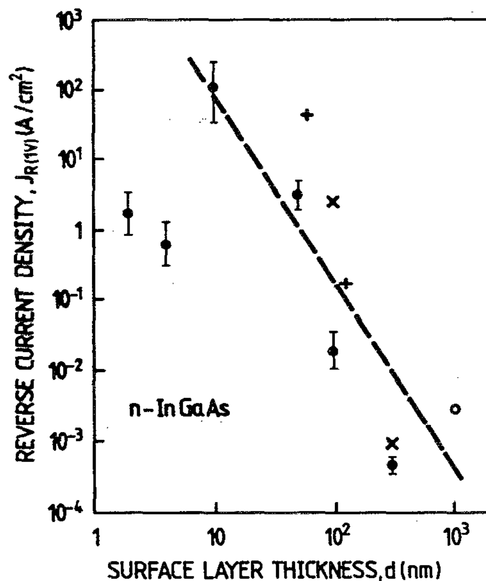

FIG. 9. Reverse current density of n-InGaAs quasi-Schottky diodes with n-GaAs surface layers of different thicknesses (●: our data; +: Ref. 14; ×: Ref. 58; ○: Ref. 59).

created and with increased thickness of the GaAs layer the number of these defects decreases. The critical layer thickness for the pseudomorphic growth of GaAs on InGaAs is in the range of d_c=2–6 nm, depending on the applied theory;[43,44] therefore, we have grown structures with n-GaAs thicknesses of 2 and 4 nm. As an illustration the "best" I-V characteristics of structures with extremely thick, relaxed n-GaAs and pseudomorphic n-GaAs layers are shown in Fig. 10. We have observed a reduction of the current density (Fig. 9), but due to the thin GaAs layer the barrier height is very low. On the other hand, it is in contradiction with results of Loualiche *et al.*,[60] where the Schottky barrier on n-InP was enhanced from 0.43 to 0.80 eV with a 1.1 nm GaP surface layer and the diodes exhibited ideal behavior, n=1.08.

In order to use higher-band-gap material than InP to enhance the Schottky barrier on n-InGaAs and to overcome the problems connected with the application of high-lattice-mismatched GaAs, InGaP surface layers might be used. We can choose the composition and the thickness of InGaP to obtain optimal conditions for the preparation of a barrier-enhanced layer. We have used undoped n-InGaP with a mole fraction of x_{GaP}=0.11 (the band-gap energy is the same as for GaAs) and with a thickness of 8 nm (the critical layer thickness is about 12 nm due to the lower lattice mismatch of InGaP than of GaAs on InGaAs). The ideality factor on prepared diodes is n=1.08 and the effective barrier height of ϕ_B=0.40 eV was obtained from I-V and I-T measurements. We have also prepared structures with an extended InGaP surface region in order to study the possibility of higher barrier enhancement by thicker surface layers, as it follows from our observations on structures with n-InP surface layers. In order to overcome the limitation of the critical layer thickness, we grew 60-nm-thick multiquantum wells of InP/InGaP (10 periods of 3 nm InP and 3 nm InGaP) on top of the n-InGaAs and obtained barrier heights of ϕ_B=0.50–0.51 eV (Table II). According to these results, the barrier height obtained using n-InGaP enhancement layers on n-InGaAs is practically the same as using n-InP surface layers, probably because of small differences between InP and InGaP (x_{GaP} =0.11) band-gap energies.

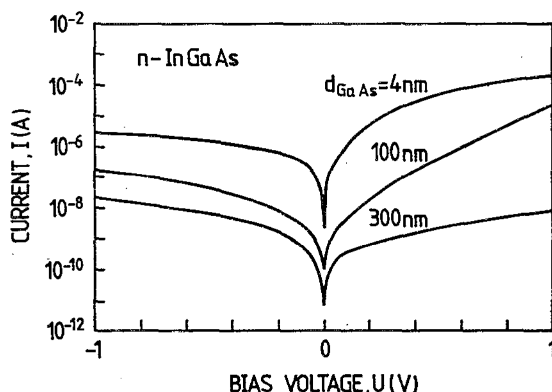

FIG. 10. I-V characteristics of n-InGaAs quasi-Schottky diodes with n-GaAs surface layers of different thicknesses.

V. CONCLUSIONS

We have studied the Schottky barrier enhancement on n-InGaAs structures with thin surface layers of different compositions. Counter-doped p^+-InGaAs layers, as well as layers of n-type and p-type InP, n-GaAs, and n-InGaP (x_{GaP}=0.11) of different thicknesses and dopant densities, respectively, were used to enhance the Schottky barrier. The results obtained can be summarized as follows.

The barrier height enhancement by band bending due to space charge in the counter-doped p^+-InGaAs surface layers increases with the layer thickness and the dopant density, respectively; but, in contradiction to the depletion-layer model, a saturation of the barrier height at higher thicknesses and dopant densities is observed. From the comparison of obtained results with present theoretical models of the barrier enhancement it follows that the ϕ_B vs d and ϕ_B vs N_A dependencies are in agreement with the two-carrier calculation. Schottky diodes with extremely low reverse current densities, $J_R(1\ V)=4.5\times10^{-6}$ A/cm², and with barrier heights up to 0.68 eV can be obtained, i.e., they reach higher barriers than reported until now on n-InGaAs.

Schottky barrier enhancement on n-InGaAs by conduction-band discontinuity at the heterointerface on InP surface layer is the simplest alternative due to its lattice matching to InGaAs, as we have observed using an undoped n-InP surface layer grown on top of the n-InGaAs that the barrier height increases with the n-InP thickness up to 0.53–0.55 eV, i.e., up to barrier heights reported directly on n-InP. Additional barrier height enhancement can be achieved by counterdoping of the surface layer, and barrier heights of 0.66 eV have been

obtained on n-InGaAs with 30-nm-thick p-InP layers doped to $N_A=2\times10^{18}$ cm^{-3}.

On n-InGaAs Schottky diodes with barrier-enhanced surface layers of highly lattice-mismatched n-GaAs a remarkable decrease of the reverse current density is observed if the layer thickness is reduced to the critical thickness for the pseudomorphic growth, but due to the small n-GaAs thickness, the barrier enhancement is low. On structures with thick, relaxed n-GaAs layers grown on top of the n-InGaAs, the measured I-V characteristics are nonideal due to the high number of defects created at the interface. On the basis of these results, it follows that GaAs surface layers are not suitable for barrier enhancement on n-InGaAs.

The barrier height enhancement of slightly lattice-mismatched n-InGaP surface layers grown on top of the n-InGaAs is similar to that for n-InP enhancement layers for the given thicknesses, but in this case it is a limitation in the layer thickness due to the lattice mismatch between InGaAs and InGaP layers.

In conclusion, we have demonstrated that, by using p-InGaAs, n- and p-InP, and n-InGaP layers, the effective barrier height on n-InGaAs can be adjusted depending on the thickness and the dopant density of the surface layers in the region from $\phi_B^0=0.2$ eV up to 0.68 eV. In such a way, electrical and materials engineers can make Schottky diodes and gates of field-effect transistors and control the barrier height on n-InGaAs.

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