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We have processed Hall contacts on InAs nanowires grown by molecular beam epitaxy using an electron beam lithography process with an extremely high alignment accuracy. The carrier concentrations determined from the Hall effect measurements on these nanowires are lower by a factor of about 4 in comparison with those measured by the common field-effect technique. The results are used to evaluate quantitatively the charging effect of the interface and surface states. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4759124]

In the implementation of concepts for the realization of future (quantum) nanoelectronic devices, semiconductor nanowires (NWs) grown by *bottom-up* techniques have shown great promise.[1,2] Without any doubt, the evaluation of the free carrier concentration is crucial for the fabrication of such devices on the nanometer scale. In this context, nanowires based on narrow band gap semiconductors, i.e., InAs, InSb, or InN, are of special interest. They have the tendency to form an accumulation layer due to Fermi level pinning in the conduction band at the surface.[3,4] Owing to the strong spin-orbit coupling, these surface 2-dimensional electron gases (2DEGs) are very interesting for spintronic applications.[5] For planar 2DEGs, the electron concentration is commonly determined very accurately utilizing the (quantum-) Hall-effect[6,7] or Shubnikov-de Haas oscillations.[8] So far, such measurements are lacking for semiconductor nanowires, as a Hall bar geometry is difficult to realize. Instead, the most common method to determine the carrier concentration is to employ the field-effect in a gate measurement setup. Within this method, there are several uncertainties. On one hand, the source and drain electrodes tend to screen the gate potential in small size devices. Additionally, the determination of the capacitance of the nanowire field-effect transistor (FET) is itself a subject to uncertainties. Most importantly, the density of surface states between the gate dielectric and the channel material affects the resulting value for the electron concentration dramatically.[9–11]

Within the field-effect based measurements, the NW carrier concentration is changed by the gate voltage. At the current pinch-off, all equilibrium carriers are removed and the corresponding carrier concentration is calculated from the applied gate voltage and the gate capacitance. In most cases, there exist spatially fixed interface/surface charges occupying interface/surface states between the metal gate electrode and nanowire surface. Apart from ideal Si/SiO_2 field-effect gate structures, interface/surface states mostly pin the Fermi level at the surface due to state densities above 10^{11} cm^{-2}. When a gate voltage is applied, most of the induced charge is trapped in the interface states and only a part of it is observed as free carriers in the channel, here the nanowire. The field-effect technique, therefore, overestimates the free carrier charge considerably.

In this context, we introduce an independent second technique based on the Hall effect, which is used besides field-effect measurements, to determine the carrier concentration in InAs nanowires. We are, thus, able to determine quantitatively the effect of interface states on the carrier concentrations which were measured by the field-effect technique.

The InAs nanowires under investigation have been grown by molecular beam epitaxy (MBE) on a GaAs (111)B substrate using an In-assisted growth mechanism. Prior to growth, the substrate is coated with a 7 nm thin SiO_x layer obtained by thermal treatment of a spin-coated thin hydrogen silsesquioxane (HSQ) layer. This film contains a high number of pin holes, which act as nucleation centers for the wire growth. The NWs grow along the [111]B direction and have a hexagonal morphology with {110} side facets of width a. Using a substrate temperature of 530 °C, an As_4 partial pressure of 1.2×10^{-6} Torr, and an equivalent InAs layer growth rate of 0.14 Å, we have obtained NWs with a width $2a$ of around 200 nm and lengths of about 2 μm. The crystal structure of the nanowires is zinc blende with a high density of regular rotational twins.[12]

After the growth, the NWs are transferred mechanically to a highly n-doped Si (100) substrate, covered with a 200 nm thick SiO_2 layer. This allows us to perform FET measurements, using the SiO_2 as a back-gate dielectric. The source, drain, and Hall contacts are defined by electron beam lithography. It is essential to adjust the Hall contacts with high accuracy on the NWs. Therefore, an optimized alignment procedure with particular emphasis on accurate marker definition was developed, which ensures overlay accuracy better than 5 nm.[13] Oxygen and Ar^+ plasmas are used to clean the contact area. Subsequently, a Ti/Au layer was evaporated as contact material. Figure 1(a) shows a typical InAs NW device. In Fig. 1(b), the exact placement of Hall contacts is visible under an angle of 35°; the Hall contacts

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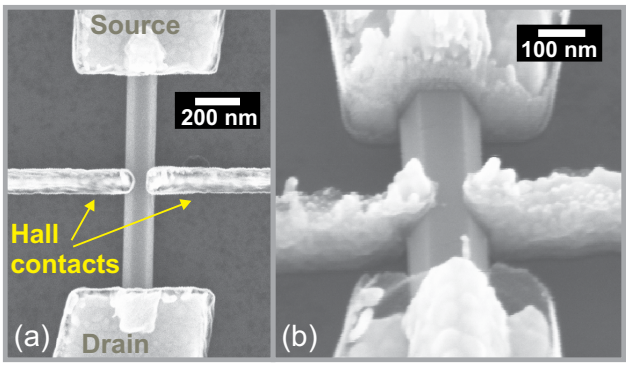

FIG. 1. Scanning electron micrograph of an InAs NW with source, drain and Hall contacts in top view (a) and under an angle of 35° (b).

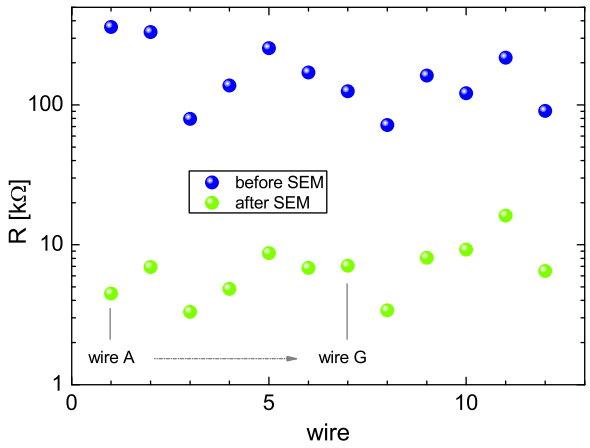

FIG. 2. Resistance R between source and drain contacts both before and after electron exposure in the SEM. Here, data of additional wires to the ones listed in Table I are shown.

cover the upper left and upper right side facets smoothly. In this way, devices with different dimensions have been fabricated. They are listed in Table I.

The Hall measurements have been performed in a measurement setup equipped with a 0.5 T magnet. The magnetic field B is oriented perpendicular to the substrate area, as indicated in the inset of Fig. 4. A constant current I_D between 1 and 5 μA is driven through the source and drain contacts, and the source-drain voltage V_{SD} as well as the voltage between the Hall contacts V_H are measured simultaneously. The measurements were performed at room temperature.

All samples in the present study have been investigated by scanning electron microscopy (SEM) to confirm the precise placement of the Hall contact electrodes. As can be seen in Fig. 2, the extensive electron irradiation decreased the initial resistance of the InAs NWs by one to two orders of magnitude.[16] Finally, this was below 20 kΩ for all nanowires under investigation. We attribute the enhanced conductance to a contribution of a surface accumulation layer (2DEG), which is induced by the SEM observation. Beside carbon contaminations, the electron beam might also create As vacancies at the surface, thus In enrichment, which is supposed to cause surface Fermi level pinning in the conduction band range.[4] The same decrease of the wire resistance is also obtained after extensive exposure of the freshly prepared wires only to atmosphere. This substantiates the interpretation of the high conductivity as being due to a surface 2DEG. The occurrence of strong surface accumulation layers on InAs after surface treatments is well known from the literature.[3,4] In the following, we therefore assign the essential current contribution along the nanowires to the current flowing in the surface accumulation layer.

The resistance measured between the Hall contacts is significantly lower than the resistance R measured along the wires and does not vary that strongly by SEM electron irradiation. Since the geometric distance between the Hall contacts is small as compared with the source and drain contacts, the resistance between the Hall contacts is attributed mainly to a contact resistance. After electron exposure, the average resistance measured between the Hall contacts is 2 kΩ, which gives an upper boundary for the contact resistance. Since the covered area of the source and drain contacts is at least 5 times larger with a corresponding low contact resistance, we neglect the contribution of the contact resistance in the following.

The current-voltage (IV) characteristics between source and drain contacts show ohmic behavior for all NWs. The 2-dimensional conductivity of the nanowires is calculated using the formula $\sigma_{2D} = L/(6aR)$, where $6a$ the nanowire circumference and L the contact separation length (see Table I). The conductivity values are in agreement with recently reported values of MBE grown InAs NWs with the same crystal structure (zinc blende with twin planes).[14] There are some fluctuations of the conductivity values, which have been observed previously for InAs nanowires grown by the same technique,[12] as well as for InAs nanowires grown by selective area metal-organic vapor phase epitaxy.[15] A likely reason for the resistivity spread is varying surface conditions. The IV-characteristic between the Hall contacts is found to be ohmic as well.

TABLE I. Compilation of data of the studied nanowires: Contact separation length L, nanowire width $2a$, Hall contact separation d_S, resistance between source and drain contacts R, normalized Hall slope m_H/I_D, conductivity σ_{2D}, carrier concentration from Hall effect n_{2D}, and from field-effect measurements n_{FE}, difference $\Delta n = n_{FE} - n_{2D}$.

Wire	L [nm]	$2a$ [nm]	d_S [nm]	R [kΩ]	m_H/I_D [Ω/T]	σ_{2D} [mS]	n_{2D} [10^{11}cm^{-2}]	n_{FE} [10^{11}cm^{-2}]	Δn [10^{11}cm^{-2}]
A	480	160	53	4.5	130	0.43	7.2	18.4	11.2
B	1300	220	75	6.9	129	0.27	6.5	36.2	27.7
C	530	230	55	3.3	128	0.21	4.5		
D	1350	220	50	4.8	75	0.45	9.3		
E	2030	235	45	8.7	69	0.27	7.4	11.6	4.2
F	1300	200	50	6.8	55	0.53	11.6	44.8	33.2
G	1000	200	50	7.1	47	0.71	13.0	48.8	35.8

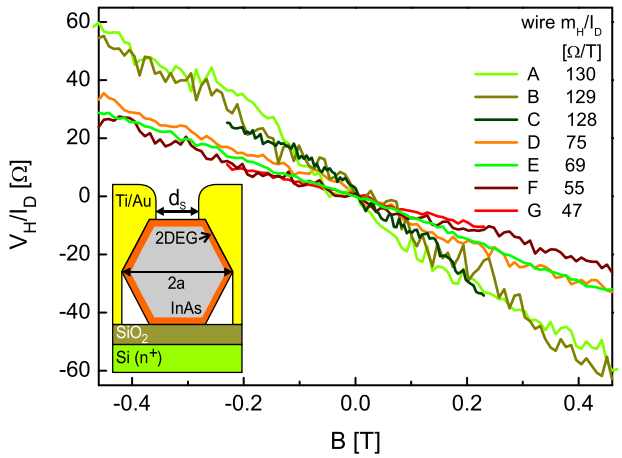

FIG. 3. Ratio between Hall voltage and drain current V_H/I_D as a function of magnetic field B for wires A to G at zero gate voltage. The inset shows a schematics of the nanowire cross section covered by the Ti/Au Hall contacts.

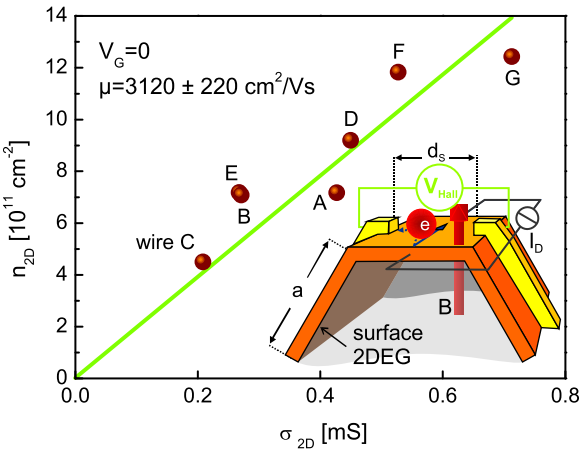

FIG. 4. Carrier concentrations n_{2D} obtained from Hall effect measurements as a function of conductivity σ_{2D} of all nanowires at zero back-gate voltage. The inset illustrates the measurement scheme.

Figure 3 shows the Hall voltage V_H normalized to the drain current I_D as a function of B for all studied NWs. Generally, the Hall voltage V_H exhibits a linear dependence on the magnetic field, which indicates that there is a layer of single type charge carriers. From the negative sign of the slope, we conclude that we have n-type conduction, consistent with the field-effect measurements described below. To calculate the electron concentration n_{2D} in the 2DEG surface layer from V_H, we have to account for the geometrical situation, which is depicted in the insets of Figs. 3 and 4. As the side contacts short the upper left and right side facets of the wire, there are two contributions to the net Hall voltage $\bar{V}_H$, i.e., from the 2DEG on the top of the wire with an electrode separation d_s: $V_{H,t} = -j_{2D}d_sB/(en_{2D})$ and from the 2DEG at the bottom with an electrode separation of $2a$: $V_{H,b} = -j_{2D}2aB/(en_{2D})$. Here, $j_{2D} = I_D/(6a)$ is the current density, with I_D the current along the nanowire. Furthermore, one has to take into account the voltage drops due to the compensation currents flowing between the Hall contact electrodes in the top and bottom 2DEG segments. These segments have the resistances $R_t = d_s/(w\sigma_{2D})$ and $R_b = 3a/(w\sigma_{2D})$, respectively, with w the Hall contact width. Finally, the net Hall voltage is given by[17]

$$\bar{V}_H = -\frac{j_{2D}\bar{d}}{en_{2D}}B\,. \tag{1}$$

Here, $\bar{d} = 5d_sa/(d_s + 3a)$ is the effective Hall electrode distance. It is useful to define the Hall slope $m_H = \Delta V_H/\Delta B$ which is easily extracted from the Hall measurements shown in Fig. 3 and which can be employed to determine the electron concentration

$$n_{2D} = -\frac{1}{e}\frac{\bar{d}}{6a}\frac{I_D}{m_H}\,. \tag{2}$$

Figure 4 shows a linear relation between n_{2D}, evaluated by using Eq. (2), and the conductivity σ_{2D}. From this linear relation, one can conclude that for all wires the electron drift mobility $\mu = \sigma_{2D}/en_{2D}$ is basically the same with an average value of $\mu = 3120 \pm 220$ cm^2/Vs. The extracted values of the carrier concentrations n_{2D} between 4.5×10^{11} and 1.3×10^{12} cm^{-2} agree with typical values obtained for 2-dimensional systems within a surface accumulation layer in InAs.[5]

The carrier concentration and thus the Hall voltage can be controlled by the back-gate voltage V_G. This is demonstrated for NW A in the inset of Fig. 5. For varying gate voltages V_G between -10 and 10 V, different Hall slopes m_H, i.e., different carrier concentrations n_{2D} are obtained. While changing V_G, the measured electron concentration n_{2D} depends linearly on σ_{2D} (cf. Fig. 5), which implies that here the electron mobility μ does not change with n_{2D} as well. The obtained value 3590 ± 75 cm^2/Vs agrees well with the value extracted from Fig. 4. This clearly demonstrates the consistency of our evaluation method.

For comparison, we have performed back-gate field-effect transistor measurements on a number of wires to estimate the carrier concentration.[18] The inset of Fig. 6 exemplarily shows the I_D versus V_G characteristic for NW E. From the extrapolation of the linear region to $I_D = 0$, we obtain a threshold voltage $V_{th} = -11$ V. Using the expression[9,15]

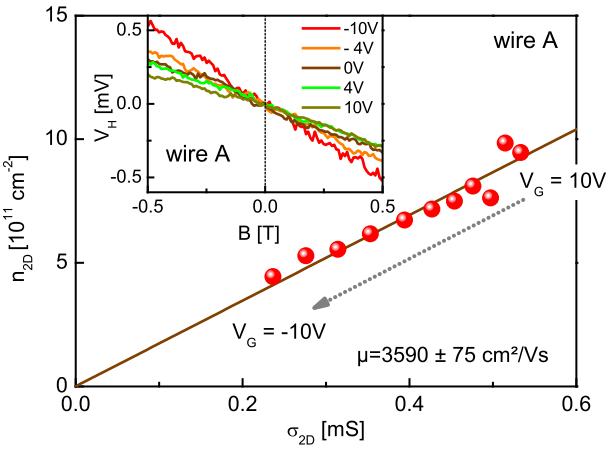

FIG. 5. Carrier concentration n_{2D} obtained from Hall-measurements on wire A plotted versus the conductivity σ_{2D} at different gate voltages V_G. The inset shows the Hall voltage V_H as a function of magnetic field for gate voltages between -10 V and $+10$ V. The source drain current is 5 μA.

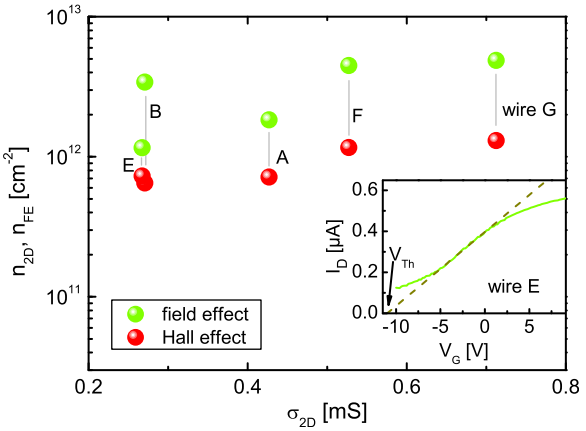

FIG. 6. Carrier concentration obtained from Hall effect, n_{2D}, and field-effect transistor measurements, n_{FE}, versus conductivity σ_{2D} of nanowires A, B, E, F, and G. The inset shows the drain current I_D as a function of gate voltage V_G of wire E. The source-drain bias voltage is 5 mV.

$$n_{FE} = \frac{C|V_{th}|}{6eLa}, \tag{3}$$

we calculate the corresponding 2-dimensional carrier concentration of $11.6 \times 10^{11}\text{cm}^{-2}$. Here, the nanowire capacitance C was calculated according to a back-gate nanowire FET model.[9] In the same way, we obtain carrier concentration values for the other wires (cf. Table I).

In Fig. 6, the electron concentrations determined by both methods are plotted for five nanowires. The field-effect data exceed those from Hall effect by a factor of about 4. This means that only about 25% of the charge induced via the back-gate electrode is found in the conduction channel, the surface 2DEG of the nanowire. The major part of the induced charge ends up in the interface/surface states and does not contribute to electrical transport in the nanowire. As can be inferred from Table I, the interface/surface charge density, i.e., the difference Δn between n_{2D} and n_{FE}, is in the order of a few $10^{12}\,\text{cm}^{-2}$. This is a typical surface state density, which pins the Fermi level at the surface and allows only tiny band bending changes by an applied gate voltage. It explains the large gate voltage sweeps (cf. Fig. 6) between ± 10 V, which are necessary to change n_{2D} by a measurable amount.

In summary, we have applied an optimized alignment procedure in electron beam lithography, which allows the processing of Hall contacts on single InAs nanowires. Thus, an accurate determination of the electron concentration within the surface accumulation layer of InAs nanowires is possible. The deviation of the results from simultaneously performed field-effect measurements using a back-gate gives direct evidence for the charging effect of interface states. The present Hall effect method is very useful for an accurate determination of carrier concentrations in nanowires and for an investigation of the interface states in gated nanostructures.

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[16]Here, data of additional wires to the ones listed in Table I are shown.
[17]See supplementary material at http://dx.doi.org/10.1063/1.4759124 for details on the derivation of the net Hall voltage.
[18]For samples C and D, no field-effect measurements were possible, because of gate leakage through the SiO_2 gate dielectric.