Si/SiGe electron resonant tunneling diodes

D. J. Paul[a] and P. See
Cavendish Laboratory, University of Cambridge, Madingley Road, Cambridge, CB3 0HE, United Kingdom

I. V. Zozoulenko[b] and K.-F. Berggren
Department of Physics and Measurement Science, University of Linköping, Linköping, S-58183, Sweden

B. Kabius
LEO Elektronenmikroskopie GmbH, 73446 Oberkochen, Germany

B. Holländer and S. Mantl
Institut für Schicht und Ionentechnik, Forschungszentrum Jülich, D-52425 Jülich, Germany

(Received 18 May 2000; accepted for publication 15 July 2000)

Resonant tunneling diodes have been fabricated using strained-Si wells and strained $Si_{0.4}Ge_{0.6}$ barriers on a relaxed $Si_{0.8}Ge_{0.2}$ n-type substrate, which demonstrate negative differential resistance at 298 K. Peak current densities of 5 kA/cm^2 with peak-to-valley current ratios of 1.1 have been achieved. Theoretical modeling of the structure demonstrates that the major current peak results from the tunneling of light-mass electrons from the relaxed substrate and not from the heavy-mass electrons in the emitter accumulation layer. © *2000 American Institute of Physics.* [S0003-6951(00)02337-8]

Resonant tunneling diodes (RTDs) are now a mature technology in the $III-V$ system with many demonstrations of memory[1] and logic[2] circuits. The vast majority of the microelectronics industry, however, is based on Si and, therefore, there is great interest in attempting to create RTDs using Si/SiGe heterostructures.[3] The performance has been substantially poorer in both the p- (Ref. 4) and the n-type Si/SiGe systems.[5] Indeed, the n-type system has the only room-temperature demonstration of negative differential resistance (NDR) with a peak current density of 0.4 kA/cm^2 at a peak-to-valley ratio (PVR) of 1.2,[5] even though many of the strained layers were above the equilibrium critical thickness.[3] The NDR in p-type Si/SiGe RTDs is quenched well below room temperature by thermally assisted tunneling through higher resonance states.[6] The best performance in Si-based tunnel diodes have come from interband diodes[7] with peak current densities of 3 kA/cm^2 with a PVR of 4.2 (Ref. 8) or 10.8 kA/cm^2 with a PVR of 1.42.[9] The major problem is that these diodes have been fabricated by molecular-beam epitaxy with δ-doped layers and will be very difficult to place in circuits and processed with metal–oxide field-effect transistors (FETs) or heterostructure FETs.

Results are presented on Si/SiGe RTDs with much higher peak current densities at room temperature. Structures were designed with strained $Si_{1-x}Ge_x$ barriers on a relaxed $Si_{1-y}Ge_y$ substrate to confirm if a barrier exists in the conduction band when $x>y$, as has been suggested by theory.[10] Theoretical modeling of the structures is also presented to understand the electronic transport mechanisms in the devices to allow future optimization of performance.

The wafers for the work were purchased from DERA, Malvern (U.K.). They were grown in an ultra-high-vacuum compatible chemical-vapor deposition (CVD) system using SiH_4 and GeH_4 gases in a H_2 carrier. AsH_4 was used to dope the contact regions n type[11] at $N_D \sim 3\times10^{18}$ cm^{-3}. The heterolayers were grown on an n-type (100) Si substrate with approximately a 3-μm-thick, n-type, strain-relaxation buffer graded from Si to $Si_{0.8}Ge_{0.2}$ and a 1-μm-thick n-$Si_{0.8}Ge_{0.2}$ buffer. The wafer was then removed from the growth chamber and given a modified RCA clean[11] to remove excess As from the surface in an attempt to circumvent the As dopant segregation problems in CVD material.[12] This technique of regrowth has already demonstrated high mobilities at low temperatures when used in modulation-doped samples with the cleaned interface 10 nm below the strained-Si quantum well.[11] The wafers were replaced in the growth chamber and the following layers grown: 10 nm i-$Si_{0.8}Ge_{0.2}$ buffer, 10 nm i-Si, 2 nm i-$Si_{1-x}Ge_x$ barrier, 3 nm i-Si well, 2 nm i-$Si_{1-x}Ge_x$ barrier, 10 nm i-Si, 50 nm n-$Si_{0.8}Ge_{0.2}$, and a 4 nm n-Si cap. Two wafer were grown with the Ge concentrations in the barriers of $x=0.2$ and 0.6. Devices were processed into mesas using reactive ion etching and Au (1% Sb) ohmic contacts were used.

Figure 1 shows a cross-sectional transmission electron micrograph (TEM) from the center of the wafer with the two $Si_{0.4}Ge_{0.6}$ barriers clearly visible. The regrowth interface appears as a light line below the lowest Si quantum well and is

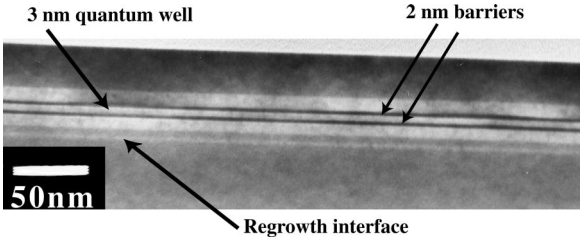

FIG. 1. Cross-sectional transmission electron (TEM) micrograph from the center of the wafer.

[a]Electronic mail: dp109@cam.ac.uk
[b]Also at: Department of Science and Technology, University of Linköping, Campus Norrköping, S-601 74 Norrköping, Sweden.

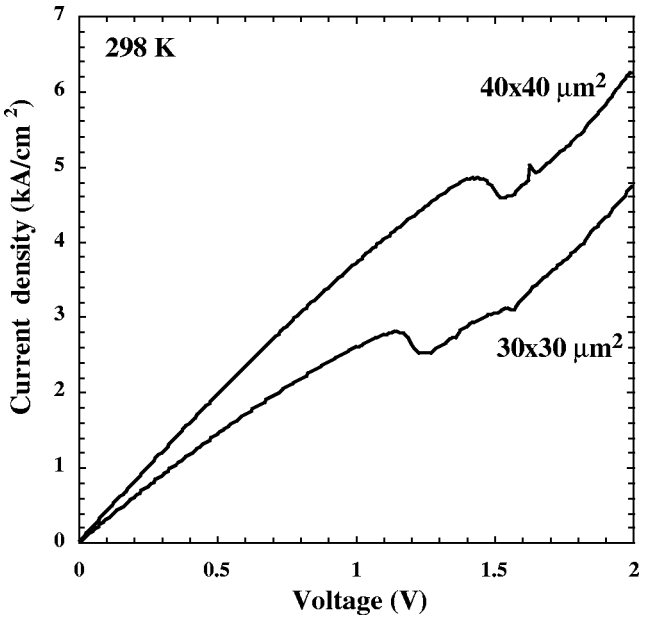

FIG. 2. $I-V$ plots for two different devices taken from different parts of the wafer with $Si_{0.4}Ge_{0.6}$ tunnel barriers. The difference in peak positions is attributed to contact and series resistances along with material composition and layer differences for the two devices.

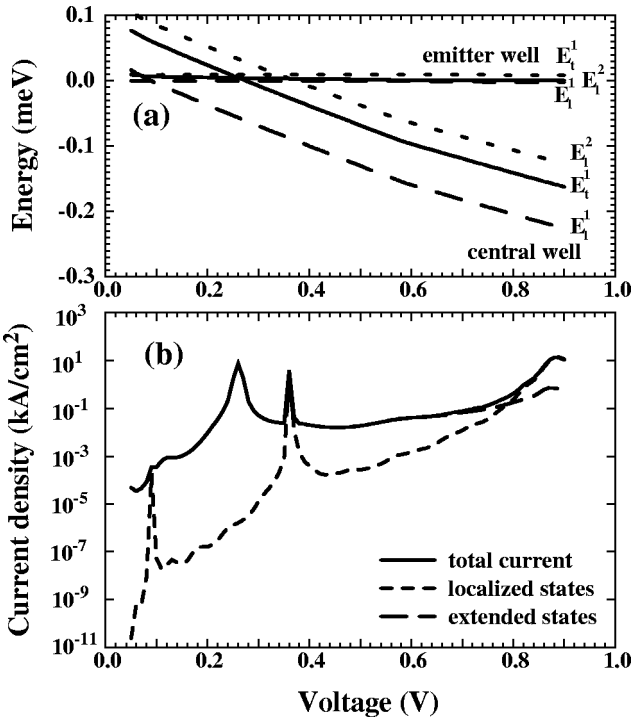

FIG. 3. (a) Position of quasibound states in the emitter and central wells. Indices t (transverse), l (longitudinal) refer to the states with the light and heavy electron masses, respectively. (b) Current characteristics as a function of the applied voltage calculated from theory. The total current is dominated by the extended states at almost all voltages.

believed to indicate a Si-rich interface.[11] This is unlikely to influence the electron transport.[11] Figure 2 shows the two-terminal current–voltage ($I-V$) characteristics from two devices fabricated from different parts of the wafer with the $Si_{0.4}Ge_{0.6}$ barriers, both showing clear NDR at 298 K. The maximum peak current density is 5 kA/cm^2 and the maximum PVR is 1.1. The wafer with $Si_{0.8}Ge_{0.2}$ barriers did not show NDR at room temperature, confirming the increased barrier height for the strained-$Si_{0.4}Ge_{0.6}$ barriers. The difference in $I-V$ characteristics from the two devices in Fig. 2 can be attributed to an approximate 20 K variation in temperature across the wafer during growth. This substantially changes the thicknesses and composition of the heterolayers across the wafer,[13] which is useful in the present case to investigate how the transport properties change with changing layer structure. Towards the edge of the wafer, the Ge content is reduced by about 2% and the layer thicknesses are reduced[13] ($30\times30\ \mu$m^2 device in Fig. 2), which results in a reduced peak current density.

The $I-V$ characteristics were also modeled theoretically. While there has been substantial modeling of $III-V$ RTDs,[14] here the valleys and anisotropic masses in the Si-based conduction band must be accounted for. There will be two main tunneling current contributions: one from the localized states from the accumulation layer in the Si spacer on the emitter side of the tunnel barriers and a second from the bulk, extended states of the relaxed n-$Si_{0.8}Ge_{0.2}$ contacts. The Tsu–Esaki[15] formula was generalized to account for the extended states with the valleys and anisotropic effective masses, $m_l=0.9m_0$ and $m_t=0.2m_0$ with m_0 the free-electron mass. No account of the small effective-mass variations in the different materials was taken.[10] The transmission coefficient and, hence, the tunneling current was obtained self-consistently using a recursive Green's function technique. For the localized states, the potential profile in the accumulation layer was calculated using a self-consistent Poisson–Schrödinger solver. This allows the wave function of the accumulation layer to be obtained which is then divided into N segments and the transmission coefficient of each segment to the collector is calculated using a recursive Green's function technique. The total current is then the sum of the two contributions. The model should be accurate in determining the peak current density but not the valley current, which is determined by numerous scattering and thermal currents.[14]

Figure 3 shows the calculation results with the subband energies in (a) and the $I-V$ in (b) at 0 K. The first resonance below 0.1 V corresponds to the heavy electron mass (m_l) from states in the accumulation layer and, therefore, the transmission probability is very small. The second quasibound state in the central well (E_t^1) is the first state from the light electron mass (m_t) in the bulk and provides the main peak in the $I-V$ characteristics. The light-mass state in the accumulation layer (E_t^1) is not occupied and, therefore, cannot contribute to the current. The second peak in the $I-V$ has approximately equal contributions from the heavy-mass and light-mass electrons from the accumulation and bulk regions, respectively. In this case, the transmission coefficient for electrons with a heavy mass is significantly higher than for the E_l^1 resonance because of the higher electron energy.

The peak voltages in the experimental and theoretical cases are different due to the parasitic series resistances from the contact regions in the experimental measurement. Only room-temperature measurements could be obtained due to the contact regions being doped too low and the contacts freezing out at lower temperatures. Higher doping will also reduce the peak current voltage as required for applications. Attempts at annealing the metallic contacts resulted in shorted devices due to spiking. The peak currents agree

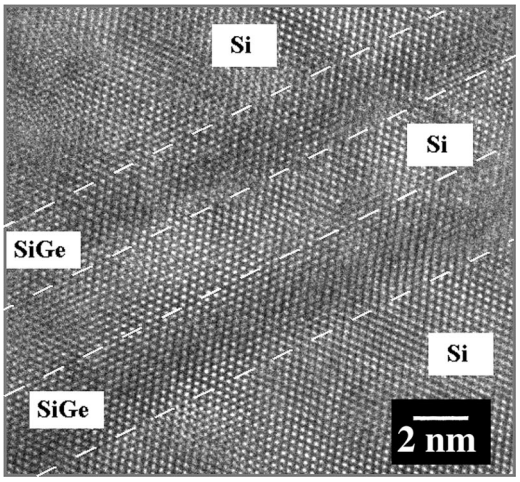

FIG. 4. High-resolution TEM micrograph showing the $Si_{0.4}Ge_{0.6}$ barriers. The dashed lines are drawn to guide the eye.

within a factor of 2 and the difference may be attributed to the interface roughness, which is evident in Fig. 1, as well as the difference in temperature between the model calculations and the experiment. The high-resolution image (Fig. 4) shows a roughness of several monolayers at the Si/SiGe interface. The SiGe layers can be recognized by their darker contrast in the high-resolution image but the barriers are too thin to accurately determine the Ge content and distribution. It is quite possible that the profile is not rectangular as has been assumed in the modeling. A second peak is visible on the $40\times40\,\mu m^2$ device (Fig. 2), which may be due to the combined localized and extended states tunneling.

In conclusion, Si/SiGe RTDs have been fabricated which demonstrated a peak current density of 5 kA/cm^2 and a PVR of 1.1 at 298 K. The results clearly demonstrated that a strained-$Si_{1-x}Ge_x$ heterolayer grown on a relaxed $Si_{1-y}Ge_y$ substrate $(x>y)$ forms a barrier to electrons as predicted by theory.[10] Theoretical modeling of the transport suggests that the tunneling current is predominantly from light-hole electrons from the relaxed $Si_{0.8}Ge_{0.2}$ contact layers and not from the accumulation layer formed in the strained-Si spacer on the emitter side. High-resolution TEM pictures show interface roughness of the order of two atomic layers, which is the major limitation of RTD devices. While the present current densities are adequate for numerous circuits, the PVR requires to be increased to over 2 with the resonance at a lower voltage before these devices can form useful circuits.

This work was funded by the European Commission under the Framework IV MEL-ARI project SiQUIC (Project No. 22987). The authors would also like to thank D. J. Robbins, A. C. Churchill, and W. Y. Leong at DERA for growth of the material along with M. Pepper for useful discussions.

[1] J. P. A. van der Wagt, Nanotechnology **10**, 174 (1999).
[2] A. Seabaugh, X. Deng, T. Blake, B. Brar, T. Broekaert, R. Lake, F. Morris, and G. Frazier, Tech. Dig. Int. Electron Devices Meet. **98**, 429 (1998).
[3] D. J. Paul, Adv. Mater. **11**, 191 (1999).
[4] H. C. Liu, D. Landheer, M. Buchanan, and D. C. Houghton, Appl. Phys. Lett. **52**, 1809 (1988).
[5] K. Ismail, B. S. Meyerson, and P. J. Wang, Appl. Phys. Lett. **59**, 973 (1991).
[6] U. Gennser, V. P. Kesan, S. S. Iyer, T. J. Bucelot, and E. S. Yang, J. Vac. Sci. Technol. B **9**, 2059 (1991).
[7] S. L. Rommel, T. E. Dillon, M. W. Dashiell, H. Feng, J. Kolodzey, P. R. Berger, P. E. Thompson, K. D. Hobart, R. Lake, A. C. Seabaugh, G. Klimeck, and D. K. Blanks, Appl. Phys. Lett. **73**, 2191 (1998).
[8] R. Duschl, O. G. Schmidt, G. Reitemann, E. Kasper, and K. Eberl, Electron. Lett. **35**, 1111 (1999).
[9] S. L. Rommel, T. E. Dillon, P. E. Thompson, K. D. Hobart, R. Lake, and A. C. Seabaugh, IEEE Electron Device Lett. **20**, 329 (1999).
[10] M. M. Rieger and P. Vogl, Phys. Rev. B **48**, 14276 (1993).
[11] D. J. Paul, A. Ahmed, N. Griffin, M. Pepper, A. C. Churchill, D. J. Robbins, and D. J. Wallis, Thin Solid Films **321**, 181 (1998).
[12] K. Ismail, J. O. Chu, K. L. Saenger, and B. S. Meyerson, Appl. Phys. Lett. **65**, 1248 (1994).
[13] A. Ahmed, D. J. Paul, M. Pepper, A. C. Churchill, W. Y. Leong, D. J. Robbins, D. J. Wallis, J. Newey, and A. J. Pidduck (unpublished).
[14] J. P. Sun, G. I. Haddad, P. Mazumder, and J. N. Schulman, Proc. IEEE **86**, 641 (1998).
[15] R. Tsu and L. Esaki, Appl. Phys. Lett. **22**, 562 (1973).