AIP | Applied Physics Letters

Phase coherent transport in InSb nanowires

Huijun Yao, Hacı Yusuf Günel, Christian Blömers, Karl Weis, Junhong Chi et al.

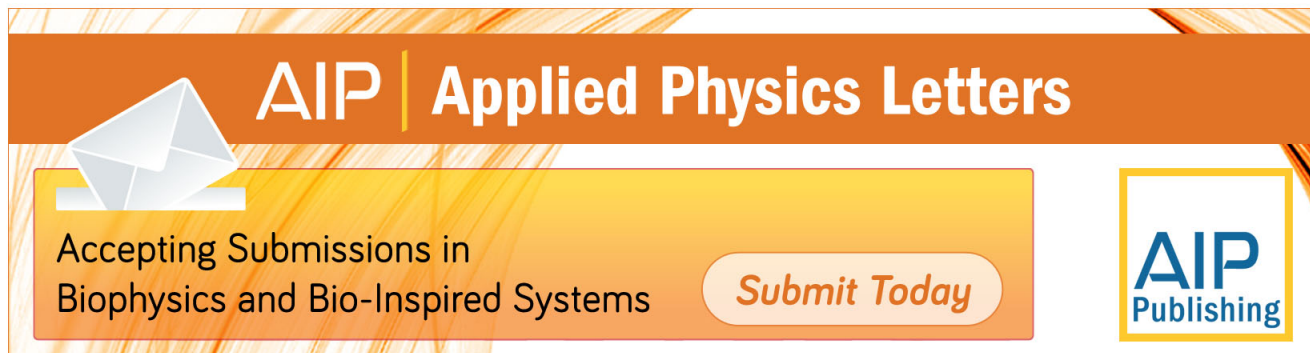## Additional information on Appl. Phys. Lett.

Journal Homepage: http://apl.aip.org/

Journal Information: http://apl.aip.org/about/about_the_journal

Top downloads: http://apl.aip.org/features/most_downloaded

Information for Authors: http://apl.aip.org/authors

Phase coherent transport in InSb nanowires

Huijun Yao,[1,2,3] Hacı Yusuf Günel,[1,2] Christian Blömers,[1,2] Karl Weis,[1,2] Junhong Chi,[4] Jia Grace Lu,[4] Jie Liu,[3] Detlev Grützmacher,[1,2] and Thomas Schäpers[1,2,5,a]

[1]Peter Grünberg Institute (PGI-9), Forschungszentrum Jülich, 52425 Jülich, Germany
[2]JARA-Fundamentals of Future Information Technology, Forschungszentrum Jülich, 52425 Jülich, Germany
[3]Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou 730000, People's Republic of China
[4]Department of Physics & Astronomy, University of Southern California, Los Angeles, California 9008-0484, USA
[5]II. Physikalisches Institut, RWTH Aachen University, 52056 Aachen, Germany

Comprehensive electrical transport studies are performed on InSb nanowires by varying temperature, gate voltage, and magnetic field. The 3-dimensional bulk conduction is found to dominate in the nanowire channel after investigating a large number of nanowires with different diameters, which show approximately a linear relation between the conductance normalized to the length and the wire cross section. At low temperatures, universal conductance fluctuations are observed. From the amplitude and the correlation voltage of the conductance fluctuations, the phase-coherence length in InSb nanowires is determined at various temperatures. © 2012 American Institute of Physics. [http://dx.doi.org/10.1063/1.4747200]

Due to the remarkable properties and versatile functionalities, semiconductor nanowires render a new class of nanoscale building blocks for a broad range of disciplines, such as quantum electronics, sensors, energy storage, or biotechnology. They receive ever growing interest of the scientific community. In particular, nanowires based on InSb are considered promising for nano-electronic device applications due to their high-speed performance and low dynamic power dissipation compared to standard Si technology.[1,2] Furthermore, InSb nanowires are also very interesting for spin-electronics and spin-based quantum information technology, owing to the fact that bulk InSb has a narrow band gap of 0.16 eV, an extremely high electron mobility, and strong spin-orbit coupling.[3,4] Very recently, InSb nanowires were even used for experiments dedicated to confirm the existence of Majorana fermions.[5]

Although there have been a number of reports on experimental investigations of InSb nanostructures,[6–12] there is still much uncertainty on the fundamental electrical transport properties. An interesting question is whether an electron accumulation layer exists at the surface of the InSb nanowire due to Fermi level pinning in the conduction band, as found in InSb layer system.[13] Thus, it is important to distinguish the surface and bulk contributions to the conduction. Furthermore, it is essential to determine the electron transport mechanisms, whether phase-coherence comes into play. Low temperature transport measurements at different magnetic fields and transverse electric fields would clarify the physical concept of electron conduction.

The InSb nanowires investigated in this study are grown by a catalytic chemical vapor deposition method. The nanowires exhibit a single crystalline zinc blende structure with a stoichiometry of 1:1. Details on the growth and material characteristics are given in Ref. 8. To probe the electron transport properties, the InSb nanowires are transferred from the original Si growth substrate to a highly n-doped Si (100)

wafer coated with a 100 nm thick SiO_2 insulating layer. The SiO_2/Si substrate has pre-patterned alignment markers which are used to determine the coordinates of the randomly dispersed nanowires for electrode patterning using electron beam lithography. In order to achieve good ohmic contacts between the metal electrodes and the nanowires, Ar^+ sputtering is used to remove the native oxide and contaminations on the surface of InSb nanowires. Then, each nanowire is contacted with four Ti/Au electrodes. Figure 2 (inset) shows a scanning electron microscopy image of a typical contacted nanowire with a diameter of 28 nm. All our data result from four-terminal measurements, in order to analyze the intrinsic electrical transport properties. The highly conductive Si substrate is used as a back-gate electrode for field-effect transistor measurements. The low-temperature measurements are carried out in a He-4 flow cryostat with a temperature ranging from 4.2 to 300 K and subsequently in a He-3 cryostat for lower temperatures between 0.3 and 25 K.

In order to distinguish between bulk and surface conduction, the diameter dependence of the conductance is analyzed for a number of samples at room temperature.[14–16] In Fig. 1, the normalized conductance $g = L/R$ is plotted as a function of diameter d. Here, R is the nanowire resistance and L the contact separation. In the inset of Fig. 1, g vs. d is plotted on a double logarithmic scale. One finds a linear increase, which can be expressed by $g \propto d^\beta$ with $\beta \approx 2.1$. Since the value of β is very close to the value of $\beta = 2$ for a three dimensional (3D) conductor, we can conclude that the transport dominates in the bulk of the nanowire. Furthermore, no major surface conductance contribution is present, since in this case a slope smaller than 2 is expected, with $\beta = 1$ for a pure surface conductance. On average, the resistivity ρ of the InSb nanowires is $(0.010 \pm 0.005) \Omega$ cm.

Figure 2 plots the drain current vs. source-drain voltage ($I_d - V_{sd}$) of an InSb nanowire at various back-gate voltages V_g ranging from -40 to $+40$ V. The nanowire has a diameter of $d = 24$ nm and a contact separation of $L = 260$ nm. In the following, we will discuss the properties of this nanowire

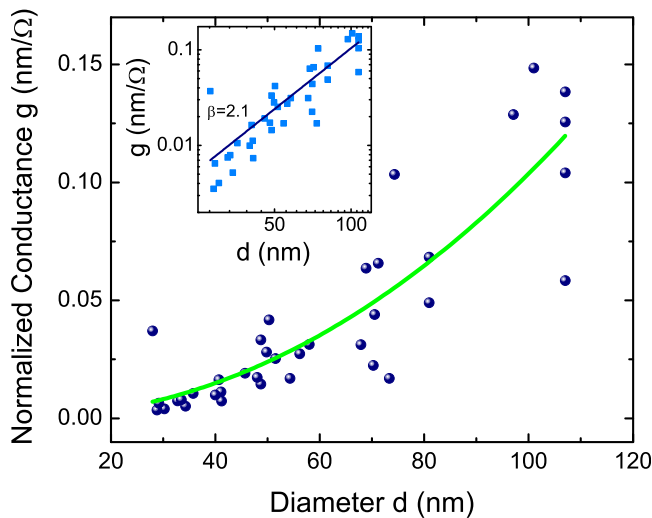a)Author to whom correspondence should be addressed. Electronic mail: th.schaepers@fz-juelich.de.

FIG. 1. Normalized conductance g vs. the diameter d at room temperature, determined from four-terminal measurements. The solid line shows a fit for $g \propto d^{\beta}$, with $\beta = 2.1$. The inset shows the same data points in logarithmic scale together with a power law fit for $g \propto d^{\beta}$, giving an exponent $\beta = 2.1$.

only as a representative, since additional nanowires investigated confirmed the findings. All curves shown in Fig. 2 exhibit a linear dependence, which indicates good ohmic contacts between the drain and source electrodes and the nanowire. The InSb nanowire shows n-type behavior as the conductance decreases with decreasing gate voltage. However, no complete suppression of the drain current is achieved within the instrument limit (here $V_g = -40$ V), probably due to a large electron concentration forming a degenerate electron system as well as the electronic states at the nanowire/dielectric interface.[17] From previous measurements on nanowires of the same growth run an electron concentration of 1.6×10^{18} cm^{-3} was determined,[8] which is well above the limit ($\approx 10^{17}$ cm^{-3}) for the formation of a degenerate electron system in InSb. From all three curves plotted in

the lower inset of Fig. 2, a threshold voltage of $V_{th} = (55 \pm 5)$ V is obtained from the extrapolation of the $I_d - V_g$ curve to the V_g axis. Note that the source-drain bias voltage is kept at a low value of 20 mV, in order to prevent any heating effect in the nanowire. The fact that the threshold voltage does not change when the temperature decreases indicates that the electron concentration remains constant, as it is expected for a degenerate electron gas.

In order to elucidate the conduction mechanisms in our nanowires in more detail, the temperature-dependence of the conductance G is investigated, as shown in Fig. 3. It increases with increasing temperature up to a transition point of around 200 K exhibiting semiconductor-like behavior. Above 200 K a decrease of G according to $T^{-0.4}$ is found, which is due to electron-phonon scattering. Overall, the temperature dependence of G is weak, which can be explained by the fact that the electron gas in the nanowire is degenerate. Since the electron concentration is basically constant in the whole temperature range, the temperature-dependence of the mobility is expected to follow the dependence of G.

In Fig. 2 (lower inset), it can be seen that at low temperature, I_d is modulated when the gate voltage is varied. In order to investigate this phenomenon in more details, the conductance G is measured as a function of V_g in the temperature range of 0.5 to 10 K. As can be seen in Fig. 4(a), for temperatures below 2.6 K pronounced conductance fluctuations are observed. For larger temperatures, these fluctuations are effectively damped with increasing temperature. The observed fluctuations are attributed to universal conductance fluctuations.[18,19] This effect originates from electron interference which is not averaged out in small disordered samples. Under ideal conditions, when phase-coherence is maintained in the complete sample, i.e., the phase-coherence length l_{ϕ} exceeds L, the average fluctuation amplitude is found to be $\alpha e^2/h$, with α a pre-factor in the order of 1 depending on the shape of the sample.[19] For InAs nanowires, $\alpha \approx 0.3$ was determined.[20] In the case when l_{ϕ} is smaller than the sample dimension or if thermal averaging occurs, the fluctuation amplitude is reduced. In the measurements shown in Fig. 4(a), the electron interference is modified by tuning the Fermi wavelength by
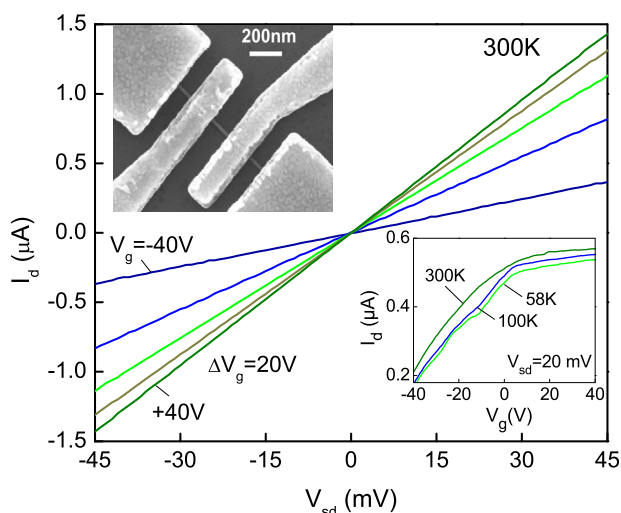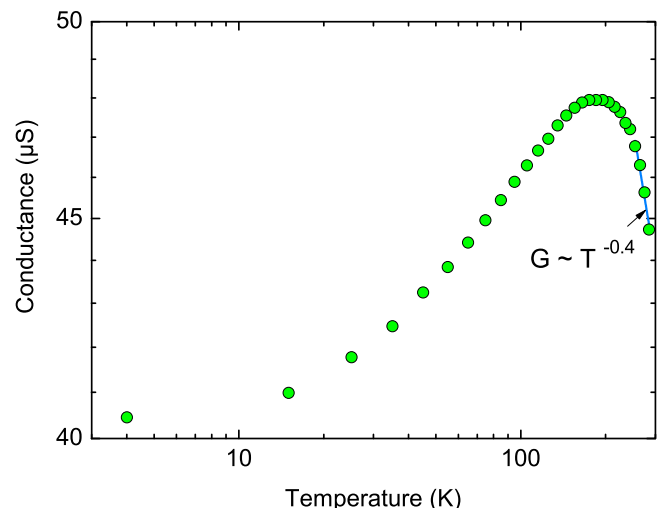

FIG. 2. Output characteristics ($I_d - V_{sd}$) of a single InSb nanowire taken at room temperature. The gate voltage was varied between -40 to $+40$ V in steps of 20 V. The length between the two inner contact fingers is 260 nm and the diameter is 24 nm. The lower inset shows the corresponding drain current I_d vs gate voltage V_g at 300 K, 100 K, and 58 K. The source-drain bias voltage V_{sd} was 20 mV. The upper inset shows a scanning electron microscope image of a representative back-gated InSb nanowire.

FIG. 3. Temperature dependence of the conductance G. At high temperatures, G decreases with $T^{-0.4}$.
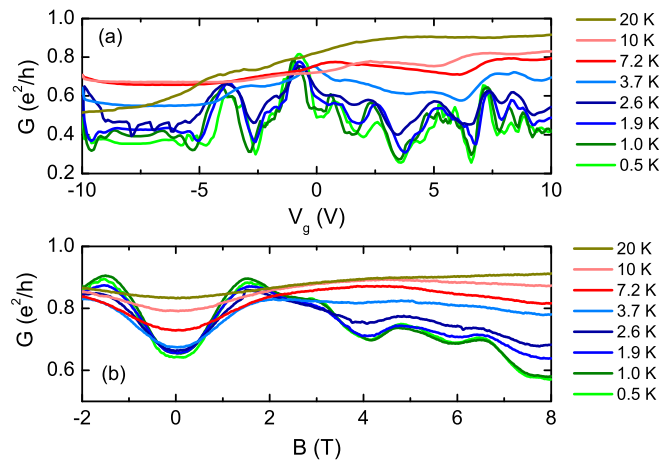
FIG. 4. (a) Conductance fluctuations G in units of e^2/h as a function of gate voltage at various temperatures in the range from 0.5 to 20 K. (b) Corresponding fluctuations as a function of the magnetic field B. The field is oriented perpendicularly to the wire axis.

the gate voltage. Alternatively, the conductance fluctuations can also be observed when the phase of the interfering electron waves is shifted by means of a magnetic field B [cf. Fig. 4(b)]. Owing to the effective two-terminal measurement, the conductance fluctuations are symmetric under magnetic field reversal. Because the limited range of the B-dependent fluctuations does not allow a reliable statistical analysis, we will focus on the measurements of the gate voltage dependent fluctuations in the following.

The mean conductance fluctuation amplitude is quantified by the root-mean-square $\mathrm{rms}(G) = \sqrt{\mathrm{var}(G)}$ over V_g. Here, the variance of G is defined by $\mathrm{var}(G) = \langle \delta G^2 \rangle_{V_\mathrm{g}}$, with $\langle \ldots \rangle_{V_\mathrm{g}}$ representing the average of the conductance fluctuations over the back-gate voltage. In Fig. 5, $\mathrm{rms}(G)$ is plotted as a function of temperature. As can be seen here, when the temperature is below about 1.9 K, $\mathrm{rms}(G)$ is basically constant with a value of about $0.11e^2/h$, which is somewhat smaller than the value of $0.3e^2/h$ for InAs nanowires.[20] The almost constant fluctuation amplitude below 1.9 K indicates that in this temperature range, the phase coherence is limited

by the sample dimensions, i.e., the contact separation $L = 260\,\mathrm{nm}$, instead of by l_ϕ.[20] Thus in this regime, l_ϕ exceeds 260 nm. For temperatures above 1.9 K, $\mathrm{rms}(G)$ decreases proportionally to $T^{-1.05}$. This decrease is larger than it is expected for electron-electron scattering limited dephasing, where a dependence of $\mathrm{rms}(G)$ proportional to $T^{-1/2}$ is predicted.[21] We attribute the strong temperature dependence to the additional contribution of thermal averaging.[19] In fact, at 1.9 K we estimate a thermal length $l_T = \sqrt{\hbar \mathcal{D}/k_B T}$, with $\mathcal{D} = 3 \times 10^{-3}\,\mathrm{m}^2/\mathrm{s}$ being the diffusion constant, of about 110 nm being comparable to L.[8] This confirms the strong contribution of thermal averaging on the temperature dependence of the fluctuation amplitude.

The phase-coherence length l_ϕ can be determined from the correlation voltage V_c, which is defined by $F_{V_g}(V_c) = \frac{1}{2} F_{V_g}(0)$ with the autocorrelation function given by $F_{V_g}(\Delta V_g) = \langle \delta G(V_g + \Delta V_g)\delta G(V_g)\rangle_{V_g}$.[19] As described by Petersen *et al.*,[22] l_ϕ is directly connected to the correlation voltage: $l_\phi = \gamma V_c^{-1/2}$, with γ depending on $\mathcal{D}$ and the electron concentration.[22] The resulting phase-coherence length l_ϕ as a function of temperature is plotted in Fig. 5 (inset). For temperatures below 1.9 K, we find a value of l_ϕ around 100 nm. Keeping in mind that for the value of $\mathcal{D}$ only a relatively rough estimate is available, the value of l_ϕ determined here is nonetheless on the same order of magnitude with the values given above.

In summary, InSb nanowire back-gate field-effect transistors have been fabricated and characterized. By comparing InSb nanowires with various diameters, we conclude that bulk transport dominates. Owing to the large electron concentration and the interface states, only a weak modulation of the nanowire resistance with back-gate voltage is achieved. This demonstrates that a metal-like degenerate electron gas exists in the nanowires, which is supported by the weak temperature dependence of the nanowire conductance. The appearance of universal conductance fluctuations at low temperatures confirms the presence of electron interference. For future investigations it could be important to control the doping in the nanowire, in order to achieve a better gate control. In addition, special attention should be devoted to the nanowire/dielectric interface. In this respect, it might be advantageous to cover the InSb nanowire by a semiconducting shell with a larger bandgap.[23] The observation that phase-coherent transport is observed at low temperatures opens up the possibility to employ interference effects for InSb nanowire-based quantum electronics.
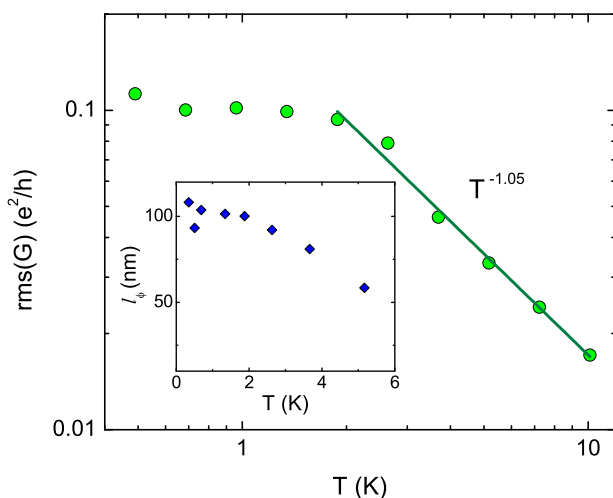
FIG. 5. Root-mean-square (rms) of the gate-dependent conductance fluctuations as a function of temperature. At $T > 1.9$ K, the fluctuation amplitude decreases as $T^{-1.05}$. The inset shows the phase-coherence length l_ϕ as a function of temperature.

[1]M. Khayer and R. Lake, IEEE Trans. Electron Devices **55**, 2939 (2008).

[2]M. Radosavljevic, T. Ashley, A. Andreev, S. Coomber, G. Dewey, M. Emeny, M. Fearn, D. G. Hayes, K. P. Hilton, M. K. Hudait, R. Jefferies, T. Martin, R. Pillarisetty, W. Rachmady, T. Rakshit, S. J. Smith, M. J. Uren, D. J. Wallis, P. J. Wilding, and R. Chau, in IEEE International Electron Devices Meeting (IEDM) Technical Digest (IEEE, 2008), p. 727.

[3]R. Winkler, *Spin Orbit Coupling Effects in Two-Dimensional Electron and Hole Systems* (Springer, Berlin, 2003).

[4]X. W. Zhang and J. B. Xia, Phys. Rev. B **74**, 075304 (2006).

[5]V. Mourik, K. Zuo, S. M. Frolov, S. R. Plissard, E. P. A. M. Bakkers, and L. P. Kouwenhoven, Science **336**, 1003 (2012).

[6]H. A. Nilsson, P. Caroff, C. Thelander, E. Lind, O. Karlström, and L.-E. Wernersson, Appl. Phys. Lett. **96**, 153505 (2010).

[7]R. Paul, M. Penchev, Z. Jiebin, M. Ozkan, M. Ghazinejad, J. Xiaoye, E. Yengel, and C. Ozkan, Mater. Chem. Phys. **121**, 397 (2010).

[8]Y. Wang, J. Chi, K. Banerjee, D. Grützmacher, Th. Schäpers, and J. G. Lu, J. Mater. Chem. **21**, 2459 (2011).

[9]D. Ercolani, F. Rossi, A. Li, S. Roddaro, V. Grillo, G. Salviati, F. Beltram, and L. Sorba, Nanotechnology **20**, 505605 (2009).

[10]D. Candebat, Y. Zhao, C. Sandow, B. Koshel, C. Yang, and J. Appenzeller, in *67th Annual Device Research Conference (DRC),* University Park, PA, USA (IEEE, 2009), p. 13.

[11]P. Caroff, M. E. Messing, B. M. Borg, K. A. Dick, K. Deppert, and L.-E. Wernersson, Nanotechnology **20**, 495606 (2009).

[12]S. R. Das, C. J. Delker, D. Zakharov, Y. P. Chen, T. D. Sands, and D. B. Janes, Appl. Phys. Lett. **98**, 243504 (2011).

[13]V. Aristov, V. Zhilin, C. Grupp, A. Taleb-Ibrahimi, H. Kim, P. Mangat, P. Soukiassian, and G. L. Lay, Appl. Surf. Sci. **166**, 263 (2000).

[14]T. Richter, Ch. Blömers, H. Lüth, R. Calarco, M. Indlekofer, M. Marso, and Th. Schäpers, Nano Lett. **8**, 2834 (2008).

[15]M. Scheffler, S. Nadj-Perge, L. P. Kouwenhoven, M. T. Borgström, and E. P. A. M. Bakkers, J. Appl. Phys. **106**, 124303 (2009).

[16]F. Werner, F. Limbach, M. Carsten, C. Denker, J. Malindretos, and A. Rizzi, Nano Lett. **9**, 1567 (2009).

[17]C. Volk, J. Schubert, M. Schnee, K. Weis, M. Akabori, K. Sladek, H. Hardtdegen, and Th. Schäpers, Semicond. Sci. Technol. **25**, 085001 (2010).

[18]B. Al'tshuler, Pis'ma Zh. Eksp. Teor. Fiz. **41**, 530 (1985) [JETP Lett. **41**, 648–651 (1985)].

[19]P. A. Lee, A. D. Stone, and H. Fukuyama, Phys. Rev. B **35**, 1039 (1987).

[20]Ch. Blömers, M. I. Lepsa, M. Luysberg, D. Grützmacher, H. Lüth, and Th. Schäpers, Nano Lett. **11**, 3550 (2011).

[21]C. W. J. Beenakker and H. van Houten, Phys. Rev. B **37**, 6544 (1988).

[22]G. Petersen, S. Estévez Hernández, R. Calarco, N. Demarina, and Th. Schäpers, Phys. Rev. B **80**, 125321 (2009).

[23]M.-E. Pistol and C. E. Pryor, Phys. Rev. B **78**, 115319 (2008).