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Aluminum oxide as passivation and gate insulator in GaAs-based field-effect transistors prepared *in situ* by metal-organic vapor deposition

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Application of GaAs-based metal-oxide-semiconductor (MOS) structures, as a “high carrier mobility” alternative to conventional Si MOS transistors, is still hindered due to difficulties in their preparation with low surface/interface defect states. Here, aluminum oxide as a passivation and gate insulator was formed by room temperature oxidation of a thin Al layer prepared *in situ* by metal-organic chemical vapor deposition. The GaAs-based MOS structures yielded two-times higher sheet charge density and saturation drain current, i.e., up to $4 \times 10^{12} \text{ cm}^{-2}$ and 480 mA/mm, respectively, than the counterparts without an oxide surface layer. The highest electron mobility in transistor channel was found to be $6050 \text{ cm}^2/\text{V s}$. Capacitance measurements, performed in the range from 1 kHz to 1 MHz, showed their negligible frequency dispersion. All these results indicate an efficient suppression of the defect states by *in situ* preparation of the semiconductor structure and aluminum oxide used as a passivation and gate insulator. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.3701584>]

The main interest on GaAs- and InP-based metal-oxide-semiconductor (MOS) devices with InGaAs channel is higher carrier mobility than in conventional Si MOSFETs can be achieved.¹ Recent studies show that an application of suitable gate insulator and passivation allows to suppress the density of defects, i.e., to prepare InGaAs channel MOS-type heterostructure field-effect transistors (MOSHFETs) with suitable performance.^{2,3} In general, two material components are essential at the preparation of a MOSFET: the semiconductor material structure and the gate dielectric. For the preparation of InGaAs channel devices, typically multilayered AlGaAs/InGaAs- and InAlAs/InGaAs-based heterostructures grown on GaAs and InP substrate, respectively, are used. They are prepared by metal-organic chemical vapor deposition (MOCVD) or molecular-beam epitaxy (MBE). At the preparation of InGaAs channel MOSHFET devices, a broad range of gate dielectrics can be applied, e.g., “classical” insulators such as SiO₂,⁴ SiN,⁵ as well as high- κ ZrO₂,⁶ HfAlO,⁷ and Ga- and Gd-based oxides.^{2,6,8} However, Al₂O₃ seems to be preferable since recently.^{3,9–11} Gate insulator is commonly used to passivate the device surface too, i.e., it is deposited on the whole source-drain access region before the gate contact is processed. Various preparation methods of the gate oxide/passivation have been investigated, such as thermal oxidation, sputtering, CVD, or atomic layer deposition (ALD). Mostly, these methods are applied in the form of an *ex situ* process, i.e., device structure is contacted with air before an insulator is deposited. Such procedure enables to create uncontrollable high density of interfacial defect states which cause a degradation of MOS device performance. Therefore, *in situ* preparation methods of semiconductor heterostructure together with a passivation and gate insulator are investigated since recently. Al₂O₃ de-

posited by ALD on *p*-GaAs in a MOCVD system was reported.¹² *In situ* preparation of GaAs and Al₂O₃ layers by MOCVD, in which isopropanol was used as an oxygen source, was also described.¹³ Drawback of these methods is that undesirable water or oxygen containing source needs to be used. Thus, there are still requirements on an optimization of GaAs-based MOS structures.

Properties of GaAs-based MOSHFETs, in which passivation and gate insulator was formed by room temperature oxidation of a thin Al layer deposited *in situ* by MOCVD, are reported in this study. Prepared devices show increased sheet charge density and saturation drain current in comparison with the unpassivated HFET counterparts. Mobility of the channel electrons up to $6050 \text{ cm}^2/\text{V s}$ was extracted for the MOSHFETs. Capacitance measurements yielded significantly lower frequency dispersion of the MOS devices than that of the HFETs. All these results underline an effectiveness and production suitability of used *in situ* preparation of GaAs-based MOSHFETs by MOCVD.

The semiconductor material structures were grown on a semi-insulating GaAs substrate using MOCVD technique. The In_{0.23}Ga_{0.77}As channel was 10 nm thick and grown on top of $\sim 200 \text{ nm}$ GaAs buffer layer. The channel carriers were achieved by placing a $3 \times 10^{12} \text{ cm}^{-2}$ silicon δ -doping into the Al_{0.3}Ga_{0.7}As barrier layer which was separated from the channel by a 4 nm Al_{0.3}Ga_{0.7}As spacer. The Al_{0.3}Ga_{0.7}As barrier was capped by a 5 nm thick GaAs layer. Finally, thin aluminum layer was deposited *in situ* on top of the GaAs cap layer in order to prepare MOSHFET device structures. The Al-oxide layer was formed by inevitable oxidation of the Al layer at room-temperature. The oxide thickness was $\sim 3 \text{ nm}$, verified by x-ray reflectivity measurements. Schematic cross-section of the MOS layer structure is shown in Fig. 1. Structures grown under identical conditions but without Al layer were prepared for comparison too. The device

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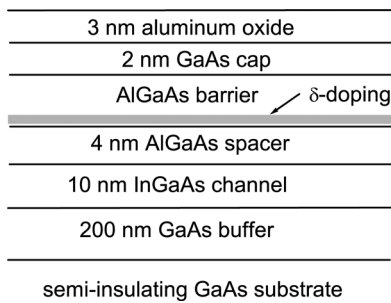


FIG. 1. Schematic cross-section of the MOS layer structure.

preparation consisted of conventional processing steps known for GaAs-based devices, i.e., mesa formation, Ni/AuGe/Ni/Au ohmic contacts annealed at 450 °C, and Ti/Pt/Au gate contacts. The MOSFETs and HFET counterparts with a gate length of 2.5 μm and a gate width of 50 and 100 μm as well as fat-FETs ($L_G = 100 \mu\text{m}$) and large area capacitors (100 \times 100 and 200 \times 200 μm^2 gate contact area) were prepared.

Static output measurements on the AlGaAs/InGaAs/GaAs structures without and with an Al oxide typically yielded I – V characteristics as shown in Fig. 2(a). The saturation drain current up to 260 mA/mm and 480 mA/mm at $V_G = 1 \text{ V}$ was obtained for the metal-semiconductor (MS) and MOS structures, respectively (Fig. 2(b)). Higher saturation drain current in the MOS structures can be explained due to an increase of the sheet charge density n_s and/or drift velocity of carriers v_d , as $I_{DS}/W_G = q \cdot n_s \cdot v_d$. This indicates on high effectiveness of the *in situ* prepared Al-oxide as a gate insulator and passivation. The peak extrinsic transconductance was found to be $\sim 120 \text{ mS/mm}$ ($V_G \cong -1 \text{ V}$) and $\sim 150 \text{ mS/mm}$ (-2 V) for the MS and MOS structures, respectively. One would expect slightly lower transconductance in the structures with Al oxide comparing to the counterpart without Al due to increased barrier-channel separation. Observed opposite effect might be explained by an enhancement of the effective velocity of the channel electrons in the MOS structure,¹⁴ as $g_m \cong C_{GS} \cdot v_d$ and the gate capacitances for the MS and MOS structures differ very slightly (as described below).

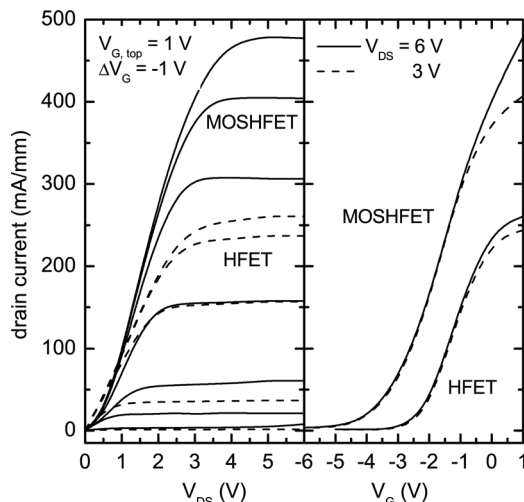
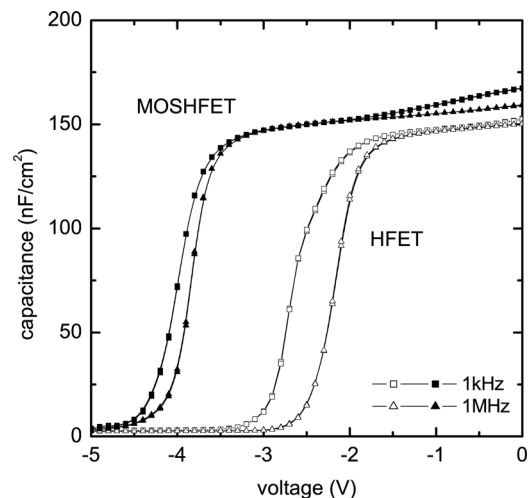


FIG. 2. Typical output (left) and transfer (right) characteristics of Al-ox/AlGaAs/InGaAs/GaAs MOSHFET in comparison with HFET counterpart.

Typical results of the room temperature C – V measurements performed at 1 kHz and 1 MHz on the structures with and without Al oxide are shown in Fig. 3. Capacitances at zero bias are nearly the same for both types of structures. This follows from large difference of the barrier and oxide thicknesses ($d_b > d_{ox}$) as well as high dielectric constant of used aluminum oxide ($\epsilon = 7$ – 10 for Al_2O_3 and even 22 for AlO_2).^{15,16} The capacitance ratio $C_{\text{HFET}}/C_{\text{MOSHFET}} = 1 + (d_{ox}/d_b) \cdot (\epsilon_b/\epsilon_{ox}) = 1.03$ – 1.07 considering possible range of the dielectric constant. Unfortunately, exact composition of the Al-oxide and thus also its dielectric constant is not known. However, formation of AlO_2 should be preferable for Al oxidation at room-temperature.¹⁵

Relatively sharp transition from accumulation to depletion in measured C – V curves shown in Fig. 3 can be observed for both types of structures. On the other hand, lower frequency dispersion of the MOS capacitance than that of the MS one follows from the measured data—the gate voltage shift at $C_0/2$ for $\Delta f = 1 \text{ kHz}$ – 1 MHz is $\Delta V_G = 0.17 \text{ V}$ and 0.5 V for MOS and MS structures, respectively. Frequency dispersion with a hump in C – V curves in the depletion region is often reported on GaAs-based MOS capacitors.^{11,13} Such effects are observed in structures with high density of defect states. This leads us to assume that the density of trap states should be low in our MOS structures. Better picture about this statement can be demonstrated by C – f dependences measured at a constant gate voltage chosen to be in depletion region, as shown in Fig. 4. Capacitance of the MS structures, i.e., without Al oxide, decreased significantly in the whole frequency range used. On the other hand, negligible frequency dispersion of the capacitance was observed for the MOS structures. This is an additional argument for high effectiveness of the *in situ* prepared Al-oxide used as a gate insulator and passivation.

An integration of the C – V curves yielded the sheet charge density of $(3.8$ – $4) \times 10^{12} \text{ cm}^{-2}$ and $(2$ – $2.3) \times 10^{12} \text{ cm}^{-2}$ ($V_G = 0 \text{ V}$) for the MOSHFETs and HFETs, respectively. The drain-source conductivity measurements combined with the n_s – V_G data were used to evaluate mobility of the channel electrons, as $\mu_e = (L_G \cdot G_{ch}) / (q \cdot W_G \cdot n_s)$. Conductance was

FIG. 3. C – V characteristics of Al-ox/AlGaAs/InGaAs/GaAs MOSHFET (full marks) and HFET counterpart (open marks) measured at 1 kHz and 1 MHz.

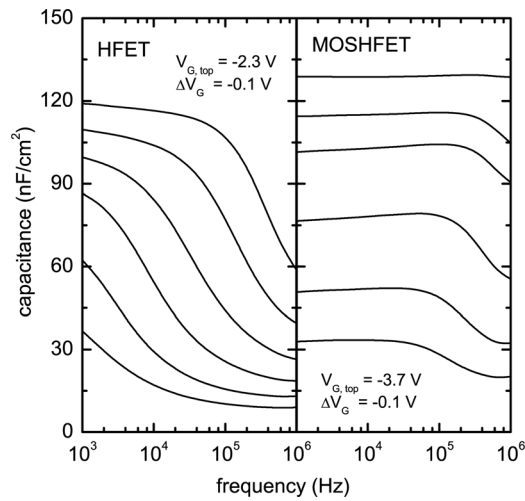


FIG. 4. Capacitance vs frequency for Al-ox/AlGaAs/InGaAs/GaAs MOSHFET (full marks) and HFET counterpart (open marks). Note that the gate voltage was chosen to be in the depletion region.

measured on the fat-FET devices at low drain voltage to reduce an influence of the source and drain resistances. Typical MOSHFET and HFET data of the mobility as a function of the sheet charge density are shown in Fig. 5. Peak values of the mobility are 6050 and 4220 $\text{cm}^2/\text{V}\cdot\text{s}$ for the MOSHFET and HFET, respectively. The MOSHFET mobility of 6050 $\text{cm}^2/\text{V}\cdot\text{s}$ can be well compared with the highest value of 6155 $\text{cm}^2/\text{V}\cdot\text{s}$ reported on GaAs-based InGaAs channel MOS devices with GdGa-based oxide.⁸ However, significantly lower mobility down to 4730 $\text{cm}^2/\text{V}\cdot\text{s}$ was also reported for GaAs- and InP-based MOS device structures.⁹

Experiments related to the trap states evaluation using frequency dependent conductance measurements are in progress, and detailed analysis will be reported elsewhere. Preliminary results show that the density of trap states is in the range of $(1.4\text{--}6.2) \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$, and their time constant is in the range of some microseconds. Similar density of trap states in the range of $10^{12} \text{cm}^{-2} \text{eV}^{-1}$ was reported recently for $\text{Al}_2\text{O}_3/\text{GaAs}$ capacitors prepared by MBE.¹⁷

Presented results demonstrate high capability of used device fabrication method in which the GaAs-based semiconductor structure and aluminum oxide as a passivation and

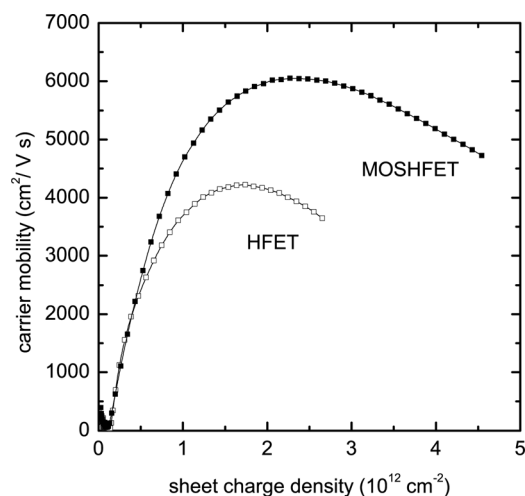


FIG. 5. Carrier mobility vs sheet charge density for Al-ox/AlGaAs/InGaAs/GaAs MOSHFET (full marks) and HFET counterpart (open marks).

gate insulator are prepared *in situ* by MOCVD. Basic advantages here are two: (1) The semiconductor surface is covered by an insulator without exposing it to air and (2) undesirable oxygen containing source does not need to be used at the *in situ* preparation. Beside the fact that properties of oxide/GaAs interface are not fully clear yet, it is believed that an interface without residual arsenic oxide can be crucial point to obtain low density of interfacial defect states.¹³ In our procedure, the GaAs surface was covered by an Al layer before native oxide was formed. This is probably the basic reason for obtained good MOS performance, i.e., an increase of n_s and consequently of I_{DS} about 2–times and low $C\text{--}f$ dispersion compared with the HFETs. Evaluated high carrier mobility of 6050 $\text{cm}^2/\text{V}\cdot\text{s}$ in the InGaAs channel also supports our conclusion. Here, it should be noted that the highest mobility of 6600 $\text{cm}^2/\text{V}\cdot\text{s}$, reported for InP-based InGaAs channel MOS devices, was obtained on MBE structures covered with arsenic cap before transferring to ALD equipment to deposit Al-oxide.³ Additional advantage is that the gate oxide formed from high- κ insulator is relatively thin, only ~ 3 nm. This is required for suitable high-frequency performance. Exact composition of prepared Al oxide, i.e., if preferably Al_2O_3 or AlO_2 was created, is not clear yet and needs additional studies. Finally, it should be mentioned that proposed *in situ* preparation method of GaAs-based MOS structures can be useful for mass production of GaAs MOS devices. On the other hand, additional studies related to reliability issues, high frequency performance, and defect states evaluation need to be made in the future.

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¹M. Heyns and W. Tsai, *MRS Bull.* **34**, 485 (2009).

²M. Hong, J. Kwo, T. D. Lin, and M. L. Huang, *MRS Bull.* **34**, 521 (2009).

³S. J. Bentley, M. Holland, X. Li, G. W. Paterson, H. Zhou, O. Ignatova, D. Macintyre, S. Thoms, A. Asenov, B. Shin, J. Ahn, P. C. McIntyre, and I. Thayne, *IEEE Electron Device Lett.* **32**, 494 (2011).

⁴H. Y. Lee and Y.-F. Lin, *Semicond. Sci. Technol.* **25**, 015005 (2010).

⁵Y. Liu, H. Wang, and K. Radhakrishnan, *Thin Solid Films* **515**, 4387 (2007).

⁶J. Hu, K. C. Saraswat, and H.-S. P. Wong, *Appl. Phys. Lett.* **99**, 092107 (2011).

⁷M. Zhu, H.-Ch. Chin, G. S. Samudra, and Y.-Ch. Yeo, *Appl. Phys. Lett.* **92**, 123513 (2008).

⁸M. Passlack, R. Droopad, K. Rajagopalan, J. Abrokwhah, R. Gregory, and D. Nguyen, *IEEE Electron Device Lett.* **26**, 713 (2005).

⁹H. Zhao, Y.-T. Chen, J. H. Yum, Y. Wang, F. Zhou, F. Xue, and J. C. Lee, *Appl. Phys. Lett.* **96**, 102101 (2010).

¹⁰M. A. Negara, D. Veksler, J. Huang, G. Ghibaud, P. K. Hurley, G. Bersuker, N. Goel, and P. Kirsch, *Appl. Phys. Lett.* **99**, 232101 (2011).

¹¹Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, *IEEE Electron Device Lett.* **32**, 485 (2011).

¹²C.-W. Cheng and E. A. Fitzgerald, *Appl. Phys. Lett.* **93**, 031902 (2008).

¹³C.-W. Cheng, G. Apostolopoulos, and E. A. Fitzgerald, *J. Appl. Phys.* **109**, 023714 (2011).

¹⁴P. Kordoš, D. Gregušová, R. Stoklas, K. Čičo, and J. Novák, *Appl. Phys. Lett.* **90**, 123513 (2007).

¹⁵H. Kaiju, Y. Otaka, and K. Shiiki, *J. Magn. Magn. Mater.* **303**, 256 (2006).

¹⁶P. Kordoš, D. Gregušová, R. Stoklas, Š. Gaži, and J. Novák, *Solid-State Electron.* **52**, 973 (2008).

¹⁷C. Merckling, Y. C. Chang, C. Y. Lu, J. Penaud, G. Brammertz, M. Scarrrozza, G. Pourtois, J. Kwo, M. Hong, J. Dekoster, M. Meuris, M. Heyns, and M. Caymax, *Surf. Sci.* **605**, 1778 (2011).