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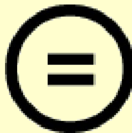

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공학박사학위논문

Stretchable and Wearable Carbon Nanotube Electronics

신축성 있고 착용 가능한 탄소 나노튜브 기반 전자 기술

2020년 8월

서울대학교 대학원

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구 자 훈

Stretchable and Wearable

Carbon Nanotube Electronics

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUESTMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY IN ENGINEERING AT THE GRADUATE SCHOOL OF SEOUL NATIONAL UNIVERSITY

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Abstract

Stretchable and Wearable Carbon Nanotube Electronics

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Networks of carbon nanotubes (CNTs) are a promising candidate for use as a basic building block for next-generation soft electronics, owing to their superior mechanical and electrical properties, chemical stability, and low production cost. In particular, the CNTs, which are produced as a mixture of metallic and semiconducting CNTs via chemical vapor deposition, can be sorted according to their electronic types, which makes them useful for specific purposes: semiconducting CNTs can be employed as channel materials in transistor-based applications and metallic CNTs as electrodes. However, the development of CNT-based electronics for soft applications is still at its infant stage, mainly limited by the lack of solid technologies for

developing high-performance deformable devices whose electrical performances are comparable to those fabricated using conventional inorganic materials. In this regard, soft CNT electronics with high mechanical stability and electrical performances have been pursued.

First, wearable nonvolatile memory modules and logic gates were fabricated by employing networks of semiconducting CNTs as the channel materials, with strain-tolerant device designs for high mechanical stability. The fabricated devices exhibited low operation voltages, high device-to-device uniformity, on/off ratios, and on-current density, while maintaining its performance during ~30% stretching after being mounted on the human skin. In addition, various functional logic gates verified the fidelity of the reported technology, and successful fabrication of non-volatile memory modules with wearable features has been reported for the first time at the time of publication.

Second, the networks of semiconducting CNTs were used to fabricate signal amplifiers with a high gain of ~80, which were then used to amplify electrocardiogram (ECG) signals measured using a wearable sensor. At the same time, color-tunable organic light-emitting diodes (CTOLEDs) were developed based on ultra-thin charge blocking layer that controlled the flow of excitons during different voltage regimes. Together, they were integrated to construct a health monitoring platform whereby real-time ECG signals could be detected while simultaneously notifying its user of the ECG status via color changes of the wearable CTOLEDs.

Third, intrinsically stretchable CNT transistors were developed, which was

enabled by the developments of thickness controllable, vacuum-deposited stretchable dielectric layer and vacuum-deposited metal thin films. Previous works employed strain-tolerant device designs which are based on the use of filamentary serpentine-shaped interconnections, which severely sacrifice the device density. The developed stretchable dielectric, compatible with the current vacuum-based microfabrication technology, exhibited excellent insulating properties even for nanometer-range thicknesses, thereby enabling significant electrical performance improvements such as low operation voltage and high device uniformity/reproducibility, which has not been realized in the most advanced intrinsically stretchable transistors of today.

Keywords: carbon nanotubes, flexible electronics, stretchable electronics, wearable electronics, soft electronics

Student number: 2014-31111

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Chapter 1. Introduction

1.1 Discovery of CNTs and their benefits for soft electronic applications

Recent efforts in the semiconductor material and device research have focused on the development of soft electronics with unusual form factors and functions, as they offer a wide variety of applications such as wearable and implantable biomedical devices,[1-3] electronic papers,[4-6] flexible and stretchable circuits,[7-9] and skin-inspired robotic systems with multiple sensing capabilities.[10-12] In often cases, a sustainable performance is required for these soft electronic devices during dynamic circumstances such as undergoing an extreme mechanical deformation. However, since most of the materials used in conventional planar electronic devices are not adequate due to their brittle and rigid nature, early stages of research focused on developing novel materials with excellent electrical and mechanical properties. A number of emerging materials have been reported including inorganic nanomaterials,[13-15] organics and small molecule materials,[16-18] metal oxides,[19-21] and two-dimensional (2D) nanomaterials.[22-24] Among the various materials, single-walled carbon nanotubes (CNTs) have stood out as an excellent and most adequate material choice owing to their high intrinsic carrier mobility, excellent mechanical stability, and good processability.[25-27] **Table 1.1** shows a brief comparison on prospective materials for soft electronics, focusing on transistor properties, deformability, cost, processability, and stability.

CNTs are carbon-based cylindrical nanostructures with diameters generally in the range of a few nanometers and lengths in the range of few hundred nanometers,[28-30] and they can be categorized into single-walled nanotubes (SWNTs) and multi-walled nanotubes (MWNTs). While MWNTs are metallic, the electronic types (semiconducting or metallic) of SWNTs can be varied according to their chirality.[31,32] Ever since their first discovery in 1991,[33] the early stages of CNT research focused on their synthesis methods as depicted in **Fig. 1.1**. These methods include arc discharge,[34-36] laser ablation,[37,38] chemical vapor deposition (CVD),[39-41] and high-pressure carbon monoxide disproportionation (HiPCO).[42,43] As a result of intense research, significant progress have been achieved in terms of lowering the production cost, massive production with high selectivity of SWNTs, and control over the diameter, length, and morphology of the CNTs. However, the as-synthesized SWNTs cannot be directly applicable for use as channel material in transistor applications since the as-synthesized SWNTs comes in mixture of semiconducting and metallic types by nature.[44-46]

*** Some contents of this chapter were published in *Nanotechnology* (2019, 30, 132001)**

Materials		Transistor Properties			Deformability		Cost	Solution-Processability	Stability
		On/off ratio	Mobility (cm^2/Vs)	On-current density (μA/μm)	Flexible	Stretch-able			
CNT networks[25]		~10^5	~80	~10	○	○	Low	○	Excellent
Inorganic nanomaterials	Si NWs[13]	~10^5	~560	~200	○	×	High	○	Excellent
	Si NMs[14]	~10^5	~490	NA	○	×	High	×	Excellent
	GaAS NWs[15]	~10^5	NA	~430	○	×	High	○	Excellent
Organics	DNTT[1]	~10^7	~1	~0.12	○	△	Low	○	Good
	CONPHINE[2]	~10^4	~1	~0.1	○	○	Low	○	Good
	Pentacene[16]	~10^6	~2	~1.6	○	×	Low	○	Average
Metal oxides	IZO[19]	~10^8	~10	~0.1	○	×	Low	○	Good
	In_2O_3[20]	~10^7	~3	~0.1	○	×	Low	○	Good
	a-IGZO[21]	~10^3	~10	~0.1	○	×	Low	○	Good
2D nanomaterials	MoS_2[22]	~10^7	~30	NA	○	×	Low	×	Good
	WSe_2[23]	~10^6	~250	NA	○	×	Low	×	Average
	Black Phosporus[24]	~10^5	~400	~0.1	○	×	Low	×	Poor

Table 1.1. Comparison of CNTs and other semiconducting materials for use as channel material in soft electronics.

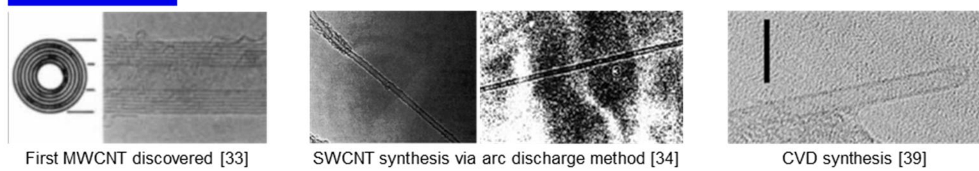


Figure 1.1. First discovery of CNTs and development of their synthesis methods.

1.2 Electrical sorting of CNTs

Extensive research efforts have been devoted to develop effective separation or sorting methods of as-synthesized SWNTs according to their electronic types (**Fig. 1.2**). In particular, various solution-based techniques have been developed that typically rely on the use of chirality-selective binding polymer dispersants and surfactants such as DNA-assisted sorting,[47-49] gel chromatography,[50-52] density gradient ultracentrifugation,[53,54] and conjugated polymer-assisted sorting.[55,56] These techniques have matured over the past decade such that it is not hard to purchase SWNT solutions with high purities of 99.999% in the market.

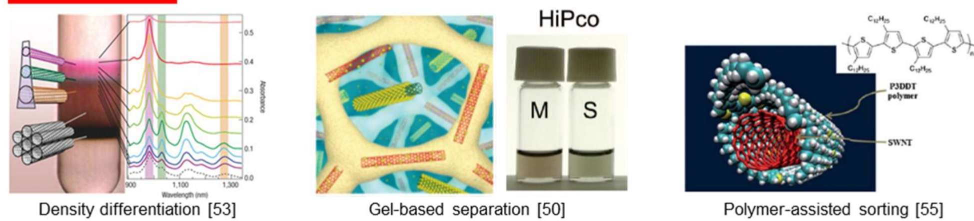


Figure 1.2. Sorting methods of semiconducting CNTs.

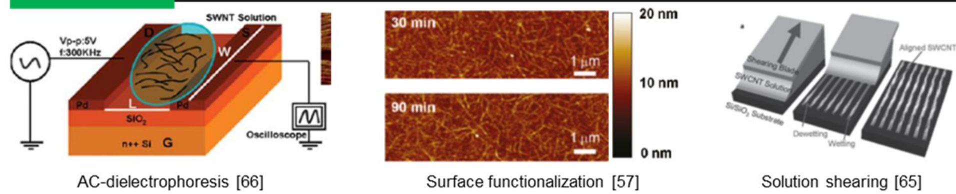
1.3 Deposition methods of solution-processed semiconducting CNTs

The deposition of semiconducting CNTs into a uniform thin film over a large area with optimized density is crucial in terms of minimizing the device-to-device performance variation and achieving high performances including high on/off ratios, carrier mobility, and current densities. Several deposition methods have been devised, such as soaking methods[57-59] and printing methods[60-62] for large-area deposition of random network semiconducting CNTs with excellent uniformity, and aligned deposition methods including Langmuir-Blodgett assembly,[63,64] solution shearing,[65] and AC-dielectrophoresis[66-68] for high electrical performances. Based on these techniques, the first generation of soft electronic devices based on SWNT thin film transistors are being reported, with novel applications including but not limit to user-interactive electronic skins (e-skins)[69] and stretchable/wearable circuits with multiple functionalities (**Fig. 1.3**).[70,71]

CNT field-effect transistors (FETs), the basic building blocks of soft CNT electronics, employ dense networks of semiconducting CNTs as the channel, which can reconfigure their percolation network with respect to the applied strain, thus maintaining their electrical performances during deformed states. Therefore, thin films of semiconducting CNT networks are highly desirable for soft electronics applications subject to extreme deformations. To form the networks, their deposition methods should be facile, reliable in terms of uniformity, and scalable to large area. In addition, the electrical performances of the CNT FETs such as carrier mobility, current on/off ratio, and on current density should be optimized.

CVD growth of CNTs is the most commonly used method to produce CNTs for electronic devices due to the superior electrical performances originating from relatively long nature of the synthesized CNTs and absence of bundles, which both reduce the number of tube-to-tube junctions that affect the resistance. However, they are not suitable for soft electronic applications, due to the following reasons: the thermal budget of the CVD-growth method is incompatible with most of the compliant substrates used in soft electronics and thus, the as-synthesized CNTs must be transferred from the original substrate. During such process, the CNTs are subject to damage, breakage, and consequent shortening, which results in the deterioration of the device performance. Furthermore, the elimination of the metallic CNTs after the transfer is troublesome, and their elimination often results in device-to-device performance variation as the metallic CNTs are randomly distributed inside the networks. One advantage for using solution-processed semiconducting CNTs is that post-treatment for elimination of metallic CNTs can be avoided. Furthermore, solution-processed semiconducting CNTs can be directly deposited in network forms on deformable substrates over a large area with relatively high uniformity.

a **2010 ~ 2015:** Deposition methods of solution-processed s-CNTs



b **2010 ~ present:** Application of solution-processed s-CNTs in soft electronics

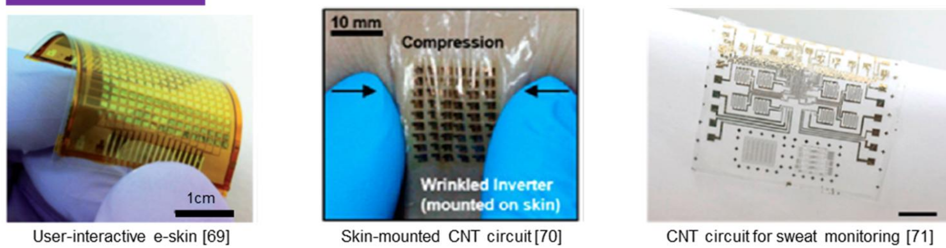


Figure 1.3. (a) Deposition methods of semiconducting CNTS and (b) their application in soft electronics.

1.3.1 Printing methods for s-SWNT network deposition

Printing methods such as dry transfer printing[72-74] or solution-based inkjet printing[75-77] are the most common methods to deposit various layers on deformable substrates. In 2011, Sun *et al*. reported the fabrication of high-performance FETs and integrated circuits on a flexible substrate using a customized dry transfer printing method of CVD-grown CNTs.[78] In specific, a simple gas-phase filtration method was used to directly collect the as-synthesized SWNTs on a membrane filter, which were then transferred from the filter to the target substrate. **Figure 1.4a** schematically illustrates such CNT synthesis and transfer processes, whereby the process is finalized by dissolving the filter in acetone, patterning the SWNT film by etching the outside region of the channel via O_2 plasma. Notably, the transferred CNT film consisted of individual and rather straight, long (~10 μm in length) nanotubes (Fig. 1.4b), which was a quite unique morphology when compared to those CNT networks prepared by other solution-based techniques. It can also be seen from the scanning electron microscope (SEM) image of **Fig. 1.4b** that the junctions formed by contacting nanotubes were mainly Y-type rather than X-type, which are known to have lower junction resistance than that of the X-junctions. The unique morphology of the transferred CNT film resulted in high performance of the FETs, with on/off ratios higher than 10^6 and effective device mobility of 35 $cm^2V^{-1}s^{-1}$ at a low V_{ds} of -0.5 V (**Fig. 1.4c**). However, the fabricated FETs suffered a severe loss in on/off ratios for those that contained metallic nanotubes within the transferred CNT film, thus leading to a low reliability in terms of device-to-device performance variation. For

such reasons, the direct transfer of CVD-grown CTs has not been considered a practical technique for soft electronic applications which require large-area uniformity.

Direct solution-based printing methods such as inkjet printing, on the other hand, can enable high-throughput and large-area fabrication of CNT FETs, with the possibility of avoiding additional photolithography or other expensive lithographic techniques. In this regard, several research groups have devoted extensive research efforts to investigate inkjet -printed SWNTs films for potential use in soft electronic applications.[79-81] Okimoto *et al.* successfully demonstrated that a relatively high on/off ratio of ~104 and a moderate carrier mobility of ~4 $cm^2V^{-1}s^{-1}$ can be achieved in inkjet-printed CNT FETs by controlling the CNT density during inkjet printing (**Fig. 1.4d**).[77] In another research by Jung *et al.*, the possibility of mass production of fully-printed flexible CNT devices have been demonstrated by combining roll-to-roll printing and inkjet printing methods.[82] The gate, dielectric layer, and source/drain electrodes were formed by roll-to-roll printing, followed by inkjet printing of CNT networks. Figure 1.4e shows an optical image of the source-channel-drain region, and the magnified view shows an SEM image of the inkjet-printed CNT networks. Except for a few variations in device performances which were mainly attributed to misalignment of the printed source/drain electrodes and thickness difference of the dielectric layers, the FETs exhibited negligible performance variation in terms of transfer and output curves. Using the scalable technique, the authors further reported the successful fabrication of various logic gates, ring oscillators, and radio frequency

identification tags. In all, recent progresses in printing technology show promising results towards commercialization of CNT-based devices for soft electronic applications.

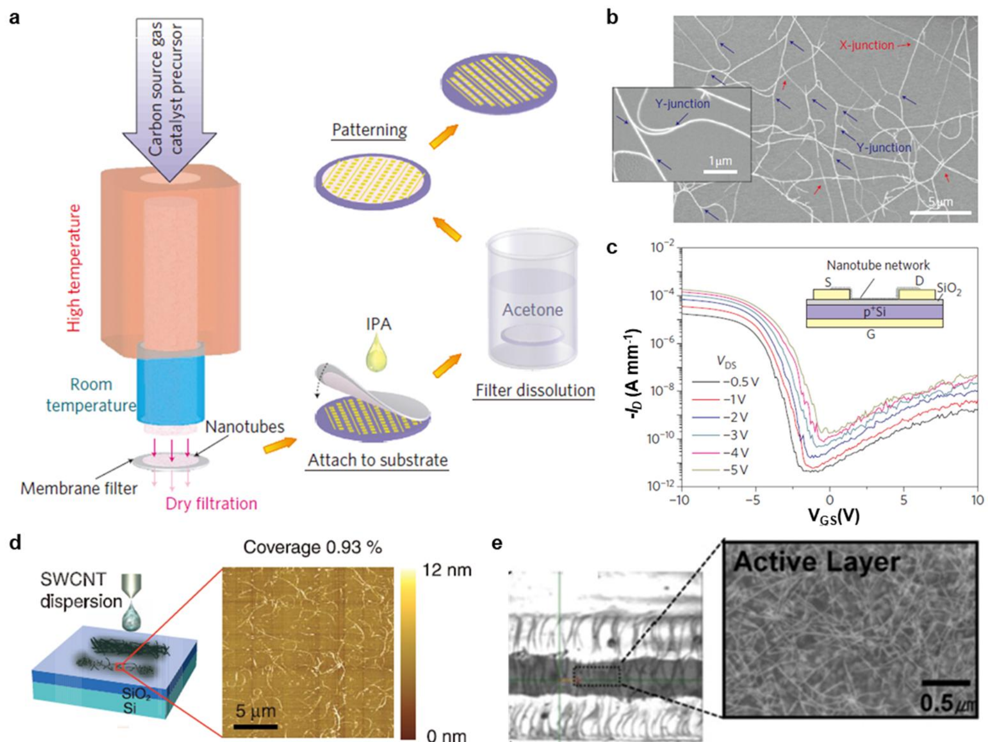


Figure 1.4. Printing methods of semiconducting CNT thin films for active layer of transistors. (a) Schematics of CNT growth, film collection by a filter, transfer, and patterning. (b) SEM image of transferred CNT film. (c) Transfer curve of a typical CNT FET with various applied drain voltages. (d) Schematic representation of CNT FET fabrication using inkjet printing and the corresponding atomic force microscope (AFM) image. (e) SEM image of the active layer of an all-printed CNT FET.

1.3.2 Soaking methods for semiconducting CNT network deposition

Soaking method refers to literal immersion of the target substrates into s-SWNT solutions for deposition of the CNT networks. It is the most common method adopted these days for fabrication of CNT FETs in soft electronic applications since it does not require the use of additional expensive tools or equipment such as printers, thereby potentially reducing the fabrication cost. Moreover, accurate control of the film density can be achieved by controlling the duration of immersion and concentration of the CNT solution. The CNTs deposited on unwanted regions of the substrate can then be easily removed by conventional photolithography processes and a brief expose to O_2 plasma. On these terms, the soaking methods have proven to be the most efficient tool for deposition of CNT films on deformable substrates using highly purified semiconducting CNT solutions.

Early reports that adopted soaking methods used self-assembled monolayer (SAM) of aminosilane groups such as aminopropyltriethoxy silane (APTES) or aminopropyltrimethoxy silane (APTMS) to generate amine-terminated surface for deposition of CNTs films.[83-85] Due to the high affinity of CNTs to the amine-functionalized surfaces, large-area uniformity and controllable density could be achieved within considerably short soaking time. In 2012, Liyanage *et al.* demonstrated a wafer-scale fabrication of CNT FETs using APTMS as the SAM and soaking the wafer in a CNT solution (**Fig. 1.5a**).[86] To precisely control the uniformity and density of the deposited CNT film, a diluted solution was used with sufficient soaking time, which resulted in deposition of near-mono-layered networks of CNTs

with thickness of 2.3 nm (AFM image of **Fig. 1.5a**). Despite the excellent uniformity and density of the CNT networks, the electrical performances of the fabricated FETs exhibited rather low performances, requiring supply of high gate voltages to switch the devices (**Fig. 1.5b**) and moderate average on/off ratios of $10^3 \sim 10^4$ (**Fig. 1.5c**). This is mainly ascribed to the shortening of the CNTs during the processes of sorting and diluting, and to the selection of materials for gate, dielectric, and source/drain.

Meanwhile, Takahashi *et al.* have reported a quick deposition of CNT film using poly-*l*-lysine as the SAM.[87] It can be seen from the AFM images in Fig. 1.5d that even for a short soaking time of 5 min, an abundance of SWNTs was deposited on the functionalized surface. The authors have systematically investigated the effect of soaking time on the electrical performances of SWNT-based FETs, where a trade-off relationship between on-current density, carrier mobility, and on/off ratio was found with respect to the amount of soaking time (**Figs. 1.5e** and **1.5f**). Longer soaking time resulted in denser networks of CNTs with multilayers, which consequently led to the loss of gate controllability on the CNTs and hence the FETs exhibited lower on/off ratios. On the contrary, since the amount of CNTs participating on current delivery significantly increased with longer soaking times, the on-current density as well as carrier mobility was found to be superior for the FETs with denser SWNT networks as their channel. The developed method proved to be highly efficient in terms of scalability and reliability, and in fact, several novel applications of CNT-based soft electronics have been further reported from the same research group in the following years.

More recently, CNT FETs with excellent electrical performances of low power consumption, high on/off ratios, large-scale performance uniformity, and low subthreshold voltage swing have been reported, which adopted the soaking method for deposition of CNT networks. Instead of using SAM to shorten the deposition time, sufficient soaking time of over 20 hours were allowed to ensure well-percolated networks of CNTs on 10 nm Y_2O_3 dielectric (**Fig. 1.5g**).[88] FETs fabricated from such CNT network film exhibited excellent p-type transfer characteristics at low gate bias voltage of -3 to 1 V, with on/off ratios as high as ~10^5 (**Figs. 1.5h** and **1.5i**). The excellent uniformity and high performance of the developed FETs allowed for fabrication of medium-scale integrated circuits such as various logic gates, multiple stage ring oscillators, and 4-bit adders which comprises of 140 transistors. As such, the soaking method are deemed a promising method for future soft electronic applications, due to their high yield, large-scale processability, low cost, and no requirement on the thermal budget, although they can be time-consuming on some occasions. In addition, the resulting random network nature is highly tolerant of metallic nanotubes due to the averaging effect of massive CNTs, which is beneficial in that s-SWNT solutions with a 100% purity is nearly impossible to attain.

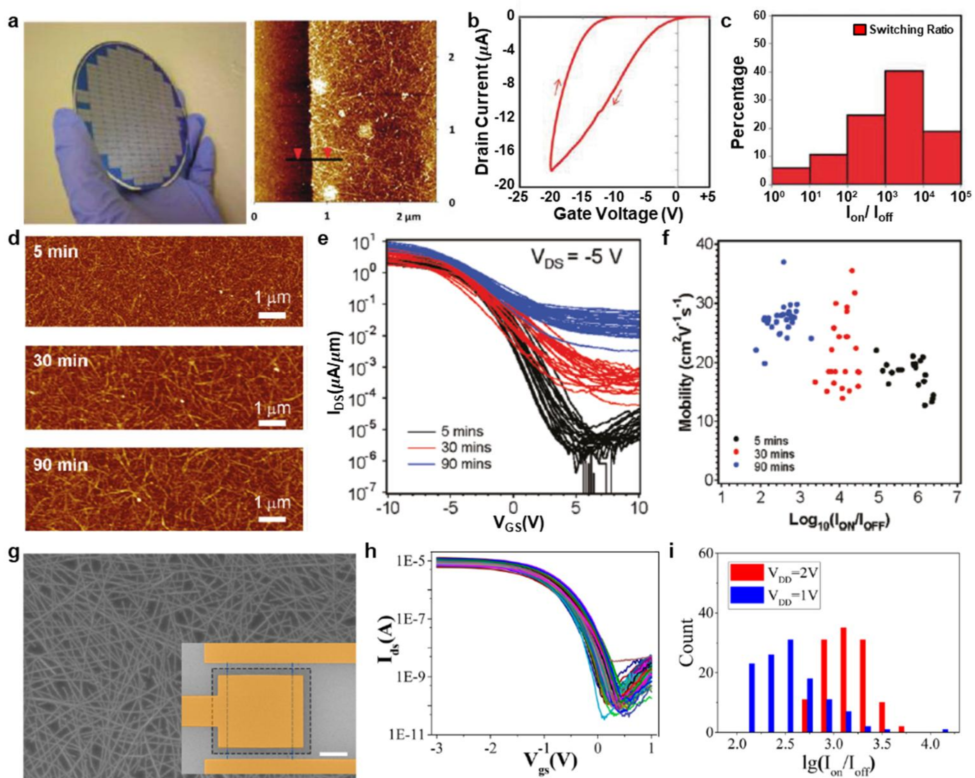


Figure 1.5. Soaking methods for semiconducting CNT network deposition. (a) Wafer-scale fabrication of CNT FETs using a soaking method, and an AFM image of a channel region. (b) Representative CNT FET transfer curve of. (c) Histogram of the on/off ratios of wafer-scale CNT FETs. (d) AFM images taken after different semiconducting CNT deposition times on poly-*l*-lysine-coated substrate using a soaking method. (e) Corresponding cumulative transfer characteristics and (f) on/off ratios and mobility measurements of CNT FETs. (g) SEM image of CNT networks deposited on a Y_2O_3 dielectric after 20 h of soaking in s-SWNT solution. Electrical characterization of CNT FETs corresponding to (h) 120 transfer curves and (i) a histogram of the on/off ratios at different drain voltages.

1.3.3 Aligned CNT deposition methods

The deposition methods discussed in section 1.3.1 and 1.3.2 generally produces random networks of CNT films, and with recent advances in fabrication and design of FETs, they exhibit excellent electrical performances in terms of high on/off ratios and current carrying capacities. However, the carrier mobility of these devices, which are usually in the range of few tens of $cm^2V^{-1}s^{-1}$, can be substantially increased by adopting a different morphology of the deposited network. In fact, the critical limiting factor of carrier transport in CNT FETs is the number of tube-to-tube junctions within the CNT network,[89-91] which can be significantly reduced by aligning the nanotubes.

Among the various alignment techniques, one of the simplest is the ac-dielectrophoresis, where the CNTs inside a solution, placed in between two electrodes, can be simply aligned by applying an ac-voltage to the electrodes (**Figs. 1.6a and 1.6b**).[92-94] Shekhar et al. reported that well-ordered arrays of nanotubes can be generated, of which their density can be varied with respect to the concentration of the CNT solution and the frequency of the applied ac-voltage.[92] By optimization of the control variables, maximum density of 30 CNTs/μm could be achieved (**Fig. 1.6c**). Despite the simplicity and effectiveness of the alignment method, the ac-dielectrophoresis proved to be inadequate for fabrication of soft electronic devices due to their nature of attracting and aligning metallic nanotubes, even with solutions enriched with semiconducting CNTs. The FETs fabricated using the ac-dielectrophoresis method exhibited relatively low on/off ratios, and additional

methods were required to remove the unwanted metallic nanotubes, which consequently resulted in severe device-to-device performance in large-area applications.

In 2013, Cao *et al.* reported a scalable method for aligning CNTs based on Langmuir-Schaefer assembly.[64] **Figure 4d** schematically illustrates the process of the alignment technique, whereby an extremely high nanotube density of over 500 SWNTs/μm could be obtained (**Fig. 1.6e**). FETs fabricated using such dense networks of aligned CNTs exhibited unprecedented current carrying capacities of 120 μA/μm-1, but due to the existence of metallic nanotubes even with the use of 99% purity s-SWNT solutions, a low on/off ratio of ~ 10^3 was reported. A year later, Joo *et al.* reported an evaporation-induced self-assembly method for aligning CNTs on the surface of a hydrophobic substrate.[95] Figure 1.6f depicts a brief schematic of the alignment method, where an organic solvent containing high-purity s-SWNTs is dropped on water, inducing diffusion of the organic solvent at the water-air interface to deposit aligned CNTs on a vertically-immersed hydrophobic substrate with packing densities of ~50 CNTs/μm (SEM image of **Fig. 1.6f**). Notably, the resulting FETs exhibited high on/off ratios of over 106, which is a direct result of using originally high-purity solution of 99.9% s-SWNTs and lesser chance to include metallic tubes within the aligned CNT films with comparably lower packing densities.

Park *et al.* investigated a solution shearing method, which was originally introduced to create densely packed single-crystalline structures of organic semiconductors with enhanced mobility, to produce well-ordered arrays of

semiconducting CNTs on alternating patterns of superhydrophobic and hydrophilic regions.[65] **Figure 1.6g** illustrates a brief schematic of the shearing process for alignment of the CNTs and the resulting SEM image of the aligned CNTs is shown in **Fig. 1.6h**. The density of the nanotubes was approximately 150 ~ 200 CNTs/μm in the aligned region, with highly focused orientation angles below ± 15° (Fig. 1.6i). Comparative analysis on electrical performances of FETs based on aligned and random networked films of CNTs revealed a significant difference in on-current density and carrier mobility, where the FETs built from aligned CNTs exhibited current carrying capacity as high as 45 times higher and mobility 10 times higher than FETs of random network CNTs. It is worthwhile to mention that the high density of nanotubes compensated for on/off ratio of the FETs due to close proximity and multi-layered nature of the CNTs, resulting in the reduction of electrostatic control of individual CNTs.

As verified from the reports on alignment methods of CNTs and their application as channel material in FETs, there are several limiting factors that can be a substantial obstacle for the use of aligned CNT films in soft electronic applications. First, many of the introduced methods are highly dependent on the purity of the s-SWNT solution, as even a single metallic nanotube can significantly deteriorate the electrical performances in terms of on/off ratio. Post treatments for elimination of metallic nanotubes are troublesome and they also affect the device-to-device performance uniformity, which is a critical issue in large-area applications. Second, the electrical performance boost of aligned CNT films is often limited to short-

channel devices, where the channel length is comparable to the length of the nanotubes. However, many of the FETs used in current soft electronic applications adopt larger dimensions than that of the nanotube length, focusing on the stability issues during deformed modes, not on reducing the device dimensions for increased packing density and higher speeds. These are some of the reasons why the random networks of CNTs based on soaking methods are mainly used in soft electronics these days, but there is no doubt that aligned CNT films will become needed in future applications that require higher carrier mobility such as in display applications.

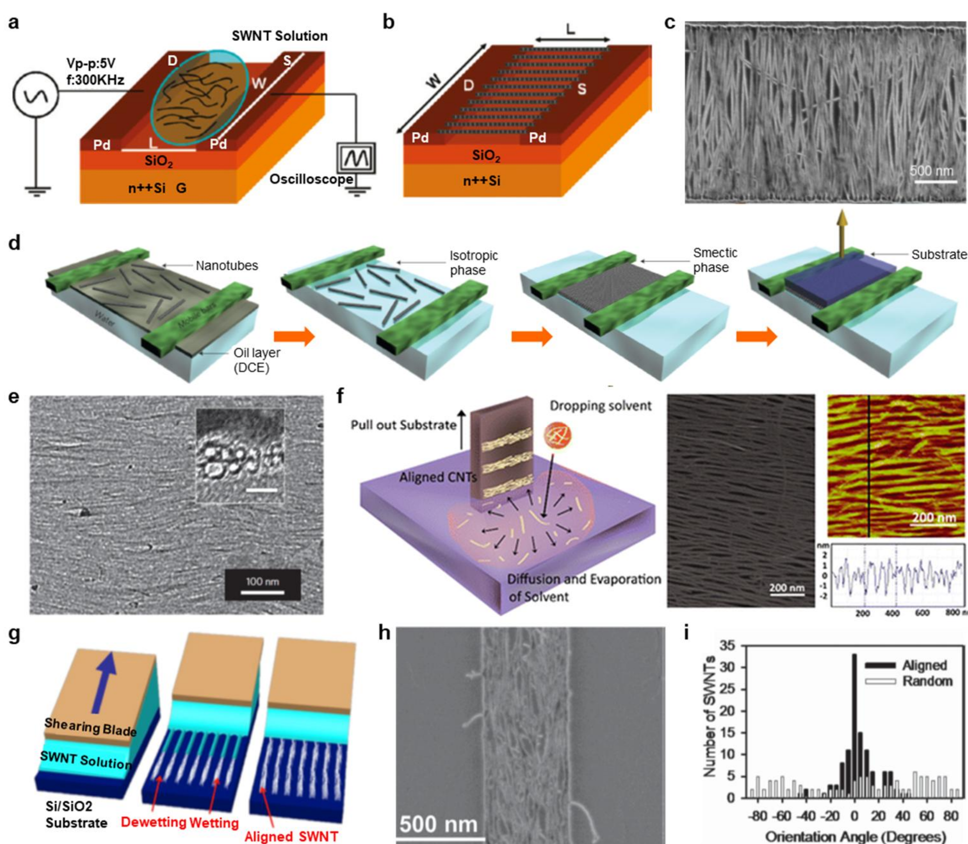


Figure 1.6. Methods for aligned semiconducting CNT deposition. Schematics of (a) dielectrophoresis and (b) CNTs aligned as a result of dielectrophoresis. (c) SEM image of a typical dielectrophoresis assembly. (d) Schematic of aligned CNT deposition using the Langmuir–Schaeffer method. (e) TEM images of aligned CNT arrays transferred onto solid substrates, where the inset shows a high-resolution cross-sectional view. (f) Schematic of evaporation-induced self-assembly for aligned CNTs and SEM/AFM images showing the morphology of the deposited CNTs. (g) Schematic of the shearing method of aligned CNT deposition. (h) SEM image of the aligned CNTs in the hydrophilic region. (i) Histogram of the orientation angles of the shear-aligned CNTs.

1.4 Conclusion

As described throughout this chapter, CNTs are one of the most appealing candidate materials which are expected to dominate the soft electronics market, which undoubtedly will continue to grow. The biggest challenges faced by CNTs for soft electronic applications lies in the cost effective and scalable methods for sorting CNTs by electronic types, and in the processing and designed deposition of CNTs onto the mechanically compliant substrates. Careful considerations must be given to developing novel materials and processing technologies that allow fabrication of high-performance soft electronics based on semiconducting CNTs, such as novel stretchable dielectrics that support intimate interfacing with the CNTs for high carrier mobility and stretchable electrodes that support superior conducting properties during high levels of deformation with excellent mechanical stability.

With the aim of developing stretchable electronic devices based on semiconducting networks of CNTs, I have focused on developing robust technologies for forming semiconducting CNT networks on desired substrates without material dependencies, novel deposition of stretchable dielectric with low thermal budget, and fabrication technology for soft CNT devices with performance metrics comparable to those of inorganic-based devices on rigid substrates. In particular, I first developed stretchable CNT electronics based on unit devices of non-volatile memory, which were then used to develop stretchable integrated circuits in conjunction with wearable organic light-emitting devices for mobile health-monitoring, and finally medium-level stretchable CNT circuits for performing sophisticated functionalities.

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Chapter 2. Stretchable Carbon Nanotube Charge-Trap Floating-Gate Memory and Logic Devices for Wearable Electronics

2.1 Introduction

Along with the increasing interests in wearable electronics, significant advancements have been achieved in technologies for flexible and stretchable devices, such as flexible displays,[1,2] skin-based electronics,[3-6] high-sensitivity deformable sensors,[7-11] wearable human-machine interfaces,[12-14] and compliant energy devices.[15-19] These unconventional electronic, optoelectronic, and energy devices are core components for next-generation wearable electronic systems. Although previous breakthroughs have dramatically advanced related technologies, current electronic devices still suffer from practical problems. One of the most significant concerns is the use of inorganic layers for the active channels and dielectric of conventional electronic devices which may incur mechanical cracks and/or breakdown in repetitive deformations and consequent accumulation of fatigues.[4] The mechanical mismatch between human tissues and inorganic semiconductors aggravates this problem, particularly in skin-based wearable devices.

Extensive research has been conducted to dissipate the induced strain in the channel and active regions, such as ultrathin thickness design approaches,[20] neutral

mechanical plane layouts,[21,22] and stretchable interconnections.[23-25] More fundamental changes have been proposed to replace channel materials with soft ones, including graphene[26-28] and CNT.[29-37] Graphene may have issues in terms of the on/off ratio owing to its zero band gap, which is critical for digital circuits. Networks of semiconducting single-walled CNT (s-SWNT) are a promising candidate owing to their potential for high speed/performance electronics by the intrinsically high carrier mobility,[38-43] although challenges in terms of device structures/designs, material optimization, and fabrication/integration strategies exist. Therefore, efforts to develop stretchable/wearable types of memory modules and other electronic device components for advanced electronic circuits/systems are important. Here, we present materials and device design/fabrication strategies for an array (17 × 15) of s-SWNT-based stretchable electronic devices consisting of capacitors, charge-trap floating-gate memory (CTFM) units, and logic gates (inverters and NAND/NOR gates). Detailed material, electrical, and mechanical characterizations and theoretical analysis in mechanics provide useful insights in the design and development of s-SWNT-based wearable electronic systems.

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2.2 Experimental section

2.2.1 Fabrication of s-SWNT-based wearable electronic devices

The detailed fabrication processes and materials used in the devices are described in **2.3 Results and discussion section**, supplemented by **Figs. 2.1**, **2.2**, and **2.3**. Before the devices are transferred onto a human skin, the entire system is picked up from an SiO_2 temporary supporting substrate using water-soluble tape (3M, USA) and transferred onto a thin layer of polydimethylsiloxane ((PDMS), Dow Corning, USA). The water-soluble tape is dissolved using deionized (DI) water to release the devices, which are subsequently transfer-printed on the skin.

2.2.2 Characterization of the device structures

The top-view images of the CTFMs, inverters, NAND/NOR gates, and capacitors are captured using an optical microscope (BX51 M, Olympus, USA). The density of the s-SWNT networks is examined using an atomic force microscope (Dimension Icon, Bruker, UK). The TEM images and the corresponding EDS data are taken using an electron microscope (JEM-2010, JEOL, Japan) operated at an acceleration voltage of 200 kV. For the cross-sectional analysis, the samples are cut using a focused ion beam (Quanta 3D FEG, FEI, USA) in the channel/trap region.

2.2.3 Characterization of the electrical properties

The *C*-*V* measurements are conducted at a 100-kHz frequency at ±10 V using a parameter analyzer (B1500A, Agilent, USA) equipped with an LCR meter

and a probe station (MSTECH, Republic of Korea). The *I*-*V* curves are obtained using the same setup. The stretching tests are conducted using an automatic stretching stage that applies compressive and tensile strains in the *x* and *y* directions.

2.2.4 Finite element analysis (FEA) of the CTFMs and inverters

Finite element simulations are used to analyze the strain distribution of the CTFMs and inverters during the stretching (Figures 8b and d) and bending tests (Figure S6b). The CTFMs and inverters are modeled using four-node composite shell elements. The devices/substrates are modeled using eight-node solid elements. We assume perfect bonding (no-slip condition) between the devices and substrates. To simulate stretching, stretching boundary conditions are applied at the bottom surface of the substrate. To simulate bending, rotation boundary conditions corresponding to the given radius of curvature are applied at the bottom of the substrate. The isotropic linear elasticity represents the behavior of the materials of the flash memory devices and inverters. The Young's moduli of the CNT, Au, Al_2O_3, SiO_2, and PI are 1 TPa, 77.2 GPa, 463 GPa, 73.1 GPa, and 2.5 GPa, respectively. The Poisson's ratios of CNT, Au, Al_2O_3, SiO_2, and polyimide (PI) are 0.22, 0.42, 0.22, 0.17, and 0.34, respectively. The incompressible neo-Hookean model is used to represent the substrate: $W = C_1(I_1 - 3)$ where W is the strain energy potential, I_1 is the first invariant of the left Cauchy-Green tensor, and C_1 (=3 kPa for the PDMS substrate) is a material parameter.

2.3 Result and discussion

2.3.1 Materials and device designs for the wearable CTFMs and logic gates

Figure 2.1 left depicts a schematic illustration of the wearable array of s-SWNT-based (99.9%-sorted s-SWNT, NanoIntegris Inc., USA) electronic devices composed of capacitors, CTFMs/transistors, and digital circuit components. The circuit diagrams (top) and layer information of the CTFM (bottom) are shown on the right. The ultrathin (< ~3 μm) and stretchable system design enables conformal integration of electronics onto the human skin. For mechanical robustness, the entire system is sandwiched between PI (Sigma Aldrich, USA; ~1 μm) ultrathin films. The detailed description of the fabrication processes and an exploded schematic illustration are shown in **Fig. 2.2**, and the corresponding large-scale view in **Fig. 2.3**. First, a PI layer (~1 μm) is spin-coated on a silicon oxide (SiO_2) wafer, followed by the deposition of Cr/Au (~5 nm/~50 nm) back-gate electrodes using thermal evaporation. All electrodes and charge-trap layers are formed using photolithography and lift-off techniques. After the deposition of a blocking oxide (B_{ox}) layer (~35-nm-thick aluminum oxide (Al_2O_3)) by plasma enhanced atomic layer deposition (PEALD), ~10 nm of gold (Au) is deposited for the charge-trap layer of flash memories. Two consecutive layers of tunneling oxides (Al_2O_3/SiO_2, ~5 nm/~3 nm) are deposited by PEALD (Al_2O_3) and e-beam evaporation (SiO_2). Even though the use of organic dielectric layers would have been advantageous in terms of mechanical flexibility than the chosen inorganic dielectrics, Al_2O_3 is used in this work due to its excellent thickness controllability and uniformity using PEALD, which in turn results

in high performance of the CTFM devices. The top surface of SiO_2 is functionalized to form an amine-terminated surface by immersing it into a poly-L-lysine solution (0.1 wt%, aqueous solution; Sigma Aldrich, USA) for 5 min. Then, random networks of SWNTs (whose average diameter and length are 0.8 ~ 1.2 nm and 100 ~ 1,000 nm, respectively) are deposited by dipping them into an s-SWNT solution (0.01 mg/mL, aqueous solution) for a few hours, followed by thorough rinsing using deionized (DI) water and isopropanol alcohol[1]. After annealing in a globe box at 200 °C for 1 h, isolation of the oxide layers and formation *via* connections follow. The fabrication of the other electronic devices uses similar procedures. But other devices, such as transistors in the logic circuits, do not contain the Au charge-trap layers and fabricated by using different patterns. The entire process is completed by depositing source/drain electrodes (Cr/Au, ~7 nm/70 nm), spin coating the top PI layer (~1 μm), and patterning the final serpentine/island layout by using photolithography and dry etching. Such design of island arrays connected with serpentine-shaped interconnects, with the assist of neutral mechanical plane designs, successfully protected the channel, dielectrics, and contacts during different bending and stretching modes.

Figure 2.4a represents high-resolution camera images of wearable s-SWNT electronic devices, consisting of CTFMs/transistors (10 × 15 array), inverters (1 × 15 array), NAND/NOR gates (2 × 15 array), and capacitors (4 × 15 array). The inset at the bottom left (black box) shows the conformal lamination on the skin during bending deformations. The inset at the top right (red-dashed box) confirms the conformal contacts of the array through magnified observation. The use of ultrathin

PI films with serpentine structures, along with the van der Waals forces, successfully dissipates the induced strains during motions, and maintains intimate contacts. The detailed mechanical and electrical characterizations of these devices under reversible deformations with induced strains (~20%) are discussed later. Further deformations that can possibly occur during daily life activities are shown in **Fig. 2.4b.** The devices show no delamination and/or mechanical fractures during poking, compression, and stretching (top, middle, and bottom of the figure, respectively).

Figure 2.5a shows an optical microscope image (top view) of the CTFM with the s-SWNT channel and Au thin-film trap layer. The red-dashed box highlights the active area. The atomic force microscopy (AFM) image shows the magnified view of the s-SWNT networks in the channel (**Figure 2.5b**). It has been reported that random networks of SWNTs are well percolated if the density of the connected SWNTs exceeds a certain threshold.[44] This percolation threshold can be approximately quantified by using the number density (per unit area; ρ), in which the average distance between SWNTs, $1/\rho^{1/2}$, equals to their average lengths, *i.e.*, $\rho_{th} \sim 1/\langle \text{SWNT length} \rangle^2$. The estimated unit density of the s-SWNT networks is approximately 30 ~ 40 tubes/μm^2: given the density, length, and device dimensions (channel lengths of 20, 30, and 40 μm), it can be concluded that the percolation of SWNTs is successfully formed to constitute an electrically conductive path between the source and drain electrodes.[45] Further improvements in the percolation of SWNT networks can be achieved by scaling down the channel length using industry facilities. To understand the structural compositions of the CTFMs, cross-sectional

transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDS) images are presented in **Figs. 2.5c** and **2.5d**, respectively. The magnified TEM image (**Fig. 2.5c**, right) shows the source/drain (Cr/Au) electrodes (~7 nm/70 nm), hybrid tunneling oxides composed of ~3 nm SiO_2 ($T_{ox}1$) and ~5 nm Al_2O_3 ($T_{ox}2$), ~10-nm Au thin-film trap, and ~35 nm B_{ox}, from top to bottom. The TEM images of the CTFM show no visible cracks or voids. The elements in each layer are confirmed by EDS data (**Fig. 2.5d**).

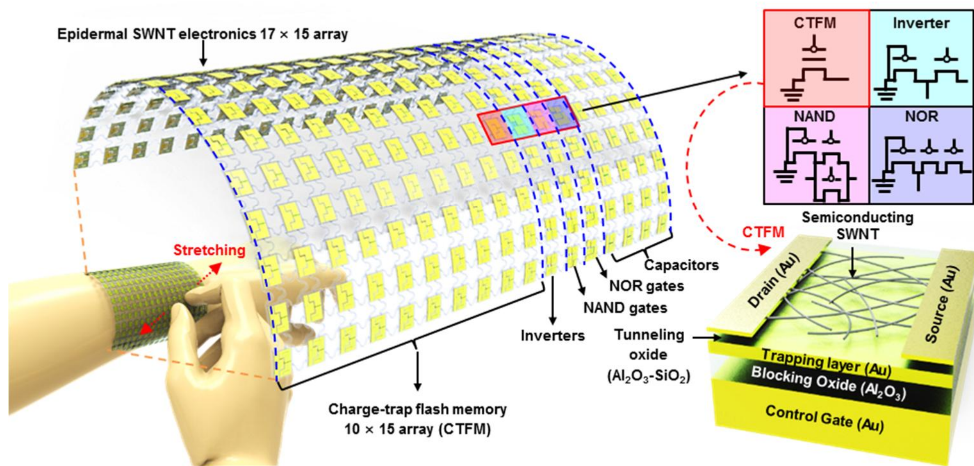

Figure 2.1. Schematic illustration of the s-SWNT-based electronic devices as a wearable array platform, which consists of memory units, capacitors, and logic circuits (left). Simple circuitry schematics (CTFM, inverter, and NAND/NOR gates) are shown in the top right colored sections. The bottom right frame shows the cross-sectional layer information of the CTFM.

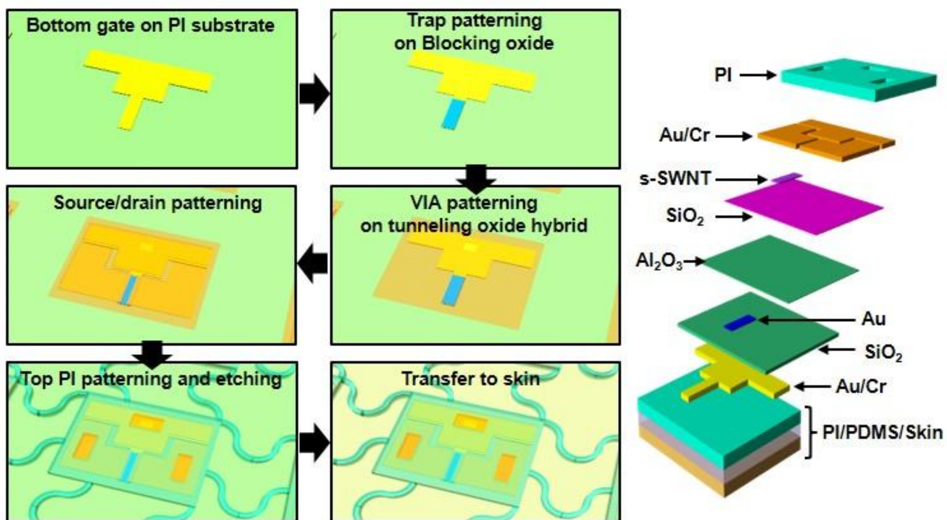

Figure 2.2. Schematic illustration of the fabrication process and exploded layer view of the wearable s-SWNT-based CTFM.

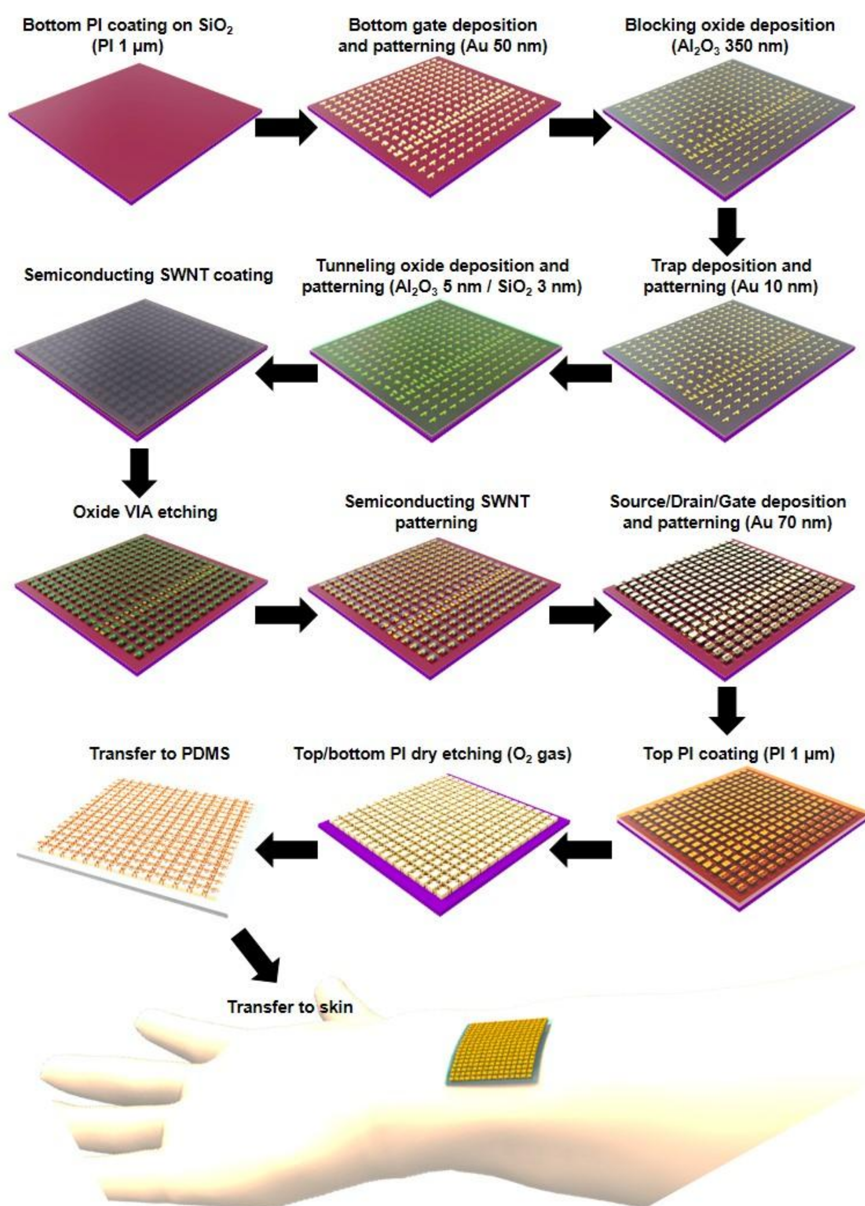

Figure 2.3. Schematic illustration of the overall fabrication process in a large-scale view.

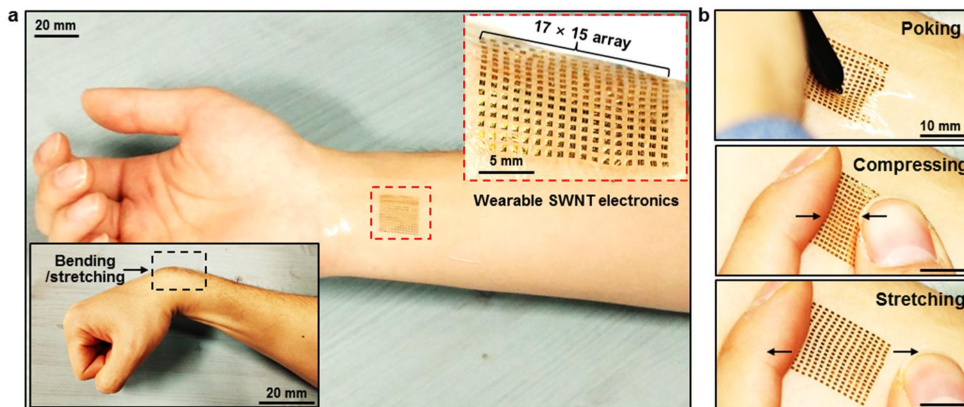

Figure 2.4. (a) Optical camera image of the array of s-SWNT electronic devices (17 × 15) composed of CTFMs, inverters, NAND/NOR gates, and capacitors. Conformal contacts are well made with a human skin. The insets show a magnified image (top right) and bending/stretching deformations (bottom left). (b) Deformed wearable s-SWNT devices under poking (top), compression (middle), and stretching (bottom).

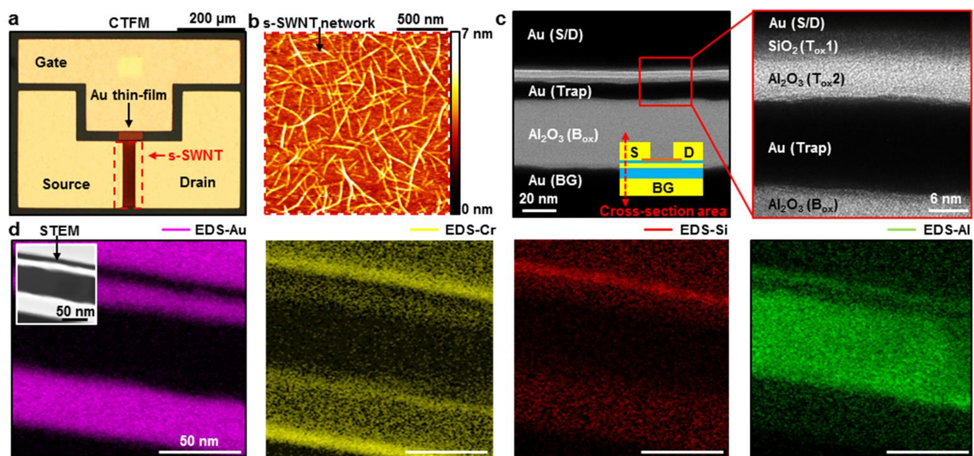

Figure 2.5. (a) Optical microscope image of a CTFM (top view). The red-dashed box indicates the active channel region composed of a random network of s-SWNTs. (b) AFM image of the 99.9%-sorted s-SWNTs layer showing high density of percolated s-SWNT networks. (c) (Left) Cross-sectional TEM image of the CTFM and (right) its magnified view. (d) EDS images showing the elements of each layer: Au, Cr, Si, and Al, from left to right, respectively.

2.3.2 Mechanism of the CTFM and capacitance measurements

Figure 2.6a shows two schematic illustrations describing the band bending of the CTFMs under applied positive/negative biases on the gate (program/erase (PGM/ERS) operation of CTFM; top/bottom, respectively). Electrons are trapped in the Au thin-film by tunneling (the band gap of SiO_2 ($T_{ox}1$) and Al_2O_3 ($T_{ox}2$) are ~9 eV and ~8.8 eV, respectively) through the ultrathin oxide hybrids (~3 nm/~5 nm for $T_{ox}1/T_{ox}2$) under a positive gate bias (PGM operation).[46-48] The ERS operation (negative gate bias) discharges electrons from the Au floating gate to the SWNTs by tunneling through the $T_{ox}1/T_{ox}2$ layers. This charge capturing and releasing behavior of the CTFM is closely related to its junction capacitance, characterized in detail using capacitors. **Figure 2.6b** plots the statistical normalized junction capacitance-voltage (*C*-*V*) characteristics (at 2 kHz) with a voltage sweep from -10 V to 10 V. A large hysteresis can be observed, which is a well-known phenomenon in SWNT-based devices that mainly results from the hydroxyl groups (–OH) at the interface between the gate dielectric and the SWNTs; the SWNTs in the channel region can be electrostatically modulated by carrier charging and discharging of –OH groups. The *C*-*V* curves with Au thin-film trap (red) exhibit larger hysteresis than that without the trap layer (blue), which proves that the Au thin film serves as a charge-trap layer of the non-volatile memory unit. The non-overlapped gate/source structures with different channel lengths/areas (**Fig. 2.6c**) are used to extract the gate capacitance per unit area (C_{ox}; **Fig. 2.6d**), while minimizing the parasitic capacitance. A C_{ox} value of

~7.60×10^{-8} F/cm^2 is extracted from the linear slope of the capacitance *versus* area plot (**Fig. 2.6e**).

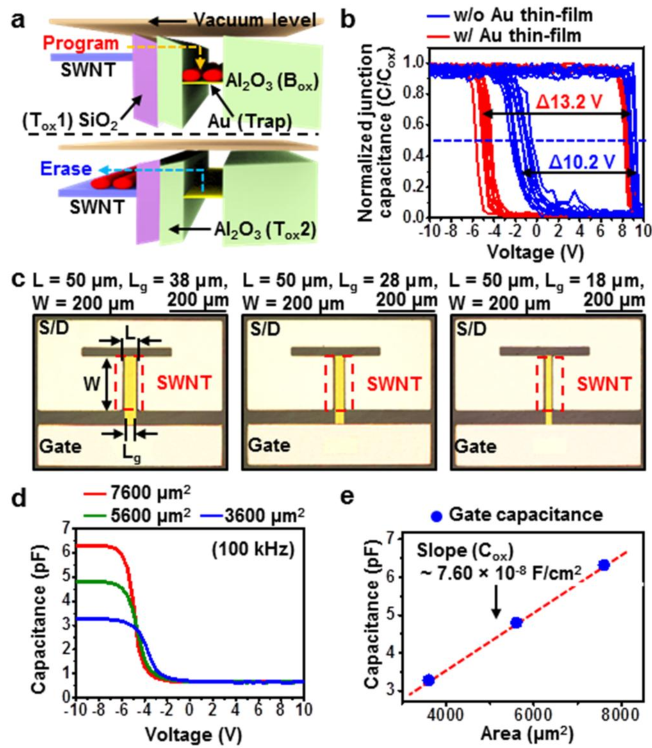

Figure 2.6. (a) Band bending of the CTFM in the electron charging/discharging process through the $T_{ox}1$ and $T_{ox}2$ layers in the PGM/ERS operations. (b) *C-V* characteristics showing different voltage hystereses (~13.2 V with trap layer (red) and ~10.2 V without trap layer (blue)) with a voltage sweep from -10 V to 10 V. (c) Optical microscope images of the non-overlapped gate/source structures with different gate lengths (L_g) of 38, 28, and 18 μm. (d) Plot of the gate capacitance per unit area. (e) Plot of the capacitance *versus* area with a linear slope (C_{ox}) of ~7.60 × 10^{-8} F/cm^2.

2.3.3 Electrical characterization of transistors that compose the CTFM

The electrical performance of the transistors that compose the CTFMs is characterized under ambient conditions. **Figure 2.7a** illustrates the transfer curves (I_d-V_g; drain current-gate voltage) of the transistors in the CTFMs with different channel lengths (L = 20 μm, 30 μm, and 40 μm) at the applied drain voltage (V_d) of -5 V. A typical transfer curve of a field-effect transistor (FET, without a charge-trap layer) with L = 20 μm is shown in **Fig. 2.8**, for comparative analysis. Owing to the better control of s-SWNTs in the channel area by the gate, the FET exhibits a higher performance in terms of on/off currents. The I_d-V_d and I_d-V_g characteristics of the transistors at L = 30 μm under different V_g are shown in **Figs. 2.9a** and **2.9b**, respectively. The 150 transistors (10 × 15 array) whose channel lengths (L) range from 20 to 40 μm effectively function without significant variations in the on/off ratio and on-current density. **Figure 2.7b** shows the cumulated I_d-V_g curves of the 50 transistors in the CTFMs at L = 30 μm, exhibiting high device-to-device uniformity. We can further validate these through statistical analysis of the on-current density per unit width (I_{on}/W; **Fig. 2.7c**), on/off ratio (I_{on}/I_{off}; **Fig. 2.7d**), transconductance per unit width (g_m/W; **Fig. 2.7e**), and carrier mobility at V_d = -5 V (μ; **Fig. 2.7f**). In summary, the averages of I_{on}/W, I_{on}/I_{off}, g_m/W, and μ are 0.36 ± 0.16 μA/μm, > 10^5, 0.057 ± 0.021 μS/μm, and 4.51 ± 1.67 cm^2/Vs, respectively. For the estimation of μ, the equation for the parallel-plate model[20] is used, namely, $\mu = Lg_m/(V_d C_{ox} W)$, where $C_{ox} = 7.60 \times 10^{-8}$ F/cm^2 (from **Fig. 2.7e**).

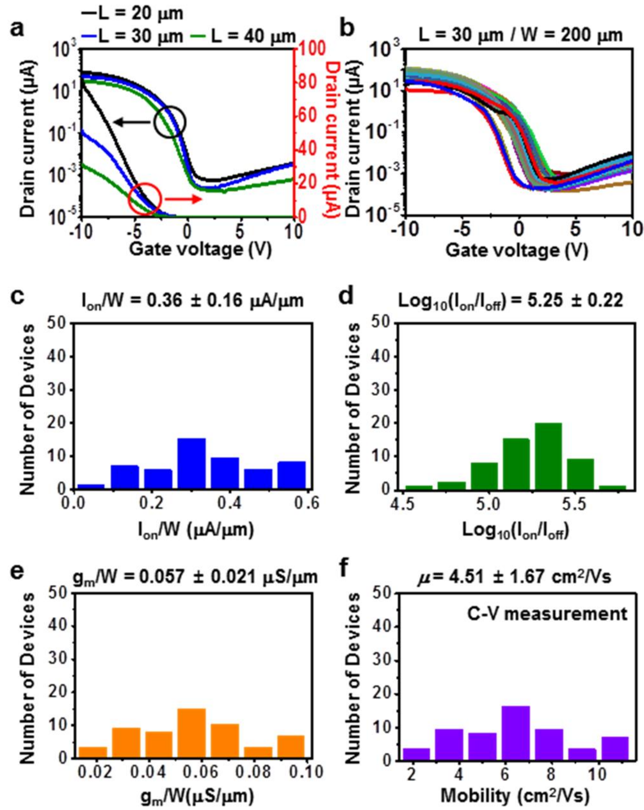

Figure 2.7. (a) I_d-V_g curves of the transistors that compose the CTFMs with different channel lengths (L = 20, 30, and 40 □m). (b) Cumulative I_d-V_g characteristics of 50 transistors with L = 30 μm. (c) On-current density per unit width at V_d = -5 V. (d) On/off ratio at V_d = -5 V. (e) Transconductance per unit width at V_d = -5 V. (f) Mobility at V_d = -5 V.

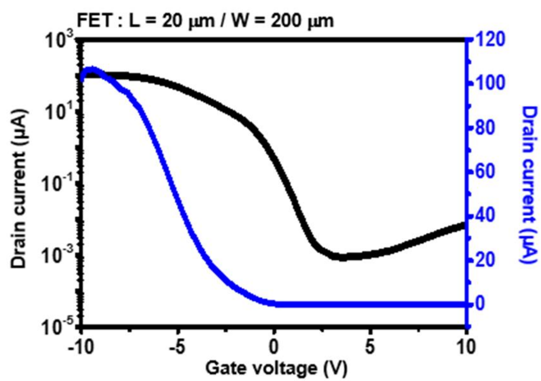

Figure 2.8. Typical I_d-V_g curve of an s-SWNT field-effect transistor with L = 20 μm and W = 200 μm.

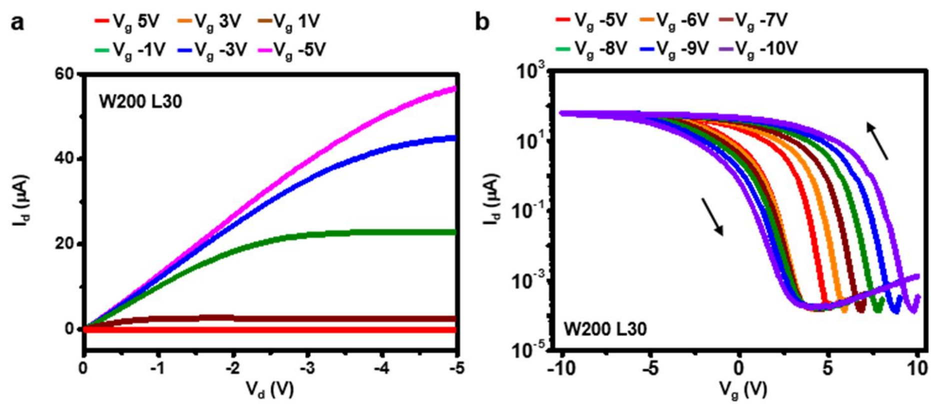

Figure 2.9. (a) I_d-V_d characteristics and (b) I_d-V_g characteristics of CTFM under different V_g (L = 30 μm).

2.3.4 Memory characteristics of the CTFM

The typical memory switching characteristics of the CTFMs as a function of the pulse time at different gate voltages ranging from ±15 V to ±25 V are plotted in **Figs. 2.10a** and **2.10b**. The drain current is the current measured at a read voltage of 0 V. For both PGM/ERS operations, increase/decrease in the drain current can be observed even for a short pulse period of 10^{-6}. This result indicates the effective charging/discharging of the carriers into/from the trap layer. Larger change in the drain current can be observed by increasing the duration of the pulse time for both PGM/ERS operations. The CTFM at L = 30 µm is characterized in two read-out PGM and ERS operations at the gate voltage/pulse time of +25 V/1 s and -25 V/1 s, respectively (**Fig. 2.10c**). The window margin that corresponds to the difference in the drain current at V_g = 0 and the device-to-device uniformity of the 50 CTFMs are appropriate for unambiguous read-out (**Fig. 2.10d**). **Figure 2.10e** shows the endurance characteristics of the CTFMs under the operating condition of ±25 V/100 µs. The CTFMs maintain substantial window margins even after PGM/ERS operations of 10,000 cycles. The retention test (**Fig. 2.10f**) also verifies the reasonable window margin maintained after approximately 10,000 s.

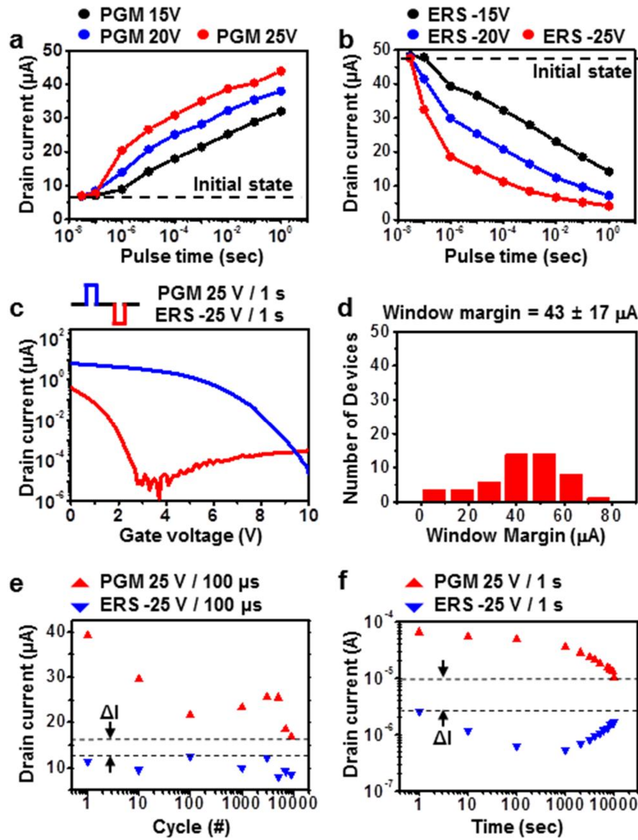

Figure 2.10. (a) Memory switching characteristics as a function of the pulse time with applied gate voltages of 15 V, 20 V, and 25 V for the PGM operation. (b) Memory switching characteristics for the ERS operation with inverse gate voltages of -15 V, -20 V, and -25 V. (c) Plot of the two read-out operations. PGM and ERS at +25 V/1 s and -25 V/1 s, respectively. (d) Statistics of the window margins of the 50 CTFMs after PGM/ERS operations at ±25 V/1 s. (e) Endurance characteristics of the CTFMs during 10,000 PGM/ERS cycles with ±25 V/100 μs. (f) Retention characteristics of the CTFMs under PGM/ERS at ±25 V/1 s.

2.3.5 Electrical characterization of the logic gates

In addition to the capacitors, transistors, and CTFMs, logic gates are important components in digital circuits. The voltage transfer curves (VTCs) and output characteristics of the logic gates (inverters and NAND/NOR gates) are shown in **Fig. 2.11**. An optical microscope image of an inverter and its VTCs (V_{DD} ranging from -5 V to -10 V) are shown in **Figs. 2.11a** and **2.11b**, respectively. The VTCs show typical input/output behavior of the logic inverter, *i.e.*, V_{OUT} decreases from 0 to V_{DD} as V_{IN} increases from V_{DD} to 0. The voltage gains at each V_{DD} are shown in **Fig. 2.11c** and their summary is shown in **Fig. 2.11d** (top). An important factor in the characterization of inverter performance is the noise margins *i.e.*, the high- and low-state noise margins (NM_H and NM_L). NM_H and NM_L are estimated as $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$, where V_{OH}, V_{OL}, V_{IH}, and V_{IL} denote the output high voltage, output low voltage, input high voltage, and input low voltage, respectively. The measured noise margins with respect to different V_{DD} are plotted at the bottom of **Fig. 2.11d**. The detailed values are listed in **Table 2.1**. The average noise margin for the applied V_{DD} is $0.190 \times V_{DD}$, which shows the reliable and robust operation of the inverters. The inverter is successfully extended for more advanced logic gates (two-input NAND and NOR; **Figs. 2.11e** and **2.11g**), as shown in their output characteristics (**Figs. 2.11f** and **2.11h**). V_{DD} of -5 V is used along with input voltages of -5 V and 0 V for logic “1” and “0”, respectively.

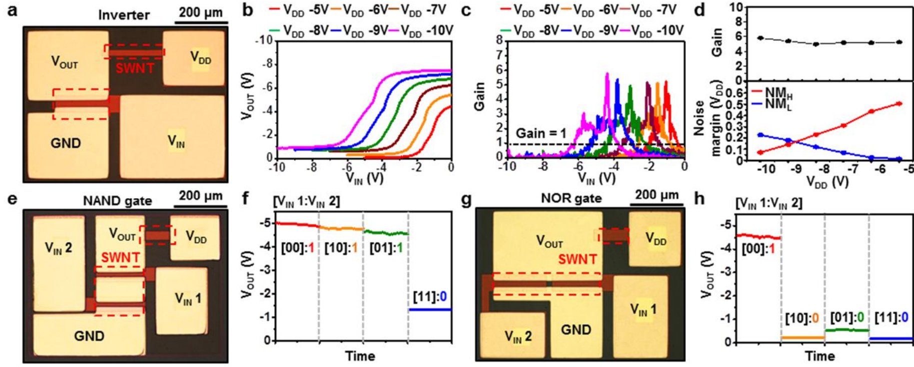

Figure 2.11. (a) Optical microscope image of an inverter. The red-dashed box indicates the random network of s-SWNTs in the active channel region. (b) VTCs showing the input and output behavior of the inverter. V_{DD} varies from -5 V to -10 V. (c) Voltage gain of the inverter. (d) (Top) Summary of voltage gains and (bottom) noise margins with respect to different V_{DD} ranging from -5 V to -10 V. (e) Optical microscope image of a two-input NAND logic gate. (f) Output characteristics of a two-input NAND logic gate with V_{DD} of -5 V and input voltages of -5 V and 0 V. (g) Optical microscope image of a two-input NOR logic gate. (h) Output characteristics of a two-input NOR logic gate with V_{DD} of -5 V and input voltages of -5 V and 0 V.

V_{DD} (V)	V_{IL} (V)	V_{IH} (V)	V_{OL} (V)	V_{OH} (V)	NM_L	NM_H
-5	-0.49	-2.05	-0.42	-4.58	$0.014V_{DD}$	$0.506V_{DD}$
-6	-0.86	-2.6	-0.71	-5.22	$0.025V_{DD}$	$0.437V_{DD}$
-7	-1.52	-3.48	-1.04	-5.66	$0.069V_{DD}$	$0.311V_{DD}$
-8	-2.22	-4.3	-1.26	-6.14	$0.120V_{DD}$	$0.230V_{DD}$
-9	-3.03	-5.2	-1.42	-6.47	$0.179V_{DD}$	$0.141V_{DD}$
-10	-3.75	-6.2	-1.49	-6.91	$0.226V_{DD}$	$0.071V_{DD}$

Table 2.1. High- and low-state noise margins of the inverter at different V_{DD}

2.3.6 Characterization of mechanical stability of the wearable CTFM

In wearable electronics, a stable electrical operation of devices under external applied strains is important. The electrical performance results of s-SWNT CTFMs and inverters with different uniaxial strains (up to ~20%; typical maximum strain induced in a human skin[5]) are characterized and compared with theoretical analyses, as shown in **Fig. 2.12**. The island-shape active and serpentine-shape interconnection designs, together with the neutral mechanical plane layout[16], enable the devices to endure an ~20% applied strain while minimizing the deformations/strains in the channels and active regions (**Figs. 2.12a** and **2.12c**; see strain distributions obtained by FEA under each applied strain in **Figs. 2.12b** and **2.12d**). It can also be inferred that the disconnection issues of SWNT network percolations and/or extraction of SWNTs from the metal source/drain contacts is effectively avoided by unwanted movements of the SWNTs due to the applied strain. The maximum induced strain in the active (~0.001) and interconnection (~0.036) regions is below the typical fracture strain of the device components. The corresponding electrical characterizations of the CTFMs and inverters during the stretching tests are shown in **Figs. 2.12e** and **2.12f**, respectively. The PGM and ERS curves of the CTFM (PGM and ERS at +25 V/1 s and -25 V/1 s) and VTCs of the inverter under external strains show no visible variations and/or signs of electrical degradations. Even after stretching for 1,000 times with ~20% applied strain, the device performance shows minimal changes (**Fig. 2.13**). In addition, the bending test of the inverter is conducted at different radii of curvature between infinite (flat) and

~5-mm bending radii (**Fig. 2.14a**). The induced strains on the inverter (FEA; **Fig. 2.14b**) are negligible. The stable electrical characterization results confirm the effectiveness of the material and design strategies (**Fig. 2.14c**).

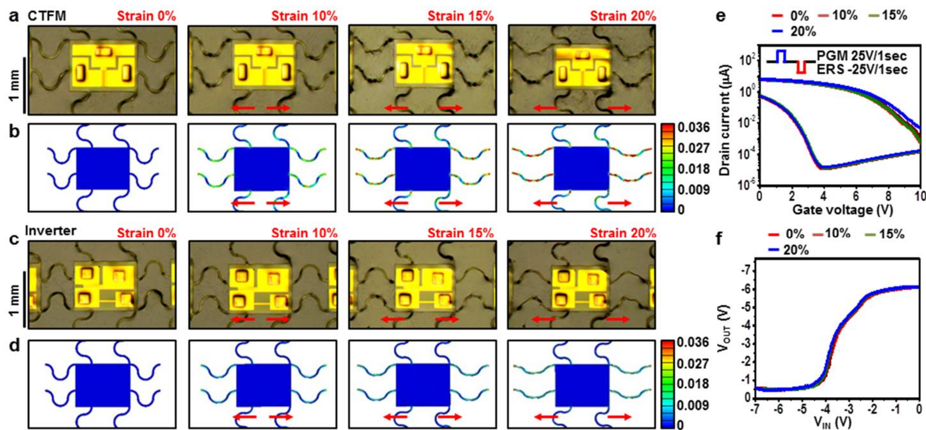

Figure 2.12. (a) Optical microscope image and (b) FEA strain distribution results of the CTFM under applied strains between 0% and 20%. The red arrows indicate the strain direction. (c) Optical microscope image and (d) FEA strain distribution results of the inverter under applied strains between 0% and 20%. (e) Electrical characteristics of the CTFM under applied strains between 0% and 20% (PGM and ERS at -25 V/1 s and +25 V/1 s, respectively). (f) VTCs of the inverter showing stable operation under applied strains between 0% and 20%.

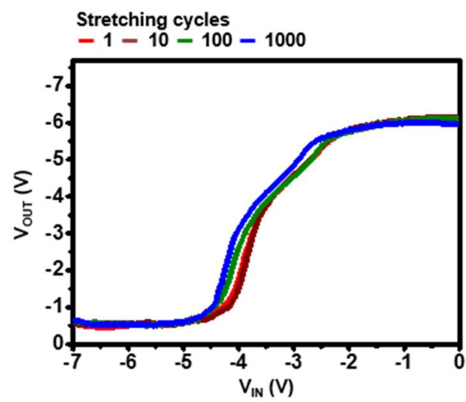

Figure 2.13. VTCs of the inverter after cycled stretching tests. The number of stretching cycles and applied strain are 1, 10, 100, and 1000 times and 20%, respectively.

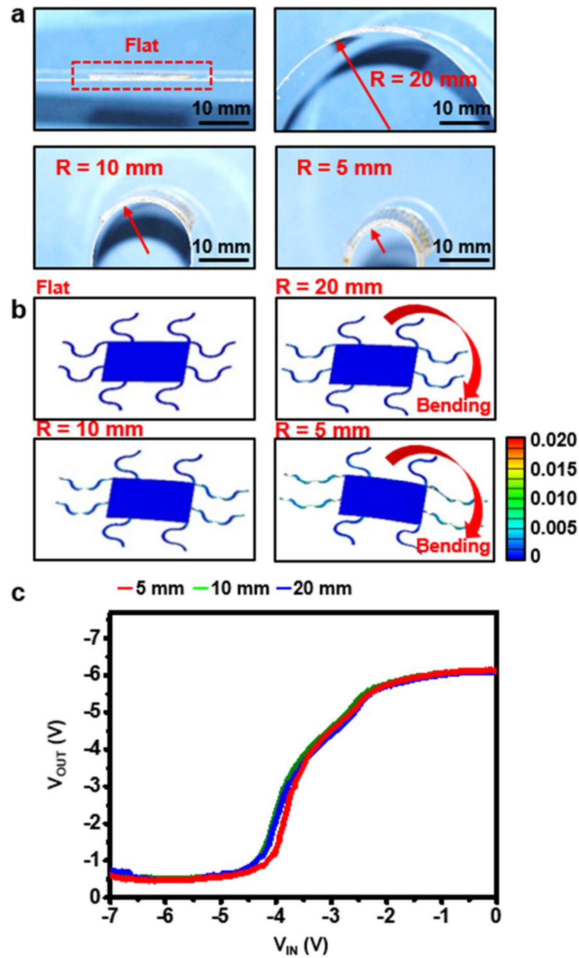

Figure 2.14. (a) Optical camera images and (b) corresponding induced strain distributions by FEA of the inverter in bending tests. The radius of curvature ranges from infinite (flat) to ~5 mm. (c) VTCs of the inverter that show stable electrical operation at different radii of curvature (5, 10, and 20 mm).

2.4 Conclusion

In summary, we have reported stretchable s-SWNT-based electronic devices, such as capacitors, transistors, nonvolatile memory units, and logic gates. The arrayed stretchable devices are conformally laminated on a curvilinear and soft human skin. Deformations including poking, compression, and stretching do not cause delamination or mechanical fractures. The detailed material analyses using electron and elemental microscopies as well as the theoretical explanations based on numerical mechanic modeling/simulations validate the electrical characterizations, *i.e.*, the reliable device operations. The performance of the memory and logic devices is well maintained even after repetitive stretching/fatigue tests. These soft electronic devices based on s-SWNTs can provide novel opportunities for wearable electronics.

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Chapter 3. Wearable Electrocardiogram Monitor Using Carbon Nanotube Electronics and Color-Tunable Organic Light-Emitting Diodes

3.1 Introduction

The recent advances in flexible and stretchable electronics have triggered significant technological progresses in wearable electronics and/or optoelectronics.[1-5] Noninvasive health-monitoring and therapy devices have particularly benefitted from such technological evolution. Some examples include wearable biomedical electronic patches,[6,7] soft optogenetic devices,[8,9] thermal therapy devices,[10,11] and electronic skins.[12-14] These achievements were mainly accompanied by aggressive researches on inorganics-based ultrathin devices,[15-17] and they are expected to create huge synergies with the recent innovations in wearable electronics.[18-20] However, the use of inorganic materials in wearable electronics poses several challenges in terms of sensing reliability and device stability, as their intrinsically brittle nature can result in mechanical breakdown after repetitive deformations occurring from the daily actions of human body. Although the nanoscale assembly and integration of inorganic

materials provides potential solutions,[21-23] intrinsically soft materials are attracting attention owing to their mechanical stability.[24,25]

Organic materials have thus been considered strong candidates for wearable electronics/optoelectronics.[26-30] To utilize the well-established materials, facilities, and know-hows in the organic industry is another important advantage. For wearable electronic applications, networks of single-walled carbon nanotubes (CNTs) are promising semiconducting materials due to their excellent electrical properties, good uniformity, and robust performance under intense mechanical stresses/strains.[31-34] In particular, remarkable advances have been made in the field of high-performance CNT electronics based on solution-processed semiconducting CNTs, showing outstanding device-to-device uniformity in the medium scale, high on/off ratios and carrier conductance, and scalability down to a few micrometers.[35-37]

Herein, we report a wearable electrocardiogram (ECG) monitor based on an ultrathin electrode and a *p*-MOS CNT signal amplifier. The integration of sensors and amplifiers enables continuous detection of the ECG signals, which are associated with diagnosis of clinical cardiac conditions such as arrhythmia and ischemia.[38,39] In addition, the developed devices can be conformally attached to the skin, providing high reliability against severe mechanical deformations on skin, as proven through the cyclic mechanical deformation tests. We integrated our wearable electronics with an ultrathin voltage-dependent color-tunable organic light-emitting diode (CTOLED) for the colorimetric display of the retrieved ECG signals. An interlayer approach has been developed for color tuning the OLEDs, which involves the use of an ultrathin

exciton-blocking layer (EBL) between two emitting layers (EMLs) for blue and red colors. By optimizing the material and thickness of the EBL, the wearable OLEDs exhibit ECG-dependent color changes from dark red, to pale red, to white, to sky blue, and finally to deep blue. The ultrathin design enables the CTOLEDs to conform to the curvilinear and dynamic surface of human skin and to exhibit excellent stability and reliability after repeated deformations.

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3.2 Experimental section

3.2.1 Fabrication of *p*-MOS CNT inverters

A polyimide (PI) layer (~1 μm) was spin-coated on a silicon oxide (SiO_2) wafer, followed by the formation of back-gate electrodes (Cr/Au, 7/70 nm) using thermal evaporation and photolithography. Two consecutive layers of ~30-nm-thick aluminum oxide and ~3-nm-thick SiO_2 were deposited on top by plasma-enhanced atomic layer deposition and e-beam evaporation, respectively. Then, the top surface of SiO_2 was functionalized using poly-L-lysine (0.1 wt %, aqueous solution; Sigma-Aldrich) to form an amine-terminated surface, followed by consecutive immersions in semiconducting CNT solution (0.01 mg/ML, aqueous solution) for a few hours to form dense networks of CNT on the top surface. After rinsing with deionized water and isopropyl alcohol, the sample was annealed inside a glove box at 200 °C for 1 h to remove the unwanted surfactants and carboxyl groups on the surface of the CNTs. Via connections were then formed, followed by the formation of source and drain electrodes (Cr/Au, 7/70 nm) through thermal evaporation and photolithography. The process was completed by spin-coating a top PI layer for passivation and mechanical stability.

3.2.2 Fabrication of CTOLEDs

NPB, CBP, FIrpic, TBPI, $pq_2Ir(acac)$, and DPEPO were purchased from commercial sources and used without purification. The CTOLEDs were fabricated through high-vacuum (2×10^{-6} Torr) thermal evaporation of the organic materials

onto ITO-coated glass (sheet resistance: 15 Ω/square; Applied Film Corp.). The evaporation rates, monitored by a quartz crystal thickness monitor, were 1 Å/s for the organic materials and 3～4 Å/s for the metals. Glass substrates with patterned ITO electrodes were washed in isopropyl alcohol and then cleaned through O_2 plasma treatment. CTOLEDs were fabricated with a configuration of ITO/NPB (70 nm)/CBP:10% FIrpic (70 nm)/EBL (0, 1, 5, and 10 nm for various materials)/$pq_2Ir(acac)$ (1 nm)/TPBI (20 nm) /LiF (1 nm)/Al (100 nm). NPB, CBP, FIrpic, different materials of EBL, $pq_2Ir(acac)$, TPBI, LiF, and Al electrodes were deposited on the substrate in a sequential order. DPEPO was used as an EBL. CBP and TPBI were also used as EBL materials for the color-tunable device.

3.2.3 Fabrication of wearable CTOLEDs

A Parylene-C layer (500 nm) was evaporation-deposited on a Teflon-AF coated glass, followed by spin-coating of epoxy (600 nm, SU-8 2000.5, MicroChem) at 3000 rpm. for 30 s. After fully curing the photoresist, Au (70 nm) was thermally evaporated and ITO was sputtered (50 W, 30 min, 5 mTorr, 200 °C), both using a shadow mask. The deposition of NPB, CBP, FIrpic, DPEPO, $pq_2Ir(acac)$, TPBI, LiF, and Al followed the same procedures/thickness described above. Parylene-C was once again deposited, and Au electrodes were exposed by reactive ion etching (150 W, 100 sccm O_2, 3 min) using a shadow mask. After connecting flexible cables for external wiring, the CTOLEDs were picked up using a commercial transparent water-proof tape (Tegaderm Film, 3M), resulting in a wearable CTOLED device.

3.2.4 Characterizations

The emission properties and external quantum efficiency were determined using a PR-650 SpectraScan SpectraColorimeter as a source meter. The current-density-voltage characteristics and electrical performances of the CNT transistors were measured using a programmable electrometer equipped with current and voltage sources (Keithley 2400). The TEM images and high-resolution TEM images were obtained using a JEOL 2100F electron microscope operated at 200 kV.

3.3 Results and discussion

3.3.1 Skin-mounted electrophysiology devices and signal amplifiers for real-time ECG monitoring

Significant efforts have been devoted toward developing more comfortable and softer wearable platforms for monitoring and displaying heart activities, to help in the diagnosis and treatment of cardiac diseases.[40,41] In this regard, we developed skin-mounted electrophysiology devices and signal amplifiers for real-time ECG monitoring. **Figure 3.1a** depicts a schematic illustration of our wearable cardiac-monitoring platform composed of an ultrathin ECG sensing electrode, a *p*-MOS CNT signal amplifier (hereinafter referred as *p*-MOS inverters or amplifiers), and a voltage-dependent CTOLED. For sensing ECG signals, a wearable electrode based on a serpentine-shaped thin Au film (**Fig. 3.1b**) is used. The retrieved signals are amplified by a *p*-MOS inverter, which comprises four transistors that employ dense networks of CNTs as their channel material (**Fig. 3.1c**). After signal processing using a data acquisition unit (DAQ)/PC (not shown in the schematics), a voltage-dependent CTOLED displays the signals in real-time through color changes (**Fig. 3.1d**). The ultrathin (< approximately 3 μm) form factor of the system enables conformal integration on human skin. The detailed description of the fabrication processes for each unit is included in the *Methods* section.

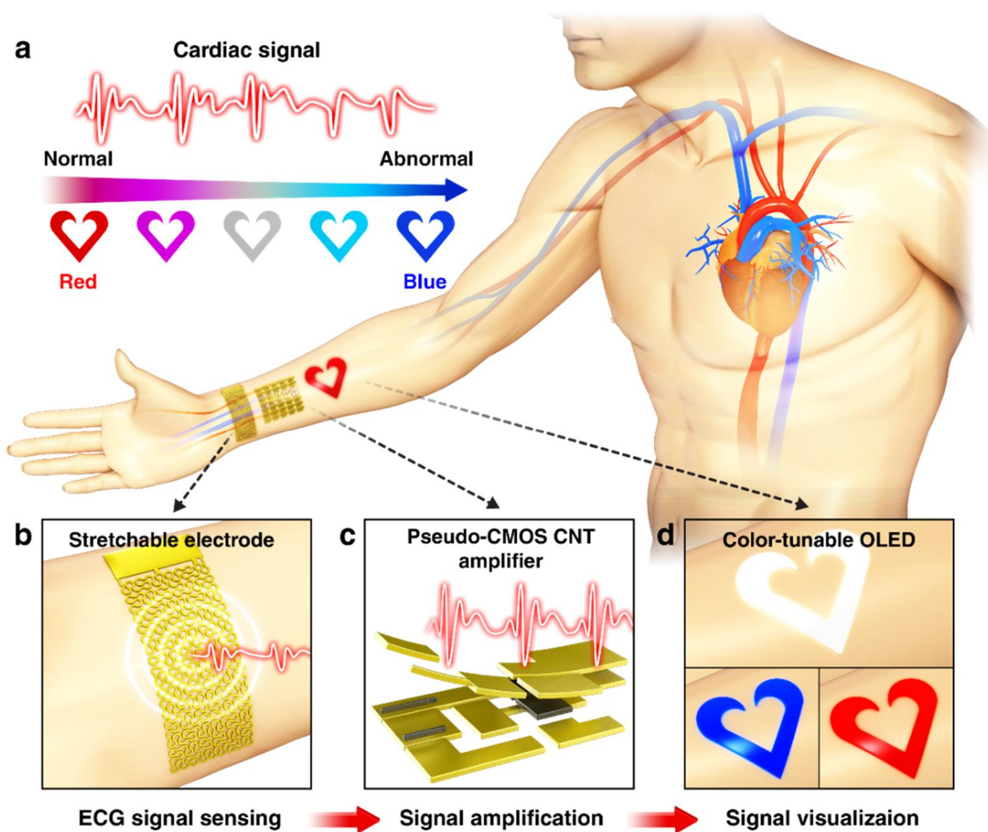

Figure 3.1. (a) Schematic illustration of the real-time wearable cardiac-monitoring system. The ECG signals are measured by (b) a stretchable Au electrode, and then amplified by (c) a *p*-MOS CNT inverter for the high signal-to-noise ratio. The retrieved ECG signals are displayed *via* synchronized color changes of (d) the wearable CTOLED.

3.3.2 Signal amplifiers based on *p*-MOS CNT inverters and their characterization

The wearable signal amplifiers are built using *p*-MOS inverters based on four *p*-type CNT transistors; the actual device image and circuit design are shown in **Fig. 3.2a** top and bottom, respectively. The networked CNT channel is prepared from a solution of semiconducting CNTs (>99% purity; NanoIntegris Inc., USA), using the same method used in our previous report but with longer deposition time.[32] The atomic force microscopy (AFM) image in **Fig. 3.2b** shows well-percolated networks of CNTs with high surface coverage, wherein the estimated unit density of a CNT network is approximately 50~60 tubes/μm^2. Given the physical dimensions of the channel (10 and 100 μm in length, 300 μm in width) and the densities of the CNTs, an electrically conductive path can be firmly established between the source and drain. **Figures 3.2c** and **3.2d** show the typical transfer and output curves, respectively, of the CNT transistors that constitute the *p*-MOS amplifier, at an applied drain voltage of −5 V. The accumulated characteristic curves in **Fig. 3.2e** are measured from 10 separate samples, and show uniform electrical performances with average on/off ratios higher than 10^4 for both the 10 μm and 300 μm channel-length devices (**Fig. 3.2f**).

Figure 3.2g plots the output voltages (V_{OUT}) of the amplifier with respect to the input voltages (V_{IN}) under various bias conditions (V_{SS}, V_{DD}). The gain of the amplifier increases with V_{SS}, and the maximum gain (V_M) is approximately 80 at a V_{IN} of approximately −4.6 V and V_{SS} of −10 V (Fig. 2h). Further characteristics of the

p-MOS inverter, including noise margins, are also calculated and presented in **Figs. 3.2i** and **3.2j**. The high- and low-state noise margins (NM_H and NM_L, respectively) with respect to different V_{SS} were calculated as $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$, respectively, where V_{OH}, V_{IH}, V_{IL}, and V_{OL} denote the output high voltage, input high voltage, input low voltage, and output low voltage, respectively. The results demonstrate the reliable and robust operation of the ultrathin and soft *p*-MOS inverter.

The ECG signals are measured from human wrists by using wearable ECG sensors, with and without integration of the CNT amplifier for comparison (**Figs. 3.2k** and **3.2l**). Specifically, ECG sensors are worn on both wrists, and the potential differences between the two electrodes (ECG signals) are measured. The as-measured signals are amplified using the *p*-MOS inverter, and then, the noise is eliminated using high/low-pass filters (0.079/19.4 Hz). The ECG signals are measured from a healthy male subject (32 years old), first using a pure ECG sensor alone, and then using our *p*-MOS inverter as the signal amplifier.[41] It can be estimated that the ECG signals are amplified by the *p*-MOS inverter with an effective gain of 60 or higher. It is observed that distinguishable ECG signals can be measured when the amplifier is used (**Fig. 3.2l**), whereas a noise-like signal is acquired when the amplifier is not used (**Fig. 3.2k**).

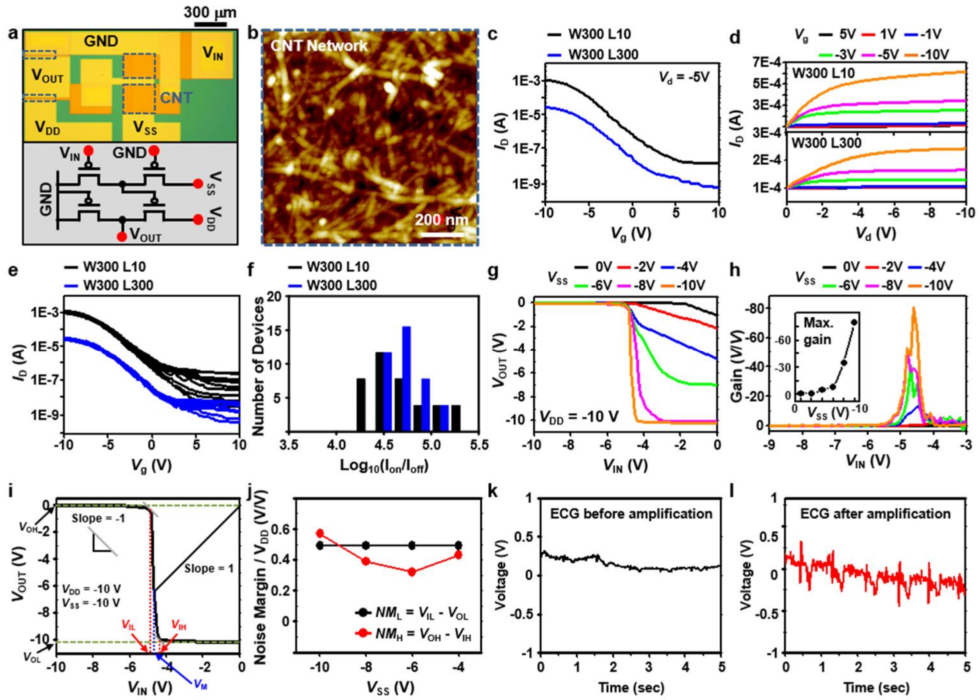

Figure 3.2. (a) Optical microscopic image of the *p*-MOS inverter (top) and corresponding schematic circuit diagram (bottom). (b) AFM image of the CNT channel showing a dense network of well-percolated CNTs. (c) Transfer curves of the CNT transistors with two different channel dimensions, at the applied drain voltage of -5 V. (d) Output curves of the CNT transistors with two different channel dimensions, at various gate voltages. (e) Accumulated transfer characteristics of CNT transistors measured from 10 different *p*-MOS inverters (40 curves) (f) On-off ratio at V_d = -5 V. (g) Voltage transfer characteristics of the *p*-MOS inverter with various biasing conditions (V_{DD} fixed to -10 V). (h) Signal gain of the inverter with respect to V_{IN} under various biasing conditions (V_{DD} fixed to -10 V). (i) Characteristic curve of the *p*-MOS inverter. Several parameters (V_{OH}, V_{OL}, V_{IL}, V_{IH}, V_M) are indicated on the

plot. (j) Noise margins of the *p*-MOS inverter as a function of V_{SS}. (k, l) ECG signals measured from the human wrist (k) before amplification and (l) after amplification using the *p*-MOS inverter.

3.3.3 Fabrication and characterization of CTOLEDs employing different emission layers and a charge blocking layer for color control

The measured ECG signals can be displayed in a colorimetric manner, by using wearable CTOLEDs. The CTOLEDs are fabricated using an EBL (DPEPO) sandwiched between two emitting materials–a blue phosphorescent layer of bis[2-(4,6-difluorophenyl)pyridinato-C^2,*N*](picolinato) iridium(III) (FIrpic) doped in a 4,4′-bis(*N*-carbazolyl)-1,1′-biphenyl (CBP) layer and an undoped red phosphorescent layer of bis(2-phenylquinolyl-N,C(2′))iridium (acetylacetonate) ($pq_2Ir(acac)$). **Figure 3.3a** schematically illustrates the device structure of the CTOLED (total thickness of ~366 nm), which consists of ITO (100 nm), *N*,*N*′-di(1-naphthyl)-*N*,*N*′-diphenyl-(1,1′-biphenyl)-4,4′-diamine (NPB, 70 nm), CBP:10% FIrpic (70 nm), bis[2-(diphenylphosphino)phenyl] ether oxide (DPEPO, 5 nm); $pq_2Ir(acac)$ (1 nm), 2,2′,2"-(1,3,5-benzinetriyl)-tris(1-phenyl-1-*H*-benzimidazole) (TPBI, 20 nm), and LiF/Al (1 nm/100 nm). NPB is used as a hole-transporting layer (HTL), TPBI as an electron-transporting layer (ETL), LiF as an electron-injection layer, and Al as a cathode. The DPEPO between the EMLs acts as a selective charge- and exciton-blocking layer, which determines the color tunability (**Figs. 3.3b** and **3.3c**). The thickness of the red EML is elaborately controlled to be substantially lesser than that of the blue EML, allowing a sharp color contrast in the higher-voltage regime. **Figure 3.3d** shows the cross-sectional transmission electron microscopy (TEM) image of the CTOLED, confirming the stacked structures. The magnified TEM image (**Fig. 3.3e**) that corresponds to the red box in **Fig. 3.3d** provides the detailed layer information. The

precise thickness control of the deposited layers can be confirmed through the high-resolution TEM image in **Fig. 3.3f** (blue box in **Fig. 3.3e**).

The detailed mechanism behind the color tunability is explained by the energy level and thickness of the layers. As can be seen from the energy band diagram in **Fig. 3.3c**, the holes injected from the ITO and HTL are easily transferred to the red EML throughout the entire working voltage regime, owing to the terraced highest occupied molecular orbitals (HOMOs) of the deposited layers. However, the electrons cannot overcome the barrier formed by the lowest unoccupied molecular orbitals (LUMOs) of DPEPO (2.0 eV) because of the electron blocking in the low-voltage regime (5~7 V), resulting in red emission by the recombination of triplet excitons in the red EML, as schematically described in **Fig. 3.3g**. In the higher-voltage regime (11~13 V), the accumulated electrons in the LUMOs of the red EML gain sufficient energy to overcome the thin (5 nm) barrier of the DPEPO, and generate the necessary excitons for recombination in the blue EML. At the same time, the DPEPO layer again acts as an energy barrier that blocks the energy transfer from the blue emission (2.7 eV) to the red emission (2.1 eV) owing to its high triplet energy (T_{DPEPO} = 3.1 eV).[42] Therefore, a clear blue emission results from the large amount of recombination in the blue EML, arising from the thickness difference between the two EMLs. Without the EBL, a red emission can be expected in both the low- and high-voltage regimes due to the favorable energy transfer from the blue EML to the red EML, as schematically depicted in **Fig. 3.3h**. Although some recombination of excitons in the blue EML can be expected in all voltage ranges, the dominant region

of emission would occur in the red EML, as the majority of the excitons in the blue EML would prefer a transfer to the lower triplet energy state of the red EML.

Figure 3.4a shows the optical camera images of the CTOLED at various operation voltages, illustrating a clear color change from dark red (5 V), to pale red (6~7 V), to white (8~10 V), to sky blue (11~12 V), and finally to deep blue (13 V). The current density (*J*)–voltage-luminance characteristics presented in **Fig. 3.4b** show a turn-on voltage of 4.5 V and a maximum brightness of 1,934 cd/m^2 at 13 V. The white emission can be explained by the balanced emission of blue and red. The amount of triplet excitons generated in the blue EML is directly proportional to the applied voltage, and so is the intensity of blue emission. Thus, it can be inferred that the color change from red to white, and then to blue is the result of the color balance between the red and blue emissions. This behavior is in good accordance with the electroluminescence (EL) spectra and the corresponding Commission Internationale de L'Eclairage (CIE) coordinates characterized from the CTOLED using 5-nm-thick DPEPO as the EBL (**Figs. 3.4c** and **3.4d**). According to the EL spectra, red-light emission is dominant at low operation voltages, while blue-light emission increases at higher operation voltages (**Fig. 3.4c**). Due to the changes in the emission intensities in the two EMLs, the CIE coordinates shift from red (0.62, 0.36) to white (0.32, 0.34), and then to blue (0.17, 0.33), by increasing the operation voltage from 5 to 13 V (**Fig. 3.4d**). The EL spectra and CIE coordinates of a CTOLED without the EBL indicate dominant emission of red light, which is also in good agreement with our hypothesis that the triplet excitons in the blue EML favor the energy transfer to the red EML,

instead of relaxation as blue light in FIrpic (**Figs. 3.4e** and **3.4f**).

To further verify the role of EBL in the CTOLED devices, different materials have been tested as EBLs, and their EL spectra have been characterized along with their corresponding CIE coordinates. When a 5-nm-thick TPBI is used as an EBL, the OLED emits only blue light (0.23, 0.31) in the same operation voltage ranges (**Figs. 3.4g** and **3.4h**). Unlike the case of DPEPO, electrons would be readily transferred to the blue EML even in the low-voltage regime, because TPBI acts as an ETL, which explains the occurrence of blue emissions starting from the turn-on voltage. Meanwhile, the relatively high triplet energy of TPBI (T_{TPBI} = 2.8 eV) results in partial blockage of the energy transfer from the blue EML to the red EML in all voltage ranges, allowing for some recombination of charges in the red EML. As a result, the emitted color from the OLED using TPBI as an EBL is light blue, and no color change is induced as the color balance between the red EML and the blue EML is maintained throughout the entire voltage regime. When a 5-nm-thick CBP is used as an EBL, a slight color shift from red (0.52, 0.37) to white (0.34, 0.34) can be observed on increasing the operation voltage (**Figs. 3.4i** and **3.4j**). It can be attributed to the relatively low triplet energy of CBP (T_{CBP} = 2.6 eV), which allows a major energy transfer of triplet excitons from the blue EML to the red EML in the high-voltage regime. The effect of the EBL thickness on the color tunability has been verified and characterized in **Figs. 3.5 ~ 3.7**, by testing 1-nm-thick and 10-nm-thick DPEPOs.

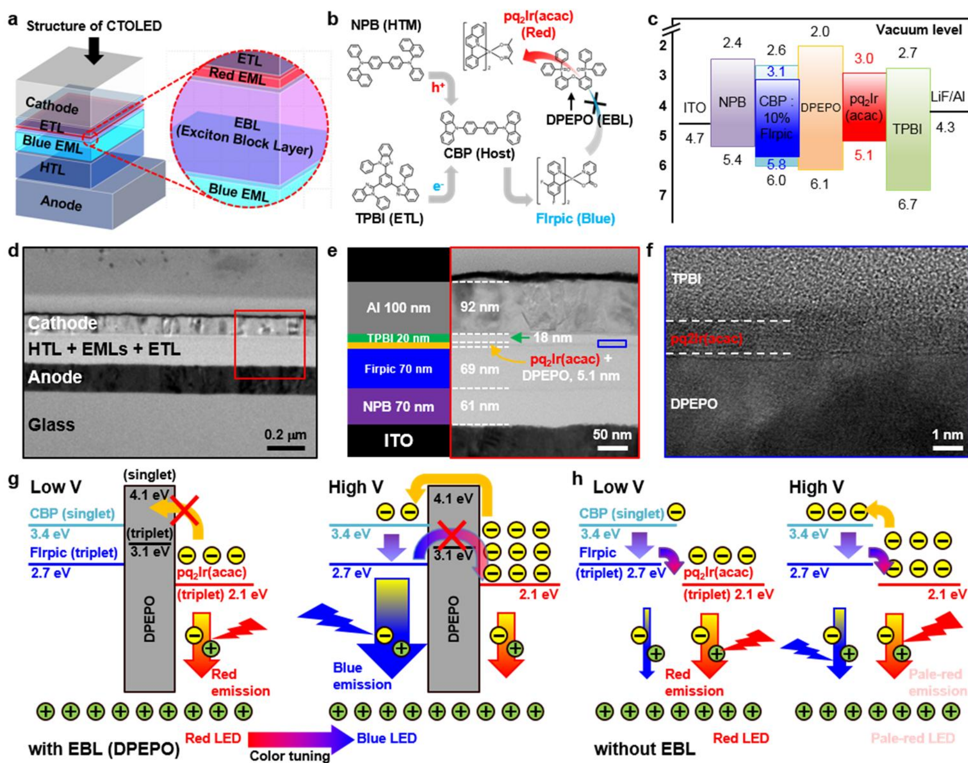

Figure 3.3. (a) Schematic illustration of the cross-sectional structure of a CTOLED. The magnified image shows the cross-sectional TEM image of an EBL sandwiched between two EMLs. (b) Chemical structures and brief roles of each layer of the CTOLED. (c) Energy band diagram of the CTOLED estimated using ultraviolet photoelectron spectrometry (thickness not drawn to scale). (d) Cross-sectional TEM image of the CTOLED. (e) Magnified TEM image showing the detailed cross-sectional structure of the CTOLED (red box in (d)). (f) High-resolution TEM image, magnified from the blue box in e). (g, h) Schematic illustrations of the color-tuning mechanism (g) with and (h) without the EBL.

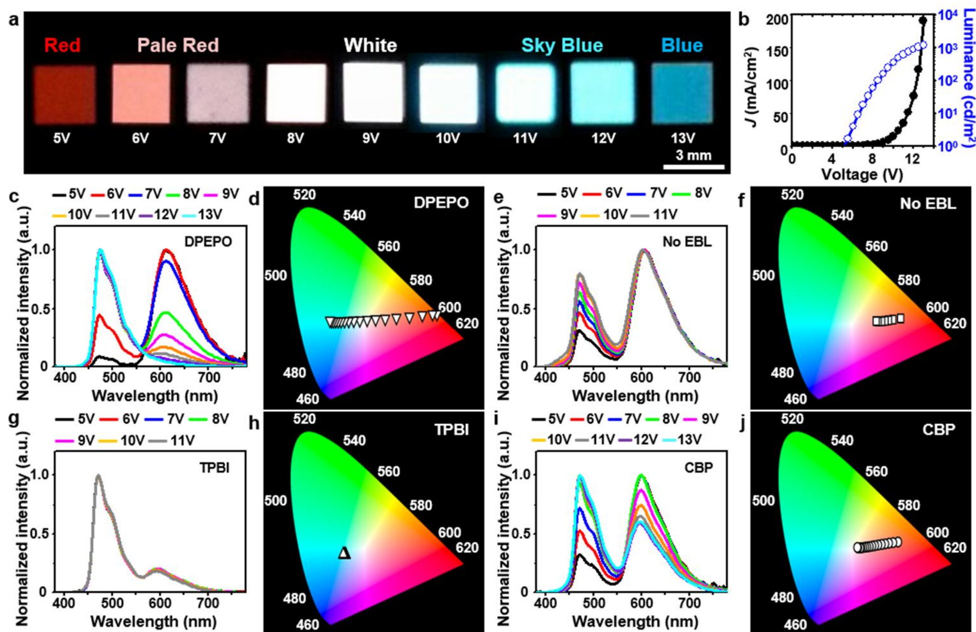

Figure 3.4. (a) Digital photographs of the CTOLED showing color changes from dark red, to pale red, to white, to sky blue, and to deep blue at different applied voltages. (b) *J*-*V*-*L* characteristics of the CTOLED. (c, e, g, i) EL spectra of the CTOLEDs using different EBLs of (c) DPEPO, (e) no EBL, (g) TPBI, and (i) CBP. The thicknesses of all EBLs are 5 nm, except for the no EBL case. (d, f, h, j) Corresponding CIE 1931 *x*-*y* chromaticity diagrams of the CTOLEDs using different EBLs of (d) DPEPO, (f) no EBL, (h) TPBI, and (j) CBP.

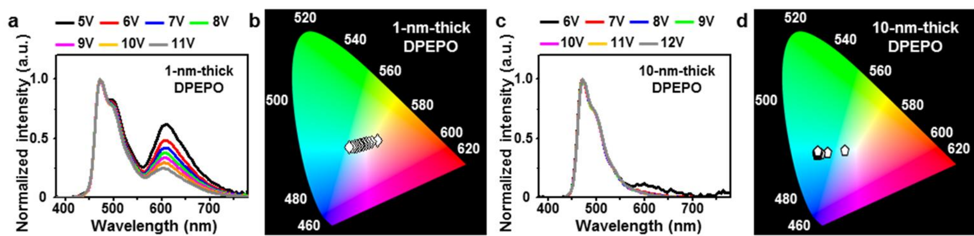

Figure 3.5. (a) EL spectra of the CTOLED using 1-nm-thick DPEPO as EBL and (b) its corresponding CIE diagram. (c) EL spectra of the CTOLED using 10-nm-thick DPEPO as EBL and (d) its corresponding CIE diagram.

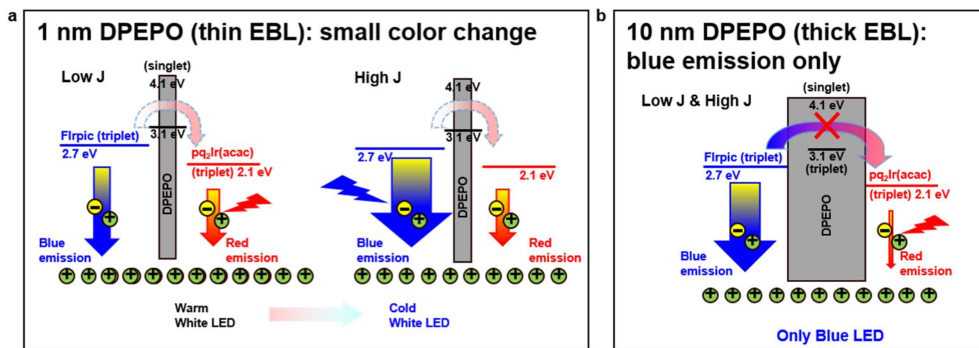

Figure 3.6. Schematic illustration of the mechanism explaining the color tuning behavior of the OLED with (a) 1-nm-thick EBL and (b) 10-nm-thick EBL.

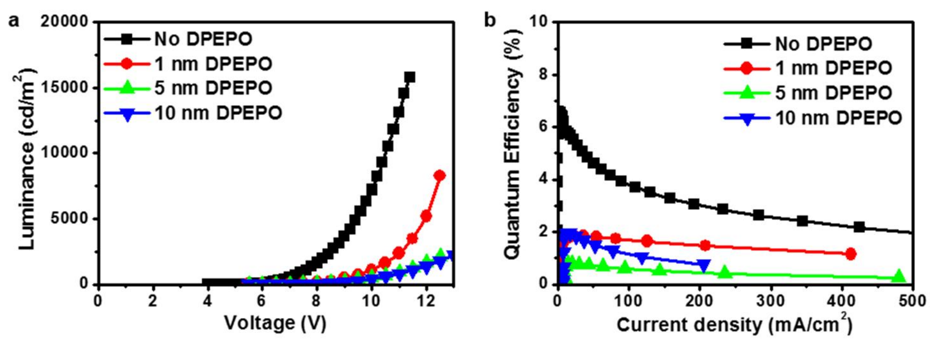

Figure 3.7. (a) Voltage-dependent luminance and (b) quantum efficiency characteristics of the fabricated CTOLED using EBLs with different thicknesses.

3.3.4 Mechanical stability characterization of the signal amplifiers and CTOLEDs

For wearable electronic/optoelectronic applications, it is crucial that the devices perform robustly even after repetitive deformations and that they withstand consequent fatigues. In this regard, the mechanical reliability of the *p*-MOS CNT inverter and the ultrathin CTOLED is verified under various deformed conditions (**Fig. 3.8**). The voltage transfer curves of the *p*-MOS inverter exhibit negligible changes after being worn on the skin and compressed inwards (**Figs. 3.8a** and **3.8b**). For further validation of the stability, up to 5,000 cycles of cyclic bending tests (to a bending radius of 5 mm) are performed, which show minimal shifts in the voltage transfer curves (**Figs. 3.8c** and **3.8d**). The deformability of the CTOLED is also tested. Although previous reports have already presented details of a substantial amount of effort toward developing flexible and/or stretchable LEDs based on inorganics,[15,16] quantum dots,[43-45] and polymers[46-48] for wearable displays, the mechanical robustness of an ultrathin wearable OLED with color-changing features has not yet been reported. The strategy to develop a wearable CTOLED is schematically illustrated in **Fig. 3.9** and details are described in the *Methods* section. The deformable CTOLED shows no degradation in the diode characteristics after folding (Fig. 5e). The photographs in **Figs. 3.8f ~ 3.8h** further confirm the robust performance of the CTOLEDs after folding against a slide glass, wrinkling on skin, and underwater operations, respectively. The stability of the wearable CTOLED is verified through cyclic bending tests (**Fig. 3.8i**), where both the red and blue emissions of the CTOLED

remain stable after 5,000 cycles of bending with a bending radius of 4 mm (**Fig. 3.8i** inset). In all, the excellent mechanical stability as well as wearability of our devices can be attributed to the ultrathin nature, use of intrinsically flexible materials, and effective passivation, and further improvements on the wearability can be expected by adopting stretchable designs (*i.e.* serpentine interconnections).[1]

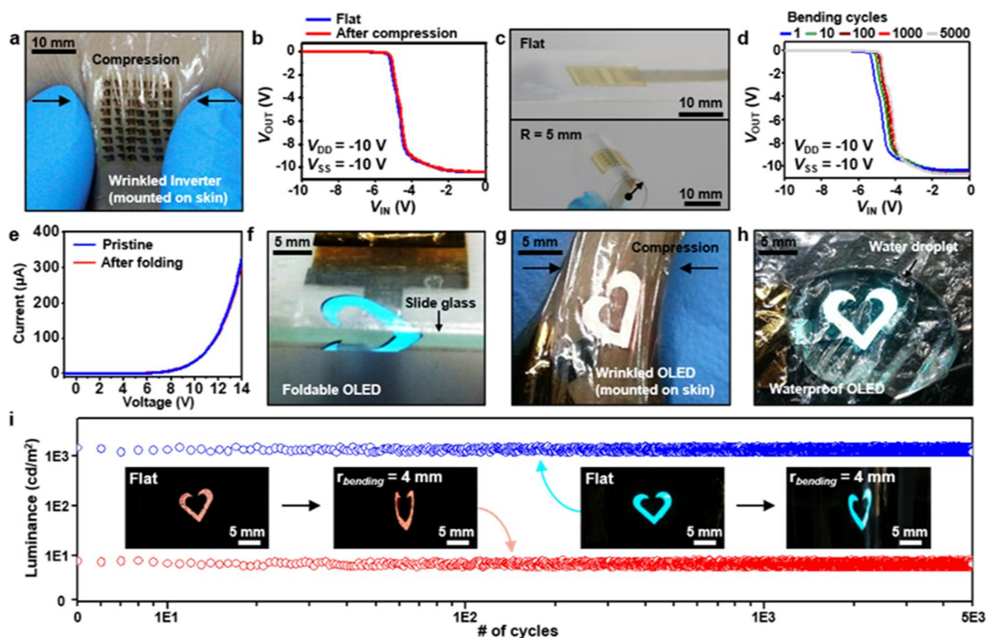

Figure 3.8. (a) Photograph of the CNT *p*-MOS inverter compressed after worn on human skin. (b) Voltage transfer characteristics of the inverter before and after compression, at V_{DD} and V_{SS} of -10 V. (c) Photographs of the inverter before bending (top) and after bending with a bending radius of 5 mm (bottom). (d) Voltage transfer characteristics of the inverter after the cyclic bending test up to 1,000 times, at V_{DD} and V_{SS} of -10 V. ($r_{bending}$ = 5 mm) (e) The *J*-*V* characteristics of the wearable CTOLED before and after bending. (f-h) Photographs of the CTOLEDs (f) after folding along a slide glass, (g) wrinkled after worn on human skin, and (h) under a water droplet. (i) Stable luminance of the blue and red emission during multiple bending experiments (with $r_{bending}$ = 4 mm, 1,000 times).

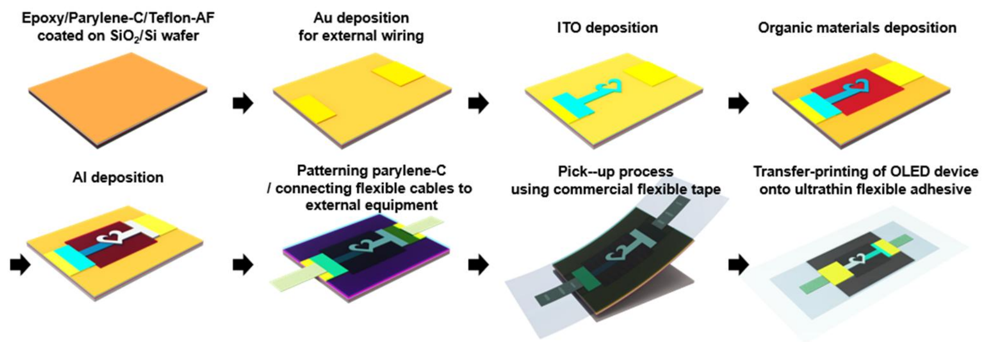

Figure 3.9. Schematic illustration of the fabrication process of wearable CTOLEDs.

3.3.5 Wearable health-monitoring platform based on ECG sensor, CNT signal amplifiers, and CTOLEDs

Finally, we demonstrate system-level integration of the wearable CTOLEDs with skin-mounted ECG electrodes and CNT signal amplifiers for the real-time display of cardiac signals through synchronized color changes of the CTOLED. **Figure 3.10a** depicts a photograph of wearable device components for the proposed monitoring system (inset shows a magnified view of the electrode). A DAQ and PC (not shown in picture) are used for analyzing the signals and delivering the adjusted voltage to the CTOLED. Specifically, the ECG signals are measured from human wrists using wearable ECG sensors, and then amplified using our *p*-MOS CNT inverters. The noise is then eliminated using high/low-pass filters (0.079/19.4 Hz). A diagram of the ECG signal processing procedure and a photograph of actual components consisting our wearable ECG monitor are described in **Fig. 3.11**. Customized software (LabVIEW, National Instruments, USA) analyzes the amplified ECG signals and delivers the adjusted voltage to the wearable CTOLED to indicate the cardiac health condition. Here, we deliberately program our software to distinguish a normal human ECG from an abnormal one (*c.f.*, abnormal cardiac signals were obtained from a postmyocardial infarction model[49]) through the color changes in the CTOLEDs (the detailed codes can be found in **Fig. 3.12**). As illustrated in **Fig. 3.10b** (right), a normal human ECG signal contains clear peaks of PQRST, which can be used to determine the activities of atrial depolarization, ventricular depolarization, and ventricular repolarization.

When a wearable ECG sensor detects a normal human ECG signal, our software delivers voltages that correspond to pale red, red, and white emissions to the CTOLEDs (5 ~ 9 V), resulting in a synchronized display of the ECG signals with the respective colors (**Fig. 3.10d**). On the other hand, when abnormal ECG signals (**Fig. 3.10c**) exhibiting delayed electrocardial conduction, such as pathologic Q waves or elevated ST peaks, are measured, the program delivers voltages corresponding to white, sky blue, and deep blue emissions to the wearable CTOLEDs (10 ~ 13 V). As a result, the CTOLEDs emit the respective colors that are synchronized with the amplitudes of the abnormal ECG signals (**Fig. 3.10e**). The system-level demonstration verifies the feasibility of a wearable indicator to display normal and diseased ECG signals.

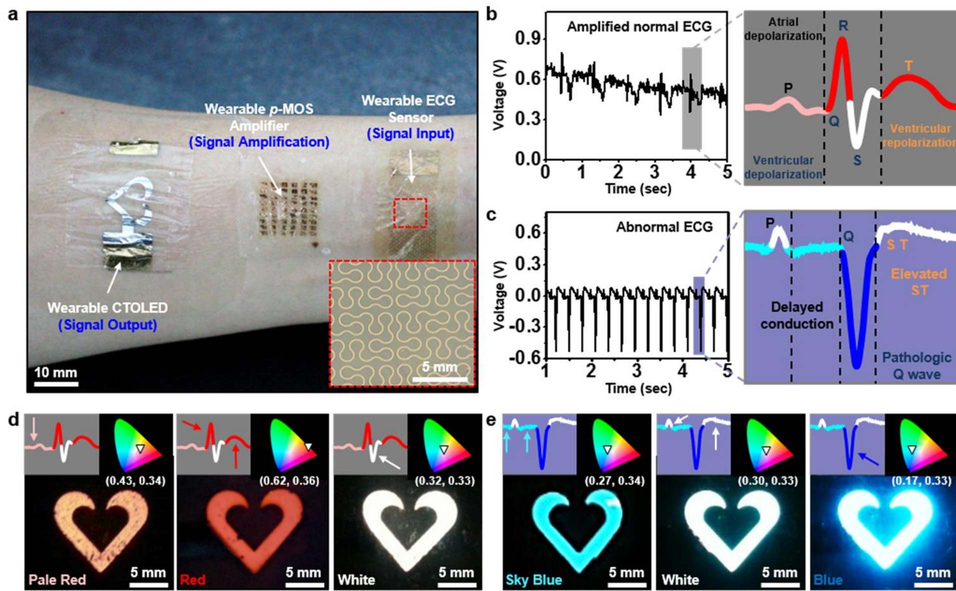

Figure 3.10. (a) Photograph of the wearable system for real-time visual-monitoring of the ECG signals, composed of the wearable ECG electrode, CNT *p*-MOS inverters, and CTOLEDs. (b) Normal ECG signals measured from a human wrist by using a wearable ECG sensor (left) and the detailed view of a single ECG signal after amplification showing PQRST peaks (right). (c) Abnormal ECG signals measured from an 8-week post-MI rat (left) and the detailed view of a single abnormal ECG signal. (d) Real-time color changes of the CTOLED, synchronized with the shape of the measured normal ECG signal. The insets indicate (left) the region of ECG signal for respective color emission and (right) corresponding CIE coordinates. (e) Real-time color changes of the CTOLED, synchronized with the shape of the abnormal ECG signal. The insets indicate (left) the region of ECG signal for respective color emission and (right) corresponding CIE coordinates.

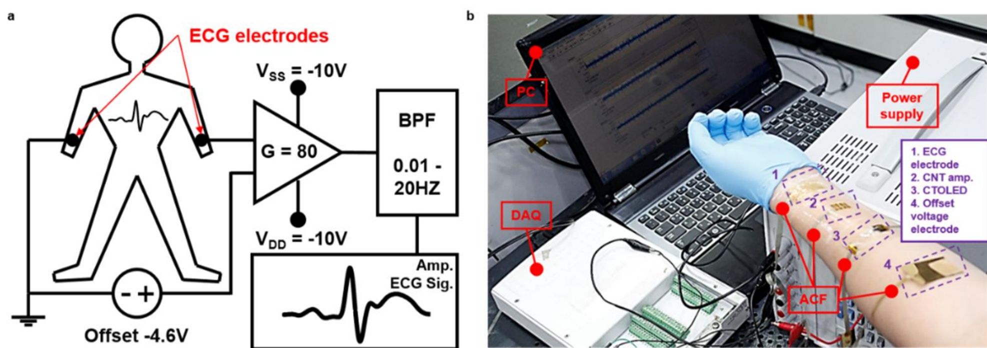

Figure 3.11. (a) Diagram of ECG signal processing procedure. (b) Photograph of the experimental setup including the DAQ unit, PC, and ACF wirings for the wearable ECG monitor system.

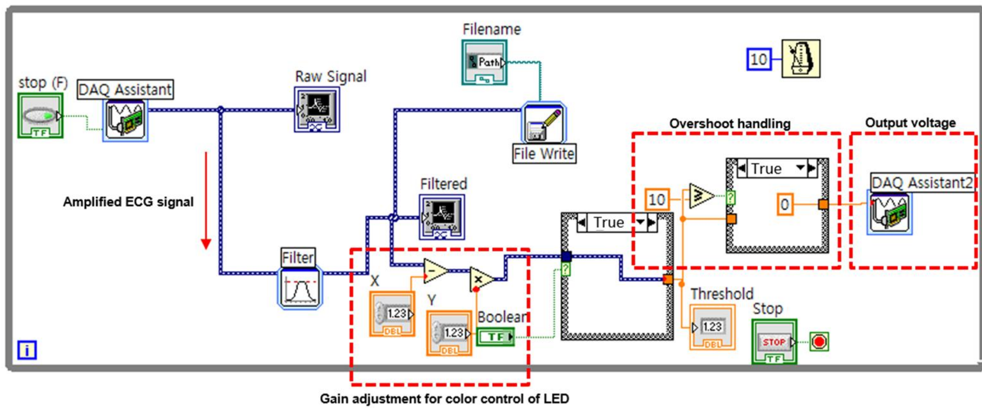

Figure 3.12. A block diagram of LabVIEW-based software for controlling the color of the OLED according to the ECG amplitude change.

3.4. Conclusion

In summary, an approach for the fabrication of ultrathin CNT electronics and color-tunable OLEDs toward a wearable ECG monitor and display was proposed. *p*-MOS inverters based on CNT transistors were developed successfully for the amplification of ECG signals. A comparative analysis on the optical properties of CTOLEDs employing different EBLs confirmed their roles, accompanied with a proper mechanism for the respective color-tuning behaviors. The ultrathin CNT electronics and CTOLEDs demonstrated high resilience against extreme bending and folding conditions, verified through repetitive bending/fatigue tests. System-level integration was accomplished whereby real-time ECG signals were visually displayed using the wearable devices. These advances will offer many opportunities for the development of future wearable biomedical monitoring devices.

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Chapter 4. Medium-scale electronic skin based on carbon nanotube transistors with vacuum-deposited stretchable dielectric film

4.1 Introduction

Soft electronics with skin-like properties have been extensively investigated over the past decade, demonstrating high potentials in versatile applications including but not limited to biomedical devices with health monitoring and therapeutic capabilities,[1-3] human-machine interfaces,[4,5] wearable/implantable optoelectronic devices,[6-8] and electronic skins.[9-11] The first-generation devices incorporated ultra-thin geometries with strain-tolerant designs to provide stable operation under various deformation modes and to make use of conventional inorganic materials for high electrical performances.[12,13] However, these strain-tolerant designs usually adopt island-type active components connected with wavy-patterned interconnects, which is space-consuming and thereby posing critical limitations in terms of device density and design of complex circuits in medium scale.[14,15] In this regard, investigation on the development of intrinsically stretchable circuits, which eliminates the need for wavy interconnects, has recently gained increasing attentions to attain skin-like electronics with maximized packaging density and circuit simplicity for performing sophisticated functionalities.

To develop intrinsically stretchable electronics, all the materials composing the electronics (i.e., electrodes, dielectrics, channel, and etc.) need to possess intrinsic deformability as well as excellent electrical properties. Moreover, these materials should be compatible to conventional fabrication techniques such as vacuum-deposition and photolithography for low-cost production, scalable fabrication, and reproducibility with excellent device uniformity. While several pioneering works have been reported on the fabrication of intrinsically stretchable transistors,[16-20] none has reported on the fabrication technology compatible with the current micro electro-mechanical systems fabrication technology. This is mainly attributed to the absence of technology for generating a high-quality stretchable insulating layer using vacuum-deposition tools. As such, the most advanced intrinsically stretchable transistors reported to this date employ solution-processed films such as polydimethylsiloxane (PDMS),[18] polyurethane (PU),[16,17] or polystyrene-block-poly(ethylene-ran-butylene)-block-polystyrene (SEBS)[20] as the gate dielectric. These solution-processed gate dielectric films are undesirable in terms of low dielectric constants (k, 2 ~ 3) and micrometer-scale thicknesses,[21-23] consequently resulting in poor electrical performances such as high operation voltages. Furthermore, conventional microfabrication techniques such as thin-film deposition and photolithography cannot be further applied due to their large thermal expansion coefficients,[24,25] and the inevitable complication in the fabrication process poses critical problems in the final device quality control (*i.e.* device-to-device performance uniformity).

Initiated chemical vapor deposition (iCVD) has been extensively

investigated as a method for synthesizing ultra-thin polymer gate dielectrics with promising performances such as excellent areal uniformity with thickness controllability and high dielectric constant.[26-28] Various flexible thin-film transistors employing iCVD-based dielectric layers have been reported, exhibiting low-power consumptions, bending-insensitive flexibilities, low leakage currents, and even high carrier mobilities.[29,30] Especially, the low thermal budget of the iCVD process makes it extremely appealing for deposition of high-quality dielectric layers with ultra-thin thicknesses (in nanometer regime) and excellent insulating properties on deformable substrates. Nonetheless, the use of iCVD has not yet been explored to develop stretchable dielectric layers, which requires a sophisticated synthesis strategy based on precise molecular control and optimal materials selection. The invention of such vacuum-deposited stretchable dielectric technology is highly expected to benefit the development of intrinsically stretchable electronics, in terms of boosting up the performances to a practical level.

Herein, we report a new materials strategy for the deposition of a stretchable dielectric layer using iCVD, and consequent fabrication of intrinsically stretchable electronics that is completely compatible to current micro electro-mechanical systems fabrication technology. The developed stretchable dielectric exhibits excellent thickness controllability, mechanical stability, and insulating properties, with higher k as compared to the commercially available PDMS and PU. Thin films of Au deposited on the stretchable dielectric and SEBS substrate of exhibit superb electrical performances even under high strains of 100%. Using networks of semiconducting

carbon nanotubes (CNTs) as the channel, intrinsically stretchable transistors with high yield and uniformity are fabricated whose electrical performances (*i.e.*, on-current density, mobility, and on/off ratios) are comparable to those fabricated using conventional inorganic layers. Such unprecedented performances enable the fabrication of stretchable logic gates and medium-level circuits composed of ~100 transistors, whose electrical/mechanical stability is validated through a wearable demonstration.

*** The contents of this chapter are to be submitted for publication**

4.2. Experimental section

4.2.1 Deposition of the stretchable dielectric films via iCVD process

The INA and V3D3 (95%) monomers were purchased from Tokyo Chemical Industry and Gelest, respectively. The *tert*-butyl peroxide (TBPO) initiator (97%) was purchased from Aldrich. All of the chemicals were used as received without further purification. The *p*(INA-*co*-V3D3), *p*INA, *p*V3D3 polymer films were deposited using a custom-built iCVD reactor. The INA and V3D3 were heated at 55 and 40℃, respectively, to obtain the desired flow rates. For synthesizing *p*INA and *p*(INA-*co*-V3D3), the flow rate of INA, V3D3, and TBPO were controlled by a needle valve as described in **Table 4.1**. During the process, the chamber pressure was maintained at 110 mTorr, and the filament was heated to 140 °C. The substrate temperature was kept at 35 °C.

4.2.2 Characterization of the stretchable dielectric films

The FT-IR and XPS spectra of the *p*V3D3, *p*INA, and *p*(INA-*co*-V3D3) were obtained using an ALPHA FT-IR spectrometer (Bruker Optics, USA) in absorbance mode and Sigma Probe Multipurpose XPS (Thermo VG Scientic) with a monochoromatized Al Kα source, respectively, to analyze the chemical composition of the synthesized copolymer films. To observe the surface morphology and roughness of the *p*I1V1, AFM images were taken by using a scanning probe microscope (NX-10; Park Systems). To test the mechanical properties of the dielectric films, all of the copolymers deposited on the slide glasses in an iCVD chamber were

scraped and formed a cylindrical shape. The mechanical properties of the polymer films were investigated by using a micro-force testing machine, Instron 8848 (Instron Inc.).

The electrical characterization of stretchable dielectric films was conducted by using an auto-stretching stage (Motorizer X-translation Stages, Jaeil optical system) and an electrochemical impedance spectroscopy (EIS) analyzer (ZIVE SP1, ZIVELAB). A sample of the stretchable MIM (Au/stretchable dielectric/Au) device was loaded on the stretching machine, and attached on the stage robustly by double-sided tape. Droplet of liquid metal (Gallium Indium eutectic, Sigma-Aldrich) was applied to the top and bottom electrodes respectively, and wires were buried in the droplet for interconnection between both electrodes and the EIS analyzer. In this way, the capacitance of the stretchable dielectric films under strain could be characterized on the stretching stage using the EIS method.[31] With an AC input voltage of 100 mV amplitude and 1 kHz frequency applied to the sample, the impedance of the films was measured according to the frequency, and the capacitance of the dielectric according to frequency was calculated based on the measured impedance. As stretched by 10% on the stage, the capacitance of the stretched sample was characterized in the same way as the pristine sample.

4.2.3 Fabrication and characterization of MIM devices

Glass substrates were cleaned by ultrasonication with the subsequent immersing in deionized (DI) water, acetone, and isopropanol (IPA). To fabricate a

rigid MIM device, 50 nm-thick Al bottom and top electrodes were fabricated by thermal evaporation with the deposition rate of 0.1 nm/s, and the polymer dielectrics were deposited by iCVD between Al electrodes. For a stretchable MIM device, the same procedures were followed except for using Au as the bottom and top electrodes, with the same deposition condition as Al. The electrical characteristics of the rigid MIM devices were measured by a B1500A semiconductor device analyzer (Agilent Technologies). The cross-sectional TEM images were obtained using a JEOL 200F electron microscope operated at 200 kV.

4.2.4 Fabrication and characterization of intrinsically stretchable CNT transistors and circuits

Glass substrates were cleaned by ultrasonication with the subsequent immersing in DI water, acetone, and IPA. An SEBS (H1052, purchased from Sigma-Aldrich) solution was first spin-coated on the glass substrate at 2,000 rpm, followed by multiple spin-coating of semiconducting CNT solution (0.01 mg/ML, aqueous solution) to form dense networks of CNTs. Source and drain electrodes were subsequently defined by thermal evaporation and standard photolithography, followed by the deposition of the stretchable dielectric using iCVD. After via formation (reactive ion etching), the gate electrodes were once again defined by thermal evaporation and photolithography. The devices were then transferred onto an SEBS substrate, separately prepared on a glass substrate by immersing and drying overnight. After making a close contact between the devices and the target SEBS

substrate, they were heated at 60 °C for 5 min on a hot plate to ensure conformal adhesion of the two SEBS layers, and were detached from the original glass substrate. The transfer and output curves were measured using the B1500A parameter analyzer. The electrical performances during stretching were measured using a similar method for stretchable MIM structures, by loading them onto an automatic stretching machine and using liquid metal droplets to connect the exposed electrodes to the parameter analyzer. For wearable demonstrations, anisotropic conducting films were connected to the electrodes of stretchable circuits for the electrical measurements.

Polymer	**Flow rate (sccm)**			**Deposition rate (nm/min.)**	**INA/V3D3 (in polymer film)**
	INA	V3D3	TBPO		
***p*INA**	0.211		0.798	5.8	
***p*I2V1**	0.527	0.552	0.570	4.2	96:4
***p*I1V1**	0.421	0.662	0.684	2.5	91:9
***p*I1V2**	0.379	0.795	0.821	1.3	87:13

Table 4.1. Flow rate of each monomer, deposition rate, and chemical composition

4.3 Result and discussion

4.3.1 Wearable electronic devices employing vacuum-deposited stretchable dielectric and electrode layers using iCVD

Figure 4.1a schematically illustrates the intrinsically stretchable electronic devices consisting transistors and logic gates, employing vacuum-deposited thin metal films and insulating layers as the electrodes and gate dielectrics, respectively. Specifically, the stretchable dielectric layer was deposited using iCVD, by copolymerizing isononyl acrylate (INA) and 1,3,5-trimethyl-1,3,5-trivinyl cyclotrisiloxane (V3D3) (**Fig. 4.1b**). The INA, an acrylic monomer containing long alkyl chain, was used as a soft segment due to its low glass transition temperature (T_g) with viscous property when converted to a polymer.[32] The V3D3 was used as a hard segment, as a crosslinker to maintain the polymer structure against repetitive stretching strain and to provide a robust insulating performance even with ultrathin thickness of the resulting layer.[33,34] The two monomers could be mixed homogeneously in the vapor phase at room temperature without a miscibility issue in the liquid phase, and the chemical composition of the resulting *p*(INA-*co*-V3D3) film could be delicately controlled by adjusting the input flow rate ratio of monomers to optimize the insulating and mechanical properties. The iCVD-based deposition of stretchable dielectric layer enabled scalable fabrication of stretchable electronics, compatible with the current vacuum-based micro-fabrication technologies used in the industry. The resulting electronics exhibited skin-like conformability and stretchability (**Fig. 4.1c ~ 4.1f**), high device yield with excellent device-to-device

uniformity, and electrical performances comparable to those fabricated using non-stretchable inorganic layers, as will be confirmed by the electrical performance analyses.

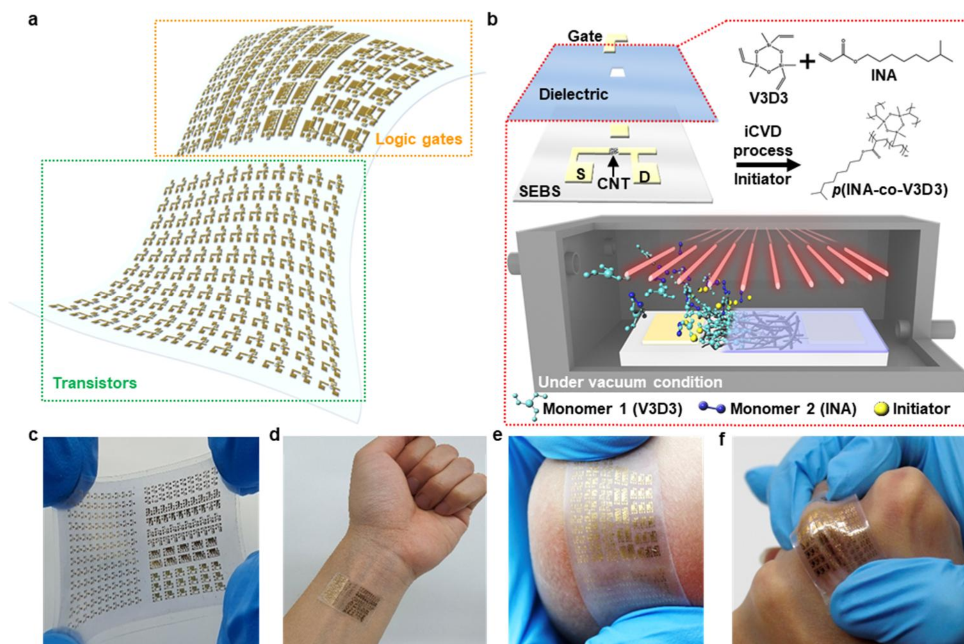

Figure 4.1. (a) Schematic illustration of the intrinsically stretchable devices employing (b) vacuum-deposited stretchable dielectric layer, deposited via iCVD. (c) ~ (f) Photographs of the intrinsically stretchable devices during various deformation and wearable modes.

4.3.2 Deposition and characterization of stretchable dielectric layers using iCVD

First, the suitability of the deposited *p*(INA-*co*-V3D3) film for stretchable electronics has been thoroughly examined, where films with three different chemical compositions (*p*I1V2, *p*I1V1 and *p*I2V1) were synthesized by controlling the input flow rate ratio of the INA and V3D3 monomers into the iCVD chamber, to find the film with the optimal stretchability and insulating performances. The flow rate information of each copolymer is summarized in **Table 4.1**. **Figure 4.2a** shows the Fourier transform infrared (FT-IR) spectra of *p*V3D3, *p*INA, and the copolymers. A C=C vinyl peak near 1,600 cm^{-1} was not detected in the spectra of all the polymers, verifying the successful radical polymerization via the iCVD process. All the polymers except for *p*V3D3 exhibited broad peaks near 2,840−3,000 cm^{-1} and peaks at 1730 cm^{-1}, which are associated with CH_2 and C=O stretching in the INA moiety, respectively.[35] On the other hand, all the polymers except for *p*INA showed asymmetric stretching peaks of Si-O-Si around 1,000 cm^{-1}, originated from the cyclotrisiloxane ring in the V3D3 segment,[36] and the peak intensities were gradually increased with increasing the V3D3 flow rate.

Next, the X-ray photoelectron spectroscopy (XPS) analysis was performed to estimate and compare the chemical composition of the deposited copolymer films quantitatively. The survey and high-resolution Si 2p spectra of the copolymers are depicted in **Fig. 4.2b**. The peak intensities of Si 2p were gradually increased with increasing the V3D3 flow rate. The chemical compositions of the copolymers were calculated from atomic percentages in the XPS survey spectra and summarized in

Table 1. The FTIR and XPS analyses clearly reveals that the chemical composition was systematically adjusted by controlling the input flow rate ratios of the INA and V3D3 monomers. In addition, the thickness of the deposited films could be controlled by varying the reaction time of the iCVD process, as confirmed by the cross-sectional transmission electron microscope (TEM) images of *p*I1V1 films in **Fig. 4.3**. The energy dispersive X-ray spectroscopy (EDS) images in **Fig. 4.3** verifies the chemical composition of the deposited *p*I1V1 film, comprised of C, O, and Si atoms. The XPS depth profile results of *p*I1V1 film also demonstrate the uniform distribution of the chemical composition throughout the film (**Fig. 4.4**), indicating a homogeneous synthesis of the copolymer films through the iCVD process.

The feasibility of the copolymer films as a stretchable dielectric was investigated by characterizing the insulating and mechanical properties. The insulating property was examined by fabricating metal/insulator/metal (MIM) structures on a stretchable SEBS substrate to analyze the dielectric performances of the deposited copolymer films. **Fig. 4.2c** plots the k values of copolymers which were estimated by calculating the slope of capacitance per unit area (C_i) versus the thickness (d) of the deposited films. The obtained k values were gradually increased from 3.14 to 3.59, and to 3.95 with increasing the portion of INA. The polarity of the carbonyl group in INA is most likely to cause this tendency.[37,38] The insulating properties of the deposited copolymer films is further examined by measuring the change in the leakage current density (J) while increasing the applied electric field (E_{field}) (**Fig. 4.2d**). It can be observed that the breakdown of the copolymer films

follows an opposite tendency as compared to the k measurements, where the films experience an early breakdown for higher amount of INA incorporation. Specifically, the estimated breakdown field (E_{break}) of *p*I2V1 was only 0.7 MV/cm, which is an insufficient insulating performance to serve as a gate dielectric layer. The E_{break} was significantly improved to 2.3 MV/cm, and 3.6 MV/cm for the *p*I1V1 and *p*I1V2 dielectric films, respectively, which is ascribed to the increased cross-linking density by the V3D3 crosslinker.[34,39]

The mechanical properties of the developed polymeric dielectric film should be thoroughly investigated to verify its feasibility as an insulating layer for stretchable electronics. As a first evaluation, the Young's modulus (*E*) of the copolymer films with different chemical compositions were calculated from a stress-strain curve (**Fig. 4.2e**). By increasing the portion of V3D3 cross-linker, the *E* values were also increased (**Table 2**) which signifies that the mechanical strength of the polymer films can be enhanced by adding more of the cross-linker moieties. The *E* values of *p*I1V2 (0.08 MPa) and *p*I1V1 (0.20 MPa) were suitable for practical device applications considering the *E* values of the human skin (*e.g.*, 25 ~ 220 kPa)[40] or silicon rubber-based dielectrics such as PDMS (*e.g.*, 0.57 ~ 3.7 MPa).[41] However, the change in ultimate tensile strain according to the chemical composition of the copolymers showed an opposite tendency (**Table 2**). The maximum deformation limit of the *p*I1V2 was only 17.7%, which is insufficient for stretchable device applications. However, with decreasing the portion of cross-linker, the tensile strain values were significantly improved to 81.5% and 158.7% for *p*I1V1 and *p*I2V1, respectively,

which is high enough for use in stretchable devices.[42] These results clearly indicate that the electrical and mechanical properties can be tuned by the manipulating the chemical composition between the soft (INA) and hard segments (V3D3) in the polymeric dielectric film. Considering both the robust insulating performance and mechanical deformability, the *p*I1V1 film was chosen as the optimal composition to serve as a stretchable dielectric layer for electronic device applications in this work.

Next, the insulating properties of the deposited *p*I1V1 film during stretching modes were investigated, by measuring the change in capacitance using MIM structure at various frequencies, with respect to stretching at different levels of strain. It should be noted that, to evaluate such property with high credibility, the metal layers used in the MIM structure must support a high stretchability and conductivity simultaneously, such that the measured capacitance values are accurate and unaffected by the change in electrical performance of the metal layers. To the best of our knowledge, this is the first time to report a proper characterization of a stretchable dielectric layer. This was enabled by employing vacuum-deposited Au thin film electrodes on stretchable layers of SEBS substrate and *p*I1V1, of which the excellent conducting and stretchable characteristics of vacuum-deposited metal thin films on stretchable supports have been well explored previously.[43,44] The Au/*p*I1V1 structure maintained its conductivity after being stretched to 100% strain, and exhibited minimal changes in the resistance with respect to applying 40% strain, even after 1,000 stretching cycles (**Fig. 4.5**). This verifies the high fidelity of the developed stretchable electrode based on Au thin films on *p*I1V1 as well as its excellent

applicability to skin electronics, considering that the human skin generally can be stretched to ~30% strain.

The TEM images of **Supplementary Figs. 4.6a** and **4.6b,** which depict cross-sectional views of the MIM structure with *p*I1V1 as the dielectric layer before and after being stretched to 100% for 1,000 cycles, respectively, further confirms the stable operation of the Au thin films on the stretchable *p*I1V1 layer. The TEM images show no signs of film delamination or interfacial damage at the electrode/dielectric interface after the cyclic stretching. Furthermore, the representative magnified cross-sectional TEM images of the top and bottom electrodes of the MIM structure in **Figs. 4.6e** and **4.6f** show that the electrodes remain unbroken after the cyclic stretching, although noticeable cracks are generated when compared to the magnified TEM images of the unstretched sample in **Figs. 4.6c** and **4.6d**. This infers that the moderate increase in the resistance of the stretched Au film can be attributed to the crack formation on the Au film, while the stretched film still remains conductive due to the maintaining of the electrical pathways.

With the evaluation platform for electrical properties of the stretchable dielectric under strain verified, the electrical properties of the *p*I1V1 film under strain were characterized by the newly devised method. (See Methods for detailed experimental setup and measurement procedures.) The *C*-*F* curves of the MIM devices with *p*I1V1 as a dielectric layer for different tensile ranges are plotted in **Fig. 4.2f**, over a wide range of operating frequencies. The C_i of a pristine *p*I1V1 film was approximately 5 nF/cm^2 over the entire operating frequencies, and the value was

maintained in between 3.9 ~ 4.4 nF/cm^2 during stretching, with the maximum tensile range of 40%. This result indicates the excellent stability of the *p*I1V1 film under strain. The durability of the stretchable dielectric film in the repeated stretching situation is verified in **Fig. 4.2g**. The *p*I1V1 film exhibited cyclic durability under repetitive stretching (up to 40% strain) and release over 1,000 cycles. Since the stretchable gold electrodes employed in the MIM devices have electrical stability with the resistance less than 20 ohms in the tensile range of 40% (**Fig. 4.5**), the reliability of the capacitance of the stretchable dielectric film can also be guaranteed. The *J-E* curves of the MIM devices with *p*I1V1 as a dielectric layer for different thicknesses are shown in **Fig. 4.2i**. The *p*I1V1 film exhibited an excellent insulating performance with an extremely low *J* (lower than 1.0×10^{-8} A/cm^2 in the range of ±1 MV/cm) even for the thickness of 184.7 nm, which is, to the best of our knowledge, the lowest thickness among the stretchable organic dielectric materials.[16-20,24,39] It is worthwhile to note that this superior insulating performance can be attributed to the iCVD process, which enables for the optimization of the film's chemical composition. Our vapor-phase method allows a defect-free deposition of the copolymer film, as shown in the atomic force microscope (AFM) image (**Fig. 4.2j**). No obvious phase separation between INA and V3D3 were observed, which verifies the formation of a homogeneous copolymerization.[45] Moreover, a 200 nm-thick *p*I1V1 film exhibited a smooth surface morphology with the root-mean-square roughness (R_{ms}) of less than 1 nm, which is crucial for both dielectric and device performances,[46] as well as for further microfabrication processes such as film deposition and photolithography.

Finally, large-area thickness uniformity is of the highest importance in terms of high throughput of device fabrication with minimal device-to-device performance variations. In this regard, the large-area uniformity of the iCVD film deposition on an 8-inch Si wafer has been investigated using an ellipsometer (**Fig. 4.2k**). An average thickness of 89.5±2.05 nm was obtained by measuring from 25 different points of the 8-inch wafer (**Fig. 4.2l**), showing an excellent uniformity in terms of the deposited film thickness. Moreover, the deposition of the stretchable dielectric film is independent of the substrate type (**Fig. 4.7**), which is a well-known feature of the iCVD process.[26-28] The excellent uniformity of the iCVD process with superior thickness controllability and insulating properties, in conjunction with vacuum-deposited stretchable Au thin films enabled the fabrication of intrinsically stretchable transistors which were further applied to construct various logic gates and medium-level circuits with unprecedented complexity.

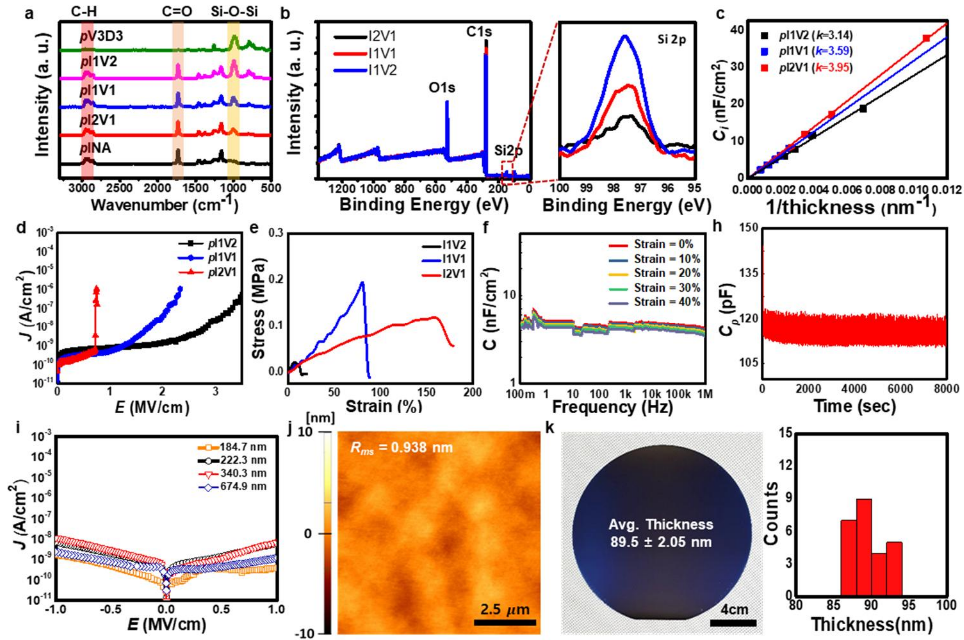

Figure 4.2. (a) FT-IR spectra of the deposited stretchable dielectrics. (b) The survey and high-resolution Si 2p spectra of the deposited layers. (c) Estimated k values, (d) J-E_{field} characteristics, and (e) stress-strain curve of the stretchable dielectric layers with different monomer compositions. (f) C-F curves of the MIM device employing *p*I1V1 dielectric layer, during different strains applied. (h) Cyclic test of *p*I1V1 for capacitance measurements during 1,000 cycles at 40% strain. (i) J-E curves of the MIM devices with *p*I1V1 as a dielectric layer for different thicknesses. (j) Representative AFM image of *p*I1V1 surface. (k) Large-area uniformity of the stretchable dielectric deposition process using iCVD on 8-inch wafer.

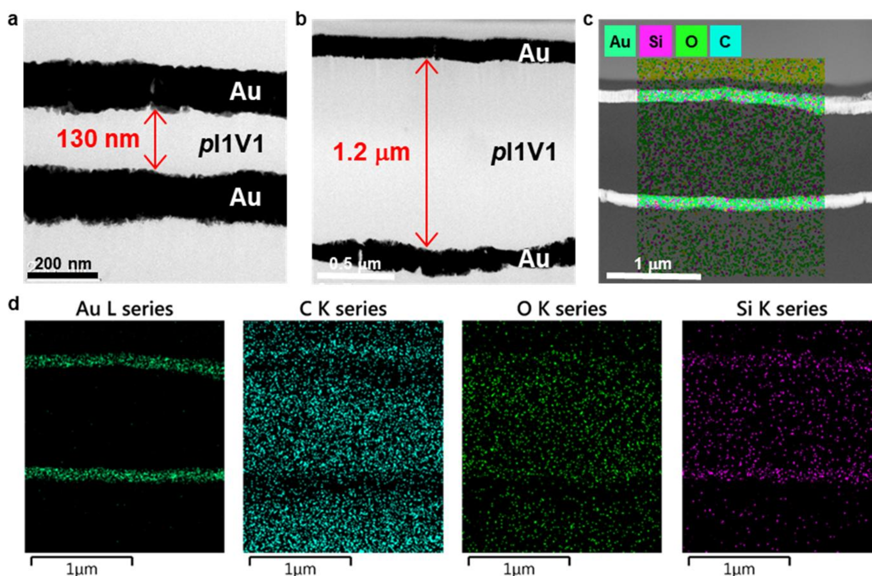

Figure 4.3. (a),(b) Cross-sectional TEM image of *p*I1V1 in Au/*p*I1V1/Au configuration. (c) Layered EDS image and (d) spectra of the deposited *p*I1V1 film.

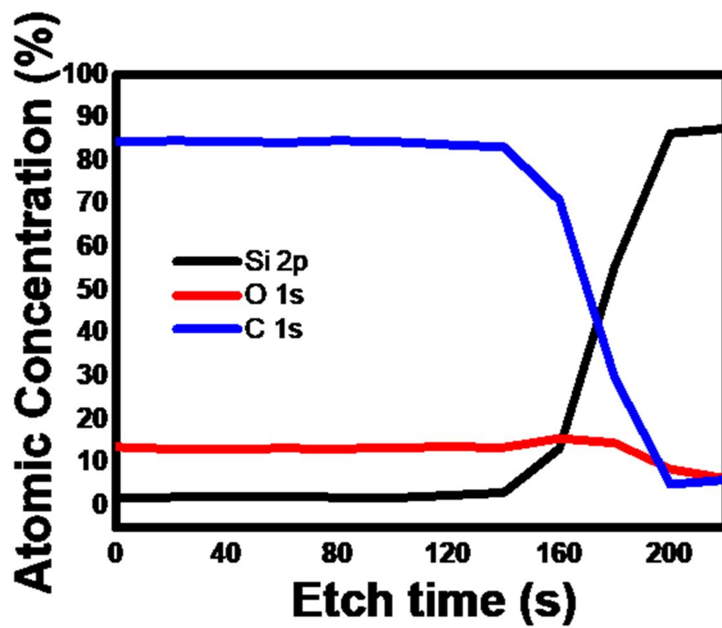

Figure 4.4. Depth profile analysis of the deposited *p*I1V1 film

Sample	Young's modulus (MPa)	Ultimate tensile strain (%)
*p*I2V1	0.32	17.7
*p*I1V1	0.20	81.5
*p*I1V2	0.08	158.7

Table 4.2. Mechanical properties of the copolymers from stretching tests

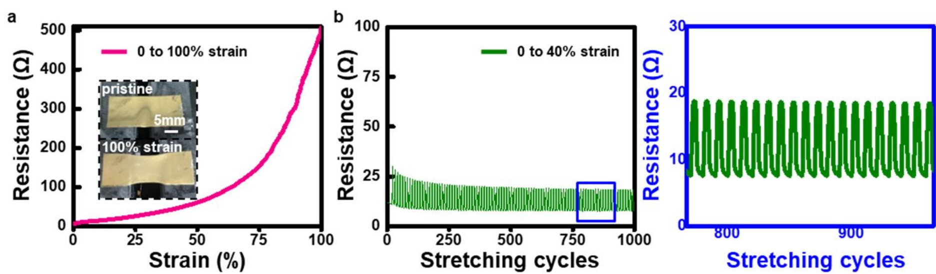

Figure 4.5. (a) Change in resistance of the stretchable Au electrode on pI1V1 with respect to increasing strain. The inset depicts photographs of the pristine and 100% stretched electrode. (b) Cyclic stretching test of the sample in a), by applying 40% strain. The plot on the right shows a magnified region in a blue box in the left plot.

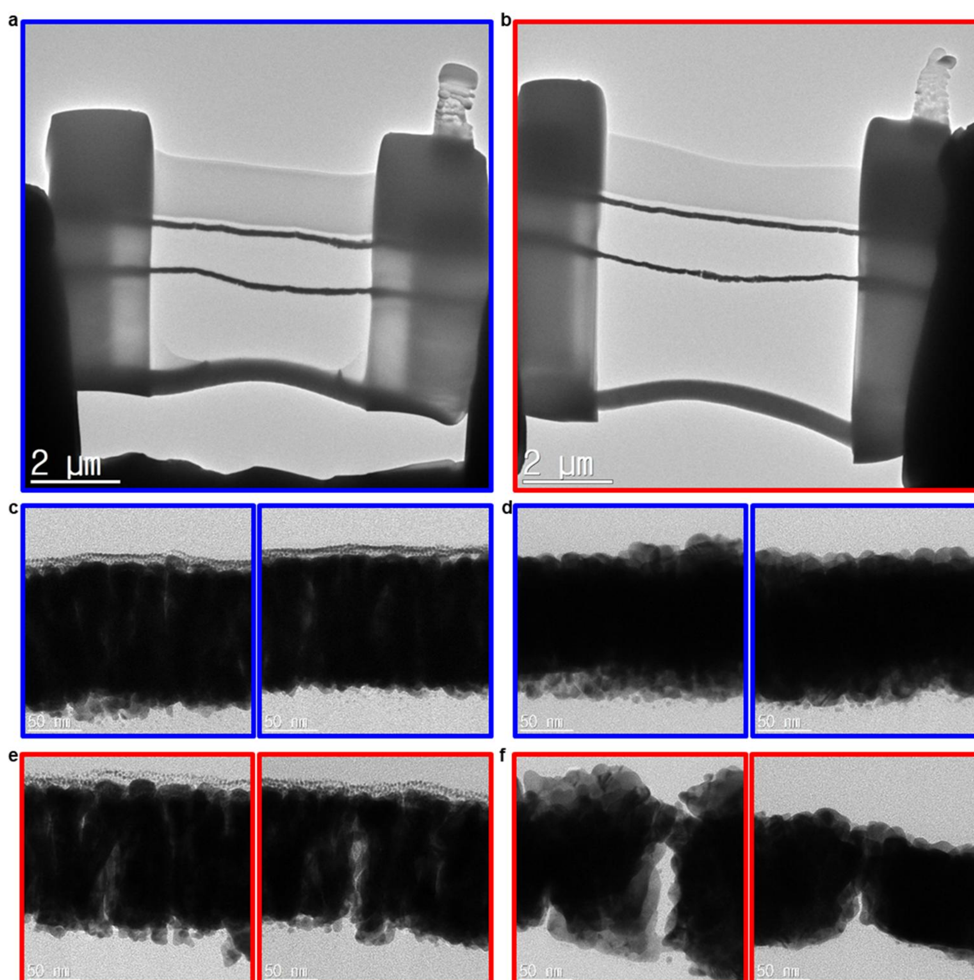

Figure 4.6. Cross-sectional TEM images of MIM samples loaded on a TEM grid, featuring a) pristine sample and b) sample after being stretched to 100% for 1,000 cycles. c) Representative magnified images of the upper electrode showing different spots of a). d) Representative magnified images of the lower electrode showing different spots of a). e) Representative magnified images of the upper electrode showing different spots of b). f) Representative magnified images of the lower electrode showing different spots of b). The scale bars in c~f) indicate 50 nm.

Figure 4.7. Photograph of the iCVD deposition on various substrates. On the left column, from the top features a bare image, iCVD deposited on PET, SEBS/glass, and Si wafer. On the right column, from the top features iCVD deposited on glass, PDMS, Ecoflex, and Latex.

4.3.4 Fabrication and characterization of intrinsically stretchable CNT transistors and logic gates

Figure 4.8a illustrates the representative transfer curves (I_d-V_g; drain current-gate voltage) of the intrinsically stretchable transistors with different channel lengths (L = 10, 30, 50, 100 μm) without applying any strains, at the applied drain voltage (V_d) of -1 V. The detailed fabrication process of the intrinsically stretchable transistors is described in the methods section. Owing to the use of nanometer-thick dielectrics (thickness of ~60 nm), the operation voltage of the stretchable transistors was substantially reduced as compared to the previously reported works on intrinsically stretchable transistors employing spin-coated dielectrics with micrometer thicknesses.[16-20] **Figure 4.8b** shows the cumulated transfer curves of the 50 transistors with L = 10 μm (the cumulated transfer curves of L = 30, 50, and 100 μm are shown in **Fig. 4.9**), which exhibit high device-to-device uniformity with minimal variations in the on/off ratios, on-current densities, and threshold voltages. The trend of increase in on/off ratios with respect to increasing L is in good agreement with the reported characteristics of CNT transistors,[47] which is primarily attributed to the averaging effect of metallic CNTs in transistors with longer channels (**Fig. 4.8c**). Inversely, the on-current density was higher for transistors with shorter L, which can also be explained by the inclusion of relatively more metallic CNTs within the shorter channels and lesser amount of junction contacts formed (**Fig. 4.8d**). Overall, the intrinsically stretchable CNT transistors with ~60-nm-thick *p*I1V1 film as the gate dielectric exhibited similar electrical performances as those fabricated using ~35-nm-

thick Al_2O_3 layers for the gate dielectrics in our previous reports,[48,49] which can be regarded as a significant breakthrough for intrinsically stretchable transistors whose electrical performances are generally not comparable to those fabricated using inorganic layers.

The mechanical stability of the fabricated intrinsically stretchable CNT transistors was evaluated by measuring the transfer curves before stretching, during stretching at 40% strain, and after stretching at 40% for 1,000 times. The transistors can be stretched parallel (**Figs. 4.8e, 4.8g** and **Fig. 4.10**) and perpendicular (**Figs. 4.8f** and **4.8h**) to the direction of charge transport without noticeable changes in their electrical performances, proving its high potential for skin electronic applications. No signs of film delamination could be observed even after repeated stretching cycles, inferring that the interface shear and vertical stresses were effectively suppressed.[50] The high performance uniformity and mechanical stability of this fabrication platform enabled the development of intrinsically stretchable basic circuit elements such as NAND, AND, NOR, OR, XOR, and XNOR gates. The stretchable logic gates exhibited stable operations under 40% strain with almost identical operations as compared to the original state, as shown through **Figs. 4.8i ~ 4.8n**, demonstrating the feasibility of using them as the basic building blocks for more complex circuits with stretchability.

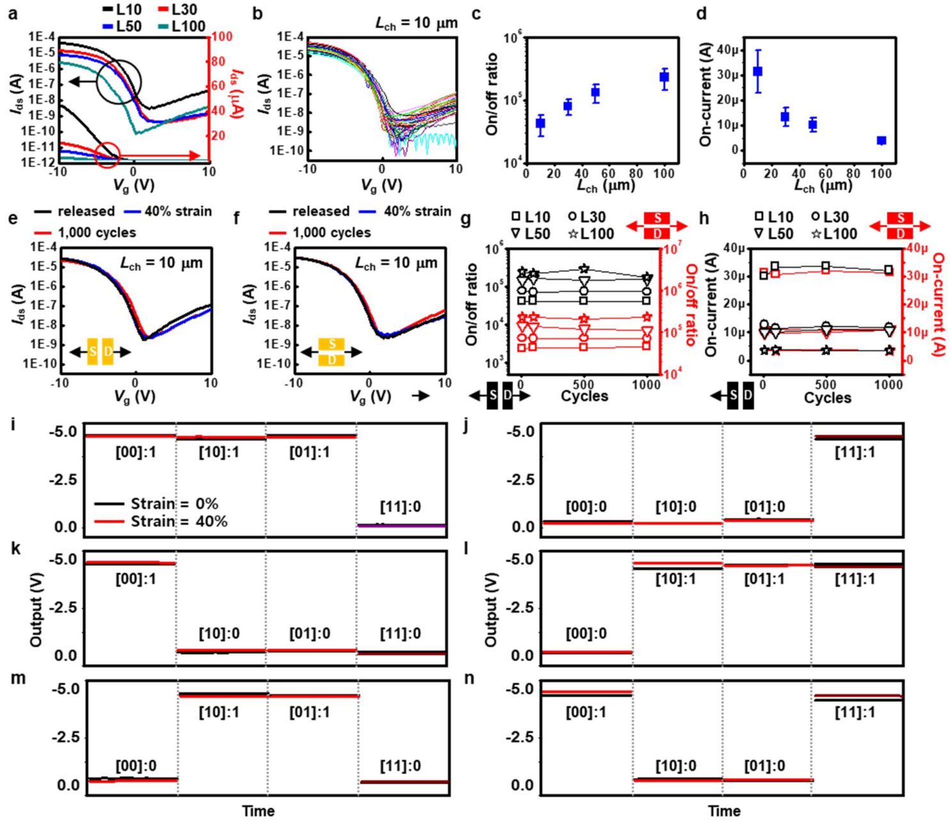

Figure 4.8. (a) Representative transfer curve of intrinsically stretchable CNT transistors with varying *L*. (b) Cumulative transfer curves of the transistors with L = 10 μm. Trend of (c) on/off ratios and (d) on-current densities of the transistors with respect to increase in *L*. Transfer curves before stretching, after stretching with 40% strain, and after 1,000 cycles of repeated stretching with 40% strain, with respect to (e) parallel and (f) perpendicular direction to charge transport. Change in (g) on/off ratios and (h) on-current densities during cyclic stretching with 40% strain. (i)~(n) Output characteristics of various logic gates before and during stretching with 40% strain.

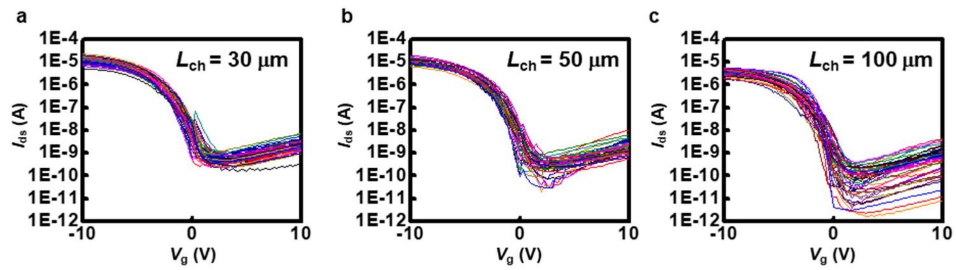

Figure 4.9. Cumulative transfer curves of 50 transistors with (a) L = 30 μm, (b) L = 50 μm, and (c) L = 100 μm.

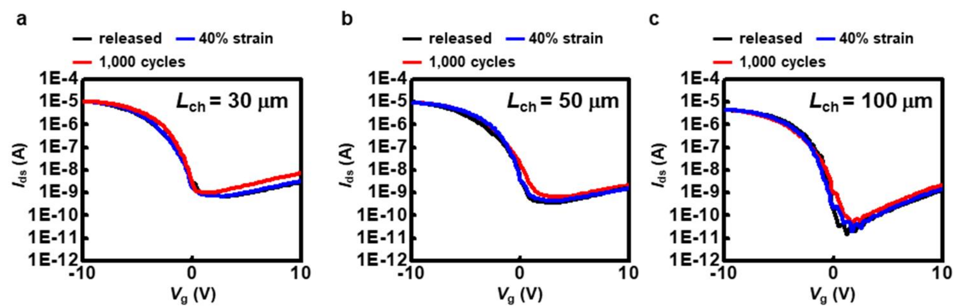

Figure 4.10. Representative transfer curves of transistors with (a) L = 30 μm, (b) L = 50 μm, and (c) L = 100 μm, before stretching, after stretching at 40% strain, and after stretching at 40% strain for 1,000 cycles.

4.3.5 Intrinsically stretchable CNT transistors for medium-level circuit demonstration

As a proof of concept, a medium-level circuit incorporating ~100 transistors was realized using the logic gates as the basic building blocks. **Figure 4.11a** represents the circuit diagram of a 2-bit magnitude comparator, which require collective operation of 15 separate logic gates, corresponding to 91 *p*-type CNT transistors. The development of such medium-level circuit using strain-tolerant interconnections would require much higher complexity in terms of circuit design; in this study, a compact circuit design could be developed to fit all the necessary transistors within the area of 5 × 1 mm^2. The 2-bit magnitude comparator could successfully differentiate the magnitude of inputs, and showed a stable logic operation after worn on skin (**Fig. 4.11b**). Such results further validate the high fidelity of our fabrication platform based on vacuum-deposited layers of gate dielectric and electrodes, which can be stretched well without any degradation of their electrical performances.

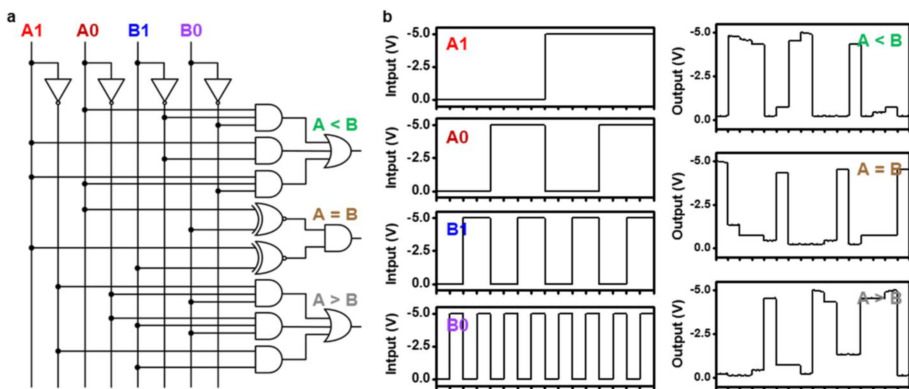

Figure 4.11. (a) Circuit diagram of 2-bit magnitude comparator consisting various logic gates (91 transistors). (b) Output characteristics of the 2-bit magnitude comparator

4.4 Conclusions

In summary, a novel fabrication strategy of intrinsically stretchable electronic devices has been presented, based on iCVD process for vacuum-deposited gate dielectric with excellent thickness controllability, large-area uniformity, and high stretchability, and vacuum-deposited metal thin films exhibiting both excellent conductivity and stretchability. The fabricated intrinsically stretchable transistors exhibited electrical performances comparable to those fabricated using inorganic materials, which can be mainly ascribed to the use of ultra-thin gate dielectric layers with thicknesses in the nanometer range, allowing for excellent gate control at significantly lower operation voltages as compared to the most advanced stretchable electronics reported to this date. Our stretchable electronics were used to demonstrate advanced electronic functionality with high skin-like stretchability, and we anticipate further research for development of vacuum-deposited stretchable layers for applications beyond skin-like electronics.

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요약 (국문초록)

신축성 있고 착용 가능한 탄소 나노튜브 기반 전자 기술

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탄소 나노튜브는 뛰어난 전기적, 화학적, 그리고 기계적 특성을 갖고 있어 차세대 유연 전자소자의 핵심 소재 중 하나로 각광을 받고 있으나, 아직까지 이를 이용한 실용적인 유연 전자소자의 개발은 실현되지 않고 있다. 이는 탄소 나노튜브의 전기적 특성대로 완벽히 분류해 낼 수 있는 기술, 탄소 나노튜브를 소자의 원하는 위치에 정확히 원하는 양만큼 네트워크 형태 혹은 정렬된 형태로 증착하는 기술, 그리고 유연 전자소자를 구성하는 다른 물질들의 개발 기술의 부재 때문이다. 지난 10여년간 해당 기술들은 광범위하게 연구되어지고 있으나, 탄소 나노튜브를 활용한 우수한 유연 전자소자 개발을 위한 핵심 기술들의 발전은 아직 초기 단계에 있다.

따라서 이 논문을 통해 탄소 나노튜브를 유연 전자소자에 적용시킬 수 있는 새로운 기술을 소개하고자 한다. 첫번째로 탄소 나노튜브와 유연 전자소자의 소자 디자인을 이용하여 피부위에 증착 가능한 비휘발성 메모리 소자를 제작하였고, 해당 기술을 이용하여 피부위에서 안전하게 동작

할 수 있는 다양한 기초 회로들을 구현하였다. 탄소 나노튜브 기반 메모리 전자 소자 및 회로는 다양한 외부 응력이 가해져도 안정적으로 동작을 하였고, 개발된 기술을 통해 보다 실용적인 탄소 나노튜브 기반 유연 전자 소자의 제작 조건을 확립할 수 있었다.

두번째로 위에 개발된 기술을 바탕으로, 보다 복잡한 탄소 나노튜브 기반 유연 회로 및 구동전압에 따라 발광색이 변환하는 색변환 소자를 제작하여 해당 소자들이 피부위에 부착되어 잘 작동되도록 구현하였다. 그리고 이 두 가지 웨어러블 전자소자를 통합하여 실시간으로 심전도를 측정하여 탄소 나노튜브 기반 전자소자를 통해 해당 신호를 증폭시키고, 신호의 상태를 색변환 소자로 나타낼 수 있는 심전도 모니터 시스템을 구현하였다.

세번째로 진공 증착이 가능한 유연 절연체를 개발하여, 기존의 유연 전자소자들이 가지고 있던 극명한 한계를 극복하였다 (높은 구동 전압, 낮은 집적도, 대면적 소자 선능 균일도 등). 기존의 액상 기반 증착을 위주로 한 유연 전자 소자들은 무기물질 기반 전자소자 대비 극심한 성능 저하를 보여주었는데, 이를 해결하기 위해 새로운 절연물질을 개발하고 탄소 나노튜브 기반 유연 전자소자에 적용하여 그 가능성을 보여주었다.

주요어: 탄소 나노튜브, 플렉서블 전자소자, 스트레쳐블 전자소자, 웨어러블 전자소자, 유연 전자소자