M.S. DISSERTATION

Resistive Switching Synaptic Device with High Rectification Ratio and its Impact on Spiking Neural Network

높은 정류비를 갖는 저항변화 시냅스 소자의 제작 및 스파이킹 뉴럴 네트워크에 미치는 영향 분석

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Abstract

This thesis suggests reverse leakage current problem which can occur when resistive random access memory (RRAM) is integrated as synaptic device with integrate-and-fire (IF) neuron circuit in spiking neural network (SNN). To this issue, self-rectifying RRAM was proposed as a solution. Ni/W/SiN_x/n-Si RRAM with different bottom electrode (BE) doping concentration was fabricated and measured. Their DC and rectifying characteristics were analyzed based on the measurement data. Among them, self-rectifying RRAM with lowest BE doping concentration exhibited foremost rectifying characteristics without any additional selector or diode device. Furthermore, hardware-based system level simulation was conducted to evaluate the effect of self-rectifying RRAM synapse on spiking neural network. As a result, total 10.2%p of accuracy increment was obtained in MNIST pattern recognition simulation, utilizing the proposed RRAM.

Keyword : Resistive random access memory (RRAM), synaptic device, neuromorphic, self-rectifying, system level simulation
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Chapter 1

Introduction

Neuromorphic systems have drawn attention for their low power consumption and parallel computing [1, 2, 3]. They often employ spiking neurons as the primary units of signal processing, which are biologically plausible artificial neuron models where tasks are performed by action potentials [4]. Among various neural networks, spiking neural network (SNN) is one of the well-known neural networks having great potential for its energy-efficient computing [5, 6, 7]. It is composed of neurons and synapse which are mostly represented by circuits and synaptic devices respectively. Previously reported integrate-and-fire neuron circuit serve as a unit that constitute SNN [8]. Integrate-and-fire circuit integrates presynaptic signals with respect to time and deliver signals to the synapses connected to the axons when its membrane voltage reaches threshold. While broadly used non-SNNs where input and output values are represented by real numbers, those values are represented by firing rate or spike timing of neurons in spiking neurons [9]. In addition, their operation are time-dependent in that they integrate the signal over

time.

Despite these differences, researchers have discovered that SNNs with spike-rate coded data is equivalent to non-SNN with Rectified Linear Unit (ReLU) activation function [4, 11]. SNNs can be trained online with various methods which is biologically plausible, such as Spike-Timing Dependent Plasticity (STDP), or it can be trained offline by weight transfer from non-SNN with the same structure [11]. These approaches allowed the researchers to successfully perform machine learning tasks such as pattern recognition and time-series analysis with SNNs. Some of the research groups have been successfully integrated synaptic devices and neuron circuits which has been presented on VLSI [12, 13].

To construct hardware based SNN, many researchers made effort to build artificial neuron circuits for intelligent systems such as integrate-and-fire circuit. For the synapse, there has been many attempts to integrate Resistive Random Access Memory (RRAM) with neuron circuit owing to their great advantages of low power, high scalability, gradual switching characteristics, and extensibility to 3D structure [14-22]. However, despite the strengths, serious problems arise when RRAM is integrated with IF circuit as synapse.

In this paper, we propose a serious problem which can occur in hardware based SNN when RRAM is used as synaptic device. Since RRAM is a passive, bidirectional device, current may not flow as expected. This can impede the postsynaptic spike to generate, causing error to various neuromorphic application. We address this issue and suggest self-rectifying RRAM as a solution. Fabricated RRAM synaptic device and its measurement data are demonstrated. To evaluate the synaptic device performance of proposed RRAM, hardware based SNN simulation is conducted within simple MNIST pattern recognition.

1.1. Integrate and Fire Neuron Circuit

Integrate-and-fire neurons are one of the simplest models for describing biological neuron behaviors, which integrate input signals on membrane capacitors and generate action potentials when the membrane voltage reaches a certain level. Connecting multiple integrate-and-fire neurons results in spiking neural networks (SNNs), which are intelligent systems capable of performing tasks such as pattern recognition [23, 24].

Various neuron circuits were presented to emulate integrate-and-fire model

and neural learning algorithms on circuits [25]. Such circuits focused on integration and action potential generation. When an integrate-and-fire circuit receives presynaptic spikes, current is injected to membrane capacitor, and the amount of which depends on state of the synaptic device. Simple illustration of integrate-and-fire neuron circuit and its operation is presented in Figure.1.

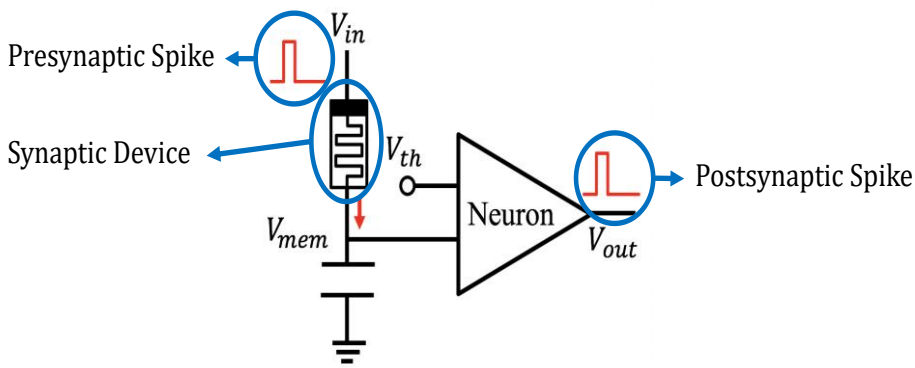

Figure 1. Illustration of integrate-and-fire neuron circuit

Integrate-and fire neuron circuits and synaptic devices compose neuromorphic systems. Each synaptic device connects two spiking neuron circuits those referred to as presynaptic neuron circuit and postsynaptic neuron circuit. Presynaptic neuron circuit transmits spike while postsynaptic neuron circuit receives the spike. Even for the same presynaptic spike, the amount of current received by postsynaptic neuron may differ depending on the state of the synaptic device. This

factor which determines such amount of current for single presynaptic spike is relatively known as synaptic weight. When current flow through the synaptic device, membrane capacitor is charged accordingly. If the amount of current is large enough, V_{mem} exceeds the threshold voltage of the postsynaptic neuron evoking the postsynaptic neuron to generate the postsynaptic spike.

1.2. Resistive Random Access Memory

Resistive random access memory (RRAM) has been broadly investigated as a leading candidate for next generation nonvolatile memory [26]. RRAM has also been drawing attentions as a synaptic device in neuromorphic system [27-32] due to its advantageous features such as simple structure, low cost, high integration density [33], fast operation [34, 35, 36], gradual switching [37], and CMOS compatibility [38].

Since neuromorphic system requires a number of synapses, high density RRAM array is highly recommended. For high density RRAM implementation, many array structures have been proposed. Figure 2 shows schematic of

representative 3D RRAM arrays.

To construct a neuro-inspired non-von Neumann computing architecture, 3D array structure with adjustable nonvolatile memory cells is key factor. Especially, cross-point RRAM is suitable for neuromorphic system thanks to its structure. This is because the input vector and the conductivity matrix, which is one of the most crucial part of machine learning algorithms, can be carried out naturally if the synaptic elements that can control the electrical conductivity are located between two crossing lines.

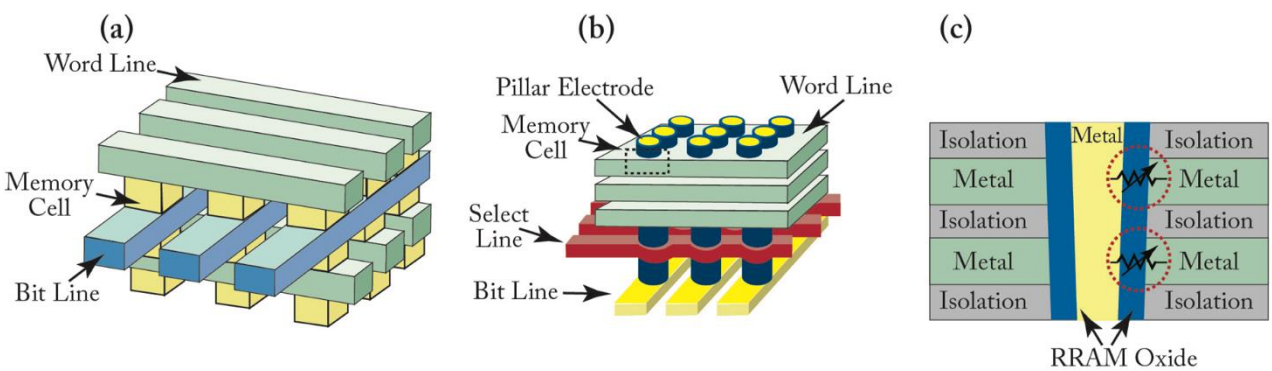

Figure 2. Schematic of (a) simply stacked 3D horizontal RRAM array; (b)D vertical RRAM array; (c) the cross-section of (b) by cutting through one pillar electrode[39].

Many researchers have been focusing on RRAM as one of candidates for such synaptic element. Number of studies which apply RRAM to neuromorphic system has been increased, while application to high density memory field has decreased every year (IEDM, 2014-2016). In addition, it has been reported that RRAM took over the proportion among other Flash-based devices and phase change memory (PCM) for the type of synaptic devices employed in the hardware implementation of the artificial neural network (IEDM, VLSI 2018).

As demonstrated so far, RRAM has become a point of interest to many researchers as synaptic device for neuromorphic system. Integration of RRAM as synaptic device with neuron circuit will be addressed in the next chapter.

Chapter 2

Reverse leakage current in neuron circuit

In this chapter, we present reverse leakage current problem which occurs in hardware based SNN when RRAM is utilized as synaptic device. For specification, the problem is sequentially described based on the integrate-and-fire neuron circuit. Furthermore, comparison with one of the established issues RRAM possess (sneak path) will be described.

2.1 Reverse Leakage Current

Although RRAM has been a renowned synaptic device for their great advantages, it also has suffered from few challenges. When RRAM is integrated in a circuit, it is a bidirectional passive component. This indicates current direction through RRAM depends on voltage difference. For this small reason, serious problem can arise in RRAM array.

Cross-point RRAM array has a well-known problem originated from above characteristics: sneak path problem [39]. During both write and read

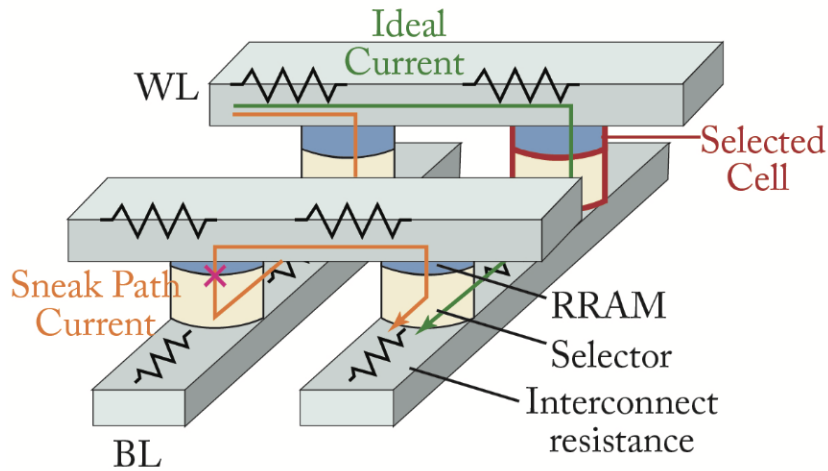

Figure 3. Schematic of the sneak path problem in the cross-point RRAM array. Figure adopted from [39].

operation, leakage current form sneak path through unselected cells. Since IR drop exists in the wire, 0 voltage is not guaranteed which leads to leakage paths. In terms of the write operation, unselected cells can be programmed without intention. Read operation can also malfunction from the sneak path problem. The cell to be read out can be HRS which is surrounded by LRS cells. In this case, the sneak path can flow through the surrounding cells in the LRS and summed with read-out current causing the output current bigger than it should be. In order to suppress the sneak path, many researchers conducted various approaches such as selector or diode.

However, sneak path problem is not the only problem RRAM suffers.

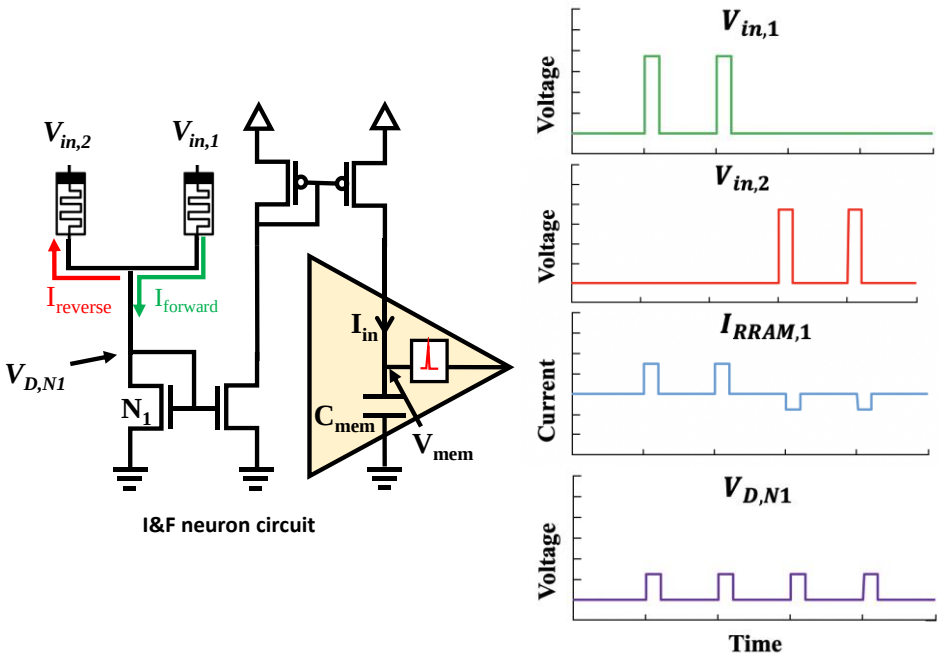

Figure 4. Reverse leakage current problem in spiking neural network

When RRAM is integrated as synapse in hardware based neural network, reverse leakage occurs in neurons where membrane voltage is larger than zero and not receiving spikes from presynaptic neurons as shown in Figure 4. This provokes error to membrane capacitor charge integration, impeding the successful operation of neuromorphic application. In this thesis, the specific situation will be named 'reverse leakage current problem'.

When $V_{in,1}$ is high, $I_{forward}$ flows through the RRAM synapse delivered by two current mirrors as depicted in Figure 4. Delivered current charges the membrane capacitor increasing V_{mem}. If this circuit function appropriately, V_{mem}

would increase according to the synapse current and generate postsynaptic spike. However, problem occurs when $V_{in,1}$ becomes low and $V_{in,2}$ becomes high. In this case, $I_{forward}$ also flows through the RRAM synapse to N_1, increasing the drain current of the NMOS. From this operation, gate voltage of N_1 increases accordingly thereby increasing the node voltage of $V_{D,N1}$. Since $V_{D,N1}$ becomes bigger than $V_{in,1}$, reverse leakage current occurs from $V_{D,N1}$ to $V_{in,1}$. On account of this event, I_{in} current delivered by current mirror would be smaller than it should be. This leads to postsynaptic spike generation failure, consequently provoking malfunction in SNN. Therefore, to properly function in SNN, RRAM should be integrated with a diode which can offer rectifying characteristics.

Chapter 3

Self-rectifying RRAM

In the previous chapter, we discussed the solemnity of reverse leakage current problem. It is evident that this problem will be solved with an additional diode integration. However, integration of additional device with RRAM would weaken one of the biggest advantages of RRAM, which is small size. Therefore, RRAM with self-rectifying characteristics will be beneficial for both size and suppression of reverse leakage current. In this chapter, introduction of self-rectifying RRAM and its DC characteristics will be analyzed.

3.1. Self-rectifying RRAM

In Ni/W/SiN_x/n-Si RRAM, we can take advantage of its metal-insulator-silicon (MIS) structure. After the forming process of SiN_x switching layer, SiN_x no longer serve as an insulator only offering conductive path for the switching process. Consequently, it becomes a metal-silicon (MS) contact indicating the presence of Schottky contact. This Schottky contact can be utilized to construct

RRAM with self-rectifying characteristics. Since rectification effect by Schottky diode will vary with BE doping concentration, three types of RRAM with different BE doping concentration was chosen in this experiment.

The proposed Ni/W/SiN_x/n-Si RRAM devices were fabricated by the following process flow. RRAM fabrication was done upon n-type Si (100) substrate. Screen oxide was thermally grown and ion implantation was conducted to form BE. In order to observe doping concentration dependency, n-type dopant was used in three different doses: type A (5×10^{12} cm^{-2}), type B ($5\times10^{14}$$cm^{-2}$) and type C ($5\times10^{15}$ cm^{-2}) with 40 keV energy. BE doping concentration of each samples are analyzed by secondary ion mass spectrometry (SIMS). After the BE formation, screen oxide was removed and 8 nm thick SiN_x switching layer was deposited by plasma enhanced chemical vapor deposition (PECVD) using SiH_4 and NH_3 gas reactant at 300°C. Tungsten TE was deposited with sputtering system while the samples were covered with shadow mask resulting circular TE pattern with 100μm diameter. Finally, nickel was deposited with thermal evaporator system to prevent TE oxidation followed by the removal of the shadow mask. The

energy-dispersive X-ray spectroscopy (EDS) was conducted for depth profile of Ni/W/SiN_x/n-Si device, containing information on atomic percentage of each element depending on the depth. All of the measurements were conducted using Keithley 4200-SCS semiconductor parameter analyzer (SPA). Control bias were applied to Ni electrode while n-Si BE were grounded during the measurements.

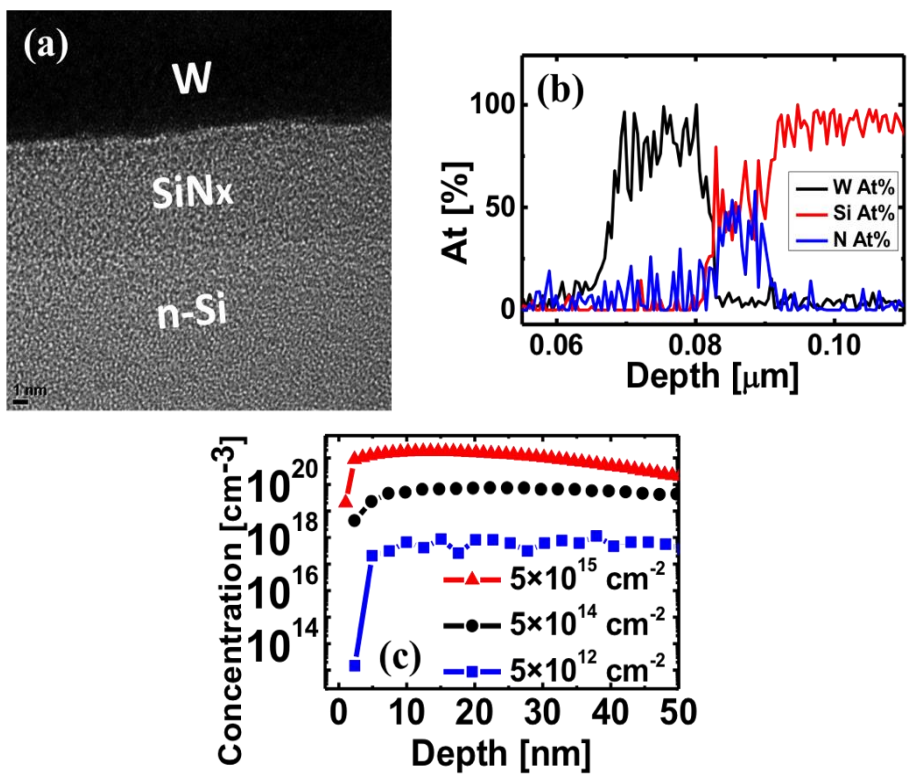

Figure 5. (a) TEM image of fabricated Ni/W/SiNx/n-Si RRAM device; (b) EDS line scan from TE to BE of self-rectifying RRAM device; (c) Doping concentration profile of 3 device with different implantation dose

Figure 5 (a) shows transmission electron microscopy (TEM) image of fabricated device. From this image, thickness and amorphous state of SiN_x can be observed. One can observe from EDS data in Figure 5 (b) that the SiN_x layer is formed Si-rich, which is advantageous for RRAM switching characteristics [31]. According to the SIMS analysis results illustrated in Figure 5 (c), doping concentrations of the Si BEs each have been well controlled by the dose.

3.2. Measurement and Analysis

Figure 6 shows DC current - voltage (*I*-*V*) characteristics of RRAM devices with different BE doping concentration. Compliance current was applied to avoid the permanent breakdown and to control appropriate switching characteristics of each device. Owing to the Schottky diode between TE metal and BE Si, highest rectification ratio was obtained in the device with lowest doping concentration BE (See Figure 6 (a)). As shown in Figure 6 (b), when doping concentration was higher than that of type A, rectifying characteristics were seen but not significantly. On the other hand, type C showed hardly any rectifying

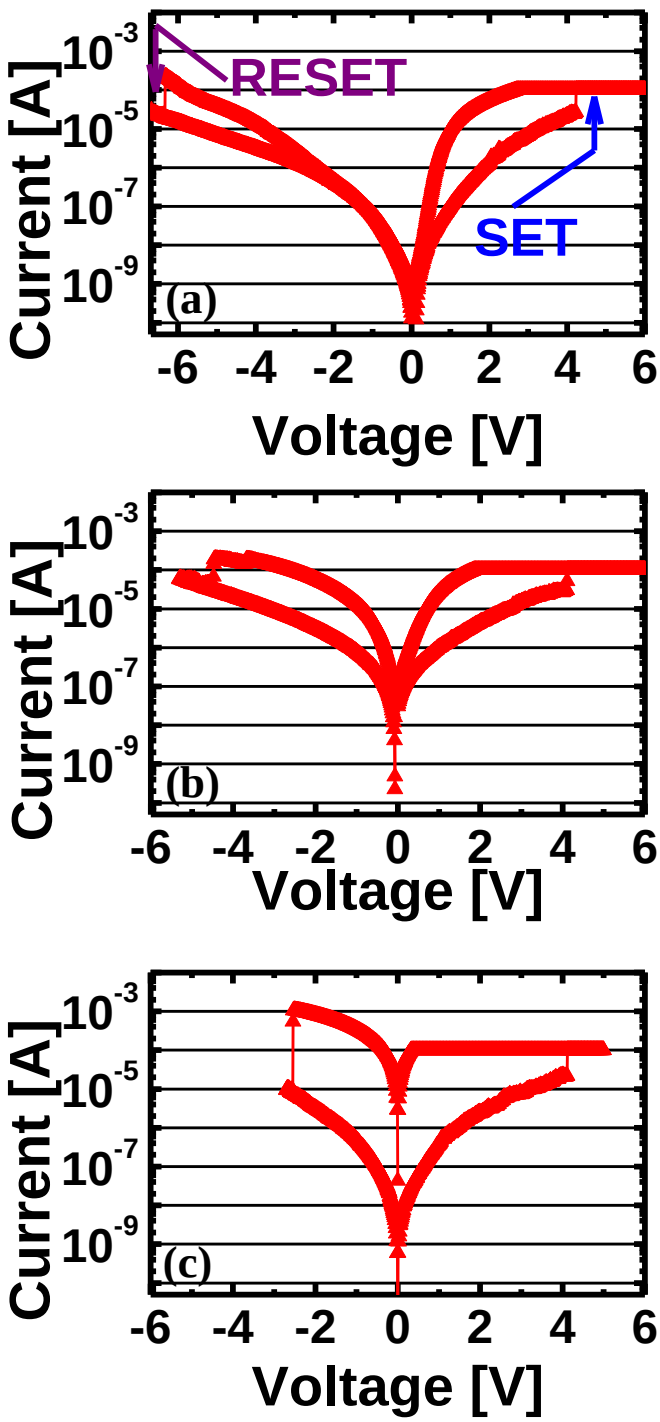

Figure 6. I-V characteristics by DC sweep measurement of fabricated (a) 5×10^{12} (b) 5×10^{14} (c) 5×10^{15} cm^{-2} dose RRAM. Among three devices, (a) has the highest rectification effect dominated by diode.

characteristics. Current at negative bias was significantly suppressed in type A than type B and C as depicted in Figure 6 (a). The low resistance state (LRS) current of type C drops sharply in low voltage region in Figure 6 (c), while that of type A drops more gradually (Figure 6 (a)).

Based on the DC sweep measurement data, the reverse bias characteristics were further examined and reset mechanism of the devices were analyzed. Figure 7 (a) shows scatter plot including reset current vs. reset voltage graph for the three devices. Here, reset current is defined as the current from reset point. As one can notice from the plot, reset power (reset voltage × reset current) is close to constant regardless of BE doping concentration. For mathematical analysis, linear fitting of the three clusters was done and plotted in Figure 7 (a). The slope of the fitted result is −1.1 indicating that the reset operation occurs from the same power. This provides evidence that all fabricated Ni/W/SiN_X/n-Si devices follow the reset switching mechanisms of Joule heating [32]. The set switching process can be explained by trap generation in SiN_X layer. When set voltage is applied to the TE, high electric field can accelerate the electrons breaking down the lattice structure. From this, dangling bond can be created and they serve as traps composing

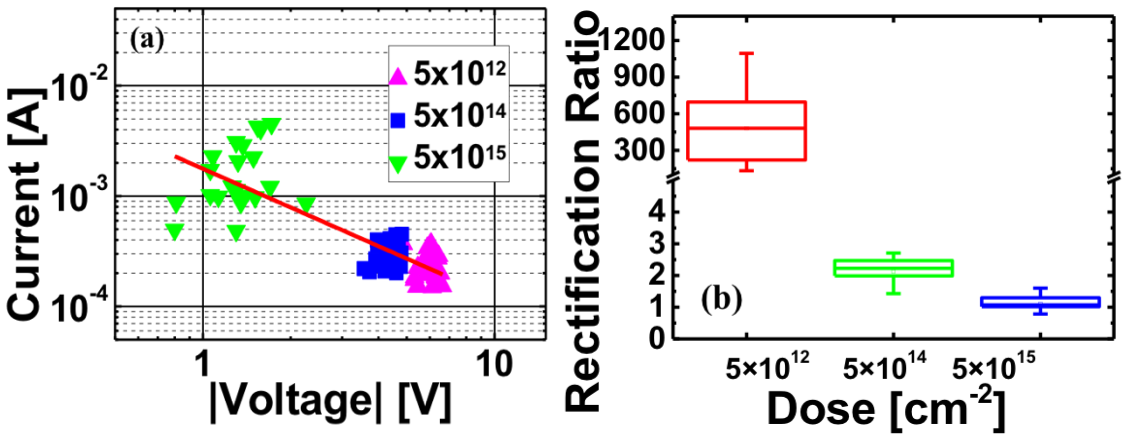

Figure 7. (a) Reset voltage vs reset current graph of type A (5×10^{12} cm^{-2}) and linear fit slope indicating Joule heating reset mechanism; (b) Statistical box graph of rectification ratio based on measurement data

conducting path [33]. Figure 7(b) depicts numerical rectification ratio based on the DC measurement data. Here, rectification ratio is defined as positive voltage LRS current divided by negative voltage LRS current. RR in type A and B was extracted from 1V, whereas RR of type C was extracted from 0.3V because of the limitation by compliance current. RRAM with lowest BE doping concentration device had maximum 3 orders of rectification ratio surpassing other devices with higher BE doping concentration. Type A with high RR also showed good retention even after extensive amount of time exposed in 125°C (Figure 8 (a)).

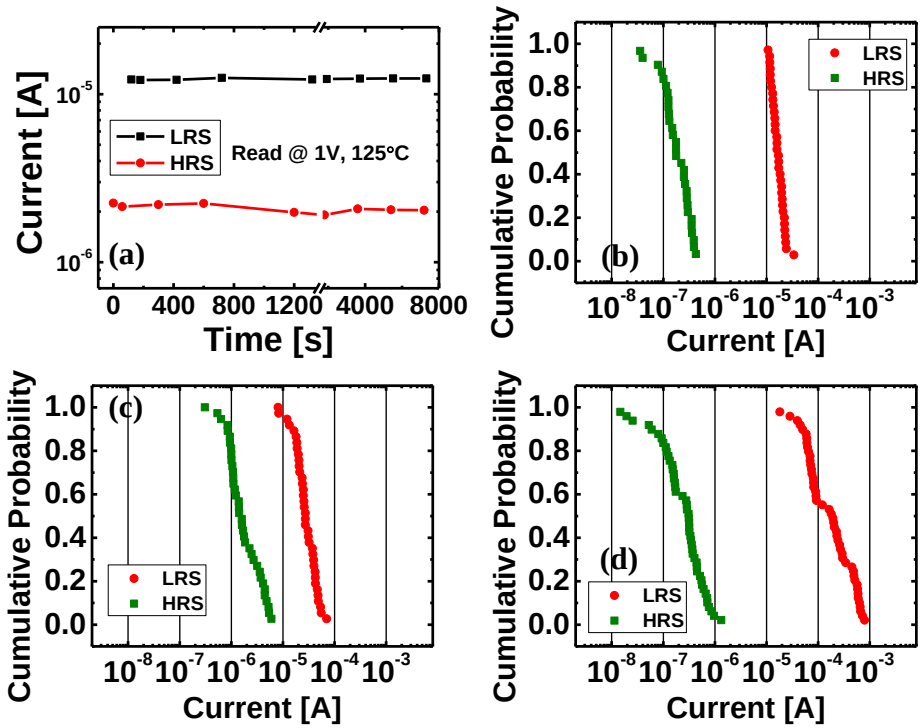

Figure 8. (a) Reset voltage vs reset current graph of type A (5×10^{12} cm^{-2}) and linear fit slope indicating Joule heating reset mechanism; (b) Statistical box graph of rectification ratio based on measurement data

Figures 8(b)-(d) show the cumulative probability distribution of LRS and HRS current measured from three types of devices. The memory window between LRS and HRS current in type A is high enough (>10^2) to use as synapse in neural network compared to other two devices. Also, the LRS and HRS current of type A had less variability than other devices. Based on the previously mentioned properties, the sample which has the lowest BE doping concentration (type A) is the most suitable self-rectifying RRAM synapse as a solution for SNN reverse leakage current problem.

Chapter 4

Hardware-Based System Level Simulation

In this chapter, we evaluate the contribution of self-rectifying RRAM to the system by conducting hardware-based system level simulation. MNIST pattern recognition simulation was conducted utilizing the measurement data of fabricated RRAM.

4.1. System Level Evaluation of Self-Rectifying RRAM

Since self-rectifying RRAM with 5×10^{12} cm^{-2} BE concentration (type A) has highest rectification ratio, it is expected to effectively suppress reverse leakage current. However, it is not clear how much this suppressed reverse leakage current effect the system. Therefore, we conducted system level evaluation based on measurement data shown in the previous chapter.

For the evaluation, MNIST pattern recognition test with hardware based SNN was conducted. Figure 6 shows the model of neural network employed in this simulation. Single layer, binary weight neural network within 784 inputs and 10 outputs was employed in this model. Since the MNIST data sets have 784 pixels (28×28) and 10 labels (0 to 9), the number of inputs and outputs were also set by 784 and 10.

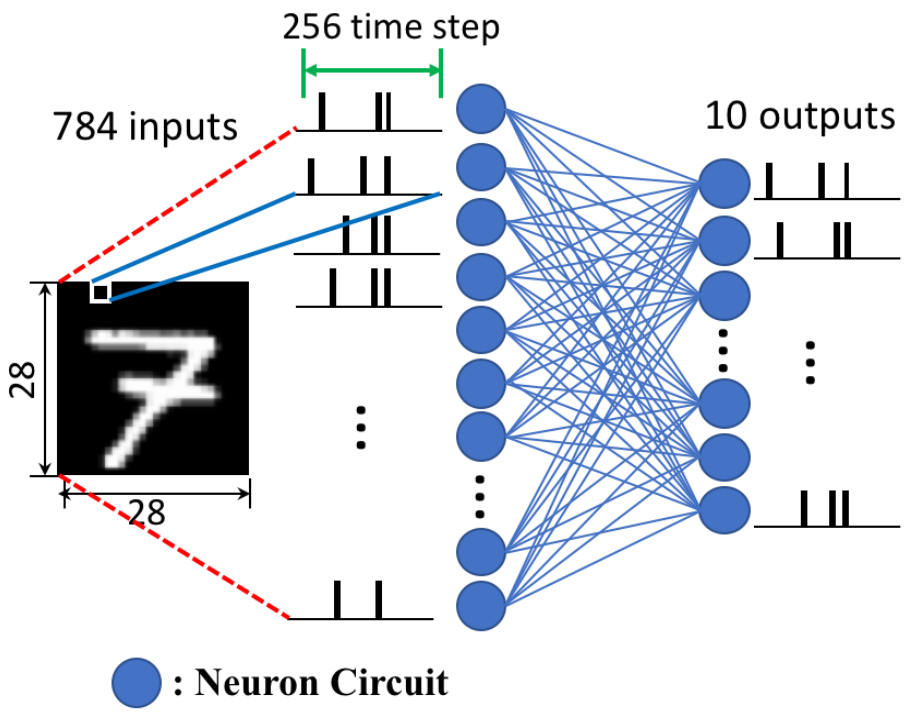

Figure 5. Hardware-based neural network system configuration

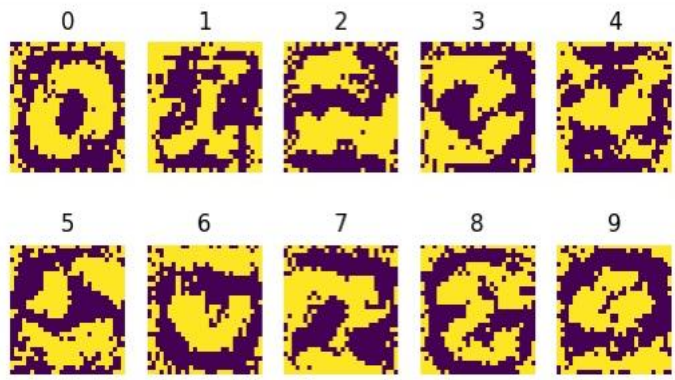

Figure 10. Binarized weight map after neural network training

As depicted in Figure 9, 7840 number of weights were first trained by gradient descent method with continuous weight values. Then the weights were binarized in to 0 and 1 by setting the proportion of each weight becomes 50:50 as shown in Figure 10. In the inference step, weights were assigned according to this binarized weight map. From this very same model, inference accuracy of non-SNN was 82.90%.

For the inference, input datasets were transformed into 256 timesteps per pixel. Since each of the pixels have values from 0 to 255, each timesteps were encoded to generate a spike by the probability proportional to the pixel values. Figure 11 illustrates the circuit diagram of multiple RRAM synapse connected to one postsynaptic IF neuron circuit. As each timestep passes by, V_{high} or V_{low} is applied to the top electrode of RRAM synapse. Then the synaptic current flowing through RRAM is determined by the voltage difference of input voltage and $V_{D,N1}$. For the realistic simulation, this synaptic current was adopted from the

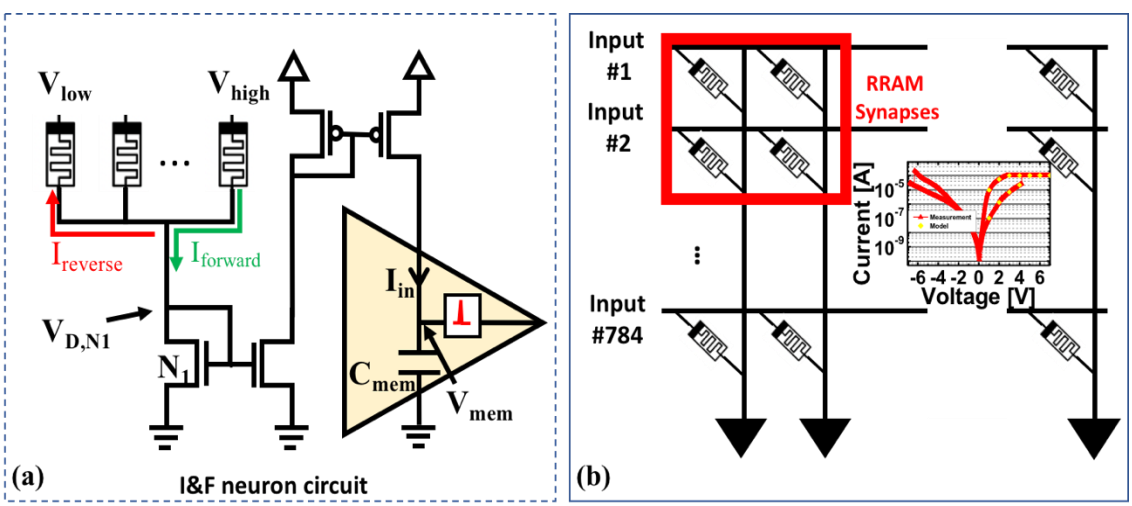

Figure 11. Circuit diagram of multiple RRAM synapses connected to one postsynaptic IF neuron circuit through current mirror. Reverse leakage was considered in this circuit. (b) Schematic of hardware-based system level simulation of binary-weight SNN employing the proposed self-rectifying RRAM synapses.

measurement data of three types of RRAM.

First, $V_{D,N1}$ was enumerated by solving Kirchoff's current law (KCL). Then by the voltage difference between input voltage and $V_{D,N1}$, current was adopted from the measurement data. From the binarized weight map in Figure 10, HRS current or LRS current was adopted when the weight was 0 or 1 respectively. After this process, current sum of 724 RRAM synapse was calculated (I_{in}). From I_{in} and C_{mem}, V_{mem} was calculated and compared with V_{th}. If V_{mem} is bigger than V_{th}, postsynaptic spike is generated.

4.2. Simulation Results

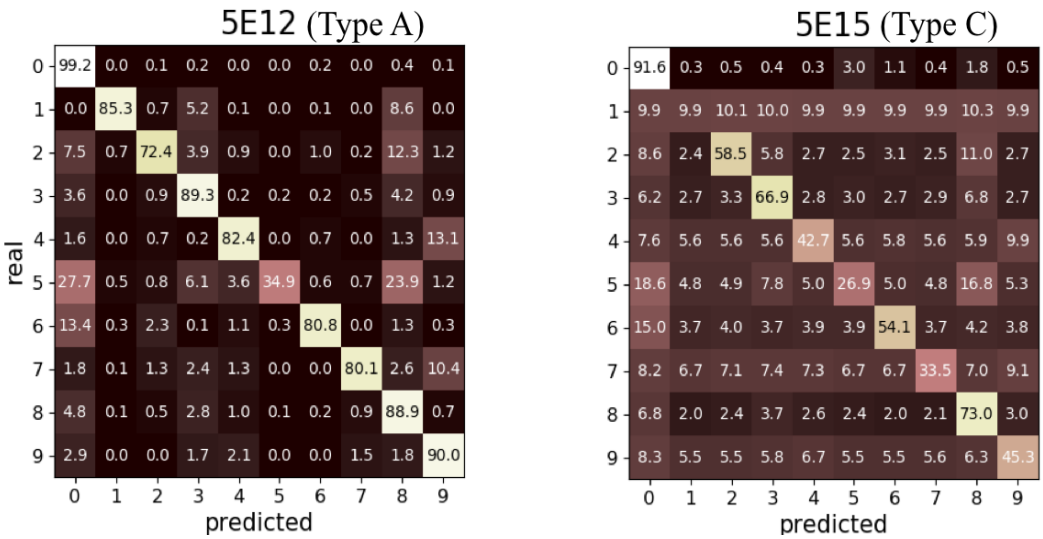

Figure 12. Confusion matrix of type A and C of the hardware-based SNN simulation results

TABLE I. MNIST classification accuracy result of hardware-based binary-weight SNN simulation

Synapse	Rectification Ratio	Accuracy [%]
Ideal	-	82.90
Type A	460 (high)	82.84
Type B	2.1	76.61
Type C	1.03 (low)	72.65

Figure 12 shows the confusion matrix illustrated by the simulation results. Y-axis represents the real label of the datasets, and X-axis represents the predicted label. High accuracy is achieved when sum of the diagonal values in the confusion matrix is big. As depicted in Figure 12, sum of the diagonal values was

bigger when type A synapse was used in the simulation. Furthermore, one can observe that label “1” accuracy is particularly small when type C synapse was employed. This result originates from the fact that MNIST pattern "1" contains larger number of dark pixels compared to other patterns, making the system more vulnerable to reverse leakage problem. Table I shows inference accuracy of each type of devices. While type A synapse with high rectification ratio shows only 0.06%p drop from ideal synapse accuracy, type C shows 10.25%p drop. Additional simulation was set up by considering the variability of type A and type C according to the measurement data depicted in Figure 8. For type A, the average accuracy was 75.3%, and its standard deviation was 1.58%p, while type C had 59.2% average accuracy and 2.66%p standard deviation. Even when the variability is taken into account, since type A has superior uniformity than that of type C, accuracy drop was considerably low. Above simulation results indicate that rectification characteristics of RRAM successfully suppressed reverse leakage current problem thereby increasing inference accuracy. Furthermore, this results also emphasize the severity of reverse leakage current problem in spiking neural network.

Chapter 5

Conclusions

In summary, we proposed self-rectifying RRAM synapse to solve reverse leakage current problem that arises when RRAM device is integrated with IF circuit as synapse in SNN. We investigated that Ni/W/SiN_x/n-Si RRAM with 5×10^{12} BE dose exhibited highest rectification ratio with built-in Schottky diode. We verified that the proposed device alleviates reverse leakage current problem by conducting hardware based SNN simulation for MNIST classification. Classification accuracy was improved by 10.19%p when self-rectifying RRAM was employed compared to non-rectifying RRAM case. As a result, proposed self-rectifying RRAM not only possess potential as synaptic device for hardware SNN but is also an expected candidate for bringing various promising results in neuromorphic system application.

References

[1] C. Mead, “Neuromorphic electronic systems,*” Proc. IEEE,* vol. 78, no. 10, pp.1629 - 1636, Oct. 1990.

[2] L. Gao, P. -Y. Chen, and S. Yu, “NbOx based oscillation neuron for neuromorphic computing,” *Appl. Phys. Lett.*, vol. 111, no.10, pp. 103503, Sep. 2017.

[3] H. Kim, S. Hwang, J. Park, and B. -G. Park, “Silicon synaptic transistor for hardware-based spiking neural network and neuromorphic system,” *Nanotechnology,* vol. 28, no. 40, pp. 405202, Oct. 2017.

[4] O. Peter, and M. Welling, “Deep spiking networks,” *arXiv preparing, arXiv: 1602.088323,* 2013.

[5] D. S. Jeong, K. M. Kim, S. Kim, B. J. Choi, and C. S. Hwang, “Memristors for Energy-Efficient New Computing Paradigms,” *Adv. Electron. Mater.*, vol. 2, no. 9, pp. 1600090, Aug. 2016.

[6] P. A. Merolla, J. V. Arthur, R. Alvares-Icaza, A. S. Cassidy, J. Sawada, F. Akopyan, B. L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Breszzo, I. Vo, S. K. Esser, R. Appuswamy, B. Taba, A. Amir, M. D. Flickner, W. P. Risk, R. Manohar, and D. S. Modha, “Artificial brains. A million spiking-neuron integrated circuit with a scalable communication network and interface,” *Science,* vol. 345, no. 6197, pp. 668 -673, Aug. 2014.

[7] A. -D. Almási, S. Wo´zniak, V. Cristea, Y. Leblebici, and T. Engbersen, “Review of advances in neural networks,” *Neurocomputing,* vol. 174, pp. 31 - 41, Jan. 2016.

[8] T. Kim, Y. S. Song, and B. -G. Park, “Overflow Handling Integrate-and-Fire Silicon-on-Insulator Neuron Circuit Incorporating a Schmitt Trigger Implemented by Back-Gate Effect,” *J. Nanosci. Nanotechnol.*, vol. 19, no. 10, pp. 6183-6186, Oct. 2019.

[9] S. M. Bohte, J. N. H. La Poutre, “Error-backpropagation in temporally encoded networks of spiking neurons,” *Neurocomputing*, vol.48, pp. 17-37, 2002.

[10] R. V. Rullen, and S.J. Thorpe, “Rate coding versus temporal order coding: what the retinal ganglion cells tell the visual cortex,” *Neural Comput.*, vol. 13, pp. 1255-1283, 2001.

[11] P. U. Diehl, D. Neil, J. Binas, M. Cook, S. –C. Liu, and M. Pfeiffer, “Fast-classifying, high-accuracy spiking deep networks through weight and threshold balancing,” *International Joint Conference on Neural Networks (IJCNN)*, 2015.

[12] X. Guo, F. M. Bayat, M. Bavandpour, M. Klachko, M. R. Mahmoodi, M. Prezioso, K. K. Likharev, and D. B. Strukov, “Fast, energy-efficient, robust, and reproducible mixed-signal neuromorphic classifier based on embedded NOR flash memory *technology,” IEEE International Electron Devices Meeting (IEDM)*, 2017.

[13] S. Mitra, S. Fusi, and G. Indiveri, “Real-time classification of complex patterns using spike-based learning in neuromorphic VLSI,” *IEEE Trans. Biomed. Circuits Syst*., vol. 3, no. 1 pp. 32-42, 2009.

[14] M. W. Kwon, S. Kim, M. H. Kim, J. Park, H. Kim, S. Hwang, and B. -G. Park, “Integrate-and-Fire (I&F) Neuron Circuit Using Resistive-Switching Random Access Memory (RRAM),” *J. Nanosci. Nanotechnol*., vol. 17, no. 5, pp. 3038-3041, May 2017.

[15] S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, and H. -S. P. Wong, “An Electronic Synapse Device Based on Metal Oxide Resistive Switching Memory for Neuromorphic Computation,” *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2729 - 2737, Aug. 2011.

[16] S. Ambrogio, S. Balatti, V. Milo, R. Carboni, Z. -Q. Wang, A. Calderoni, N. Ramaswamy, and D. Ielmini, “Neuromorphic Learning and Recognition With One-Transistor-One-Resistor Synapses and Bistable Metal Oxide RRAM,” *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1508 - 1515, April 2016.

[17] S. Kim, S. Jung, M. –H. Kim, S. Cho, and B. –G. Park, “Resistive switching characteristics of Si3N4-based resistive-switching random-access memory cell with tunnel barrier for high density integration and low-power applications,” *Appl. Phys. Lett.,* vol. 106, no. 21, pp. 212106, May 2015.

[18] R. Waser, and M. Aono, “Nanoionics-based resistive switching memories,” *Nat. Mat.,* vol. 6, pp. 833 - 840, Nov. 2007.

[19] Y. –F. Chang, P. –Y. Chen, B. Fowler, Y. –T. Chen, F. Xue, Y. Wang, F. Zhou, and J. C. Lee, “Understanding the resistive switching characteristics and mechanism in active SiOx-based resistive switching memory,” *J. Appl. Phys*., vol. 112, no.12, pp. 123702, Dec. 2012.

[20] M. –J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y. –B. Kim, C. –J. Kim, D. H. Seo, S. Seo, U. –I. Chung, I. –K. Yoo, and K. Kim, “A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta2O(5-x)/TaO(2-x) bilayer structures,” *Nat. Mat.,* vol. 10, no. 8, pp. 625-630, Jul. 2011.

[21] A. Sawa, “Resistive switching in transition metal oxides,” *Mater. Today,* vol. 11, no. 6, pp. 28 - 36, Jun. 2008.

[22] H. S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, and M.-J. Tsai, “Metal-oxide RRAM,” *Proc. IEEE,* vol. 100, no. 6, pp. 1951 - 1970, Jun. 2012.

[23] H. Kim, S. Hwang, J. Park, and B. –G. Park, “Silicon synaptic transistor for hardware-based spiking neural network and neuromorphic system,” *Nanotechnology*, vol. 28, no. 40, p. 405202, 2017.

[24] D. Marti, M. Rigotti, M. Seok, and S. Fusi, “Energy-efficient neuromorphic classifiers,” *Neural Comput.*, vol. 28, no. 10, pp. 2011-2044, 2016.

[25] G. indiveri, B. Linares-Barranco, T. J. Hamilton, A. Van Schaik, R. Etienne-cummings, T. Delbruck, S. –C. Liu, P. Dudek, P. Haflinger, and S. Renaud, “Neuromorphic silicon neuron circuits,” *Front. Neurosci.,* vol. 5, p. 73, 2011.

[26] R. Waser and M. Aono, “Nanoionics–based resistive switching memories,” *Nature Mater.*, vol. 6, no. 11, pp. 833-840, 2007.

[27] S. H. Jo, T.Chang, I. Ebong, B. B. Bhadviya, P. Mazumder and W. Lu, “Nanoscale Memristor Device as Synapse in Neuromorphic Systems,” *Nano Lett.*, vol. 10, no. 4, pp. 1297-1301, Mar.2010.

[28] T. Chang, S. –H. Jo, and W. Lu, “Short-Term Memory to Long-Term Memory Transition in a Nanoscale Memristor,” *ACS Nano*, vol. 5, no. 9, pp. 7669-7676, Aug. 2011.

[29] S. B. Eryilmaz, D. Kuzum, S. Yu, and H. –S. P. Wong, “Device and System Level Design Considerations for Analog –Non-Volatile-Memory Based Neuromorphic Architectures,*” IEEE IEDM Tech. Dig.,* Dec. 2015, pp.5.1.1-4.1.4.

[30] G. W. Burr, P. Naratanan, R. M. Shelby, S. Sidler, I. Boybat, C. di Nolfo and Y. Leblebici, “Large-scale neural networks implemented with non-voltatile memory as the synaptic weight element: comparative performance analysis (accuracy, speed, and power),” *IEEE IEDM Tech. Dig.*, Dec. 2015, pp. 4.4.1-4.4.4.

[31] S. Yu, P. –Y. Chen, Y. Cao, L. Xia, Y. Wang and H. Wu, “Scaling-up Resistive Synaptic Arrays for Neuro-inspired Architecture: Challenges and Prospect,” *IEEE IEDM Tech. Dig.*, Dec. 2015, pp. 17.3.1-17.3.4.

[32] M. Prezioso, I. Kataeva, F. Merrikh-Bayat, B. Hoskins, G. Adam, T. Sota, K. Likharev and D. Strukov, “Modeling and Implementation of Firing-Rate Neuromorphic-Network Classifiers with Bilayer Pt/Al_2O_3/TiO_{2-x}/Pt Memristors,” *IEEE IEDM Tech. Dig.*, Dec. 2015, pp.17.4.1-17.4.4.

[33] S. H. Jo, K. –H. Kim and W. Lu, “High-Density Crossbar Arrays Based on a Si Memristive System,” *Nano Lett.*, vol. 9, no. 2, pp. 870-874, Jan.2009.

[34] H. Y. Lee et al., “Evidence and solution of Over-RESET Problem for HfO_x Based Resistive Memory with Sub-ns Switching Speed and High Endurance,” *IEEE IEDM Tech. Dig.*, Dec. 2010, pp. 460-463.

[35] A. C. Torrezan, J. P. Strachan, G. Medeiros-Ribeiro and R S. Williams, “Sub-nanosecond switching of a tantalum oxide memristor,”

Nanotechnology, vol. 22, no. 48, pp. 485203-1-485203-7, Nov. 2011.

[36] M. –J. Lee et al., "Electrical Manipulation of Nanofilaments in Transition-Metal Oxides for Resistance-Based Memory," *Nano. Lett*, vol.9, no. 4, pp. 1476-1481, Mar. 2009.

[37] S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, and H. -S. P. Wong, "An Electronic Synapse Device Based on Metal Oxide Resistive Switching Memory for Neuromorphic Computation," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2729 - 2737, Aug. 2011.

[38] S. H. Jo and W. Lu, "CMOS Compatible Nanoscale Nonvolatile Resistance Switching Memory," *Nano Lett.*, vol. 8, no. 2, pp. 392-397, Jan. 2008.

[39] S. Yu. (2016). Resistive Random Access Memory (RRAM). Morgan & Claypool Publishers.

초 록

본 논문에서는 저항변화메모리가 시냅스 소자로서 스파이킹 뉴럴 네트워크에 인테그레이트-앤-파이어 뉴런 회로와 집적될 때에 발생하는 역방향 누설 전류 문제에 대해서 제안한다. 또한, 이러한 문제를 해결하기 위해 자가정류기능이 있는 저항변화메모리를 제안 및 제작하였다. 니켈/텅스텐/실리콘나이트라이드/실리콘 의 구조를 가진 자가정류기능의 저항변화메모리를 하부전극의 도핑 농도를 다르게 하여 제작하였고 측정하였다. 측정결과를 바탕으로 소자들의 전압-전류 특성과 정류 특성을 분석한 결과, 제작한 소자들 중 가장 낮은 도핑 농도의 하부전극을 가진 저항변화메모리의 정류비가 가장 큰 것으로 확인하였다. 나아가 제안하는 자가정류기능의 저항변화메모리가 스파이킹 뉴럴 네트워크에 어떤 영향을 미치는지 확인하기 위하여 하드웨어 기반 시스템 레벨 시뮬레이션을 진행하였다. 그 결과, 자기정류기능의 소자를 시냅스로 한 뉴럴 네트워크에서의 MNIST 패턴 인식 시뮬레이션 인식률이 총 10.2%p 증가 하였다. 본 논문에서 제시하는 자가정류 소자는 이후 다양한 뉴로모픽 어플리케이션의 결과를 성공으로 이끌 수 있는 가능성을 지닌다.

주요어 : 저항변화메모리 (RRAM), 시냅스 소자, 뉴로모픽, 자가정류기능, 시스템 레벨 시뮬레이션
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