Ph.D. Dissertation

A Study on low damage etching and gate dielectrics for E-mode AlGaN/GaN-on-Si FETs

AlGaN/GaN 전력소자의 특성 향상을 위한 식각과 절연막에 관한 연구

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Abstract

The Si technology for power devices have already approached its theoretical limitations due to its physical and material properties, despite the considerable efforts such as super junction MOSFET, trench gate, and insulated gate bipolar transistors. To overcome these limitations, many kinds of compound materials such as GaN, GaAs, SiC, Diamond and InP which have larger breakdown voltage and high electron velocity than Si also have been studied as future power devices. GaN has been considered as a breakthrough in power applications due to its high critical electric field, high saturation velocity and high electron mobility compared to Si, GaAs, and SiC. Especially, AlGaN/GaN heterostructure field-effect transistors (HFETs) have been considered as promising candidates for high power and high voltage applications.

However, these AlGaN/GaN heterostructure field-effect transistors with the 2DEG are naturally normally-on, which makes the devices difficult to deplete the channel at zero gate bias. Among the various methods for normally-off operation of GaN devices, gate-recess method is a promising method because it can be easier to implement than other approaches and ensure normally-off operation. However, charge trapping at the interface between gate dielectric and (Al)GaN and in the gate dielectric is a big issue for recessed gate MIS-HEMTs. This problem leads to degradation of channel mobility, on-resistance and on-current of the devices. Especially, V_{th} hysteresis after a positive gate voltage sweep and V_{th} shift under a gate bias stress are important reliability challenges in gate recessed MIS-HEMTs.

The scope of this work is mainly oriented to achieve high quality

interface at dielectric/(Al)GaN MIS by studying low damage etching methods and the ALD process of various dielectric layers.

In the etching study, various etching methods for normally-off operation have been studied. Also, etching damage was evaluated by various methods such as atomic force microscopy (AFM), photoluminescence (PL) measurements, X-ray photoelectron spectroscopy (XPS) measurements and electrical properties of the recessed schottky devices. Among the etching methods, the ALE shows the smoothest etched surface, the highest PL intensity and N/(Al+Ga) ratio of the etched AlGaN surface and the lowest leakage current of the gate recessed schottky devices. It is suggested that the ALE is a promising etching technique for normally-off gate recessed AlGaN/GaN MIS-FETs.

In the study of dielectrics, excellent electrical characteristics and small threshold voltage drift under positive gate bias stress are achieved by employing the SiON interfacial layer. However, considerable threshold voltage drift is observed under the higher positive gate bias stress even at the devices using the SiON interfacial layer. For further improvement of interface and reliability of devices, we develop and optimize an ALD AlN as an interfacial layer to avoid the formation of poor-quality oxide at the dielectric/(Al)GaN interface. We also develop an ALD AlHfON as a bulk layer, which have a high dielectric constant and low leakage current and high breakdown field characteristics. Devices with AlN/AlON/AlHfON layer show smaller I-V hysteresis of ~10 mV than that of devices with AlON/AlHfON layer. The extracted static R_{on} values of devices with AlN/AlON/AlHfON and AlON/AlHfON are 1.35 and 1.69 $m\Omega \cdot cm^2$, respectively. Besides, the effective mobility, D_{it} and threshold voltage instability characteristics are all improved by employing the ALD AlN.

In conclusion, for high performance and improvement of reliability of normally-off AlGaN/GaN MIS-FETs, this thesis presents an etching technique for low damage etching and high-quality gate dielectric layer and suggests that the ALE and ALD AlN/AlON/AlHfON gate dielectric are very promising for the future normally-off AlGaN/GaN MIS-FETs

Keyword : Gallium nitride (GaN), Metal-insulator-semiconductor (MIS), Reliability, Aluminum nitride (AlN), Atomic layer etching (ALE), Aluminum hafnium oxynitride (AlHfON)

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Chapter 1. Introduction

1.1. Background

The silicon technology has been the main stream in the semiconductor industry for many decades because of its several advantages such as fundamentally good electrical properties and low-cost compared to other materials [1-3]. the Si-based devices also have been developed in power applications such as mobile, electric vehicles and home appliances. However, as shown in Fig. 1.1, the Si technology for power devices have already approached its theoretical limitations due to its physical and material properties, despite the considerable efforts such as super junction MOSFET, trench gate, and insulated gate bipolar transistors [4-6]. To overcome these limitations, many kinds of compound materials such as GaN, GaAs, SiC, Diamond and InP which have larger breakdown voltage and high electron velocity than Si also have been studied as future power devices [7-11]. Table 1.1 lists characteristics of various semiconductor materials. Among them, GaN has been considered as a breakthrough in power applications due to its high critical electric field, high saturation velocity and high electron mobility compared to Si, GaAs, and SiC [12].

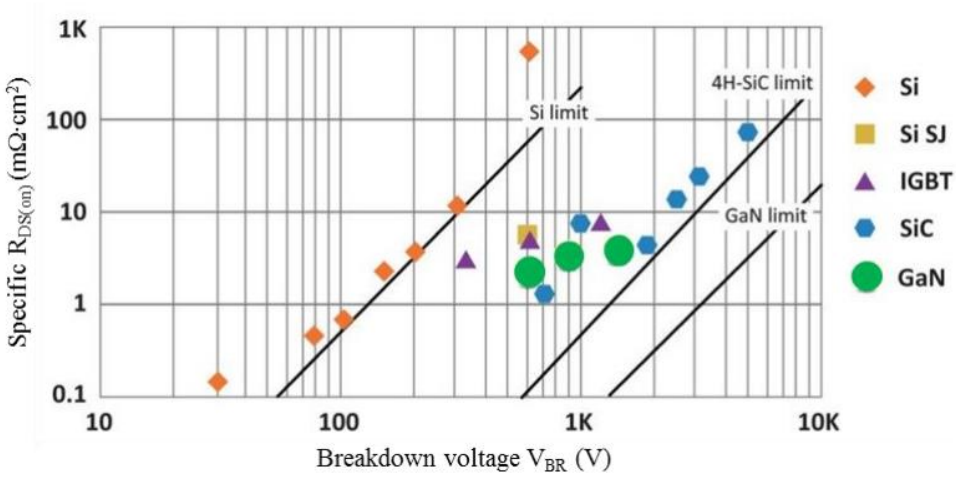


Fig. 1.1 Theoretical limits for Si, SiC and GaN [13].

	Si	GaAs	4H−SiC	GaN	Diamond	InP
Bandgap (eV)	1.1	1.42	3.26	3.39	5.45	1.34
Electron mobility ($cm^2/V \cdot s$)	1350	8500	700	900(Bulk) 2000(2DEG)	1900	5400
Saturation velocity (10^7 cm/s)	1.0	1.0	2.0	2.5	2.7	2.4
Critical field (MV/cm)	0.3	0.4	3.0	3.3	5.6	0.6
Thermal conductivity (W/cm · K)	1.5	0.43	3.7	1.3	20	0.7

Table 1.1 Characteristics of various semiconductor materials

1.2. Normally-off Operation in AlGaN /GaN HFETs

AlGaN/GaN heterostructure field-effect transistors (HFETs) have been considered as promising candidates for high power and high voltage applications. Two-dimensional electron gases (2DEGs) in AlGaN/GaN heterostructure can be achieved without intentionally doping, which contribute to the excellent performance of AlGaN/GaN based HFETs. The most common growth direction of GaN is normal to the [0001] basal plane, where the atoms are arranged in bilayers. These bilayers consist of two closely spaced hexagonal layers, One with cations and the other with anions. The basal surface should be either Ga- or N-faced as shown in Fig. 1.2 [14].

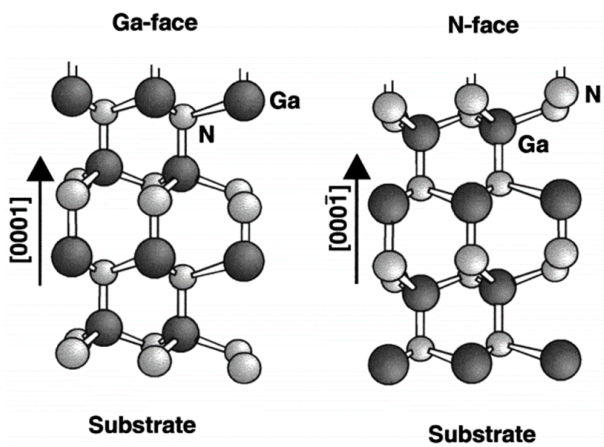


Fig. 1.2 Schematic drawing of the crystal structure of wurtzite Ga-face and N-face GaN [14].

The large electron sheet densities and high mobilities of 2DEGs have been correlated to the spontaneous and piezoelectric polarization. Without external electric fields, the total polarization P of AlGaN or GaN is the sum of the spontaneous polarization and piezoelectric polarization. Each polarization can be defined by

$$\mathbf{P}_{\mathrm{SP}} = P_{SP}\mathbf{z} \ , \ \mathbf{P}_{\mathrm{PE}} = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{\mathrm{C}_{13}}{\mathrm{C}_{33}}\right).$$

α: the lattice constant of the strained layer

α_0: the length of the hexagonal edge

e_{31}, e_{33}: the the piezoelectric coefficients

C_{13}, C_{33}: elastic constants [15, 16]

The spontaneous polarization can cause electric fields up to 3MV/cm in III-N crystals, and strain from AlGaN/GaN grown pseudomorphically cause an additional piezoelectric field of about 2 MV/cm [17].

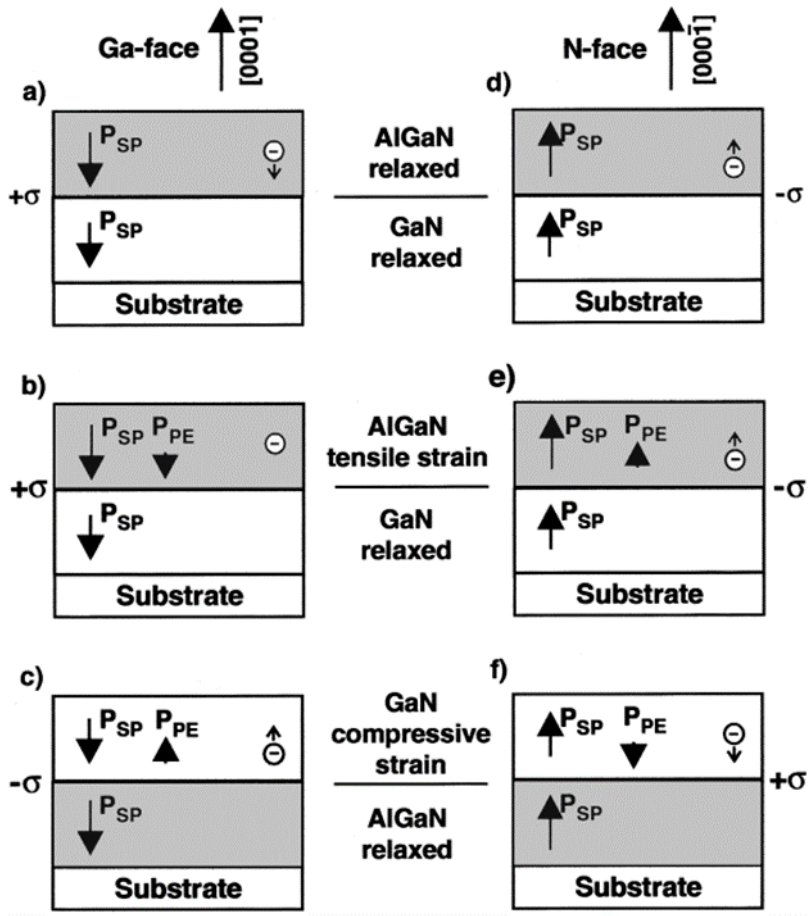


Fig. 1.3 Polarization induced sheet charge density and directions of the spontaneous and piezoelectric polarization in Ga- and N-face strained and relaxed AlGaN/GaN heterostructures [14].

The negative sign of the spontaneous polarization is reported for GaN and the negative piezoelectric polarization and the positive piezoelectric polarization are formed for tensile strained AlGaN and compressive strained AlGaN, respectively. As a result, parallel piezoelectric and spontaneous polarization are formed at tensile strain and antiparallel piezoelectric and

spontaneous polarization exist at compressive strain as shown in Fig. 1.3.

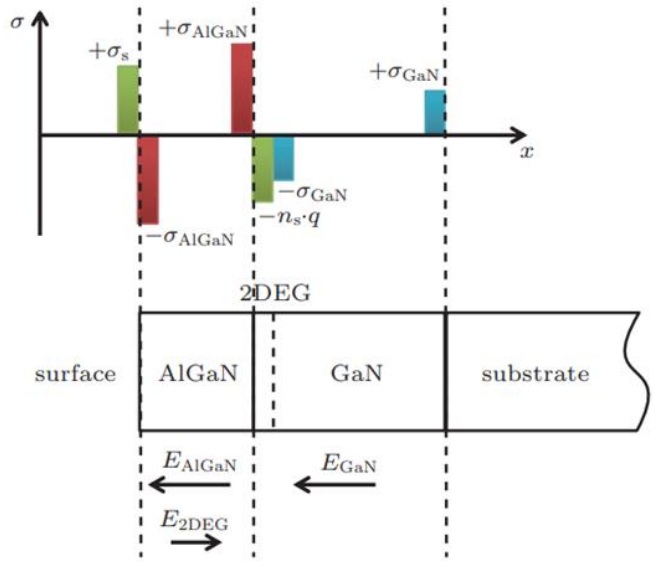


Fig. 1.4 Charge distribution profile of an AlGaN/GaN heterostructure [17]

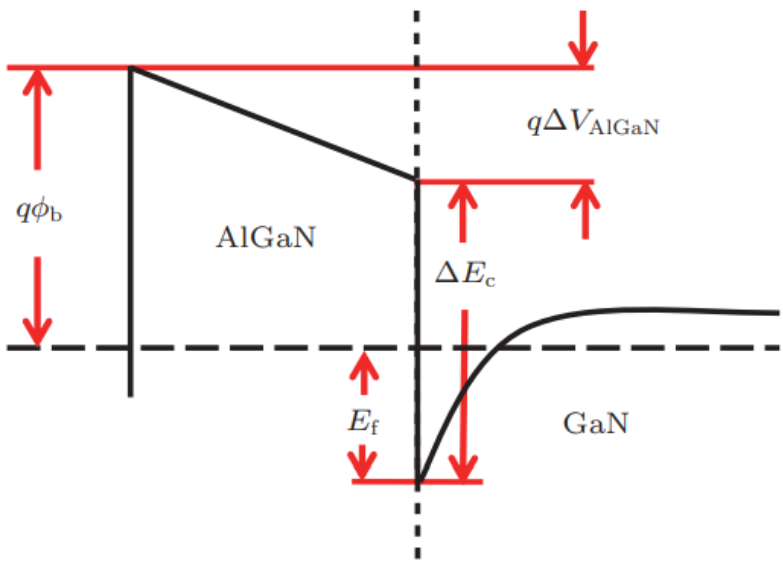


Fig. 1.5 Band diagram of an AlGaN/GaN heterostructure[17]

In the case of pseudomorphic AlGaN/GaN heterostructures with Ga-face polarity and parallel piezoelectric and spontaneous polarization formed at tensile strain, the profile of the charge distributional of an AlGaN/GaN heterostructure can be depicted in Fig. 1.4. σ_{AlGaN} and σ_{GaN} are the polarization charges induced by AlGaN and GaN respectively, and σ_s is the ionized surface charge. The sheet density of 2DEG can be defined as

$$n_s = \frac{\sigma_{AlGaN}}{q} - \frac{\varepsilon}{q^2 d}(q\phi_b + E_f - \Delta E_c).$$

Where φ_b, E_f and ΔE_c are the surface barrier height, the Fermi level position with respect to the GaN conduction-band edge at the AlGaN/GaN interface, and the conduction band discontinuity between GaN and AlGaN, respectively, as seen in Fig. 1.5 [17]. The sheet density of 2DEG can be increased by increasing the Al-content of the AlGaN barrier and the AlGaN barrier thickness on GaN [14, 18].

The 2DEG in AlGaN/GaN heterostructures enables GaN devices to operate in high frequency applications due to the high electron mobility and high saturation electron velocity of the 2DEG. However, these devices with the 2DEG are naturally normally-on, which makes the devices difficult to deplete the channel at zero gate bias. For power applications, normally-off devices offer desirable fail-safe operation conditions and simple circuit and system architecture because normally-off operation allow the elimination of negative-polarity power supply [19, 20]. For normally-off operation of GaN devices, several methods have been reported; recessed gate [19], fluorine treatment [21], cascode configuration [22] and the p-GaN gate [23] as shown in Fig. 1.6.

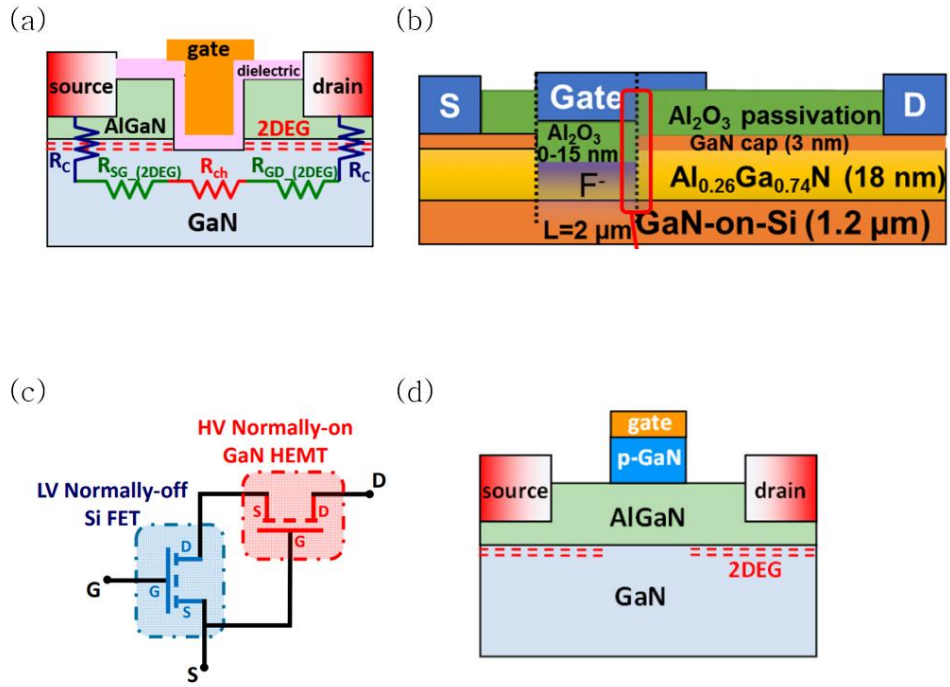


Fig. 1.6 Methods for normally-off AlGaN/GaN FETs; (a) recessed gate [22], (b) Fluorine treatment [24], (c) cascode configuration [22], (d) p-GaN gate [22].

Method	Advantages	Disadvantages
Recessed gate	• Large forward breakdown	• Electron trapping at dielectric/(Al)GaN • Etching damage
Fluorine treatment	• High current density	• Thermal instability • Fluorine ion damage
Cascode configuration	• Stable $V_{th} > 0$ of the Si MOSFET	• Package complexity • Parasitic inductance • High temperature operation limit by si devices
P−GaN gate	• Low resistance under the gate • No dielectric issues	• Limited positive gate voltage swing • P−GaN etching issue

Table. 1.2 Advantages and disadvantages of the various methods for normally-off GaN HEMT.

The recessed gate approach can easily deplete the 2DEG channel by reducing the barrier layer thickness under the gate which can be realized by ICP dry etching [25]. However, low damage etching and high-quality dielectric/(Al)GaN interface are required for the high channel mobility and reliability of the devices. The fluorine treatment introducing negatively charge fluorine ions under the gate also depletes the channel by raising the potential of the AlGaN barrier. As a result, normally-off operation can be realized, but this approach has drawbacks in view of temperature stability

and dispersion behavior as the charged ions might introduce deep traps [21, 26]. P-GaN gate on the AlGaN/GaN is the one of promising approaches for normally-off operation. The big advantage of this approach is that there are no dielectric issues. However, the limited positive gate voltage swing and the P-GaN etching issue are disadvantages of this approach [22]. With the cascode configuration, normally-off operation also can be obtained like in a Si MOSFET. This approach has some drawbacks such as the package complexity and parasitic inductances that affect the switching performance of the devices [27]. More details on methods for normally-off operation can be found in Table 1.2.

1.3. Issues and Feasible Strategies in AlGaN/GaN MIS-HFETs

Among the various methods for normally-off operation of GaN devices, the recessed gate is a promising method because it can be easier to implement than other approaches and ensure normally-off operation. However, as discussed in the former section, charge trapping at the interface between gate dielectric and (Al)GaN and in the gate dielectric is a big issue for recessed gate MIS-HEMTs [28]. This problem leads to degradation of channel mobility, on-resistance and on-current of the devices. Especially, V_{th} hysteresis after a positive gate voltage sweep and V_{th} shift under a gate bias stress are important reliability challenges in gate recessed MIS-HEMTs [29]. Therefore, it is important to understand the basic mechanism of V_{th} shift of the devices. If gate bias is applied to the devices which is large enough for the electrons in the 2DEG to spill over to the dielectric/(Al)GaN interface, the interface traps are quickly filled with electrons and become negatively charged. Also, Bulk traps which is very close to the interface can be filled with electrons and negatively charged. When gate bias returns to zero, the filled traps above Fermi level start to detrap. Although the traps with short time constant release electrons quickly, the traps with long time constant remain filled for a long time, resulting in the V_{th} shift of the devices as shown in Fig. 1.7 [30].

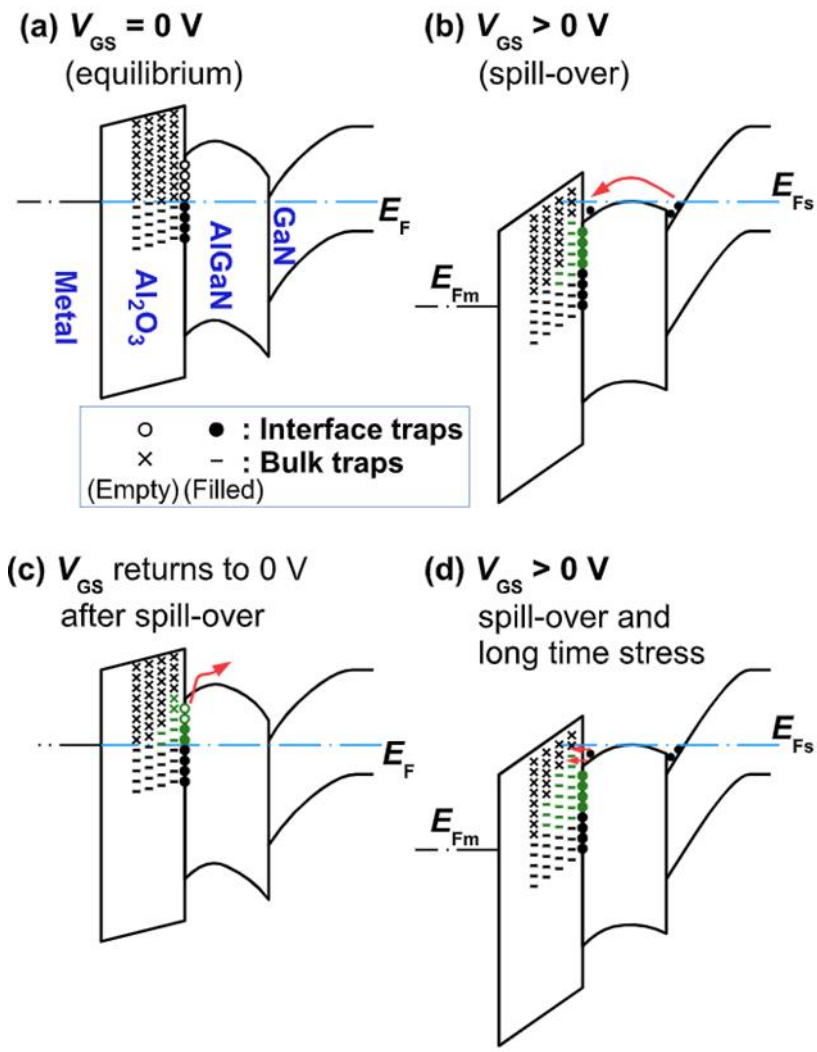


Fig. 1.7 Band diagram of the dielectric/AlGaN/GaN MIS structure under various gate biases [30]

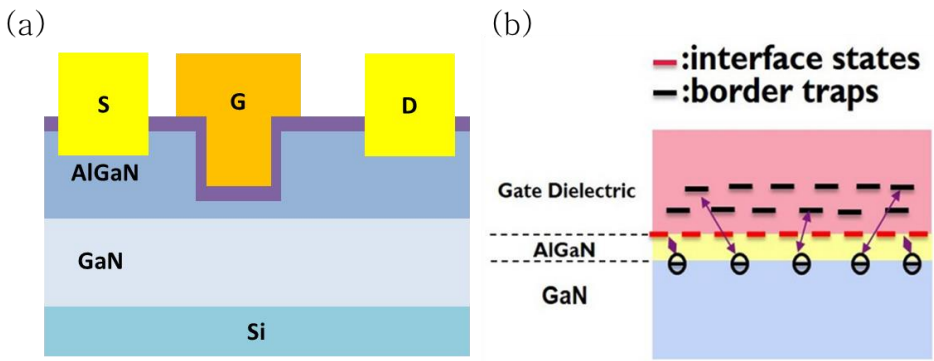
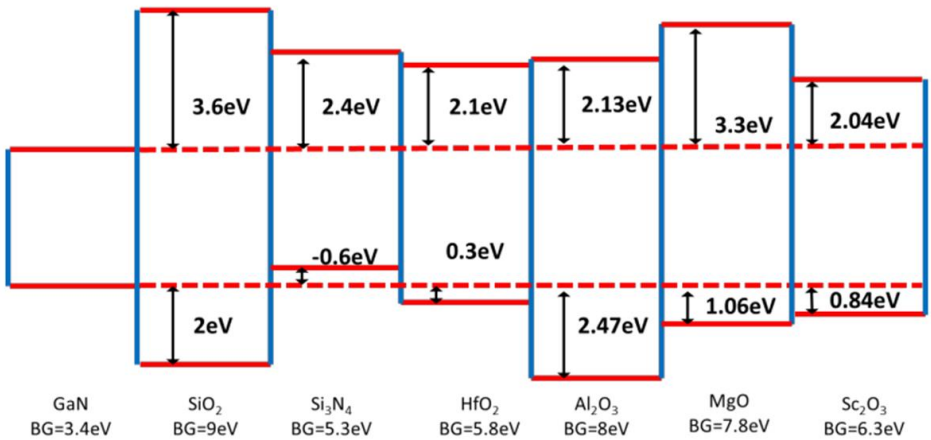


Fig. 1.8 (a) Schematic cross-sectional view of gate recessed MIS-HEMTs, (b) schematic of interface states and border traps in recessed AlGaN/GaN MIS-HEMTs [29]

in order to minimize the V_{th} shift, a gate recess etching with low plasma induced damage and a high-quality gate dielectric are needed for low interface states and border traps in the gate recessed MIS-FETs as shown in Fig. 1.8. In gate recess etching, some methods have been developed for smooth and high-quality interface between the gate dielectric and etched (Al)GaN surface such as slow etch rate of (Al)GaN recipes [31], digital etching using thermal oxidation or oxygen plasma [32, 33] and TMAH wet etching [34]. Also, many studies for reducing the high interface and bulk traps in the gate dielectric have been done using various gate dielectric layers such as SiNx, Al_2O_3, HfO_2 and SiO2 of which various properties such as conduction and valence band offsets of dielectrics on GaN, dielectric constant and bandgap of dielectrics as shown in Fig. 1.9.

(a)



(b)

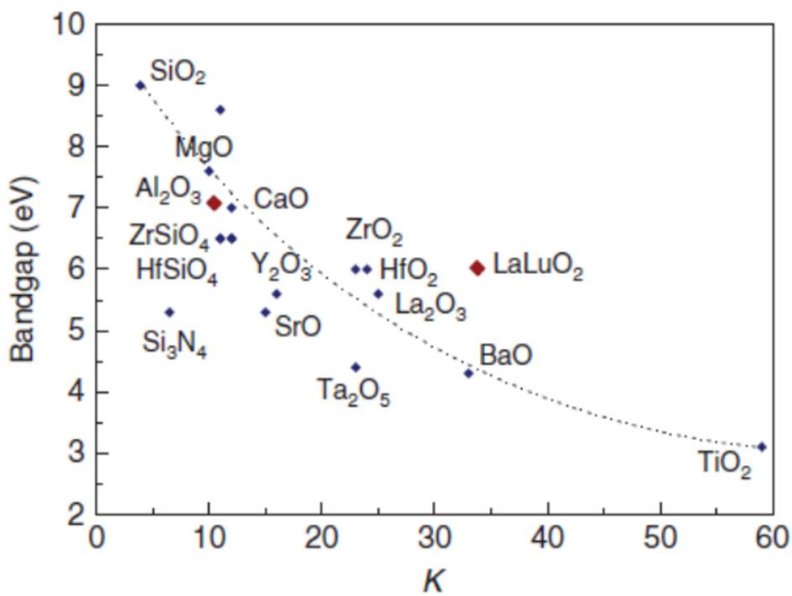


Fig. 1.9 (a) Conduction and valence band offsets for various dielectric on GaN [35], (b) dielectric constant vs bandgap for various dielectric layers [36]

1.4. Research Aims

In this research, process development and characterization of normally-off AlGaN/GaN MIS-FETs are carried out for high power and voltage applications. The final goal of this work is to achieve high quality dielectric/(Al)GaN interface of normally-off AlGaN/GaN MIS-FETs. The detailed outline of this dissertation is described below.

In chapter 2, various etching methods for normally-off operation have been studied. Also, etching damage was evaluated by various methods such as atomic force microscopy (AFM), photoluminescence (PL) measurements, X-ray photoelectron spectroscopy (XPS) measurements and electrical properties of the recessed schottky devices. It was suggested that ALE can break through the limitations of the digital etching and continuous etching processes and enables more precise etching depth control. Also the smoothest etched surface, the highest PL intensity and N/(Al+Ga) ratio of the etched AlGaN surface and the lowest leakage current of the gate recessed schottky devices were obtained by using the ALE.

In chapter 3, normally-off AlGaN/GaN MIS-HEMTs with atomic layer deposited 5 nm SiON/16 nm HfON and with atomic layer deposited 22 nm HfON gate insulator were demonstrated. The devices using SiON also exhibited excellent pulsed I-V and dynamic on-resistance characteristics. In addition, small threshold voltage drift under positive gate bias stress was achieved due to the SiON interfacial layer.

In chapter 4, ALD AlN as an interfacial layer was developed and optimized to avoid the formation of poor-quality oxide at the dielectric/(Al)GaN interface. Also, ALD AlHfON as a bulk layer which had

a high dielectric constant and low leakage current and high breakdown field characteristics was developed. Finally, Normally-off AlGaN/GaN MIS-FETs with 2 nm AlN/3 nm AlON/15 nm AlHfON layer were fabricated. The devices with AlN/AlON/AlHfON layer showed smaller I-V hysteresis of ~10 mV and high drain current density of ~566 mA/mm. the effective mobility, D_{it} and threshold voltage instability characteristics were all improved by employing the ALD AlN.

1.5. References

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Chapter 2. Development and Evaluation of Low Damage Etching Processes

2.1. Introduction

As mentioned in the former section, the gate recess is a promising technique for normally-off operation because it is easier to implement than other approaches and ensure normally-off operation. Due to the high chemical inertness of GaN, many dry etching techniques and plasma chemistries have been used for etching of GaN based materials using reactive ion etching (RIE) [1,2], electron-cyclotron-resonance reactive ion etching [3,4] and inductively coupled plasma reactive ion etching (ICP-RIE) [5-7] as shown in Fig. 2.1. However, plasma induced damage in the gate recess process using such dry etching methods can generates trapping centers on the etched surface and forms a nonstoichiometric surface due to preferential loss of nitrogen [8-10], decreasing the electron mobility and increasing the leakage current of the fabricated devices [8, 11].

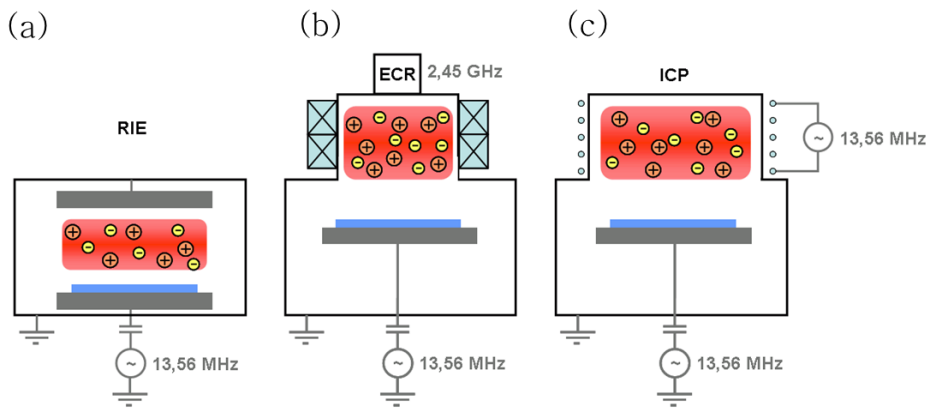


Fig. 2.1 Various dry etching methods (a) reactive ion etching (RIE), (b) electron-cyclotron-resonance reactive ion etching, (c) inductively coupled plasma reactive ion etching (ICP-RIE) [12]

For low etching damage, many research groups have studied various etching methods and resulted in great achievements [13-15]. However, efforts to reduce the etching damage are still needed for improving the electrical performance and reliability of the devices.

2.2. Various Evaluation Methods of Etching Damage

Dry etching is widely used for AlGaN/GaN HFETs due to the limitation of wet chemical etching of (Al)GaN. However, plasma induced damage in the dry etching process can affects the electrical properties of the devices such as channel mobility, leakage current, on-current and V_{th} instability due to formation of traps on the etched surface [16-17]. Therefore, to improve the device performance, it is necessary to clarify the influence and remove etching damage.

Etching damage can be evaluated by various methods such as atomic force microscopy (AFM), photoluminescence (PL) measurements, X-ray photoelectron spectroscopy (XPS) measurements and electrical properties of the recessed schottky devices. Generally, plasma induced damage create nitrogen vacancies of shallow donor levels, resulting in a nonstoichiometric surface [18]. some research groups have used AFM to quantify the surface morphology as root-mean-square (rms) roughness as shown in Fig. 2.2 because rough etch morphology often indicates a nonstoichiometric surface [1, 19].

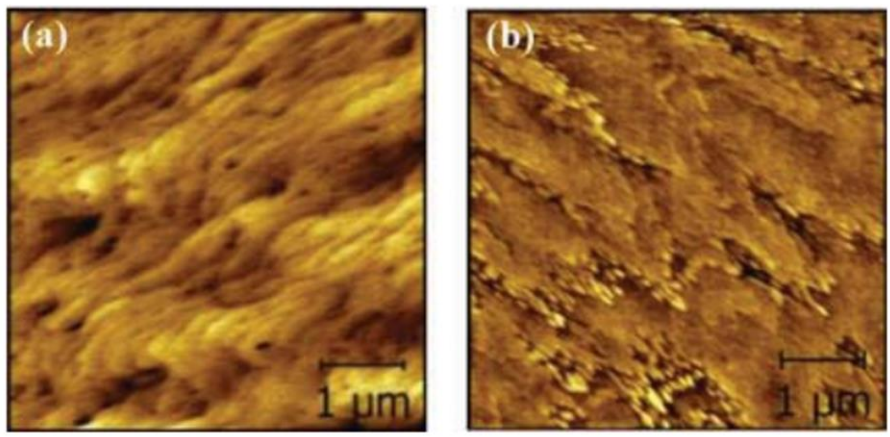


Fig. 2.2 AFM images of GaN surfaces (a) After BCl_3/Cl_2 plasma dry etching (b) After BCl_3/Cl_2 plasma dry etching in ICP system [16]

Also, etching damage can be investigated by observing the electrical properties of recessed schottky devices [8, 16]. As shown in Fig. 2.3.

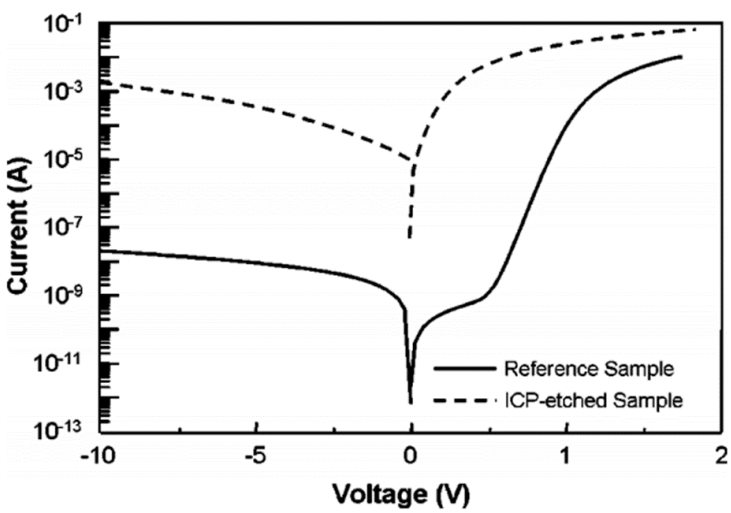


Fig. 2.3 I-V characteristics of Schottky diodes fabricated on both the reference and ICP-etched surfaces [8]

The leakage current of Schottky devices by the dry etching can be explained by tunneling of electrons via plasma induced traps because the traps provide a conducting path with lower energy barrier [8]. Tunneling of electrons through the plasma induced traps is shown in Fig. 2.4.

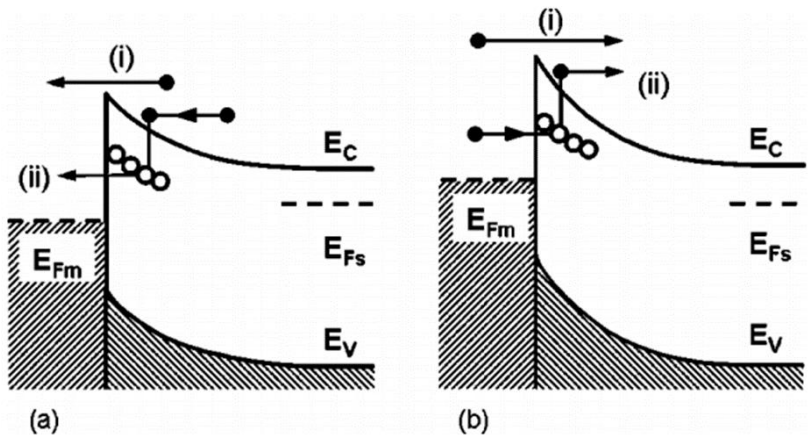


Fig. 2.4 Schematic illustration of electron transport through the interface of metal with ICP -etched GaN: (a) forward bias condition and (b) reverse bias condition [8]

Another method for evaluation of etching damage is to investigate atomic concentration ratio of N/Ga at the etched surface. Physical sputtering of dry etching process removes N atoms preferentially compared to Ga atoms [20]. X-ray photoelectron spectroscopy (XPS) surface analysis can be performed to investigate the surface composition as shown in table 2.1.

	As grown *n*-GaN	Dry etched *n*-GaN (ICP: 500 W, rf chuck: 250 W, and 33% Cl_2 in Cl_2/BCl_3)	Etched *n*-GaN subjected to HF treatment and RTA in N_2 ambient at 900 °C
Ga (%)	28.5±0.2	23.3±0.2	28.1±0.2
N (%)	17.2±0.2	11.1±0.2	16.3±0.2
C (%)	38.5±0.2	34.8±0.2	20.8±0.2
O (%)	15.6±0.2	30.6±0.2	24.6±0.2
Ga/N ratio	1.6±0.1	2.1±0.1	1.7±0.1

Table 2.1 Surface composition of GaN during different processing steps estimated from the XPS data [10]

Additionally, photoluminescence (PL) studies can be used for evaluation of etching damage because plasma induced damage from dry etching process introduce non-radiative centres. photoluminescence intensity is very sensitive to surface recombination [20]. Many research groups have used photoluminescence measurement to evaluate etching damage [20-23] as shown in Fig. 2.5.

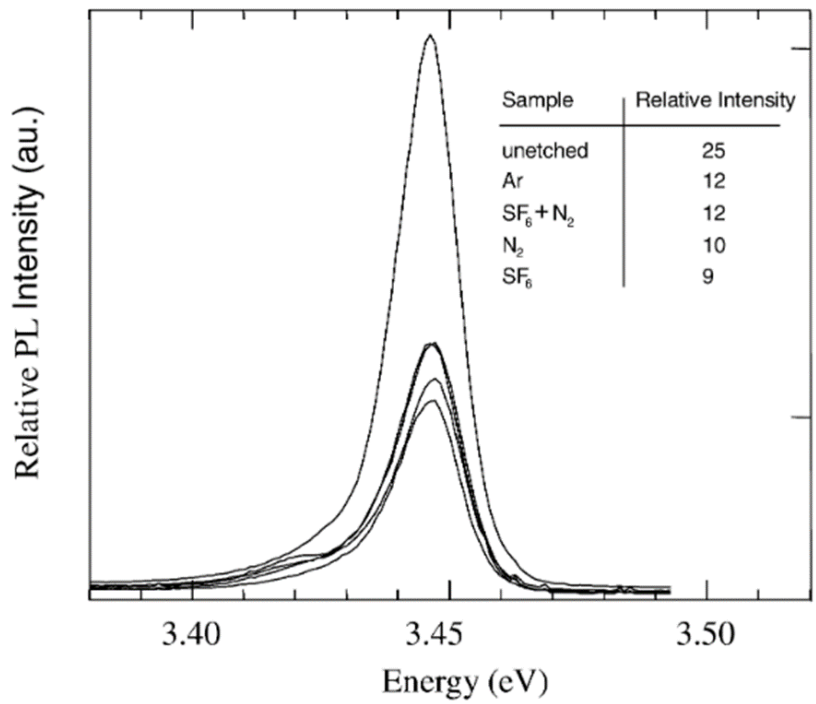


Fig. 2.5 Photoluminescence spectra at 20 K of an unetched GaN sample and samples subject to various plasma exposures [20]

2.3. Low-Damage Dry Etching Methods

2.3.1. Inductively Coupled Plasma–Reactive Ion Etching Using BCl3/Cl2 gas mixture

Dry etching was done using a inductively coupled plasma -Reactive Ion Etching system. It is capable of accommodating 6-inch wafer and can control source and bias power of 13.56 MHz independently. The process chamber was evacuated using a turbo pump and has a helium backside cooling system. The ICP-RIE etcher used in the following experiments is shown in Fig. 2.6.

To estimate the etch rate in each etching condition, AlGaN/GaN on Si epi-wafers were used. The epi structure consists of a Si substrate, a carbon-doped GaN buffer layer, UID GaN channel layer and an AlGaN barrier layer with a GaN cap layer. The samples for estimation of etch rate were prepared as follow: SiN_x layer of 60 nm was deposited on the epi-wafers as a hard mask and patterned using optical lithography and reactive ion etching (RIE) etching using SF_6 gas as shown in Fig. 2.7. After dry etching, the SiN_x mask layer was removed using the dilute hydrofluoric acid (DHF). The etched depth of the samples was measured by atomic force microscopy (AFM).

- Source power: 13.56 MHz
- Bias power: 13.56 MHz
- Controllable DC bias
- Helium backside cooling system
- Automatic loadlock

Fig. 2.6 Configuration of the ICP-RIE system in ISRC

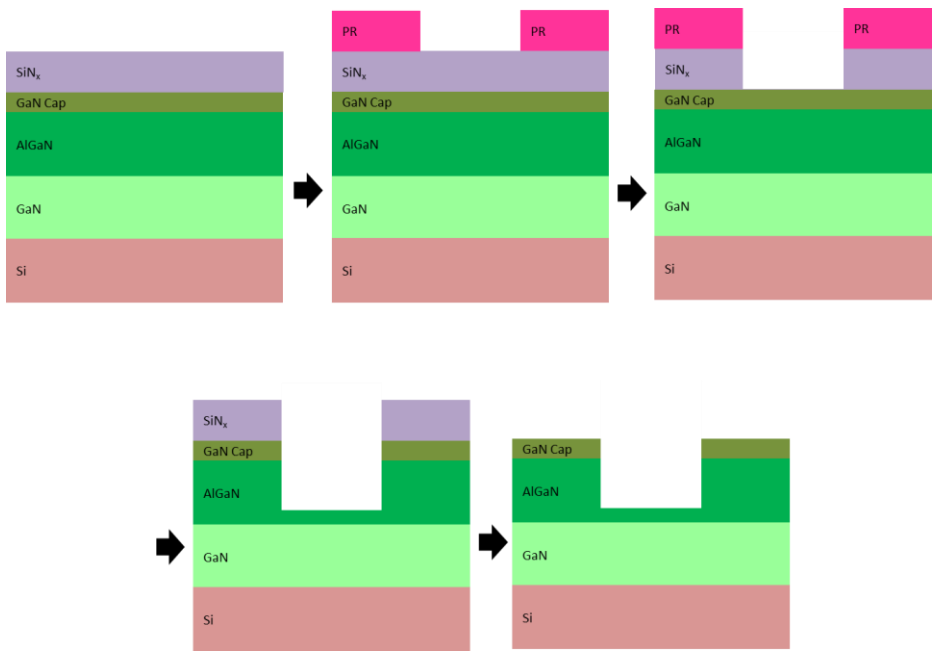
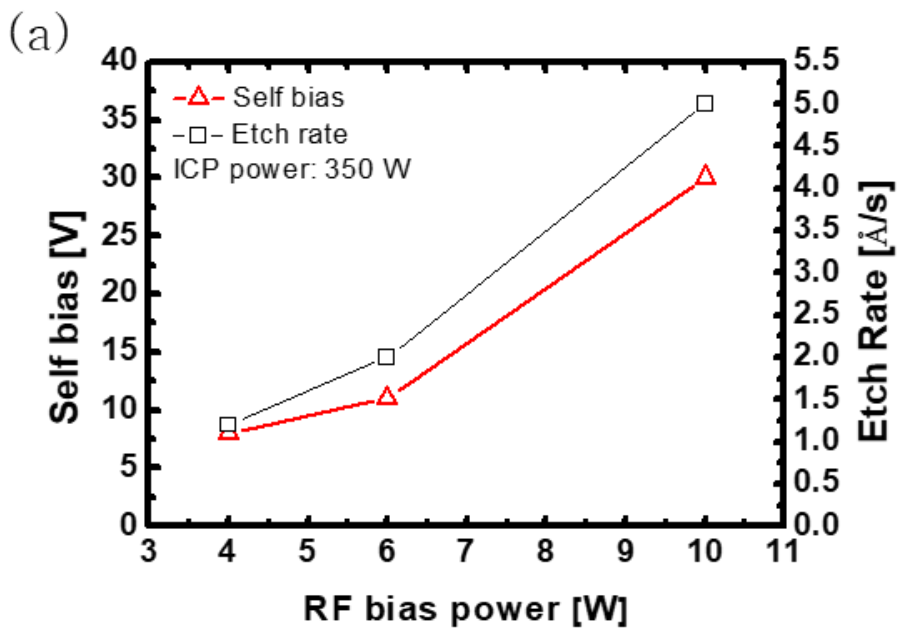


Fig. 2.7 Process flow for estimation of etch rate.

To optimize the etching condition of (Al)GaN, BCl_3/Cl_2 gas mixture was used. The temperature of chuck which samples is placed on was maintained at 5℃ with a chiller system. ICP power and RF bias power are controlled independently at 13.56MHz. It is important to reduce the DC self-bias because it increases ion bombardment energy that can result in plasma induced damage [24-27]. The DC self-bias is strong function of RF bias power and the decreasing trend of DC self-bias was shown as the ICP power increases. It is mainly due to the enhanced ion density at higher ICP power [28]. Detailed results of etching according to the ICP power and RF bias power is well described in Fig. 2.8.



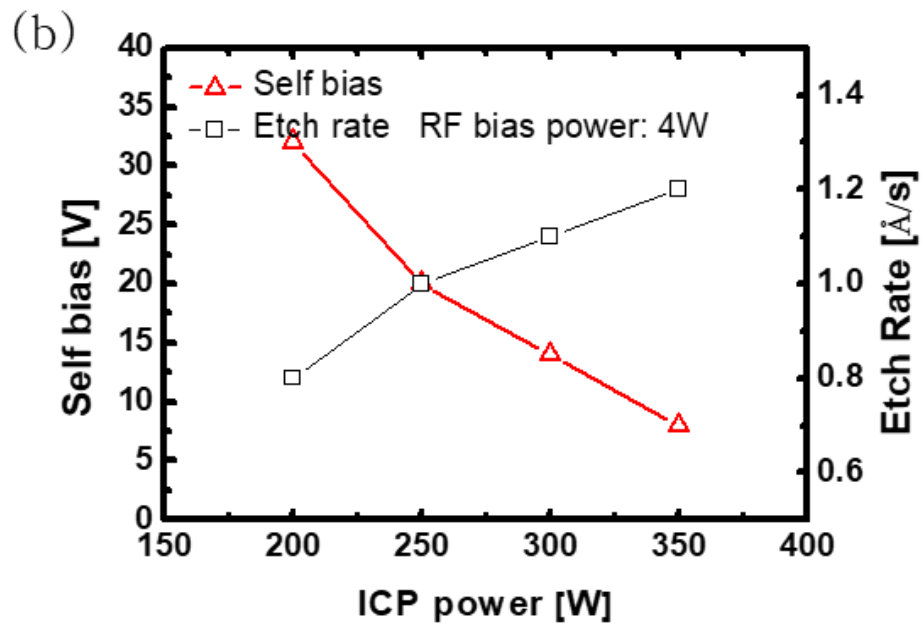


Fig. 2.8 Self bias and etch rate as functions of (a) RF bias power and (b) ICP power

The surface morphology of etching conditions as a function of RF bias power is shown in Fig. 2.9. It is seen that RMS roughness increases with the increasing the RF bias power. It is suggested that the low DC self-bias resulted in the low physical bombardment effect, leading to the smooth surface morphology of the etched surface [29]. The smallest RMS value of 0.28 nm is obtained at the RF bias power of 4 W and the ICP power of 350 W. The lower RF bias power and higher ICP power were not considered due to unstable etch rate and reflected power in those conditions.

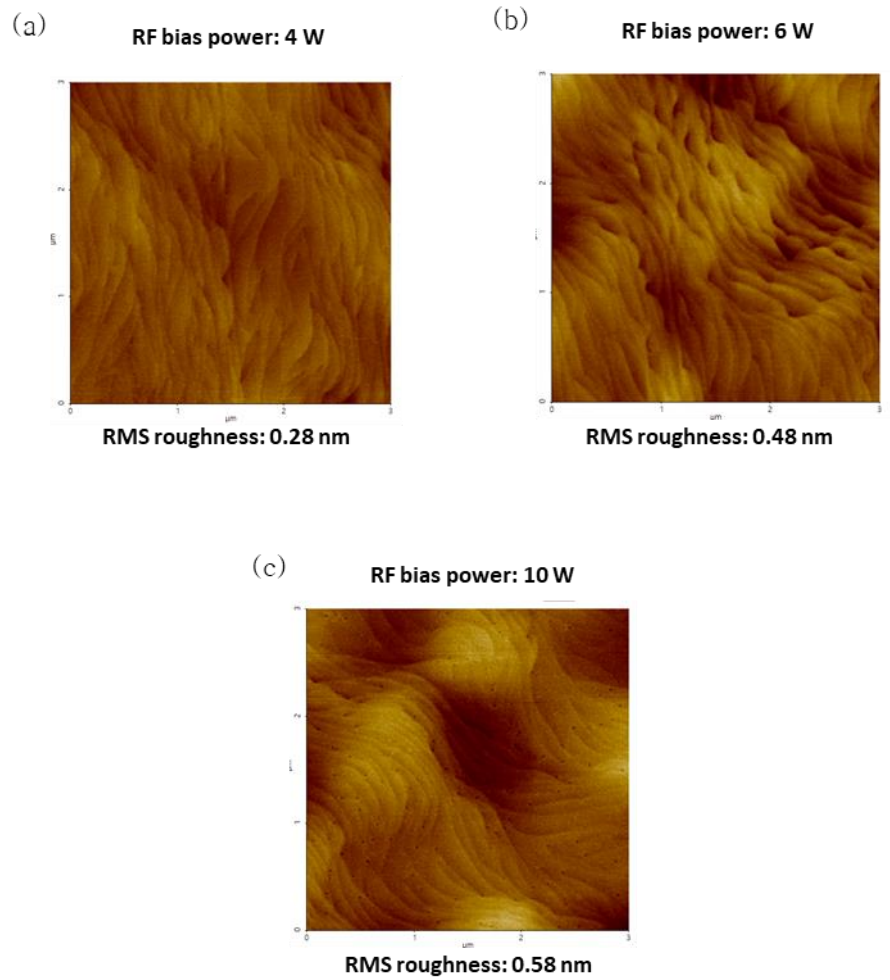


Fig. 2.9 AFM images as functions of RF bias power (a) 4 W, (b) 6 W and (c) 10 W (ICP power: 350 W)

2.3.2. Digital Etching Using Plasma Asher and HCl

As discussed in the former section, the conventional dry etching using the BCl_3/Cl_2 gas mixture has a possibility of damage to the etched surface and limitation to reduce etching damage. Recently, the digital etching consisting of plasma oxidation and wet etching of the oxide has been studied for low etching damage [14, 30] as shown in Fig 2.10.

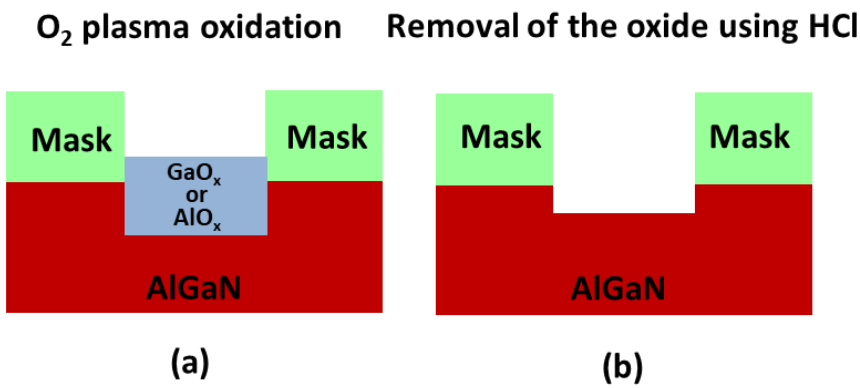


Fig. 2.10 The process of digital etching. (a) plasma oxidation and (b) removal of the oxide using HCl

The digital etching technique can reduce etching damage of the etched surface and easily control the recess depth. Conventionally, plasma oxidation in digital etching has been performed using the reactive ion etch (RIE) or inductively coupled plasma etch (ICP). However, as shown in Fig. 2.11, we used microwave plasma asher for plasma oxidation because microwave-excited plasma is characterized high density and low plasma induced damage [31].

- Manufacturer: Plasma-finish
- Model: V15G
- Rated power output: 300 W
- Frequency: 2.45 GHz

Fig. 2.11 The image of microwave plasma asher which is used for plasma oxidation

Also, After plasma oxidation of AlGaN samples, HCl:H_2O (1:3) at 80 ℃ was used for the removal of oxide because high temperature HCl was more effective in removing the oxide than room temperature HCl. As shown in Fig. 2.12, the lower O1s peak intensity was observed from the AlGaN surface treated with HCl at 80 ℃ than that treated with HCl at room temperature.

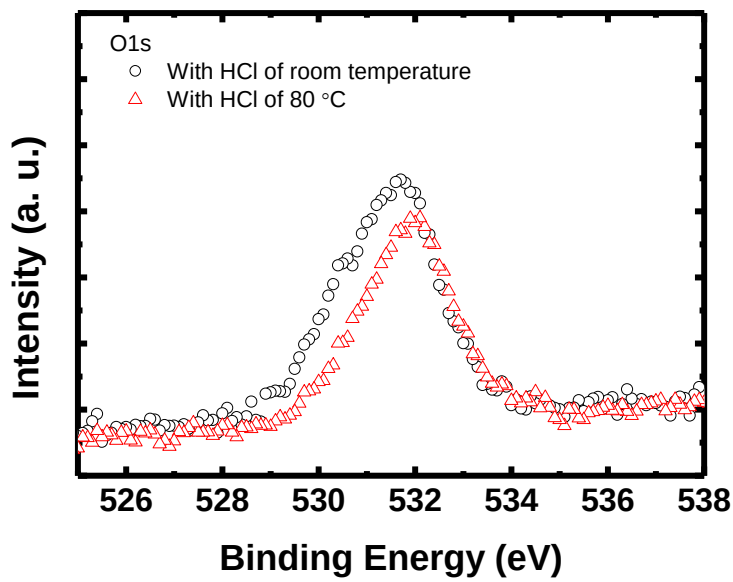


Fig. 2.12 XPS spectra of O1s from the AlGaN surfaces which are treated with HCl at room temperature and HCl at 80 ℃, respectively for 5 minutes after plasma oxidation

To study the effect of the O_2 plasma time, O_2 plasma oxidation of various times were carried out at a fixed dipping time in HCl. As shown in Fig. 2.13, the etch rate per cycle increased with O_2 plasma time up to 3 minutes. Above 3 minutes, the etch rate per cycle remained constant.

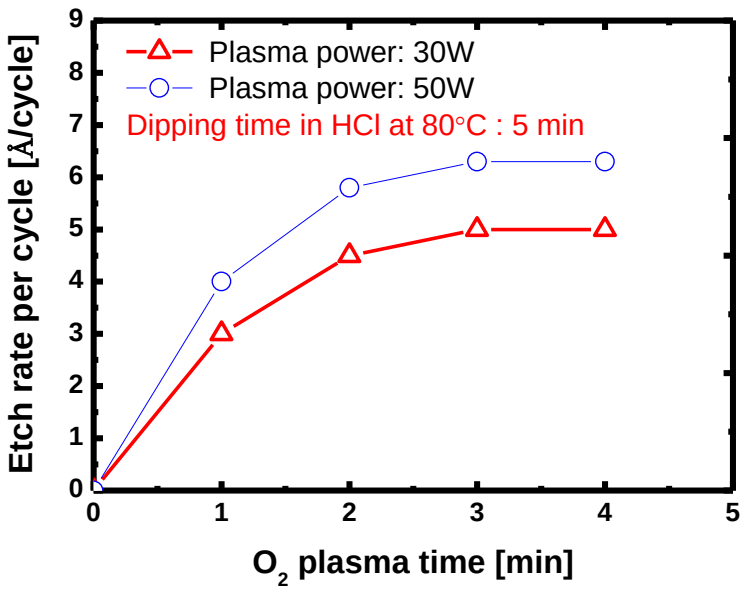


Fig. 2.13 The etch rate per cycle for a fixed dipping time of 5 minutes in HCl at 80 ℃, varying oxygen plasma time and plasma power

The etch rate per cycle for a fixed plasma oxidation time of 3 minutes and varying dipping time in HCl at 80 ℃ was evaluated. The etch per cycle increased by increasing the dipping time in HCl and remained constant at 4 minutes as shown in Fig. 2.14.

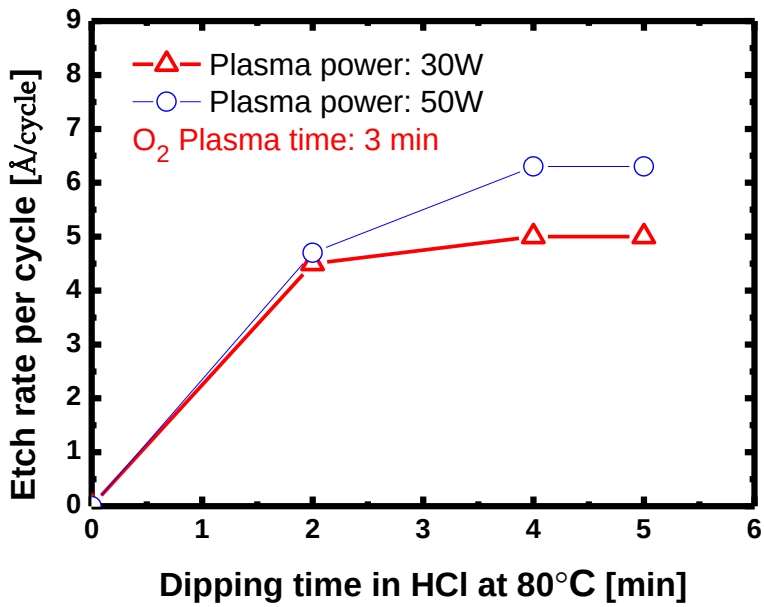


Fig. 2.14 The etch rate per cycle for a fixed oxygen plasma time of 3 minutes, varying dipping time in HCl at 80 ℃ and plasma power

The etch rate per cycle for a fixed plasma oxidation time of 3 minutes and varying dipping time in HCl at room temperature was also evaluated to study the temperature effect of HCl. The etch per cycle increased by increasing the dipping time in HCl and remained constant at 3 minutes as shown in Fig. 2.15. However, the etch rate per cycle was lower than that in HCl at 80 ℃ which shows high temperature HCl was more effective in removing the oxide than room temperature HCl.

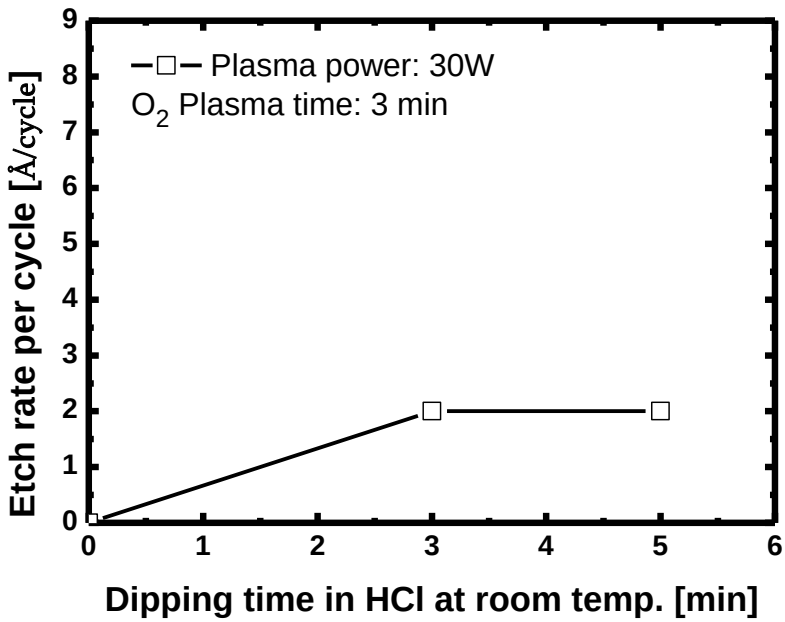


Fig. 2.15 The etch rate per cycle for a fixed oxygen plasma time of 3 minutes and varying dipping time in HCl at room temperature

To evaluate etching damage of the digital etching using asher and HCl, gate recessed schottky devices are fabricated. We used a epi-wafer grown by metal-organic chemical vapor deposition consisting of a 10nm SiN_x in-situ capping layer, a 3.8nm GaN capping layer, a 22.1nm undoped AlGaN barrier layer, a 490nm GaN channel layer, a 4450nm GaN buffer and a Si (111) substrate. The device fabrication was begun by solvent cleaning. The ohmic contacts were formed with partially recessed using BCl_3/Cl_2 plasma, Ti/Al/Ni/Au metallization and rapid thermal annealing at 830 ℃ in N_2 ambient. The contact resistance was 0.7 Ω·mm, which was measured using the transmission line method (TLM) with contact spacings of 2, 4, 6, 8 and 12 um. After MESA isolation using BCl_3/Cl_2 based inductively coupled

plasma reactive ion etch (ICP-RIE), the surface cleaning was carried out using a buffered oxide etch solution (BOE, HF : NH_4F = 1 : 30) for 1 minute and N_2 plasma treatment for 2 minutes with a microwave plasma system, followed by deposition of SiN_x film as a passivation layer. The gate-recess regions were patterned and SiN_x opening was performed with SF_6 based reactive ion etching (RIE) at 20 W. After gate-recess and pad opening process, Ni/Au (40 nm/ 250 nm) gate metal was deposited with e-gun evaporation. Detailed fabrication process for the gate recessed schottky devices was described in Fig. 2.16.

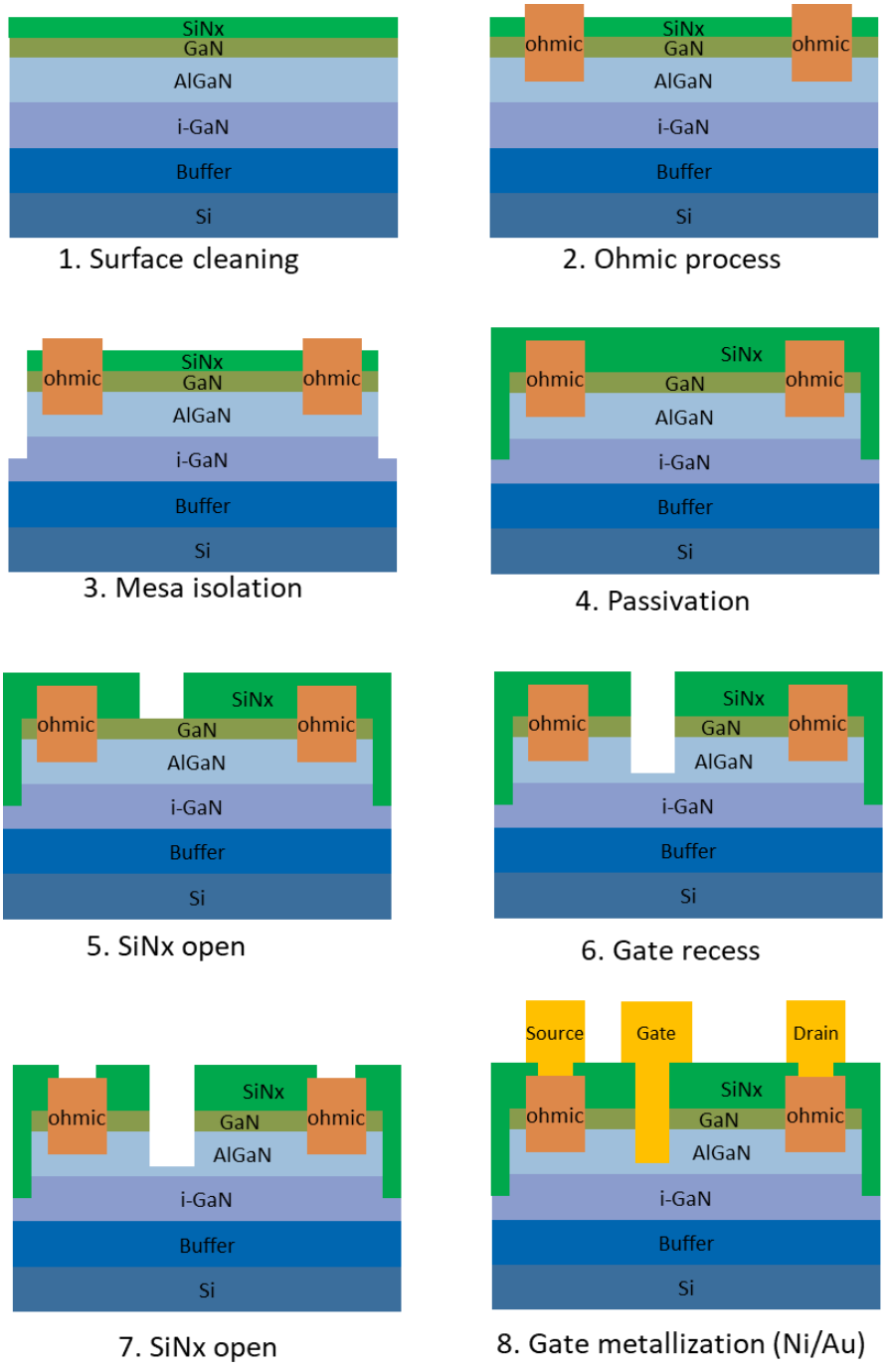


Fig. 2.16 Fabrication process for the gate recessed schottky devices

The gate-recess was performed using two methods. The first method was only BCl_3/Cl_2 based dry etching, while the second method was a combination of BCl_3/Cl_2 based dry etching and digital etching using asher and HCl as shown in Fig. 2.17.

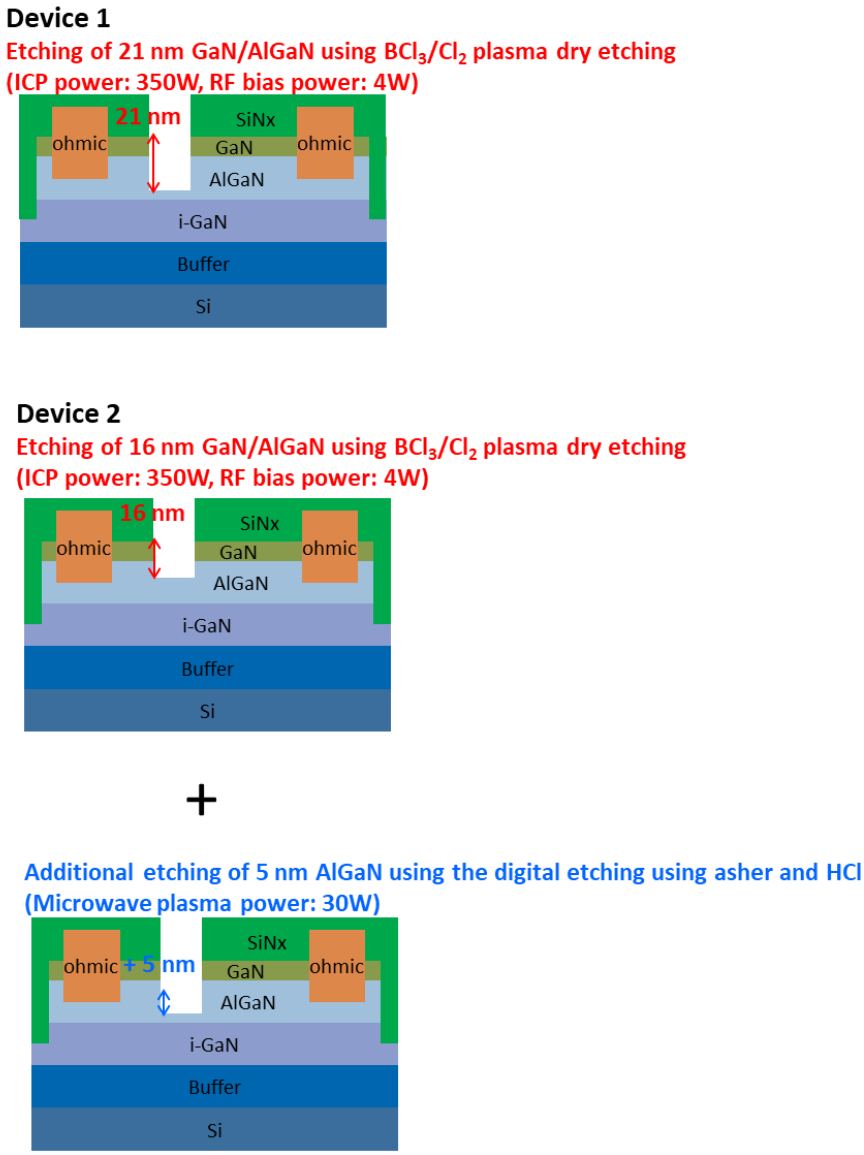


Fig. 2.17 The gate-recess processes for the gate recessed schottky devices

The gate length, source to gate distance, gate to drain distance and gate width of the fabricated devices were 2, 2, 15 and 100 um, respectively as shown in Fig. 2.18.

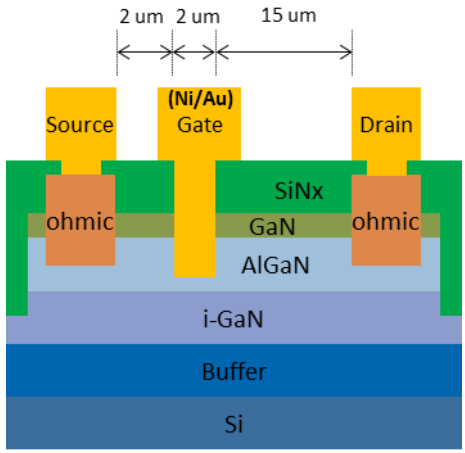
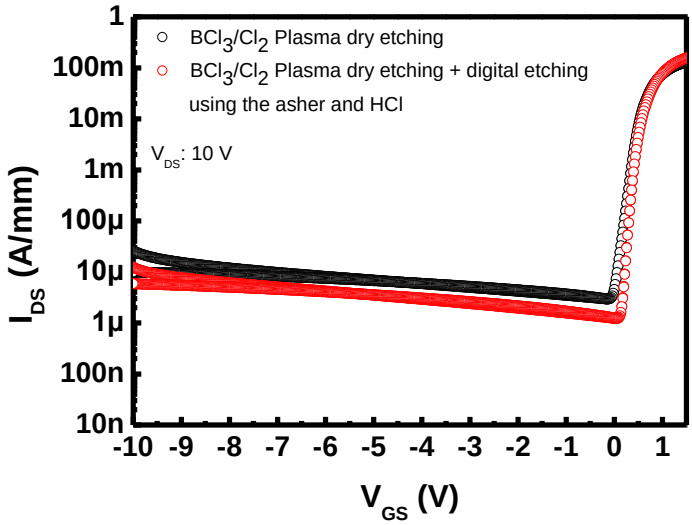


Fig. 2.18 The schematic cross section and dimensions of the fabricated devices

Fig. 2.19 shows I-V characteristics of the gate recessed Schottky devices for the only BCl_3/Cl_2 based dry etching and the combination of BCl_3/Cl_2 based dry etching and digital etching using asher and HCl. The reverse leakage current of the device with digital etching using asher and HCl was lower than that using only BCl_3/Cl_2 based dry etching, showing low etching damage of the device using the digital etching.

(a)



(b)

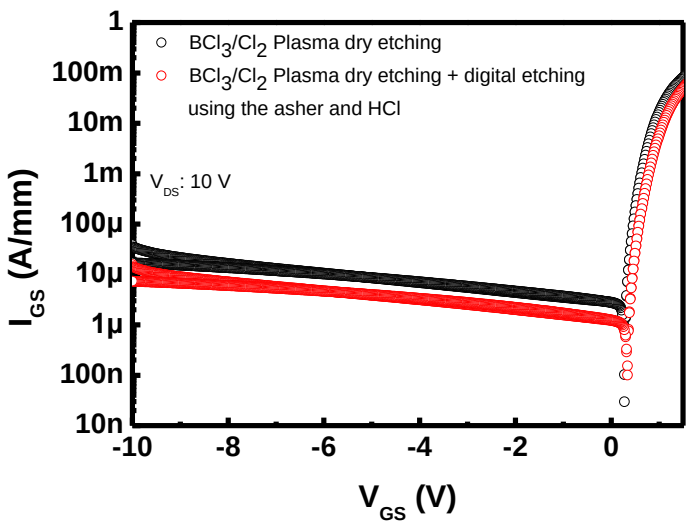


Fig. 2.19 I-V characteristics of the fabricated gate recessed Schottky devices. (a) drain current and (b) gate current

We also investigated the photoluminescence characteristics of three GaN samples. one sample was etched by the BCl_3/Cl_2 based dry etching, another sample was etched by the digital etching using asher and HCl and the other sample was kept unetched as a control sample. The etching depth was ~5 nm for samples. For the photoluminescence experiments, we used a 266 nm laser source with a power of $2W/cm^2$. Fig. 2.20 shows the PL spectra of the three samples.

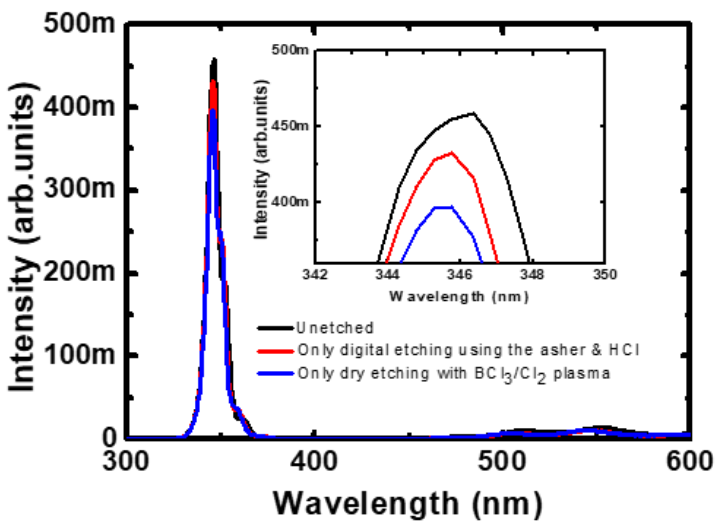


Fig. 2.20 PL characteristics for the samples.

The sample etched by the digital etching using asher and HCl showed the higher band edge peak compared to the sample etched by the BCl_3/Cl_2 based dry etching. This suggests that the digital etching produces less plasma-induced damage on the GaN surface than the BCl_3/Cl_2 based dry etching.

Fig. 2.21 shows atomic force microscopy (AFM) images of a 3 um x

3um area of GaN and AlGaN surface (a) before etching (GaN) (b) after ~5 nm etching by the BCl_3/Cl_2 based dry etching (AlGaN surface) and (c) ~5 nm etching by the digital etching using asher and HCl (AlGaN surface). The used epi structure consists of a Si substrate, a carbon-doped GaN buffer layer, UID GaN channel layer and an AlGaN barrier layer with a GaN cap layer. The root mean square (RMS) surface roughnesses of the surface unetched, the surface etched by the BCl_3/Cl_2 based dry etching and the surface etched by the digital etching were 0.19, 0.28 and 0.25 nm respectively. This result indicates the low plasma-induced damage characteristics of the digital etching.

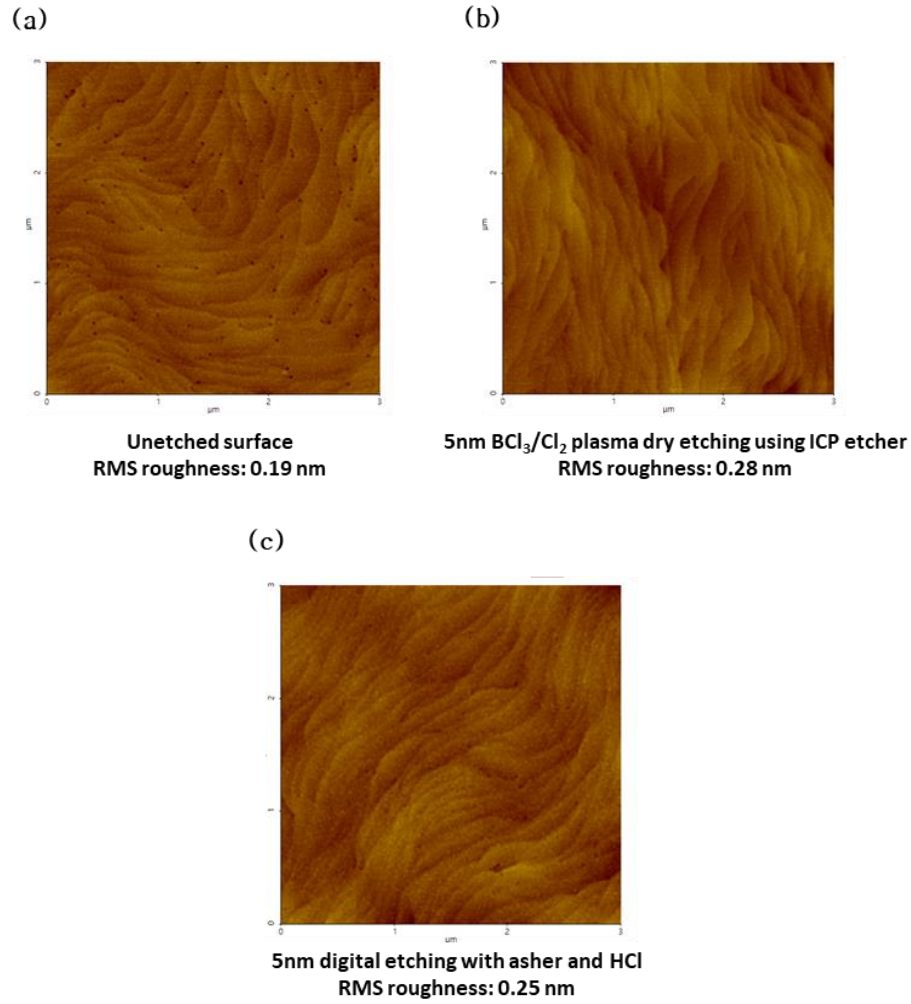


Fig. 2.21 Atomic force microscopy (AFM) images of a 3um x 3um area. (a) before etching, (b) after ~5 nm etching by the BCl_3/Cl_2 based dry etching using ICP etcher and (c) ~5 nm etching by the digital etching using asher and HCl

We also performed X-ray photoelectron spectroscopy (XPS) measurements on the etched samples as an evaluation method of etching damage. An epi-wafer consisting of a Si substrate, a carbon-doped GaN buffer layer, UID GaN channel layer and an AlGaN barrier layer with a GaN cap layer was used for XPS analysis. one sample was etched by the BCl_3/Cl_2 based dry etching and the other sample was etched by the digital etching. The etched depth of samples was ~5 nm. The XPS results of the etched AlGaN surfaces are shown in Table 2.2.

	BCl_3/Cl_2 based dry etching	Digital etching using asher & HCl
Al (%)	9.6	8.6
Ga (%)	28.7	25.8
N (%)	29.9	28.2
O (%)	5.4	8
C (%)	26.4	29.4

Table 2.2 The XPS results of the etched AlGaN surfaces by the BCl_3/Cl_2 based dry etching and the digital etching using asher and HCl

Fig. 2.22 also show the N/(Al+Ga) ratios for the two samples. We found that the etched sample by the digital etching using asher and HCl had N/(Al+Ga) ratio of 0.82, while the etched sample by the BCl_3/Cl_2 based dry etching had less nitrogen on the AlGaN surface (N/(Al+Ga)=0.78). High N/(Al+Ga) ratio of the sample etched by the digital etching indicates that the digital etching technique has less physical sputtering component and lower etching damage characteristics compared to the BCl_3/Cl_2 based dry etching

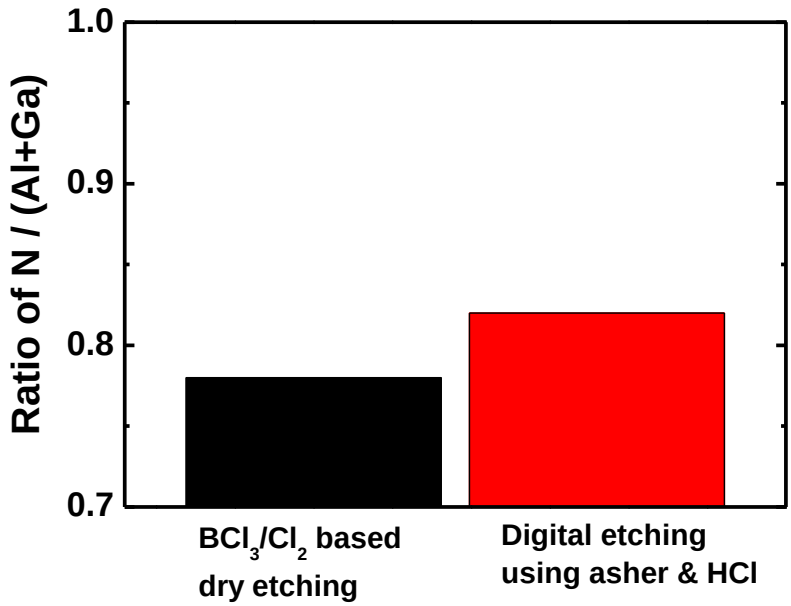


Fig. 2.22 N/(Al+Ga) ratios of the etched samples by the BCl_3/Cl_2 based dry etching and the digital etching using asher and HCl

2.3.3. Atomic Layer Etching Using Inductively Coupled Plasma – Reactive Ion Etching System

The digital etching process using O_2 plasma asher for oxidation of AlGaN and HCl : H_2O solution for removal of the formed oxide layer has been presented, but it is labor-consuming and take much process time due to the low etch rate (~0.5 nm/cycle) compared to other etching processes. The recent studies on atomic layer etching (ALE) have demonstrated that Atomic layer etching using O_2 and BCl_3 gases could reduce etching damage and improve the surface roughness [32-34]. Also, ALE can break through the limitations of continuous etching processes and enables more precise etching depth control. However, It is important to have a self-limiting characteristics in ALE resulting in the good linearity between the etching depth and the number of cycles. Also Efforts to reduce the dc self-bias in ALE are needed for low etching damage.

We studied a ALE using the ICP-RIE system and O_2 and BCl_3 gases for AlGaN etching. The ALE is composed of four steps as shown in Fig. 2.23.

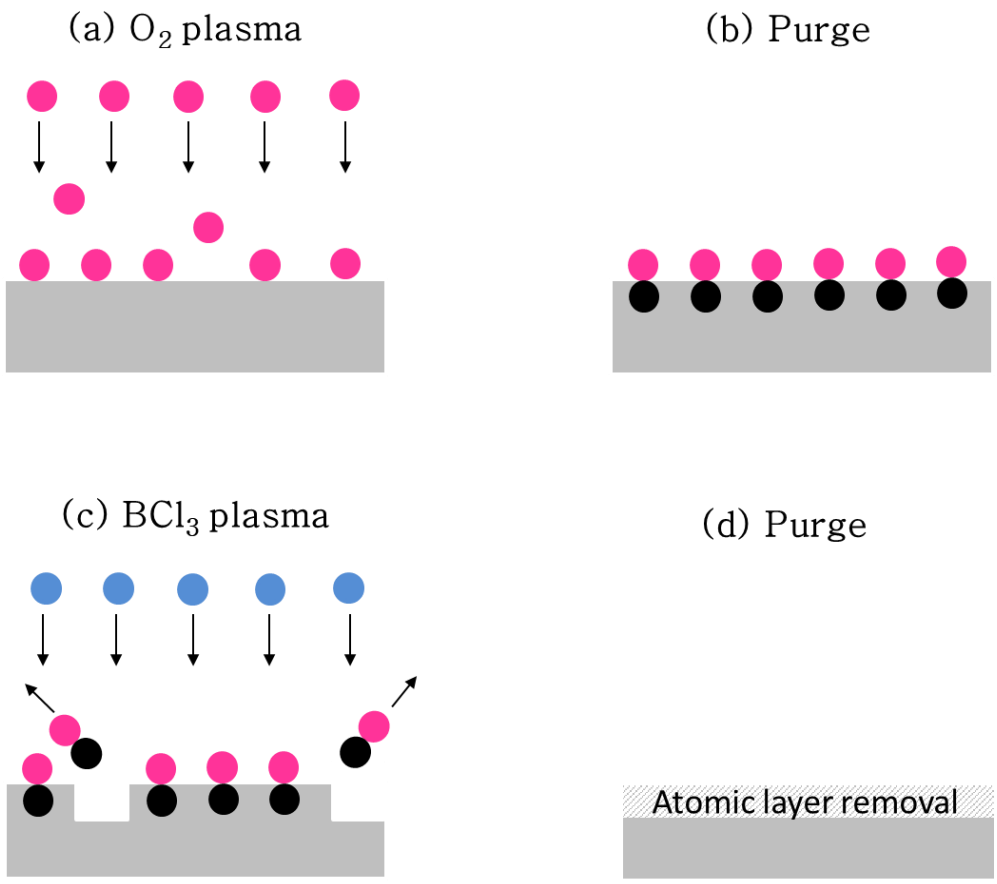


Fig. 2.23 Schematic illustration of one cycle of ALE. (a) O_2 plasma, (b) purge, (c) BCl_3 plasma and (d) purge.

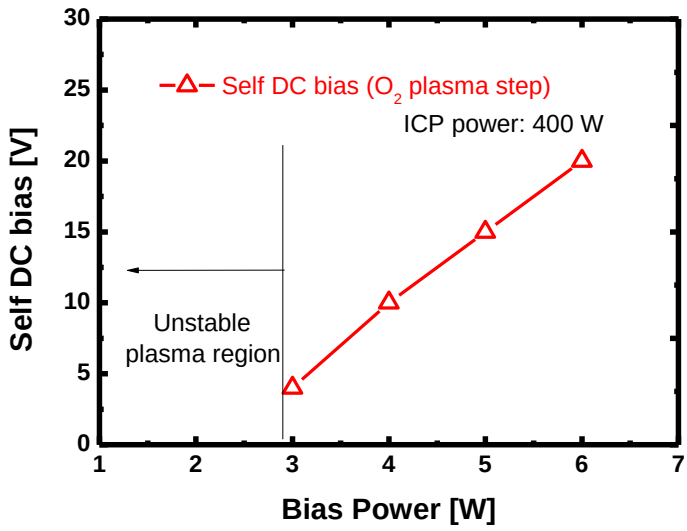
The AlGaN was oxidized with O_2 plasma and a purge step was carried out to remove residual gases and radicals in the chamber. Then, the oxidized layer was removed with BCl_3 plasma and a purge step was carried out.

The ALE process was performed in the ICP-RIE system, operating at a 13.56MHz RF bias power and a separate 13.56MHz RF ICP power. The temperature of the chuck was room temperature and the chamber pressure of the O_2 plasma step and the O_2 flow rate were 50mtorr and 50sccm respectively. the chamber pressure of the BCl_3 plasma step and the BCl_3 flow rate were 10mtorr and 10sccm respectively.

To estimate the etch rate of the ALE, AlGaN/GaN on Si epi-wafers consisting of a Si substrate, a carbon-doped GaN buffer layer, UID GaN channel layer and an AlGaN barrier layer with a GaN cap layer were used. Also, a SiN_x was used as a mask layer. After the ALE, the SiN_x mask layer was removed using the dilute hydrofluoric acid (DHF). The etched depth of the samples was measured by atomic force microscopy (AFM).

To study the effect of the bias power on the DC self-bias, for varying bias power and a fixed ICP power of 400W, the DC self-biases were investigated. The results are shown in Fig. 2.24

(a)



(b)

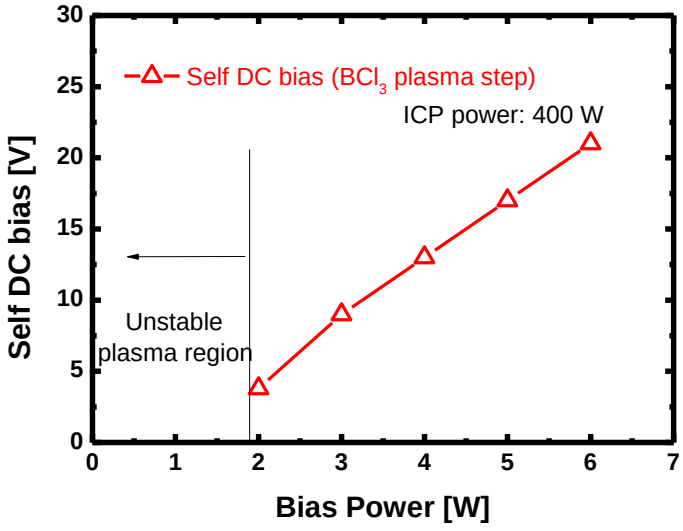
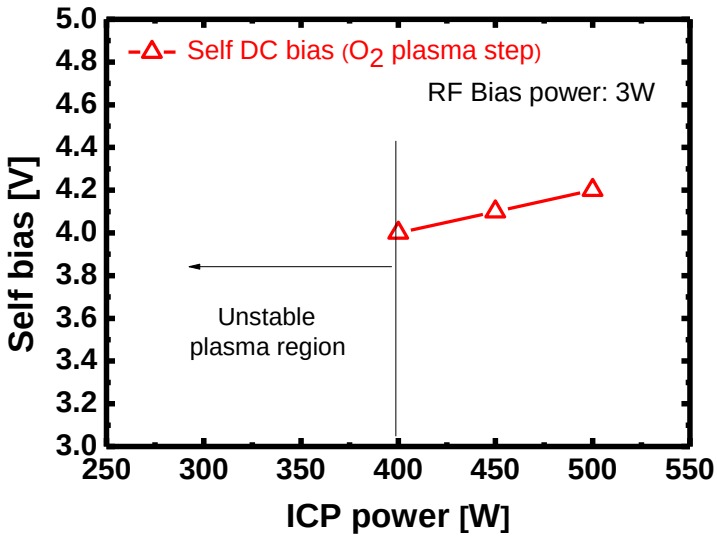


Fig. 2.24 The DC self-biases for varying bias power and a fixed ICP power of 400W. (a) O_2 plasma step and (b) BCl_3 plasma step

The DC self-bias increased with an increase of the bias power. We chose the bias power of 3W in the O_2 plasma step and the bias power of 2W at the BCl_3 plasma step for the ALE process because each plasma step was unstable at lower bias powers. As shown in Fig. 2.25, the effect of the ICP power on the DC self-bias was also investigated for varying ICP power and a fixed bias power. The DC self-bias decreased with an increase of the ICP power at the both plasma steps. This decreasing trend of the DC self-bias is mainly due to the enhanced ion density at higher ICP power [28]. We chose the ICP power of 400W at both plasma steps for the ALE process.

(a)



(b)

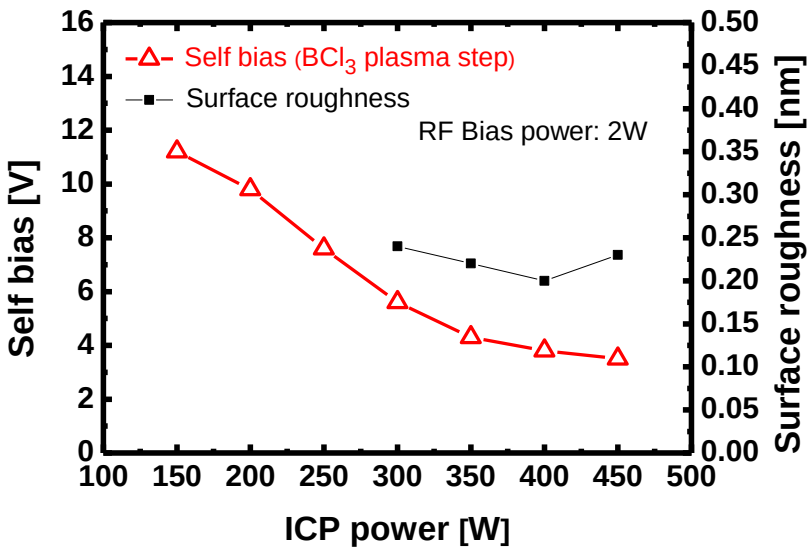
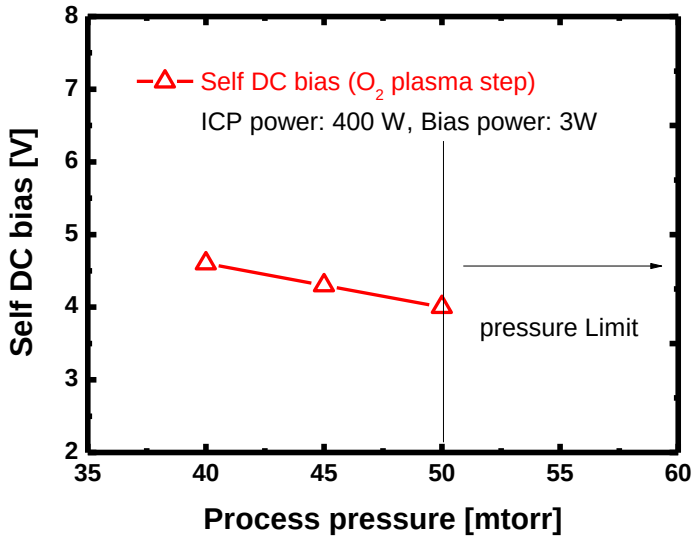


Fig. 2.25 The DC self-biases for varying ICP power and the fixed bias power. (a) O_2 plasma step and (b) BCl_3 plasma step

The effect of the pressure at the both plasma steps was studied at the fixed ICP power of 400W and the fixed bias power of 3W (O_2 plasma step) or 2W (BCl_3 plasma step) as shown in Fig. 2.26. The DC self-bias decreased with an increase of the pressure at the O_2 plasma step. However, the DC self-bias increased with an increase of the pressure at the BCl_3 plasma step. For the low DC self-bias, the pressure of 50mtorr and 10mtorr were chosen for the O_2 plasma step and the BCl_3 plasma step, respectively.

(a)



(b)

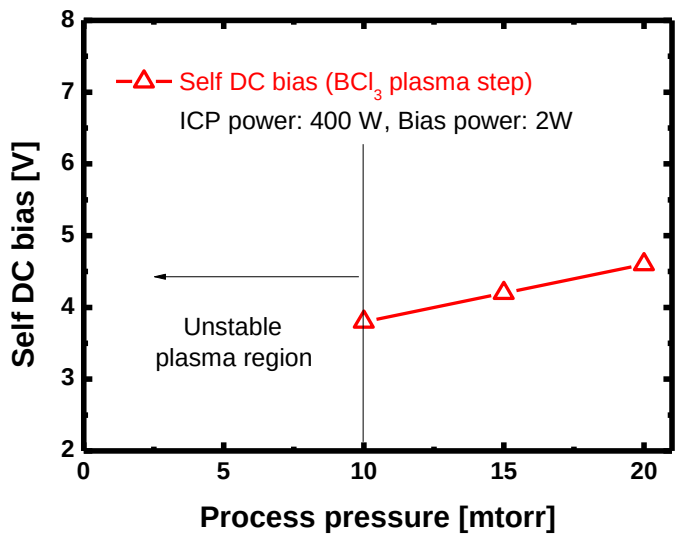


Fig. 2.26 The DC self-biases for varying pressure and the fixed bias and ICP power. (a) O_2 plasma step and (b) BCl_3 plasma step

As mentioned above, It is important to have a self-limiting characteristics in ALE, resulting in the good linearity between the etching depth and the number of cycles. For varying bias power and the fixed ICP power of 400W with BCl_3 plasma, etch rates are investigated as shown in Fig. 2.27. The AlGaN layer is not etched at the bias power of 2W and the etch rates increased with the increase of the bias power. It indicates that our ALE technique is a self-limiting etch process at the bias power of 2W with BCl_3 plasma.

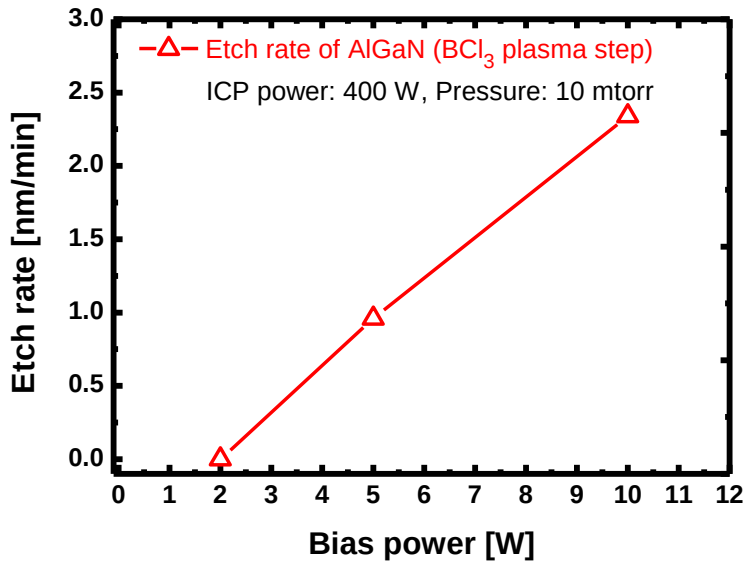


Fig. 2.27 Etch rates for varying bias power and the fixed ICP power of 400W with BCl_3 plasma

Fig. 2.28 shows that the etch rate per cycle for varying O_2 plasma time per cycle and each different BCl_3 plasma time per cycle. The etch rate increased with O_2 plasma time per cycle up to 60 sec. Above 60 sec of O_2 plasma time per cycle, the etch rate per cycle remained fairly constant at the both BCl_3 plasma times. The etch rate per cycle at the BCl_3 plasma time of 60sec was higher than that at BCl_3 plasma time of 30sec. Fig. 2.29 shows that the etch rate per cycle for varying BCl_3 plasma time per cycle and each different O_2 plasma time per cycle. The etch rate increased with BCl_3 plasma time per cycle up to 45 sec at the O_2 plasma time per cycle. Above 45sec of BCl_3 plasma time per cycle, the etch rate per cycle became saturated. The etch rate per cycle at the O_2 plasma time of 60sec was higher than that at the O_2 plasma time of 30sec.

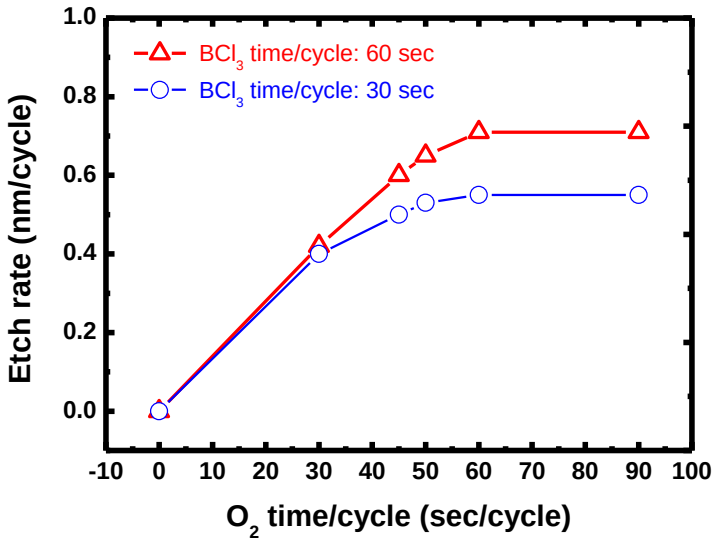


Fig. 2.28 Etch rates for varying O_2 plasma time and each different BCl_3 plasma time per cycle

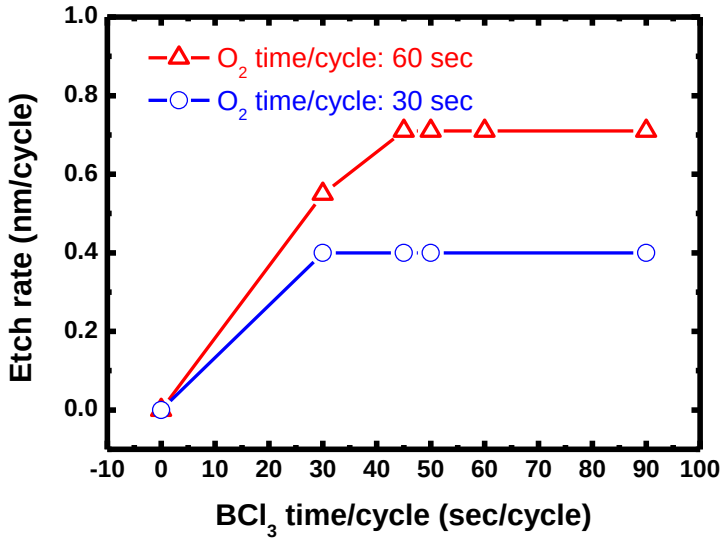


Fig. 2.29 Etch rates for varying BCl_3 plasma time and each different O_2 plasma time per cycle

The linearity of the ALE was investigated as shown in Fig. 2.30. the result showed a good linearity between the etched depth versus the number of cycles, indicating that the ALE technique had good controllability in terms of the etch depth.

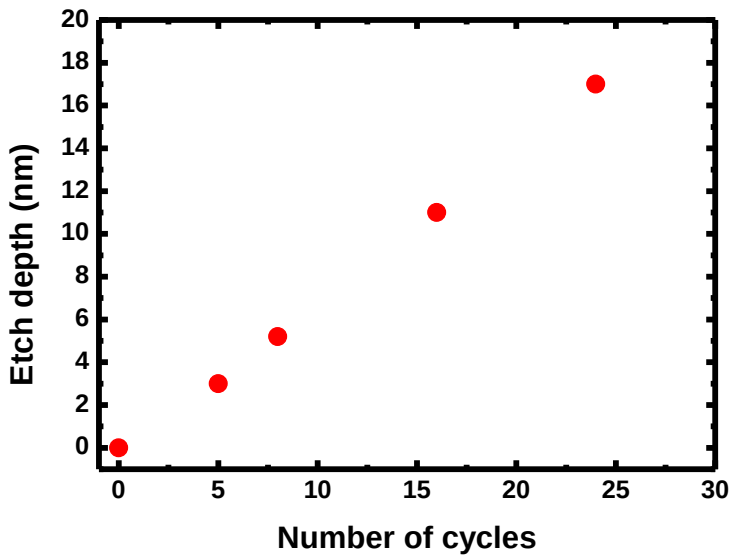
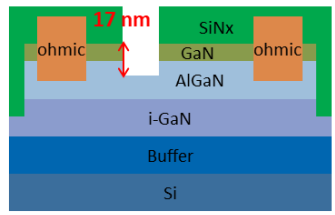


Fig. 2.30 The ALE linearity between the etch depth and the number of cycles

To evaluate etching damage of the ALE, gate recessed schottky devices are fabricated. We used an epi-wafer grown by metal-organic chemical vapor deposition consisting of a 9.9nm SiN_x in-situ capping layer, a 3.7nm GaN capping layer, a 22nm undoped AlGaN barrier layer, a 490nm GaN channel layer, a 4450nm GaN buffer and a Si (111) substrate. Because the epi-wafer had a different epi-structure with that used in the previous section 2.3.2, we fabricated gate recessed schottky devices using the digital etching with asher and HCl again as the reference devices. The fabrication process for the gate recessed Schottky devices was same to the process in the section 2.3.2. The gate-recess was performed using two methods. The first method was a combination of BCl_3/Cl_2 based dry etching and digital etching using asher and HCl, while the second method was a combination of BCl_3/Cl_2 based dry etching and ALE. Details of the gate-recess processes for the gate recessed Schottky devices are shown in Fig. 2.31.

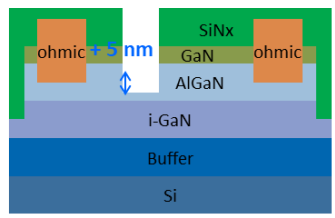
Device 1

Etching of 17 nm GaN/AlGaN using BCl_3/Cl_2 plasma dry etching



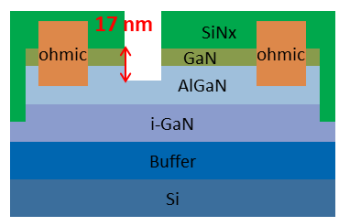
+

Additional etching of 5 nm AlGaN using digital etching using asher & HCl



Device 2

Etching of 17 nm GaN/AlGaN using BCl_3/Cl_2 plasma dry etching



+

Additional etching of 5 nm AlGaN using ALE

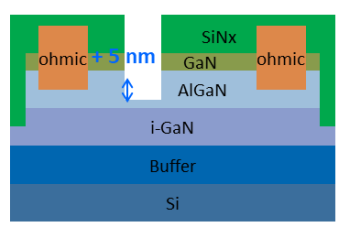


Fig. 2.31 The gate-recess processes for the gate recessed Schottky devices

The gate length, source to gate distance, gate to drain distance and gate width of the fabricated devices were 1.5, 2, 10 and 100 um, respectively as shown in Fig. 2.32.

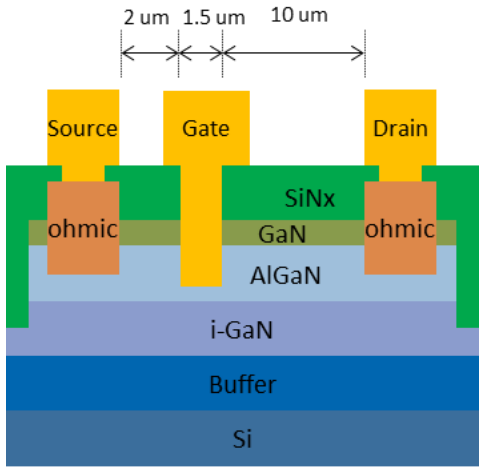


Fig. 2.32 The schematic cross section and dimensions of the fabricated devices

I-V characteristics of the fabricated gate recessed Schottky devices is shown in Fig. 2.33. The reverse leakage current of the device using ALE was lower by one order than that using the digital etching with asher and HCl. It can be explained by reduction of electrons tunneling via plasma induced traps because the traps provide a conducting path with lower energy barrier. It also suggests that lower etching damage can be achieved by the ALE than the digital etching with asher and HCl.

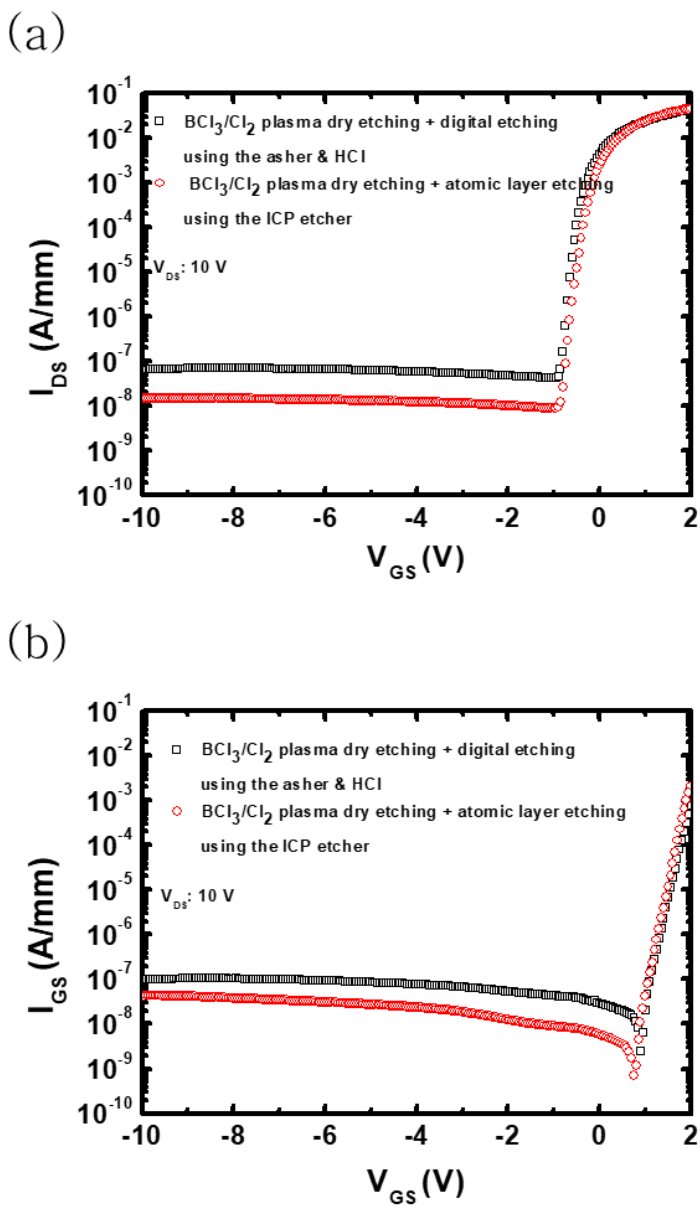


Fig. 2.33 I-V characteristics of the fabricated gate recessed Schottky devices. (a) drain current and (b) gate current

Photoluminescence characteristics of GaN samples were investigated. A sample was etched by the ALE and the etching depth was ~5 nm. A GaN sample which was etch by the digital etching using asher and HCl and an unetched control GaN sample were also plotted for comparison. For the photoluminescence experiments, we used a 266 nm laser source with a power of 2W/cm^2. Fig. 2.34 shows the PL spectra of the three samples.

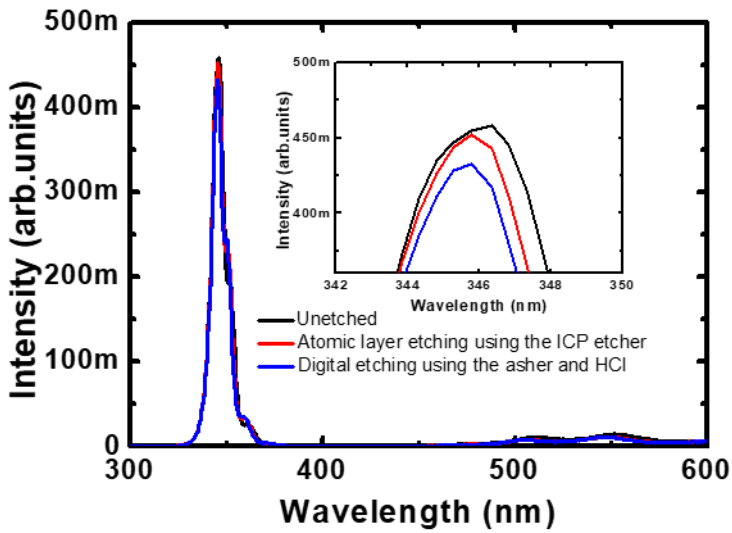


Fig. 2.34 PL characteristics for the samples.

The sample etched by the ALE showed the higher band edge peak compared to the sample etched by the digital etching using asher and HCl. This result indicates that the ALE produces less plasma-induced damage on the GaN surface than the digital etching using asher and HCl. Also, PL intensity of the GaN sample etched by the ALE was almost comparable to that of the unetched control sample.

The surface morphology of the AlGaN samples and the control sample

were investigated by atomic force microscopy (AFM). Fig. 2.35 shows images of a 3um x 3um area of AlGaN and GaN surfaces (a) before etching (GaN) (b) after ~5 nm etching by the digital etching using asher and HCl (AlGaN surface) and (c) ~5 nm etching by the ALE (AlGaN surface). The root mean square (RMS) surface roughnesses of the surface unetched, the surface etched by the digital etching and the surface etched by the ALE were 0.19, 0.25 and 0.2 nm respectively. The surface roughness of the sample etched by the ALE was almost comparable to that of the control sample indicating the low plasma-induced damage characteristics of the ALE.

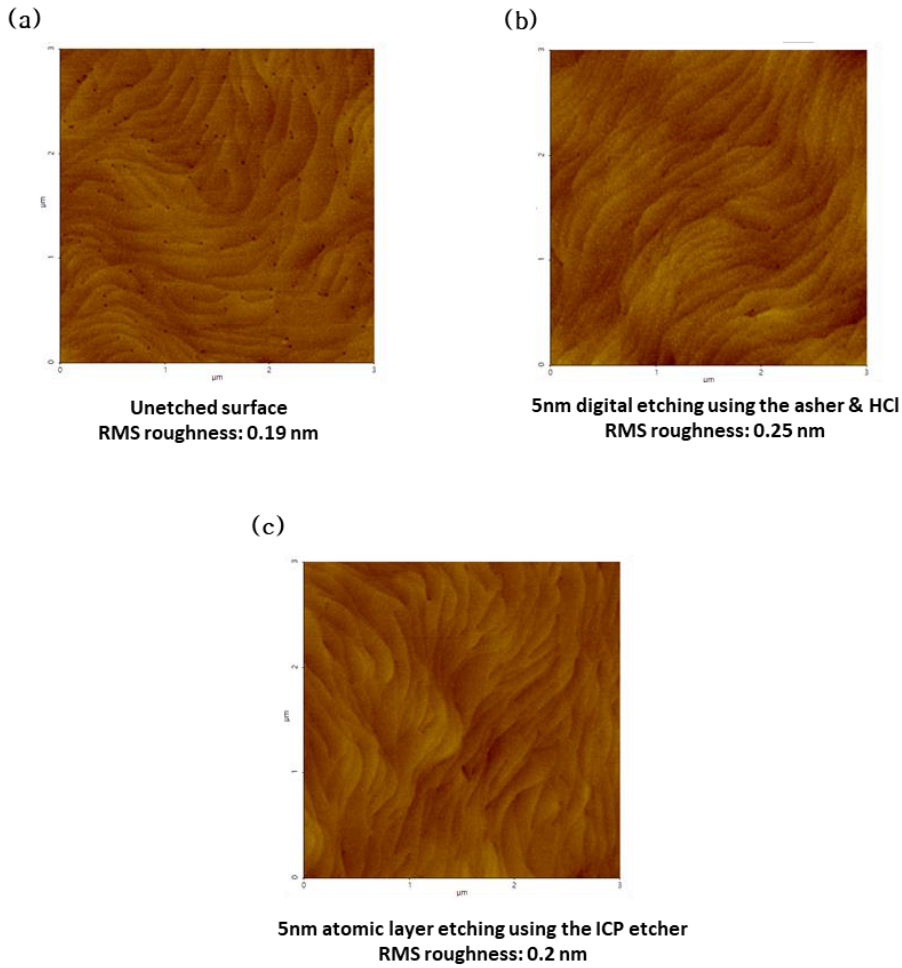


Fig. 2.35 Atomic force microscopy (AFM) images of a 3um x 3um area. (a) before etching, (b) after ~5 nm etching by the digital etching using asher and HCl and (c) ~5 nm etching by the ALE

Table. 2.3 shows the results of X-ray photoelectron spectroscopy (XPS) measurements on the etched samples for evaluation of etching damage. one sample was etched by the digital etching using asher and HCl and the other sample was etched by the ALE. The etched depth of samples was ~5 nm.

	Digital etching using asher & HCl	Atomic layer etching using ICP etcher
Al (%)	8.6	9
Ga (%)	25.8	27.2
N (%)	28.2	32.7
O (%)	8	5.8
C (%)	29.4	25.2

Table 2.3 The XPS results of the etched AlGaN surfaces by the digital etching using asher and HCl and the atomic layer etching using ICP etcher

From the XPS results, the N/(Al+Ga) ratios for the two samples are evaluated as shown in Fig 2.36. The sample etched by the ALE showed higher N/(Al+Ga) ratio of 0.9 than the sample etched by the digital etching which showed N/(Al+Ga) ratio of 0.82. It indicates that the generation of N vacancies can be reduced by using the ALE [35-36].

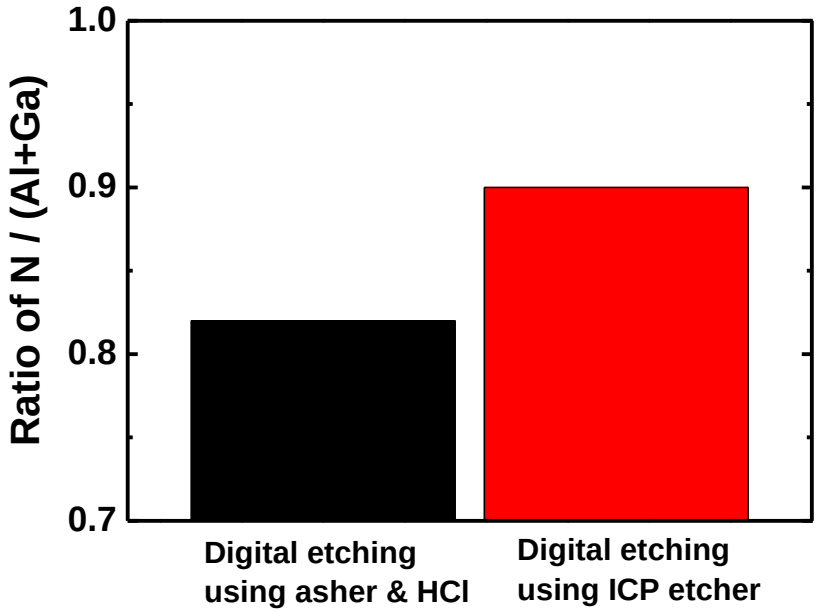


Fig. 2.36 N/(Al+Ga) ratios of the etched samples by the digital etching using asher and HCl and the ALE using ICP etcher

The etching damage of ALE was also evaluated using schottky diodes on the etched n-GaN by ALE. For comparison, diodes on the as-grown n-GaN and the etched n-GaN by digital etching using asher and HCl were also fabricated. We used a n-GaN on Si wafer consisting of a 300 nm n-GaN with 2.5E+17cm^{-3} Si doping concentration, a 700 nm n-type GaN layer, a 700 nm n-GaN with 2~3E+18cm^{-3} Si doping concentration, a 3900 nm GaN buffer layer and Si substrate. The device fabrication was begun by solvent cleaning using acetone, methanol and isopropanol. Then, 200 nm SiN_x passivation layer was deposited as an etching mask layer. Ohmic contacts were formed with Ti/Al metallization and RTA annealing at 550 ℃ in N_2 ambient. Then SiN_x opening was performed with SF_6 based reactive ion

etching (RIE) at 20 W and etching processes of 5 nm were carried out using the ALE and digital etching, respectively. After SiNx opening process, Ni/Au (40/200 nm) metal electrode was deposited with e-gun evaporation. The circular metal electrodes had diameters of 50 um and was separated by a 15 um gap from a concentric contact. The device cross-section is shown in Fig. 2. 37.

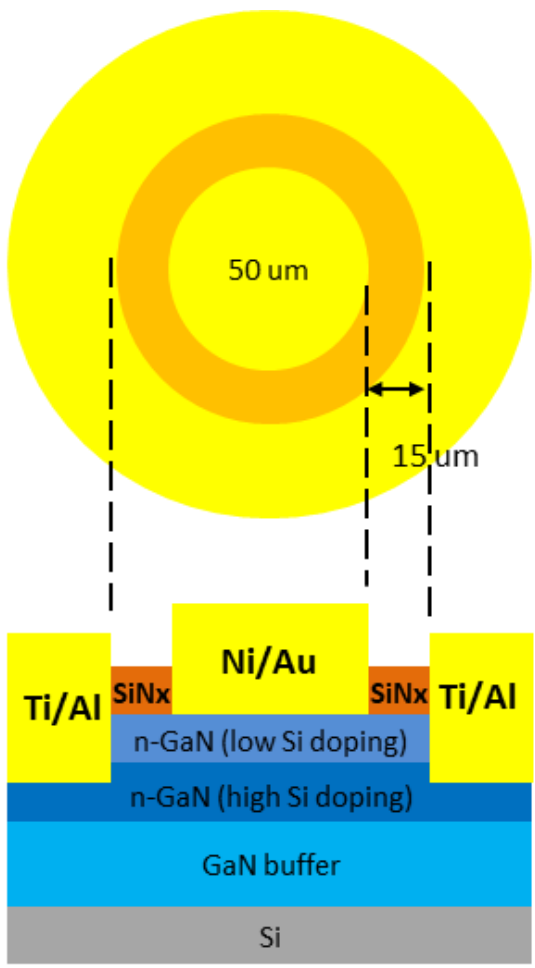
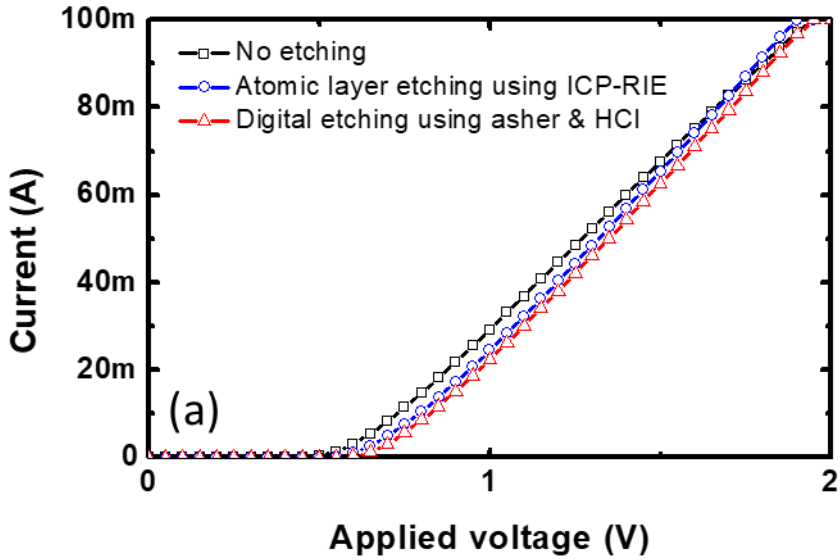
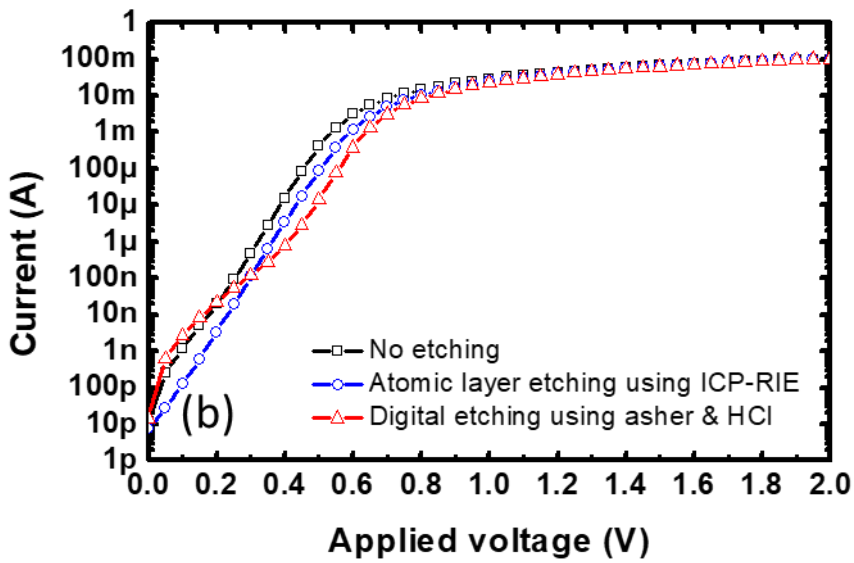


Fig. 2.37 Cross-section of the fabricated diodes on n-GaN

Fig. 2.38 and Table 2.4 show I-V characteristics of the fabricated diodes on n-GaN and ideality factors and barrier heights determined from I-V measurements, respectively.





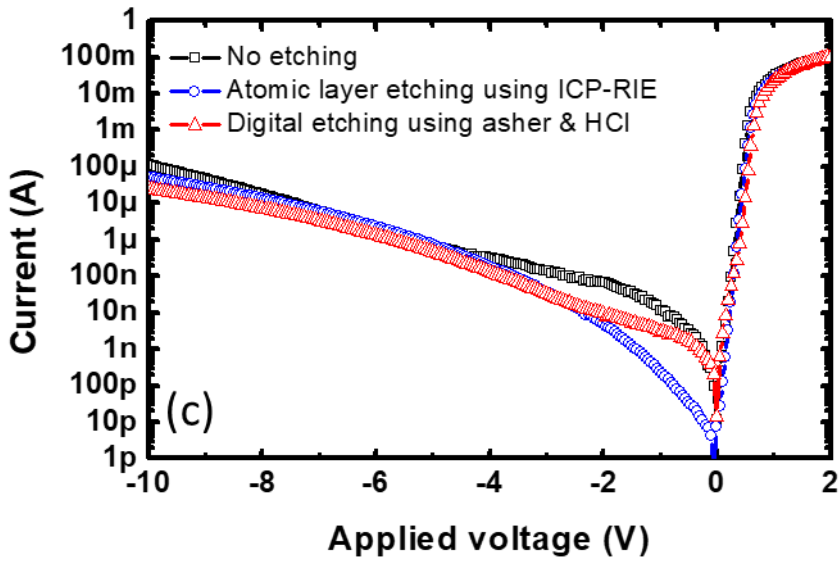


Fig. 2.38 I-V curves of the fabricated diodes on n-GaN. (a) forward I-V characteristics (linear scale), (b) forward I-V characteristics (log scale) and (c) reverse I-V characteristics (log scale)

Sample	Room temperature ideality factor n	Barrier height Φ_{B0}
No etching	1.38	0.75
Atomic layer etching using ICP-RIE	1.17	0.81
Digital etching using asher and HCl	1.83	0.72

Table 2.4 Ideality factors and barrier heights determined from I-V characteristics of the fabricated diodes on n-GaN

Schottky diodes on n-GaN etched by the ALE showed the lowest reverse leakage current less than 10^{-8} A at -2 V and ideality factor of 1.17 and the highest zero-bias barrier height of 0.81 eV among the fabricated Schottky diodes on n-GaN. It indicates that the ALE has very low etching damage and improve the I-V characteristics of Schottky diodes on n-GaN.

2.4. Conclusion

In this chapter, various etching methods for normally-off operation have been studied. Also, etching damage was evaluated by various methods such as atomic force microscopy (AFM), photoluminescence (PL) measurements, X-ray photoelectron spectroscopy (XPS) measurements and electrical properties of the recessed schottky devices. It was suggested that the low DC self-bias resulted in the low physical bombardment effect, leading to the smooth surface morphology of the etched surface in the BCl_3/Cl_2 based dry etching. As another etching method, the digital etching using plasma oxidation with a microwave asher and removal of oxide with $HCl:H_2O$ (1:3) was investigated. The digital etching method showed lower etching damage than the BCl_3/Cl_2 based dry etching. However, it is labor-consuming and take much process time due to the low etch rate (~0.5 nm/cycle) compared to other etching processes. ALE can break through the limitations of the digital etching and continuous etching processes and enables more precise etching depth control. Also, the smoothest etched surface, the highest PL intensity and N/(Al+Ga) ratio of the etched AlGaN surface and the lowest leakage current of the gate recessed schottky devices were obtained by using the ALE. It is suggested that the ALE is a promising etching technique for normally-off gate recessed AlGaN/GaN MIS-FETs.

2.5. References

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Chapter 3. SiON/HfON Gate Dielectric Layer by ALD for AlGaN/GaN MIS-FETs

3.1. Introduction

Enhanced-mode (E-mode) GaN-based FETs have attracted great interests for high-power applications including electric vehicles, because GaN provides excellent characteristics for power devices such as large energy bandgap, high mobility, and high breakdown field. Though recessed-gate AlGaN/GaN metal-insulator-semiconductor field-effect transistors (MIS-FETs) are considered as most promising for E-mode operation, the MIS interface issues are still challenging to limit the device performances and the reliabilities.

Recently, high-k dielectrics such as hafnium, zirconium, and lanthanum based oxides have been applied for MIS insulators of GaN MIS-FETs [1, 2, 3]. They provided a decreased off-state leakage current, a high on-state current, a high on/off current ratio, and a low subthreshold swing, which would improve the efficiency in power conversion systems. However, when a high-k dielectric with a relatively-small band gap such as HfO_2 with a band gap of 5.7 eV [4] is employed as a gate insulator, significant gate leakage currents could occur due to small conduction band discontinuity [5, 6]. Another common problem with high-k gate dielectric concerns the poor

characteristics of the interface between the high-k dielectric and the III-N semiconductor, which degrades the device performances [7].

HfO_2 has been widely used as a high-k gate dielectric for Si CMOS and III-V MOS devices, but its applications for GaN power devices have been mostly limited to depletion-mode (D-mode) devices [1, 8]. High trap density of HfO_2 could induce much larger hystereses in I-V and C-V characteristics and more prominent reliability problems in E-mode devices. To improve HfO_2 bulk properties, incorporation of nitrogen, leading to HfON, has been extensively utilized to passivate oxygen vacancies [9].

The recent studies demonstrated that SiN_x deposited by advanced deposition techniques such as plasma-enhanced atomic layer deposition (PE-ALD) could provide high-quality interface characteristics for AlGaN/GaN MIS-FETs [10, 11]. However, the band gap of SiNx is smaller than that of SiO_2 or Al_2O_3, which could lead to a high degree of gate leakage currents. On the other hand, the most popular insulator SiO_2 provided low gate leakage currents and high breakdown voltages for AlGaN/GaN MIS-FETs [12], even though it showed large electron trapping effects at the dielectric/III-N interface. SiON is a promising candidate for use in gate insulator because it has the advantages of both SiO_2 and SiN_x [13]. However, few studies have investigated E-mode AlGaN/GaN FETs employing a nitrogen-incorporated oxide such as SiON or HfON as a gate insulator or a gate interfacial layer Except our recent study on SiON for AlGaN/GaN FETs. Recently, we fabricated normally-off recessed-gate AlGaN/GaN MIS-FETs with dual gate insulator employing PEALD-SiNx interfacial layer and RF-sputtered HfO_2 [14]. In this study, we demonstrated high performance E-mode AlGaN/GaN MIS-FETs with atomic layer deposited 5 nm SiON/16 nm HfON. Plasma nitridation was employed in every atomic

layer deposition cycle to deposit SiON and HfON dielectrics. SiON was used as an interfacial layer to ensure a high-quality AlGaN/dielectric interface and a high-k HfON was employed to realize a large transconductance and a high on-state current. The fabricated devices exhibited low gate and off-state drain leakage current (~10^{-10} and ~10^{-11} A/mm, respectively), a high on/off current ratio (1.2 x 10^{11}) and a maximum drain current of 602 mA/mm. A high effective channel mobility of 887 $cm^2/V{\cdot}s$ and excellent dynamic characteristics during the switching operation were also achieved. AlGaN/GaN MIS-FETs employing 22 nm ALD HfON gate insulator were also fabricated with the otherwise identical process and compared.

3.2. ALD Processes for SiON and HfON

High-quality gate dielectric layer is strongly demanded in AlGaN/GaN MIS-FETs for low leakage current and interface trappings between (Al)GaN and gate dielectric layer [15-16]. There are many deposition processes that can decide dielectrics and interface quality. Inductively coupled plasma-chemical vapor deposition (ICP-CVD) CVD, plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), physical vapor deposition (PVD) and atomic layer deposition (ALD) are typical deposition processes of gate insulator or passivation layer [17-21] as shown in Fig. 3.1.

ALD gate dielectric has been considered as a good candidate for gate insulator because fine film thickness control, superior conformability and excellent electrical characteristics of applied devices can be achieved by ALD [22-23]. Details of the advantages for ALD and comparison of ALD and other deposition processes were shown in Table 3.1.

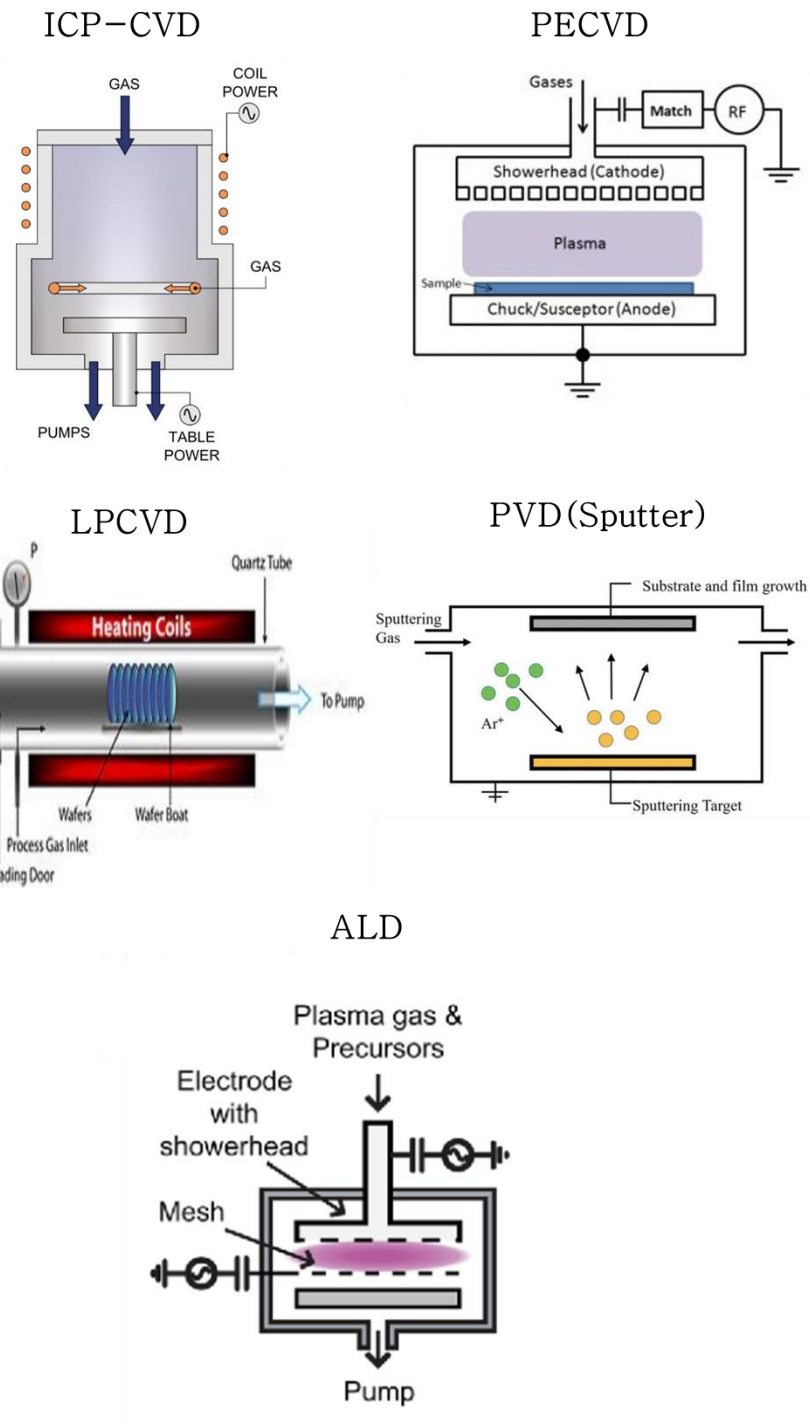


Fig. 3.1 Various deposition processes for gate dielectrics

Properties	PVD	CVD	ALD
Uniformity	~80 Å range	~10 Å range	Å range
Conformity	< 50 %	< 70 %	100%
Cleanliness	Particles	Particles	No Particles
Vacuum	High	High/Med	Medium
Temperature range	Low	Low	Wide
Technology	~100 nm	~90 – 65 nm	No limit

Table 3.1 Comparison of PVD, CVD and ALD

Our ALD dielectrics were deposited with a direct plasma enhanced atomic layer deposition system (PEALD) as shown in Fig. 3.2. It has a showerhead injector and can accommodate 6-inch wafers. The showerhead is capacitively coupled with a RF of 13.56 MHZ and the chuck on which wafers are loaded is grounded. The distance between shower head and chuck is 35 mm. The chamber has a load-lock and is evacuated using a dry pump.

- Capacitively coupled plasma
- RF power, 13.56MHz
- Oxidant: O_3, IPA, O_2
- Precursor: TMA, TEMAHf, BTBAS
- Showerhead type
- One process chamber + one load-lock chamber

Fig. 3.2 Configuration of the PEALD system in ISRC

To deposit ALD SiON, Bis (tertiarybutylamino) silane (BTBAS) and ozone (O_3) were used as the Si precursor and the oxidant, respectively. N_2 plasma process was carried out after ozone step, followed by N_2 gas stabilization step. N_2 purge was performed after precursor injection, the oxidant process and N_2 plasma process. The temperature of BTBAS and chuck were maintained at 75 ℃ and 300 ℃, respectively.

HfON was deposited using Tetrakis(ethylmethylamido)hafnium (TEMAHf), ozone and N_2 plasma. The ALD process of HfON was similar to the ALD process of SiON. Likewise, a cyclic nitrogen plasma step was added after ozone step and N_2 purge was performed after precursor injection, the oxidant process and N_2 plasma process. The temperature of TEMAHf and chuck were maintained at 75 ℃ and around 280 ℃, respectively. The schematic of the ALD process for SiON and HfON was shown in Fig. 3.3.

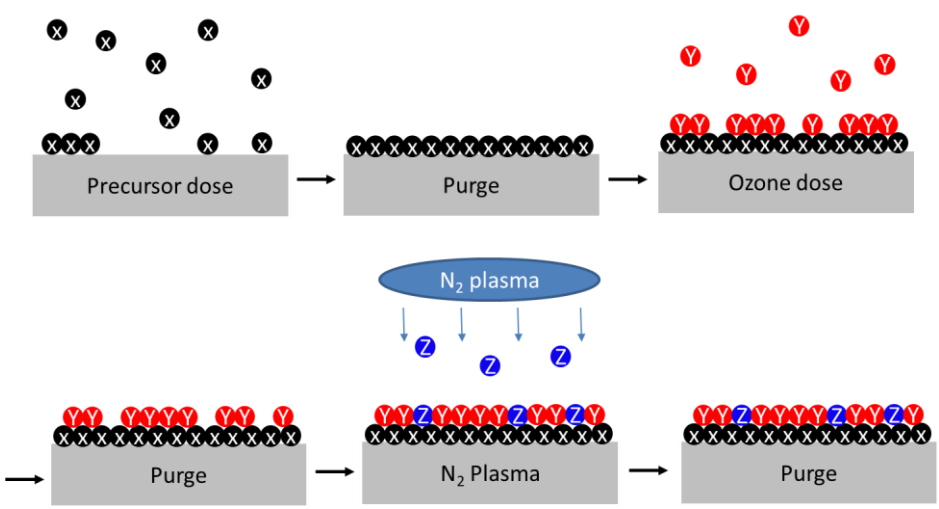
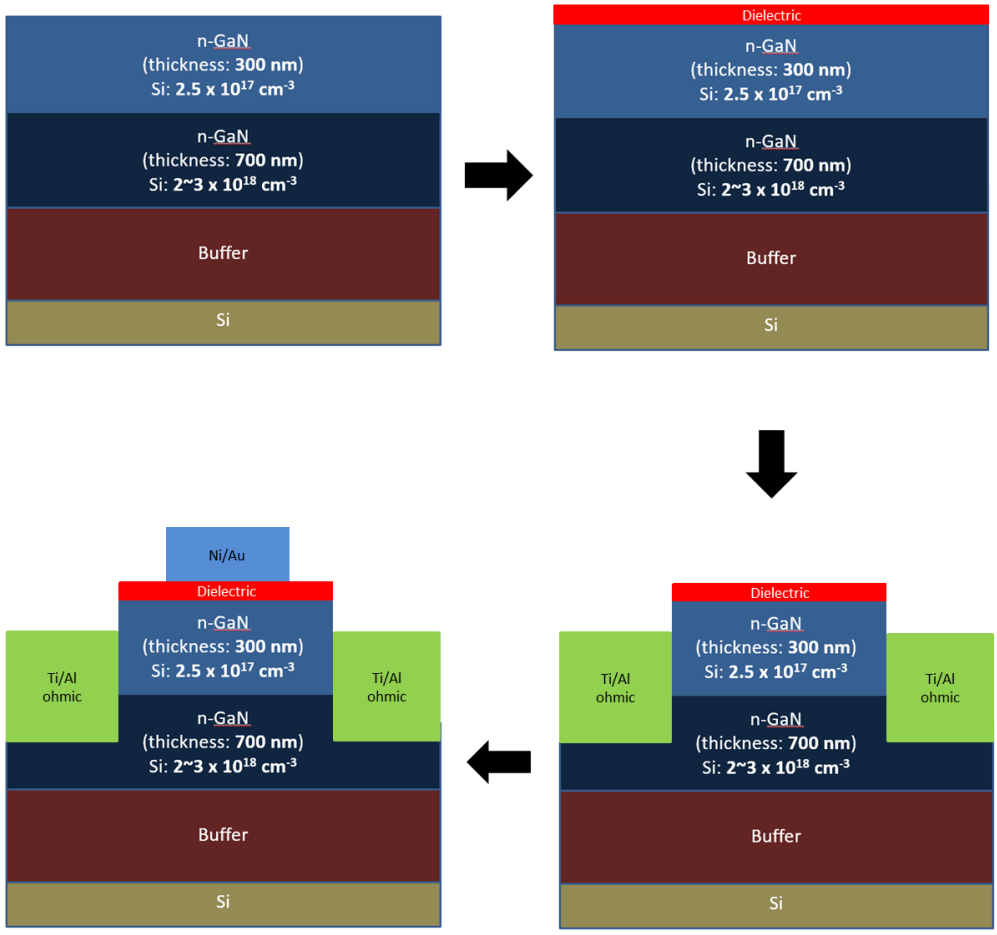


Fig. 3.3 Schematic of one deposition cycle of ALD SiON and HfON

3.3. Electrical Characteristics of ALD SiON, HfON and SiON/HfON Dual Layer on n-GaN

To investigate the electrical properties of SiON, HfON and SiON/HfON dual layer, we fabricated MIS capacitors with a n-GaN epi wafer. The epitaxial layers consisted of a 300 nm n-GaN with 2.5E+17cm^{-3} Si doping concentration, a 700 nm n-type GaN layer, a 700 nm n-GaN with 2~3E+18cm^{-3} Si doping concentration and a 3900 nm GaN buffer layer were grown on Si substrate.

For excellent MIS characteristics, pretreatments are performed before dielectric deposition. First, to remove organic materials, including remaining photoresist, all samples were cleaned with SPM (H_2SO_4:H_2O_2 = 4:1) for 10 minutes at 80 ℃, followed by deionized water (DI) rinse [24-25]. Then, samples were dipped in dilute HF (HF: DI H_2O = 1:10) for 5 minutes to remove native oxides on the surface [36-27]. After that, 11.8 nm SiON, 20.8 nm HfON and 5 nm SiON/15 nm HfON dual layer were deposited on each sample. Post deposition annealing (PDA) was carried out at 500 ℃ in N_2 ambient for 10 minutes. After ohmic patterning and ohmic recess, ohmic contacts were formed with Ti/Al (40/200 nm) metallization. Annealing for ohmic contact formation was carried out at 500 ℃ in N_2 ambient for 1 minute. By using the Ti/Al ohmic contacts, low contact resistance can be obtained at low annealing temperature [28-30]. Finally, Ni/Au (40/130 nm) metal electrode was deposited with e-gun evaporation. The circular metal electrodes had diameters of 100 um or 50 um and was separated by a 10 um gap from a concentric contact. Details for fabrication of the circular MIS capacitors are shown in Fig. 3.4.

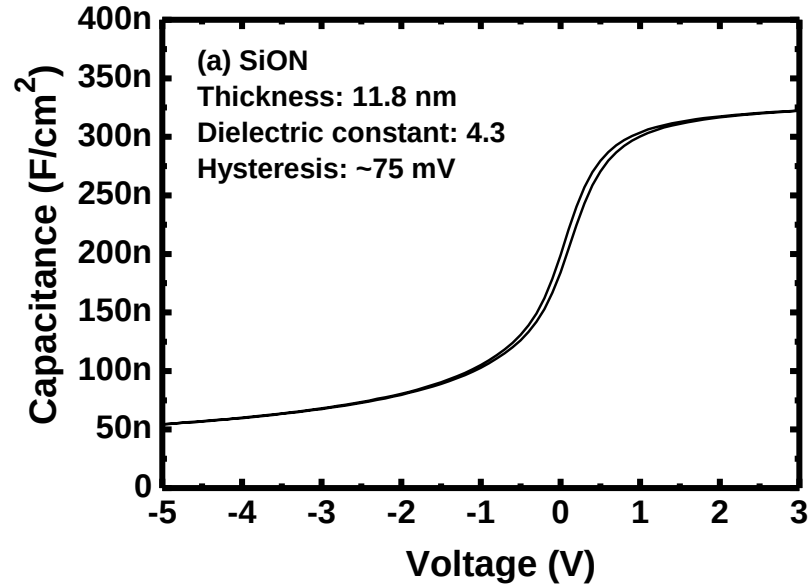


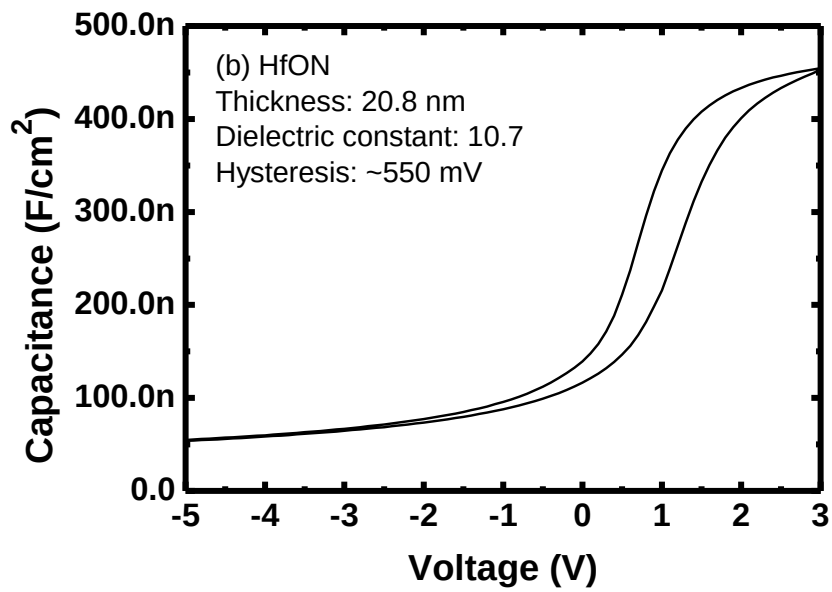
Process flow

- Pretreatment (SPM, DHF)
- ALD dielectric deposition (SiON, HfON, SiON/HfON dual layer)
- Post deposition annealing (500 ℃ for 10 minutes in N_2 ambient)
- Ohmic formation (Ti/Al)
- Gate metallization (Ni/Au)

Fig. 3.4 Process flow of circular MIS capacitors

C-V curves for 11.8 nm SiON, 20.8 nm HfON and 5 nm SiON/15 nm HfON dual layer are shown in Fig. 3.5.





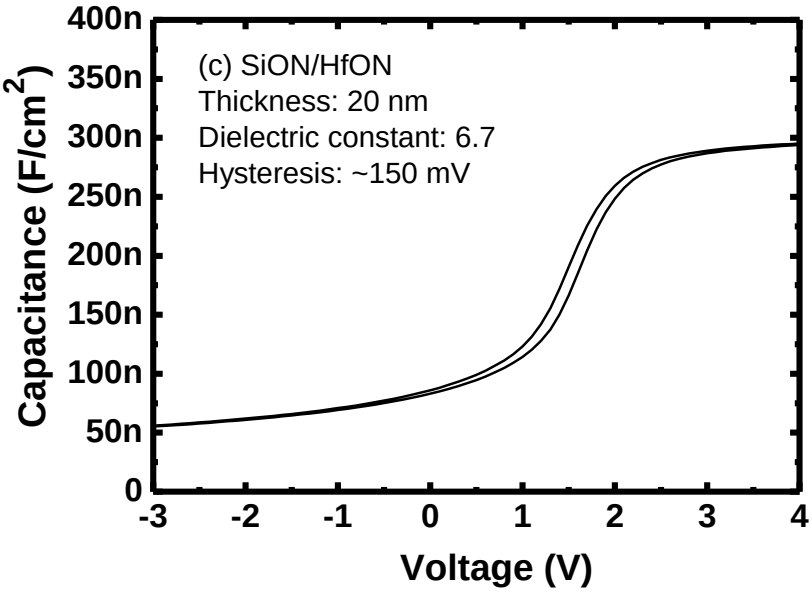
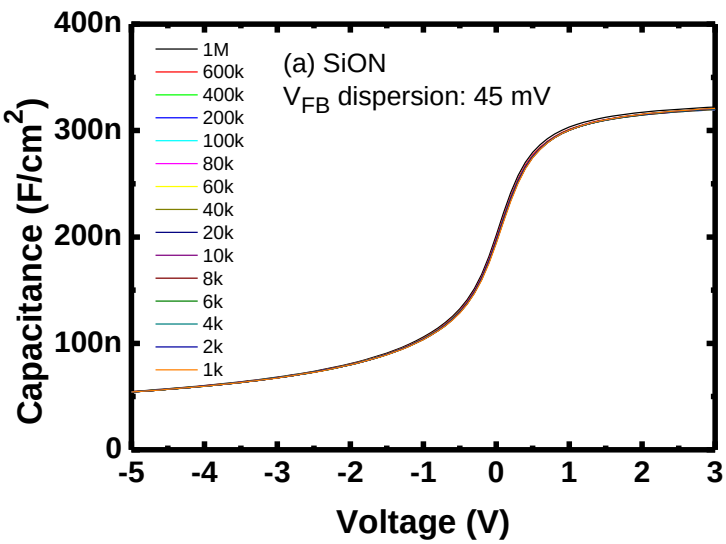


Fig. 3.5 C-V curves of (a) 11.8 nm SiON, (b) 20.8 nm HfON and (c) 5 nm SiON/15 nm HfON on n-GaN at 1MHz

The SiON on n-GaN capacitor showed the lowest amount of hysteresis (~75 mV), whereas the HfON on n-GaN capacitor demonstrated the largest amount of hysteresis (~550 mV). The SiON/HfON on n-GaN capacitor showed lower amount of hysteresis (~150 mV) than that of the HfON on n-GaN capacitor, indicating that SiON efficiently prevent the electron trapping at the SiON/GaN interface [31]. In addition, a higher dielectric constant was obtained by using the SiON/HfON layer compared to the SiON layer.

To evaluate charge trapping at the dielectric/GaN and in the dielectric layer, we also measured C-V curves with multi frequency range from 1 MHz to 1 KHz as shown in Fig. 3.6 [32]. The magnitude of AC signal was 25 mV. The C-V curves of the SiON/HfON on n-GaN sample showed the

smallest V_{FB} dispersion (10 mV) that is comparable to V_{FB} dispersion of the SiON on n-GaN sample (45 mV). The C-V curves of the HfON on n-GaN sample showed the largest V_{FB} dispersion (125 mV). It is assumed that the SiON/HfON sample has smaller density of interface defect states and trap sites in the dielectric than those of the HfON sample.



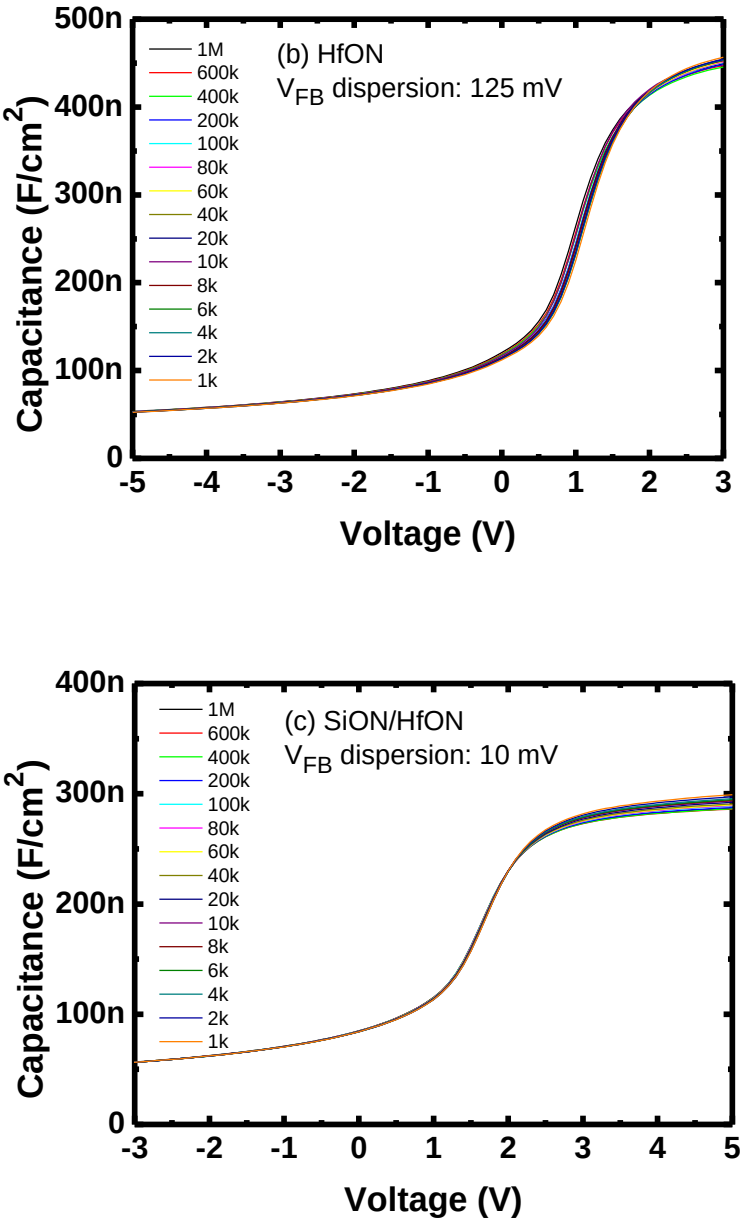
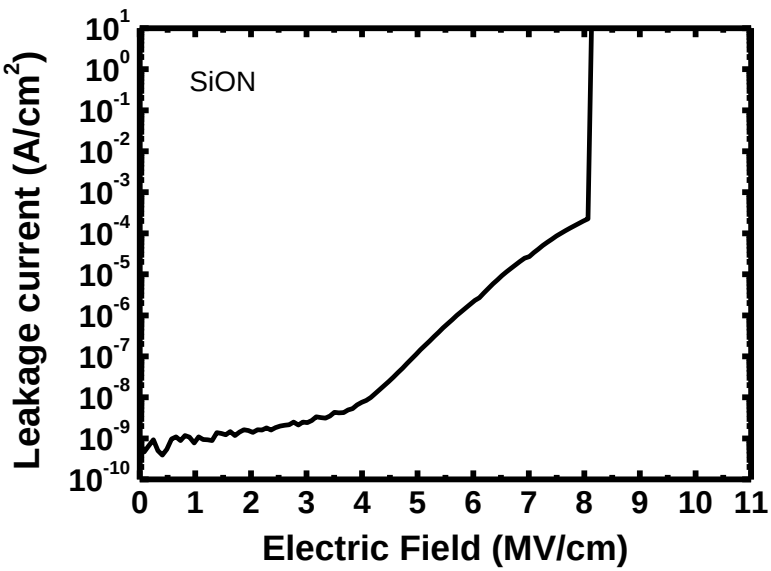


Fig. 3.6 C-V curves with multi frequency range from 1 MHz to 1 KHz of (a) SiON, (b) HfON and (c) SiON/HfON on n-GaN

Fig. 3.7 shows current density-electric field (J-E) characteristics of the fabricated dielectric on n-GaN capacitors. An outstanding improvement of leakage current and breakdown field was observed in the SiON/HfON sample. The breakdown field of the SiON/HfON layer was 6.8 MV/cm which was higher than that of the HfON (3.1MV/cm) and comparable to that of the SiON (8.1MV/cm). It was attributed to the high breakdown field characteristics of SiON [33]. High breakdown field and dielectric constant, low leakage current and high-quality dielectric/GaN interface can be achieved by employing the SiON/HfON dual layer.



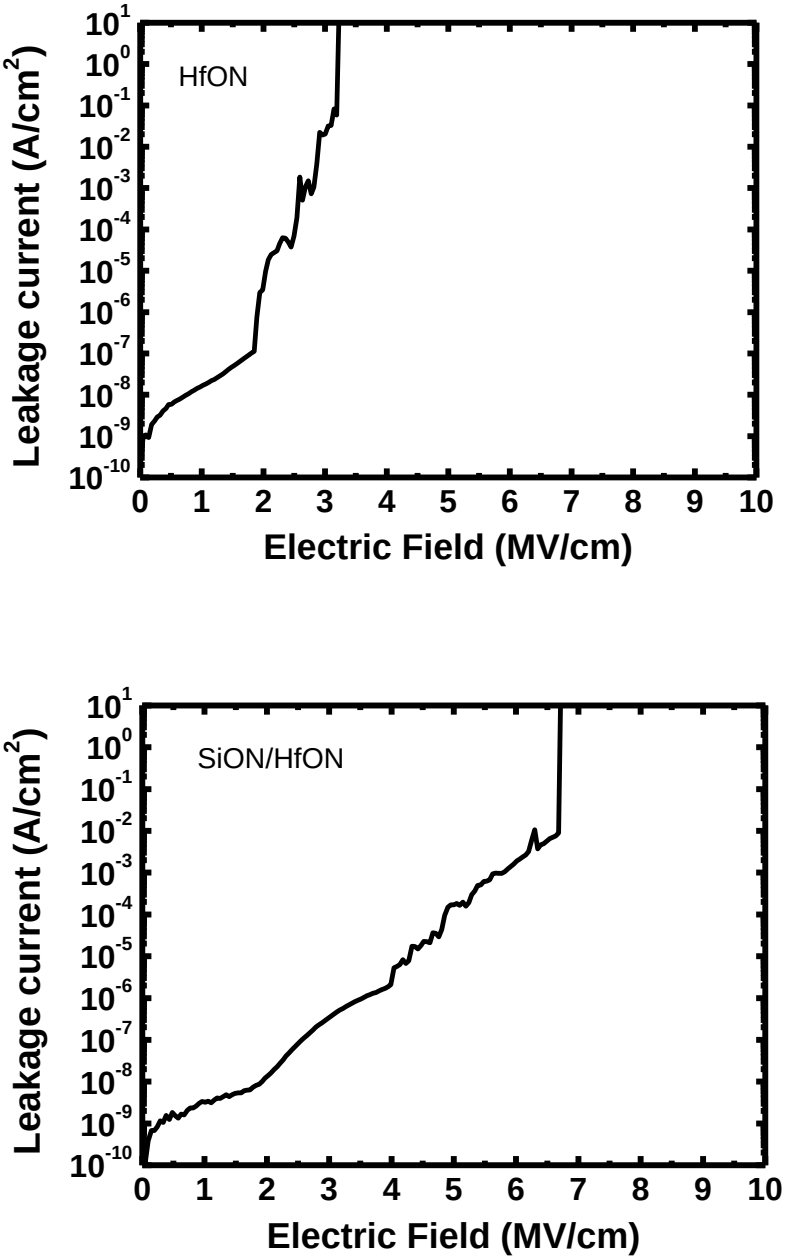


Fig. 3.7 J-E curves of the fabricated dielectric on n-GaN capacitors

3.4. Device Characteristics of Normally-off AlGaN/GaN MIS-FETs with SiON/HfON dual layer

The SiON/HfON dual layer as a gate insulator has been studied using the MIS capacitors in the previous chapter. The high-quality SiON/HfON dual layer showed low excellent leakage current, high dielectric constant and excellent dielectric/GaN interface characteristics compare to the SiON and HfON. However, study of MIS capacitors provides limited information of the actual AlGaN/GaN MIS-FETs.

We fabricated E-mode AlGaN/GaN MIS-FETs with atomic layer deposited 5 nm SiON/16 nm HfON. E-mode AlGaN/GaN MIS-FETs with atomic layer deposited 22 nm HfON gate insulator were also fabricated for comparison. Fig. 3.8 shows the cross-sectional schematics of the fabricated AlGaN/GaN MIS-FETs. The epitaxial layer structure consists of 10 nm SiN in situ capping layer, 3.8 nm GaN interlayer, 22.1 nm undoped AlGaN barrier layer, GaN channel, and buffer on Si (111) substrate.

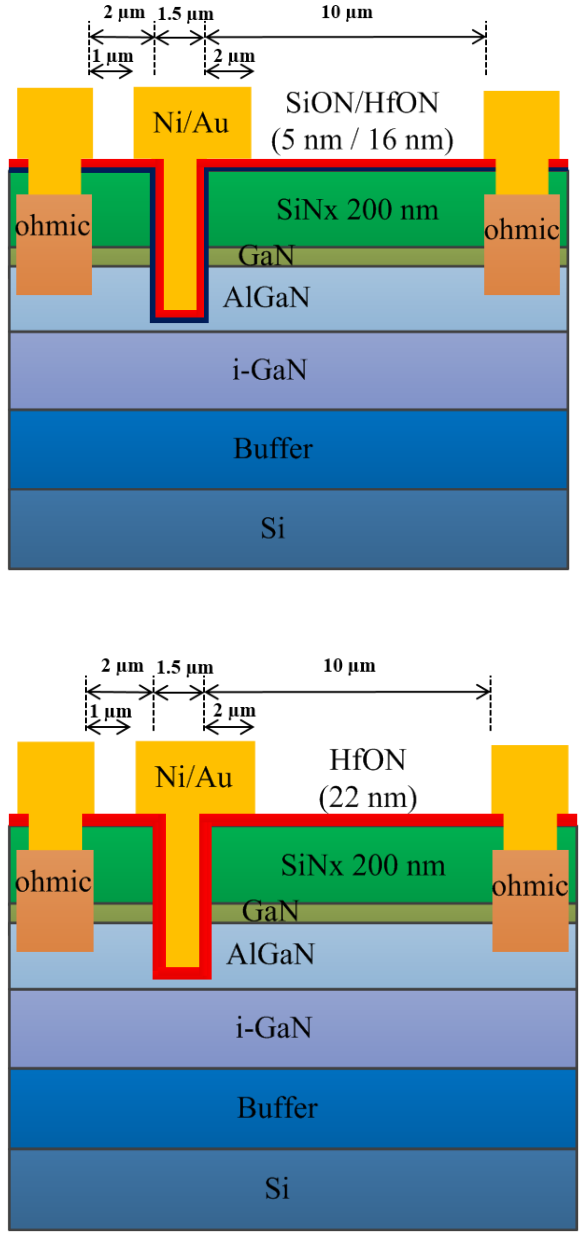


Fig. 3.8 Cross-sectional views of gate recessed AlGaN/GaN MIS-FETs with 5 nm SiON/16 nm HfON and with 22 nm HfON

The device fabrication was begun by solvent cleaning using acetone, methanol and isopropanol. Then, SiN_x passivation layer was deposited using inductively coupled plasma chemical deposition (ICP-CVD) [34]. Ohmic contacts were formed with Ti/Al/Ni/Au metallization and RTA annealing at 830 ℃ in N_2 ambient. The contact resistance measured using the transmission line method (TLM) with contact spacings of 2, 4, 6, 8 and 12 um was 0.7 Ω·mm. Mesa isolation was performed by etching 400 nm depth with Cl_2/BCl_3-based inductively coupled plasma reactive ion etching (ICP-RIE). 200 nm SiNx film was re-deposited on the entire surface. After the gate-recess patterning and SiNx opening with SF_6 based reactive ion etching (RIE) at a low RF power of 20 W, the gate recess was carried out using Cl_2/BCl_3-based inductively coupled plasma reactive ion etching (ICP-RIE). High temperature gate recessing at 100 ℃ with optimized etching conditions for reduced self-bias was performed to minimize the surface etching damage. ~2 nm AlGaN barrier layer was left, which was confirmed by observing the etched depth of the co-processed dummy sample using atomic force microscope (AFM).

The wafer was cleaned with a sulfuric acid peroxide mixture and diluted HF acid after the gate recess etching to avoid the contamination and to remove the native oxide [35]. Before the deposition of the ALD gate insulator, the quality ALD SiON was deposited at 300 ℃ with N_2 plasma in every atomic layer deposition cycle for nitrogen incorporation. Bis (tertiarybutylamino) silane (BTBAS) and ozone (O_3) were employed as Si precursor and oxidant, respectively. The amount of nitrogen incorporated in ALD SiON was found to be about 7 % from X-ray photoelectron spectroscopy. The details of ALD SiON deposition and the performances of AlGaN/GaN MIS-FETs with ALD SiON gate insulator are reported

elsewhere [36]. Then 16 nm high-k ALD HfON was deposited at 260 °C with tetrakis(ethylmethylamino)hafnium (TEMAH) and ozone as Hf precursor and oxidant, respectively, and with cyclic N_2 plasma for nitrogen incorporation. Post deposition annealing (PDA) was carried out at 500 °C in N_2 ambient for 10 minutes. Ni/Au (40 nm/250 nm) gate metal was deposited with e-gun evaporation. Finally, post metallization annealing (PMA) was carried out at 400 °C in forming gas ambient, H_2 (5%) + N_2 (95%) for 10 minutes. AlGaN/GaN E-mode MIS-FET with ALD HfON of 22 nm was also fabricated with the otherwise identical process as the reference device. The schematic of the process flow of the gate recessed MIS-FETs are depicted in Fig. 3.9.

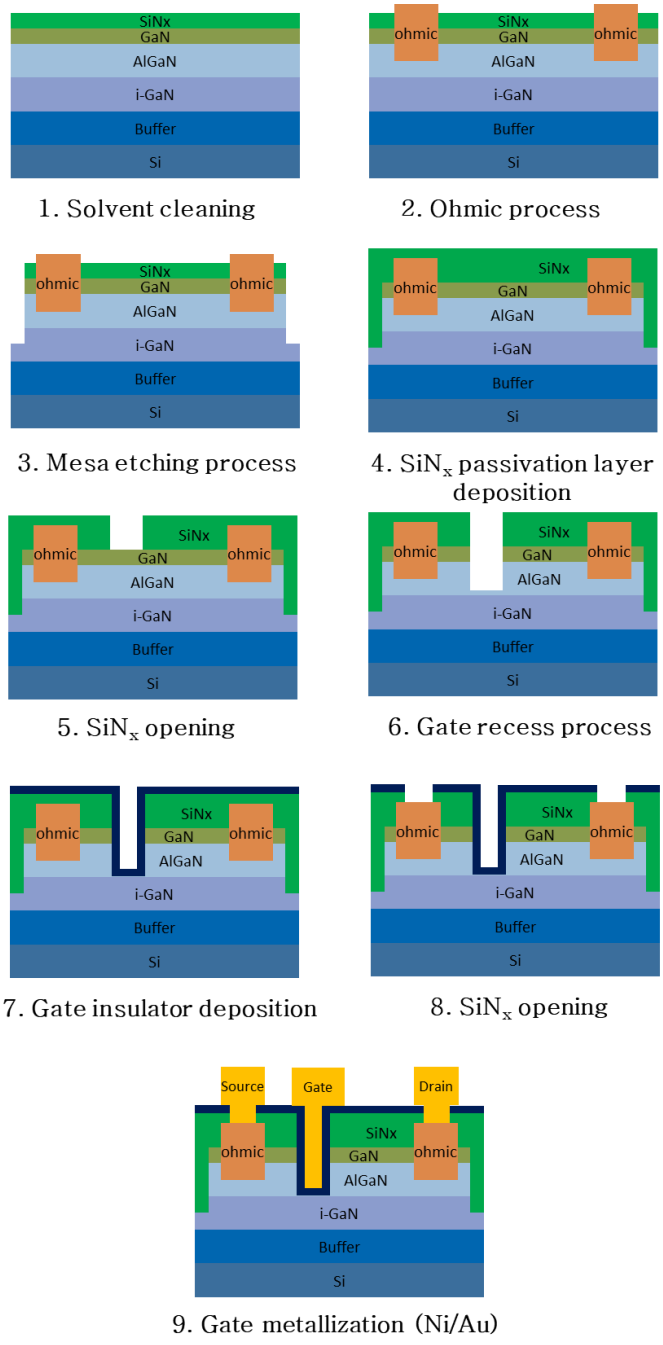


Fig. 3.9 Schematic of the process flow of the gate recessed MIS-FETs

Fig. 3.10 shows the transfer characteristics of the fabricated AlGaN/GaN MIS-FETs. Threshold voltage of 1.1 V determined by linearly extrapolation of the drain current-gate voltage curve was obtained for the MIS-FETs with atomic layer deposited 5 nm SiON/16 nm HfON. The maximum drain current and transconductance were 602 mA/mm and 145 mS/mm, respectively. The off-state drain leakage current was very low (less than 10^{-11} A/mm), which resulted in an excellent on-off current ratio (1.2 x 10^{11}). A very small gate leakage current of 5 x 10^{-11} A/mm was also obtained at V_{GS} of 6 V as shown in Fig. 3.11. It was attributed to the large conduction band offset of ALD SiON, for which we estimated a large value of 3.37 eV on a recessed GaN surface [36].

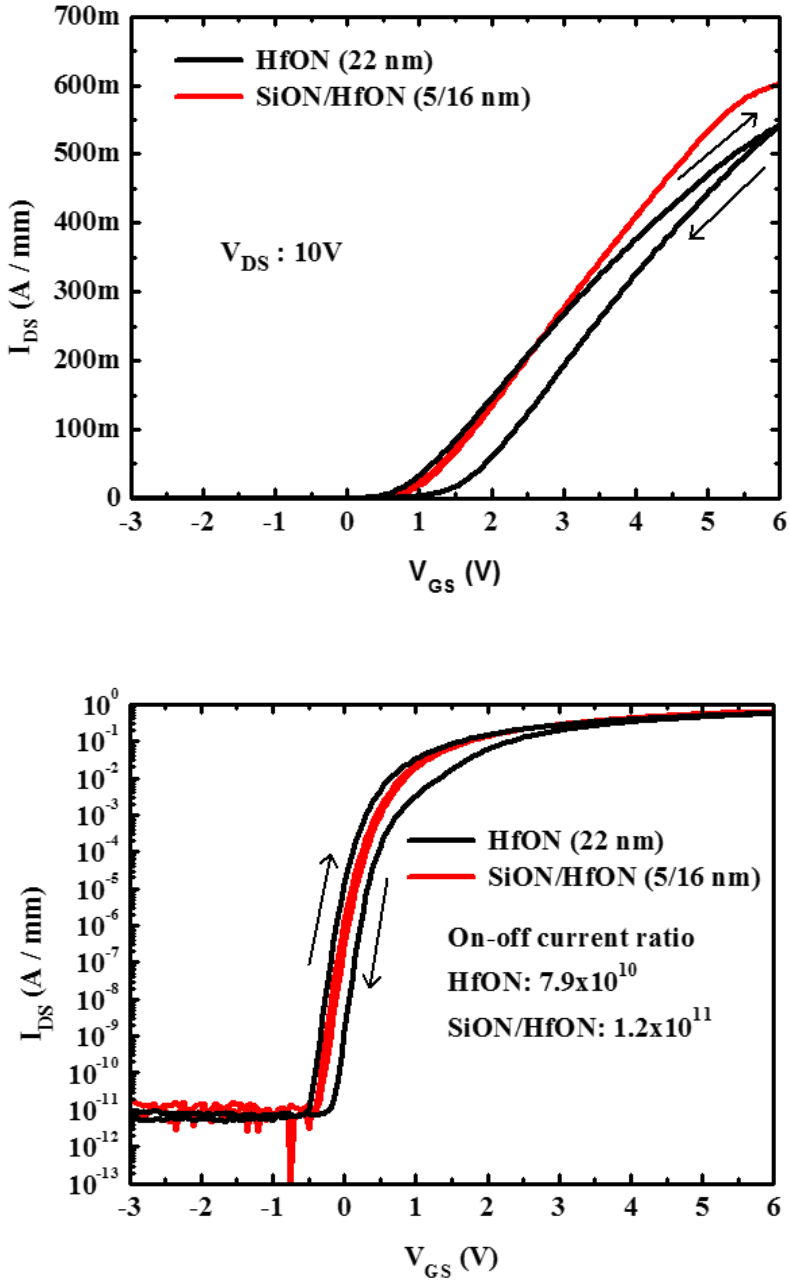


Fig. 3.10 Transfer characteristics of gate recessed AlGaN/GaN MIS-FETs with 22 nm HfON and with 5 nm SiON/16 nm HfON

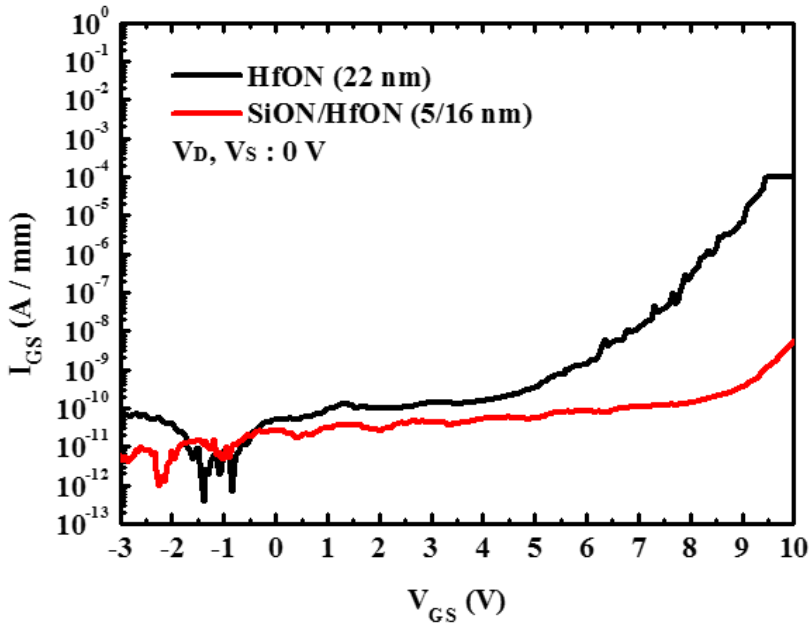


Fig. 3.11 Gate leakage current characteristics of gate recessed AlGaN/GaN MIS-FETs with 22 nm HfON and with 5 nm SiON/16 nm HfON

The threshold voltage hysteresis during the gate voltage swing was negligibly small, about 50 mV hysteresis observed with the gate voltage swing up to 6 V. Whereas, the MIS-FETs with 22 nm HfON showed the threshold voltage of 0.8 V, the maximum drain current of 543 mA/mm, and the maximum transconductance of 143 mS/mm. The gate leakage current was higher than one order compared to that of the MIS-FET with 5 nm SiON/16 nm HfON at V_{GS} of 6 V. It was attributed to the small conduction band offset of ALD HfON for which we estimated a small value of 1.4 eV on a recessed AlGaN surface from Fowler-Nordheim plot. In addition, a large threshold voltage hysteresis of 450 mV was observed in the MIS-FET with 22 nm HfON, indicating that the HfON could not effectively suppress

electron trapping.

The interface trap density (D_{it}) extracted by the conductance method and conductance as a function of applied voltage at room temperature are shown in Fig. 3.12. D_{it} values were extracted from 0 to 0.5 V for MIS-FET with 22 nm HfON and from -0.1 to 0.4 V for MIS-FET with 5 nm SiON/16 nm HfON. The D_{it} values of SiON/HfON MIS-FET were less than those of HfON MIS-FET within the overall trap level range of 0.3 ~ 0.44 eV. The D_{it} was also evaluated from subthreshold swing values obtained from I-V characteristics [37]. The measured subthreshold swing value for the MIS-FET with 22 nm HfON was 79 mV/dec and the extracted D_{it} values were 1.1 x 10^{12} cm^{-2} eV^{-1}. Whereas, the measured subthreshold swing value for the MIS-FET with 5 nm SiON/16 nm HfON was 77 mV/dec, and the extracted D_{it} values were 7.9 x 10^{11} cm^{-2} eV^{-1} at room temperature.

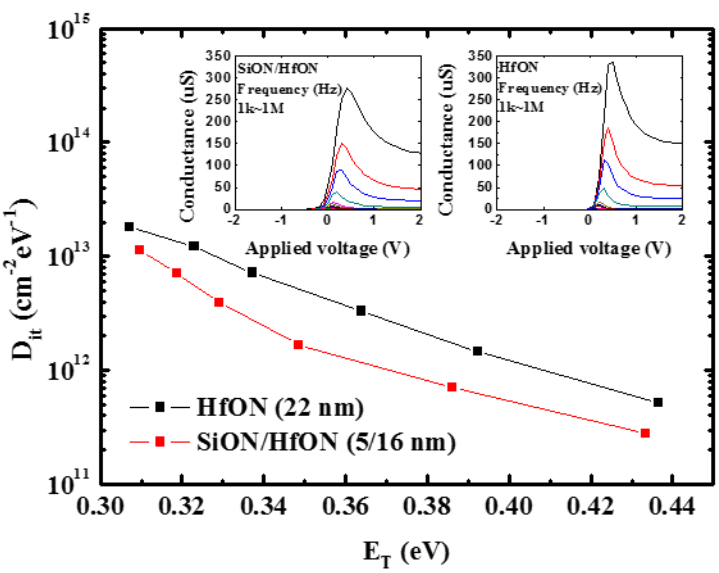


Fig. 3.12 Interface trap density extracted using the conductance method. The measured conductances were shown in the insets

The effective mobility was extracted from the measured conductance for the normally-off GaN channel of a FAT-FET with a gate length of 100 um. As shown in Fig. 3.13, the maximum effective mobility value was 887 $cm^2/V{\cdot}s$ for the MIS-FET with 5 nm SiON/16 nm HfON, which was as high as other E-mode GaN FETs with partially recessed MIS-gate structure [38]. The high value of field-effect mobility for the MIS-FET with 5 nm SiON/16 nm HfON was attributed to the low damage gate recess process with high temperature ICP–RIE and the high-quality SiON interfacial layer.

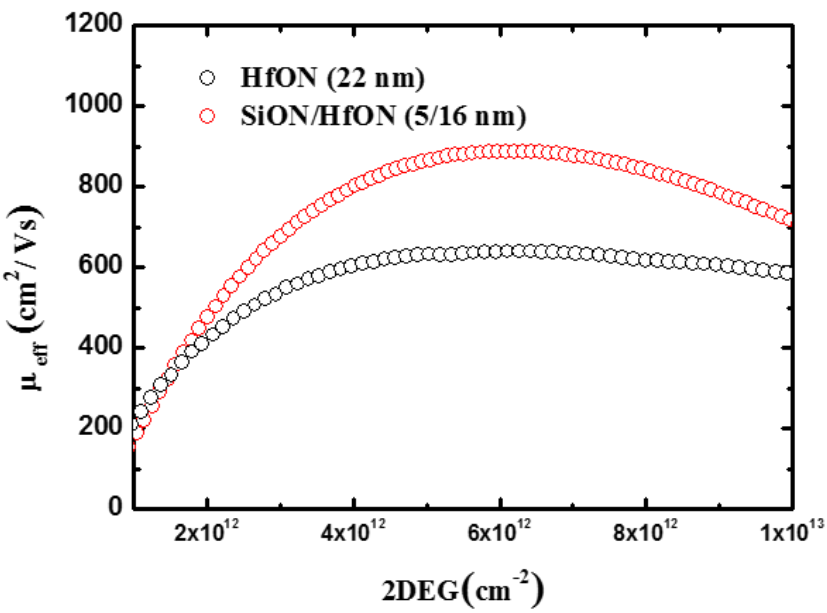


Fig. 3.13 Effective mobility in the normally-off GaN channel of a FAT-FET with a gate length of 100 μm with 22 nm HfON and with 5 nm SiON/16 nm HfON

In order to investigate the dynamic switching characteristics associated with electron trapping, pulsed I-V and dynamic Ron measurements were

made. As shown in Fig. 3.14, we measured on-wafer pulsed I-V at two initial bias conditions of (V_{GSQ}, V_{DSQ}) = (0 V, 0 V) and (V_{GSQ}, V_{DSQ}) = (0 V, 60 V). The pulse width was 1 μs with a duty cycle of 0.1 %. No special process was made for the back-side thermal contact. For the MIS-FET with 5 nm SiON/16 nm HfON, the maximum drain current at V_{GS} of 6 V and the bias condition of (V_{GSQ}, V_{DSQ}) = (0 V, 60 V) was 684 mA/mm, which was only 7.2 % lower than that of (V_{GSQ}, V_{DSQ}) = (0 V, 0 V). However, much larger current collapse occurred in the MIS-FET with 22 nm HfON. There is a significant current difference between DC and pulsed (0, 0) curves in HfON MIS-FET. It is considered that this is due to the self-heating [39] and trapping effect at the HfON/AlGaN.

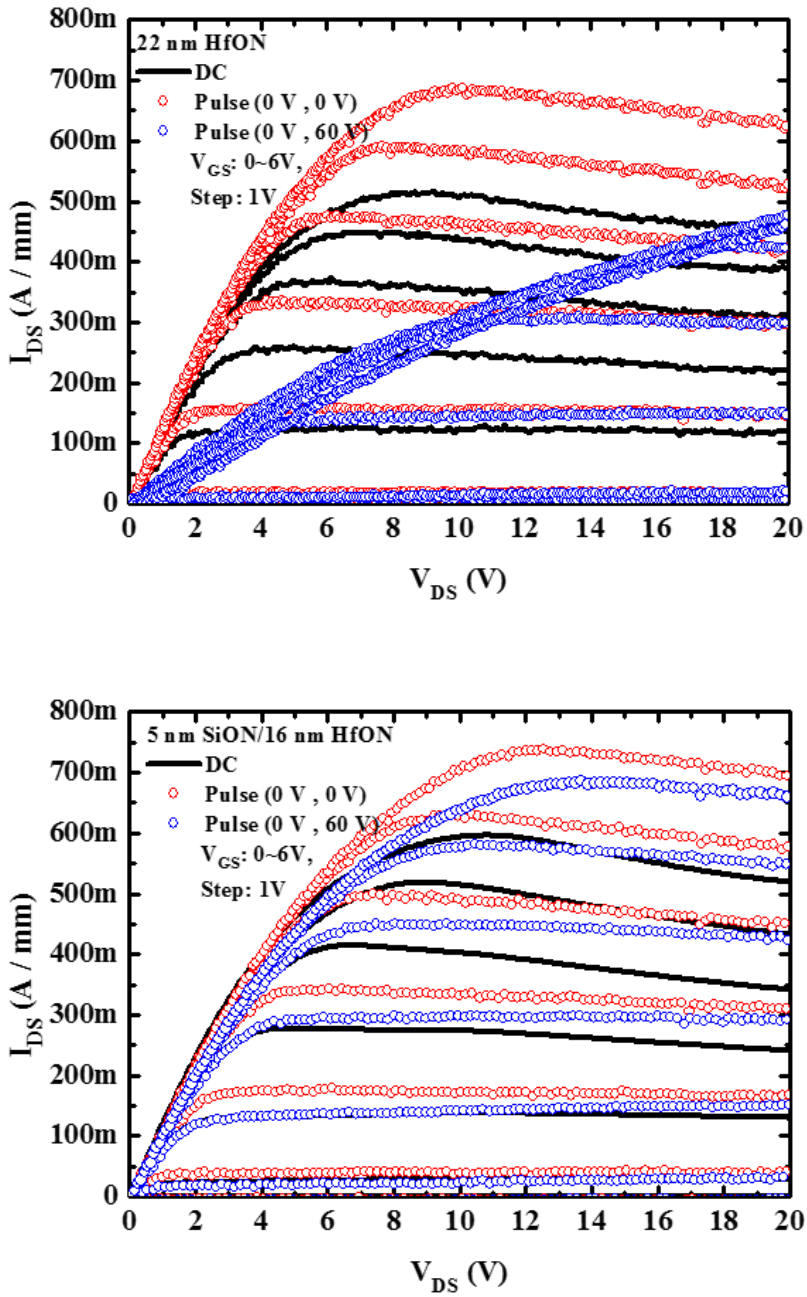


Fig. 3.14 Pulsed I-V characteristics of gate recessed AlGaN/GaN MIS-FETs with 22 nm HfON and with 5 nm SiON/16 nm HfON.

Fig. 3.15 shows the measurement results for the dynamic on-resistance (R_{on}). The measurement frequency was 10 KHz with a duty cycle of 50 %. The off-state drain bias was applied up to 200 V for the MIS-FET with 5 nm SiON/16 nm HfON. For the MIS-FET with 22 nm HfON, maximum drain bias was limited to 100 V due to enhanced charge trapping in HfON. The dynamic R_{on} was only 1.43 times higher than the static R_{on} at the off-state drain bias of 200 V for the MIS-FET with 5 nm SiON/16 nm HfON. The low current collapse and small variation between the dynamic R_{on} and the static R_{on} in the MIS-FET with 5 nm SiON/16 nm HfON indicate that the fabricated device had high-quality interface characteristics with a SiON interfacial layer, which led to very small electron trapping [13].

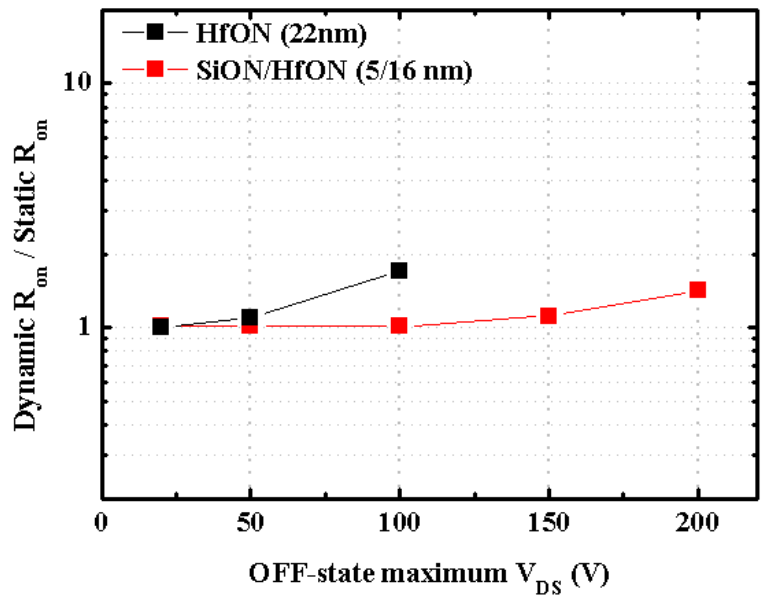


Fig. 3.15 Dynamic on-resistance characteristics of gate recessed AlGaN/GaN MIS-FETs with 22 nm HfON and with 5 nm SiON/16 nm HfON

The off-state I-V characteristics of the fabricated devices are shown in Fig. 3.16. For the MIS-FET with 5 nm SiON/16 nm HfON, the measured breakdown voltage was 800 V with V_{GS} = 0 V and the drain leakage current of 1.6 μA/mm.

Fig. 3.17 shows the specific on-resistance (specific on-resistance extracted from the I–V characteristics by using the active area between the source and drain contacts) versus the breakdown voltage for the fabricated devices, including other results reported for E-mode GaN MIS-FETs [38], [40]-[46]. Compared to the previous results, E-mode AlGaN/GaN MIS-FET with 5 nm SiON/16 nm HfON fabricated in this study exhibited the excellent performances.

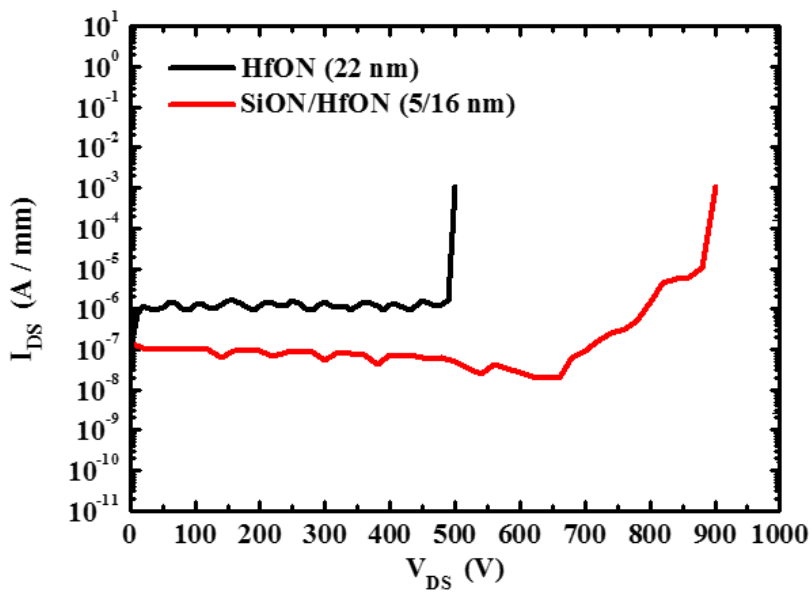


Fig. 3.16 Off-state I-V characteristics at V_{GS} = 0 V for gate recessed AlGaN/GaN MIS-FETs with 22 nm HfON and with 5 nm SiON/16 nm HfON

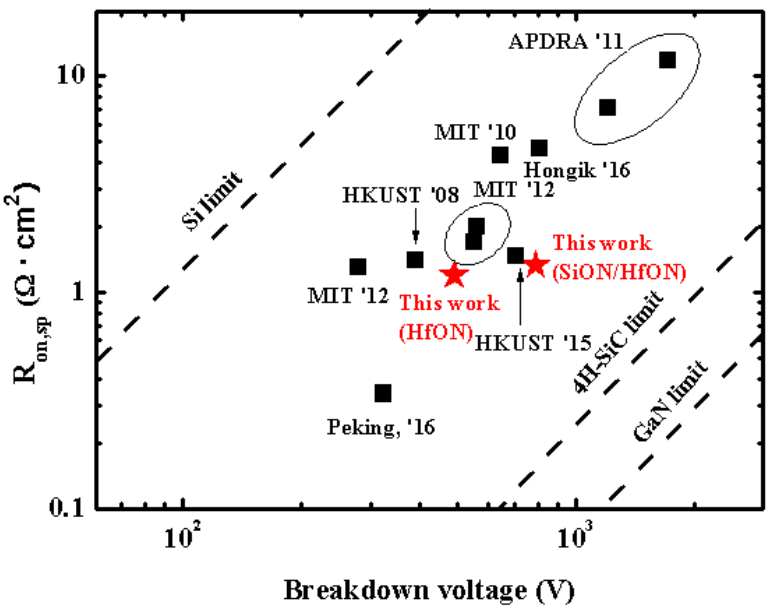


Fig. 3.17 Benchmark of breakdown voltage and specific R_{on} for gate recessed AlGaN/GaN MIS-FETs

In recent years, threshold voltage instability has been considered as one of the most important reliability issues in AlGaN/GaN MIS-FETs. This phenomenon is known to be caused by interface traps at the dielectric/III-N interface, border traps and bulk traps in the dielectric [47]. The threshold voltage was measured at 1, 10, 100, 1000 s under the gate bias stress of 3.5 V at room temperature and at 150 ℃. As shown in Fig. 3.18, for the MIS-FET with 5nm SiON/16 nm HfON, the threshold voltage drift of 74 mV was measured after the stress time of 1000 s at room temperature. At 150° C, the threshold voltage drift of 252 mV was measured after the stress time of 1000 s. It should be stressed that the observed threshold voltage drifts for the MIS-FET with 5 nm SiON/16 nm HfON belong to one of the best data

for positive threshold voltage instability (PBTI) in AlGaN/GaN MIS-FETs [10, 47, 48], which is attributed to the high quality AlGaN/dielectric interface and the large conduction band discontinuity provided by ALD SiON interfacial layer. Whereas, for the MIS-FET with 22 nm HfON, much larger threshold voltage drift was measured at room temperature and 150 ℃.

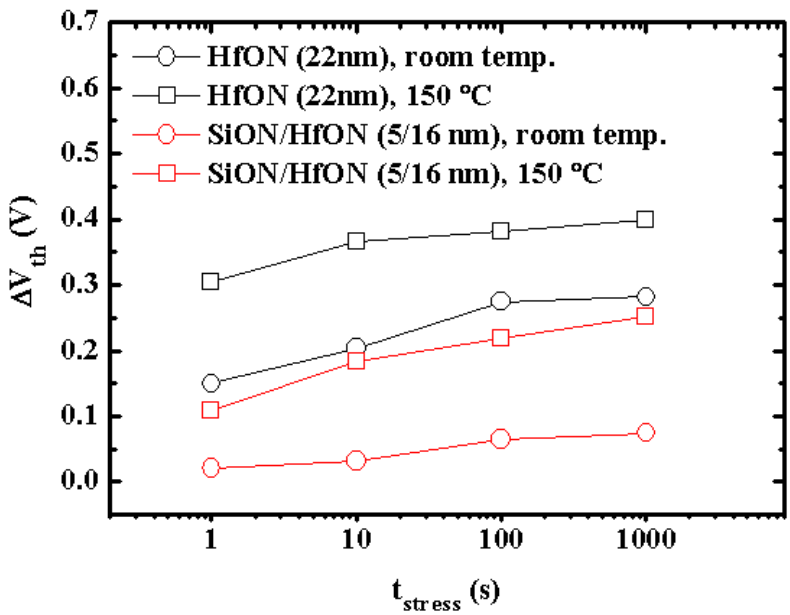
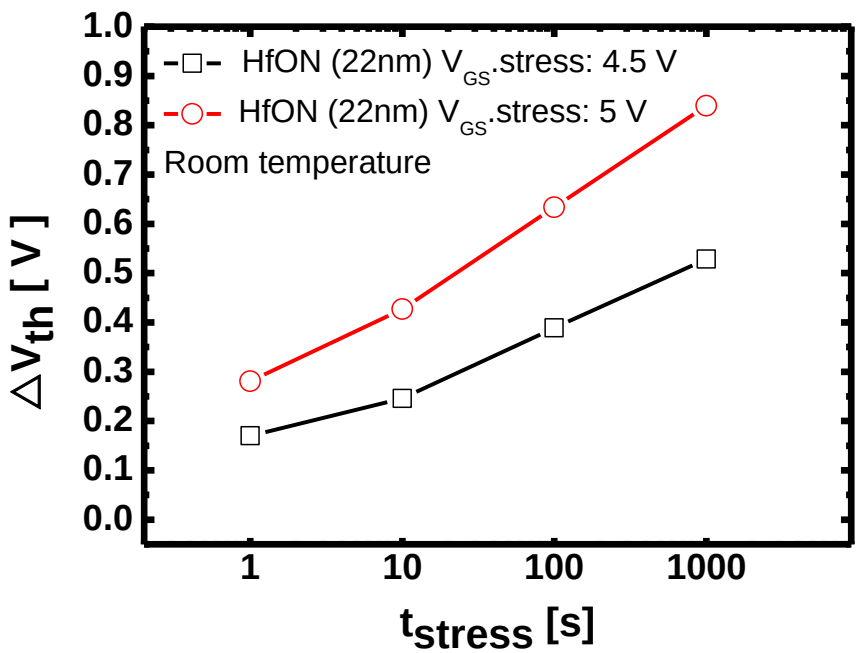


Fig. 3.18 Threshold voltage instability of gate recessed AlGaN/GaN MIS-FETs with 22 nm HfON and with 5 nm SiON/16 nm HfON under positive gate bias of 3.5 V and various stress time

The threshold voltage was also measured under the higher gate bias stress of 4.5 and 5 V at room temperature. As shown in Fig. 3.19, for the MIS-FET with 5nm SiON/16 nm HfON, the threshold voltage drift of ~550 mV was measured after the stress time of 1000 s at room temperature. However, for the MIS-FET with 22 nm HfON, larger threshold voltage drift of ~840 mV was measured at room temperature. Even at the higher gate bias, SiON could reduce the electron trapping in defects located at the dielectric/AlGaN interface and the bulk high-k dielectric. However, more efforts to reduce electron trapping were needed for stable operation of the devices.



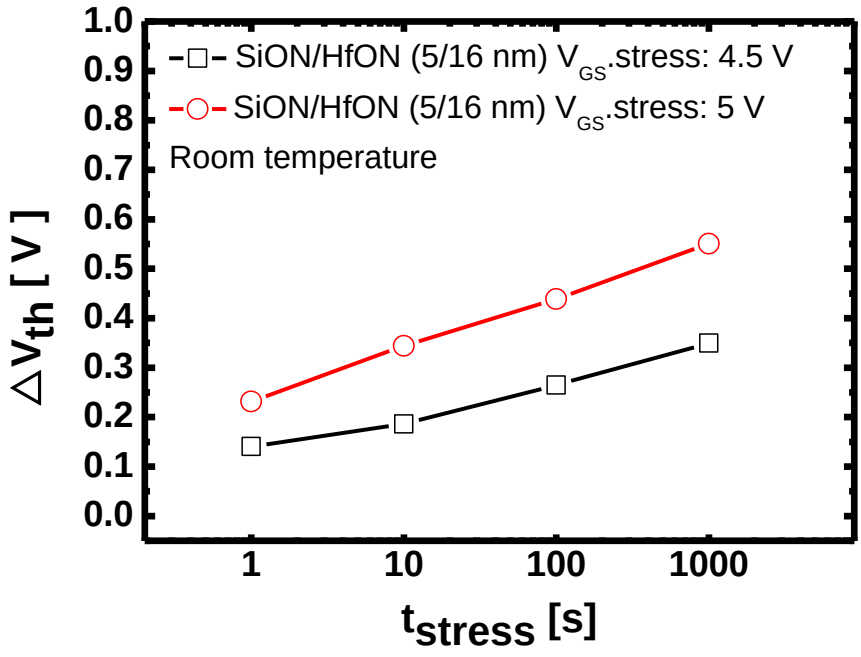


Fig. 3.19 Threshold voltage instability of gate recessed AlGaN/GaN MIS-FETs with 22 nm HfON and with 5 nm SiON/16 nm HfON under positive gate biases of 4.5 and 5 V and various stress time

3.5. Conclusion

In this chapter, SiON/HfON as a gate dielectric was studied. High breakdown field and dielectric constant, low leakage current and high-quality dielectric/GaN interface can be achieved by employing the SiON/HfON dual layer on n-GaN when compared to SiON and HfON on n-GaN. Also, we fabricated high-performance E-mode AlGaN/GaN MIS-HEMTs with atomic layer deposited 5 nm SiON/16 nm HfON and with atomic layer deposited 22 nm HfON gate insulator and compared their characteristics. Plasma nitridation was employed in every atomic layer deposition cycle to deposit SiON and HfON dielectrics. SiON was used as an interfacial layer to ensure a high-quality AlGaN/dielectric interface, and high-k HfON was employed to realize a large transconductance, a high on-state current, and a high on/off current ratio. The fabricated device with SiON/HfON showed a high on/off current ratio of ~1.2 x 10^{11}, a low off-state drain leakage current less than 10^{-11} A/mm, and a maximum drain current of 602 mA/mm. The device also exhibited excellent pulsed I-V and dynamic on-resistance characteristics. In addition, small threshold voltage drift under positive gate bias stress was achieved due to the SiON interfacial layer. However, considerable threshold voltage drift was observed under the higher positive gate bias stress even at the devices using SiON/HfON dual layer. More efforts to reduce electron trapping under high positive gate bias stress are needed for stable operation of devices.

3.6. References

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Chapter 4. High Quality AlN/AlON/AlHfON Gate Dielectric Layer by ALD for AlGaN/GaN MIS-FETs

4.1. Introduction

For the AlGaN/GaN normally-off MIS-FETs which are for power switching application, high positive gate voltage can easily induce the electrons in the 2DEG channel to enter the high-density deep states at the oxide/III-nitride interface, resulting in the threshold voltage (V_{th}) instability [1]. It has been reported that the poor-quality native oxide (GaO_x) is detrimental to the dielectric/III-V interface quality that accounted for the V_{TH} instability issue in the III-V based devices [2]. Recently, GaAs and InGaAs channels MOSFETs have exhibited good performance when native oxides (GaO_x and AsO_x), which caused Fermi-level pinning, were removed from the channel during oxide deposition [3-4]. Our group reported ALD HfO_2 using isopropyl-alcohol (IPA) as a oxidant during the ALD process of oxide because IPA can efficiently reduce surface oxidation, while O_3 is known to affect the III-V surface during initial deposition cycles neglecting prior surface treatments that easily cause the formation of inferior native

oxides [5-6]. As another method to avoid surface oxidation, employing nitride-based dielectrics such as AlN and SiN_x are more favored because oxidant is not used for nitride-based dielectrics by ALD. Especially, AlN has smaller lattice mismatch between (Al)GaN and AlN compared to that between (Al)GaN and SiN_x [7-8]. Some groups have reported PEALD AlN on (Al)GaN with in situ low-damage plasma pre-treatment that enables to remove the surface native oxide and suppress surface oxidation, resulting in reduction of surface defects and current collapse and reliable device performance [9-11].

Also, high-k dielectrics such as HfO_2, La_2O_3, ZrO_2 and Ta_2O_5 as gate dielectrics have been applied for GaN MIS-FETs [12-15]. They have many advantages for low leakage current, high on-state current and ON/OFF current ratio due to the good channel controllability of high-k dielectrics. From these characteristics, high efficiency and low power loss can be realized in the power switching applications.

4.2. Development of ALD AlN and AlHfON

4.2.1. Process Optimization for ALD AlN

For ALD AlN deposition, a new cluster ALD system was used. The ALD system has two chambers (oxide chamber and nitride chamber), load-lock and transfer chamber which are evacuated using turbo pumps. It has showerhead injectors and can accommodate 6-inch wafers. The showerhead is capacitively coupled with a RF of 27.12 MHZ and the chuck on which wafers are loaded is grounded. The distance between shower head and chuck is 35 mm. The ALD system used for the following experiments of various dielectrics including AlN was shown in Fig. 4.1.

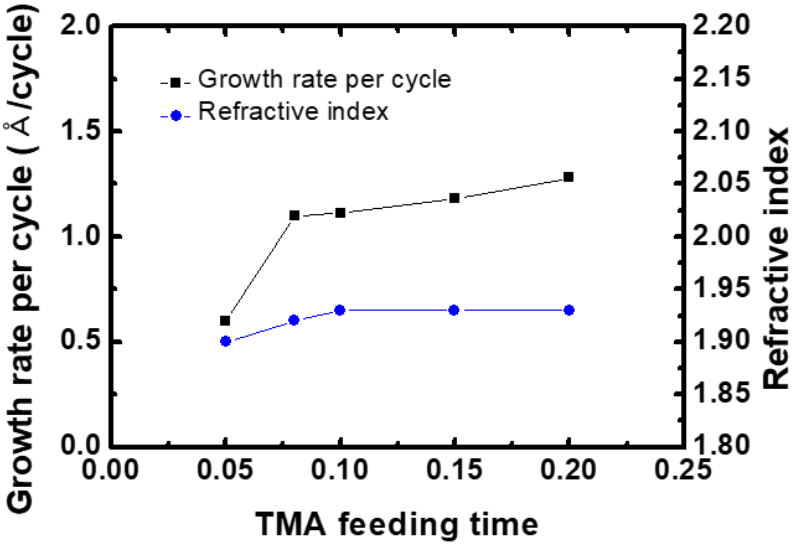
- ✓ Direct RF plasma of 27.12 MHz
- ✓ Two chamber (oxide and nitride chamber) + transfer chamber + loadlock
- ✓ Oxidant: IPA, H_2O, O_2, O_3
- ✓ Shower head type

Fig. 4.1 Configuration of cluster ALD system in ISRC

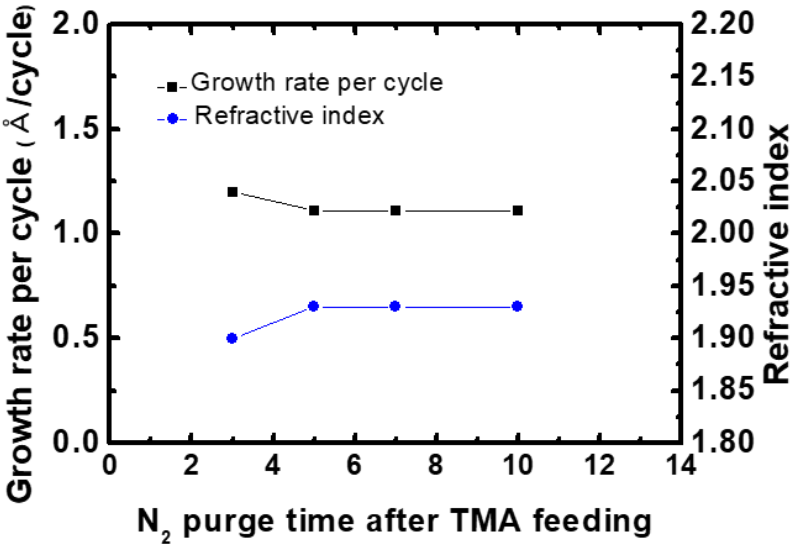
AlN using the new cluster ALD system was deposited on n-type Si (111) and optimized with TMA source as the Al precursor and NH_3 gas as the N precursor. Purge process was carried out using N_2 gas after the TMA precursor injection and NH_3 plasma step. The top lid and wall temperature of the chamber were kept at 150 ℃ to reduce impurities such as carbon and oxygen in the dielectric layer [16]. Gas lines and TMA precursor was kept at 90 and 5 ℃, respectively. The deposition temperature of AlN was at 330 ℃ and the pressures of NH_3 plasma and purge step were 120 and 500 mtorr, respectively.

The growth rate per cycle (GPC) was saturated with increasing TMA feeding and NH_3 plasma times at the deposition temperature. The GPC was saturated at the TMA feeding time of 0.1 sec and NH_3 plasma time of 10 sec and the saturated value was 1.1Å/cycle. the Purge times after the TMA precursor injection and NH_3 plasma step were both chosen to be 10 sec and NH_3 plasma power was 100 W. Details of the ALD process of AlN was described in Fig. 4.2.

(a)


Growth rate per cycle
Refractive index
Growth rate per cycle (Å /cycle)
Refractive index
TMA feeding time
2.0
1.5
1.0
0.5
0.0
2.20
2.15
2.10
2.05
2.00
1.95
1.90
1.85
1.80
0.00
0.05
0.10
0.15
0.20
0.25

(b)


Growth rate per cycle
Refractive index
Growth rate per cycle (Å /cycle)
Refractive index
N2 purge time after TMA feeding
2.0
1.5
1.0
0.5
0.0
2.20
2.15
2.10
2.05
2.00
1.95
1.90
1.85
1.80
0
2
4
6
8
10
12
14

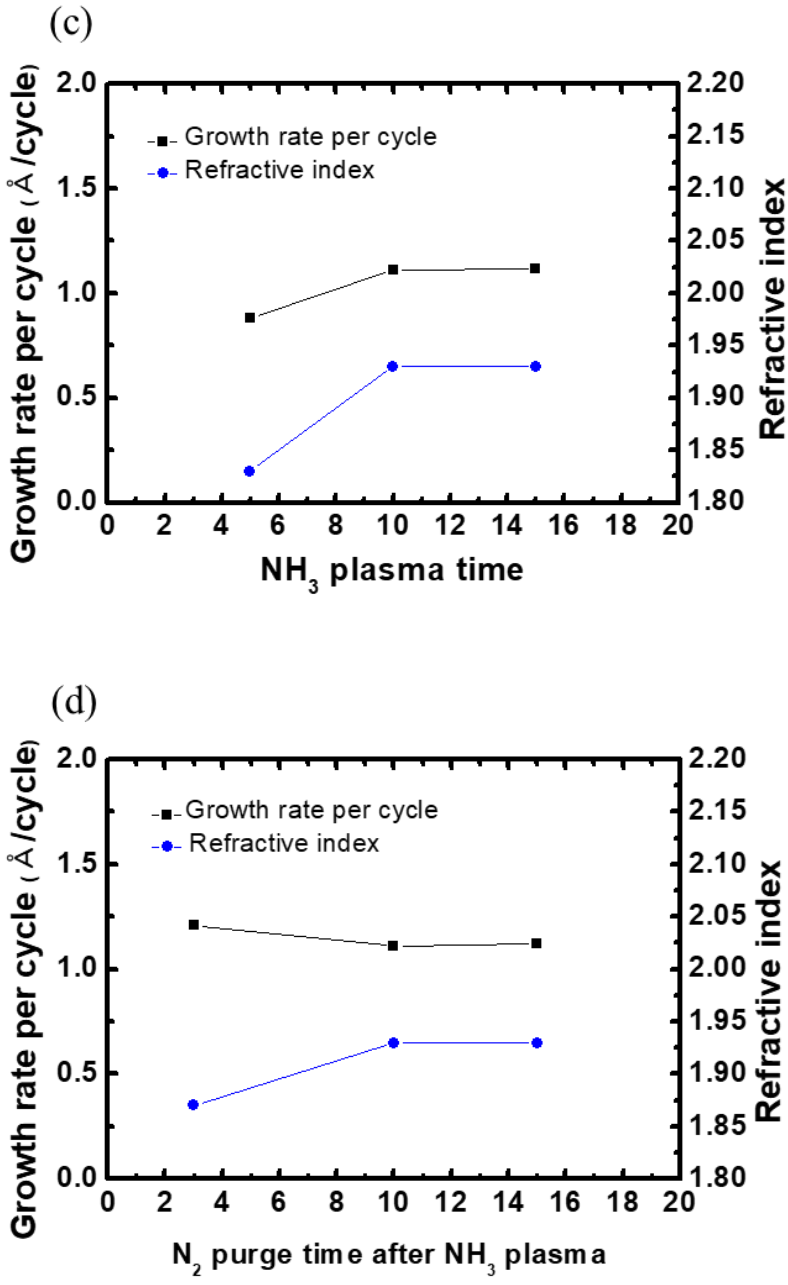


Fig. 4.2 ALD window of ALD AlN. (a) TMA feeding time, (b) N_2 purge time after TMA feeding, (c) NH_3 plasma time and (d) N_2 purge time after NH_3 plasma

Fig. 4.3 shows a linear dependence of the AlN film thickness with the number of ALD cycles. No interface layer appears to be existed between the Si and AlN. It is attributed to the surface oxidation suppression effect of AlN.

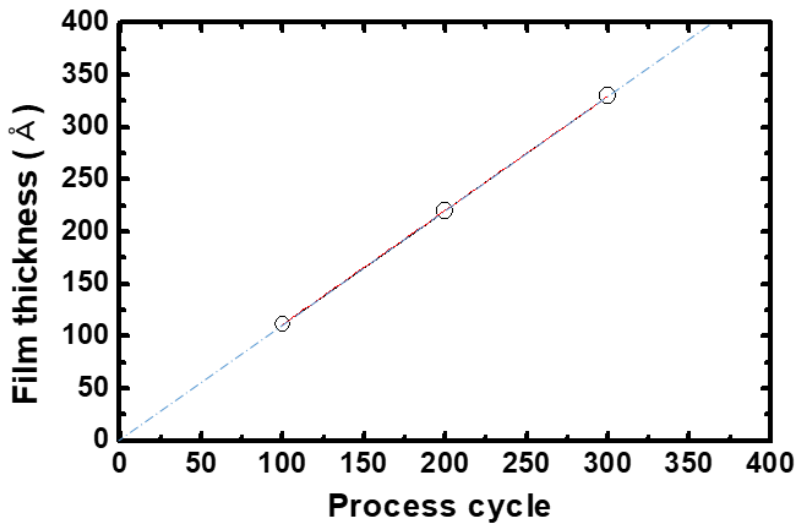
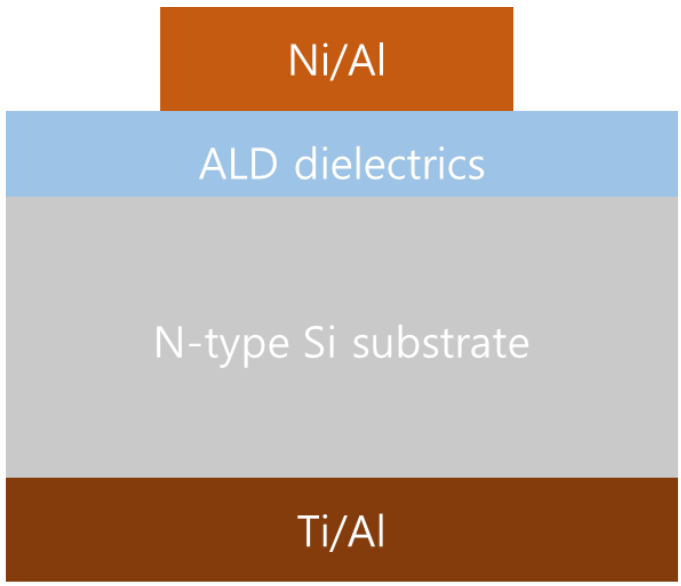


Fig. 4.3 AlN film thickness vs number of ALD cycles

To evaluate and optimize electrical characteristics of ALD AlN, we deposited AlN on Si wafers and fabricated MIS capacitors. The process flow of the MIS capacitors is shown in Fig. 4.4. Before AlN deposition, Si wafers are cleaned with SPM and DHF(10:1) for 10 and 5 minutes, respectively and then immediately moved to ALD chamber. After that, AlN was deposited on the Si wafers and post deposition annealing was carried out at 500 ℃ for 10 minutes in nitrogen ambient using a RTA equipment. then, a lift-off patterning process was performed for gate metallization and a Ni/Al (20/130 nm) stack was deposited on the patterned sample and a Ti/Al

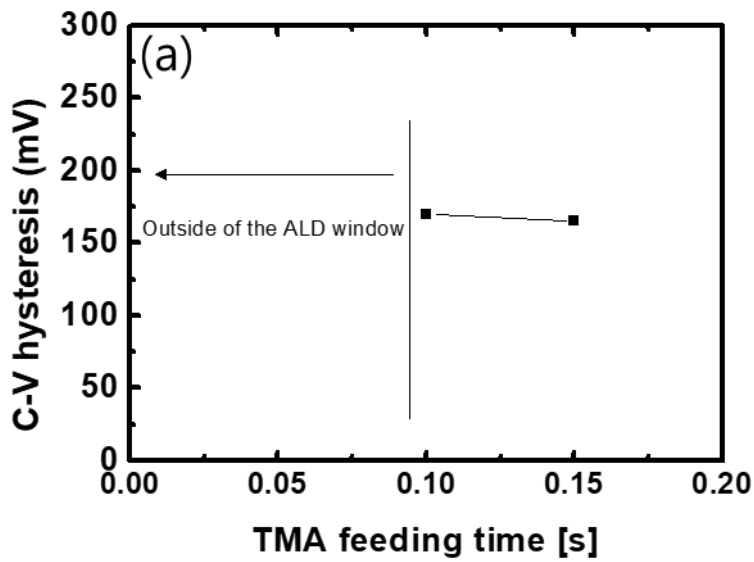
(20/130 nm) stack was deposited on the backside of the sample. The diameter of the fabricated MIS capacitors were 50 um for forward leakage current-voltage measurements and 100 um for capacitance-voltage measurements.



- Si wafer cleaning using SPM and DHF (10:1)
- ALD dielectrics deposition
- Post deposition annealing
- Lift-off patterning process
- Gate metal deposition (Ni/Al=20/130 nm)
- Ohmic metal deposition (Ti/Al =20/130 nm)

Fig. 4.4 Process flow of Si MIS-capacitors

To confirm the TMA feeding time effect on the electrical characteristics of AlN, the TMA feeding time was varied from 0.1sec to 0.15 sec. The NH_3 plasma time, NH_3 plasma power, pressure at the NH_3 plasma step and deposition temperature were 10 sec, 100W, 200 mtorr and 330 ℃, respectively. As shown in Fig. 4.5, the C-V hysteresis was almost the same regardless of the change of the TMA feeding time. However, forward leakage current of AlN was degraded as the TMA feeding time increased.



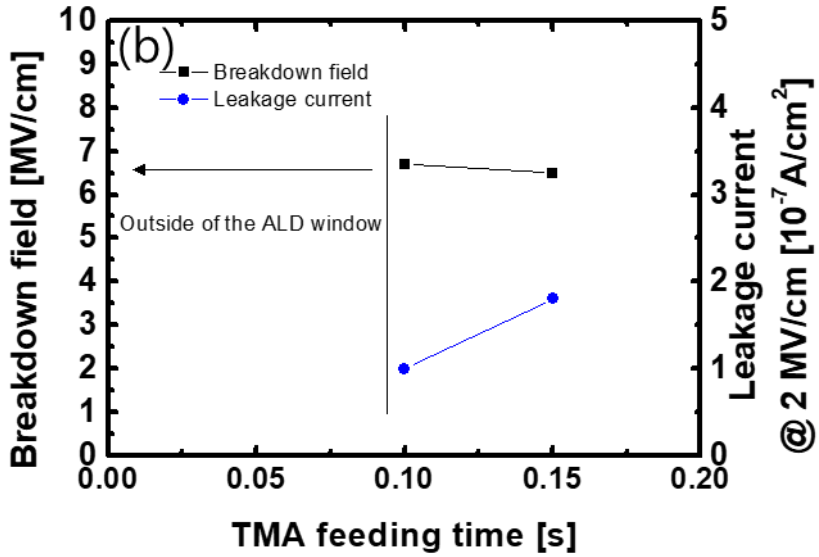
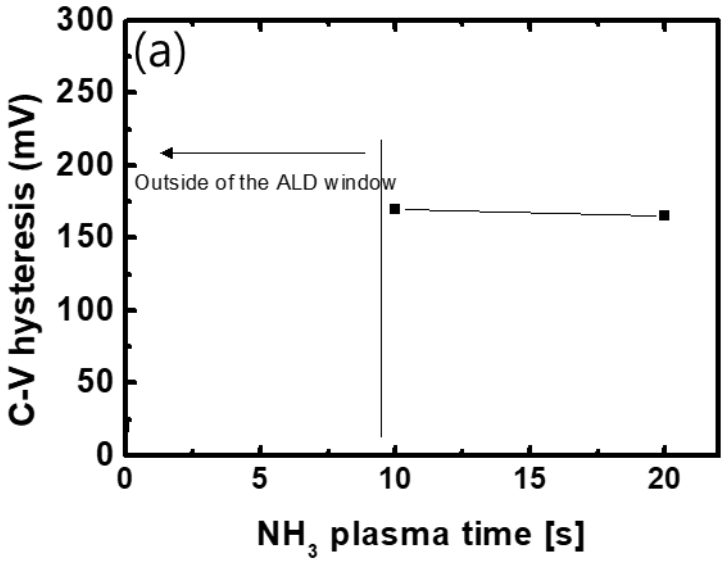


Fig. 4.5 Electrical characteristics of AlN as a function of TMA feeding time. (a) C-V hysteresis vs TMA feeding time and (b) breakdown field and leakage current at 2 MV/cm of AlN vs TMA feeding time

the NH_3 plasma time was also varied from 10 sec to 20 sec. The TMA feeding time, NH_3 plasma power, pressure at the NH_3 plasma step and deposition temperature were 0.1 sec, 100 W, 200 mtorr and 330 ℃, respectively. Likewise, the C-V hysteresis was almost same regardless of the change of the NH_3 plasma time. However, forward leakage current of AlN was degraded as the NH_3 plasma time increased as shown in Fig 4.6. It is thought that excessive plasma exposure during ALD process could result in plasma induced damage on the surface [17].



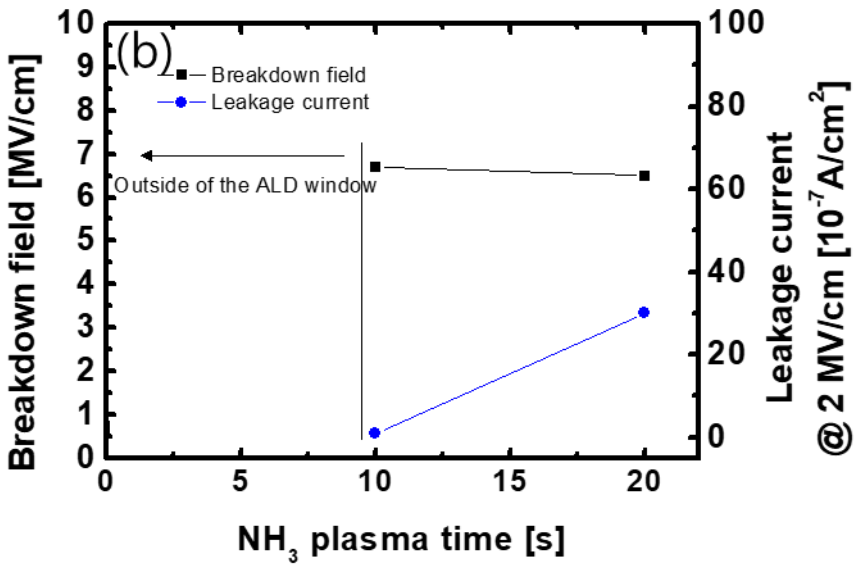
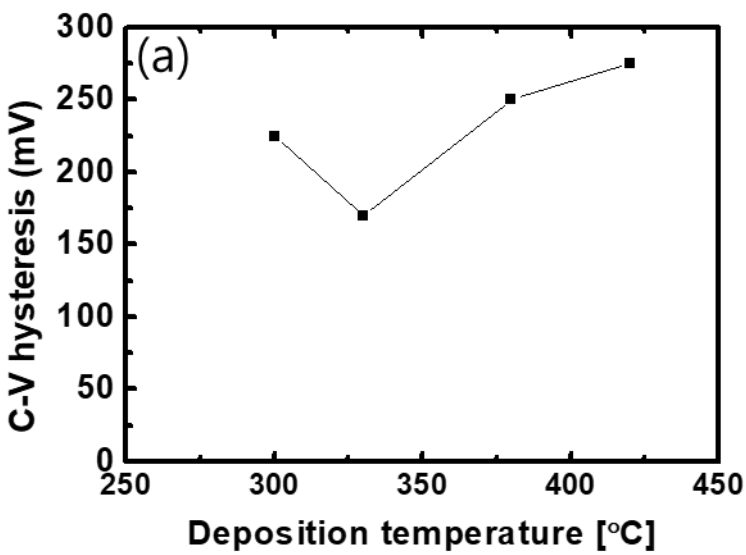


Fig. 4.6 Electrical characteristics of AlN as a function of NH_3 plasma time. (a) C-V hysteresis vs NH_3 plasma time and (b) breakdown field and leakage current at 2 MV/cm of AlN vs NH_3 plasma time

The pressure at the NH_3 plasma step in the ALD process of AlN had considerable effect on the electrical characteristics of ALD AlN. The forward leakage current and C-V hysteresis of AlN were both improved as the pressure at the NH_3 plasma step increased as shown in Fig. 4.7. Higher pressure effect at the NH_3 plasma step was not investigated due to NH_3 gas flow limit. Additionally, deposition temperature effect on the electrical characteristics of ALD AlN was evaluated. Considerable increases of forward leakage current were observed at the higher temperatures than 330 ℃. Also, large C-V hysteresis characteristics were confirmed at over 330 ℃. It is considered that TMA thermally decomposes in the range from 350 to 550 ℃, increasing carbon concentration which can degrade the electrical characteristics of AlN [18-19].



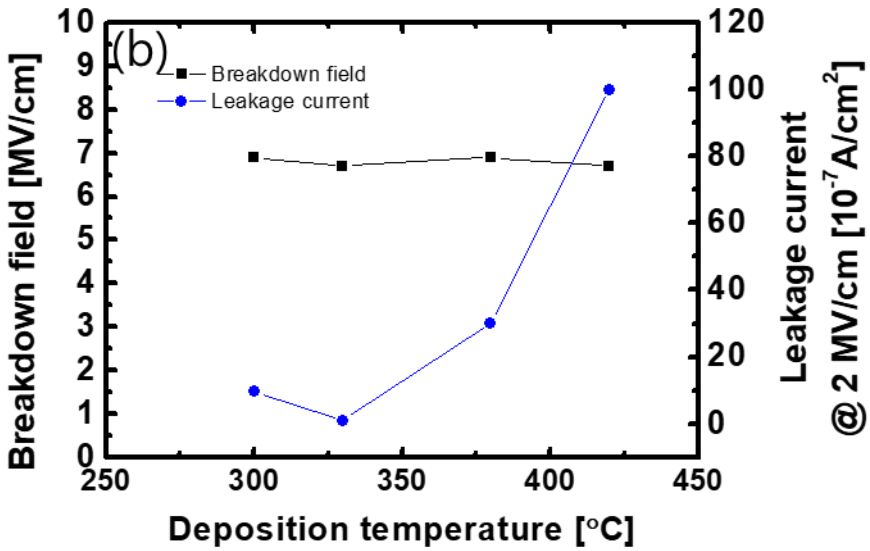


Fig. 4.7 Electrical characteristics of AlN as a function of deposition temperature. (a) C-V hysteresis vs deposition temperature and (b) breakdown field and leakage current at 2 MV/cm of AlN vs deposition temperature

Fig. 4.8 shows the C-V and J-V characteristics of the optimized AlN on Si capacitor. The TMA feeding time of 0.1 sec, NH_3 plasma power of 100 W, NH_3 plasma time of 10 sec, pressure of 200 mtorr at the NH_3 plasma step and deposition temperature of 330 ℃ were chosen for deposition of ALD AlN on Si.

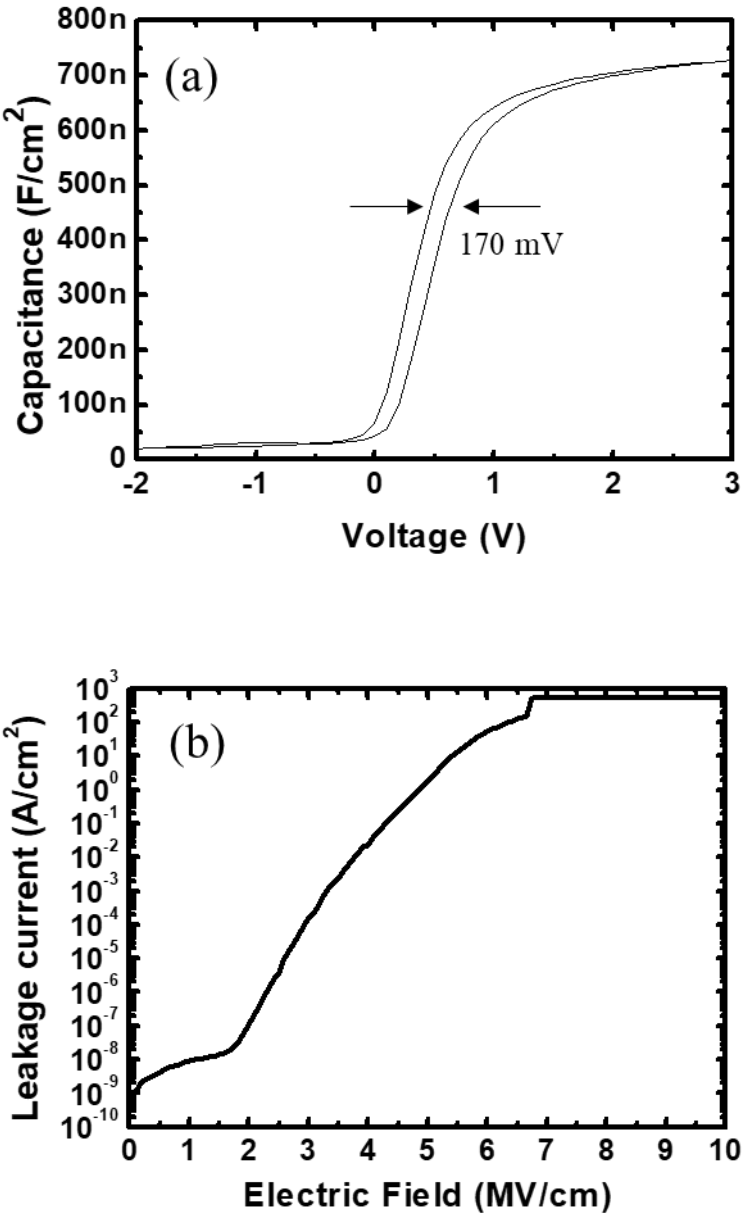
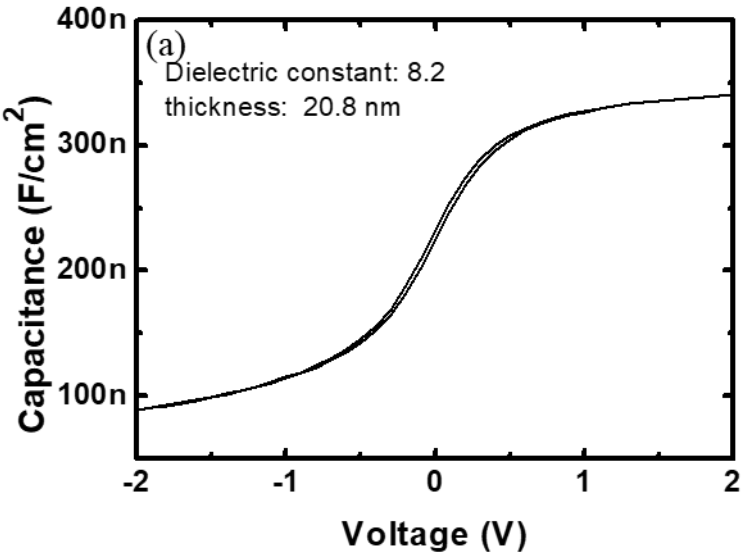
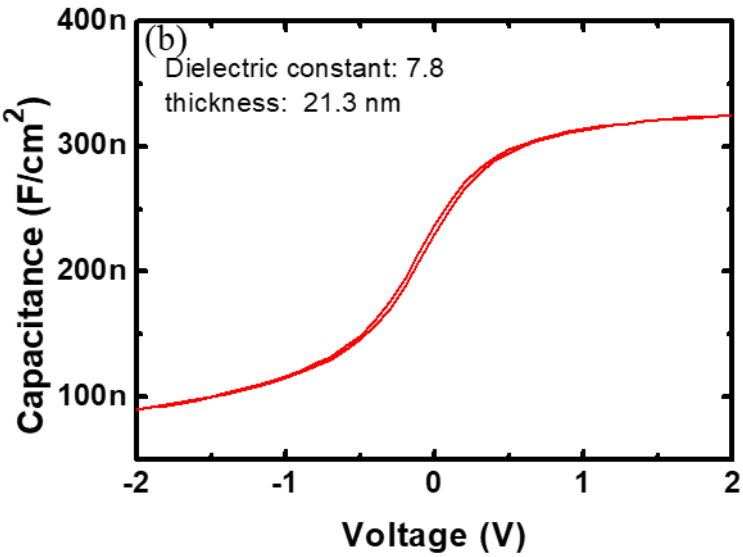


Fig. 4.8 Electrical characteristics of the optimized AlN on Si. (a) C-V characteristics and (b) J-V characteristics

The MIS capacitors using n-GaN were fabricated to investigate the electrical properties of AlN on n-GaN. The epitaxial layers consisted of a 300 nm n-GaN with 2.5E+17cm^{-3} Si doping concentration, a 700 nm n-type GaN layer, a 700 nm n-GaN with 2~3E+18cm^{-3} Si doping concentration and a 3900 nm GaN buffer layer were grown on Si substrate. The AlN layer which was optimized on Si was deposited on n-GaN. To confirm the NH_3 plasma power effect on the electrical characteristics of AlN, AlN on n-GaN capacitors with different plasma powers, ranging from 30 to 100 W were also fabricated. Before AlN deposition, treatments are carried out. The treatments are divided in to ex-situ and in-situ treatments. Ex-situ treatments include SPM and diluted HF (10:1) to remove organic contaminants and native oxides on the surface. In-situ treatments includes TMA pulsing (10 times of 0.2 sec) and NH_3 thermal treatment for 5minutes which were carried out for removal of oxides and surface nitridation, respectively. After AlN deposition, post deposition annealing (PDA) was carried out at 500 ℃ for 10 minutes in N_2 ambient. Fig. 4.9 and Fig. 4.10 show the double sweep C-V characteristics of the AlN on n-GaN capacitors with various NH_3 plasma powers at 1MHz and C-V characteristics with various frequencies varying from 1k to 1MHz, respectively. The C-V hysteresis and frequency dispersion characteristics were almost the same regardless of the change of the NH_3 plasma power. All samples showed very small C-V hysteresis and frequency dispersion.


(a)
Dielectric constant: 8.2
thickness: 20.8 nm
Capacitance (F/cm^2)
400n
300n
200n
100n
-2
-1
0
1
2
Voltage (V)


(b)
Dielectric constant: 7.8
thickness: 21.3 nm
Capacitance (F/cm^2)
400n
300n
200n
100n
-2
-1
0
1
2
Voltage (V)

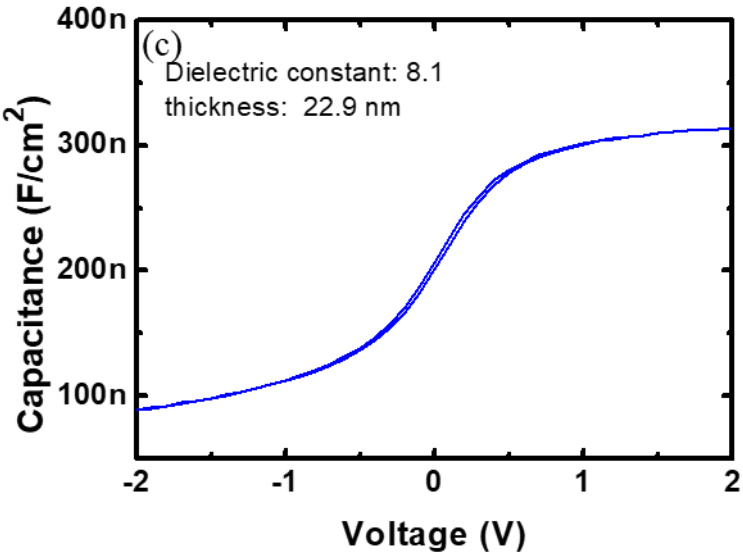
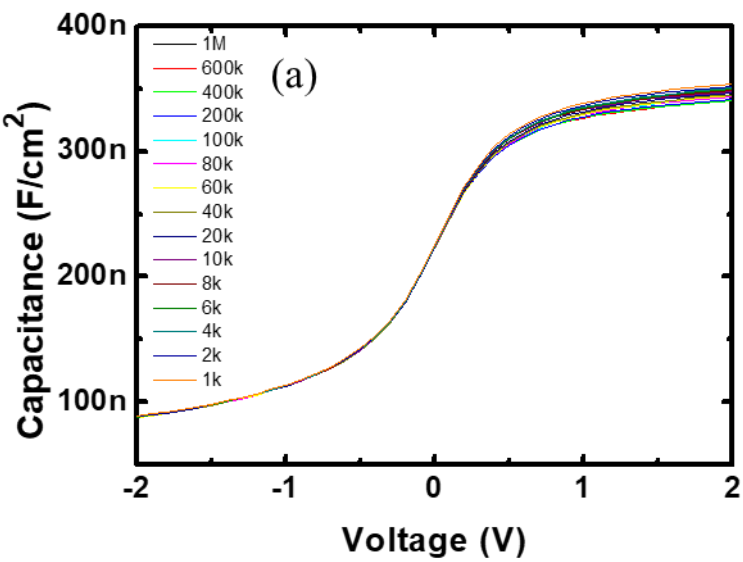


Fig. 4.9 C-V characteristics of the ALD AlN on n-GaN capacitors. NH_3 plasma power (a) 100 W, (b) 50 W and (c) 30 W



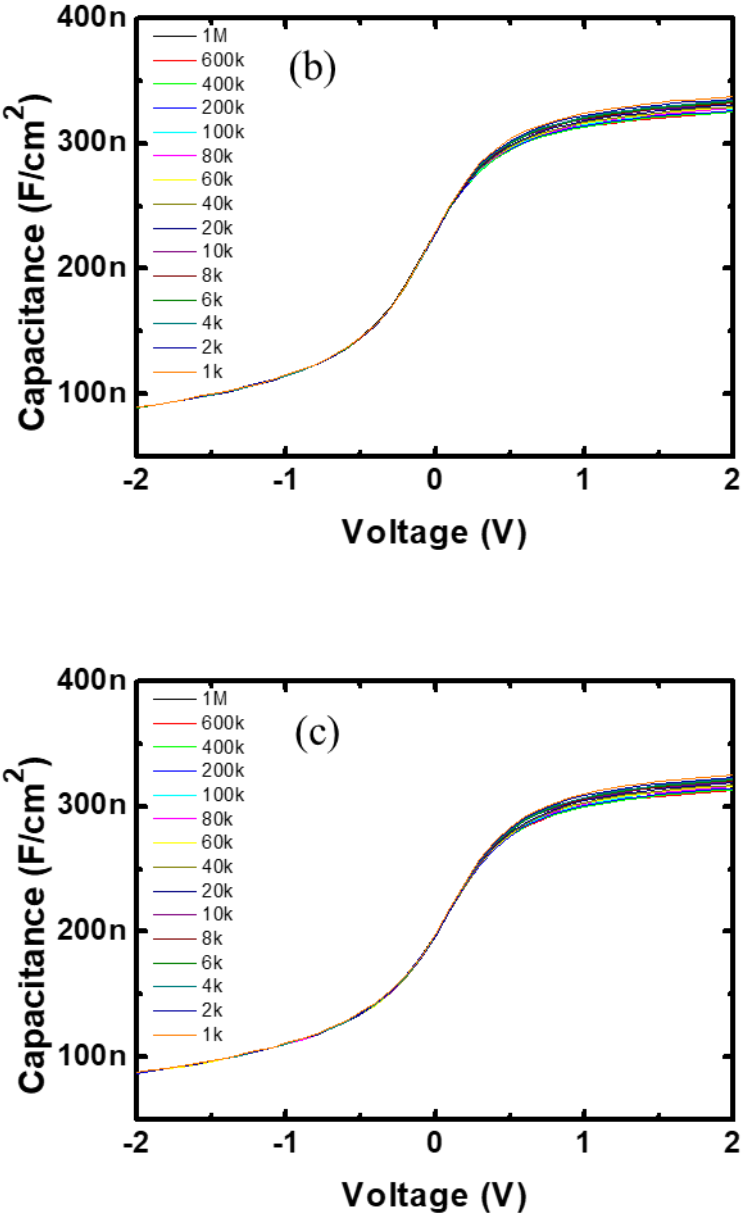


Fig. 4.10 C-V characteristics of the ALD AlN on n-GaN capacitors with various frequencies varying from 1k to 1MHz. (a) 100 W, (b) 50 W and (c) 30 W

However, in J-V characteristics, the AlN on n-GaN capacitor with NH_3 plasma power of 30 W showed the improved breakdown field characteristics and lower leakage current at the low electrical field than the capacitors with plasma powers over 30 W, as shown in Fig. 4.11. It is thought that low plasma power at the NH_3 plasma step can reduce plasma induced damage on the n-GaN surface, resulting in the low leakage current of the AlN on n-GaN capacitor [20]. In conclusion, the TMA feeding time of 0.1 sec, NH_3 plasma power of 30 W, NH_3 plasma time of 10 sec, pressure of 200 mtorr at the NH_3 plasma step and deposition temperature of 330 ℃ were chosen as the optimized deposition condition of AlN on n-GaN.

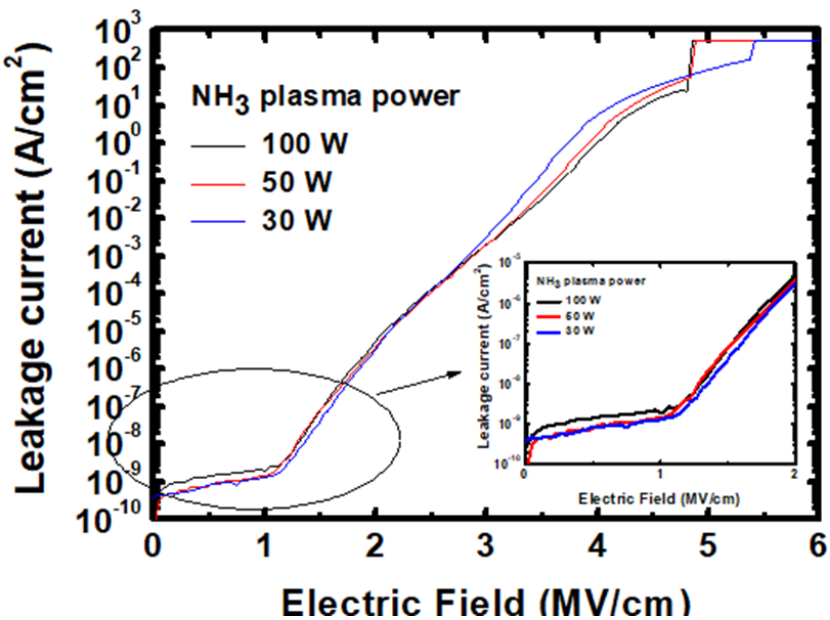


Fig. 4.11 J-V characteristics of the ALD AlN on n-GaN capacitors with various NH_3 plasma powers

Fig. 4. 12 shows an X-ray diffraction (XRD) result of the ALD AlN of

100 nm deposited on n-GaN. A Polycrystalline AlN was observed from the XRD result. Different diffraction peaks at 2θ value of ~33°and ~36° which are assigned to the (100) and (002), respectively were confirmed [21-22]. The FWHM of the rocking curve of AlN (002) was 1045 arcsec as shown in Fig. 4.13.

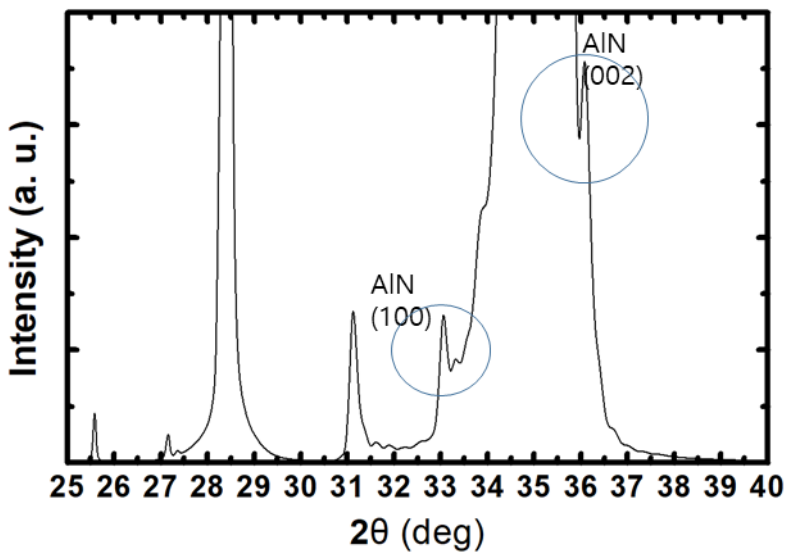


Fig. 4.12 XRD result for the ALD AlN of 100 nm on n-GaN

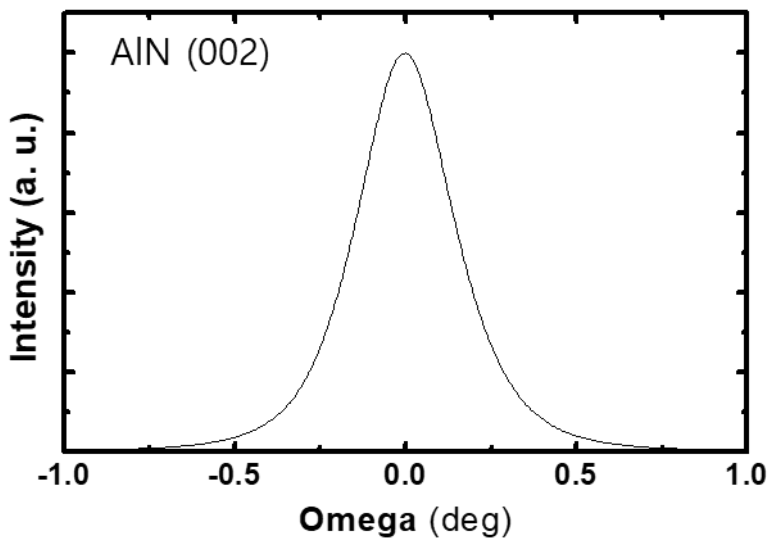


Fig. 4.13 Rocking curve of AlN (002) plane of the ALD AlN

The density of the ALD AlN was also evaluated by fitting of the X-ray reflectivity (XRR) data as shown in Fig. 4.14. The ALD AlN had a density of 3.27 g/cm^3, which is higher than results shown in early studies [23-26].

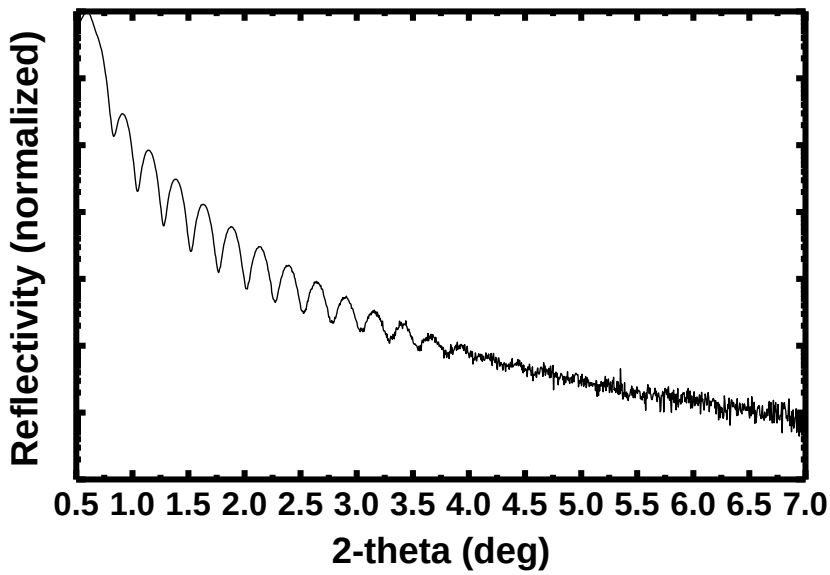


Fig. 4.14 XRR measurement of the ALD AlN of ~ 30 nm on n-GaN

Fig. 4.15 shows the high-resolution TEM cross-section of the AlN of ~ 10 nm on n-GaN. A sharp interface between the n-GaN and ALD AlN and crystalline AlN were observed from the TEM image. GaN surface oxidation is successfully suppressed by employing the AlN layer.

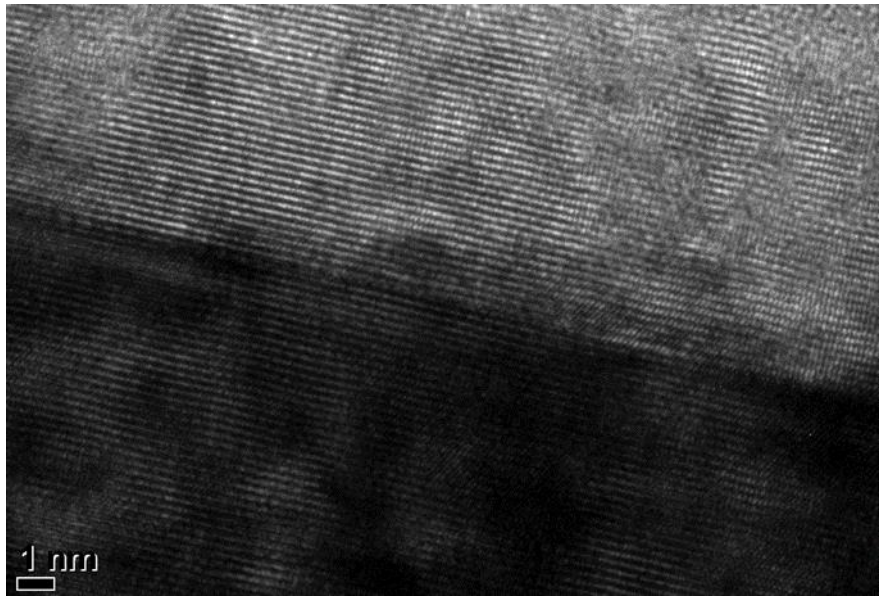


Fig. 4.15 Cross-sectional TEM image of the AlN/n-GaN interface

We also performed x-ray photoelectron spectroscopy (XPS) analysis to investigate the composition of AlN. Spectra of the core level of Al, N, O and C were analyzed as shown in Fig. 4.16 and atomic percentages of Al, N, O and C from the XPS data is shown in Table 4.1.

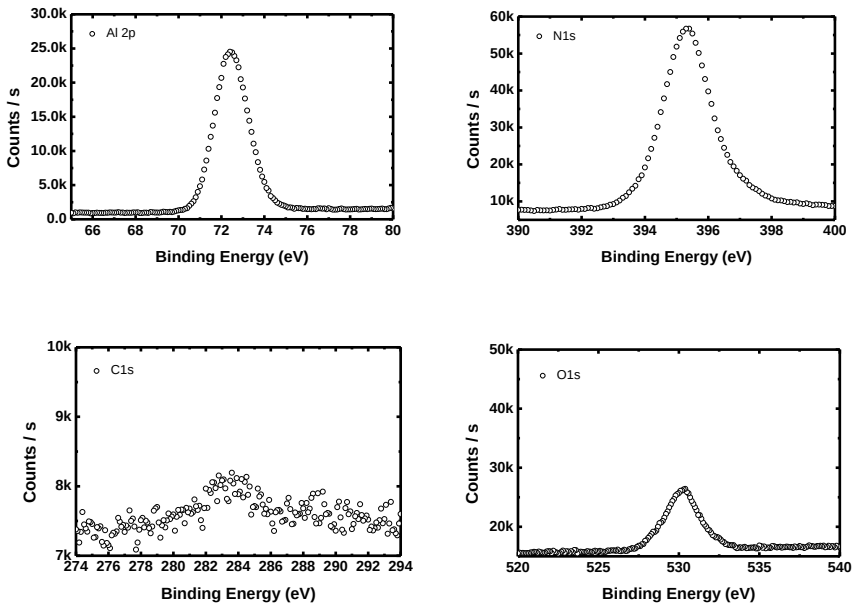


Fig. 4.16 XPS spectra of Al 2p, N 1s, C 1s and O 1s of the AlN

Material	Al 2p (%)	N 1s (%)	C 1s (%)	O 1s (%)
ALD AlN	47.4	44.2	0.9	7.5

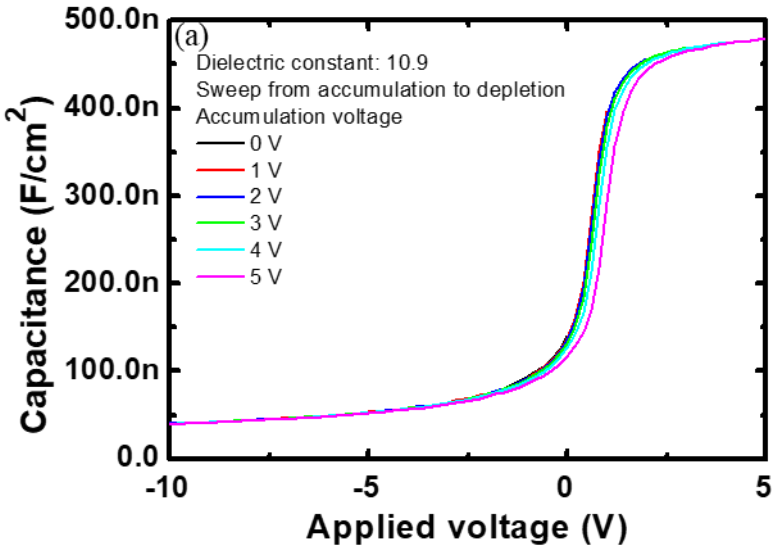
Table 4.1 Atomic percentages of Al, N, C and O for the ALD AlN

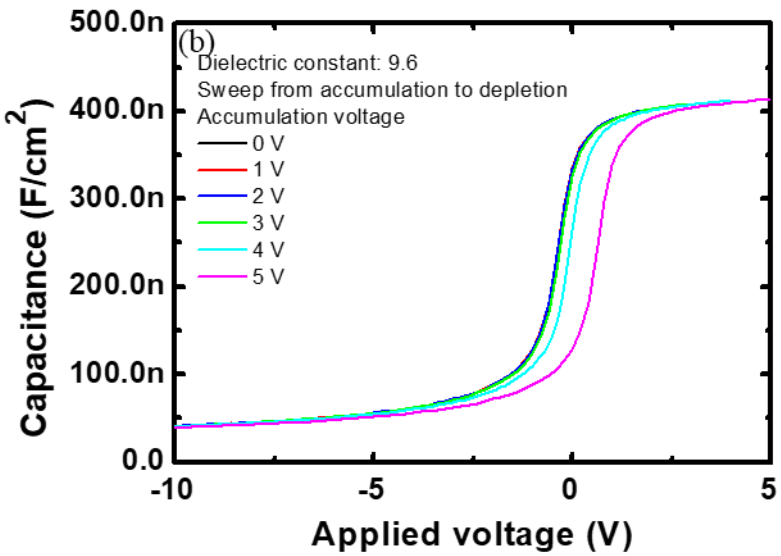
4.2.2. ALD AlN as an Interfacial Layer

We fabricated GaN MIS capacitors using the ALD AlN to evaluate the electrical characteristics of the AlN as an interfacial layer. GaN MIS capacitors using ALD AlON and SiON as an interfacial layer were also fabricated for comparison purposes. An ALD AlHfON layer from AlON/HfO_2 laminate with alternate AlON of 1cycle and HfO_2 of 1cycle was used as a bulk layer due to the high leakage current of the ALD AlN. More details about the AlHfON layer will be discussed in the next section.

The n-GaN on Si epi-wafer used in the former section was used and the same ex-situ and in-situ treatments were carried out for removal of organic contaminants and native oxides on the surface before the dielectric deposition. Total thickness of the dielectric layers deposited on n-GaN was ~20 nm. After deposition of dielectric layers, post deposition annealing (PDA) was carried out at 500 ℃ for 10 minutes in N_2 ambient.

The leakage current density (J) – effective electric field (E_{eff}) characteristics and C-V characteristics of the fabricated GaN MIS capacitors were investigated. The effective electric field was defined as the (applied voltage – flat band voltage)/CET. We conducted repeated C-V measurements sweeping the gate voltage from accumulation to depletion. the accumulation voltage was varied from 0 to 5 V to evaluate the immunity against electron injection into the dielectrics. The diameters of the fabricated MIS capacitors were 50 um for forward leakage current-voltage measurements and 100 um for capacitance-voltage measurements. Fig. 4.17 and Fig. 4.18 show C-V characteristics of the GaN MIS capacitors by sweeping the voltage from accumulation to depletion and V_{FB} shift of the GaN MIS capacitors as a function of accumulation voltage, respectively.


(a)
Dielectric constant: 10.9
Sweep from accumulation to depletion
Accumulation voltage
0 V
1 V
2 V
3 V
4 V
5 V
Capacitance (F/cm2)
500.0n
400.0n
300.0n
200.0n
100.0n
0.0
-10
-5
0
5
Applied voltage (V)


(b)
Dielectric constant: 9.6
Sweep from accumulation to depletion
Accumulation voltage
0 V
1 V
2 V
3 V
4 V
5 V
Capacitance (F/cm2)
500.0n
400.0n
300.0n
200.0n
100.0n
0.0
-10
-5
0
5
Applied voltage (V)

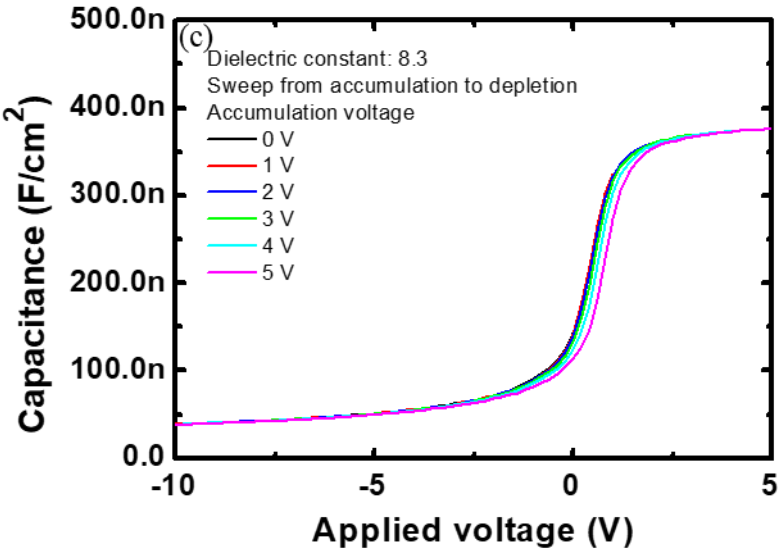


Fig. 4.17 C-V characteristics of the GaN MIS capacitors with accumulation voltages ranging from 0 to 5 V. (a) AlON 5 nm/AlHfON 15 nm, (b) AlN 5 nm/AlHfON 15 nm and (c) SiON 5 nm/AlHfON 15 nm

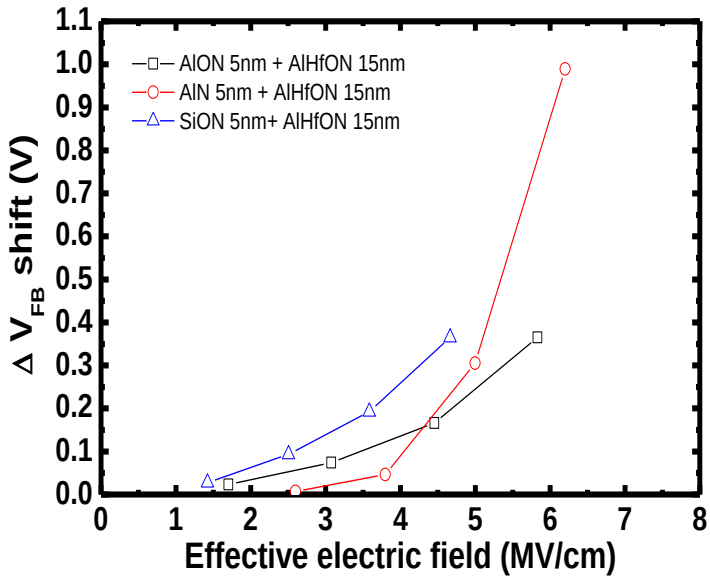


Fig. 4.18 V_{FB} shift as a function of effective electric field in the fabricated GaN MIS capacitors

The sample using the AlN as an interfacial layer showed the smallest V_{FB} shift up to the effective electric field of ~4 MV/cm, which is attributed to the small density of interface states between the AlN and GaN by suppressing the formation of unintentional interfacial oxides. However, the sample showed large V_{FB} shifts above 4MV/cm. The sample using the AlON as an interfacial layer showed the smallest V_{FB} shift above the effective electric field of ~5 MV/cm.

Fig. 4.19 shows J-E_{eff} characteristics of the fabricated GaN MIS capacitors. The sample using the AlN as an interfacial layer showed the highest leakage current in the initial effective electric field range and the lowest breakdown field which is attributed to the low breakdown field and

high leakage current of the AlN.

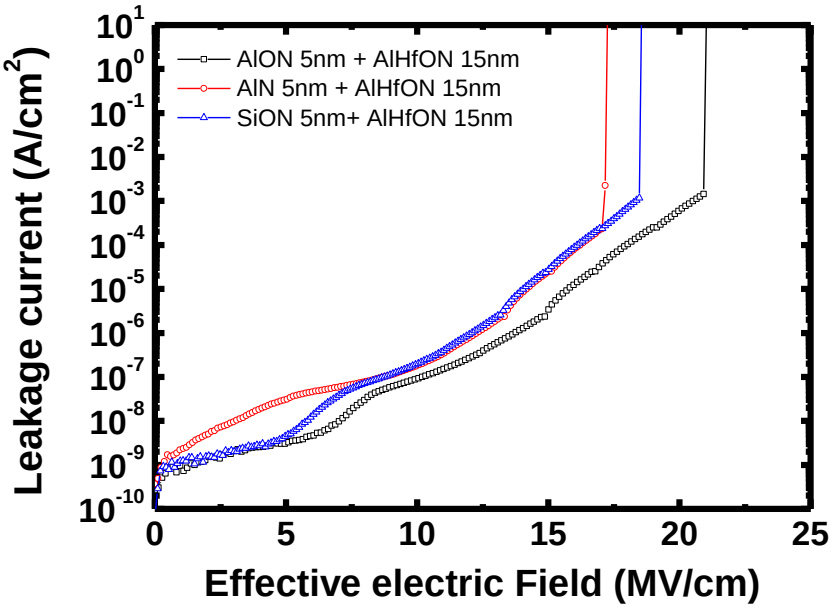


Fig. 4.19 J-E_{eff} characteristics of the fabricated GaN MIS capacitors

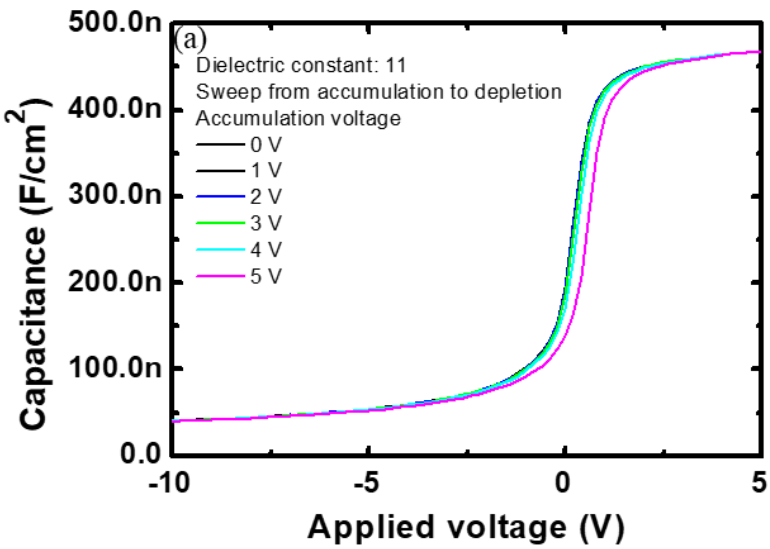
4.2.3. Thickness Optimization of AlN/AlON/AlHfON Layer

As discussed in the former section, the AlN as an interfacial layer efficiently suppressed charge injection into the dielectrics in the low effective electric field up to 4 MV/cm. However, in the effective electric field over 5 MV/cm, smaller electron trapping was observed in the GaN MIS capacitor using the AlON as an interfacial layer than that in the GaN MIS capacitor using the AlN. These results suggested that the charge injection into the surface states and dielectrics could be more suppressed by employing the AlN/AlON layer under the AlHfON layer. In this section, we studied the AlN and AlON thickness effect on the electron trapping into the surface states and dielectrics and J-E_{eff} characteristics in the GaN MIS capacitors. First, the AlN thickness effect on the electrical characteristics of the GaN MIS capacitors was studied. The total AlN/AlON layer thickness and AlHfON layer thickness were maintained to ~5 nm and ~15 nm, respectively for all samples as shown in Table 4.2.

Sample	AlN/AlON/AlHfON layer		
	AlN	AlON	AlHfON
A	~3 nm	~2 nm	
B	~2 nm	~3 nm	~ 15 nm
C	~1 nm	~4 nm	

Table 4.2 Description of studied AlN/AlON/AlHfON layers

Fig. 4.20 show C-V characteristics of the GaN MIS capacitors by sweeping the voltage from accumulation to depletion with various accumulation voltages. From these results, V_{FB} shifts of the GaN MIS capacitors as a function of accumulation voltage were determined as shown in Fig. 4.21. The values of V_{FB} shift in the GaN MIS capacitors using the AlN of 5 nm and AlON of 5 nm as an interfacial layer were also plotted for comparison.



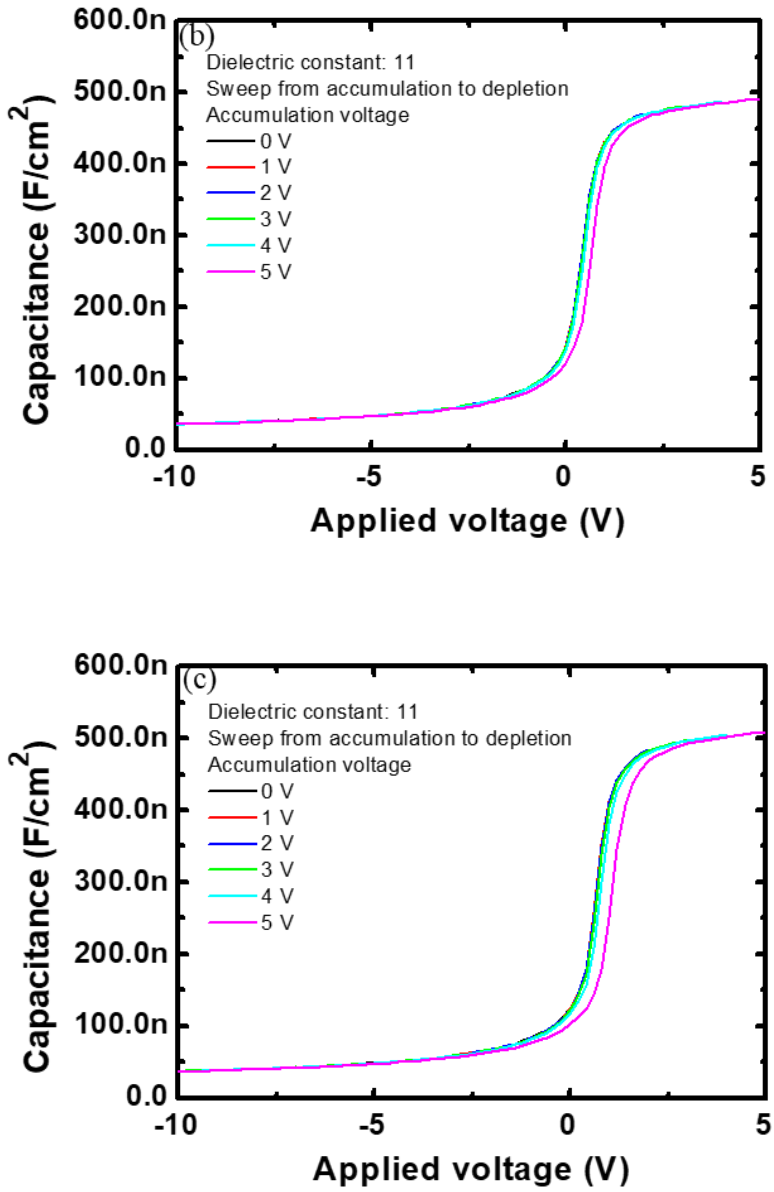


Fig. 4.20 C-V characteristics of the GaN MIS capacitors with accumulation voltages ranging from 0 to 5 V. (a) AlN 3 nm/AlON 2 nm/AlHfON 15 nm, (b) AlN 2 nm/AlON 3 nm/AlHfON 15 nm and (c) AlN 1 nm/AlON 4 nm/AlHfON 15 nm

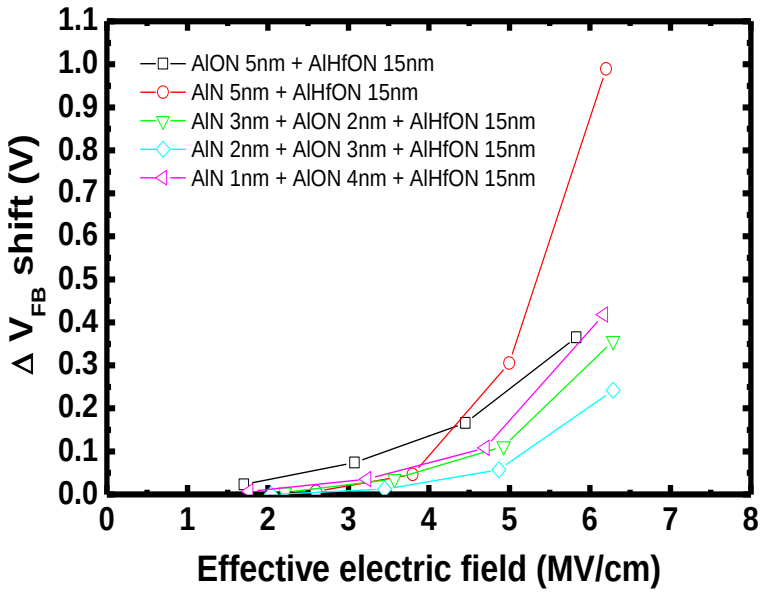


Fig. 4.21 V_{FB} shift as a function of effective electric field in the fabricated GaN MIS capacitors

The amount of V_{FB} shift decreased as the AlN thickness increased and increased at the AlN thickness over 2 nm. This result represents that the AlN thickness of 2 nm is the optimum point as an interfacial layer. J-E_{eff} characteristics of the fabricated GaN MIS capacitors with different AlN/AlON ratios were almost the same regardless of the AlN/AlON ratios as shown in Fig. 4.22. J-E_{eff} characteristics in the GaN MIS capacitors using the AlN of 5 nm and AlON of 5 nm as an interfacial layer were also plotted for comparison.

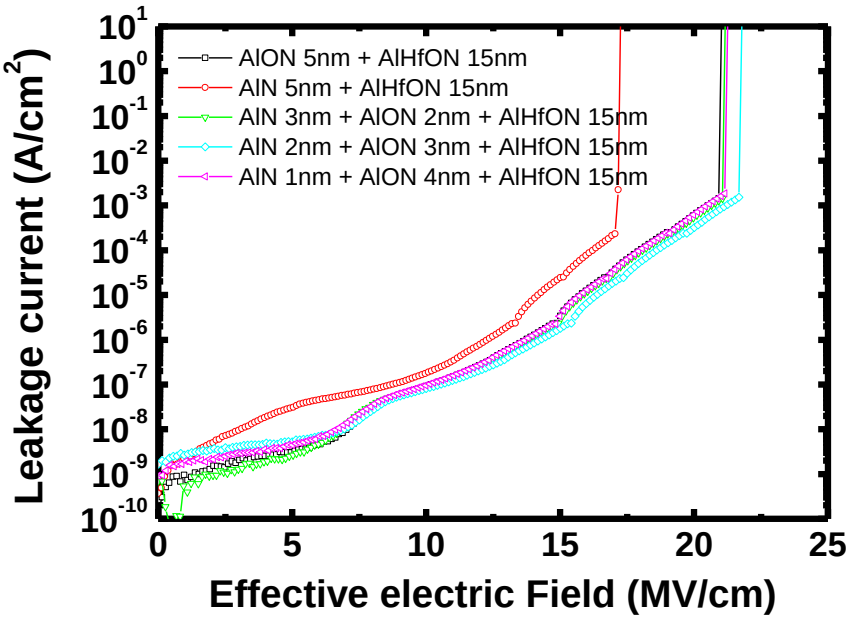


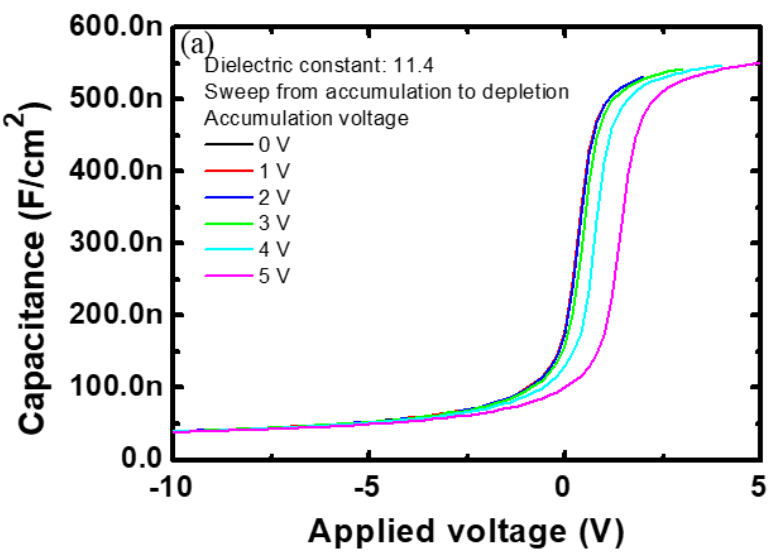
Fig. 4.22 J-E_{eff} characteristics of the fabricated GaN MIS capacitors

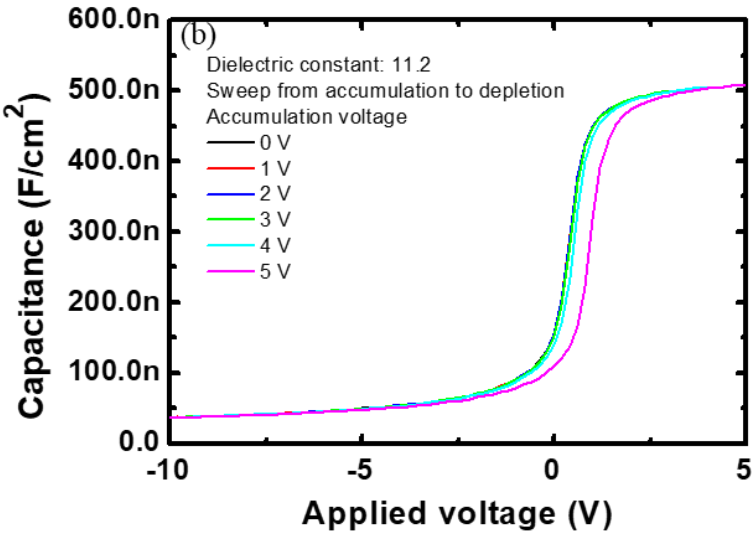
Next, the AlON thickness effect on the electrical characteristics of the GaN MIS capacitors was also studied. The AlN layer thickness and AlON/AlHfON layer thickness were maintained to ~2 nm and ~18 nm, respectively for all samples as shown in Table 4.3.

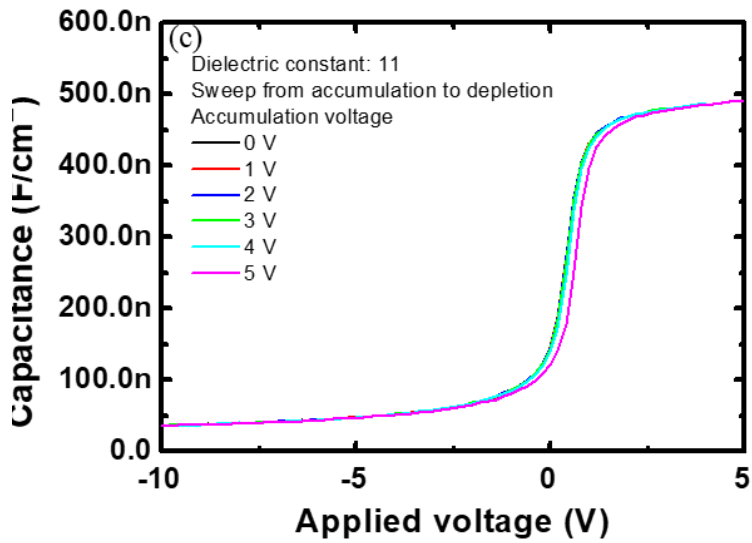
Sample	AlN/AlON/AlHfON layer		
	AlN	AlON	AlHfON
A	~2 nm	~1 nm	~ 17 nm
B		~2 nm	~ 16 nm
C		~3 nm	~ 15 nm
D		~4 nm	~ 14 nm
E		~5 nm	~ 13 nm

Table 4.3 Description of studied AlN/AlON/AlHfON layers

Fig. 4.23 show C-V characteristics of the GaN MIS capacitors with different AlON/AlHfON ratios by sweeping the voltage from accumulation to depletion with various accumulation voltages. From these results, V_{FB} shifts of the GaN MIS capacitors as a function of accumulation voltage were determined as shown in Fig. 4.24.




(b)
Dielectric constant: 11.2
Sweep from accumulation to depletion
Accumulation voltage
0 V
1 V
2 V
3 V
4 V
5 V
Capacitance (F/cm^2)
600.0n
500.0n
400.0n
300.0n
200.0n
100.0n
0.0
-10
-5
0
5
Applied voltage (V)


(c)
Dielectric constant: 11
Sweep from accumulation to depletion
Accumulation voltage
0 V
1 V
2 V
3 V
4 V
5 V
Capacitance (F/cm^2)
600.0n
500.0n
400.0n
300.0n
200.0n
100.0n
0.0
-10
-5
0
5
Applied voltage (V)

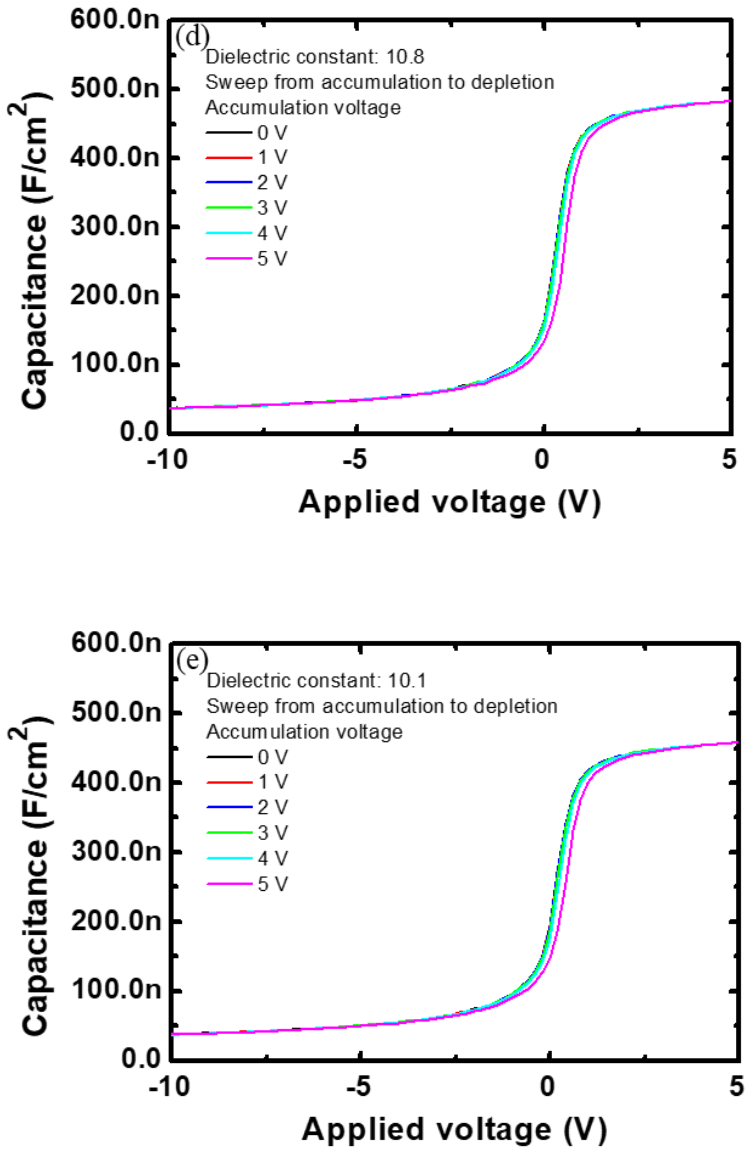


Fig. 4.23 C-V characteristics of the GaN MIS capacitors with accumulation voltages ranging from 0 to 5 V. (a) AlN 2 nm/AlON 1 nm/AlHfON 17 nm, (b) AlN 2 nm/AlON 2 nm/AlHfON 16 nm, (c) AlN 2 nm/AlON 3 nm/AlHfON 15 nm, (d) AlN 2 nm/AlON 4 nm/AlHfON 14 nm and (e) AlN 2 nm/AlON 5 nm/AlHfON 13 nm

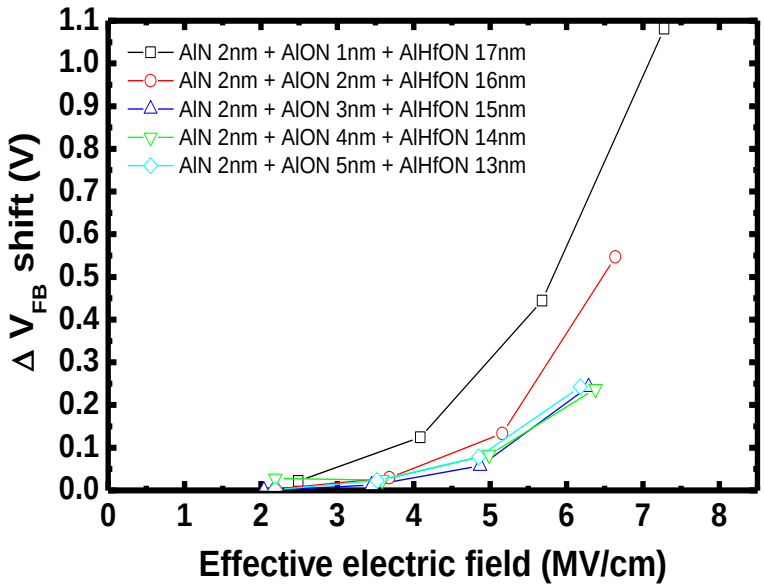


Fig. 4.24 V_{FB} shift as a function of effective electric field in the fabricated GaN MIS capacitors

The amount of V_{FB} shift decreased as the AlON thickness increased and it saturated at the AlON thickness of 3 nm under the same accumulation voltage. However, the dielectric constant of the GaN MIS capacitors decreases as the AlON thickness increases. These results represent that the AlON thickness of 3 nm is the optimum point for AlN/AlON/AlHfON gate stack. J-E_{eff} characteristics in the fabricated GaN MIS capacitors with different AlON/AlHfON ratios were shown in Fig. 4.25.

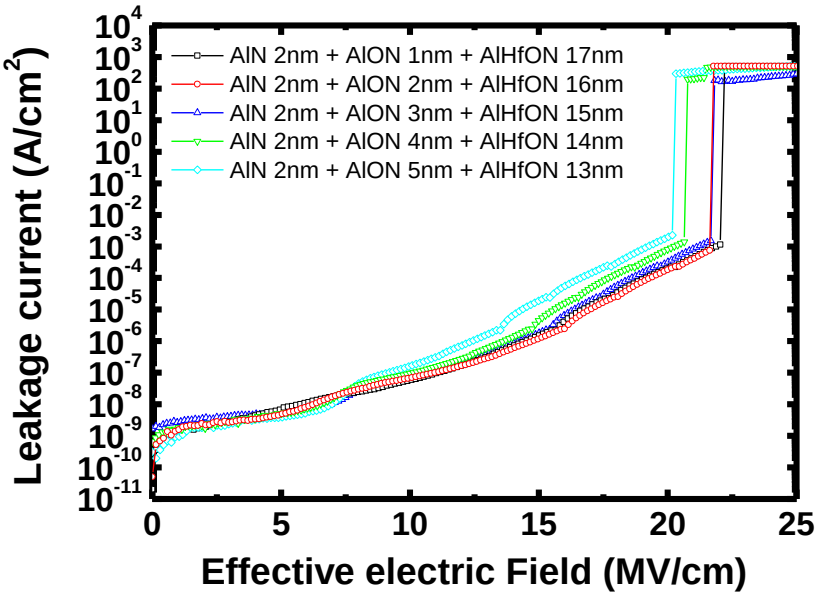


Fig. 4.25 J-E_{eff} characteristics of the fabricated GaN MIS capacitors

Similar J-E_{eff} characteristics were observed for the GaN MIS capacitors with the AlON thickness between 1 nm to 3 nm. J-E_{eff} characteristics were degraded with the AlON thickness over 3 nm. The optimized thicknesses of the AlN, AlON and AlHfON layers are 2 nm, 3 nm and 15 nm, respectively.

4.2.4. ALD AlHfON Optimization

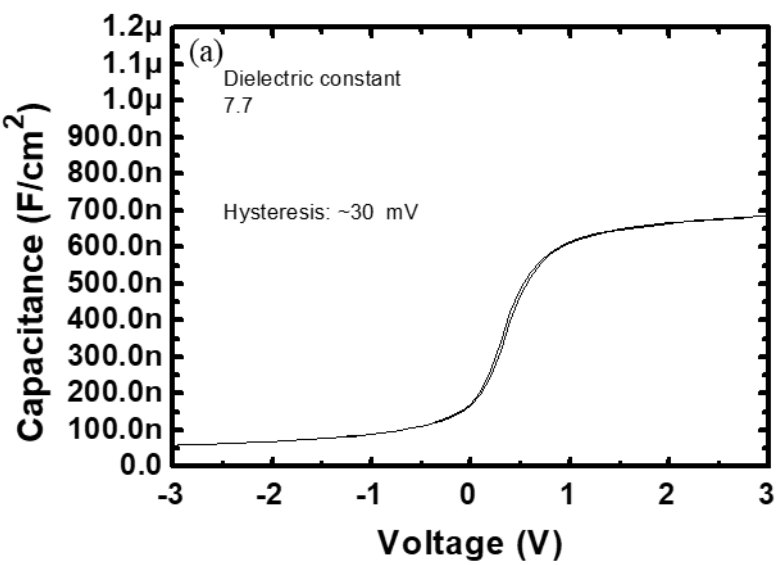
As discussed in the previous section, High-k dielectrics provide a decreased off-state leakage current, a high on-state current, a high on/off current ratio, and a low subthreshold swing in GaN based power devices, resulting in the improvement of the efficiency in power conversion systems. Among the high-k dielectrics, HfO_2 is considered as the most promising dielectric layer because of their ease of manufacture by ALD. However, when a HfO_2 is employed as a gate insulator, significant gate leakage currents could occur and it suffers from poor thermal stability and poor blocking of oxygen diffusion through the HfO_2 and low crystallization temperature. It has been reported that Al incorporation into HfO_2 can reduce electrical defects and gate leakage current and increase the dielectric constant and crystallization temperature.

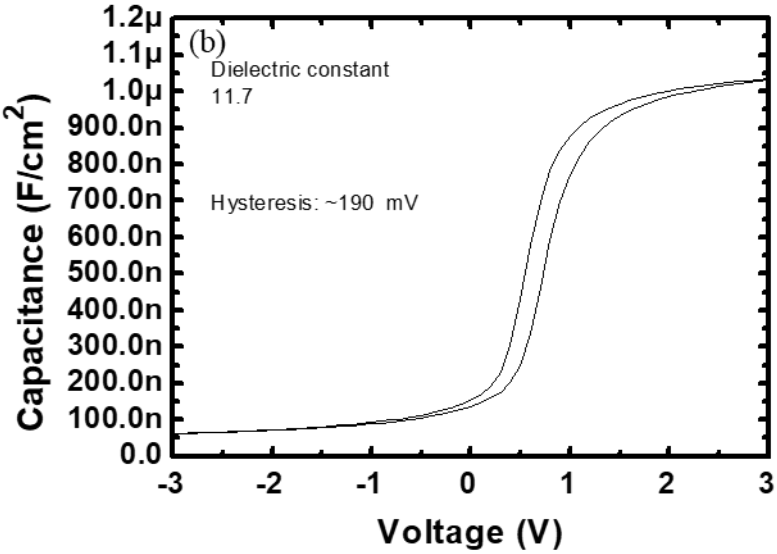
In this study, we investigated the electrical and material characteristics of ALD AlHfON layers (AlON-HfO_2 laminate). The effect of ratio of Al to Hf on the electrical characteristics of AlHfON was also studied. To deposit ALD AlHfON, $Al_2(CH_3)_6$ (TMA), $[(CH_3)_2N]_4Hf$ (TDMAH), N_2 plasma and ozone (O_3) were used as Al, Hf, N precursors and an oxidant, respectively. One cycle of the AlHfON deposition was defined by TMA pulse (0.3s)/N_2 purge (10s)/O_3 pulse (0.5s)/N_2 purge (7s)/N_2 stabilization (5s)/N_2 plasma (7s)/N_2 purge (7s)/TDMAH pulse (0.4s)/N_2 purge (6s)/O_3 pulse (0.5s)/N_2 purge (9s). The temperature of chuck was maintained at 330 ℃. 10~12 nm AlHfON layers were deposited on n-GaN. After that, post deposition annealing (PDA) was carried out at 500 ℃ for 10 minutes in N_2 ambient. GaN MIS capacitors using AlHfON layers were fabricated to investigate the electrical properties of AlHfON on n-GaN. GaN MIS capacitors using AlON

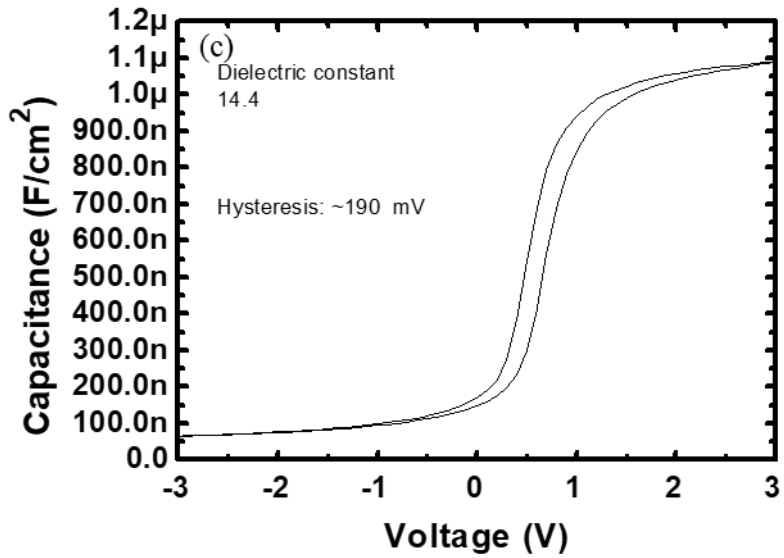
and HfO_2 layers were also fabricated for comparison. Table 4.4 shows the gate stacks studied in this study. Fig. 4.26 shows the C-V characteristics, the dielectric constants and the amount of C-V hysteresis of the fabricated GaN MIS capacitors.

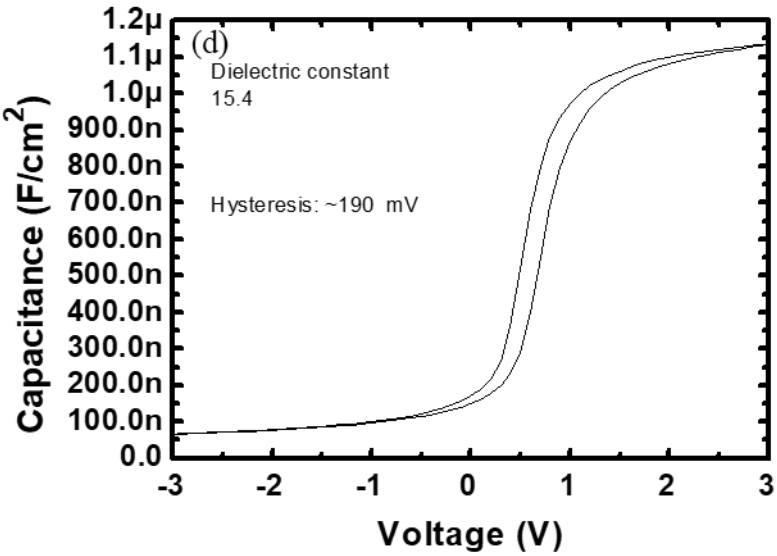
Sample	AlON:HfO_2 cycle ratio		
	AlON	HfO_2	Layer
A	1	0	AlON
B	1	1	AlHfON
C	1	2	
D	1	3	
E	1	4	
F	0	1	HfO_2

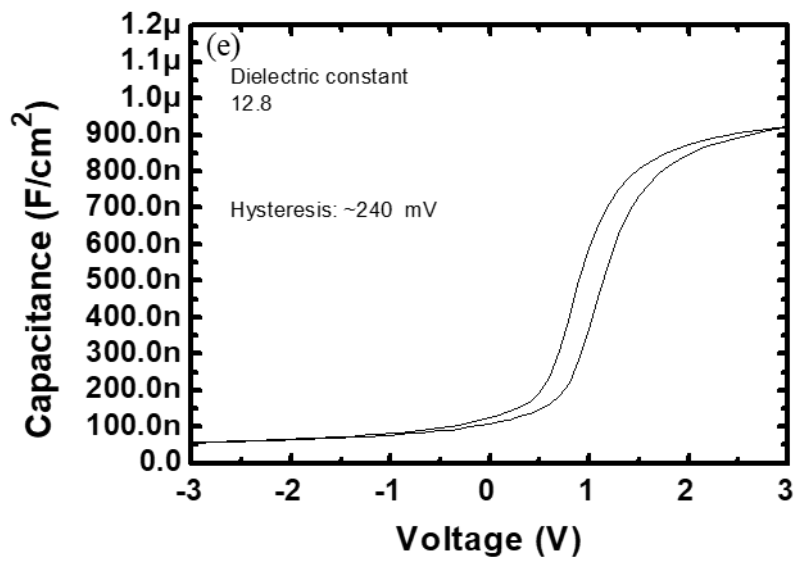
Table 4.4 Description of studied AlON, AlHfON and HfO_2 layers

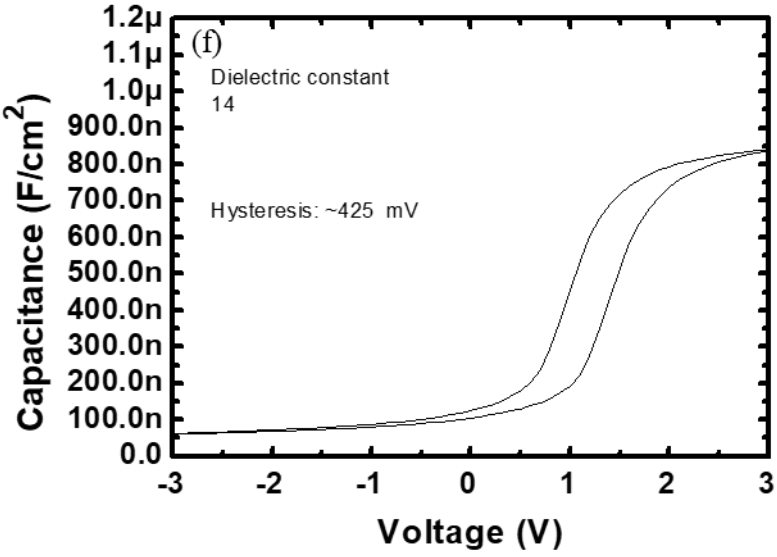


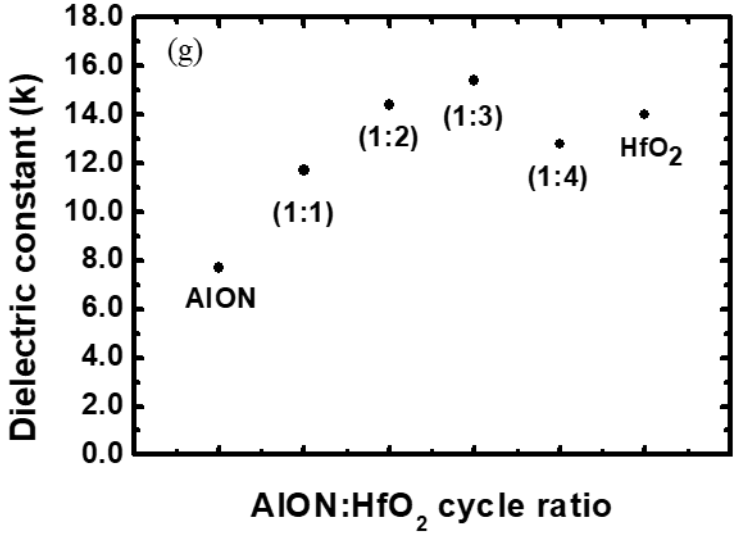

(b)
Dielectric constant
11.7
Hysteresis: ~190 mV
Capacitance (F/cm^2)
1.2µ
1.1µ
1.0µ
900.0n
800.0n
700.0n
600.0n
500.0n
400.0n
300.0n
200.0n
100.0n
0.0
-3
-2
-1
0
1
2
3
Voltage (V)


(c)
Dielectric constant
14.4
Hysteresis: ~190 mV
Capacitance (F/cm^2)
1.2µ
1.1µ
1.0µ
900.0n
800.0n
700.0n
600.0n
500.0n
400.0n
300.0n
200.0n
100.0n
0.0
-3
-2
-1
0
1
2
3
Voltage (V)


(d)
Dielectric constant
15.4
Hysteresis: ~190 mV
Capacitance (F/cm^2)
1.2µ
1.1µ
1.0µ
900.0n
800.0n
700.0n
600.0n
500.0n
400.0n
300.0n
200.0n
100.0n
0.0
-3
-2
-1
0
1
2
3
Voltage (V)


(e)
Dielectric constant
12.8
Hysteresis: ~240 mV
Capacitance (F/cm^2)
1.2µ
1.1µ
1.0µ
900.0n
800.0n
700.0n
600.0n
500.0n
400.0n
300.0n
200.0n
100.0n
0.0
-3
-2
-1
0
1
2
3
Voltage (V)


(f)
Dielectric constant
14
Hysteresis: ~425 mV
Capacitance (F/cm^2)
1.2µ
1.1µ
1.0µ
900.0n
800.0n
700.0n
600.0n
500.0n
400.0n
300.0n
200.0n
100.0n
0.0
-3
-2
-1
0
1
2
3
Voltage (V)


(g)
Dielectric constant (k)
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
AlON
(1:1)
(1:2)
(1:3)
(1:4)
HfO$_2$
AlON:HfO$_2$ cycle ratio

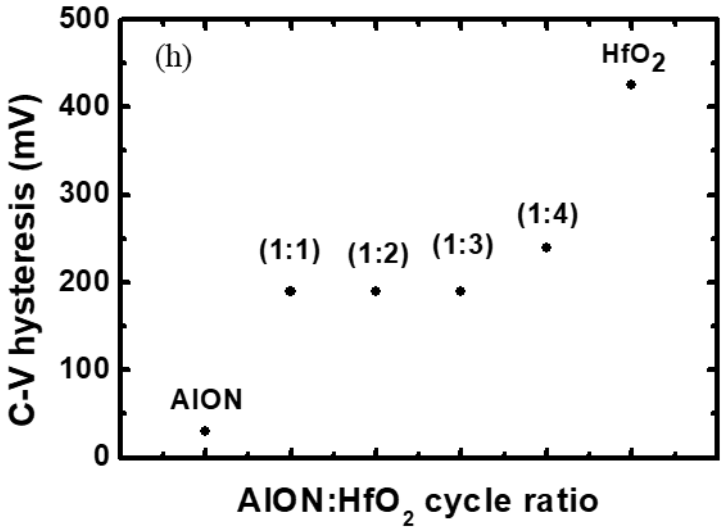


Fig. 4.26 C-V characteristics of (a) AlON, AlHfON with AlON : HfO_2 cycle ratio of (b) 1:1, (c) 1:2, (d) 1:3, (e) 1:4 and (f) HfO_2 and (g) the dielectric constants and (h) the amount of C-V hysteresis of the dielectric layers

The dielectric constant of AlHfON increased up to the AlON : HfO_2 cycle ratio of 1:3 as the cycle of HfO_2 increased. The AlHfON with AlON : HfO_2 cycle ratio of 1:3 showed higher dielectric constant than the HfO_2. This result is similar to the results of other groups for AlHfO in which Al incorporation into HfO_2 increases the dielectric constant. The amount of C-V hysteresis of AlHfON decreased as the AlON cycle in the ALD process of AlHfON increased and it saturated at the AlON : HfO_2 cycle ratio of 1:3. These results represent that the AlHfON with AlON : HfO_2 cycle ratio of 1:3 is the optimum point for a bulk layer.

We performed x-ray photoelectron spectroscopy (XPS) analysis to investigate the composition of AlHfON with AlON : HfO_2 cycle ratio of 1:3.

Spectra of the core level of Hf, Al, N, C and O were analyzed as shown in Fig. 4.27 and atomic percentages of Hf, Al, N, C and O from the XPS data were 27, 9.7, 1.4, 1.9 and 59.6 %, respectively as shown in Table 4.5.

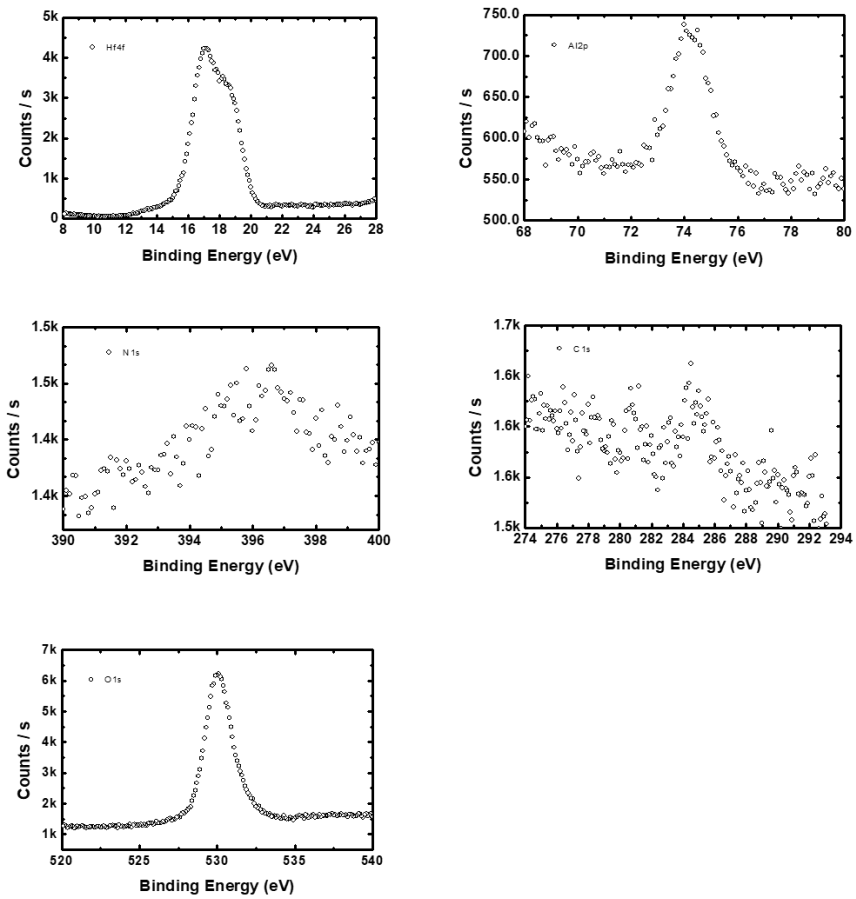


Fig. 4.27 XPS spectra of Hf 4f, Al 2p, N 1s, C 1s and O 1s of the ALD AlHfON layer

Material	Hf 4f (%)	Al 2p (%)	N 1s (%)	C 1s (%)	O 1s (%)
ALD AlHfON	27.3	9.7	1.4	1.9	59.6

Table 4.5 Atomic percentages of Hf, Al, N, C and O for the ALD AlHfON

The crystal structures of the HfO_2 and AlHfON with AlON : HfO_2 cycle ratio of 1:3 were investigated using an x-ray diffractometer (XRD) as shown in Fig. 4.28. The HfO_2 showed several peaks reflecting the monoclinic phases, while the AlHfON with AlON : HfO_2 cycle ratio of 1:3 had few peaks evidencing the amorphous phase. This result may explain the reason why the leakage current of AlHfON is lower than that of HfO_2.

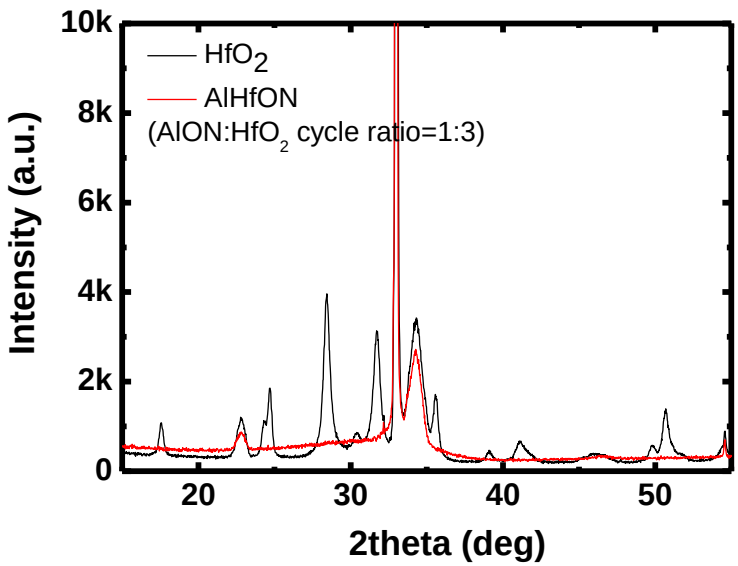
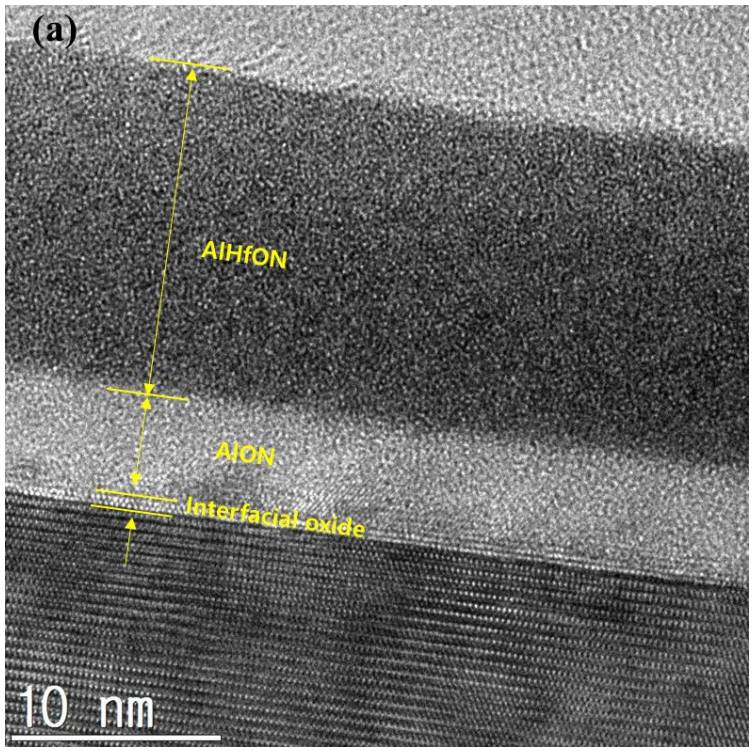
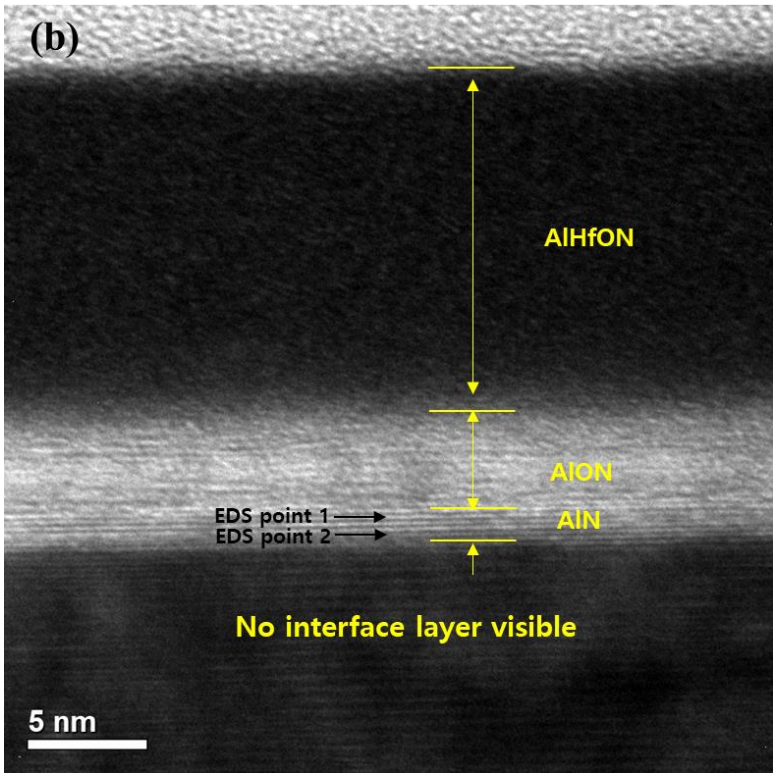


Fig. 4.28 XRD patterns of the ALD HfO_2 and AlHfON with AlON : HfO_2 cycle ratio of 1:3

4.2.5. Material Characteristics of AlN/AlON/AlHfON Layer

TEM images of AlON/AlHfON and AlN/AlON/AlHfON on n-GaN layers are shown in Fig. 4.29. Interfacial layer of ~1 nm was observed at the interface between AlON and n-GaN while no interface layer between AlN and n-GaN was observed. Also, less oxygen atomic percent was confirmed at the AlN near the n-GaN layer than that near the AlON layer as shown in the EDS results. This result represents that The ALD AlN efficiently suppresses surface oxidation while the AlON using O_3 as an oxidant forms interfacial layers on n-GaN layer.





Selected point	Atomic (%)		
	Al	O	N
1	40.3	34.7	25
2	44.5	14.3	41.2

Fig. 4.29 TEM images of (a) AlON/AlHfON and (b) AlN/AlON/AlHfON on n-GaN layers and energy dispersive spectroscopy (EDS) results for the selected points

In order to further analyze detailed information of the interface between dielectrics and n-GaN, TOF-SIMS analysis of AlON/AlHfON and AlN/AlON/AlHfON on n-GaN layers was carried out as shown in Fig. 4. 30.

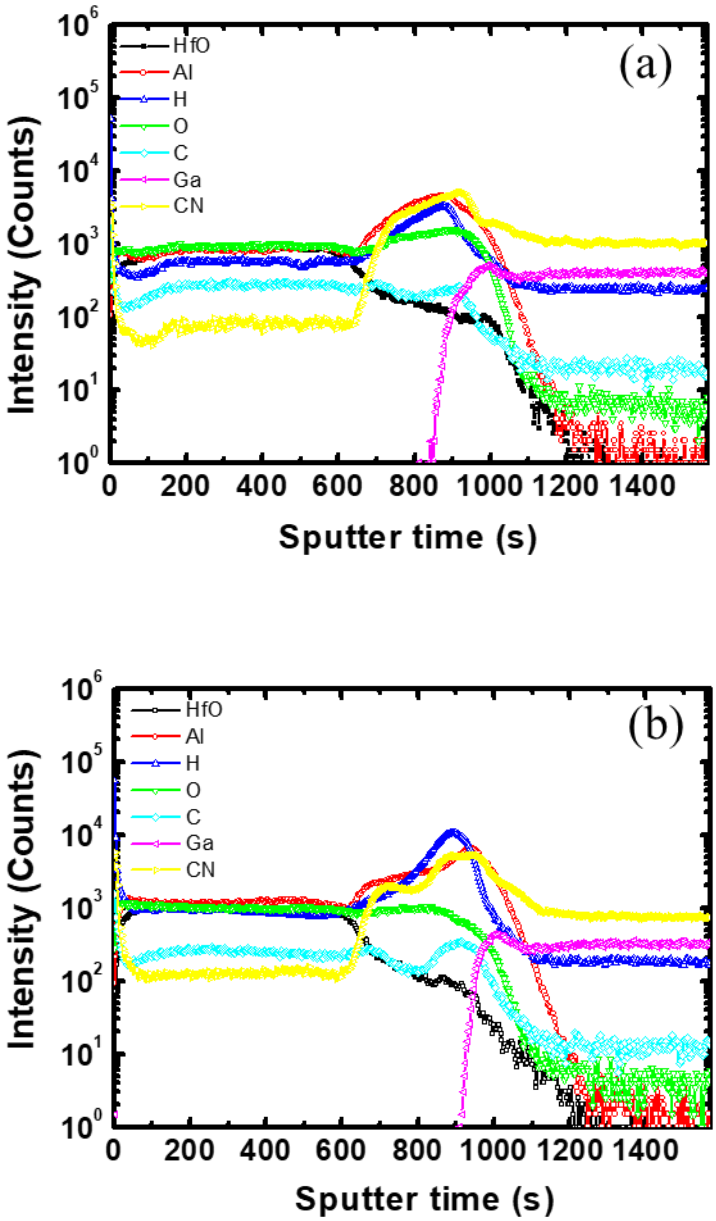


Fig. 4.30 TOF-SIMS results of (a) AlON/AlHfON and (b) AlN/AlON/AlHfON on n-GaN layers

Broad and high oxygen intensity peak was observed at the AlON/n-GaN interface, while, narrow and low oxygen intensity peak was observed at the AlN/n-GaN interface. Also, decline of the Ga is steeper at the AlN/n-GaN interface compared to that at the AlON/n-GaN interface. These result supports our hypothesis that using an ALD AlN as an interfacial layer has advantage over using an AlON with O_3 oxidant at the III-V interface by suppressing the surface oxidation.

4.3. Device Characteristics of Normally-off AlGaN/GaN MIS-FETs with AlN/AlON/AlHfON Layer

We developed and optimized an AlN/AlON/AlHfON layer as a gate insulator on n-GaN as discussed in the former section. The ALD AlN interfacial layer suppressed unintentional interfacial oxide and the AlHfON efficiently reduced the leakage current and increased the dielectric constant of the gate insulator.

Normally-off AlGaN/GaN MIS-FETs with 2 nm AlN/3 nm AlON/15 nm AlHfON layer were fabricated. Devices with 5 nm AlON/15 nm AlHfON layer were also fabricated for comparison. The epitaxial layer structure consists of 10 nm SiN in situ capping layer, 3.9 nm GaN interlayer, 22.6 nm undoped AlGaN barrier layer, GaN channel, and buffer on Si (111) substrate. The process flow of the devices was almost the same as the former section. However, Gate-recess process was carried out with the ALE discussed in the former section. ~2 nm AlGaN barrier layer was left, which was confirmed by observing the etched depth of the co-processed dummy sample using atomic force microscope (AFM). Then, the samples were cleaned with a sulfuric acid peroxide mixture and diluted HF acid. In the ALD chamber, in-situ treatments including TMA pulsing (10 times of 0.2 sec) and NH_3 thermal treatment for 5minutes were carried out for removal of oxides and surface nitridation, respectively. After dielectric layer deposition at 330 ℃ in the ALD chamber, post deposition annealing (PDA) was carried out at 500 ℃ for 10 minutes in N_2 ambient. Ni/Au (40 nm/250

nm) gate metal was deposited with e-gun evaporation. Finally, post metallization annealing (PMA) was carried out at 400 ℃ in forming gas ambient, H_2 (5%) + N_2 (95%) for 10 minutes. Gate to source distance, gate length and gate to drain distance were 2, 1.5 and 10 um, respectively.

Fig. 4. 31 shows the transfer characteristics of the fabricated devices in linear scale and log scale. The maximum drain current density of devices with AlN/AlON/AlHfON layer was ~566 mA/mm while that of devices with AlON/AlHfON layer was ~466 mA/mm at V_{DS} of 10 V. Devices with AlN/AlON/AlHfON layer showed I-V hysteresis of ~10 mV while I-V hysteresis of devices with AlON/AlHfON layer was ~125 mV. This result represents that The AlN layer efficiently suppresses the electron trapping into the gate insulator. The threshold voltage values which is defined as the gate voltage at I_{DS} of 1uA/mm of devices with AlN/AlON/AlHfON and AlON/AlHfON were 0.5 and 0.51 V, respectively.

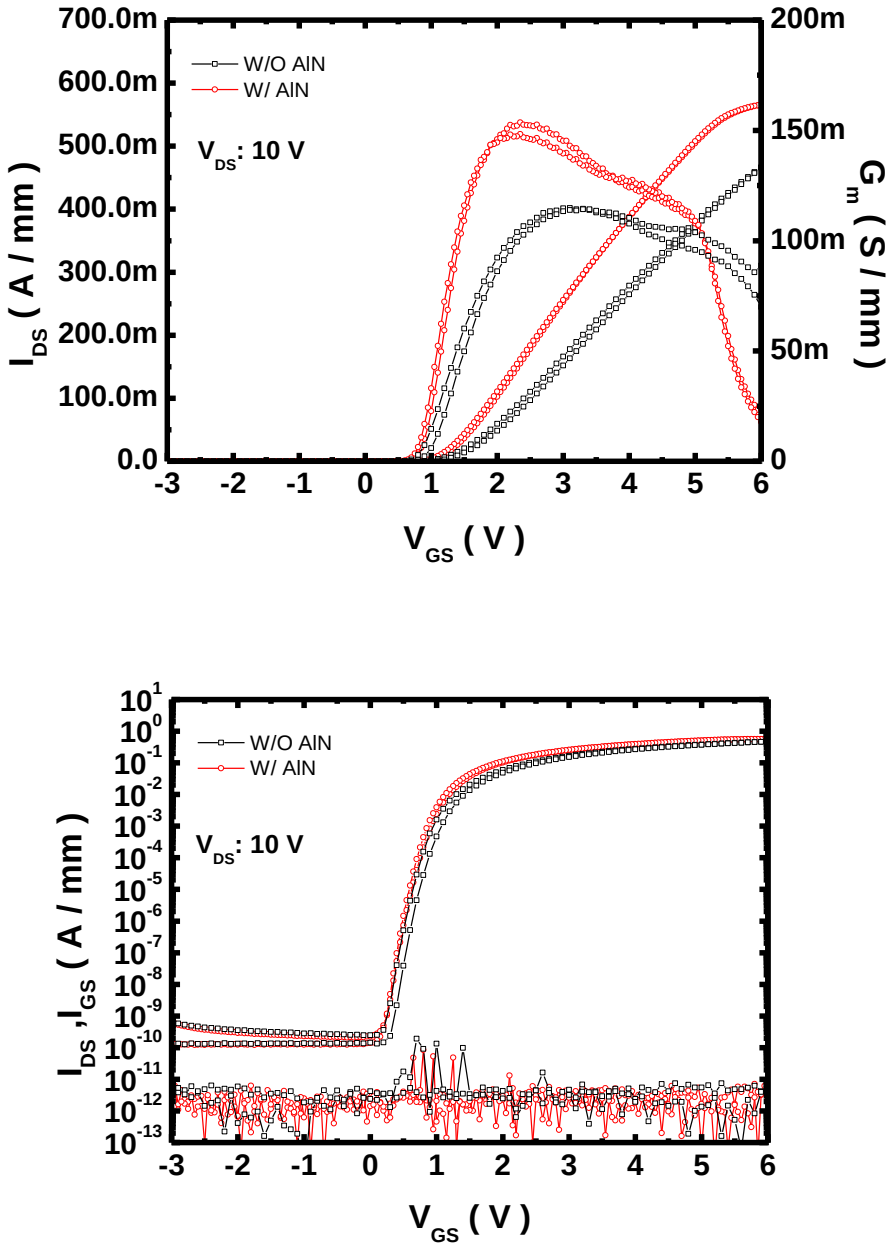


Fig. 4.31 Transfer characteristics of the fabricated devices in linear scale and log scale

Fig. 4. 32 shows the output I-V characteristics of the fabricated devices. The extracted static R_{on} values of devices with AlN/AlON/AlHfON and AlON/AlHfON were 1.35 and 1.69 m$\Omega \cdot cm^2$, respectively.

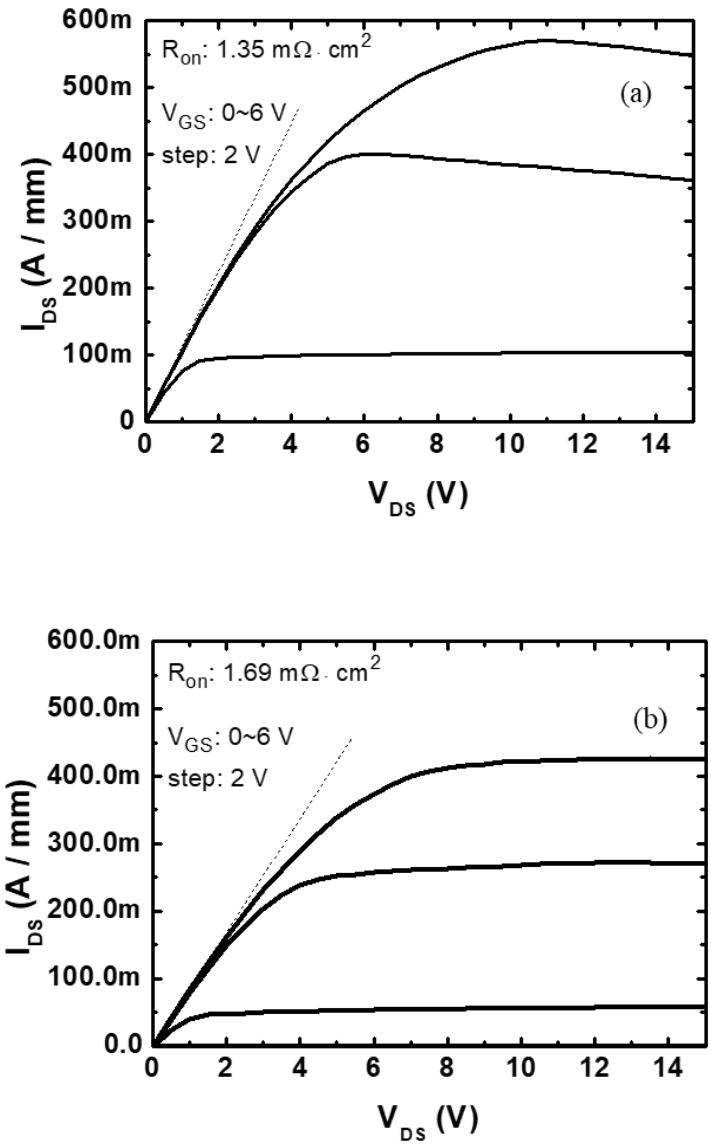


Fig. 4.32 Output characteristics of the fabricated devices with (a) AlN/AlON/AlHfON and (b) AlON/AlHfON

To investigate the interface quality, the effective mobility and D_{it} were extracted as shown in Fig. 4.33 and 4.34, respectively. The effective mobility was extracted from a FAT-FET with a gate length of 100 um. The maximum effective mobility value was 949 $cm^2/V{\cdot}s$ for devices with AlN/AlON/AlHfON layer while that for devices with AlON/AlHfON was 320 $cm^2/V{\cdot}s$. The D_{it} values of AlN/AlON/AlHfON MIS-FET were less than those of AlON/AlHfON MIS-FET within the overall trap level range of 0.29 ~ 0.44 eV. These results were attributed to the high-quality AlN interfacial layer.

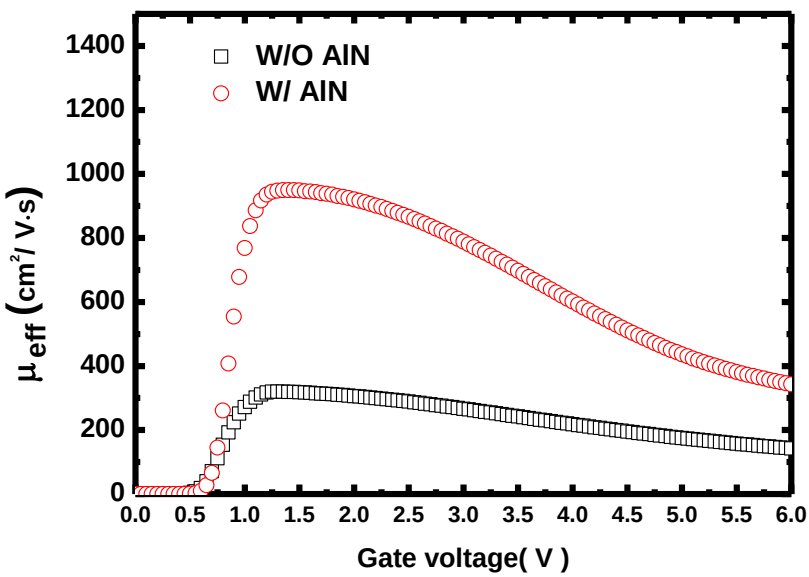


Fig. 4.33 Effective mobility in the normally-off GaN channel of FAT-FETs with a gate length of 100 um with AlON/AlHfON and AlN/AlON/AlHfON

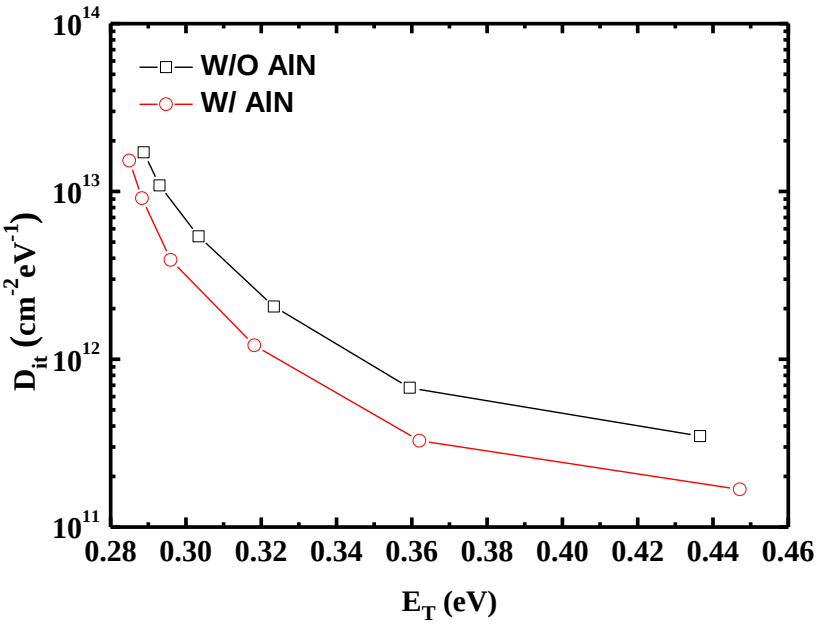


Fig. 4.34 Interface trap density extracted using the conductance method from MIS capacitors with AlON/AlHfON and AlN/AlON/AlHfON

Fig. 4.35 show the gate leakage current characteristics of devices with AlON/AlHfON and AlN/AlON/AlHfON. The gate breakdown voltage of devices with AlN/AlON/AlHfON was lower than that of devices with AlON/AlHfON. It was attributed to the low breakdown field characteristics of AlN as shown in the former section.

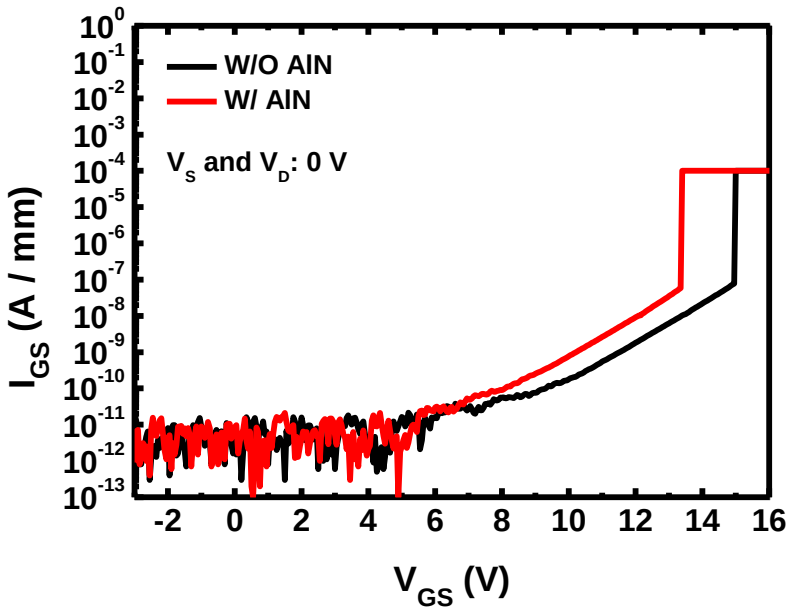


Fig. 4.35 Gate leakage characteristics of the fabricated devices with AlN/AlON/AlHfON and AlON/AlHfON

The off-state I-V characteristics of the fabricated devices are shown in Fig. 4.36. For the devices with AlN/AlON/AlHfON and AlON/AlHfON, the measured breakdown voltages defined at the drain current of 1 uA/mm were both 860 V at V_{GS} = 0 V.

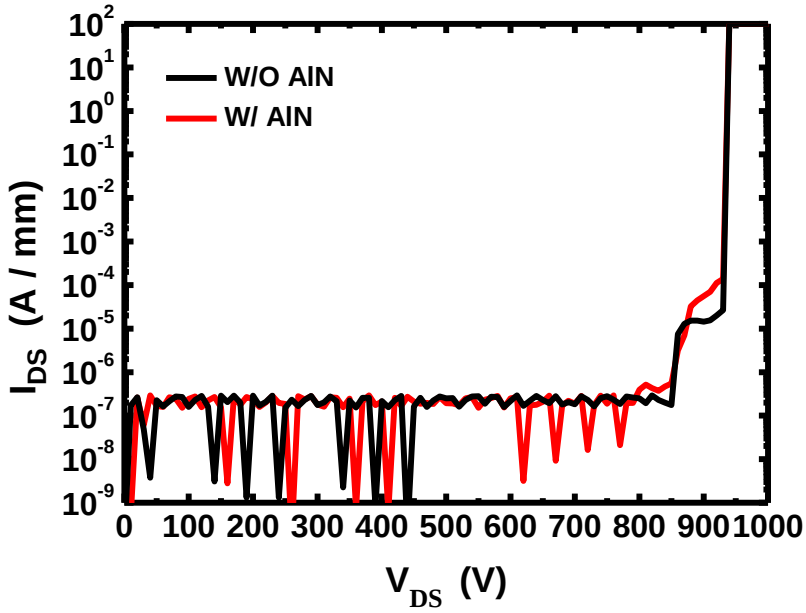


Fig. 4.36 Off-state I-V characteristics of the fabricated devices with AlN/AlON/AlHfON and AlON/AlHfON at V_{GS} = 0 V

Fig. 4.37 shows the specific on-resistance versus the breakdown voltage for the fabricated devices, including other results reported for E-mode GaN MIS-FETs. Compared to the other results, the devices using AlN showed the excellent specific on-resistance and breakdown voltage characteristics [27-35].

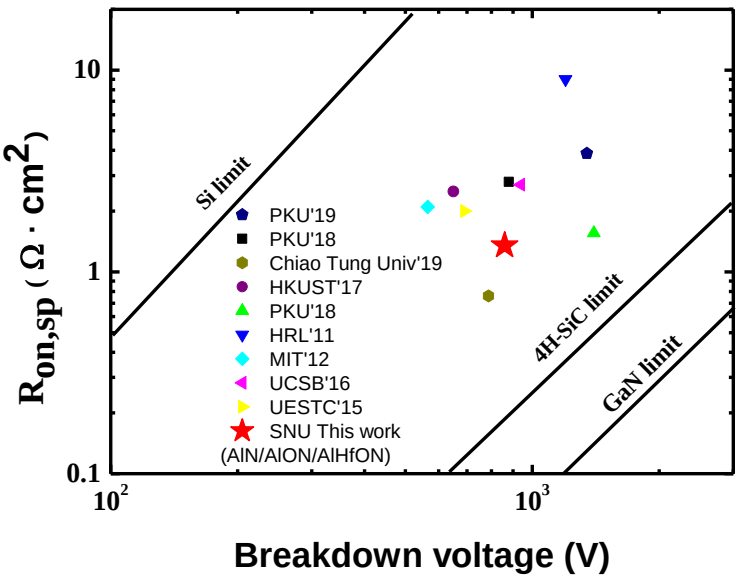


Fig. 4.37 Specific on-resistance versus the breakdown voltage for the fabricated devices, including other results reported for E-mode GaN MIS-FETs

Fig. 4.38 shows threshold voltage instability characteristics of the fabricated devices. The threshold voltage was measured at 1, 10, 100, 1000 s under the gate bias stress of 3.5, 4,5 and 5 V at room temperature and 5 V at 150 ℃. the threshold voltage drift of ~290 mV was measured in the device with AlN/AlON/AlHfON while large threshold voltage drift of ~716 mV was observed in the device with AlON/AlHfON after the stress time of 1000 s under the gate bias stress of 5 V. Also, smaller threshold voltage drift was confirmed at the device with AlN/AlON/AlHfON even at the high temperature of 150°C. Compared to the other results, the devices using AlN show less V_{th} shift after gate bias stress of 1000 sec as shown in Fig. 4.39. This result is attributed to the high quality AlGaN/dielectric interface by

ALD AlN.

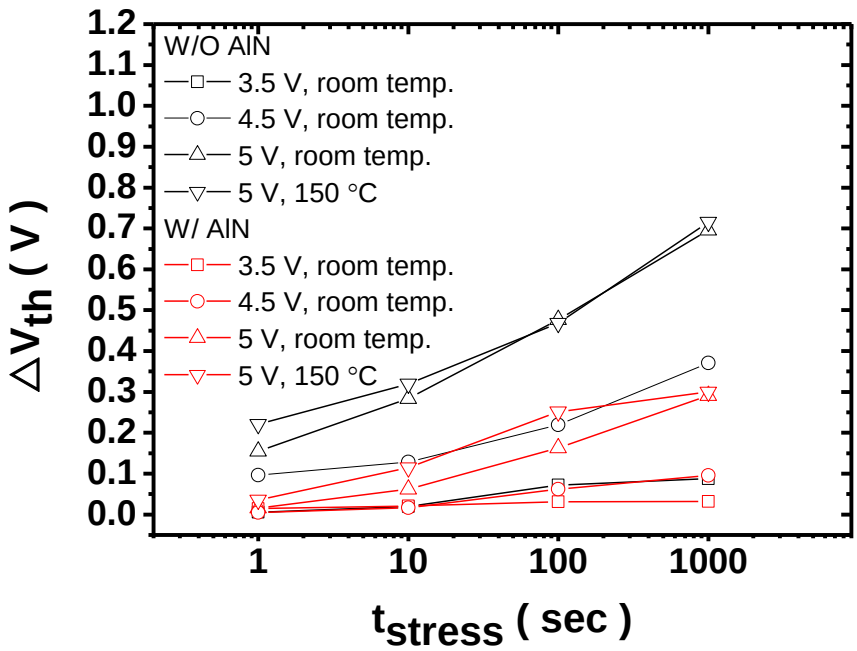


Fig. 4.38 Threshold voltage instability of the fabricated devices with AlN/AlON/AlHfON and AlON/AlHfON under various positive gate bias and stress time

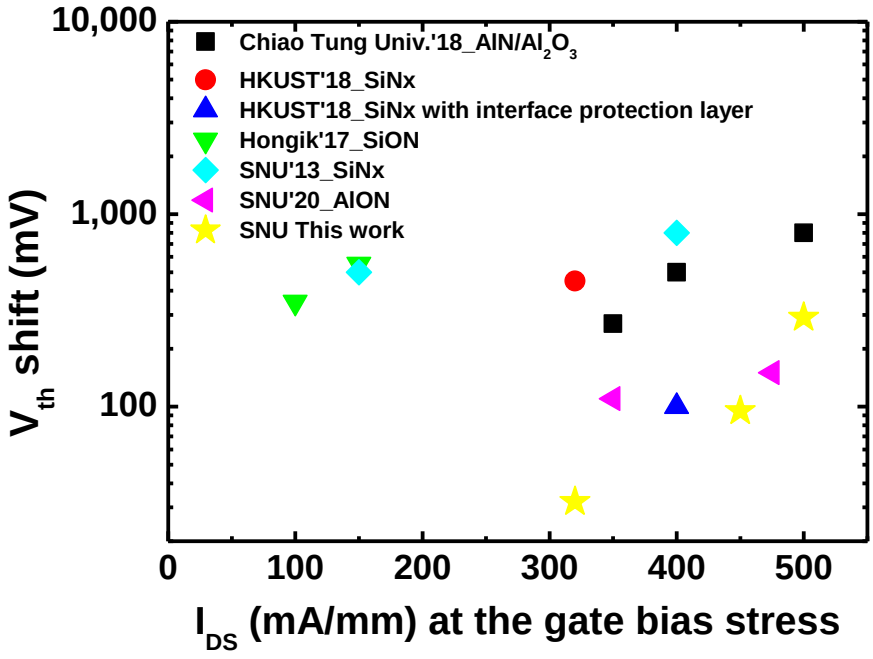


Fig. 4.39 V_{th} shift comparison with other normally-off GaN MIS-FETs under positive gate bias stress of 1000 sec

4.4. Conclusion

Poor-quality oxide (GaO_x) is detrimental to the dielectric/III-V interface quality that accounted for the V_{TH} instability issue in the III-V based devices. To avoid the formation of poor-quality oxide, we developed and optimized an ALD AlN as an interfacial layer. We also developed an ALD AlHfON as a bulk layer, which had a high dielectric constant and low leakage current and high breakdown field characteristics. Finally, Normally-off AlGaN/GaN MIS-FETs with 2 nm AlN/3 nm AlON/15 nm AlHfON layer were fabricated. Devices with 5 nm AlON/15 nm AlHfON layer were also fabricated for comparison. The maximum drain current density of devices with AlN/AlON/AlHfON layer was ~566 mA/mm while that of devices with AlON/AlHfON layer was ~466 mA/mm at V_{DS} of 10 V. Furthermore, Devices with AlN/AlON/AlHfON layer showed smaller I-V hysteresis of ~10 mV than that of devices with AlON/AlHfON layer. The extracted static R_{on} values of devices with AlN/AlON/AlHfON and AlON/AlHfON were 1.35 and 1.69 $m\Omega \cdot cm^2$, respectively. Besides, the effective mobility, D_{it} and threshold voltage instability characteristics were all improved by employing the ALD AlN. These results suggest that the ALD AlN/AlON/AlHfON gate dielectric is an excellent candidate for normally-off AlGaN/GaN MIS-FETs

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Chapter 5. Concluding Remarks

This study has been focused on the development of low damage etching process and high-quality gate stack for normally-off AlGaN/GaN MIS-FETs because charge trapping at the interface between gate dielectric and (Al)GaN and in the gate dielectric is a big issue for recessed gate MIS-HEMTs. This problem leads to degradation of channel mobility, on-resistance and on-current of the devices. Especially, V_{th} hysteresis after a positive gate voltage sweep and V_{th} shift under a gate bias stress are important reliability challenges in gate recessed MIS-HEMTs.

In order to minimize the V_{th} shift, a gate recess etching with low plasma induced damage and a high-quality gate dielectric are needed for low interface states and border traps in the gate recessed MIS-FETs.

For low etching damage, many research groups have studied various etching methods and resulted in great achievements. However, efforts to reduce the etching damage are still needed for improving the electrical performance and reliability of the devices. We propose the atomic layer etching which showed smoother etched surface, higher PL intensity and N/(Al+Ga) ratio of the etched AlGaN surface when compared to other etching methods. Also the gate recessed schottky devices using the ALE showed the lowest leakage current. Meanwhile, the poor-quality native oxide (GaO_x) is detrimental to the dielectric/III-V interface quality that accounted for the V_{TH} instability issue in the III-V based devices. To avoid surface oxidation, we developed and optimized AlN layer as an interfacial layer. we also investigated the electrical and material characteristics of ALD

AlHfON layers (AlON-HfO_2 laminate). The effect of ratio of Al to Hf on the electrical characteristics of AlHfON was also studied. After that, we optimized an AlN/AlON/AlHfON layer as a gate insulator. The ALD AlN interfacial layer suppressed unintentional interfacial oxide and the AlHfON efficiently reduced the leakage current and increased the dielectric constant of the gate insulator. In the device results, AlGaN/GaN MIS-FETs with AlN/AlON/AlHfON layer showed smaller I-V hysteresis of ~10 mV than that of devices with AlON/AlHfON layer. The extracted static R_{on} values of devices with AlN/AlON/AlHfON and AlON/AlHfON were 1.35 and 1.69 $m\Omega \cdot cm^2$, respectively. Besides, the effective mobility, D_{it} and threshold voltage instability characteristics were all improved by employing the ALD AlN. These results prove that the developed AlN/AlON/AlHfON stack have a lot of potential for high performance normally-off AlGaN/GaN MIS-FETs.

Appendix

A. N_2 plasma treatment before dielectric deposition

The results were reported at the 24th Korean Conference on Semiconductors 2017.

1	Pre-passivation (SiNx)
2	Ohmic metal deposition
3	Mesa etching
4	Pre-passivation film removing
5	Passivation layer deposition
6 (Gate recess)	SiN_x Opening
	AlGaN etching (AlGaN 2nm remain)
	cleaning
7	**Surface treatment** **1. w/o N_2 plasma treatment** **2. w/ N_2 plasma treatment** **(Microwave plasma, 20W, 3min)**
8	Al_2O_3 Gate dielectric deposition
9	Post deposition annealing (500℃, 10min)
10	Gate metal deposition (Ni/Au)

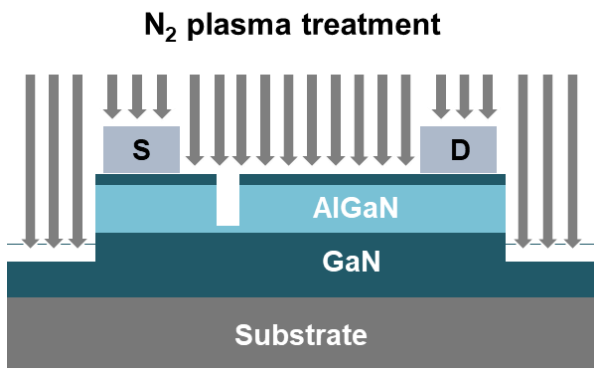


Figure A.1 (a) Process flow for normally-off AlGaN/GaN MIS-FETs using N_2 plasma treatment

(a)

(b)

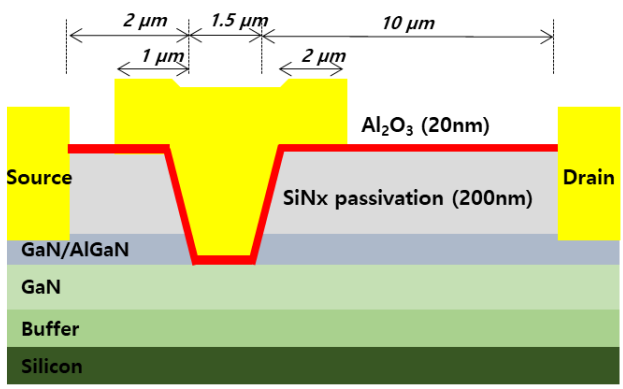
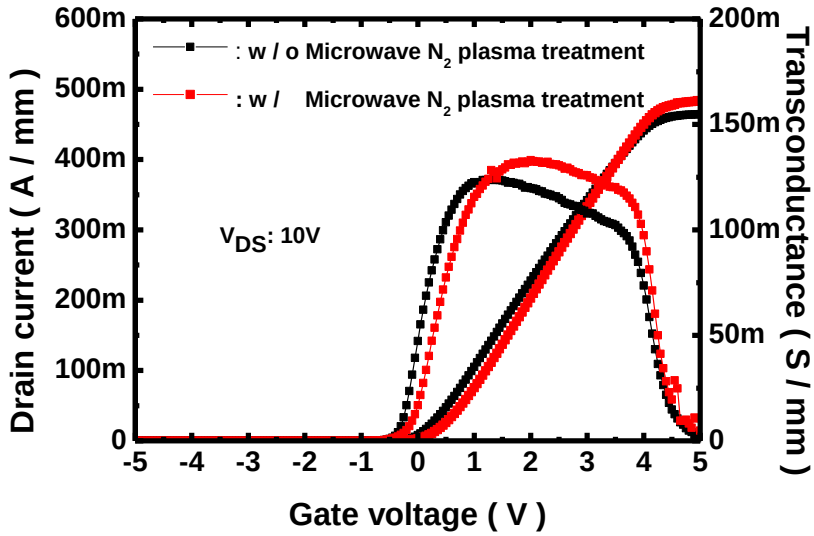


Figure A.2 (a) Microwave reactor (Plasma-finish, V15-G, Germany) for N_2 plasma treatment and (b) schematic of the fabricated normally-off AlGaN/GaN MIS-FETs



	W/O N_2 plasma treatment	W/ N_2 plasma treatment
Maximum drain current (mA/mm)	464	483
Peak transconductance (mS/mm)	124	133
Off-state drain leakage current (A/mm)	1.6×10^{-11}	2.8×10^{-11}

Figure A.3 (a) Microwave reactor (Plasma-finish, V15-G, Germany) for N_2 plasma treatment and (b) schematic of the fabricated normally-off AlGaN/GaN MIS-FETs

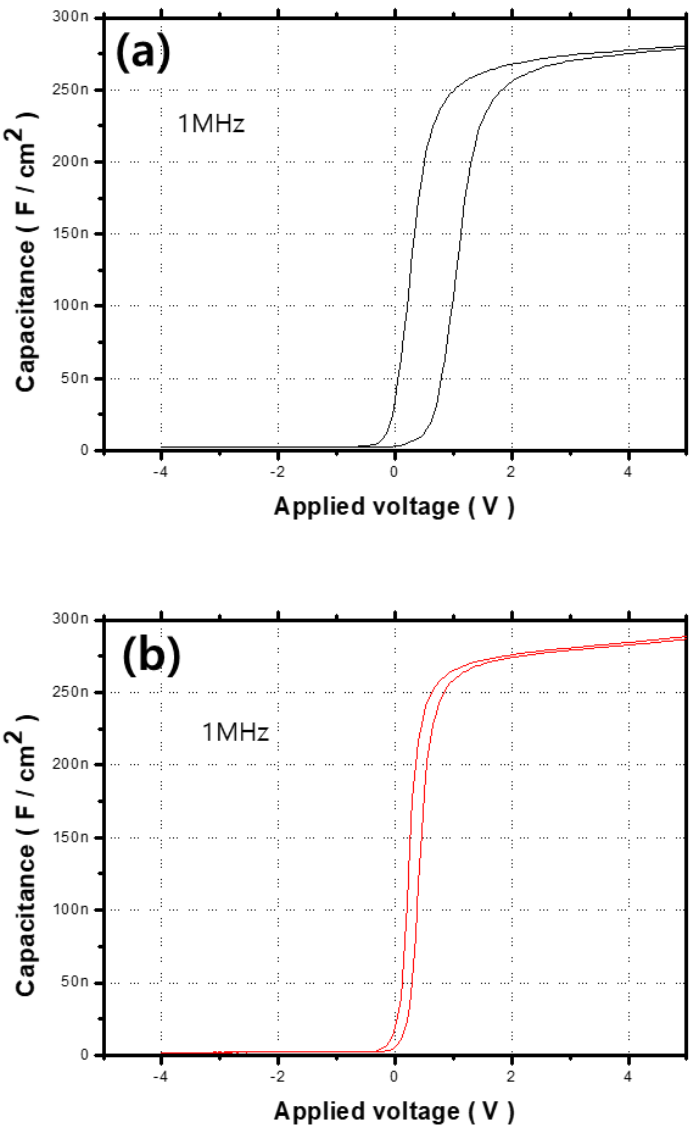


Figure A.4 C-V curve of MIS capacitor (a) without N_2 plasma treatment and (b) with N_2 plasma treatment

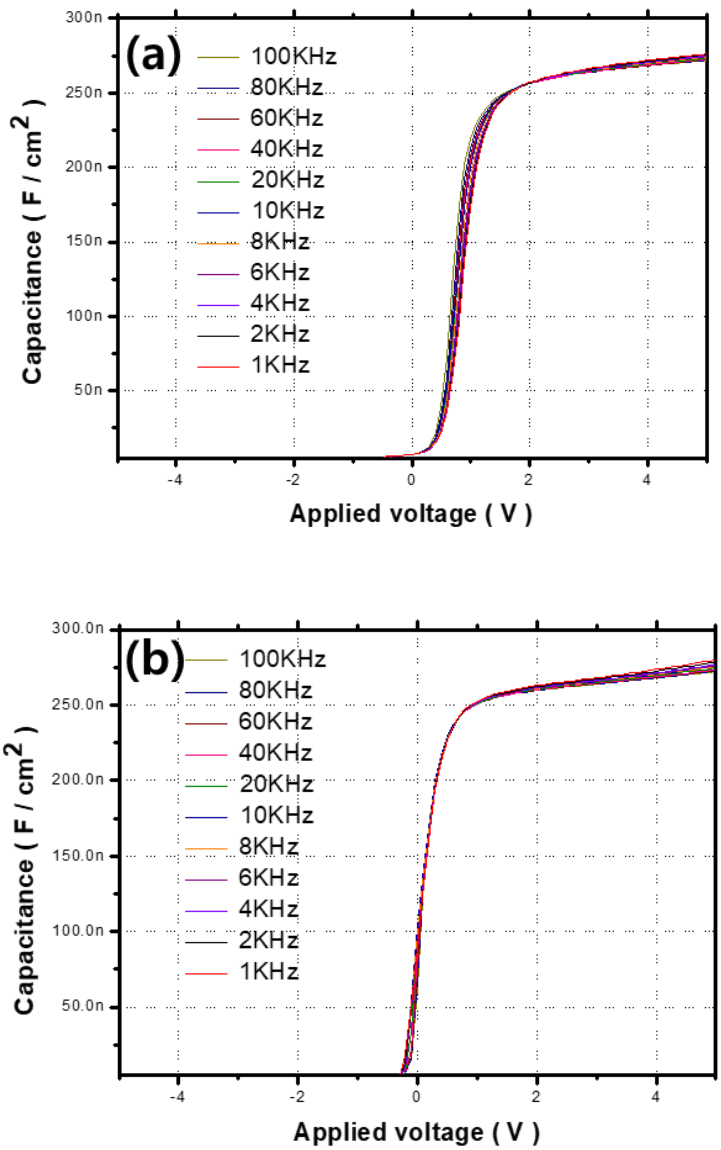
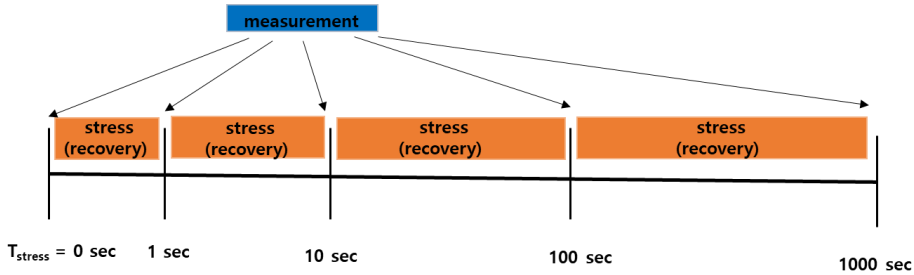
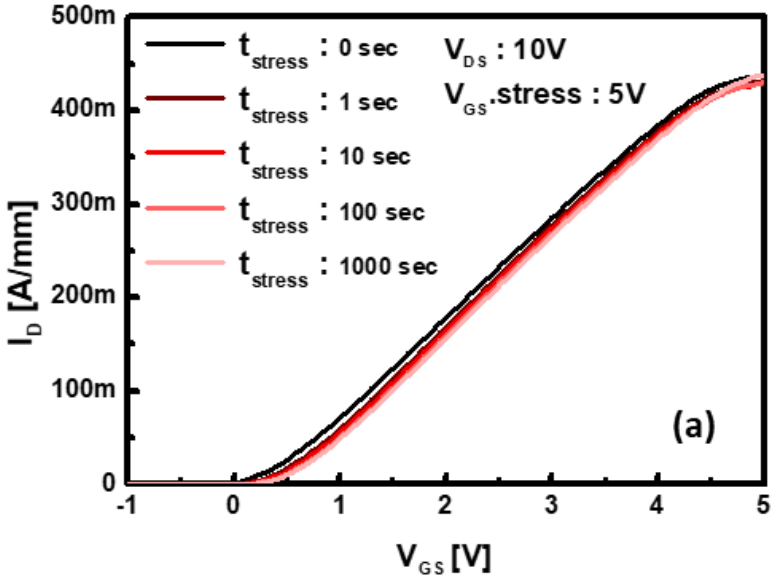


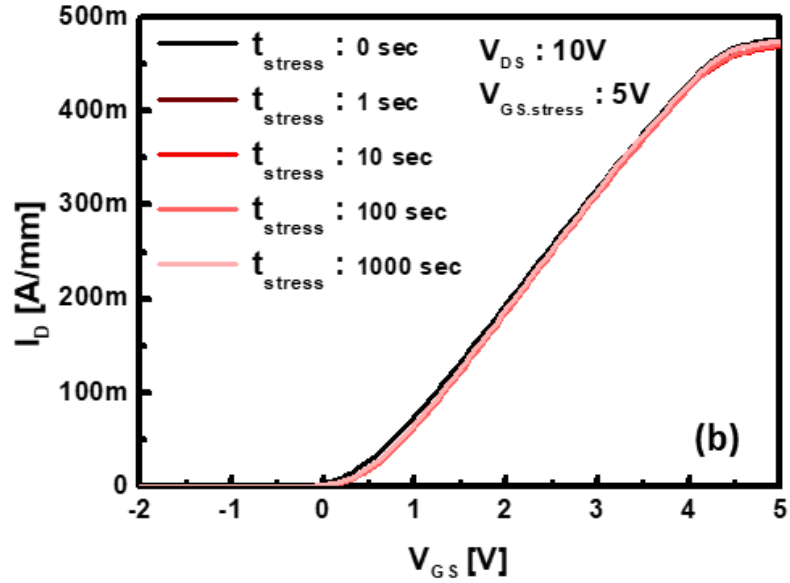
Figure A.5 CV frequency dispersion characteristics of MIS capacitor (a) without N_2 plasma treatment and (b) with N_2 plasma treatment



- ***Stress condition : $V_D = V_S = 0$ V***
  positive gate bias (5V), negative gate bias (-5V)
- ***Compare two samples with same gate bias.***
- ***Temperature condition : room temp.***

Figure A.6 Stress-recovery measurement method for capture emission time (CET) map


500m
400m
300m
200m
100m
0
I_D [A/mm]
-1
0
1
2
3
4
5
V_{GS} [V]
t_{stress} : 0 sec
t_{stress} : 1 sec
t_{stress} : 10 sec
t_{stress} : 100 sec
t_{stress} : 1000 sec
V_{DS} : 10V
V_{GS}.stress : 5V
(a)


500m
400m
300m
200m
100m
0
I_D [A/mm]
-2
-1
0
1
2
3
4
5
V_{GS} [V]
t_{stress} : 0 sec
t_{stress} : 1 sec
t_{stress} : 10 sec
t_{stress} : 100 sec
t_{stress} : 1000 sec
V_{DS} : 10V
$V_{GS.stress}$: 5V
(b)

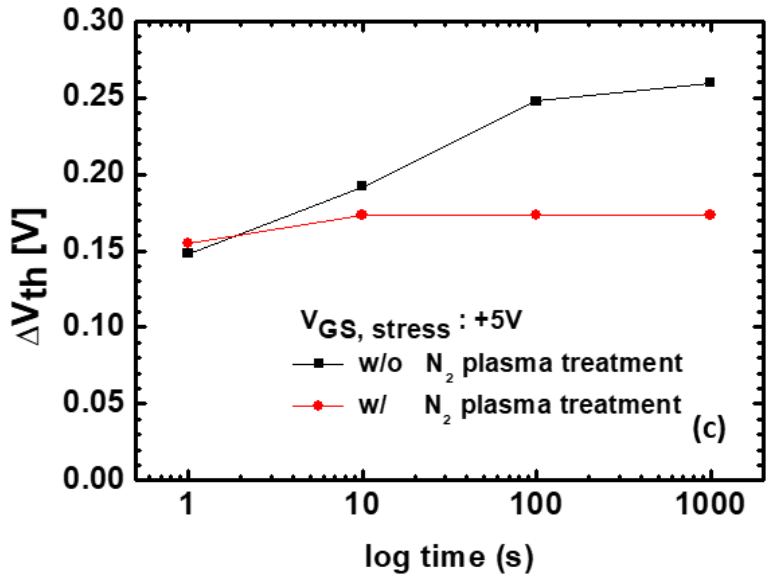
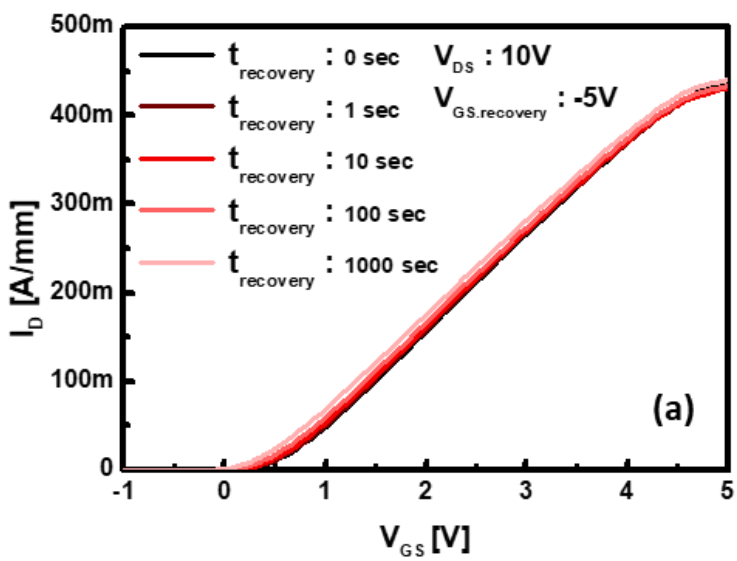
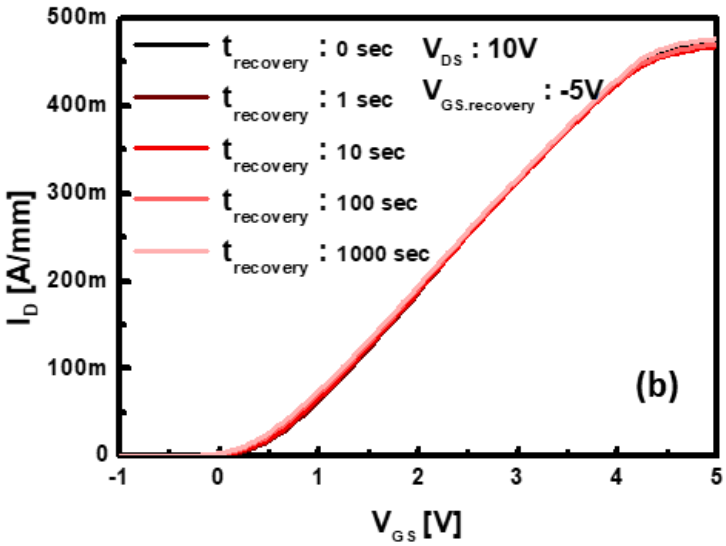


Figure A.7 Consecutive transfer characteristics with increasing stress time for (a) device without N_2 plasma treatment and (b) device with N_2 plasma treatment. (c) $\triangle V_{th}$ – log time curve for the fabricated devices with increasing stress time





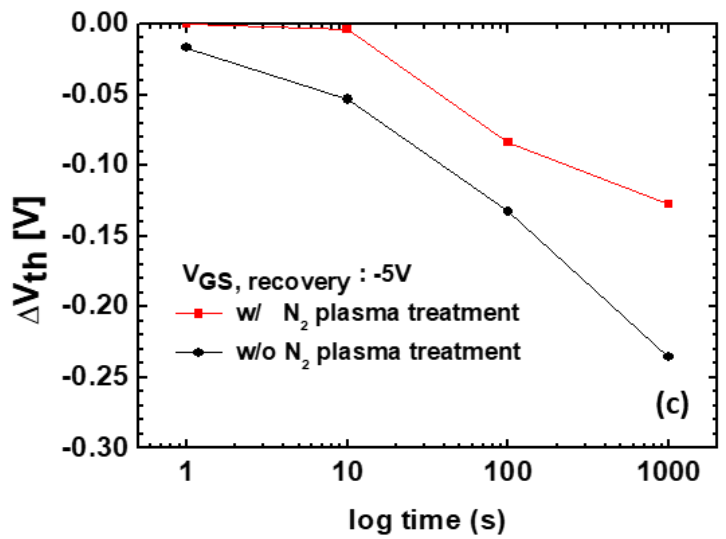


Figure A.8 Consecutive transfer characteristics with increasing recovery time for (a) device without N_2 plasma treatment and (b) device with N_2 plasma treatment. (c) $\triangle V_{th}$ – log time curve for the fabricated devices with increasing recovery time

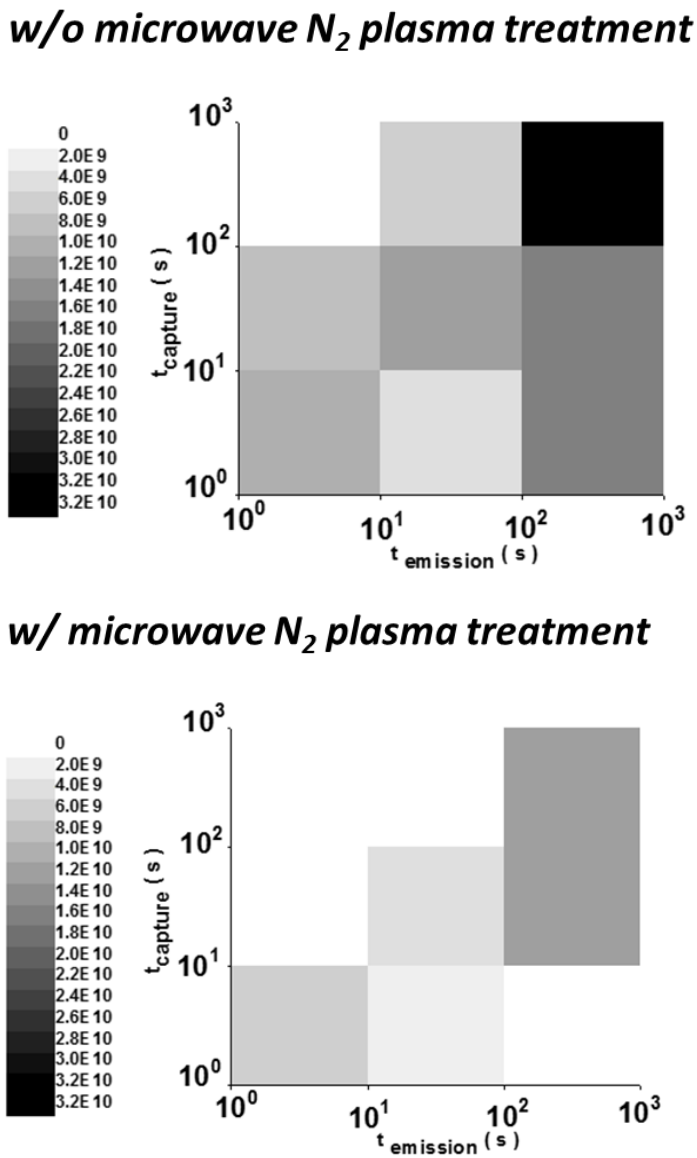


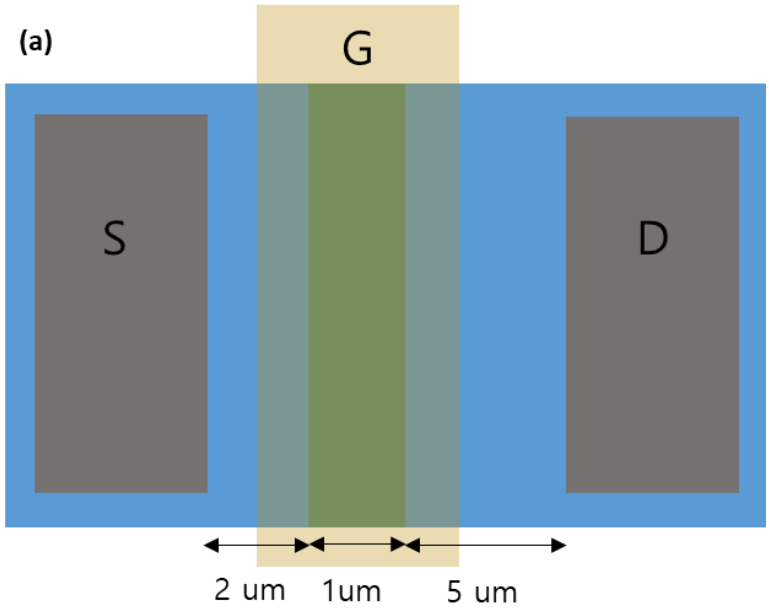
Figure A.9 Capture emission time map (CET map) of the fabricated devices

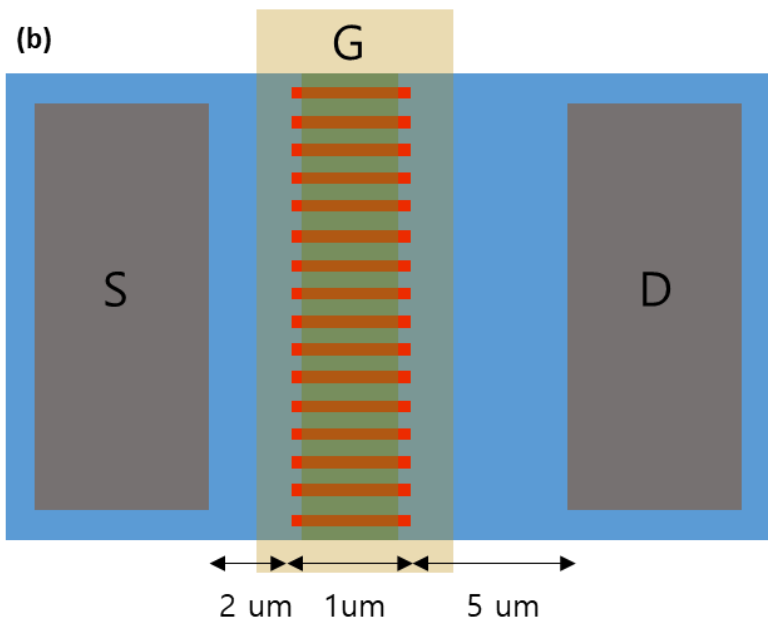
Devices without N_2 plasma treatment show higher trap density with long time constant and emission time constant. Overall, devices with N_2 plasma treatment show lower trap density.

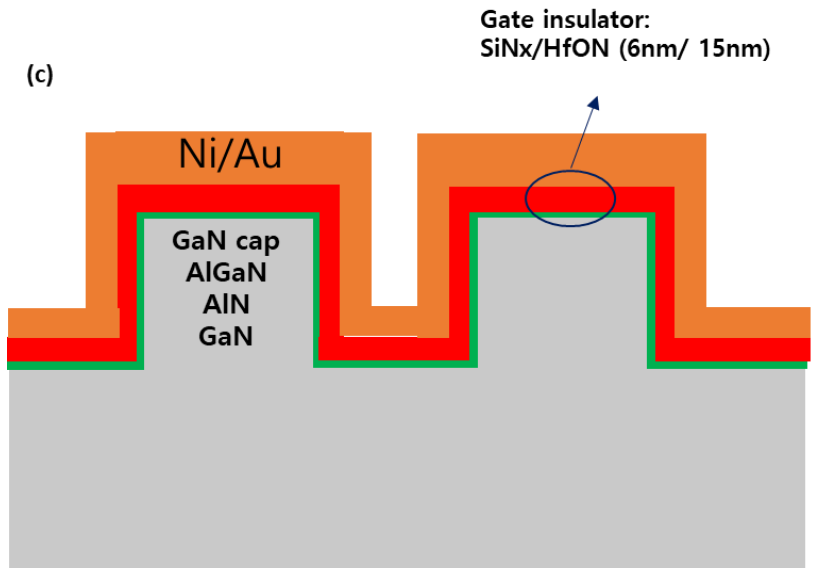
B. Tri-gate normally-on/off AlGaN/GaN MIS-FETs

1	Solvent cleaning
2	Ohmic (Ti/Al/Ni/Au=20/120/25/50 nm)
3	Mesa etching
4	Passivation (Cat-CVD 60 nm)
5	Fin definition (E-beam litho.)
6	SiN_x opening
7	BCl_3/Cl_2 based etching (130 nm)
8	Etching of SiN_x on Fin by wet etching
9	Cleaning (SPM & BOE 30:1)
10	Gate insulator deposition (PEALD SiN_x 6 nm + HfON 15 nm)
11	Post deposition annealing (500℃, 10min, N_2 ambient)
12	SiN_x opening
13	Gate metal deposition (Ni/Au=40/200 nm)

Figure B.1 Process flow for tri-gate normally-on AlGaN/GaN MIS-FETs


(a)
G
S
D
2 um
1um
5 um


(b)
G
S
D
2 um
1um
5 um



Fin width : Spacing between Fins = 1 : 1

Fin width : 500, 300, 200, 150, 100 nm

Gate length: 1um

Fin # : 250

Gate insulator: SiNx/HfON (6nm/ 15nm)

Figure B.2 Cross-section of the (a) planar AlGaN/GaN MIS-FETs and (b, c) tri-gate normally-on AlGaN/GaN MIS-FETs.

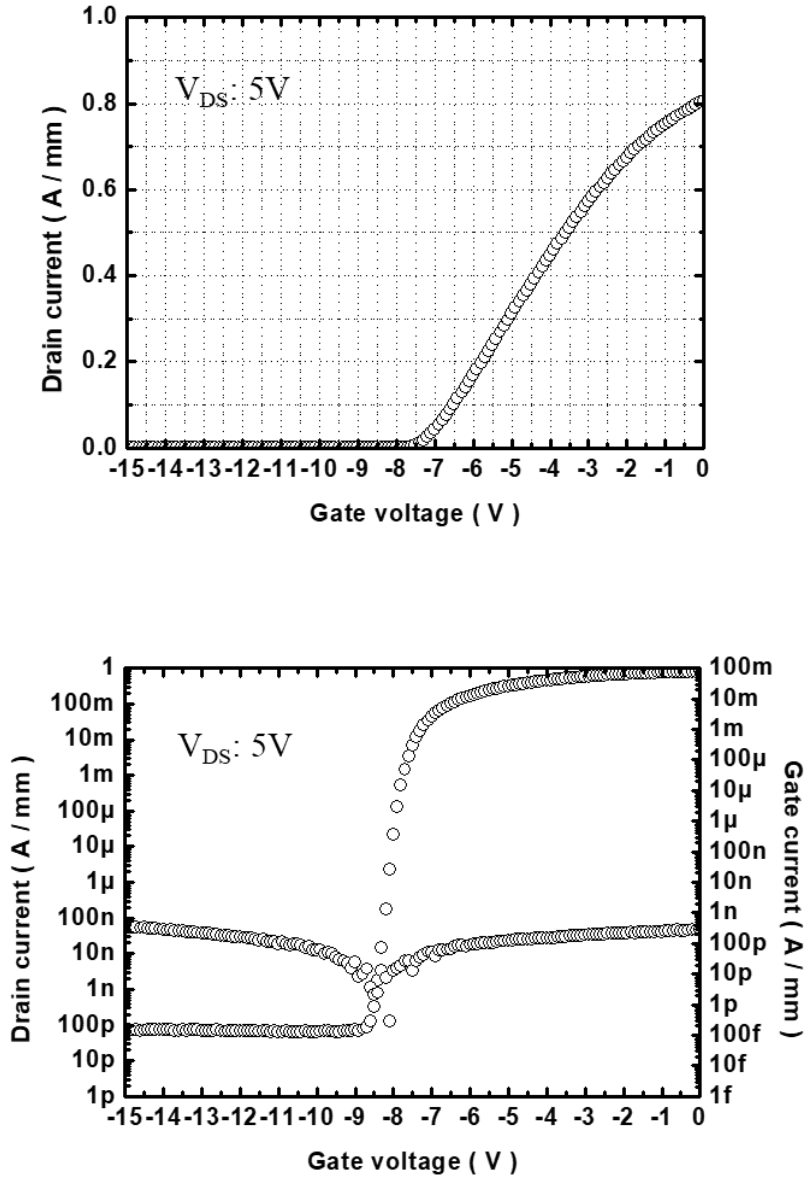


Figure B.3 Linear and log-scaled transfer curves of the normally-on planar AlGaN/GaN MIS-FETs

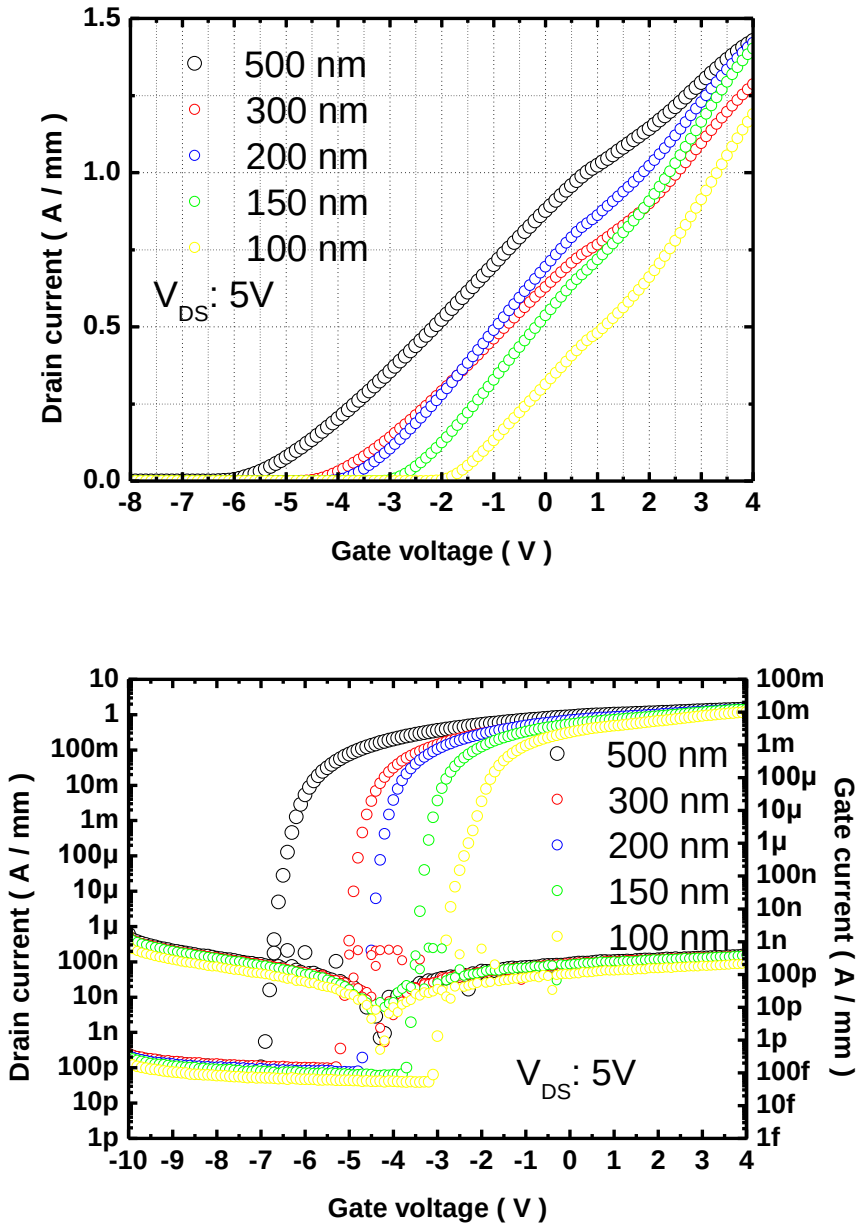


Figure B.4 Linear and log-scaled transfer curves of the normally-on tri-gate AlGaN/GaN MIS-FETs

1	Solvent cleaning
2	Ohmic (Ti/Al/Ni/Au=20/120/25/50 nm)
3	Mesa etching
4	Passivation (Cat-CVD 60 nm)
5	Fin definition (E-beam litho.)
6	SiN_x opening
7	BCl_3/Cl_2 based etching (130 nm)
8	Etching of SiN_x on Fin by wet etching
9	Additional BCl_3/Cl_2 based etching for normally-off operation (remaining AlGaN barrier layer thickness: ~2 nm)
10	Cleaning (SPM & BOE 30:1)
11	Gate insulator deposition (PEALD SiN_x 6 nm + HfON 15 nm)
12	Post deposition annealing (500℃, 10min, N_2 ambient)
13	SiN_x opening
14	Gate metal deposition (Ni/Au=40/200 nm)

Figure B.5 Process flow for tri-gate normally-off AlGaN/GaN MIS-FETs

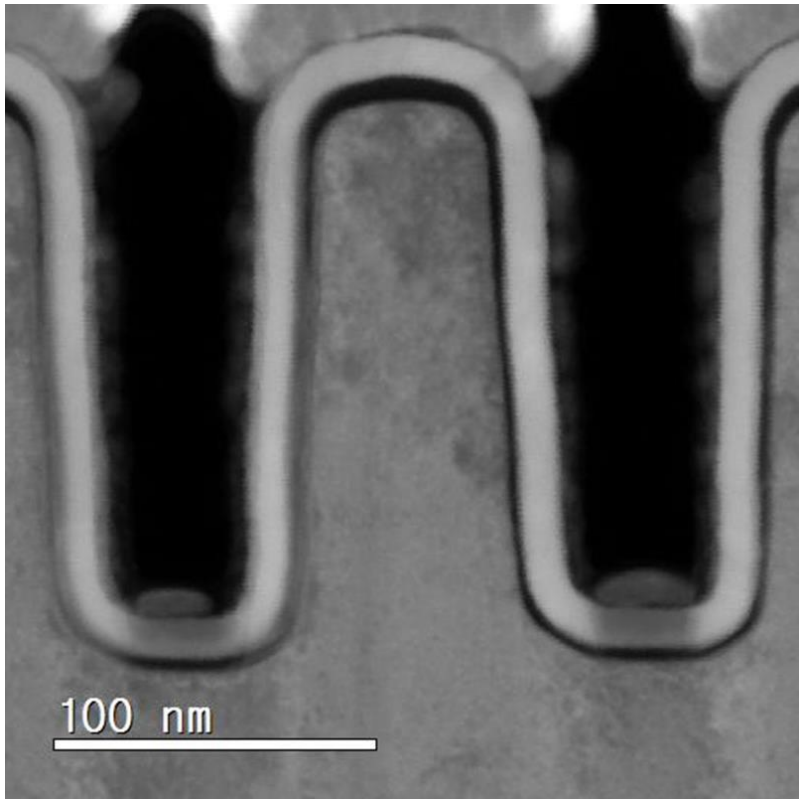


Figure B.6 Tem result of the fin width of 50 nm in the tri-gate normally-off AlGaN/GaN MIS-FETs

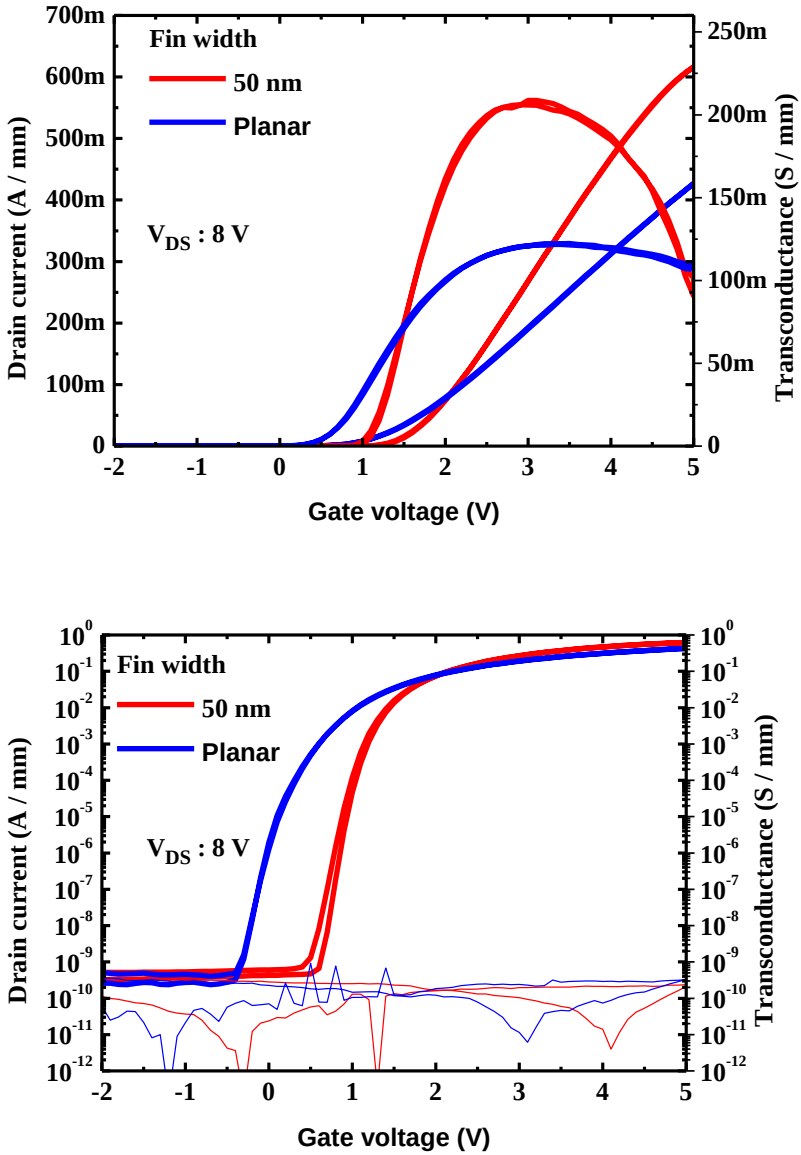


Figure B.7 Linear and log-scaled transfer curves of the normally-off tri-gate AlGaN/GaN MIS-FETs with 50 nm fin width and the planar AlGaN/GaN MIS-FETs (L_{GS}: 2 um, L_G: 1 um and L_{GD}: 10 um)

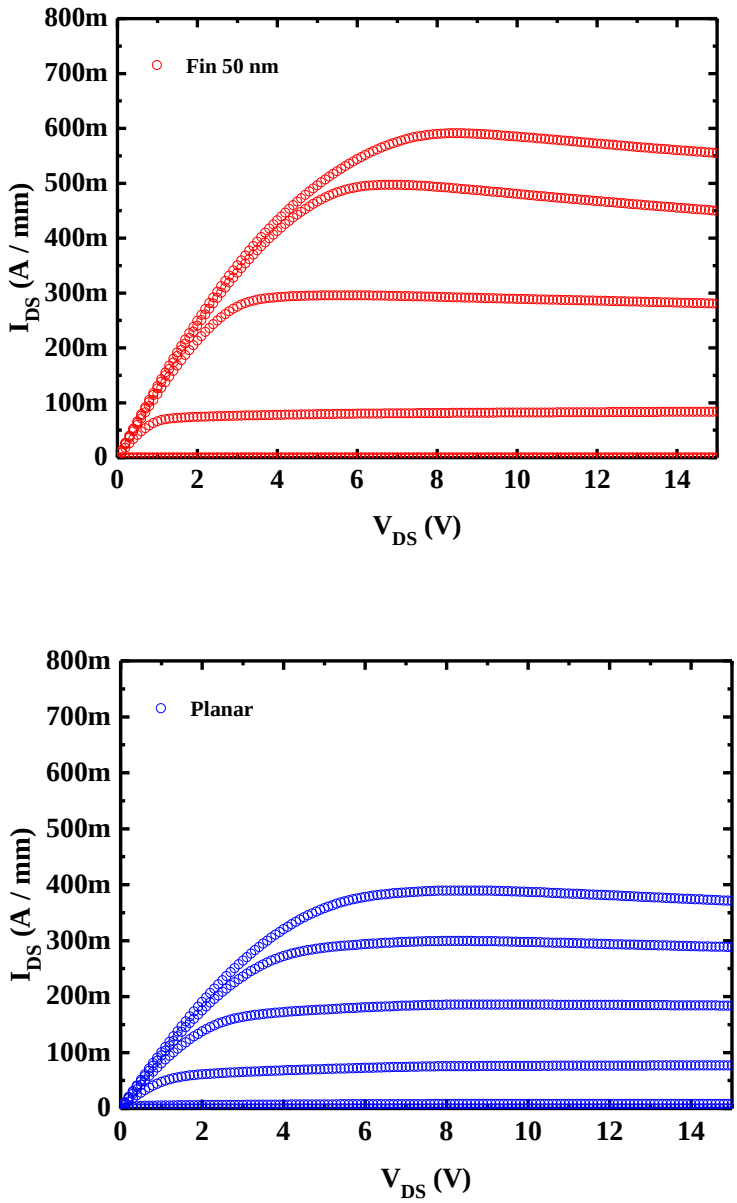


Figure B.8 Family curves of the fabricated normally-off tri-gate AlGaN/GaN MIS-FETs with 50 nm fin width and the planar AlGaN/GaN MIS-FETs (L_{GS}: 2 um, L_G: 1 um and L_{GD}: 10 um)

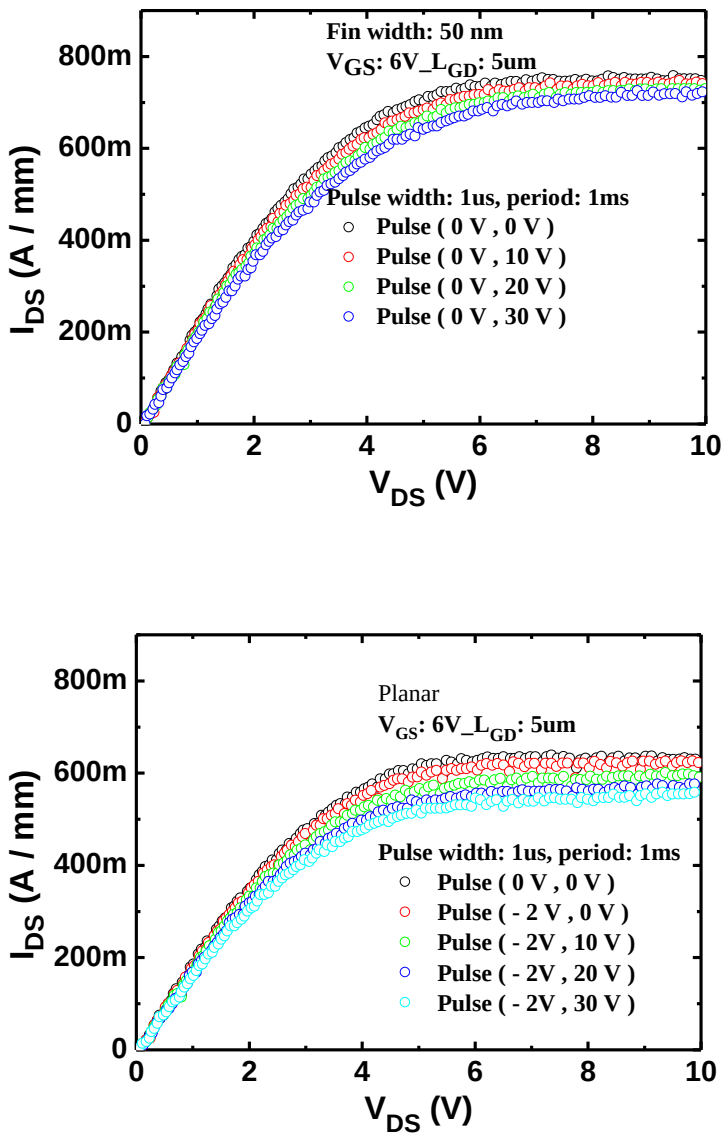


Figure B.9 Pulsed I-V characteristics of the fabricated normally-off tri-gate AlGaN/GaN MIS-FETs with 50 nm fin width and planar AlGaN/GaN MIS-FETs (L_{GS}: 2 um, L_G: 1 um and L_{GD}: 5 um)

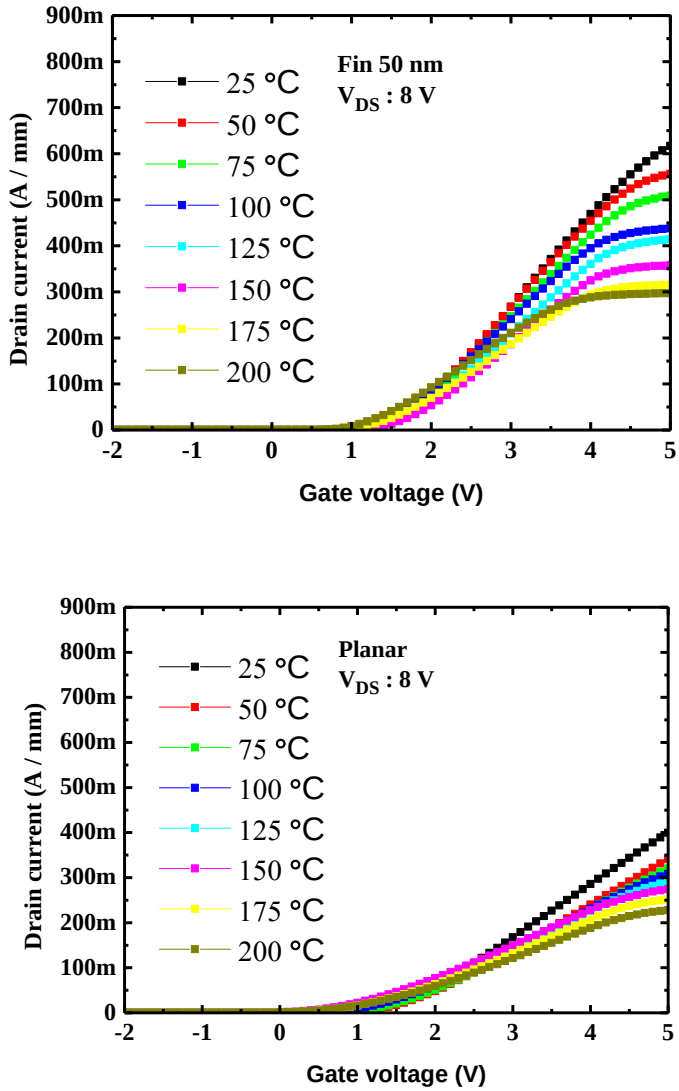


Figure B.10 Linear-scaled transfer characteristics of the fabricated normally-off tri-gate AlGaN/GaN MIS-FETs with 50 nm fin width and planar AlGaN/GaN MIS-FETs at room and increased temperatures (L_{GS}: 2 um, L_G: 1 um and L_{GD}: 10 um)

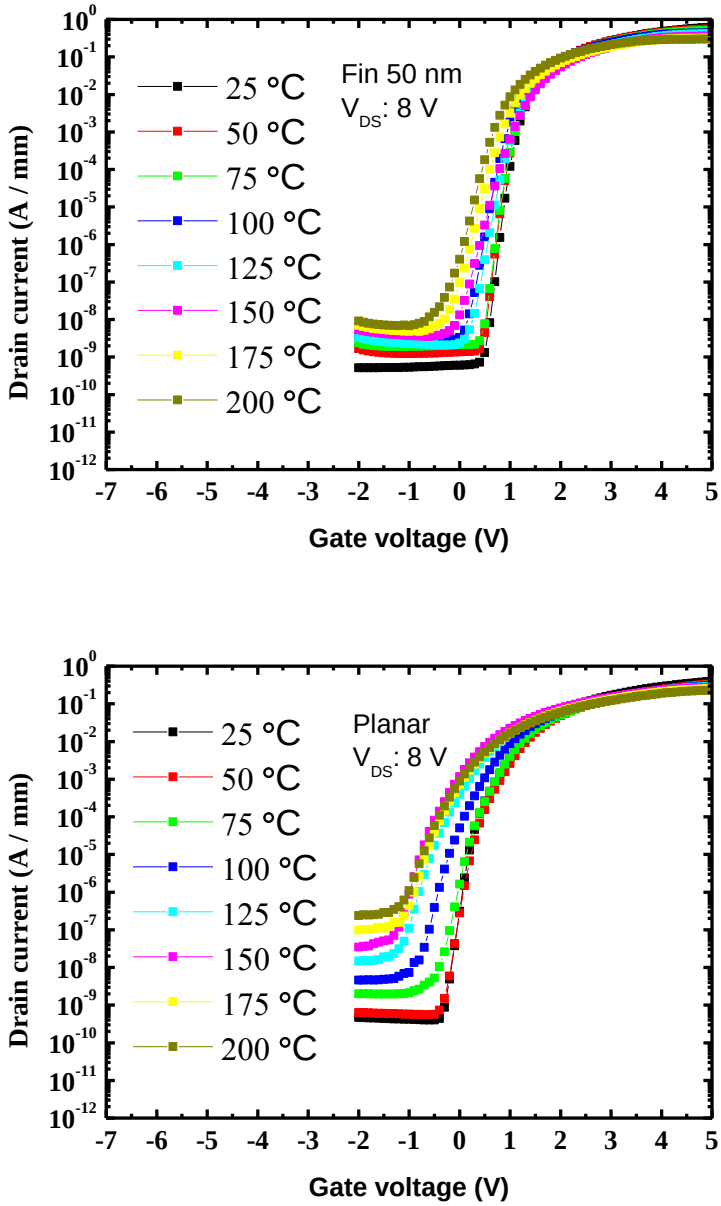


Figure B.11 Log-scaled transfer characteristics of the fabricated normally-off tri-gate AlGaN/GaN MIS-FETs with 50 nm fin width and planar AlGaN/GaN MIS-FETs at room and increased temperatures (L_{GS}: 2 um, L_G: 1 um and L_{GD}: 10 um)

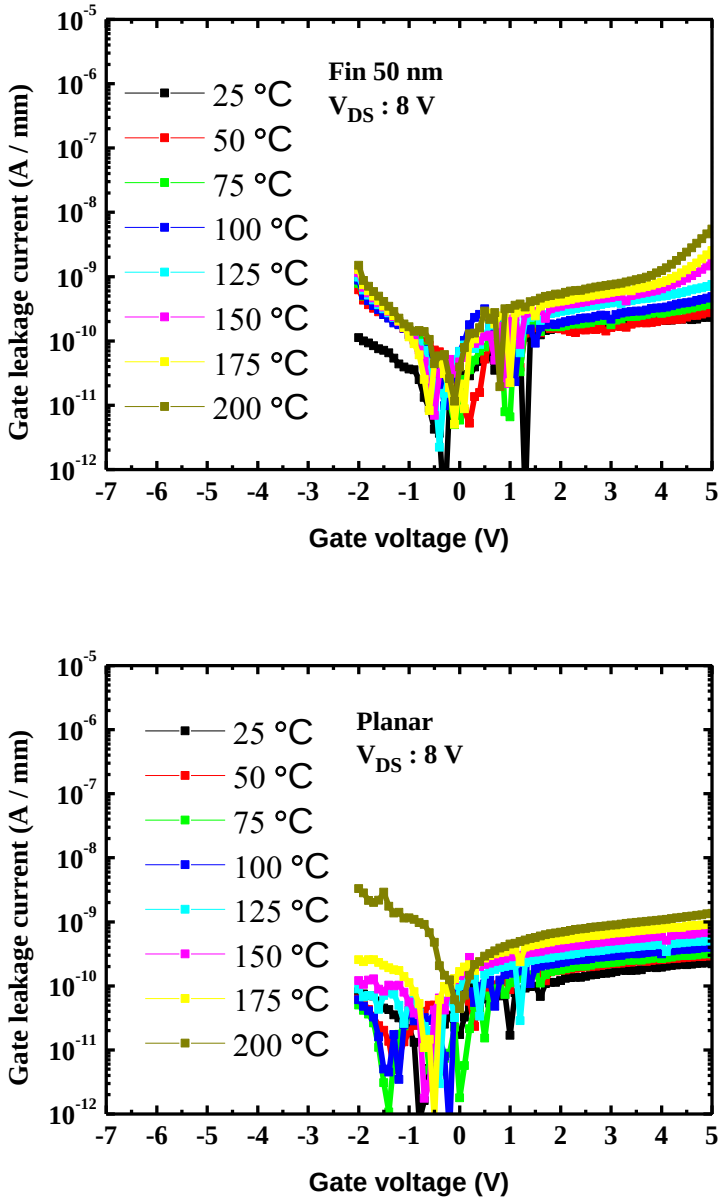


Figure B.12 Gate leakage current of the fabricated normally-off tri-gate AlGaN/GaN MIS-FETs with 50 nm fin width and planar AlGaN/GaN MIS-FETs at room and increased temperatures (L_{GS}: 2 um, L_G: 1 um and L_{GD}: 10 um)

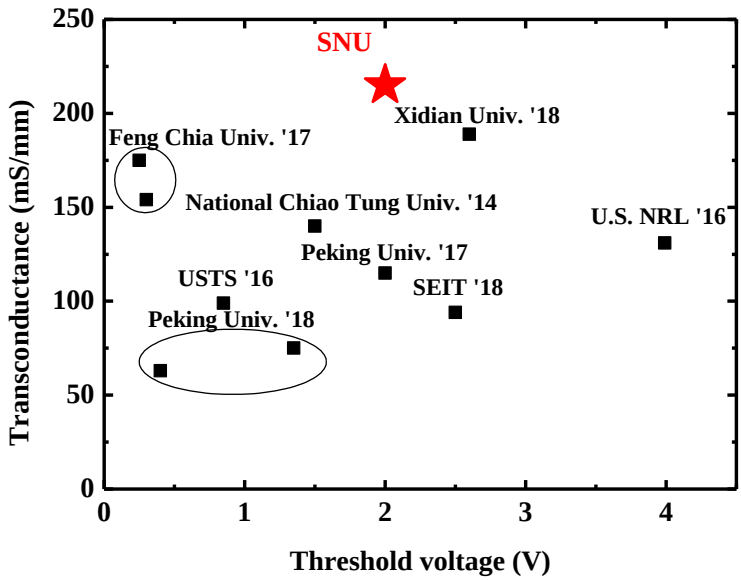


Figure B.13 Benchmark of threshold voltage and transconductance for normally-off tri-gate AlGaN/GaN MIS-FETs with 50 nm fin width

C. AlGan/GaN diode with MIS-gated hybrid anode and edge termination

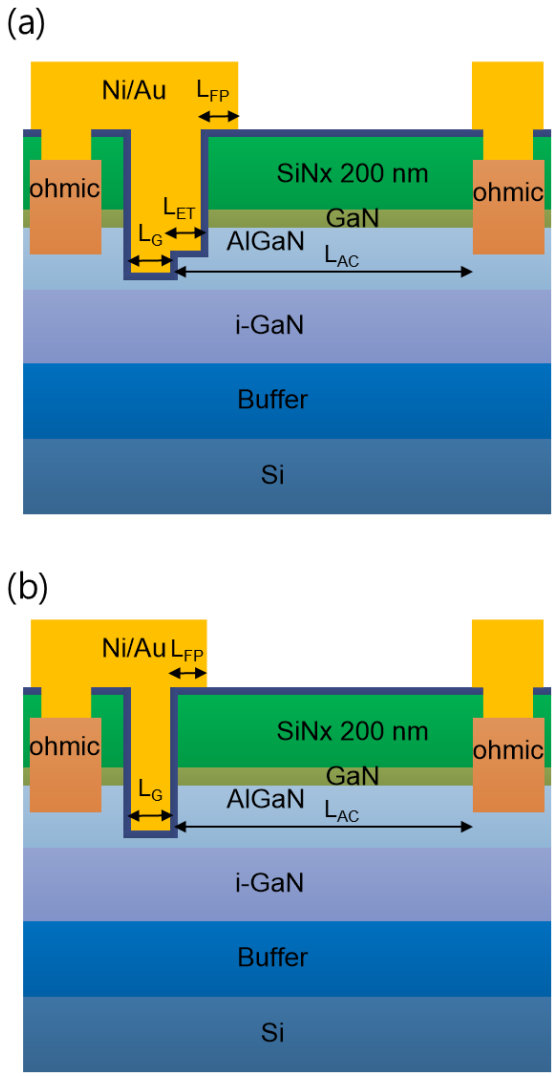


Figure C.1 The schematic cross section of MIS-gated hybrid anode AlGaN/GaN diodes (a) with edge termination and (b) without edge termination

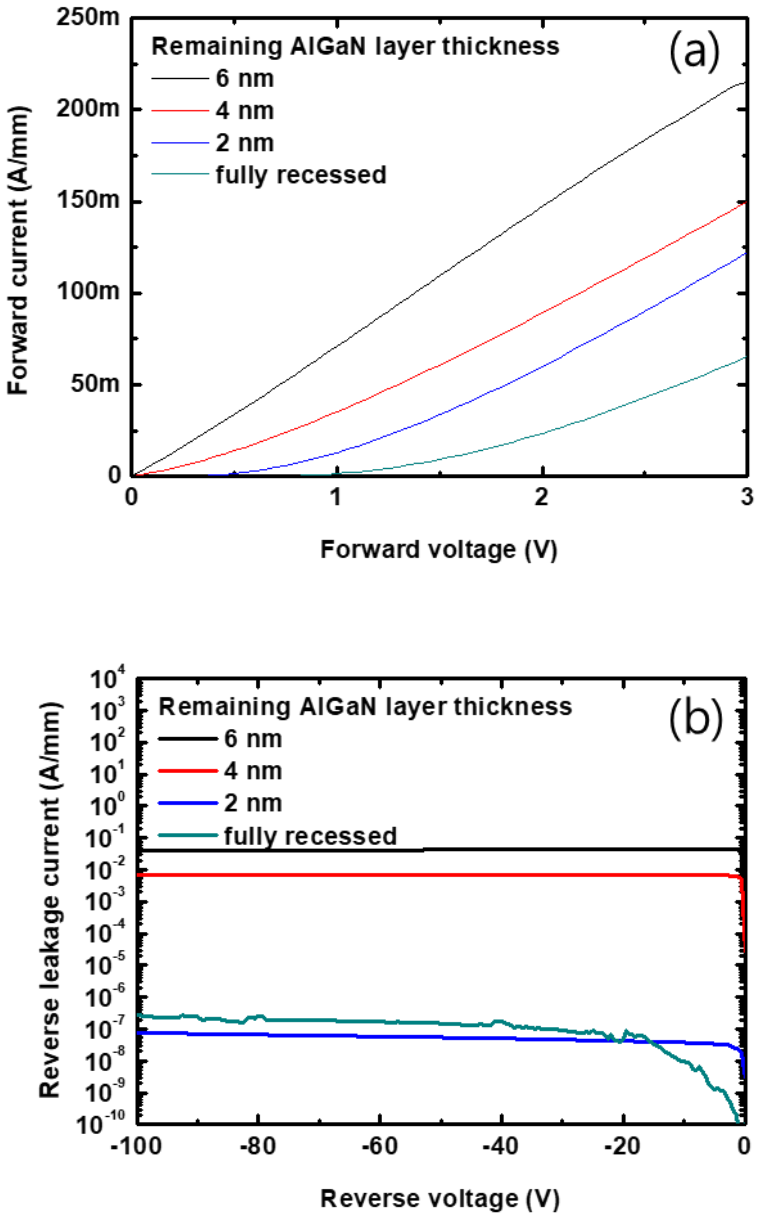


Figure C.2 (a) Forward and (b) reverse characteristics of the fabricated MIS-gated hybrid anode diode with edge termination

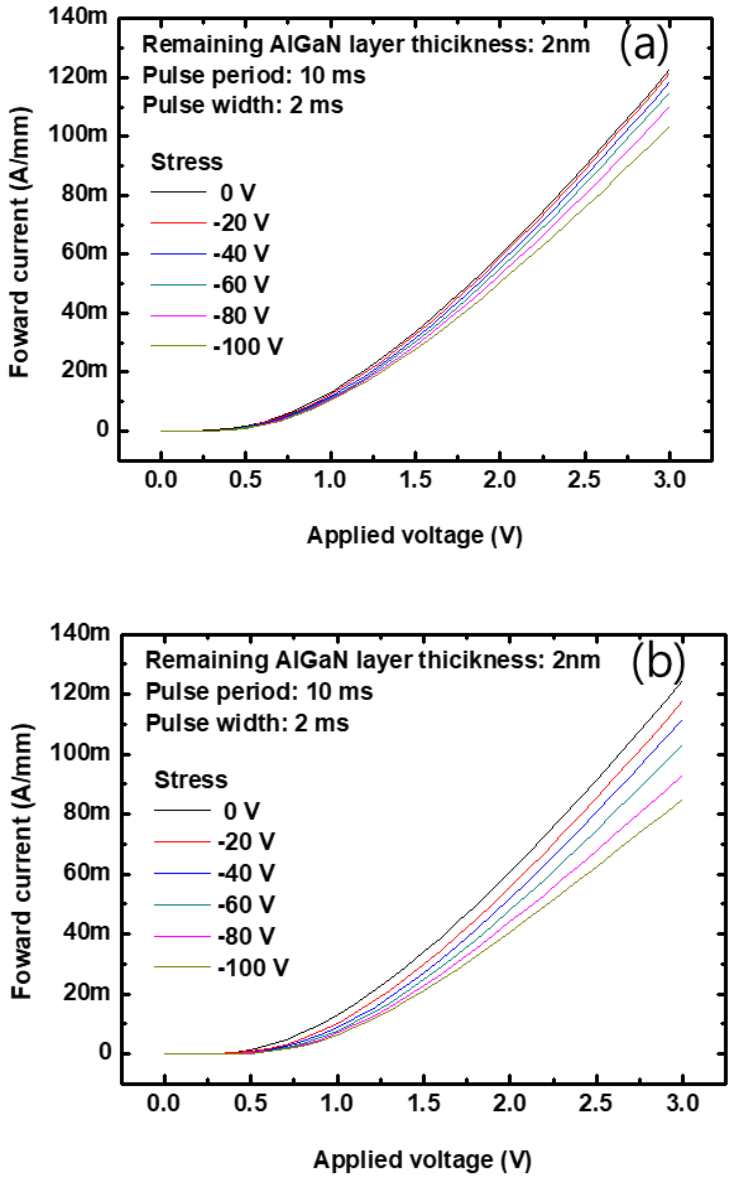


Figure C.3 Pulsed I-V characteristics of fabricated MIS-gated hybrid anode diode (a) with edge termination and (b) without edge termination

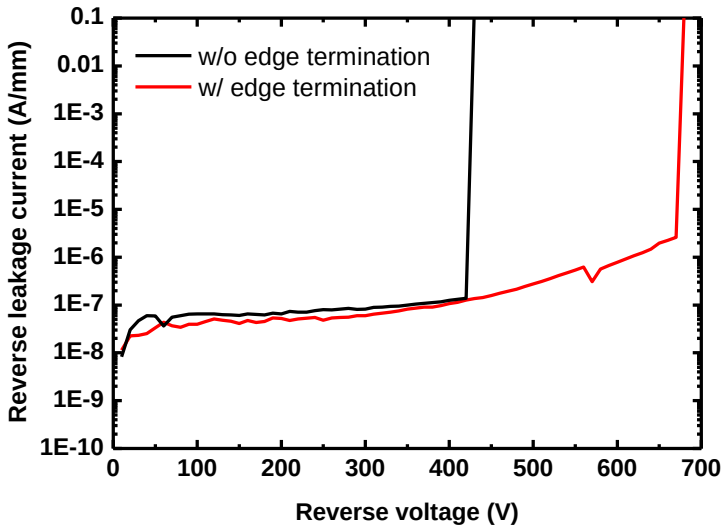


Figure C.4 Breakdown voltage characteristics of the fabricated MIS-gated hybrid anode diode with edge termination and without edge termination

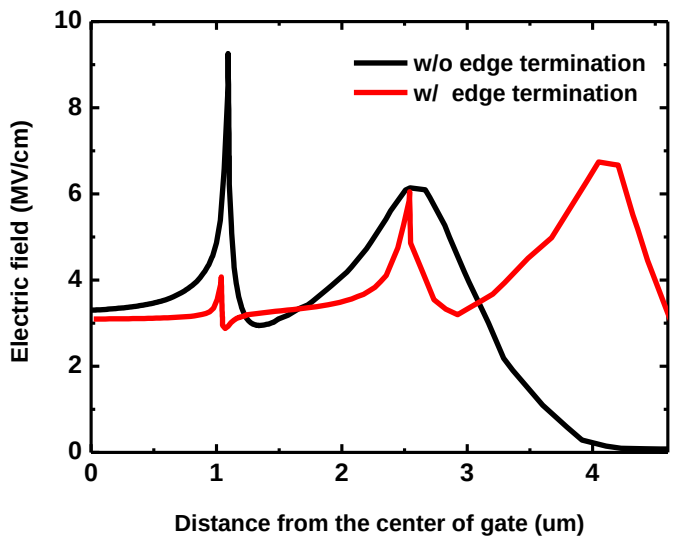


Figure C.5 Simulated electric-field distributions of the fabricated diodes at the 2DEG channel and reverse voltage of -500 V

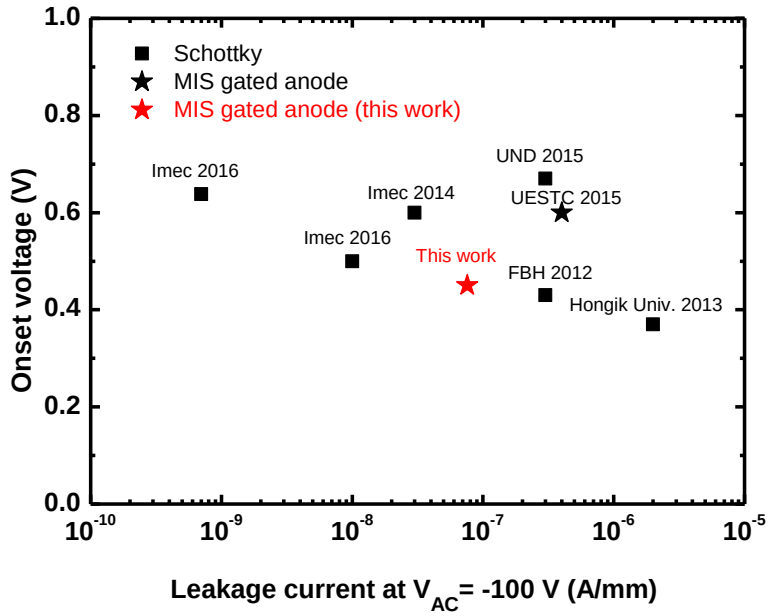


Figure C.6 Benchmark of off-state leakage current and onset voltage for the fabricated MIS-gated hybrid anode diode with edge termination

Abstract in Korean

최근 에너지 위기와 환경규제 강화, 친환경 녹색성장 등의 이슈가 대두되어 에너지 절감과 환경 보호 분야에 IT 기술을 접목, 활용하는 그린 IT 패러다임이 부각되고 있다. 현재 고유가 환경규제 강화에 대응하기 위해 하이브리드 자동차, 전기자동차 등 친환경 미래형 자동차 개발이 요구되고 있으며, 자동차에서 전장부품이 차지하는 원가비중은 약 40%까지 달할 것으로 전망되고 이 중 반도체가 차지하는 비용은 약 30% 정도로 추정된다. 이러한 자동차 전장부품에서 전력소자가 핵심부품으로 자리 잡을 전망이다. 지금까지는 실리콘 기반의 전력소자 기술이 전력반도체 시장의 대부분을 주도하고 있지만 전력기기 로드맵에 의하면 전력밀도가 해를 거듭하면서 지속적으로 증가하기 때문에 내열, 내압, 전력손실, 전력밀도 등에서 나타나는 많은 한계를 가지고 있는 현재의 실리콘 기반 전력시스템은 효율이 눈에 띄게 감소할 것이 자명하므로 전력시스템의 전력전송효율과 신뢰성의 중요성이 크게 대두되고 있다. 이 같은 사회적 요구로 볼 때 현재의 실리콘 전력소자의 기술적 한계를 뛰어넘는 고효율의 차세대 전력반도체 소자의 개발이 시급히 요구되며 SiC와 GaN와 같은 광대역 반도체가 차세대 전력반도체 소재로 유력해지고 있다. 또한 전력시스템에서는 시스템의 안전성과 회로의 간략화를 위하여 normally-off (증강형) 전력소자가 요구되기 때문에 normally-off (증강형) GaN 전력소자에 대한 개발이 필수적이다.

본 그룹에서는 gate-recess 공정을 이용하여 normally-off 동작을 실현하는 연구를 진행하였고, gate-recess 시 발생하는 식각 데미지를 줄이고 우수한 성능의 게이트 절연막을 개발하여 GaN 전력 반도체

소자의 전기적 특성 및 신뢰성을 개선하는 연구를 진행하였다. 식각 연구에서는 최종적으로 셀프 DC 바이어스가 낮은 O_2, BCl_3 플라즈마를 이용한 atomic layer etching을 개발하였고, 이를 통해 거칠기가 작고 표면 N vacancy가 적은 고품질의 (Al)GaN 표면을 얻을 수 있었다. 박막 연구에서는 Oxide 박막 증착 시, (Al)GaN 표면에 생성되어 계면 특성을 악화시키는 Ga_2O_3 생성을 막기위해 ALD AlN layer를 개발 및 적용하여 박막/(Al)GaN 계면 특성을 향상시켰다. 이로 인해 소자의 동작전류 증가 및 D_{it} 감소 결과를 얻을 수 있었고 스트레스에 따른 문턱전압 이동 특성의 감소로 소자의 신뢰성 또한 개선시킬 수 있었다. 이는 타 기관의 결과와 비교해도 뒤떨어지지 않는 우수한 특성을 보여주었다.

결론적으로 본 연구의 작은 플라즈마 데미지를 갖는 식각공정과 고품질 절연막 개발을 통해 우수한 특성의 GaN 전력소자를 구현할 수 있었고 향후 차세대 전력소자에 적용을 위한 가능성을 확보하였다.

주요어: 갈륨나이트라이드, 금속 절연막 반도체 구조, 신뢰성, 알루미늄나이트라이드, 원자층식각, 알루미늄하프늄옥시나이트라이드

Research Achievements

Journals

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감사의 글

기대와 설렘을 가지고 대학원에 입학한 지가 엊그제 같은데 어느덧 박사학위 논문의 마지막 페이지에 감사의 글을 쓰고 있다니 참 감회가 새롭습니다. 6년 반 동안 힘든 일도 많았지만 곁에서 힘이 되어 주시고 도움을 주신 많은 분들이 계셨기에 무사히 논문을 마칠 수 있었다고 생각합니다. 미흡하지만 도움 주신 모든 분들께 감사의 말씀을 전하고 싶습니다.

먼저 부족한 저를 제자로 받아 주시고 열정적으로 지도해 주신 서광석 교수님께 감사의 말씀을 드리고 싶습니다. 학생들을 위해 휴일에도 출근하시고 밤 늦게까지 학교에 남아 열정적으로 지도해 주셔서 감사합니다. 교수님을 본받아 더 발전하는 사람이 될 수 있도록 노력하겠습니다. 그리고 미팅 때마다 올바른 연구의 길을 걸어갈 수 있도록 조언해 주시고 도움을 주신 차호영 교수님께 감사드리고 더 좋은 논문을 완성할 수 있도록 지도해주신 이종호 교수님, 박병국 교수님, 황철성 교수님께도 감사의 말씀을 드리고 싶습니다.

또한 많은 연구실 선후배 분들의 도움이 있었기에 무사히 졸업을 할 수 있었습니다. 처음 대학원에 입학했

을 때 연구실 방장이셨고 제가 연구실 생활에 빨리 적응할 수 있도록 배려해 주시고 연구적으로도 많은 조언해 주신 민성이형, 항상 열정적으로 연구하시는 모습으로부터 많은 것들을 배울 수 있었던 재길이형, 저의 첫 연구실 사수시고 공정에서 모르는 게 없으셔서 연구적으로 많은 도움을 주셨던 동환이형, 모르는 것이 있으면 항상 친절하게 조언해 주시고 도움을 주신 상우형, 항상 옆자리에서 아낌없이 조언을 해주고 동생이지만 배울 점이 많았던 수근이, 박막연구 관련해서 많은 도움을 주고 연구실 사람들을 잘 챙겨줬던 명진이, 중간에 연구주제가 바뀌어 힘들지만 묵묵히 연구해 나가는 라성이, 어려운 주제로 연구하느라 고생이 많은 민우, 어려운 장비 맡아 고생이 많았던 준석이, 박막연구에서 큰 도움을 줬던 광호, 열정이 넘치고 연구하느라 밤을 많이 샜던 승현이, 항상 친절하고 연구실 막내생활이 길어 고생이 많았던 철희 그리고 다른 연구실이지만 연구에 집중할 수 있도록 많은 도움을 주고 같이 생활했던 현섭이, 원호, 김정진 연구교수님, 동민이, 준행이, 태현이, 준혁이, 찬희 모두 감사드립니다.

그리고 대학원 생활을 잘 해 나갈 수 있도록 지원해 주시고 응원해 주신 아버지, 어머니 감사합니다. 자랑스

러운 아들이 되도록 노력하겠습니다. 그리고 생활이 부족하지 않도록 많은 지원을 해주고 따뜻한 격려를 해줬던 큰 누나, 작은 누나, 고민이 있을 때마다 진심 어린 조언을 해 주셨던 큰 매형, 작은 매형 모두 감사드립니다.