Ph.D. DISSERTATION

Investigation of Bipolar Resistive Switching Characteristics with Silicon Nitride device and bi-layer application by introducing the Al_2O_3 barrier layer

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Abstract

The resistance switching random access memory (ReRAM), which changes the resistance state of the device by the external electrical stimulation, is one of the promising candidates for a next-generation nonvolatile memory. Due to its simple metal-insulator-metal (MIM) structure, low power consumption, scalability, and complementary metal-oxide-semiconductor compatibility, ReRAM has been attracted enormous attention as a highly integrated memory to replace NAND flash memory. The transition metal oxides, such as NiO, TiO_2, HfO_2, and Ta_2O_5, were the main focus on the ReRAM device fabrication and mechanism analysis. On the other hand, the insulating nitride films, such as silicon nitride (Si_3N_4), have no reason for not being regarded as the feasible ReRAM material. In fact, the Si:N ratio of Si_3N_4 can be readily controlled to induce defects inside the film, which is already in massive use for charge-trap layer in NAND flash memory. The defect generation and possible percolation of the defects to form the so-called “conducting filament (CF)” is the main mechanism for the fluent ReRAM performance. Therefore, N-deficient Si_3N_4, i.e., Si_3N_{4-x}, can be a feasible resistance switching (RS) material.

In the first part of this study, a bipolar resistive switching (BRS) property of a Si_3N_{4-x} thin film depending N-deficiency was investigated with Pt/Si_3N_{4-x}/TiN devices with various NH_3 gas flow rate during plasma enhanced chemical vapor deposition process of Si_3N_{4-x} thin film. By X-ray photo-electron spectroscopy analysis, it was confirmed that the fraction of nitrogen element in Si_3N_{4-x} thin film decreased as NH_3 gas flow rate decreased and the degree of N-deficiency could be controlled by changing NH_3 gas flow rate. The change of N-deficiency affected the current-voltage (I-V) characteristics of Si_3N_{4-x} thin film, and the behavior of BRS and the optimized condition could be achieved. In addition, the series line resistance of Pt/TiN electrode was attributed to the self-compliance behavior, having a stable BRS behavior even without compliance current. The Si_3N_{4-x} devices didn't show cell area dependency of I-V characteristics, implying the formation and rupture of CF involved in the RS behavior. To further investigation of RS mechanism, the temperature dependent I-V behavior was examined. With a double logarithmic plot of the I-V curves, the slope of the best-linear-fitted data in the low and high voltage regions was ~1 and ~2, respectively, which coincide with the Child's law and space charge

limited conduction mechanism dominated the conduction of Si_3N_{4-x} device. In addition, the activation energy and hopping distance for hopping conduction were calculated and both values decreased as NH_3 gas flow rate decreased and after switching occured. From these results, CF is formed by the local repelling N to TiN BE and the percolation of the traps. The trap condition of the initial Si_3N_{4-x} played an important role in the formation of CF, otherwise the device underwent a hard breakdown.

On the basis of the BRS property of a Si_3N_{4-x} thin film in the first part of this study, Al_2O_3 interfacial barrier layer (IBL) was inserted between the Si_3N_{4-x} thin film with optimized deposition condition ($Si_3N_{3.0}$) and Pt top electrode, forming the $Pt/Al_2O_3/Si_3N_{3.0}/Ti$ devices with various Al_2O_3 film thickness (3-5 nm). The seperation between Al_2O_3 and $Si_3N_{3.0}$ layer could be identified with TEM image and EDS mapping image. While the $Pt/Si_3N_{3.0}/Ti$ device showed filamentary BRS, the $Pt/Al_2O_3/Si_3N_{3.0}/Ti$ devices showed electronic BRS with forming free property. In addition, the devices had self-rectifying and nonlinearity characteristics, which is necessary to prevent sneak current for big crossbar-array structure, due to the high band gap of Al_2O_3 IBL. The devices showed

area dependency at HRS and LRS, indicating the interfacial electronic BRS dominated the RS mechanism. The temperature dependency analysis revealed the trap depth of trap sites in $Si_3N_{3.0}$ layer and schottky barreir height between Pt and Al_2O_3. Thus, the device switched its resistance state by trapping/detrapping of electrons at the trap sites in $Si_3N_{3.0}$ RS layer. To estimate the available maximum crossbar-array size (CBA), HSPICE simulation was performed and it was confirmed that ~10^6 density could be obtained.

To form crossbar-array structure with ReRAM, sneak current is main issue for proper operation of selected cell. To suppress the sneak current, using transistor is a solution. However, relatively large size of transistor device hinders the scaling-down of ReRAM device. In this respect, selector device ,which has simple MIM sutucture, could replace a transistor while suppressing sneak current sufficiently. Therefore, it is needed to investigate the issue of integrated device with 1 selector and 1 RS material (1S1R). In the third part of this study, 1S1R device was fabricated with the Pt/Si_3N_{4-x}/TiN RS layer in the first part of this study and Pt/TiO_2/TiN selector layer using the atomic-layer deposited TiO_2 film. The device was fabricated via lift-off process with

single cell, 2 by 2 and 9 by 9 crossbar-array pattern. By comparing each device, optimized deposition condition of selector and RS layer could be founded and additional issue to overcome was identified.

Keywords : resistive switching, Silicon nitride, self compliance, Nonvolatile memory, plasma enhanced chemical vapor deposition

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List of Abbreviations

AC	Alternating Current
AES	Auger Electron Spectroscopy
ALD	Atomic Layer deposition
BE	Bottom Electrode
BRS	Bipolar Resistive Switching
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical Vapor Deposition
DRAM	Dynamic Random Access Memory
DC	Direct Current
E_a	Activation Energy
e-BRS	Electronic Bipolar Resistive Switching
EDS	Energy Dispersive Spectroscopy
E_g	Bandgap
FIB	Focused Ion Beam
HRS	High Resistance State
HRTEM	High Resolution Transmission Electron Microscopy
IBL	Interfacial Barrier Layer
I_{cc}	Compliance Current
I-V	Current-Voltage
LRS	Low Resistance State
MEMS	Micro Electro Mechanical System
MIM	Metal-Insulator-Metal
NAND	Not And

PECVD	Plasma Enhanced Chemical Vapor Deposition
RAM	Random Access Memory
ReRAM	Resistive Random Access Mermory
RF	Radio Frequency
RS	Resistive Switching
TCM	Thermal Change Mechanism
TE	Top Electrode
URS	Unipolar Resistive Switching
VCM	Valence Change Mechanism
XPS	X-ray Photoelectron Spectroscopy
ε_r	Dielectric constant

1. Introduction

1.1. Resistive switching Random Access Memory

Resistive switching random access memory (ReRAM) switches its resistive state to low resistance state (LRS) and high resistance state (HRS) by the external electrical stimulation. ReRAM is a one of the most promising next-generation non-volatile memory devices due to simple metal-insulator-metal (MIM) structure, scalability, low power consumption, sub-ns operation speed and complementary metal-oxide-semiconductor (CMOS) compatibility.[1–5] These attributions make ReRAM an attractive substitute for NAND flash memory.

ReRAM operation occurs either in ther manner of unipolar or bipolar resistive switching (URS or BRS). In Figure 1.1 (a), URS is the resistive switching whose set (switching from HRS to LRS) and reset (switching from LRS to HRS) occurs irrespective of the polarity of the applied bias, which is also reffered as nonpolar switching. On the other hand, BRS is the resistive switching set and reset only occurs in the opposite polarity of the applied voltage in Figure 1.1 (b).[6]

Figure 1.2 shows many mechanisms for resistive switching (RS) which categorized to phase change mechanism (PCM), thermo-chemical mechanism (TCM), valence change mechanism (VCM), electrochemical metallization

(ECM), and electronic mechanism.[6] In VCM., the movement of ionic species occurs by applied external electrical bias, causing the formation or rupture of conduction filaments (CFs). On the other hand, the electronic mechanism is usually attributed to the trapping/detrapping of electrons according to the bias polarities at trap sites in the switching layer.[6–8]

The transition metal oxides (TMO), such as NiO, TiO_2, HfO_2, and Ta_2O_5, were widely reserched for ReRAM and the switching mechansim of TMO was mostly revealed. Besides TMO, the insulating nitride films, such as silicon nitride (Si_3N_4), is also widely used in the industry, and the research of Si_3N_4 for floating gate in NAND flash memory has already been conducted. There are serveral reports on the Si_3N_4 based ReRAM with low power consumption, good endurance, and retention. However, the detalied switching mechanism is not very clear, although the N-deficient CFs must be involved. Also, the influence of N-deficiency has not been systematically examined, although it must bear a critical influence on the ReRAM performance.

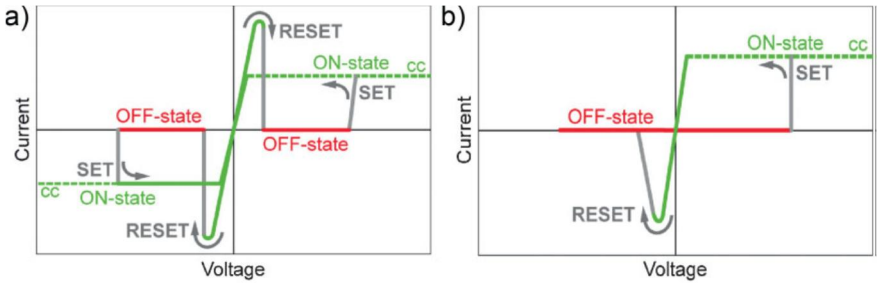

Figure 1. 1 ReRAM operation modes. (a) unipolar resistive switching (URS) and (b) bipolar resistive switching (BRS). Adapted from [6]

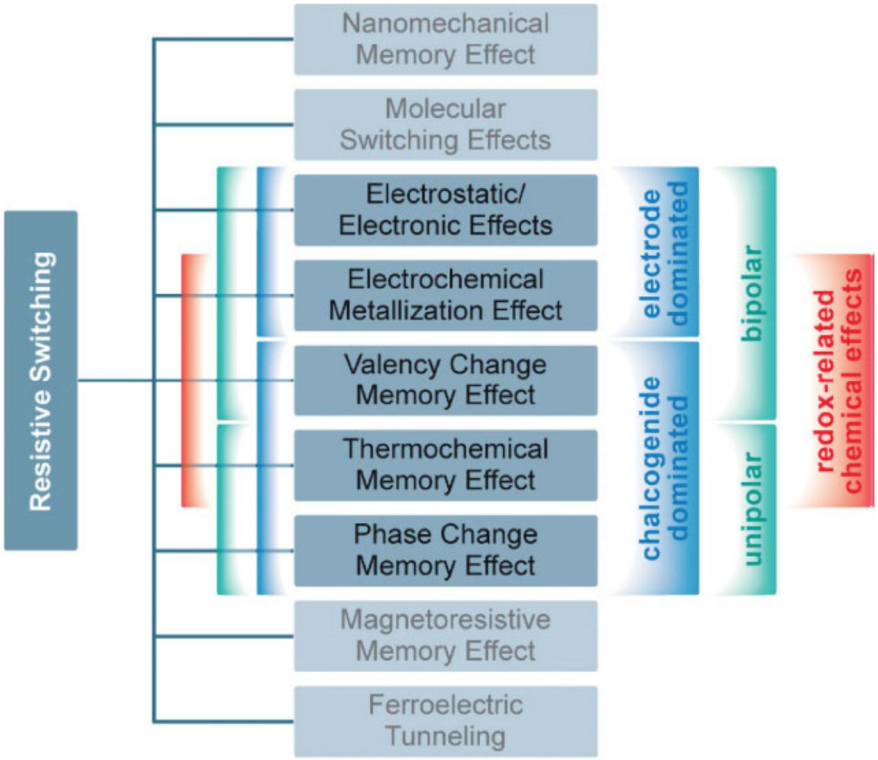

Figure 1. 2 Classification of the resistive switching. Adapted from [6]

1.2. Research scope and objective

The objective of the present thesis is to study the switching behavior of N-deficient Si_3N_4 (Si_3N_{4-x}) thin film with various device design.

Chapter 2 present the bipolar resistive switching of a Si_3N_{4-x} thin film depending N-deficiency was investigated with Pt/Si_3N_{4-x}/TiN devices. By varying the NH_3 gas flow rate during plasma enhanced chemical vapor deposition process of Si_3N_{4-x} thin film, the degree of N-deficiency could be controlled. The change of N-deficiency was checked by X-ray photo-electron spectroscopy analysis and it was confirmed that the fraction of nitrogen element in Si_3N_{4-x} thin film decreased as NH_3 gas flow rate decreased. Comparing the I-V characteristics of Si_3N_{4-x} devices with various NH_3 gas flow rate, the optimized condition could be achieved. In addition, the series line resistance of Pt/TiN electrode were attributed to the self-compliance behavior, having a stable BRS behavior even without compliance current. Through cell area and temperature dependency of I-V characteristics, the formation and rupture of CF involved to the RS behavior and different condition of trap sites in Si_3N_{4-x} with various NH_3 gas flow rate was identified.

Chapter 3 suggests the effects of Al_2O_3 interfacial barrier layer (IBL) between the Si_3N_{4-x} thin film with optimized deposition condition ($Si_3N_{3.0}$) and Pt top electrode, forming the Pt/Al_2O_3/$Si_3N_{3.0}$/Ti devices with various Al_2O_3 film thickness (3-5 nm). The TEM image and EDS mapping image revealed the

seperation between Al_2O_3 and $Si_3N_{3.0}$ layer. While the Pt/$Si_3N_{3.0}$/Ti device showed filamentary BRS, the Pt/Al_2O_3/$Si_3N_{3.0}$/Ti devices showed electronic BRS with forming free property. In addition, the devices had self-rectifying and nonlinearity characteristics, which is necessary to prevent sneak current for crossbar-array structure, due to the high band gap of Al_2O_3 IBL. By cell area and temperature dependency of I-V characteristics, it can be identified that the device switched its resistance state by trapping/detrapping of electrons at the trap sites in $Si_3N_{3.0}$ RS layer. To estimate the available maximum crossbar-array size (CBA), HSPICE simulation was performed and it was confirmed that ~10^6 density could be obtained.

Chapter 4 covers 1S1R device fabricated with the Pt/Si_3N_{4-x}/TiN RS layer in the first part of this study and Pt/TiO_2/TiN selector layer using the atomic-layer deposited TiO_2 film. The device was fabricated via lift-off process with single cell, 2 by 2 and 9 by 9 crossbar-array pattern. By comparing each device, optimized deposition condition of selector and RS layer could be founded and additional issue to overcome was identified.

Finally, in chapter 5, the conclusion of the thesis is made.

2. Bipolar resistive switching property of Si_3N_{4-x} thin film depending on N-deficiency

2.1. Introduction

Resistive switching random access memory (ReRAM), regarded as a next-generation nonvolatile memory, has the potential to replace a conventional charge-based nonvolatile memory due to its simple metal-insulator-metal (MIM) structure, low power consumption, scalability and complementary metal-oxide-semiconductor (CMOS) compatibility.[9–11] Transition metal oxides, such as NiO, TiO_2, HfO_2, and Ta_2O_5, have been mainly focused on ReRAM research and device fabrication.[12–14] On the other hand, insulating nitride films, such as silicon nitride (Si_3N_4), have no reason for not being regarded as the feasible ReRAM material.[15] In fact, the Si:N ratio of Si_3N_4 can be readily controlled to induce defects inside the film, which is already in massive use for charge-trap layer in NAND flash memory. As the defect generation and possible percolation of them to form the so-called "conducting filament (CF)" is the main mechanism for the fluent ReRAM performance, N-deficient Si_3N_4, i.e., Si_3N_{4-x}, can be a feasible resistance switching (RS) material. In this regard, the recent reports by the group of Prof. Chen are eye-catching.[16] They dispersed metallic elements in various disordered oxides, including the

Si_3N_{4-x}, in which the defective sites in the disordered insulators work as the charge trapping/detapping centers depending on the bias polarity. They called this mechanism as the nanometallic memory, which may avoid the reliability concerns about the ionic-defect mediated mechanism.[16] Their assertion on the fundamental reasons why such disordered insulators could play the role as the stable charge trapping center is based on the argument of negative-U center theory. The recent theoretical work by Kang et al.,[17] however, revealed that the seemingly negative U is not the real negative U but due to the almost continuous distribution of energy levels of the traps within the band gap of the Si_3N_{4-x}. Therefore, the fundamental mechanism of the nanometallic memory is under question.

There are several other reports on the Si_3N_4-based ReRAMs, which have shown several advantages, such as low power consumption, good endurance, and retention.[18–21] However, the detailed switching mechanism is not very clear yet, although there must be an involvement of N-deficient CF. Also, the influence of N-deficiency, i.e., x-value, has not been systematically examined yet, although it must bear a critical influence on the ReRAM performance.

One of the critical merits of the Si_3N_{4-x} compared with other defective oxides as the RS layer is its easier control of defect concentration by changing the process condition of the film growth, such as the NH_3 gas flow rate during the Si_3N_{4-x} plasma enhanced chemical vapor deposition (PECVD) process.[22]

There have been similar approaches for the above-mentioned oxide-based RS

materials, i.e., changing the oxidation environment during the oxide film growth to vary the oxygen stoichiometry, but it becomes difficult due to much higher affinity between the transition metals and oxygen than that between the silicon and nitrogen. Therefore, Si_3N_4 could be a viable material as an RS layer if the nitrogen stoichiometry could be changed readily. In this paper, therefore, various Si_3N_{4-x} films with the different degree of N-deficiency was grown by a PECVD using SiH_4 and NH_3 gas as the Si-precursor and N-source, respectively. By controlling the NH_3 gas flow rate, the N-deficiency was controlled, of which detailed states were examined by various analysis techniques. As expected, the RS performance, as well as the pristine state resistance, was critically dependent on the nitrogen concentration of the as-deposited film. The RS performances were analyzed and the best experimental conditions to achieve the optimal device performance were examined.

2.2. Experimental

The 4-nm-thick Si_3N_{4-x} thin films were deposited by PECVD using 800 standard cubic centimeters per minute (sccm) 5%SiH_4/N_2 gas and 1000 sccm N_2 gas with different flow rates of NH_3 gas ranging from 1 to 6 sccm. The applied plasma was with 187 kHz frequency and 60 W RF power. The substrate was 50-nm-thick TiN/Si, where the TiN film was grown by a reactive sputtering technique using a commercial sputtering tool (Applied Materials, Endura. Resistivity ~190 μohm cm). The cross-sectional image of the device was examined via transmission electron microscope (TEM, Tecnai F20). The film compositions of the 10-nm-thick Si_3N_{4-x} films with the various NH_3 gas flow rates were examined by Auger electron spectroscopy (AES, Perkin-Elmer, PHI) and X-ray photo-electron spectroscopy (XPS, Thermo VG, SIGMAPROBE, using monochromatic Al-Kα radiation) analysis. The Pt top electrode (TE), which was deposited by an electron-beam evaporation method, and TiN bottom electrode (BE) were patterned in a crossbar structure by ultra-violet photo-lithography followed by a lift-off process. The electrical property was measured using a semiconductor parameter analyzer (Hewlett Packard, 4145B) at room temperature in the voltage sweep mode. Also, a temperature-dependent test was carried out to analyze the electrical conduction mechanism and retention performance. All the biases were applied on the TE, while the BE was grounded.

2.3. Results and Discussions

The cross-section of Pt/Si_3N_{4-x}/TiN was examined via TEM, as shown in Figure 2.1 (a). The 4-nm-thick Si_3N_{4-x} layer remained an amorphous state, and form uniform interfaces with the TiN BE. AES depth profiling technique was used to confirm the depth concentration profile of each element in the Si_3N_{4-x}/TiN films. Figure 2.1 (b) shows a typical depth concentration profile (4 sccm of NH_3 flow rate) indicating the uniform Si and N concentration with low carbon and oxygen impurity concentrations.

Figure 2.2 (a) and (b) show Si 2p and N 1s XPS spectra, respectively, of the Si_3N_{4-x} thin film with various NH_3 flow rates from 1 to 5 sccm. Binding energies were referenced to the C1s peak at 284.6 eV derived from the ubiquitous adventitious carbon. The binding energies of Si 2p and N 1s peaks are 102.1 eV and 398.0 eV for the stoichiometric Si_3N_4.[23,24] For the Si 2p peak in Figure 2.2 (a), the mean binding energy was ~101.5 eV, which was slightly lower than the binding energy of Si_3N_4, suggesting the involvement of not fully nitrided Si atoms.[25] The Si 2p peaks were deconvoluted with four peaks locating at 103.5 eV (SiO_2),[26] 102.1 eV (Si_3N_4), 101.3 eV ($SiN_{0.73}$), and 99.8 eV ($SiN_{0.45}$) to analyze the chemical state of the Si atoms in the films with the various NH_3 flow rate, and the area portions of each peak are shown in Figure 2.2 (c) as a function of the NH_3 gas flow rate. The increase of NH_3 flow rate decreases the area portion of the peak with the binding energy of 101.3 eV, implying that the

Si_3N_{4-x} thin film becomes more N-deficient as the NH_3 flow rate decreases. The peak with the binding energy of 103.5 eV, coinciding with the stoichiometric SiO_2, was also appeared. However, this is not an important factor since the area portion of the peak is less than 0.1, and they showed almost no change with the varying NH_3 flow rate. Similarly, the N 1s peaks were deconvoluted with the two peaks having the binding energies of 398.0 eV (Si_3N_4) and 397.1 eV ($SiN_{0.73}$), and the area portions of each peak are shown in Figure 2.2 (d) as a function of NH_3 gas flow rate, indicating that the area portion of peak with the binding energy of 398.0 eV (397.1 eV) increases (decreases) as NH_3 flow rate increases. The mole fractions of Si, N, O were calculated using the peak areas of the Si 2p, N 1s, and O 1s, of which mean binding energy was ~532.0 eV (data not shown). The results are presented in Figure 2.2 (e) as a function of the NH_3 flow rate and summarized in a Table 1. While the N (Si) mole fraction increased (decreased) from 51.5 % (31.9 %) to 53.8 % (30.1 %) with the increasing NH_3 gas flow rate from 1 to 6 sccm, O mole fraction remained fairly constant with low values (< 17 %). The oxygen atoms must be incorporated into the surface of the film by the air exposure during the transfer from the PECVD chamber to the XPS analysis tool. Also, the surface of the TiN BE must have been partly oxidized, as shown from the AES-depth profile results in Figure 2.1 (b). This implies that the O may have little influence on the variation of the RS behavior, which could be related to the different NH_3 flow rates. Figure 2.2 (c)–(e) and Table 2.1, in contrast, clearly indicate that the film

became less stoichiometric, or N-deficient, as the NH_3 flow rate decreased, suggesting that the film properties might be largely controlled by this parameter. This was indeed the case as shown in Figure 2.3.

The pristine devices with different electrode areas (16, 36, 64, 100 μm^2, i.e., line width of 4, 6, 8, and 10 μm, respectively, in crossbar type devices) were examined by the current-voltage (I-V) curves and the current level at ± 1.5 V were plotted as a function of the NH_3 flow rate (from 1 to 6 sccm) as shown in Figure 2.3 (a) and (b), respectively. Every data point contains the distribution of different cells (at least ten cells per each data point), and the narrow distribution of the data indicates good uniformity of the devices. Also, the pristine current level is inversely proportional to the NH_3 gas flow rate. It is notable that the current varied by almost four orders of magnitude by varying the NH_3 gas flow rate by 6 times, demonstrating the critical influence of the minute change of the N-concentration on the insulating property of the films. The following discussion analyzes the influence of the NH_3 flow rate on the RS behavior.

Figure 2.4 (a)–(d) show the electroforming (EF) and subsequent RS behaviors via the I-V sweep of the 1~5 sccm devices with an electrode area of 100 μm^2. All the devices showed set switching (switching from high resistance state (HRS) to low resistance state (LRS)) in the negative bias region and reset switching (switching from the LRS to HRS) in the positive bias region, after the EF in the negative bias region. When the EF was attempted in the positive

bias region, almost all the devices were either hard-broken down or did not show fluent RS during the subsequent I-V sweeps. It could be reasonable to assume that N atoms are migrated rather fluently between the TiN BE and Si_3N_{4-x} layer upon the negative (migration from the Si_3N_{4-x} layer to TiN BE) and positive (reversed migration) bias applications, while it between Pt TE and Si_3N_{4-x} layer would be unfavorable. This hypothesis can explain the bias-polarity dependent EF and subsequent RS properties shown in Figure 2.4.

As shown in Figure 2.3, the pristine film had a higher insulating property as the NH_3 gas flow rate increased, which must increased the EF voltage too. This was indeed the case as shown in Figure 2.4 (a)–(d), (blue dash line), and the EF voltages are summarized in Figure 2.4 (e). Even though all the devices showed the EF performance in the negative bias region, the subsequent RS performance was critically dependent on the NH_3 gas flow rate.

Without the compliance current (I_{cc}) application, 1 and 2 sccm devices in Figure 2.4 (a) and (b) experienced an initial reset at a voltage less than 4 V and showed a feasible bipolar resistance switching (BRS) behavior with -2~-3 V set voltage. However, other devices with higher NH_3 gas flow rates experienced hard breakdown (data not shown).

The subsequent set voltages (~-2 V) in the 1 and 2 sccm devices were less than their EF voltages, implying that a weak filament was formed after the EF process. Also, the 1 and 2 sccm devices exhibited a self-compliance behavior, having a stable BRS behavior even without settling the I_{cc}. The self-compliance

behavior can be explained with the concept of series resistance.[27] The device is composed of series resistance and RS layer, and its resistance can be expressed by equation (1)

$$R_{tot} = R_r + R_S \cdots (1)$$

, where R_{tot} is the total resistance, R_s is the series resistance, and R_r is the resistance of the switching layer. The switching layer changes its resistance to either LRS or HRS, while the R_s has a fixed value. Even if the switching layer becomes LRS through the set process, the R_{tot} cannnot fall below the R_s. As a result, the device can be protected from hard breakdown which also results in the self-compliance operation. It was confirmed that all devices had different pristine current values, as shown in Figure 2.3 (a) and (b), but after the forming process without settling the I_{cc}, their currents converged to a certain level. This means that the presence of the R_s is not related to the deposition condition, but to the finite resistance of the TE and BE. The I-V curve of a Pt/TiN the film without the Si_3N_4 layer was measured, as shown in Figure 2.4 (f), and they showed almost identical I-V curves of the LRS of all devices. This concludes that the finite resistance of the TE and BE which could be the origin of the R_s and the self-compliance behavior.

To further examine the possibility of the RS from the films with higher NH_3 gas flow rates, the appropriate value of I_{cc} (0.1mA) was settled as shown in Figure 2.4 (c) for the 3 sccm device, and it showed reasonable BRS performance. Despite the implementation of the I_{cc}, however, the 4 and 5 sccm

devices in Figure 2.4 (d) did not show any reasonable RS performance but only hard breakdown. Figure 2.4 (d) showed the I-V curves when the I_{cc} was decreased to 0.01 mA during the sweep into the negative voltage region. The subsequent I-V curve in the positive bias region showed the curve similar to Figure 2.4 (f), with no reset, suggesting that the highly insulating Si_3N_4 film was hard broken down even with such a small I_{cc} value. When no I_{cc} was applied (inset figure), the film was also broken down and showed no subsequent reset and set behavior but only I-V curve of the TE/BE. Therefore, such highly insulating pristine films could not be used for the RS application.

Next, the RS mechanism was scrutinized by examining the electrode area-dependent current and the electrical conduction mechanism analysis. Figure 2.5 (a) shows the variations in the logarithm of current levels measured at 1.5 V of the pristine devices for 1~5 sccm devices as a function of logarithm of the electrode area. The data were best-linear-fitted, and the slope values from 0.96 to 1.48 were obtained. The 1 and 2 sccm films showed the slope of almost 1, suggesting that the leakage current flow uniformly across the entire electrode area. The 3~5 sccm films, however, showed slope values obviously higher than 1, suggesting that the leakage current of these more insulating films was more prone to the involvement of the local defects; the larger area the higher chance of involving more leaky spots.

After the switching, cell area dependency disappeared for both the LRS and HRS as shown in Figure 2.5 (b). These behaviors are related to the filamentary

resistance switching as CF are formed to a constant dimension regardless of the cell area. As shortly discussed above these CFs are believed to be composed of highly N-deficient Si_3N_{4-x} or even Si-clusters.

The nature of the CF could be usually identified by estimating the temperature dependent I-V behaviors of the LRS. If it is of the metallic nature, the temperature coefficient of resistance is positive, usually coinciding with the nano-wire value of the corresponding metal.[28] If it is semiconducting nature, the temperature coefficient of resistance is negative, and generally show hopping conduction behavior suggesting the heavily-doped property of the CF.[29] Unfortunately, the resistance of the LRS in this work was dominated by the R_s of the TE and BE, making such an approach impractical. Therefore, only HRS could be examined, and the nature of the CF must be indirectly deduced from the results. Figure 2.5 (c) shows the variation in the I-V curve of the 2 sccm device in HRS with the varying temperature from 30 to 120 ℃. With a double logarithmic plot of the I-V curves, the current increased with the increasing temperature at the low voltage region whereas the current converged to a certain level at the high voltage region. The slopes of the best-linear-fitted data in the low and high voltage regions were ~1.02 and 2.16, respectively, which coincide with the Child's law, which is a characteristic feature of the space charge limited conduction (SCLC) mechanism.[18–21,30] In such SCLC case, the current flow in the low voltage region is mediated by the hopping conduction mechanism with generally small activation energy (E_a) values (~

0.1 eV). To examine the possible relationship between the pristine Si_3N_{4-x} film and HRS, the temperature dependent I-V curves of the 1-5 sccm devices were also measured. It was identified that all the pristine devices showed a conduction mechanism dominated by the SCLC behavior too. All the devices area was 100 μm^2. Figure 2.5 (d) and (e) show the hopping conduction plots of the 2 sccm device at the pristine and HRS, respectively.

According to the hopping conduction, the current density follows equation (2),[29]

$$J = qNav_0 e^{-q\varphi/kT} e^{qaV/2dkT} \cdots (2)$$

, where $\mathrm{N}, \mathrm{a}, \varphi, v_0$ and d are the density of space charge, the mean of hopping distance, the barrier height of hopping, the intrinsic vibration frequency, and the film thickness, respectively. From the plot in the form of Ln(I) vs. 1/T in the insets of Figure 2.5 (d) and (e), the data fitted well with hopping conduction. From equation (2), E_a can be calculated by equation (3)

$$E_a = E_c - E_F - qV\frac{\Delta z}{2u_a} = -\frac{dlnI}{d\frac{1}{T}} \times k \cdots (3)$$

, where V is the applied voltage, Δz is the average hopping distance, u_a is the thickness of the switching layer, k is the Boltzmann's constant, and T is the absolute temperature. In Figure 2.5 (d) and (e), the E_a values were calculated to be ~0.13 and 0.097 eV, respectively. Also, the Δz can be calculated by equation (4)

$$\frac{dE_a}{dV} = -V\frac{q\Delta z}{2u_a} \cdots (4)$$

From the $\frac{dE_a}{dV}$ value obtained from Figure 2.5 (d) and (e), the Δz was obtained. The calculated E_a and the Δz for all the devices in pristine (for 1-5 sccm) and HRS (for 1-3 sccm, since the 4 and 5 sccm could not be reversibly switched) are shown in Figure 2.6 (a) and (b), respectively. The black squares represent the pristine state at different NH_3 flow rates, indicating that the E_a and the Δz decrease as the NH_3 flow rate decreases. This tendency clarifies the relationship between the deposition condition and the trap density in the Si_3N_{4-x} thin film. The increase of defective phase as the NH_3 flow rate decreases in Figure 2.2 (c) and (d) allows Si_3N_{4-x} thin film to have more Si dangling bond, which acts as a trap site. The increase of the trap site makes electrons move more easily in the Si_3N_{4-x} thin film and causes an increase of pristine current level shown in Figure 2.3 (a) and (b). In addition, the red square in Figure 2.6 (a) and (b) represent the values of the HRS for the 1, 2 and 3 sccm devices after forming process and these values are smaller than the value of the pristine state for each device. Therefore, It can be assumed that the filament, which is more defective than pristine, was formed after the forming process, and HRS was formed through partial recovery of the defects within the CF during the reset. The E_a and Δz of HRS increase as NH_3 flow rate increases. Considering the formation of CF as percolation of the traps, the lack of traps in pristine makes percolation more difficult. Therefore, 4 and 5 sccm devices suffer hard breakdown before percolation of the traps ends during forming process.

From these results, it can be assumed that CF is formed by the local repelling

N to TiN BE and percolation of the traps (or Si atoms) (See Figure 2.6 (c)). With the help of R_s of the Pt/TiN, the permanent break down of the Si_3N_{4-x} film was prohibited in the 1 and 2 sccm devices. The reset operation of Si_3N_{4-x} layer could be induced by the (partial) recovery of N atoms from the TiN under the positive bias condition (See Figure 2.6 (c)). Due to the involvement of larger R_s than that of the LRS resistance of the CF, the set voltage became rather large, even though the Si_3N_{4-x} film was quite thin (4 nm).

Figure 2.7 (a) shows the retention performances of the 2 sccm device having 100 μm^2 cell area at different temperatures from 140 ℃ to 200 ℃ with the reading voltage of 1 V. At 200 ℃, the resistance of LRS maintains its initial value over 10^4 seconds, suggesting that the CF of LRS is strong enough not to be disturbed by the thermal energy of 200 ℃. The resistance value of the HRS, however, was relatively unstable and increased to a higher value at a certain time depending on the retention test temperature. Such variation in the HRS resistance might be understood from the detrapping of carriers within the residual CFs by the thermal energy. As discussed earlier, the electrical conduction of the HRS is mediated by the hopping mechanism within the SCLC. The hopping conduction mechanism corresponds to the tunneling of the trapped electronic carrier (electrons) between the trapping sites. Therefore, if the thermal energy detrapped the electrons from the defect centers, the electrical conduction must decrease. While such a trend, i.e., the increase in the HRS resistance, was better than the opposite trend, i.e., decrease in the LRS

resistance, it still can incur problems in the circuit operation.

To estimate the retention time at room temperature, the degeneration time at which the HRS resistance becomes doubled is plotted to the Arrhenius-type graph fashion in Figure 2.7 (a) inset. As a result, the estimated retention time for HRS at room temperature is over 10 years. The activation energy estimated from the slope of the best-linear-fitted graph was 0.89 eV.

Figure 2.7 (b) shows the endurance test results of the 2 sccm device with cell area of 100 μm^2 at room temperature under the DC I-V sweep condition, where the resistance values were measured at 1 V. The HRS almost continuously decreased with the increasing cycle number and suffered failure after ~500 cycles while the LRS remained stable. The HRS variation trend is opposite to the retention case, suggesting either that the recovery of the lost N atoms during the reset sweep was insufficient of that the trapping of electrons at the traps within the residual CFs increased. It was anticipated that the pulse-type AC switching may improve the endurance performance significantly, but the involvement of the relatively large R_s inhibited efficient application of the AC test protocol. This will be the topic of subsequent research.

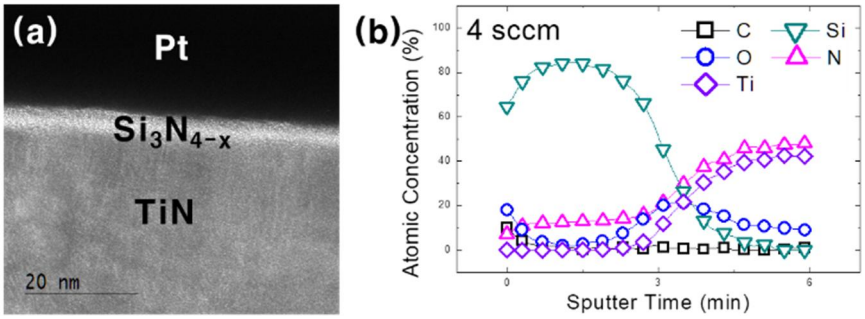

Figure 2. 1 (a) TEM image of Pt/Si_3N_{4-x} (4 nm)/TiN. (b) AES data of Si_3N_{4-x} (4 sccm) thin film.

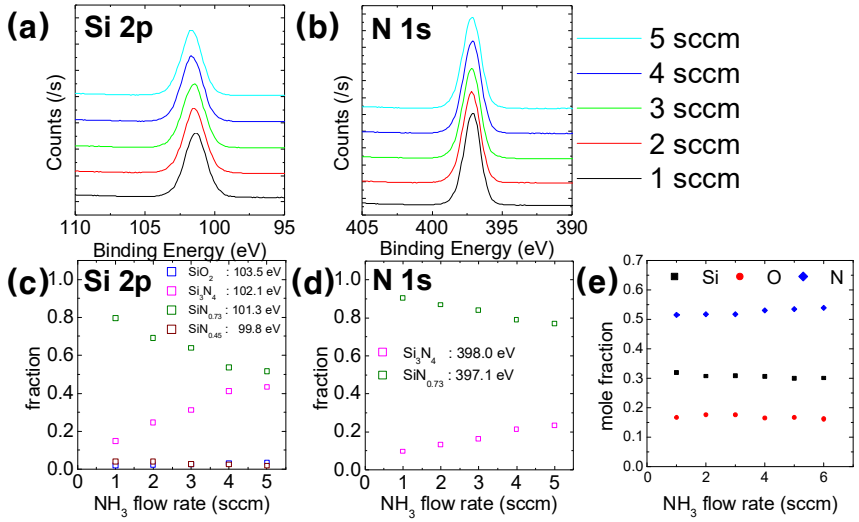

Figure 2. 2 XPS data extracted from the surface of the Si_3N_{4-x} thin film, including binding energy for (a) Si 2p and (b) N 1s. The intensity ratio of energy peaks of (c) Si 2p and (d) N 1s by deconvolution. (e) The mole fraction of Si, O, N extracted from XPS result.

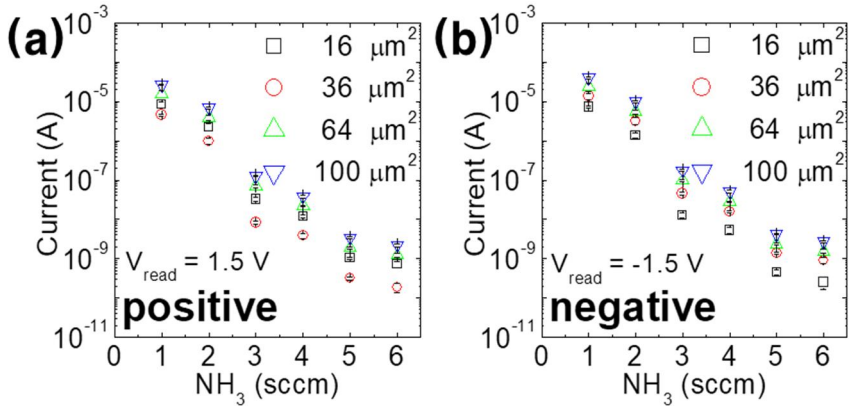

Figure 2. 3 Pristine current level at (a) positive 1.5 V & (b) negative -1.5 V.

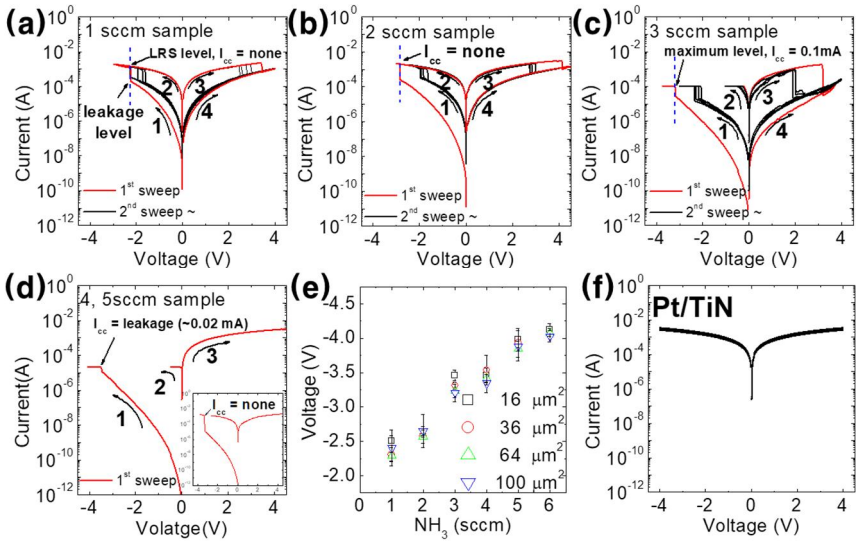

Figure 2. 4 Typical BRS characteristics of (a) 1 sccm, (b) 2 sccm without compliance current. (c) 3 sccm shows BRS with compliance current under 0.1 mA. (d) 4, 5 sccm doesn't show BRS with compliance current from leakage to none (inserted). (e) Forming voltage for different NH_3 flow rate. (f) I-V curve of Pt/TiN device without the Si_3N_{4-x} RS layer.

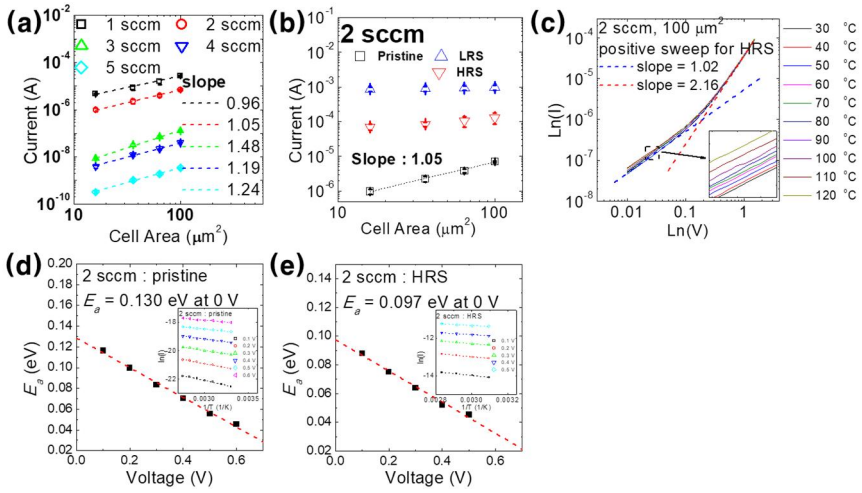

Figure 2. 5 (a) Area dependency of current at 1.5 V for pristine (1~5 sccm devices). (b) Area dependence of current at 1.5 V for pristine, HRS, LRS (2 sccm device). (c) SCLC fitting of the positive sweep for HRS (2 sccm device). E_a vs. Voltage are drawn for (d) pristine and (e) HRS of 2 sccm device. (Ln(I) vs. 1/T is inserted in each figure)

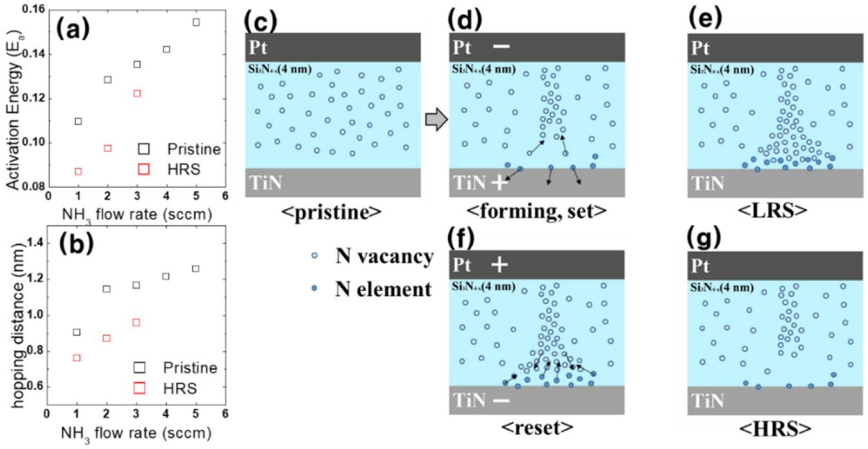

Figure 2. 6 (a) Calculated E_a and (b) hopping distance of hopping conduction vs. NH_3 flow rate for pristine and HRS. Schematic diagram of switching behavior of Si_3N_{4-x} device for (c) pristine, (d) set(forming), (e) LRS, (f) reset and (g) HRS.

NH_3 flow rate (sccm)	**1**	**2**	**3**	**~4**
BRS behavior	Yes (self-compliance)	Yes (self-compliance)	Yes (with proper I_{cc})	No (hard breakdown)

Table 2. 1 The RS behavior of each device.

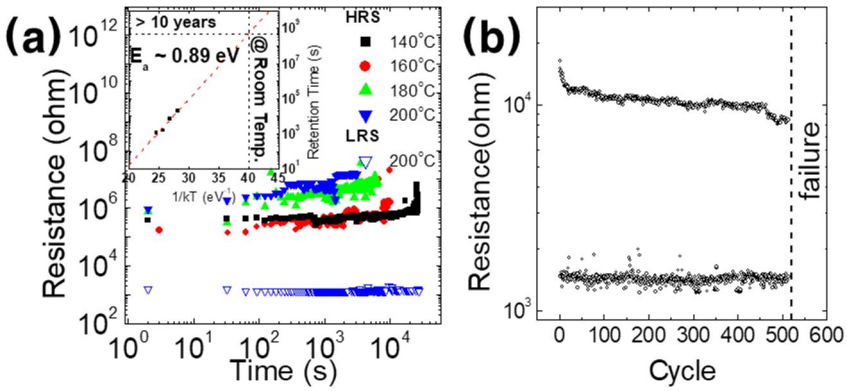

Figure 2. 7 (a) The retention of 2 sccm device. (b) The endurance of 2 sccm device with DC sweep, respectively.

2.4. Conclusion

In conclusion, the electrical property of bipolar resistive switching of Si_3N_{4-x} becomes tunable and be optimized by controlling the NH_3 gas flow rate during Si_3N_{4-x} thin film deposition process. Through XPS examination, the decrease of NH_3 gas flow rate induces Si_3N_{4-x} thin film to become more defective. The device with 2 sccm NH_3 gas flow rate shows the best performance and the self-compliance behavior due to the involvement of the line resistance of the Pt/TiN electrode. Also, the resistance switching is governed by recovery/rupture of the conducting filament which might be composed of heavily reduced Si ions (or their clusters). The electrical conduction mechanism analysis of the HRS revealed that the conduction was mediated by the electron hopping process in the low voltage region whereas the conduction in the high voltage region was dominated by the space charge limited conduction. The activation energy and hopping distance decrease with the decreasing NH_3 gas flow rate during the PECVD of the Si_3N_{4-x} thin film for both the pristine and HRS. The 2 sccm device shows excellent retention performance over 10 years at room temperature. It was found that the Si_3N_{4-x} could be a feasible contender to be used as a fluent resistance switching device only when the growth condition was appropriately controlled to make the pristine film relatively defective. If the pristine film was too insulating by depositing stoichiometric Si_3N_4, it was improbable to switch them into the feasible memory state by normal electrical stresses with the settled compliance current.

3. Area-type electronic bipolar resistive switching of $Pt/Al_2O_3/Si_3N_{3.0}/Ti$ with forming free, self-rectification, and nonlinearity characteristics

3.1. Introduction

Electronic bipolar resistive switching (e-BRS) is attracting a great deal of interest as a potential contender to solve various issues with resistive switching random access memory (ReRAM) based on ionic BRS (i-BRS).[8,9,12,20,31,32] The remaining issues in i-BRS include cell-to-cell and switching-to-switching variation, which is related to the electroforming (EF) step, and generally high power consumption, especially in multi-level programming using incremental-step-pulse-programming.[6,11] These problems are closely related to the formation and rupture of localized conducting filaments (CFs) in many transition-metal-oxide (TMO)-based ReRAM systems, where field-induced generation and percolation of ionic defects constitute the CFs.[9] While the localized CF mechanism may guarantee the scaling down of the device size to only a few nm, it also incurs those problems. In this regard, an area-type resistance switching (RS) mechanism could provide a feasible solution, especially when the e-BRS mechanism, which is mediated by carrier (electron) trap/detrap, is the working principle.[12,32,33] e-BRS has been

demonstrated in several TMO systems, where abundant oxygen vacancies (V_O's) mostly played the role of the carrier trapping centers. As might be expected, however, the high V_O concentration, which could be induced by either the film fabrication process or electrical operation of the initially insulating (low V_O-concentration) film, brought about instability in device performance due to uncontrolled annihilation or further generation of V_O's.[32] While the stacked Ta_2O_5/HfO_2 layer has demonstrated superb performance over the TiO_{2-x} single-layer e-BRS, a too-high operation voltage was required.[8]

In this regard, Si_3N_{4-x} films grown by plasma-enhanced chemical vapor deposition (PECVD) using SiH_4 and plasma-enhanced NH_3 gas with various NH_3 gas flow rate, which resulted in different x values in the film, was notable.[34] The original intention of the previous work was to maximally utilize the matured defective material properties of Si_3N_{4-x} film, which is already in mass-production for the charge trap layer in NAND flash. An optimum x-value (~ 1.0) was identified in that previous work. When it was too large, the film became too leaky to induce a useful RS, and when it was too small, the film became too insulating – they only broke down under a high field. Even with an optimal $Si_3N_{3.0}$ film, however, the RS operation of the film was still based on the localized i-BRS mechanism, which was mediated by the migration of N atoms between the $Si_3N_{3.0}$ layer and TiN bottom electrode (BE).[34] Therefore,

apart from the original intention, Pt/$Si_3N_{3.0}$/TiN proved to be another i-BRS system, with most of the above-mentioned problems remaining.

In this work, therefore, a thin (3 – 5 nm) Al_2O_3 interfacial barrier layer (IBL) was interposed between the $Si_3N_{3.0}$ layer and the Pt top electrode (TE). Although a similar approach, i.e., interposing an IBL, which generally has higher bonding energy and a larger bandgap than those of the main RS layer, has been pursued in TMO-based ReRAM, the role of such systems has been controversial.[35–37] In contrast, this work clearly demonstrates the role of such an IBL. Most notably, it changed the switching mechanism from localized i-BRS to area-type e-BRS. Also, the IBL prevented carrier injection from the Pt to the Al_2O_3 IBL, making the memory cell self-rectifying. Such an additional feature greatly facilitated an increase in the integration density of the ReRAM cell with a crossbar array (CBA) structure by suppressing sneak current.

3.2. Experimental

The $Pt/Al_2O_3/Si_3N_{3.0}/Ti$ structure in CBA configuration with electrode areas of 16 – 100 μm^2 were fabricated by standard photolithography and lift-off processes. On a Si/SiO_2 substrate, a 50 nm-thick Ti film was deposited with an electron-beam evaporator (Maestech, ZZS550-2/D), and patterned into a line shape with a line width of 4 to 10 μm. Then, a 4 nm-thick $Si_3N_{3.0}$ thin film was deposited with a PECVD system (Surface Technology System, 310PC) using 800 sccm $5\%SiH_4/N_2$ gas and 1000 sccm N_2 gas with 2 sccm NH_3 gas. The applied plasma had a frequency of 187 kHz frequency and 60 W RF power. Under this condition, the x-value was appropriately adjusted to ~ 1.0. Then, Al_2O_3 IBL with thicknesses of 3, 4, and 5 nm were deposited via thermal ALD with $Al(CH_3)_3$ and O_3 as a precursor and an oxygen source, respectively, at 250℃. Finally, 50 nm-thick Pt film was deposited with an electron-beam evaporator (Maestech, ZZS550-2/D) and patterned into a line shape with a line width of 4 to 10 μm in the direction orthogonal to the Ti BE, which completed TE fabrication. Part of the $Al_2O_3/Si_3N_{3.0}$ on the contact pad of the Ti BE was etched out for the electrical contact.

The cross-sectional image of the device and EDS image were examined via a transmission electron microscope (HRTEM, JEOL, JEM-2100F). The electrical properties were measured using a semiconductor parameter analyzer (Hewlett Packard, 4145B) at room temperature in voltage sweep

mode. Additionally, a temperature-dependent test was carried out to analyze the electrical conduction mechanism and retention performance. All biases were applied on the TE, while the BE was grounded. A CBA simulation was performed using the HSPICE tool based on the I-V characteristics of the device in order to elucidate the achievable integration density of the cell in CBA without write and read disturbances.

3.3. Results and Discussions

The samples were fabricated in CBA format with device sizes ranging from 4 x 4 μm^2 to 10 x 10 μm^2, where the IBL thickness was varied from 3 to 5 nm, and $Si_3N_{3.0}$ layer thickness fixed at 4 nm (see Experimental section). In Figure 3.1 (a), the cross-section of the $Pt/Al_2O_3/Si_3N_{3.0}/Ti$ device was examined via a transmission electron microscope. The Ti BE showed a columnar structure with relatively high rough surface morphology, but the 4 nm-thick Al_2O_3 layer and the 4 nm-thick $Si_3N_{3.0}$ layers were uniformly deposited, comprising a reliable ReRAM structure. It is probable that the thin $Si_3N_{3.0}$ layer was chemically modified during the Al_2O_3 layer deposition on top. To examine the possible chemical interactions, energy dispersive spectroscopy (EDS) mapping of each element was performed, as shown in Figure 3.1 (b). The very thin thicknesses of the two layers render a clear assessment rather challenging. Still, the enlarged mapping image of Si, Ti, and O elements at the lower part of the figure indicated that the two layers are generally well separated, but slight oxidation of the lower-lying $Si_3N_{3.0}$ layer could not be disregarded. Also, the top Al_2O_3 layer could be slightly oxygen-deficient, which could not be clearly identified. Nonetheless, the highly insulating property of the Al_2O_3 layer could be identified from the very low leakage current in the negative bias region, as shown in Figure 3.2 (d).

In the authors' previous work, the Pt/$Si_3N_{3.0}$/TiN device showed i-BRS performance when the $Si_3N_{3.0}$ layer was grown under identical conditions with 2 standard cubic centimeters per minute (sccm) NH_3 gas during deposition. [34] To reconfirm the properties of the $Si_3N_{3.0}$ single layer on a Ti instead of TiN electrode, the Pt/$Si_3N_{3.0}$(4 nm)/Ti device was fabricated. Its current-voltage (I-V) characteristic was shown in Figure 3.2 (a), and was almost identical to that of the previous Pt/$Si_3N_{3.0}$(4 nm)/TiN device. This must be due to slight nitridation of the surface of the Ti BE during the PECVD of the $Si_3N_{3.0}$ layer. It was noted that such an i-BRS showed a high operation current (~ mA) and CF-type switching behavior once it was electroformed.

Introducing the Al_2O_3 IBL induced several notable changes. First, the operating current decreased significantly, as seen in Figure 3.2 (b)-(d). When the compliance current (I_{cc}) was increased to ca. 0.5 mA, as in Figure 3.2 (a), the devices usually permanently failed via hard breakdown. Second, due to the suppression of electron injection at the Pt/Al_2O_3 interface under the negative bias condition, the devices showed self-rectification ability. Figure 3.2 (b)-(d) shows representative I-V curves of the samples with IBL thicknesses of 3, 4, and 5 nm, respectively (electrode area, 100 μm^2). Appropriate I_{cc} values were selected from the initial screening experiments for each case. All samples showed an initially insulating pristine state, as expected, but the samples with thicker

IBL showed even more insulating performance. The sample with 3 nm-thick Al_2O_3 in Figure 3.2 (b) did not show useful RS performance – once it was switched to the low-resistance-state (LRS) by the first I-V sweep in the positive bias direction (red line, curves 1 and 2), it did not return to the high-resistance-state (HRS) even after the reset (switching from LRS to HRS) sweep down to -5 V (red and black lines, curves 3 and 4). As elucidated in previous works regarding e-BRS in TMO-based ReRAM, the e-BRS in this stacked samples may also proceed in the following mechanism.[8,12,32] When the positive bias was applied, electrons are readily injected from the Ti BE to the $Si_3N_{3.0}$ layer because of the low energy barrier at the $Si_3N_{3.0}$/(TiN) Ti interface, and a part of the injected electrons are trapped at the trap sites, mostly N-vacancy (V_N), switching the layer from HRS to LRS. During this switching process, the IBL suppresses the loss of electrons from their trap sites by blocking them from moving from the trap sites to the TE. For the reset process (switching from the LRS to HRS) to proceed, a negative bias was applied, and the trapped electrons detraped and moved toward the Ti BE. During this detrapping process, the electron injection from the Pt TE must be sufficiently suppressed, with the help of the IBL. Otherwise, a part of the injected electrons (from the Pt TE) will also be trapped within the $Si_3N_{3.0}$, making the reset difficult. According to this mechanism, the failure of the

reset process in Figure 3.2 (b) can be understood based on the high leakage current even under negative bias.

When IBL thickness was increased to 4 nm, the leakage current in the negative bias region decreased significantly, and fluent RS performance could be achieved in the positive bias region, as shown in Figure 3.2 (c). In this case, the appropriate I_{cc} was ~ 0.1 μA, and the maximum on/off ratio and rectification ratio of ~ 10^2 could be achieved at ~ 4V. It is also notable that the sample showed electroforming-free behavior, as can be identified from the overlap of the red (1st sweep) and black (2nd sweep) I-V curves. When IBL thickness was further increased to 5 nm, as shown in Figure 3.2 (d), the leakage current in the negative bias region was further suppressed, and a rectification ratio of as high as ~ 10^3 could be achieved at ~ 5 V. However, due to the interference of the on-current flow across the thick Al_2O_3 layer in the positive bias region at LRS, the on/off ratio was decreased to lower than 60, and the on-switching voltage was also increased to ~ 4 V, which was ~ 3 V in Figure 3.2 (c). Therefore, it can be concluded that the optimum IBL thickness was 4 nm. The ReRAM performance of this sample is further scrutinized below.

In Figure 3.3 (a)-(d), the RS mechanism was analyzed by examining the electrode area-dependent current and the electrical conduction mechanism analysis. Figure 3.3 (a) shows the variations in the logarithm of the current levels measured at 4 V in the pristine, HRS, and LRS as a

function of the logarithm of the electrode area. All the data well coincided with best-linear-fitting with a fixed slope of 1. This finding indicated that the current flows uniformly across the entire electrode area in the three states. This data is in stark contrast to the previous case with the Pt/$Si_3N_{3.0}$/TiN structure, where the pristine film showed area-type leakage current (slope of 1 in a similar plot), and the LRS and HRS showed almost no area-dependency, indicating an involvement of the CFs.[34] Therefore, trap sites uniformly spread in the $Si_3N_{3.0}$ layer contributed to the e-BRS of the device, which might be useful in achieving better uniformity in large-density array devices.

When measuring I-V characteristics at different temperatures, the current of the device at HRS generally increased, suggesting a thermally activated mechanism. Each current for positive and negative bias was attempted to be fitted with the Poole-Frenkel (P-F), Schottky, and Fowler-Nordheim (F-N) tunneling mechanisms. The HRS current for positive bias was fitted well with the P-F fitting. The plots in the form of $Ln(I/(E*T^{3/2}))$ *vs. 1/T* according to the P-F equation for voltages ranging from 4 to 5 V are shown in Figure 3.3 (b). For the fittings, the electric field (*E*) was calculated by dividing the voltage applied over the $Si_3N_{3.0}$ layer, which could be estimated from the thicknesses and dielectric constants of $Si_3N_{3.0}$ (4 nm, ~7) and Al_2O_3 (4 nm, ~8) and the total applied voltage, assuming that conduction was governed by the $Si_3N_{3.0}$ layer.

Because the bandgap of PECVD Si_3N_4 and amorphous atomic layer deposition (ALD) Al_2O_3 are ~ 5 and ~ 7 eV, respectively, it is tempting to conclude that the electrical conduction in such a stacked-layer system is governed by the Al_2O_3 layer.[38,39] However, as shown in Figure 3.4 below, the energy level of the conduction band edge (CBE) of the Al_2O_3 layer fell well below that of the $Si_3N_{3.0}$ layer and the Fermi level of Ti under the sufficiently high positive bias condition. Therefore, it is plausible that electrical conduction is controlled by the $Si_3N_{3.0}$ layer under this bias condition, meaning that the status of the traps inside this layer would determine RS performance. From the slopes of the best-linear-fitted graphs at each voltage, the activation energy, which corresponded to the trap depth at each voltage, could be calculated, and the results are summarized in Figure 3.3 (c). According to the P-F theory, which explains the trap depth decrease with increasing field due to Coulombic interactions, the data were extrapolated to $E = 0$, and a trap depth of 0.75 eV was estimated. This value is reasonably consistent with the reported trap depth in CVD Si_3N_4 films, suggesting the feasibility of this analysis.[40,41] The relatively low trap depth can be ascribed to the high density of traps because of the very high value of x ~ 1.0. The estimated value of the dielectric constant from the P-F fitting near room temperature was ~ 2.3, which coincided reasonably well with the value of the optical dielectric constant ranging from 2.95 to 4.16 calculated from the square

of the refractive index (n ranging from 1.72 to 2.04).[42,43] Unfortunately, the noisy current of the LRS under the positive bias condition makes it difficult to analyze the conduction mechanism through temperature dependency.

Under the negative bias condition, the F-N tunneling fits the experimental data well. Figure 3.3 (d) shows the *Ln(J/E²) vs. 1/E* graphs plotted at voltages ranging from -4.5 to -5 V. The tunneling barrier height could be calculated from the slope of the best-linear-fitted graphs, using the equation,

$$\mathrm{J} = \frac{q^2}{8\pi h}\frac{E^2}{\psi_0} exp\left(-\frac{2}{3}\frac{a^*\psi_0^{3/2}}{E}\right) \quad (1)$$

, where q is the elementary charge, h is Planck's constant, E is the electric field, ψ_0 is an F-N tunneling barrier height. a^* is $\frac{2(2m_0q)^{1/2}}{h}\left(\frac{m^*}{m_0}\right)^{1/2}$, where m_0 is the free electron mass and m^* is the electron effective mass. The calculated F-N tunneling barrier height is plotted in the inset of Figure 3.3 (d), indicating ~ 1.3 – 1.5 eV of barrier height. For this estimation, the electric field (E) was calculated by dividing the voltage applied over the Al_2O_3 layer, which could be estimated from the thicknesses and dielectric constants of $Si_3N_{3.0}$ (4 nm, ~7) and Al_2O_3 (4 nm, ~8) and the total applied voltage. This estimation suggests that the low leakage current for negative bias was caused by the suppression of electron injection from the Pt to Al_2O_3 layer by the presence of a high Schottky barrier. When the voltage became high

enough, electrons could get through the barrier by F-N tunneling. Although a 1.4 eV barrier does not correspond to the ideal Schottky barrier at the Pt/Al_2O_3 interface, it can be lowered by several factors, pinning the Fermi level close to the conduction band edge.

It should be noted that equation (1) is an approximation, assuming low temperature (T) of a more rigorous form of the tunneling current with a trapezoidal barrier configuration. The rigorous equation reveals that the tunneling current increases with increasing T with a T^2-dependency.

A schematic band diagram is shown in Figure 3.4 based on the data discussed so far. The conduction band offset between Al_2O_3 and $Si_3N_{3.0}$ was calculated as ~ 0.7 eV considering the reported electron affinities of the two materials, which is slightly lower than the trap depth in the $Si_3N_{3.0}$ layer.[44–46] The actual value must be smaller than 0.7 eV due to the lowered bandgap of amorphous Al_2O_3. Thus, electron transport across the stacked-layer under the positive bias condition must be governed by the $Si_3N_{3.0}$ layer, not by the Al_2O_3 IBL or the interface between them. When a positive bias was applied to the Pt TE, the electron injected from the Ti BE filled the trap sites in the $Si_3N_{3.0}$ layer, which are represented as empty circles in Figure 3.4 (a). After a sufficient voltage was applied, the trap sites were filled with electrons in Figure 3.4 (b), and the sample switched to LRS, which is dominated by the conduction involving shallow trap or band conduction. The reset operation proceeded by applying a negative

bias to the Pt TE, as shown in Figure 3.4 (c). In this circumstance, the trapped electrons in the trap sites detrapped, and the sample returned to the HRS in Figure 3.4 (d), while the carrier injection from the Pt TE must have been suppressed by the high Schottky barrier at the Pt/Al_2O_3 interface.

Rectifying I-V characteristics are useful for applying the sample to the passive CBA because sneak current could be suppressed. The authors′ group has developed a quantitative method to estimate the available maximum CBA size using the HSPICE simulation.[47,48] The simulation requires the on/off current ratio and rectification ratio, which could be identified from the I-V curve shown in Figure 3.2 (c), and interconnection wire resistance, which could be calculated from the resistivity of the given electrode materials (~ 200 and ~ 20 μΩ cm for Ti BE and Pt TE, respectively). Figure 3.5 shows the calculated read margin (RM, left y-axis) and writing margin (WM, right axis) as a function of the total number of bits in a given CBA block. Here, RM is defined as $\frac{I_{REF}-I_{HRS}}{I_{REF}-I_{HRS,0}}$, where I_{REF} is defined as $\sqrt{I_{LRS,0}I_{HRS,0}}$, and $I_{HRS,0}$ ($I_{LRS,0}$) indicates the reading current of HRS (LRS) with a single device.[47] Since the square shape of the CBA was assumed in this simulation, the number of word-lines and bit-lines were identical and were given as the square-root of the allowed number of bits. When the RM decreased to 10% at an increased number of bits, the bit number corresponded to the allowed

array size for the read without disturbance due to the involvement of sneak current. In the simulation, CBA size allowing for a 10% RM was over 10^6, with the scheme of all the unselected BLs grounded. The WM was calculated with a 1/2 voltage (1/2 V) scheme.[47] In the 1/2 V scheme, half of the operation voltage was applied to all unselected WL and BL, where the main disturbing factor occurred at the half-selected cells. The WM could be defined as $\frac{|V_{set\ (or\ reset)}|-|V_{unwant}|}{|V_{set\ (or\ reset)}|}$, where $V_{set\ (or\ reset)}$ is set or reset voltage of the sample and V_{unwant} is the applied voltage at the unselected cell. In Figure 3.5, the achievable CBA size through the WM calculation was over 10^6 cells. These values are superior to those of the previous work because of the increased rectification ratio and on/off ratio over 10^2.[34]

Figure 3.6 (a) shows the retention performances of the sample with 4 nm-thick Al_2O_3 IBL with a cell area of 100 $\square m^2$ at different temperatures and a reading voltage of 4 V. At 110ºC, the resistance of HRS maintains its initial value over 10^4 seconds, suggesting the stability of HRS. As the stability of the HRS must be decided by the persistence of the detrapped state of the $Si_3N_{3.0}$ traps, such stability suggested that the Fermi level of the Ti electrode located below the energy level of the $Si_3N_{3.0}$ traps. This relative energy position of the Ti Fermi level and $Si_3N_{3.0}$ traps is, however, unfavorable for the stability of LRS, as shown in the same figure. The trapped electrons tend to detrap by transporting to the Fermi level of Ti.

The estimated activation energy, shown in Figure 3.6 (b), must correspond to the hopping energy for the electrons to move from the trap to Ti. In this case, the LRS retention failure time was defined as the time to reach LRS resistance of 10^9 Ohm, as shown in Figure 3.6 (a) (horizontal red dashed line), and the time is plotted as a function of retention measurement temperature according to the Arrhenius form. Figure 3.6 (c) shows the schematic band diagram under no external bias. Due to the work function mismatch between the Pt TE and Ti BE, there should be an internal field, which favors the detrapped state of the traps in the $Si_3N_{3.0}$ layer. Therefore, subsequent research should seek an appropriate TE material, which would not induce such a high internal field but still maintain the high Schottky barrier with Al_2O_3.

Figure 3.6 (d) shows the endurance test results of the same sample at room temperature under the DC I-V sweep condition, where the resistance values were measured at 4 V. The sample showed stable switching only up to ~ 100 cycles. The degradation was mainly caused by the continuous decrease in HRS resistance and sudden increase in LRS resistance in the later stages of the test. Such degradation may be related to the decrease in V_N concentration with the increasing endurance test cycle. Similar degradation has been observed in the V_O-related e-BRS case using the TiO_{2-x} material, and the degradation could be partially recovered by applying a bias that rejuvenated the V_O concentration.[32] A

similar test should be done in the future to further understand the RS performance of this material system.

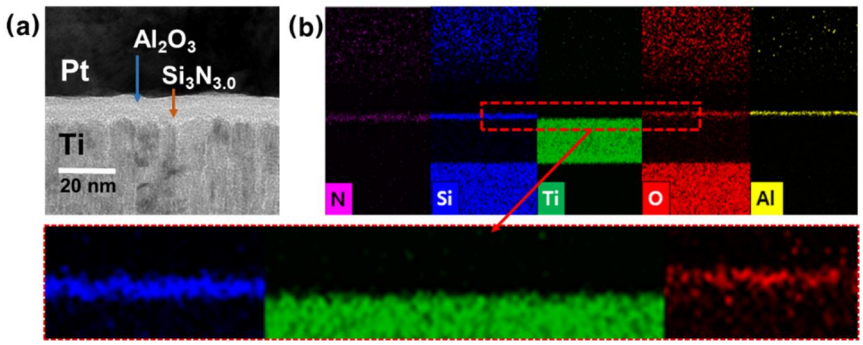

Figure 3. 1 (a) TEM image of the Pt/Al_2O_3(4 nm)/$Si_3N_{3.0}$(4 nm)/Ti device and (b) EDS mapping image of each element. The lower image shows the enlarged portion indicated by the dashed rectangle.

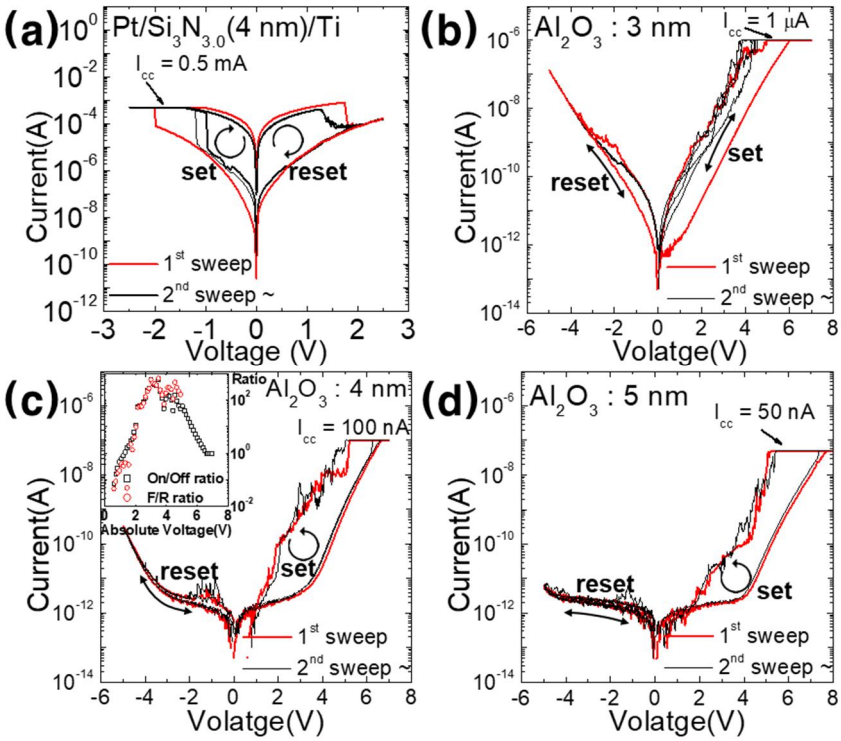

Figure 3. 2 Typical e-BRS characteristics of (a) $Pt/Si_3N_{3.0}$(4 nm)/Ti device and $Pt/Al_2O_3/Si_3N_{3.0}$ (4 nm)/Ti devices with Al_2O_3 thickness of (b) 3 nm, (c) 4 nm, and (d) 5 nm. The resistance ratio between HRS and LRS, and the rectification ratio as a function of absolute voltage (Inset in (c)).

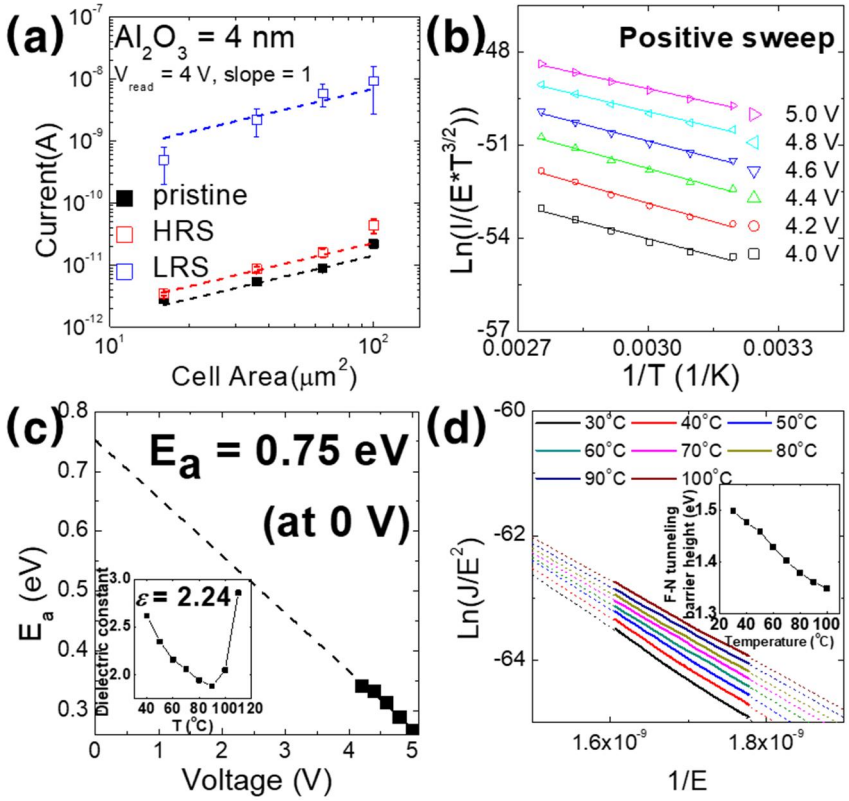

Figure 3. 3 (a) Area dependency of current at 4V for pristine, HRS, and LRS of $Pt/Al_2O_3/Si_3N_{3.0}/Ti$ device. (b) Poole-Frenkel fitting of HRS at positive sweep with the equation $Ln(I/(E*T^{3/2}))$ *vs.* $1/T$ and (c) calculated activation energy and dielectric constant (inset in (c)). (d) Fowler-Nordheim tunneling fitting of HRS at negative sweep and the calculated tunneling barrier height (inset in (d)).

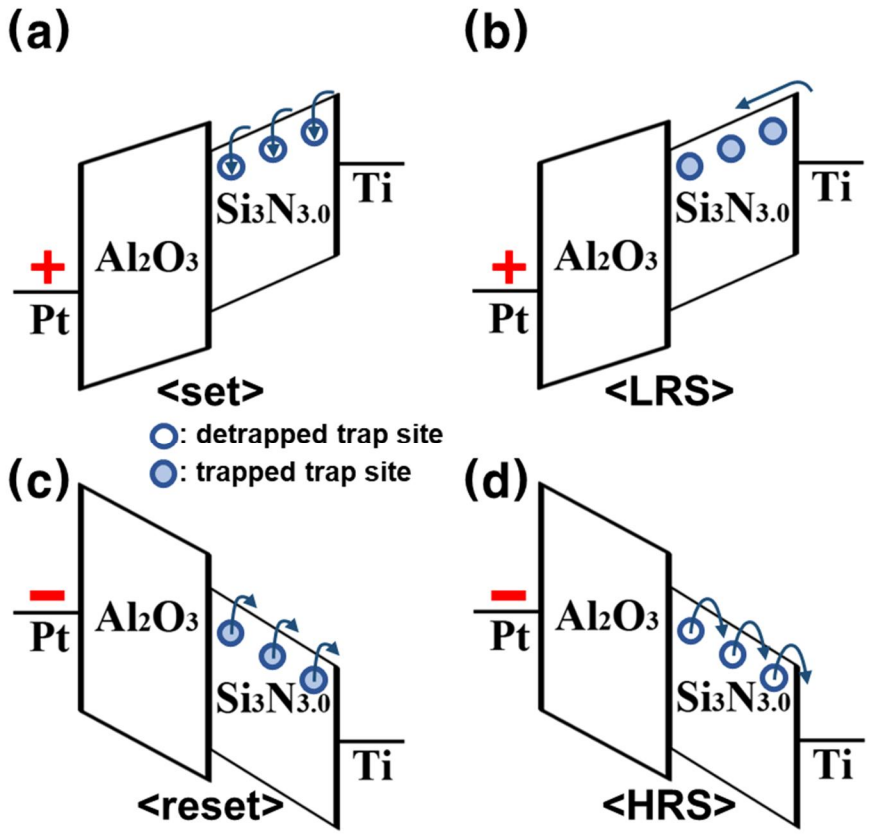

Figure 3. 4 Band diagram and electron behavior in (a) pristine (HRS) and (b) LRS for positive bias and in (c) LRS and (d) HRS for negative bias.

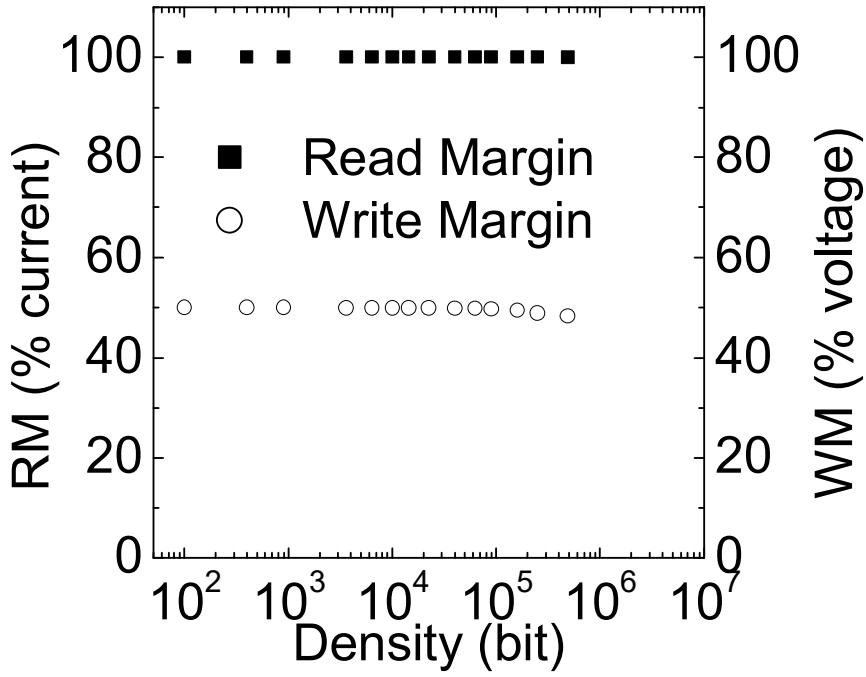

Figure 3. 5 Results of HSPICE simulation done to obtain the allowable CBA size considering read and write margins.

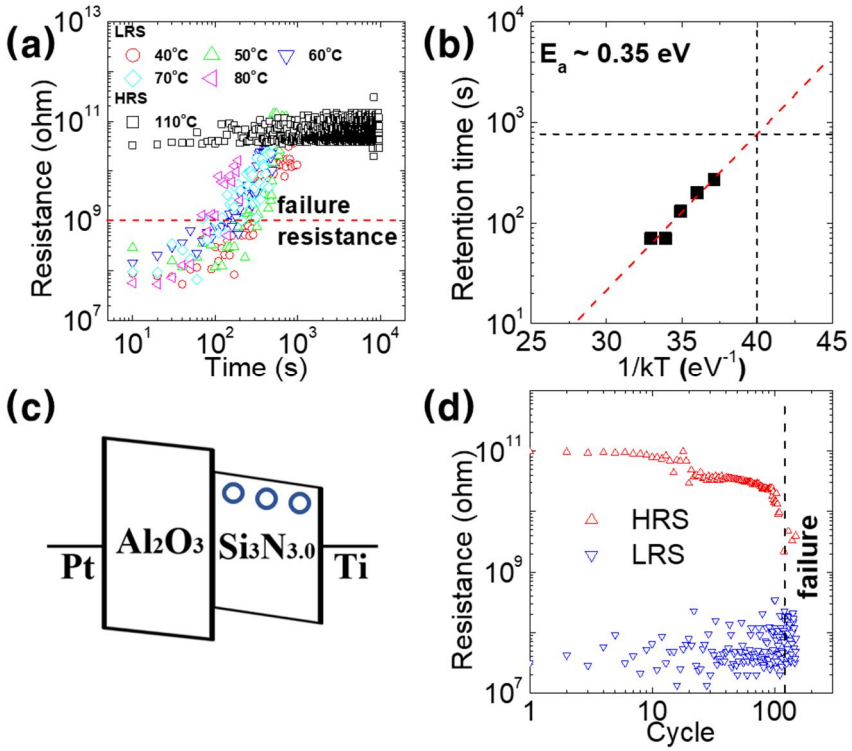

Figure 3. 6 (a) Retention and (b) the Arrhenius-type graph of retention time. (c) Schematic diagrams of band structure for the zero-bias condition. (d) Endurance of the Pt/Al_2O_3/$Si_3N_{3.0}$/Ti device.

3.4. Conclusion

In conclusion, the e-BRS property could be obtained from a $Pt/Al_2O_3/Si_3N_{3.0}/Ti$ device with a 4 nm-thick $Si_3N_{3.0}$ layer. At the optimized 4 nm thickness of the Al_2O_3 IBL, the device efficiently blocked the injection of electrons from the Pt electrode, while carrier transport in the positive bias direction interfered minimally. Such a role of IBL provided the device with the ability to self-rectify. Electron trapping/detrapping at the trap sites in the $Si_3N_{3.0}$ layer contributed to the creation of a forming-free e-BRS. The cell-area-dependency revealed that the trap sites, uniformly distributed over the $Si_3N_{3.0}$ thin film area, were involved in the resistive switching. Electrical conduction mechanism analysis of the HRS revealed that P-F conduction dominated overall conduction at positive bias with a trap depth of ~0.75 eV at 0 V in $Si_3N_{3.0}$. The conduction at negative bias was dominated by F-N tunneling conduction with 1.4 eV of barrier height between Pt and Al_2O_3. The HSPICE simulation of RM and WM confirmed that the maximum CBA cell size was available over 10^6 bits. However, the data retention and endurance of the 4 nm-thick Al_2O_3 device were not satisfactory due to the shallow trap depth of trap sites in the $Si_3N_{3.0}$ layer, which were annihilated as cycle number increased. Also, the setup of an internal field due to the work function mismatch of the two electrodes preferred the detrapped state of the $Si_3N_{3.0}$ thin film. The retention can be improved by replacing

the Pt TE with another TE material having slightly lower work function to reduce the internal field. If it is too low, the rectification would be degraded. Therefore, the TE material should be carefully chosen to ensure a subtle balance between retaining the rectification and decreasing the internal field. In addition, optimized silicon nitride thin film with higher trap depth would improve the reliability properties of the device. Perhaps doping the silicon nitride film with aliovalent cation or decreasing N-deficiency would be the viable option for this direction.

4. 1S1R property with $Pt/Si_3N_{4-x}/TiN$ resistive switching device and $Pt/TiO_2/TiN$ selector device

4.1. Introduction

Resistive switching random access memory (ReRAM), which has simple metal-insulator-metal structure, maximize its scalability by adopting to crossbar-array structure.[49–52] Since the CBA is a passive array device, the selector is indispensable to suppress the sneak current.[53–56] When the ReRAM shows unipolar or nonpolar resistive switching, the diode with sufficient high forward/reverse rectification ratio and forward current density is the most suitable selector.[57] However, the diode cannot be used for the ReRAM with bipolar resistive switching, because of its polarity operation, and the device with nonlinearity could be a solution for bipolar-type ReRAM. Besides the polarity issue, operation condition like voltage, current density and nonlinearity should be optimized for 1S1R integration, as well as additional problem with stacked devices.

The authors' group have reported the property of $Pt/TiO_2/TiN$ device for nonlinear selector device.[48] Using this nonlinear selector device, 1S1R

device with Pt/$Si_3N_{3.0}$/TiN device with bipolar resistive switching property was fabricated via lift-off process, forming single cell structure and crossbar-array structure with 2 by 2 and 9 by 9 dimension, respectively. By investigating the characteristics of the device from single cell to 9 by 9 CBA, the deposition condition of each layer was optimized and additional problems, such as side-wall conduction and series line resistance, were confirmed.

4.2. Experimental

The Pt/TiO_2/TiN/Pt/$Si_3N_{3.0}$/TiN structure in single cell structure and crossbar-array structure with 2 by 2 and 9 by 9 cell dimension were fabricated by standard photolithography and lift-off processes. On a Si/SiO_2 substrate, a 50 nm-thick TiN film was grown by the reactive sputtering technique using a commercial sputtering tool. Then, $Si_3N_{3.0}$ thin film was deposited with a PECVD system (Surface Technology System, 310PC) using 800 sccm 5%SiH_4/N_2 gas and 1000 sccm N_2 gas with 2 sccm NH_3 gas. The applied plasma had a frequency of 187 kHz frequency and 60 W RF power. Then, Pt and TiN electrode with thicknesses of 20 nm were deposited via an electron-beam evaporator (Maestech, ZZS550-2/D) and the reactive sputtering technique using a commercial sputtering tool, respectively. The TiO_2 films were deposited via atomic layer deposition using $Ti(OC_3H_7)_4$ and O_3 as the Ti-precursor and oxygen source, respectively. Then, 80 nm thick Pt top electrode was deposited by the e-beam evaporator.

The electrical properties were measured using a semiconductor parameter analyzer (Hewlett Packard, 4145B) at room temperature in voltage sweep mode.

4.3. Results and Discussions

Figures 4.1 showed the optical images of the 1S1R device with single cell (a), 2 by 2 CBA (b), and 9 by 9 CBA (c), respectively. It was confirmed that the bottom/top electrode patterns were aligned well, keeping each other perpendicular. The more the number of devices connected in parallel increases, the higher the chance that the device will not operate properly. And, in a large CBA structure, it is difficult to determine the cause of the malfunction due to its complicated structure. Therefore, the issue in the large-sized CBA was analysed based on the evaluation in the small-sized CBA.

Figure 4.2 showed the properties of (a) Pt/TiO_2/TiN selector device and (c) Pt/$Si_3N_{3.0}$(4 nm)/TiN RS device, respectively.[34,48] The selector device with various cell area shows ~10 of nonlinearity at reading voltage of 1.5 V. Figure 4.2 (b) showed the selector property with various TiO_2 thickness and it could be confirmed that negative current decreased as the thickness of TiO_2 increased. In Figure 4.2 (c), the $Si_3N_{3.0}$ RS device shows proper BRS property with -3 V of set voltage and 4 V of reset voltage. Based on the properties of each device, 1S1R device was fabricated and the deposition condition was optimized.

To fabrication of 1S1R, the stacking order of each layer was one of the issues to consider. Figure 4.3 (a) and (b) shows reversed stacking order of 1S1R with single cell structure. In Figure 4.3 (a), where selector layer deposited first and RS layer deposited later, the device didn't show nonlinearity both positive and negative bias. On the other hand, In Figure 4.3 (b), where RS layer deposited first and selector layer deposited later, the device showed nonlinearity and proper BRS behaviour occurred. This failure was related with the deposition temperature of $Si_3N_{3.0}$ RS layer with 300ºC and the heat budget during $Si_3N_{3.0}$ deposition process broken down the TiO_2 selector layer, deposited previously. Therefore, $Si_3N_{3.0}$ RS layer deposition should be preceded to TiO_2 selector layer deposition. In addition, an existing 4 nm of $Si_3N_{3.0}$ thin film was deposited at 3 nm to improve the cell yield, shown in Figure 4.3 (c). As a result, stable 1S1R operation could be obtained with single cell structure.

Figure 4.4 (a) shows 1S1R property with 2 by 2 CBA structure with identical deposition condition of Figure 4.3 (c) and all the cells in 2 by 2 CBA structure showed proper BRS property with ~100 of nonlinearity. However, the device with 9 by 9 CBA structure didn't show BRS property without operation of reset at positive bias, shown in Figure 4.4 (b). This failure was due to high line resistance, shown in Figure 4.4 (c). That is, the applied voltage for $Si_3N_{3.0}$ layer became lower as the line resistance increased by the voltage distribution. As a result, the applied voltage for

$Si_3N_{3.0}$ layer was not sufficiently high enough to reset operation. Thus, this problem could be solved by lowering line resistance of electrode.

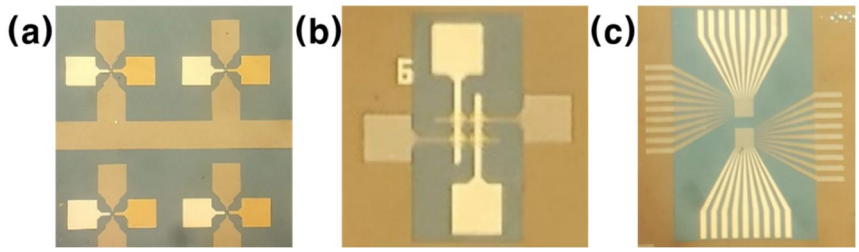

Figure 4. 1 Optical image of (a) single cell, (b) 2 by 2 CBA structure, and (c) 9 by 9 CBA structure of $Pt/TiO_2/TiN/Pt/Si_3N_{3.0}/TiN$ 1S1R device

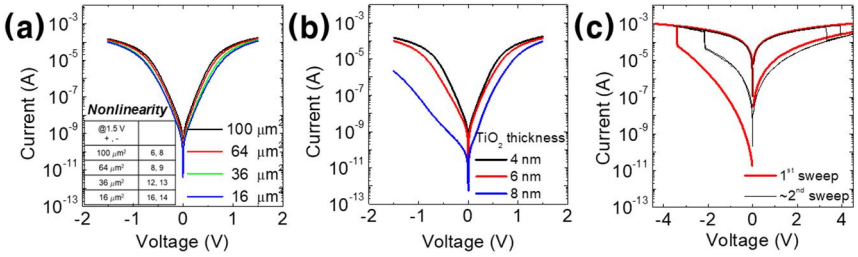

Figure 4. 2 I-V characteristics of Pt/TiO_2/TiN selector device with (a) various cell area and (b) various TiO_2 thickness. (inset table of (a) represent the nonlinearity at 1.5 V) (c) I-V characteristics of Pt/Si3N3.0(4 nm)/TiN device.

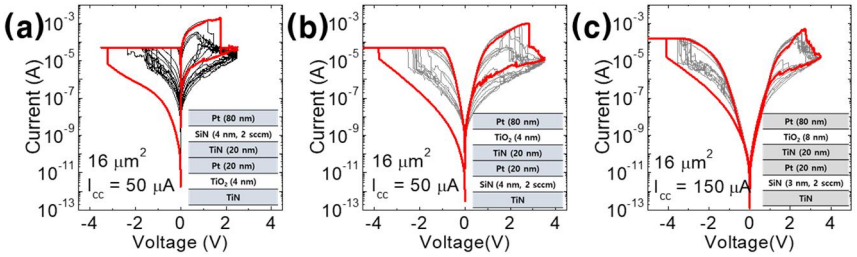

Figure 4. 3 I-V characteristics of (a) Pt/$Si_3N_{3.0}$(4 nm)/TiN/Pt/TiO_2/TiN device,

(b) Pt/TiO_2/TiN/Pt/$Si_3N_{3.0}$(4 nm)/TiN device, and

(c) Pt/TiO_2/TiN/Pt/$Si_3N_{3.0}$(3 nm)/TiN device

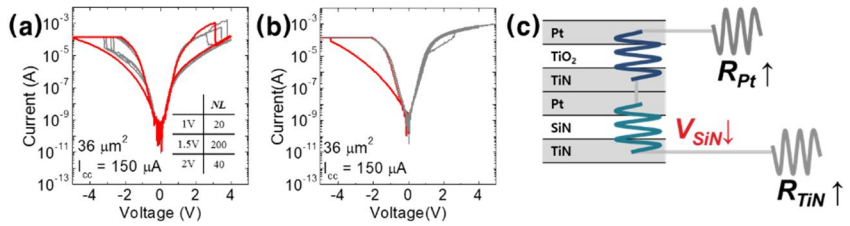

Figure 4. 4 I-V characteristics of Pt/TiO_2/TiN/Pt/$Si_3N_{3.0}$(3 nm)/TiN device with (a) 2 by 2 CBA structure and (b) 9 by 9 CBA structure. (c) schematic diagram of resistance component.

4.4. Conclusion

In conclusion, 1S1R device was fabricated with the Pt/Si_3N_{4-x}/TiN RS layer and Pt/TiO_2/TiN selector layer using the atomic-layer deposited TiO_2 film. The device was fabricated via lift-off process with single cell, 2 by 2 and 9 by 9 crossbar-array pattern. Based on the property of selector device and RS device respectively, 1S1R device with single cell structure and 2 by 2 CBA structure, which showed proper nonlienar BRS property, was fabricated. However, the device didn't show reset operation due to the series line resistance of top/bottom electrode and this could be solved by lowering the line resistance.

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6. Conclusion

In this dissertation, resistive switching based on Si_3N_{4-x} was examined, and the switching mechanism was prosed. The N-deficiency of Si_3N_{4-x} is crucial factor for filamentary BRS operation and optimized condition can be found. By inserting Al_2O_3 IBL, the device change its switching mechanism from filamentary BRS to electronic BRS.

In the first part of the study, the electrical property of bipolar resistive switching of Si_3N_{4-x} becomes tunable and be optimized by controlling the NH_3 gas flow rate during Si_3N_{4-x} thin film deposition process. Through XPS examination, the decrease of NH_3 gas flow rate induces Si_3N_{4-x} thin film to become more defective. The device with 2 sccm NH_3 gas flow rate shows the best performance and the self-compliance behavior due to the involvement of the line resistance of the Pt/TiN electrode. Also, the resistance switching is governed by recovery/rupture of the conducting filament which might be composed of heavily reduced Si ions (or their clusters). The electrical conduction mechanism analysis of the HRS revealed that the conduction was mediated by the electron hopping process in the low voltage region whereas the conduction in the high voltage region was dominated by the space charge limited conduction. The activation energy and hopping distance decrease with the decreasing NH_3 gas flow rate during the PECVD of the Si_3N_{4-x} thin film for

both the pristine and HRS. The 2 sccm device shows excellent retention performance over 10 years at room temperature. It was found that the Si_3N_{4-x} could be a feasible contender to be used as a fluent resistance switching device only when the growth condition was appropriately controlled to make the pristine film relatively defective. If the pristine film was too insulating by depositing stoichiometric Si_3N_4, it was improbable to switch them into the feasible memory state by normal electrical stresses with the settled compliance current.

In the second part of the study, the e-BRS property could be obtained from a Pt/Al_2O_3/$Si_3N_{3.0}$/Ti device with a 4 nm-thick $Si_3N_{3.0}$ layer. At the optimized 4 nm thickness of the Al_2O_3 IBL, the device efficiently blocked the injection of electrons from the Pt electrode, while carrier transport in the positive bias direction interfered minimally. Such a role of IBL provided the device with the ability to self-rectify. Electron trapping/detrapping at the trap sites in the $Si_3N_{3.0}$ layer contributed to the creation of a forming-free e-BRS. The cell-area-dependency revealed that the trap sites, uniformly distributed over the $Si_3N_{3.0}$ thin film area, were involved in the resistive switching. Electrical conduction mechanism analysis of the HRS revealed that P-F conduction dominated overall conduction at positive bias with a trap depth of ~0.75 eV at 0 V in $Si_3N_{3.0}$. The conduction at negative bias was dominated by F-N tunneling conduction with 1.4 eV of barrier height between Pt and Al_2O_3. The

HSPICE simulation of RM and WM confirmed that the maximum CBA cell size was available over 10^6 bits. However, the data retention and endurance of the 4 nm-thick Al_2O_3 device were not satisfactory due to the shallow trap depth of trap sites in the $Si_3N_{3.0}$ layer, which were annihilated as cycle number increased. Also, the setup of an internal field due to the work function mismatch of the two electrodes preferred the detrapped state of the $Si_3N_{3.0}$ thin film. The retention can be improved by replacing the Pt TE with another TE material having slightly lower work function to reduce the internal field. If it is too low, the rectification would be degraded. Therefore, the TE material should be carefully chosen to ensure a subtle balance between retaining the rectification and decreasing the internal field. In addition, optimized silicon nitride thin film with higher trap depth would improve the reliability properties of the device. Perhaps doping the silicon nitride film with aliovalent cation or decreasing N-deficiency would be the viable option for this direction.

Finally, 1S1R device was fabricated with the Pt/Si_3N_{4-x}/TiN RS layer and Pt/TiO_2/TiN selector layer using the atomic-layer deposited TiO_2 film. The device was fabricated via lift-off process with single cell, 2 by 2 and 9 by 9 crossbar-array pattern. Based on the property of selector device and RS device respectively, 1S1R device with single cell structure and 2 by 2 CBA structure, which showed proper nonlienar BRS property, was fabricated. However, the device didn't show reset operation due to the

series line resistance of top/bottom electrode and this could be solved by lowering the line resistance.

This thesis presnets a deeper understanding on the resistive switching of the Si_3N_{4-x} device and its application. By introducing Al_2O_3 IBL layer or Pt/TiO_2/TiN selector device, the device shows the potential to suppress the sneak current at CBA structure. These results in this thesis could shed light on this field by suggesting new pathways different from the conventional approach.

List of publications

1. Refereed Journal Articles (SCI)

1.1 Domestic

1.2. International

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7. Kyung Jean Yoon, Seul Ji Song, Jung Ho Yoon, Tae Hyung Park, **Dae Eun Kwon**, Young Jae Kwon, Hae Jin Kim, and Cheol Seong Hwang, "Effect of charging and discharging by parasitic capacitance in complementary resistive switching transition metal oxides", 14th Annual Non-Volatile Memory Technology Symposium, Jeju, Korea, October 27-29 (2014), poster

Abstract (in Korean)

외부 자극에 의해 소자의 저항상태를 변화시키는 저항 변화 메모리는 차세대 비휘발성 메모리의 유망한 후보 중 하나이다. 간단한 MIM 구조, 저전력 소모, 고 집적성 그리고 CMOS 적합성으로 인해 저항 변화 메모리는 NAND 플래시 메모리를 대체할 고집적 메모리로 많은 기대를 받고 있다. NiO, TiO_2, HfO_2 그리고 Ta_2O_5 와 같은 전이금속 산화물이 저항변화 메모리 소자 제작과 거동 분석의 주된 초점이였다. 반면에 Si_3N_4 와 같은 질화막 또한 저항 변화 메모리로 쓰이지 않을 이유가 없을 것이다. 실제로 Si_3N_4 의 Si 와 N 의 비율은 박막내의 결함을 유도하기위해 손쉽게 조절 가능하며, NAND 플래시 메모리에서의 charge trap layer 로서도 이미 널리 쓰여지고 있다. 결함의 생성으로 인한 일명, 전도 필라멘트는 저항 변화 메모리의 주된 거동이다. 따라서 N 원소가 부족한 Si_3N_4 즉 Si_3N_{4-x} 는 저항변화 물질로 사용 가능 할 것이다.

본 연구의 첫번째 파트에서는 N 원소의 부족한 정도에 따른 Si_3N_{4-x} 의 양극성 저항변화 특성 (BRS) 을 조사하기위해 Si_3N_{4-x} 박막의 plasma enhanced chemical vapor deposition 과정 중에 사용되는 NH3 가스 유량을 다양하게 하여 $Pt/Si_3N_{4-x}/TiN$ 소자를 제작하였다. X-ray photo-electron spectroscopy 분석을 통해, NH_3 가스 유량이 감소함에 따라 Si_3N_{4-x} 박막내의 질소 원소의 분율이 감소함을 확인할 수 있었고 NH_3 가스 유량을 조절함으로서 질소 원소의 부족한 정도를

조절할 수 있음을 알아내었다. 질소 원소의 부족한 정도는 Si_3N_{4-x} 의 전류-전압 특성과 BRS 거동에 영향을 미치며 최적화된 조건을 찾을 수 있었다. 또한 Pt/TiN 전극의 직렬 선저항으로 인해 compliance 전류 없이 안정적인 BRS 거동을 보이는 self-compliance 거동이 나타남을 확인하였다. Si_3N_{4-x} 소자는 전류-전압 특성에서 면적 의존성을 보이지 않았으며 이는 전도 필라멘트의 형성과 끊어짐에 의해 저항 변화 거동이 보임을 암시하였다. 저항 변화 거동의 추가적인 분석을 위해 전류-전압 특성의 온도의존성 측정을 진행하였다. 전류-전압 그래프의 더블 로그 플롯을 통해, 저전압과 고전압 영역대에서 피팅을 한 결과 1 과 2 가 각각 나옴을 확인하였으며 이는 child's law 를 따르며 Si_3N_{4-x} 의 전도가 space charge limited conduction 에 의해 이루어짐을 알 수 있었다. 또한 hopping conduction 을 위한 활성화 에너지와 hopping 거리도 계산하였으며 두개의 값 모두 NH_3 가스 유량이 감소함에따라, 그리고 스위칭이 나타난 후에 감소함을 알 수 있었다. 이러한 결과로부터 질소 원소가 TiN 하부전극으로 밀려나가며 trap 들이 뭉침으로 인해 전도 필라멘트가 형성됨을 확인할 수 있었다. 또한 초기 Si_3N_{4-x} 의 trap 상태가 전도 필라멘트 형성에 중요한 역할을 하며 그렇지 않으면 소자는 망가지는 것을 확인하였다.

본 연구의 첫 번째 파트에서의 Si_3N_{4-x} 박막의 BRS 특성에 기초하여, Al_2O_3 계면 장벽 층이 최적화 된 증착 조건으로 만들어진

$Si_3N_{3.0}$ 층과 Pt 상부 전극 사이에 삽입되며 그 결과 다양한 Al_2O_3 막 두께 (3-5 nm)를 갖는 $Pt/Al_2O_3/Si_3N_{3.0}/Ti$ 소자를 형성 하였다. TEM 이미지와 EDS 매핑 이미지로 Al_2O_3 와 $Si_3N_{3.0}$ 층 사이의 분리를 확인 가능하였다. $Pt/Si_3N_{3.0}/Ti$ 소자는 필라멘트의 BRS 특성을 나타내지만, $Pt/Al_2O_3/Si_3N_{3.0}/Ti$ 소자는 forming-free 특성을 갖는 e-BRS 특성을 나타냈다. 또한 이 소자는 자체 정류 특성 및 비선형성 특성을 가지는데, 이러한 특성은 큰 사이즈의 크로스바 어레이 (CBA) 구조에서 누설전류를 방지하는데 도움이 되며, Al_2O_3 층의 높은 밴드 갭으로 인해 이러한 특성이 나타나게 된다. 장치는 HRS 및 LRS 에서 면적 의존성을 보여 주었으며 이는 계면의 e-BRS 저항 변화 메커니즘을 지배 한다는 것을 나타낸다. 또한 온도 의존성 분석을 통해 $Si_3N_{3.0}$ 층에 존재하는 trap site 의 trap 깊이 및 Pt 와 Al_2O_3 사이의 쇼트키 배리어 높이를 알아낼 수 있었다. 따라서, 해당 소자는 $Si_3N_{3.0}$ 저항 변화층의 trap site 에서 전자를 트래핑 / 디트랩핑하여 저항 상태를 바꾼다는 걸 확인 가능하였다. 또한 가능한 최대 CBA 크기를 추정하기 위해 HSPICE 시뮬레이션을 수행하였으며 약 10^6 의 값을 얻을 수 있음을 확인하였다.

저항 변화 메모리로 CBA 구조를 형성할 때, 선택된 셀의 적절한 구동을 위해선 누설 전류가 가장 큰 문제이다. 누설 전류를 억제하기 위해, 트랜지스터의 사용은 하나의 해결책이 될 수 있다. 하지만, 상대적으로 큰 사이즈의 트랜지스터 소자는 저항 변화

메모리의 고집적을 방해하게 된다. 이러한 점에서 간단한 MIM 구조를 갖는 선택소자는 누설전류를 충분히 억제하면서 트랜지스터를 대체할 수 있을것이다. 따라서 1 선택소자 1 저항변화 물질의 적층된 소자 (1S1R) 에서 생길 수 있는 문제점에 대해 조사할 필요가 있다. 본 연구의 세번째 파트에서는, 첫번째 파트에서의 $Pt/Si_3N_{4-x}/TiN$ 저항 변화 소자와 ALD TiO_2 박막을 사용한 $Pt/TiO_2/TiN$ 선택소자를 이용하여 1S1R 소자를 제작하였다. 해당 소자는 lift-off 공정을 통해 단일소자, 2 by 2 그리고 9 by 9 CBA 패턴으로 제작되었다. 각각의 소자를 비교하면서 선택소자와 저항변화 층의 최적화된 증착 조건을 찾아내었고 극복해야할 추가적인 문제또한 확인 하였다.

주요어: 저항 변화 스위칭, 실리콘 나이트라이드, 비휘발성 메모리, 누설 전류, **plasma enhanced chemical vapor deposition**

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