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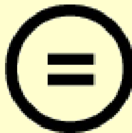

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Ph.D. DISSERTATION

Surface Ge-rich SiGe Channel Tunnel Field-Effect Transistor Fabricated by Ge Condensation Technique

Ge 국소 응축 기술을 적용하여 채널 표면의 Ge 함량을 높인 SiGe 채널 터널링 전계효과 트랜지스터

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지도교수 박 병 국

이 논문을 공학박사 학위논문으로 제출함

2020년 2월

서울대학교 대학원

전기 컴퓨터 공학부

이 준 일

이준일의 공학박사 학위 논문을 인준함

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Abstract

Complementary metal oxide semiconductor (CMOS) technology has been a key technology for transforming lifestyles and expanding productivity and functionality. Currently, this technology has been evolving into extreme scales: nanoscale, in terms of device feature sizes. This development was possible because of the lithography technology. However, if electric field control is not performed as the device size decreases, undesirable short channel effect (SCE) will occur and the device will break down or standby power consumption will increase. In order to reduce the electric field in proportion to reducing the size of the device, scaling of the V_{DD} is required. But, there is a limit to downsizing voltage due to non-scaling factors such as threshold voltage (V_{TH}) of transistor. In situations where voltage scaling is not possible, increasing power consumption is a problem. Moving only threshold voltage V_{TH} near 0V will increase the off-current, and reducing V_{DD} with the V_{TH} fixed will lower the drive current. In order to solve this dilemma, performance improvement such as subthreshold swing (SS) is essential. MOSFETs (Metal oxide semiconductor field-effect transistors), in terms of SS, exhibit a fundamental limitation for the drain current increase per applied gate voltage difference. The tunnel field-effect transistor (TFET) provides the ability for beating this limitation. Current injection in TFETs relies on band-to-band tunneling

from the source contact to the channel cutting off the high energy tail of the Fermi distribution of carriers which causes the SS limitation in MOSFETs. Thus offering a performance advantage over MOSFETs for ultra-low V_{DD}. In this thesis, TFET which have surface Ge-rich SiGe nanowire as a channel has been demonstrated. Before the demonstration, validation was first performed using technology computer aided design (TCAD) simulation. Based on the simulation results of the TFET, a real device is fabricated. There are improvements in terms of on-current and SS comparing with control groups (constant Ge concentration SiGe TFET and Si TFET) fabricated by the same process flow except for the channel formation step. In order to obtain the concentration-graded SiGe channel, Ge condensation method which is a kind of oxidation is adopted. The rectangular shape of the channel becomes a rounded nanowire through the Ge condensation process. The TFET with the concentration-graded SiGe channel can improve drive current due to a smaller band gap at the Ge-condensed surface of the channel compared to Si or non-condensed SiGe channel TFET.

keywords: band to band tunneling, tunnel field-effect transistor, TFET, SiGe channel, Ge condensation, low-power device, subthreshold swing, current drivability

student number: 2013-20859

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Chapter 1

Introduction

1.1 Power Issues on CMOS Technologies

Semiconductor industries based on metal-oxide-semiconductor field-effect transistor (MOSFET) has been developed with Moore's Law. Moore's Law is a theory that the number of transistors in a dense integrated circuit (IC) doubles approximately every two years and it brings more features on chips and provides speed boosts. Thus, for decades, IC has been added to more transistors while reducing the size and cost of a chip. In recent years, the cause of the limitations of lithography technology shrink trend has not kept pace with Moore's law, but has continued to scale down using double patterning (or quadruple patterning) technology and extreme ultra-violet (EUV) lithography. It helps make smartphones, tablets, and desktop computers faster and

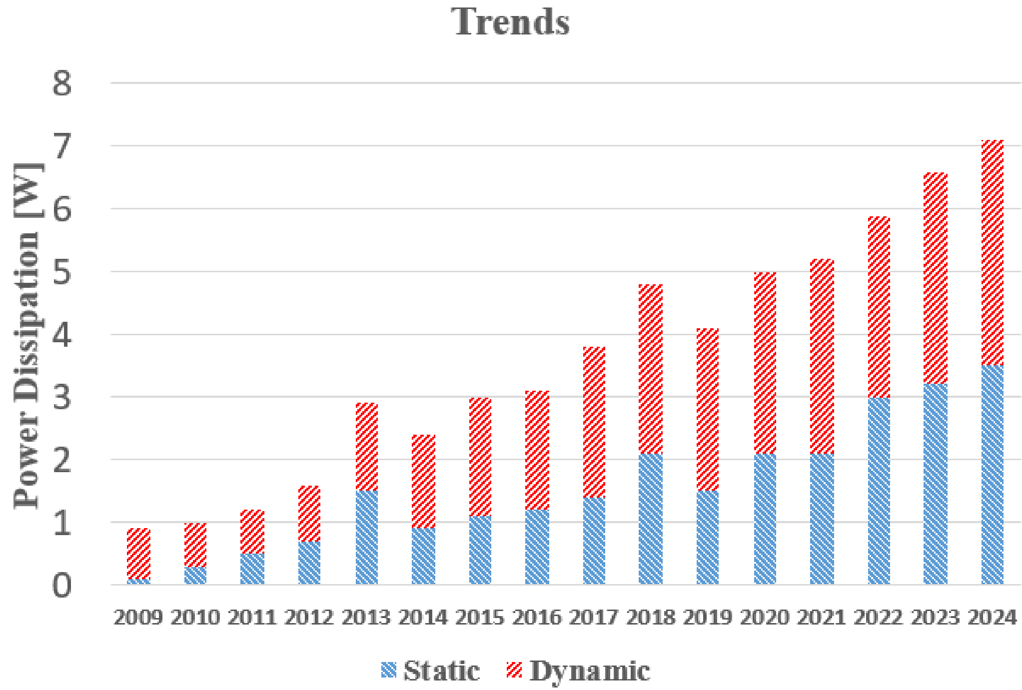


Figure 1.1: Power consumption trends and future forecasts.

more power-efficient. With the rise of mobile devices and the limitations of increased battery capacity, reducing power consumption has become a hot topic [1]-[4]. The following equation defines overall power consumption as the sum of dynamic and static power:

$$P = ACV_{DD}{}^{2}f + V_{DD}I_{OFF} \tag{1.1}$$

where A is the fraction of gates actively switching and C is the total capacitance load. The first term is the dynamic power lost from charging and discharging the load capacitors. The second term means the static power lost due to leakage current. As shown in Fig 1.1, as times evolve, power consumption is increasing every year. The distinctive

point is that in the past, dynamic power accounted for the majority of the total power consumption, whereas in recent years, the share of static power consumption has become equivalent to the dynamic power consumption. In the days of dynamic power consumption, it has been possible to reduce power consumption only by reducing the operating voltage (V_{DD}). However, as shown in eq. 1.1, static power consumption is not correlated with V_{DD} and is greatly affected by the leakage current (I_{OFF}) of the device itself. Most static leakages come from short-channel effects (SCEs) in MOSFETs such as threshold voltage (V_{TH}) roll-off, drain induced barrier lowering (DIBL), and punch-through, etc. To overcome this SCEs, the structure of the gate has been developed to surround the channel for effectively transfer gate potential to the channel [5]. However, this cannot be a fundamental solution beyond the basic limits of MOSFETs, which can not have a subthreshold swing (SS) of less than 60 mV/decade [6]. Given the constraints of SS, there are two options for reducing operating voltage. The first way is just shift the graph in Fig. 1.2 to the left. Since V_{DD} can be kept low while maintaining the overdrive voltage (V_{DD}-V_{TH}), there is no loss in terms of on current, but as shown in Fig. 1.2, off current is exponentially increased. I_{OFF} is proportional to exp(-qV_{TH}/mk_BT). The second way is lower V_{DD} only (without horizontal movement of the graph) while maintaining the off-state current. If the overdrive voltage is not secured enough, the device's drive current will be low, and low current will hinder AC

performance. This is confirmed by the increased gate delay as shown in Fig. 1.3 [8]. For each reason, neither option can be the correct way. Thus, in order to achieve high I_{ON}/I_{OFF} in a device with lower V_{DD}, it needs a new mechanism device, unlike MOSFET that operates by thermal carrier injection over the source-side potential barrier. Recently, various devices have been proposed, one of which is the tunnel field-effect transistor (TFET) as an alternative to low operating power devices [9]-[11].

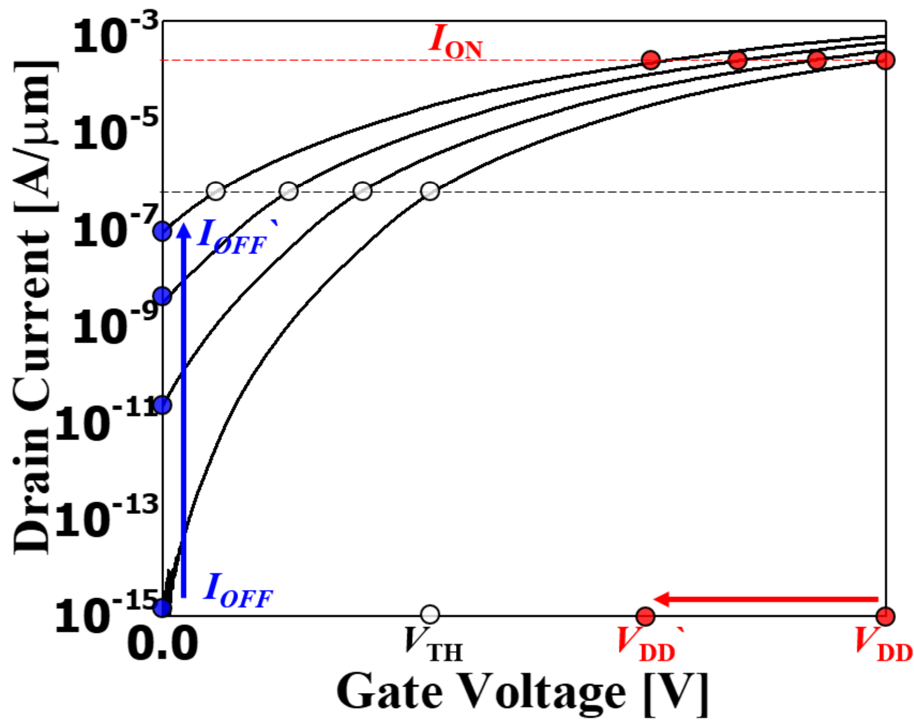


Figure 1.2: Transfer characteristics of MOSFET showing an exponential increase in I_{OFF} .

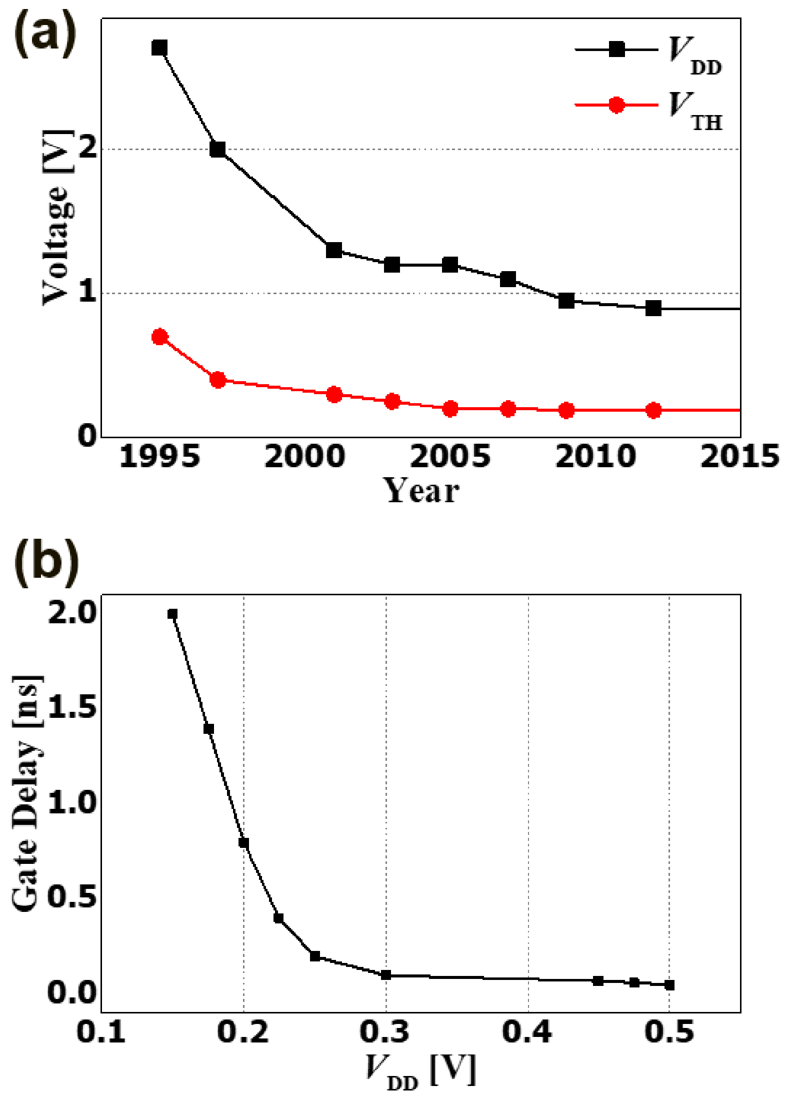


Figure 1.3: Scaling of CMOS (a) supply voltage and threshold voltage and (b) sub-threshold delay behavior.

1.2 Tunnel Field Effect Transistors and Requirements

In the previous section, the dilemma that couldn't solve the power consumption problem with the MOSFET, which has a fundamental limit that cannot have SS below 60 mV / dec is discussed. As can be seen in Fig. 1.4 (a), carriers that make up the MOSFET current is affected by temperature because it passes over the gate barrier through thermionic emission method in the source carrier. As shown in Fig. 1.4 (b), the TFET has a structure similar to the MOSFET, but has a structure in which the doping type of the source and the drain is reversed. As a result, the shape of the energy bands different from the energyband of MOSFET, and the method of injecting carriers from the source to the channel follows a completely different mechanism. The carrier injection mechanism in TFETs relies on band-to-band tunneling (BTBT) and this mechanism is known to be independent of temperature. Also, at small gate voltages (V_{GS}), the Fermi-tail part is cut from participating in the current drive, resulting in a small off current and (SS) [12],[13]. For these reasons, TFET has been regarded as promising energy-efficient switching devices because they can achieve (SS) below 60 mV/decade, which is the limit of conventional metal-oxide-semiconductor FETs (MOSFETs) at the room temperature. As you can see in Fig. 1.5, there is a possibility of getting closer to an ideal switch. As the transistor gets closer to the ideal switch, it allows V_{DD}-V_{TH} to be scaled down aggressively while maintaining high I_{ON}. When demanding high per-

formance while minimizing power consumption, the performance is better than using CMOS with MOSFET [14].

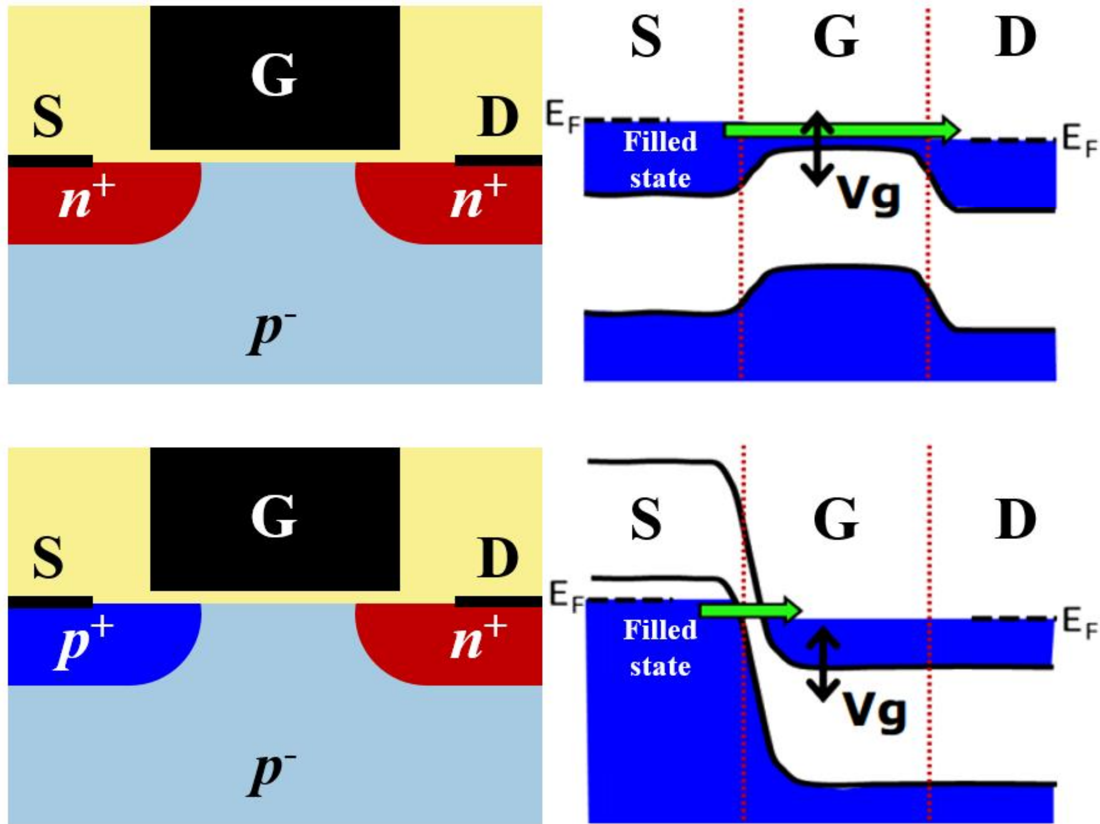


Figure 1.4: (a) Schematic cross-sectional view and its energy band diagram when on state (a) MOSFET and (b) TFET.

1.3 Issues for TFETs

Although TFETs have the advantage of being able to switch on and off quickly with low off-current and low SS values, despite extensive research, they have not completely replaced the MOSFET. One common problem with experimentally verified

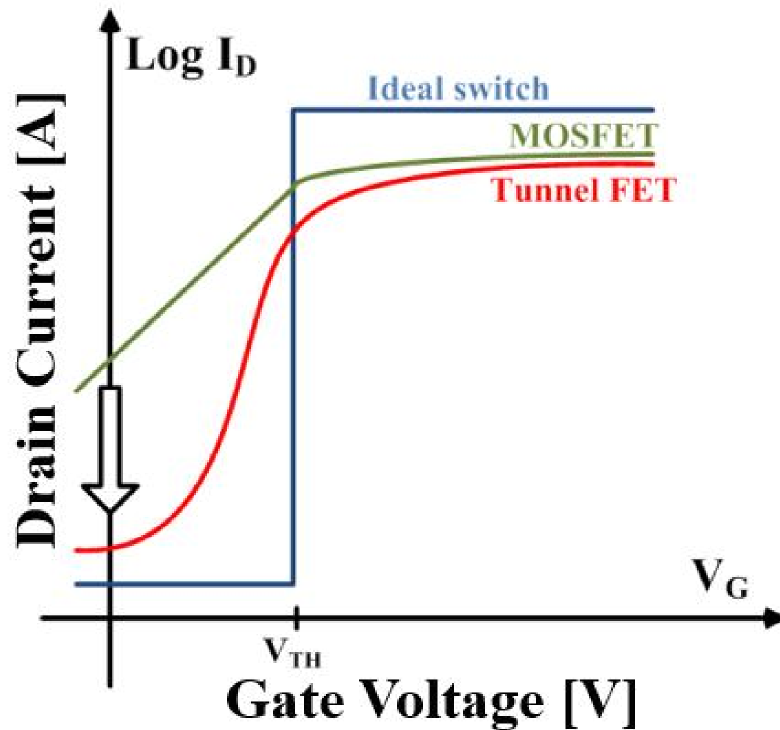


Figure 1.5: Switching properties of Ideal switch, MOSFET and TFET.

TFETs is low drive current. Additionally, there is the possibility of unintended tunneling currents, called ambipolar current, generating between the drain and the channel, not between the source and the channel. In this case, there exists a possibility that the electric current which flows in reverse in the off state will become large again. In order to solve these problems and approach the ideal switch beyond the MOSFET, the TFET requires the following efforts.

1) Channel wrapping gate structure and low EOT

2) Reducing ambipolar current

3) Narrow bandgap materials

First, the structural evolution of CMOS using MOSFETs is also required in CMOS using TFETs, and in TFETs, it is important to have a structure surrounding the channel, such as a finFET or gate all-round structure, in order to increase the channel influence of the gate. There is a need for gate dielectric materials with low EOT for the same purpose. If a small gate voltage can move energy bands widely, the energy barrier seen from the source becomes thinner, increasing the probability that the carriers will tunnel through. Improving the ability to control many gate-side bands even with small voltage changes is the key to making TFET. The second factor to solve is the ambipolar current. As mentioned earlier, this is an unintended tunneling current flowing between the drain and the channel, which causes the transistor to turn on without turning off in the off state, as shown in Fig. 1.6. It is possible to reduce the ambipolar current by placing an underlap region between the channel and the drain or by making the gradual doping between the drain and the channel [15], [16].

Since the TFET utilizes band to band tunneling, the current increases as the width of the tunnel barrier seen by the carrier become shorter. In addition to structurally increasing the effect of the gate on the channel, changing the material can also help. It has been reported that tunneling rate of carriers from source to channel is inversely proportional to the band gap of channel materials [17]. Therefore, materials having a small band gap are preferred to increase the current of TFET. In recent years, extensive

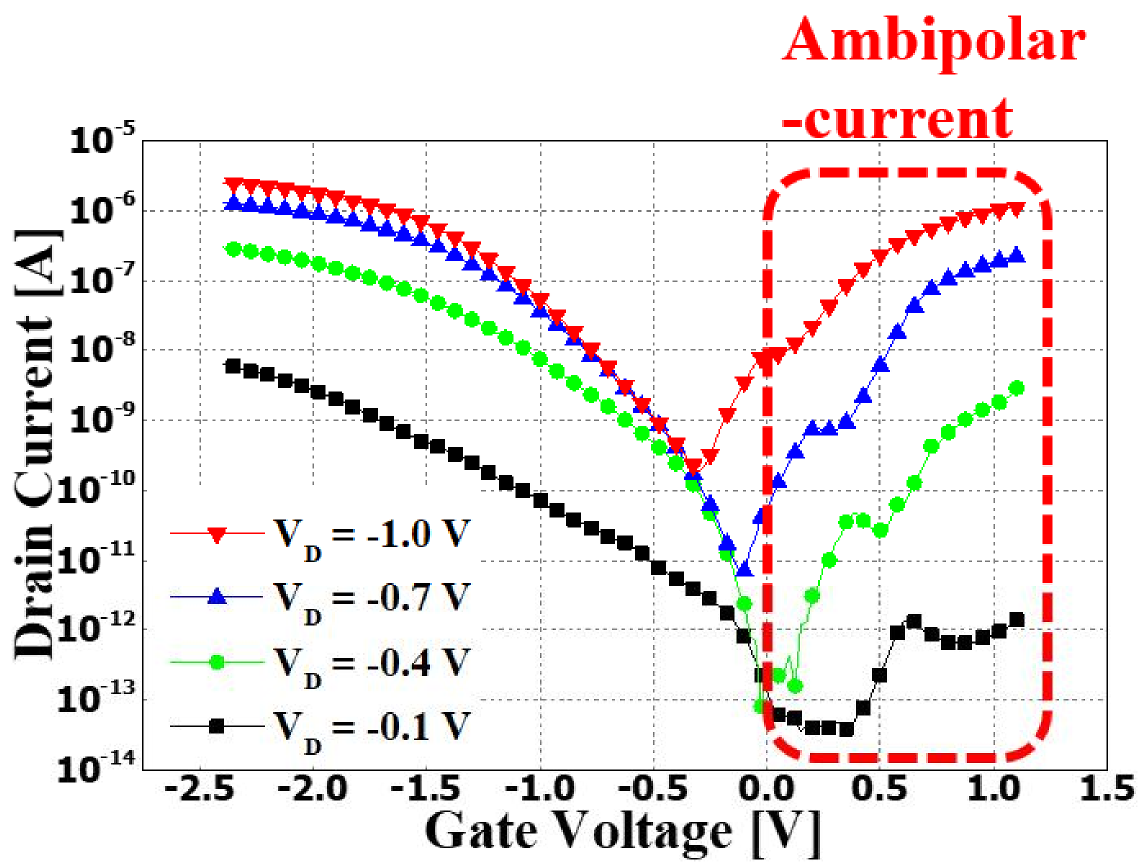


Figure 1.6: Transfer characteristics of fabricated p-type TFET device with ambipolar current.

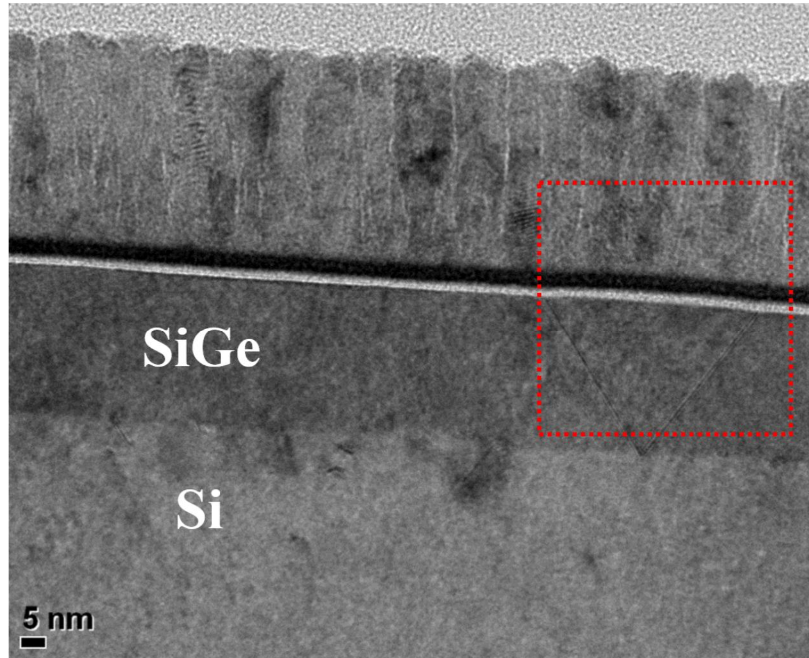
research has been conducted to improve on-current. Various materials have been studied to reduce the width and height of tunnel barriers [18]-[20]. Generally, Si-TFETs exhibit low on-current due to large band gap. In order to overcome large tunneling barrier, SiGe, which has a smaller band gap than that of Si, is a good alternative. In addition, SiGe is complementary MOS (CMOS) compatible because it is a group IV material [21]. When stacking other materials on the silicon substrate to serve as channel material, the lattice constant must be considered. Ge or SiGe, which have a smaller band gap than Si, are also preferred because they can increase the operating current. But, there is a trade-off especially in terms of process capability due to the crystal lattice mismatch with the Si substrate which increases the defect concentration on the channel surface. Figure 1.7 (a) and (b) show dislocation lines starting from interface between Si substrate and SiGe channel. These lines act as trap sites on the surface and degrade the mobility of carriers when current flows through the SiGe channel. To reduce the threading dislocation density caused by the lattice mismatch, some studies have been conducted to form a trap-less channel with thick lattice matched-buffer layer [22, 23]. However, there are two problems with the thick buffer layer. First, in terms of the fabrication of a transistor, additional works are required to block the leakage path to the buffer layer. For example, it needs additional blanket stacks (SiGe/Ge/SiGe) to match the lattice constant with virtual substrate [24], which is not suitable for modern

CMOS which requires a thin body. Also, the thick body requires additional ground-plane doping to suppress body leakage. When a TFET is fabricated, it is necessary to reduce the body leakage in the subthreshold region to obtain a low subthreshold swing (SS) [25]. Second, when the thicker crystal layer is grown, the cost increases in proportion to the thickness.

1.4 Scope of Thesis

The purpose of this dissertation is to improve the performance of the TFETs, and the main targets are improved current and low SS values. In order to ensure the suitability of the simulation, extracting the appropriate model parameters is preceded, and then, the performance of the TFETs made with the proposed structure is predicted. Then the proposed TFETs have been verified with measured results. Chapter 2 shows the device to be fabricated. Before verifying this, the task of determining the suitability by simulation is preceded. In order to increase the accuracy to predict device performance of the simulation tool, the process of extracting the parameters to be used for the BTBT model from the reference device is performed first. After that, the features of the proposed structure and the simulation results are shown. The structure of the device to overcome the problems presented in the section 'Issue for TFET' is presented and shows the process of verification by simulation. In Chapter 3, an introduction to the

(a)



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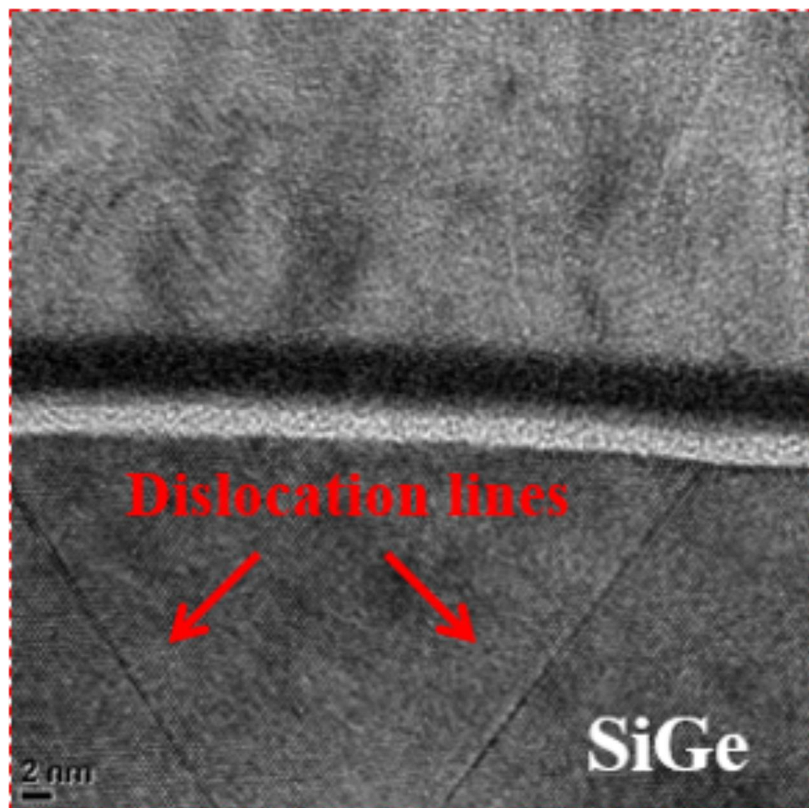


Figure 1.7: (a) SiGe epitaxial growth result on Si substrate and its (b) magnified image inside red dotted line. Threading dislocation lines found at the channel surface of SiGe due to different lattice constants with Si.

process of making a device is presented. There are an introduction and description of the entire process, and the key processes, such as Ge condensation technology, nano-wire formation, asymmetric source and drain formation, and metal gate processes, are discussed in more detail in the subsection. There will be a comparison of the electrical performance of the proposed and control devices in chapter 4. The operation of the hy-brid inverter with the proposed device and MOSFET also be confirmed. Finally, works will be concluded with a summary and suggestions for future work.

Chapter 2

Ge Condensed SiGe Channel TFET

2.1 Extraction model parameters for simulation

Before introducing the device to be proposed, the model and parameter used in the simulation tool should be verified. The fitting measured and simulated data of the device, which was manufactured for the previous study[26], is performed first. The structure of the device fabricated before is shown in the Fig. 2.1. All the fabricated TFETs have the planar structure. The control group, Fig. 2.1 (a), of Si TFET is fabricated on a (100) p-type silicon-on-insulator (SOI) wafer with 100 nm thick Si on top of 375 nm buried oxide. The experimental group, Fig. 2.1 (b), of SiGe TFET is also fabricated on the same type of wafer with 60-nm-thick Si. By using Epsilon 2000, SiGe with Ge content of 30% and a thickness of 40 nm is epitaxially-grown. Then, to reduce defects at the

interface between the gate stack and SiGe channel, the Si capping layer is grown on the SiGe channel. the total thickness of channel materials is about 100 nm. The gate stack consists of 200 nm polycrystalline-silicon layer and 3-nm-thick SiO_2. After gate patterning, asymmetric doping is performed to make TFET. After measuring the transfer characteristics of the fabricated devices, the tunneling model is firstly calibrated to experimental data for the fabricated planar Si and SiGe TFETs. Then, TCAD simulations are performed. It is especially suitable for accurate tunneling current calculation because it automatically defines the tunneling path and the mesh on the basis of the valence band gradient [27]-[29]. Also, it completely gets rid of the uncertainty of the current calculations due to the inappropriate assumption of the tunneling direction. In the simulations, Fermi statistics is assumed, the gate leakage current is ignored, and the bandgap narrowing model is applied since source and drain region are doped heavily. Additionally, Shockley-Read-Hall (SRH) recombination with electric field (e-field) dependence, nonlocal BTBT, and drift-diffusion carrier transport models are used.

Figures 2.2 show the comparisons between measured and simulated transfer characteristics. All the transfer characteristics are extracted at V_{DS} of 0.1 V in n-type Si and SiGe TFETs. In the simulations, to calculate the BTBT generation rate (G) per unit volume in the uniform electric field, Kane's model is used and fitted parameters are as follows (Eq. (2.1)).

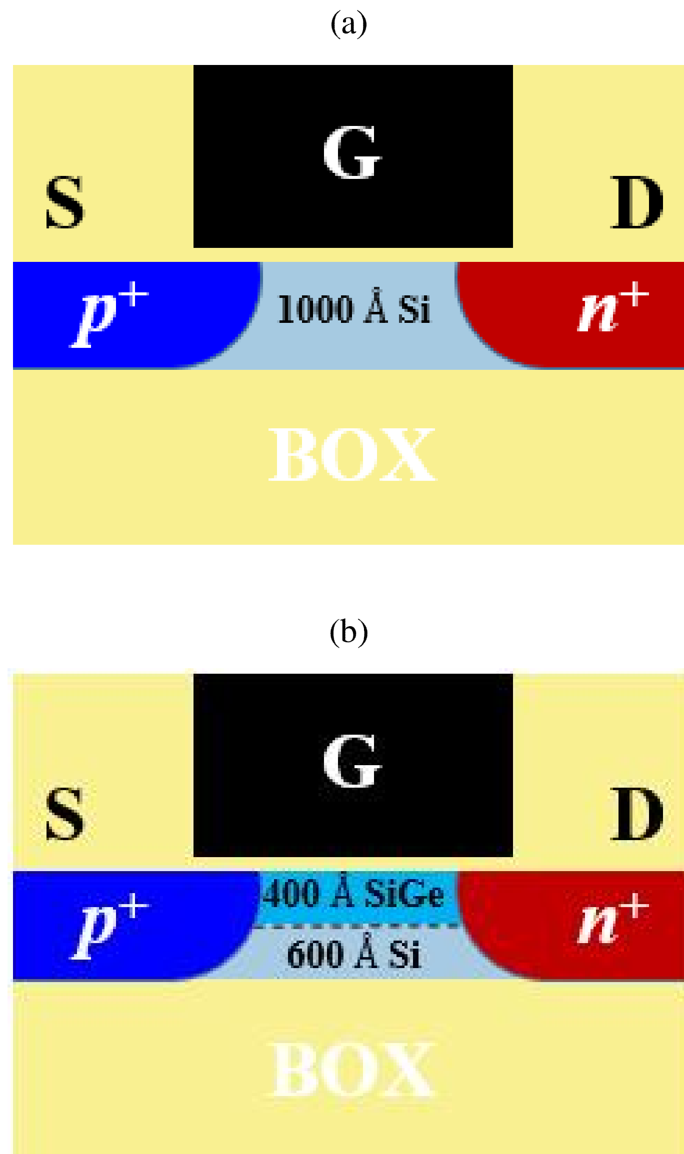
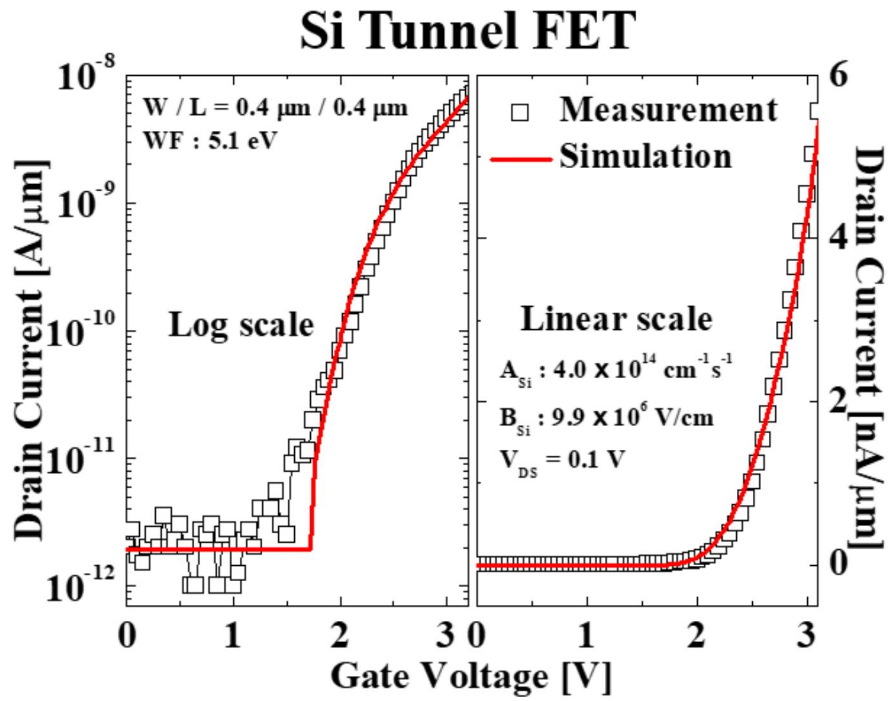


Figure 2.1: Cross-sectional views of fabricated and simulated (a) Si TFET and (b) SiGe TFET [26].

(a)



(b)

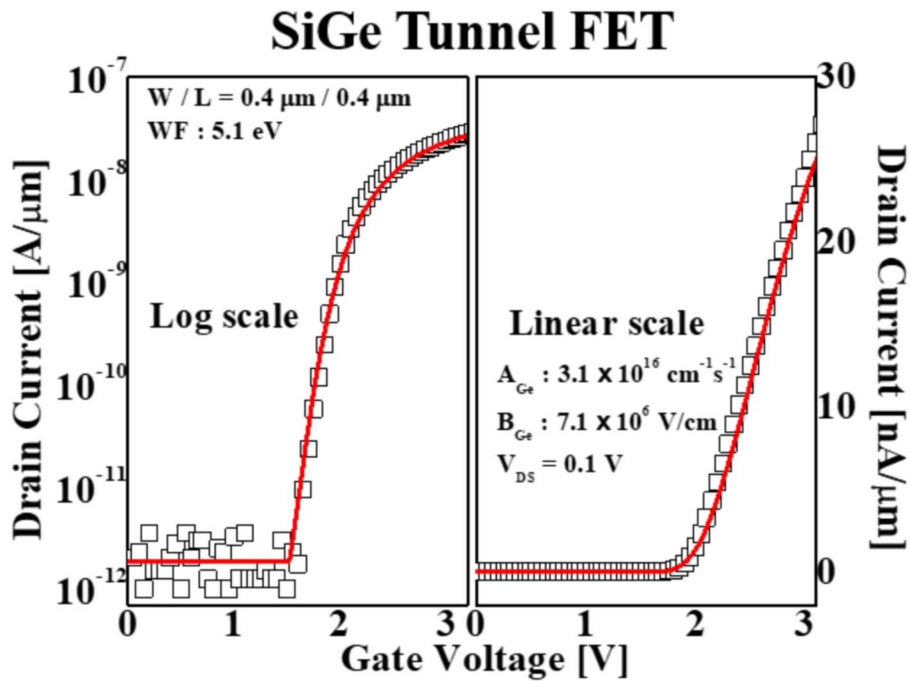


Figure 2.2: Calibrated transfer characteristics from simulation and measurement results for (a) Si and (b) SiGe TFETs.

$$G = A(\frac{F}{F_0})^P exp(-\frac{B}{F}) \quad (2.1)$$

where F_0 = 1 V/m, P = 2.5 for indirect BTBT. Prefactor A and exponential factor B are the Kane parameters and F is the electric field. Both linear and log scale simulated transfer characteristics are well matched to experimental data when using parameter values in the table 2.1 and table 2.2. In all subsequent simulations, these parameters are used for accurate analysis.

Table 2.1: Calibrated Kane's parameters for Si

Parameter	Si	Unit
A	4×10^{14}	cm$^{-1}s^{-1}$
B	9×10^{6}	V/cm

Table 2.2: Calibrated Kane's parameters for SiGe

Parameter	SiGe	Unit
A	3×10^{16}	cm$^{-1}s^{-1}$
B	7×10^{5}	V/cm

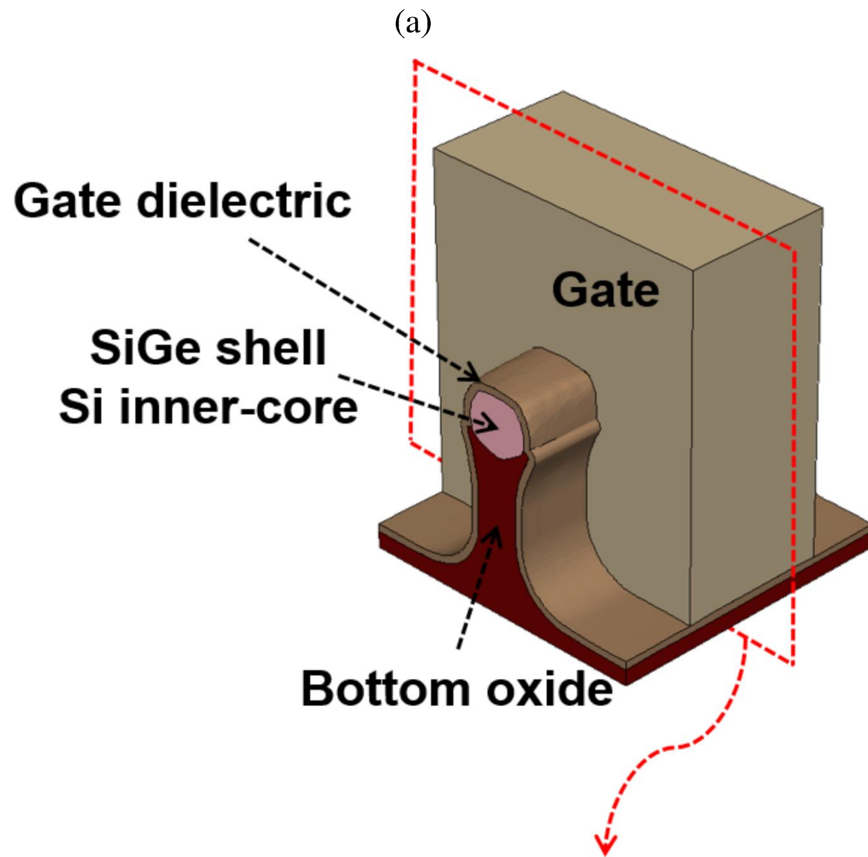
2.2 Features of Ge Condensed SiGe Channel TFET

The structure of the proposed device is shown in Fig. 2.3 (a). The cross-section of the channel after two-step oxidations (rounding oxidation Ge condensation) is shown in Fig. 2.3 (b). The core part (bright part in the figure) is pure Si, but it can be seen that the portion surrounding the core (dark part of the figure) is SiGe and the Ge content increases to 45% with increasing distance from the core. The control devices utilize a channel with a constant Ge content and a channel consisting only of Si, not a shell on the core structure.

2.3 Design Verification with TCAD Simulation

In order to confirm the electrical performance of the surface Ge-rich TFET and the controls (constant Ge content $Si_{0.8}Ge_{0.2}$ TFET and Si TFET), the TCAD simulation is performed using Synopsys Sentaurus. Figures 2.4 (a)-(c) show the two-dimensional (2D) cross-sectional structures of the simulated TFETs. The content of Ge used in the simulation for each group is shown in Fig. 2.5 (It will be described later, the Ge content used in the simulations is based on unit experiment results). The physical parameters of the TFETs used for the simulations are shown in table 2.3. The cylindrical model is applied to simulate the structure in which the gate surrounds the channel. Figure 2.7 and its inset show the energy band diagrams and Fig. 2.7 depicts BTBT

(a)



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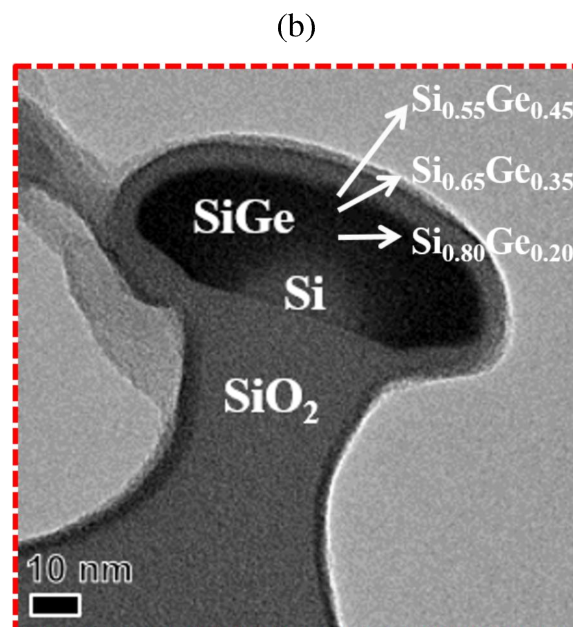


Figure 2.3: (a) Schematic diagrams of proposed surface Ge rich SiGe channel TFET, and (b) HR cross-sectional TEM images in perpendicular to channel directions.

generation rates when the device is turned on [V_{GS} = -1 V, drain voltage (V_{DS}) = -1 V], respectively. The tunnel barrier width (W_T) seen by the carrier on the source side of the experimental group is reduced compared to the control groups. This is because the bandgap of the material becomes smaller as the content of Ge increases. As W_T decreases, the probability that the carrier goes through from the source to the channel exponentially increases [7], so that the drive current can be expected to increase. Actually, the amount of electrons generated in the same structure on the simulation is 4.27×10^{30} cm^{-3}/s, which is larger than 6.71×10^{29} cm^{-3}/s and 1.63×10^{29} cm^{-3}/s of the control groups. The DC characteristics of the proposed TFET are compared to those of the SiGe-channel TFET without Ge condensation and the Si-channel TFET. Figure 2.8 demonstrates that the proposed TFET has enhanced Ion and steeper SS although there is a small amount of I_{OFF} increase. In the case of TFETs which has a fatal disadvantage of low driving current, the small increase of I_{OFF} is acceptable if the driving current and SS can be enhanced at the same time because I_{OFF} can be reduced by adjusting the gradual drain doping. The enhanced Ion and steeper SS result from the reduction of bandgap with the help of Ge condensation since the tunneling is predominantly generated near the channel surface in TFETs. Figures 2.10 (a)–(c) show that the number of the generated tunneling carriers increases as the Ge concentration near the channel becomes higher.

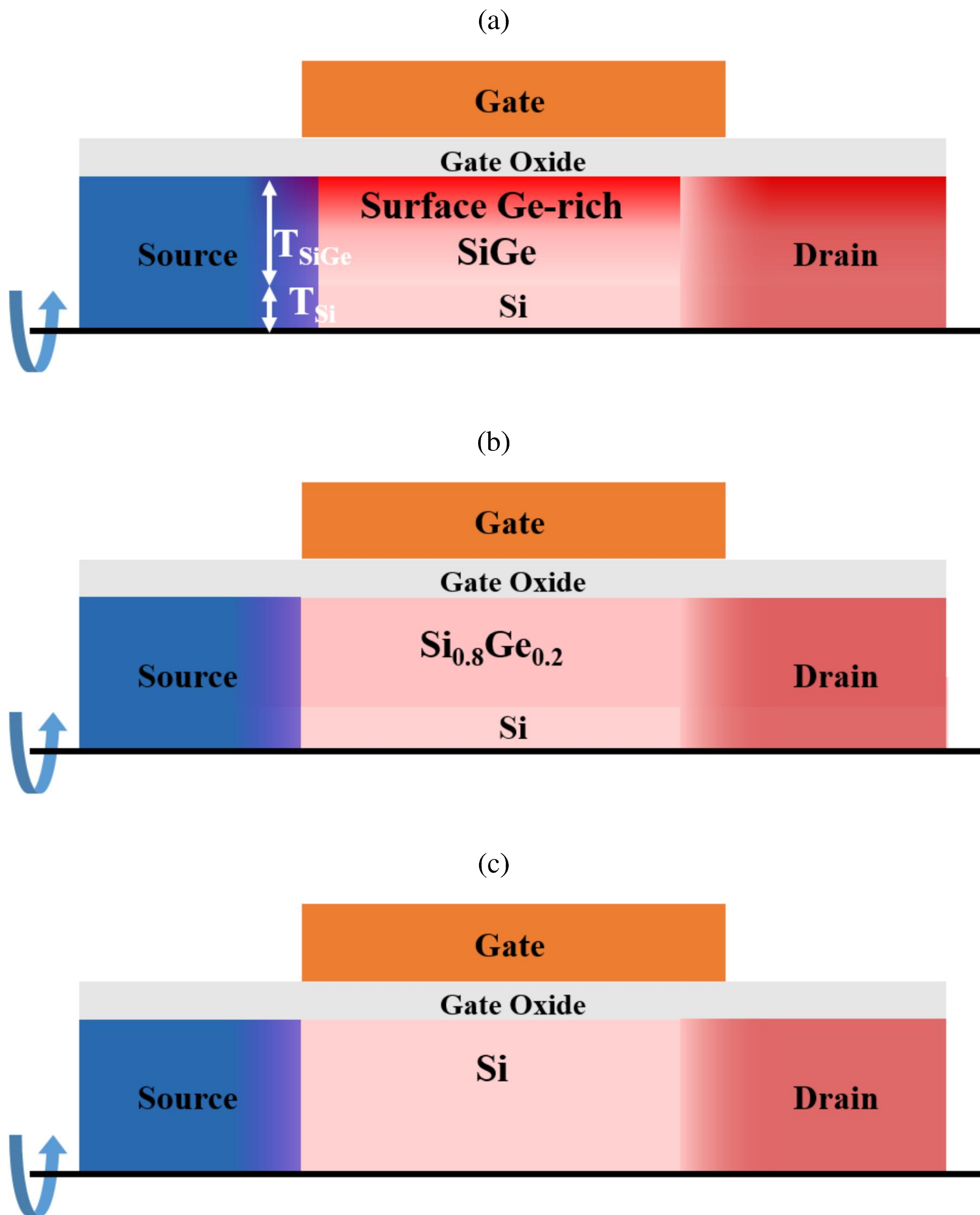


Figure 2.4: Simulated TFET structures. (a) surface Ge-rich SiGe TFET, (b) constant Ge concentration SiGe TFET, and (c) Si TFET. (The structure is drawn in 2D, and then rotated around the bottom of the Si substrate to form a nanowire structure.

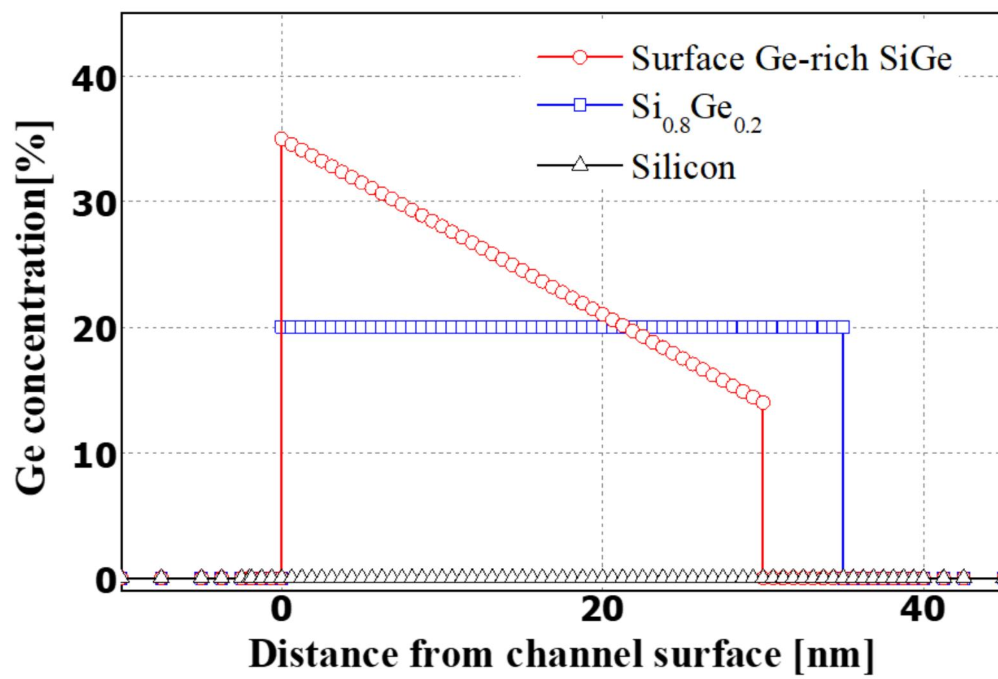


Figure 2.5: Ge contents utilized in simulation.

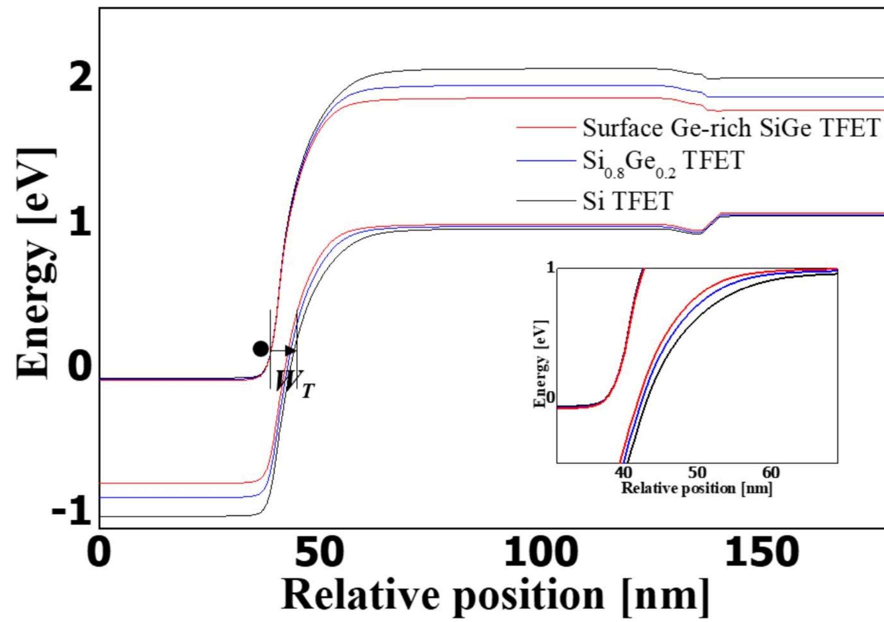


Figure 2.6: Energy band diagrams of pTFEs at turn on state (V_{GS} and V_{DS} = -1 V).

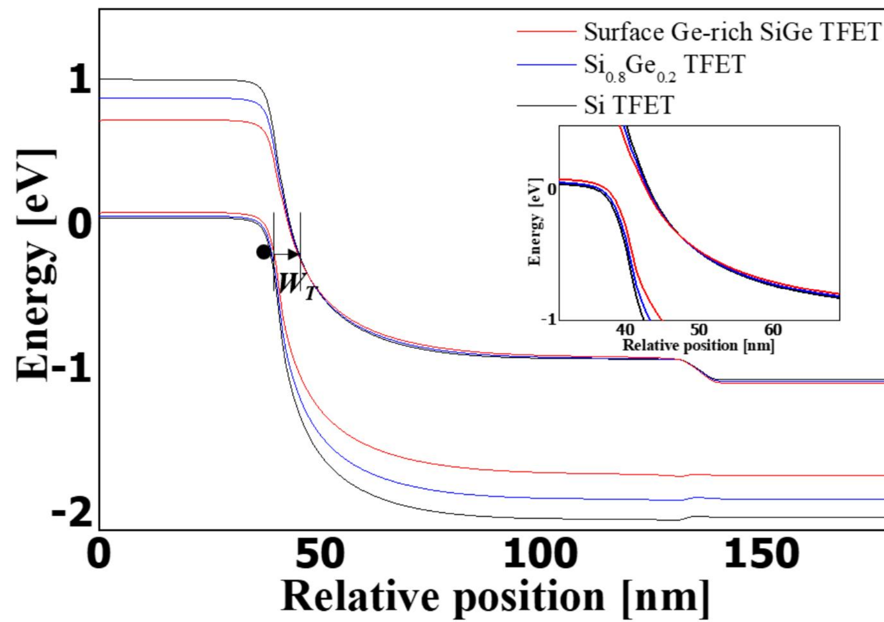


Figure 2.7: Energy band diagrams of nTFETs at turn on state (V_{GS} and V_{DS} = +1 V).

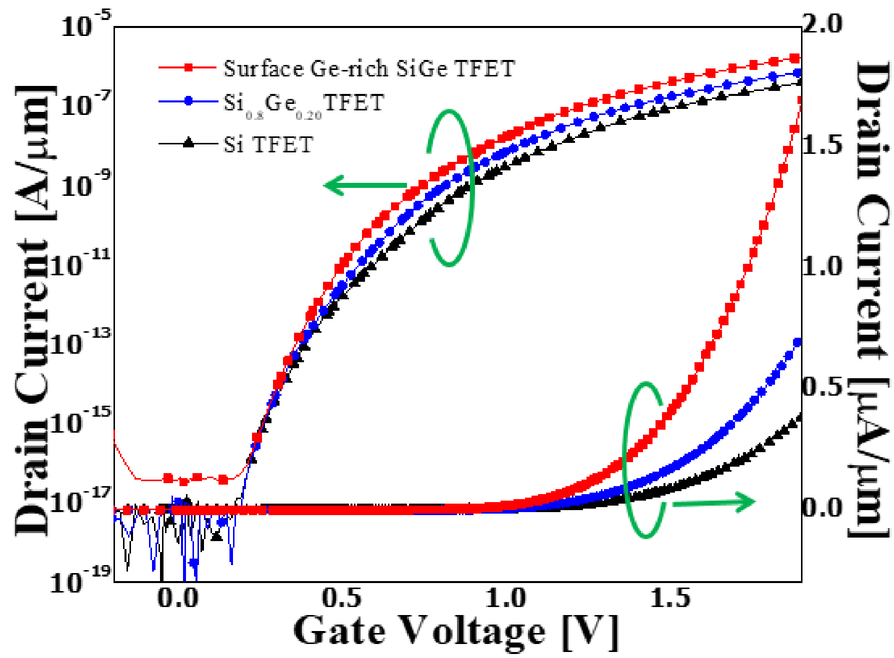


Figure 2.8: Comparison of simulated transfer characteristics of nTFETs V_{DS} =1 V.

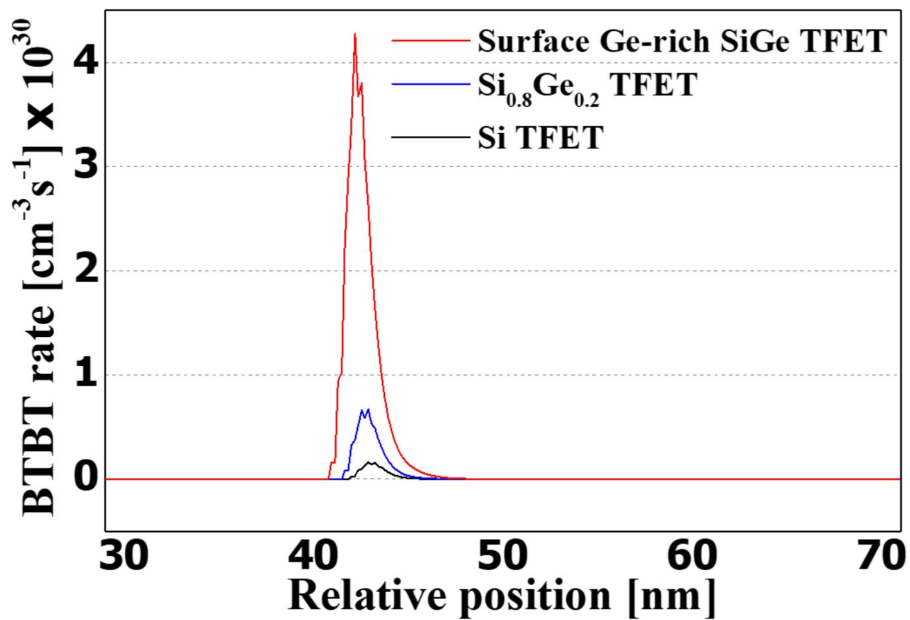


Figure 2.9: Comparison of electron band to band generation rate at turn on state (V_{GS} and V_{DS} = -1 V).

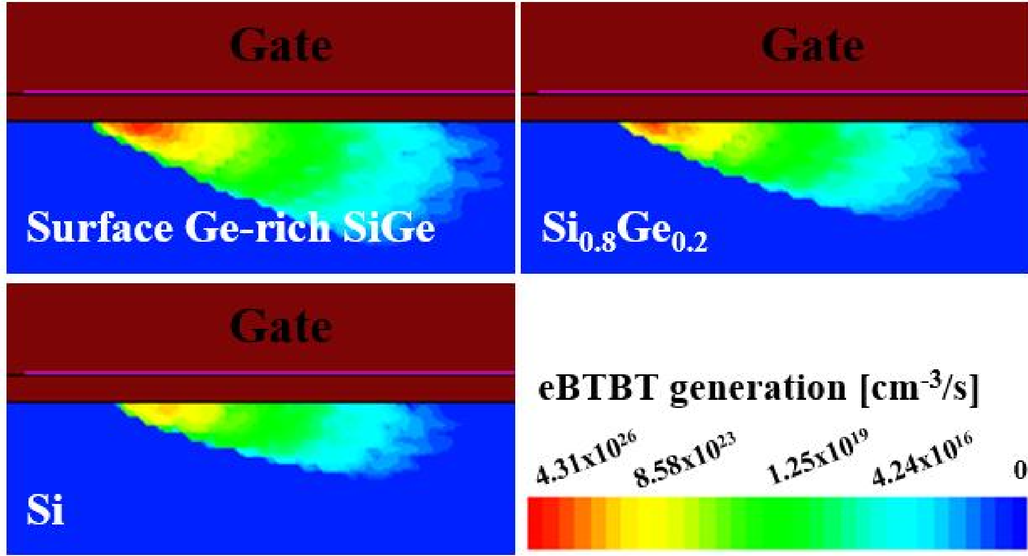


Figure 2.10: 2D contour of electron band to band generation rate with turn on state at the channel surface (V_{GS} and V_{DS} = -1 V).

Table 2.3: The physical parameters of the TFETs used for the simulations

Parameter	Value
L_{gate}	100 nm
EOT	1.7 nm
T_{SiGe}	30 nm
T_{Si}	10 nm
N_{Source}	$1\times10^{20}\ cm^{-3}$
N_{Drain}	$1\times10^{19}\ cm^{-3}$
N_{Body}	$1\times10^{16}\ cm^{-3}$

Chapter 3

Device Fabrication

In this chapter, process flows are firstly explained for device fabrication. Also, the key unit process among process flows describes in detail. Next, the electrical characteristics of fabricated devices are investigated with control groups.

3.1 Whole Process Procedure

The actual experiments are performed in the order shown in Fig. 3.1, and unit tests are conducted for some important steps such as active formation step and Ge condensation step. The process of forming the active channel at the front-end of the line (FEOL) is very important. The experiment is divided into one experimental group and two control groups (total of three groups), and then the middle-end of the line (MEOL) and back-end of the line (BEOL) steps follow the same flow. Diagrams containing the

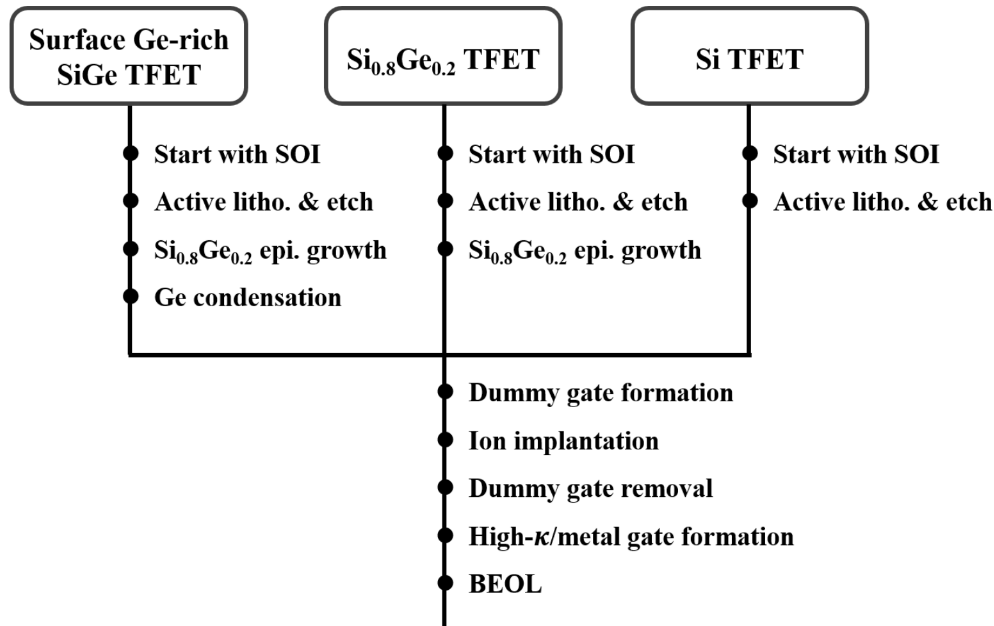
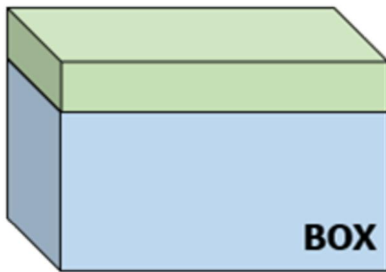


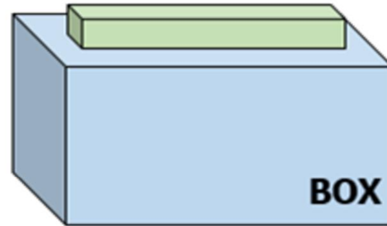
Figure 3.1: Process sequence in this work.

whole process flow are shown in Fig 3.2. After showing the overall flow, key processes will be covered further in the subsection. First, devices are fabricated on the full 6 in sized Si-on-insulator (SOI) substrate. Si dioxide (SiO_2) used as a buried oxide layer has 375 nm thickness while silicon as a substrate is 60 nm thickness (Fig. 3.2 a). Combine lithography and etching to form a frame part that will become a core of active channel (Fig. 3.2 b). The Si TFET, which will be used as a control, is stopped at this stage, and the other two groups cover an additional 30 nm of SiGe with 20% Ge content. (Fig. 3.2 c). After that, Ge condensation is applied to the experimental group to increase the surface Ge content (Fig. 3.2 d). After processes that follow are the same for all three groups and forming a dummy gate process (photolithography & etch)

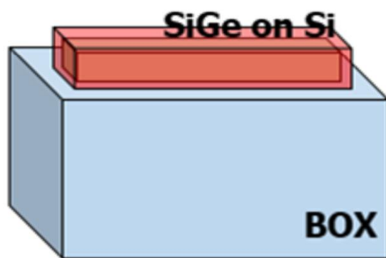
is followed. The dummy gate material is used by sequentially deposited poly-Si and Silicon-nitride (SiN), (Fig. 3.2 e), Then ion implantation is performed on the source and drain. In the case of TFETs, n- and p-type TFETs have different doping types, and in this experiment, drain doping concentration is set lower than the source concentration, so the ion implantation process is performed a total of four times. In detail, annealing is performed immediately after the drain implant and source formation (ion implantation & annealing) is performed later (The related content will be covered in detail in a subsequent subsection) (Fig. 3.2 f). Inter-layer dielectric (ILD) is deposited 3.2 g), followed by chemical-mechanical polishing (CMP) (Fig. 3.2 h). After the CMP process, SiN wet etch and poly-Si dry etch are applied to the dummy gate material to reveal the channel material3.2 i). The SiO_2 formed during the Ge condensation, which has been previously performed, has a high selectivity to poly-Si etch, thus resisting dry etch. Finally, the SiGe is exposed when the SiO_2 is removed by dilute hydrofluoric acid (dHF). The process is completed by working with high-κ metal-gate (HKMG) formation and wiring the contact pad. (Fig. 3.2 j $\sim$ l).



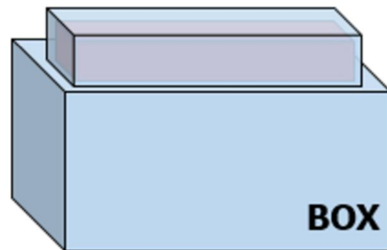
(a) Start from SOI



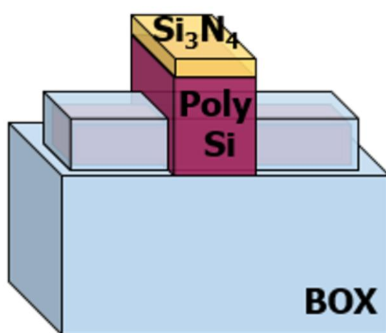
(b) Active litho. & etch



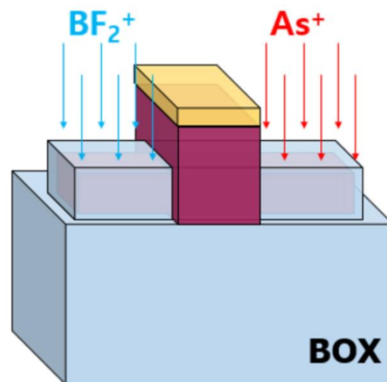
(c) SiGe epi. growth



(d) Ge condensation



(e) Dummy gate formation



(f) S/D implantation

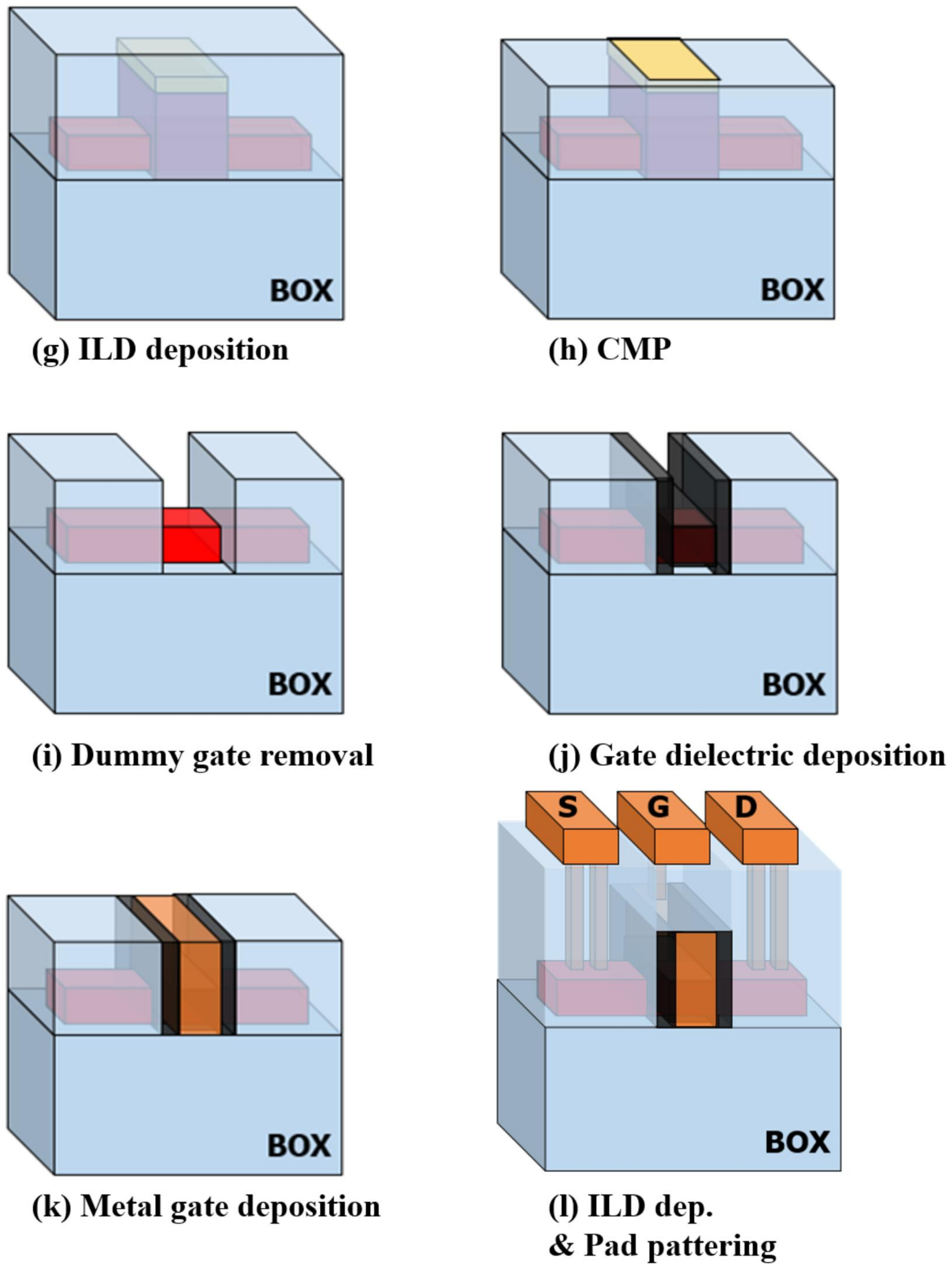


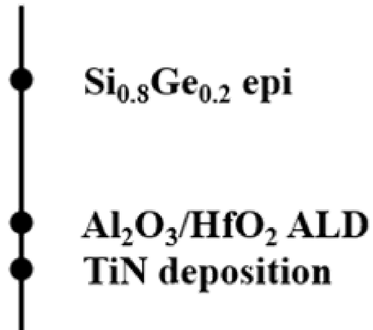
Figure 3.2: (a)∼(i) Fabrication flow of the proposed tunnel FET. The first control group ($Si_0.80Ge_0.2$ TFET) does not perform step (d) and the second control group (Si TFET) does not perform step (c), (d).

3.2 Key Processes

3.2.1 Ge Condensation

Simulation results showed that using Ge-rich SiGe channels to improve the performance of the TFET gave better results in terms of on-current and swing than using Si or SiGe channels with low Ge content. It has been also confirmed in 1.7 that it is impossible to directly grow SiGe channels having a high content of Ge. The solution can be to epitaxially SiGe with low Ge content so that dislocation does not occur due to the lattice constant difference, and increase the Ge content near the surface through subsequent heat treatment. For this purpose, a unit process experiment is conducted and the flow is shown in Fig. 3.3. On the basis of the results of this unit experiment, the same Energy-dispersive x-ray spectroscopy (EDS) is confirmed in the actual fabricated device, and as a result, the Ge content of the surface is increased as expected (Fig. 3.5).

(a)



(b)

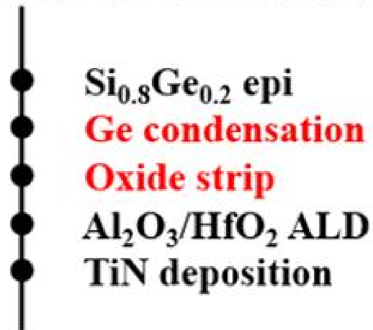


Figure 3.3: Unit experiment flow to verify condensation effect (a) without condensation and (b) with condensation.

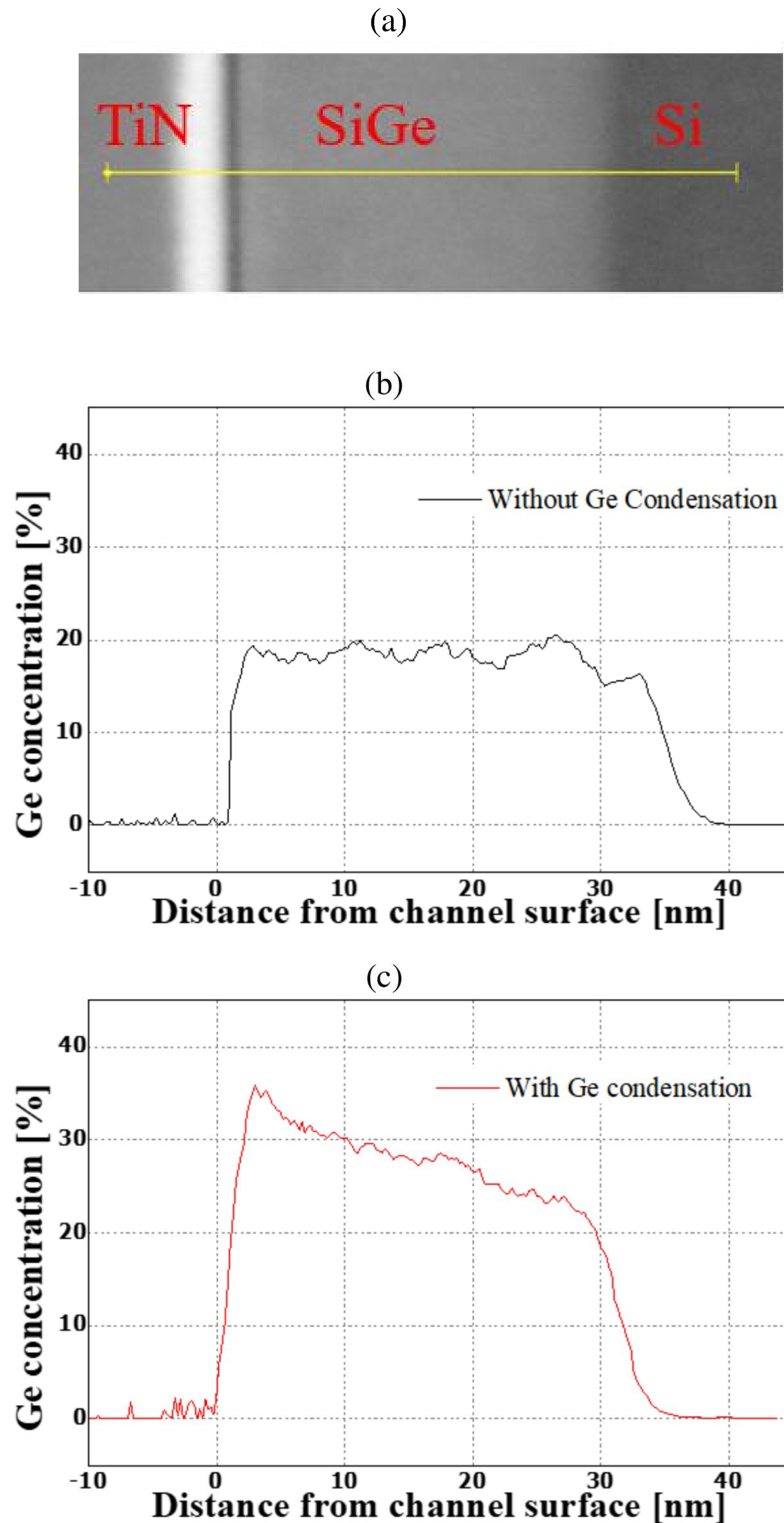
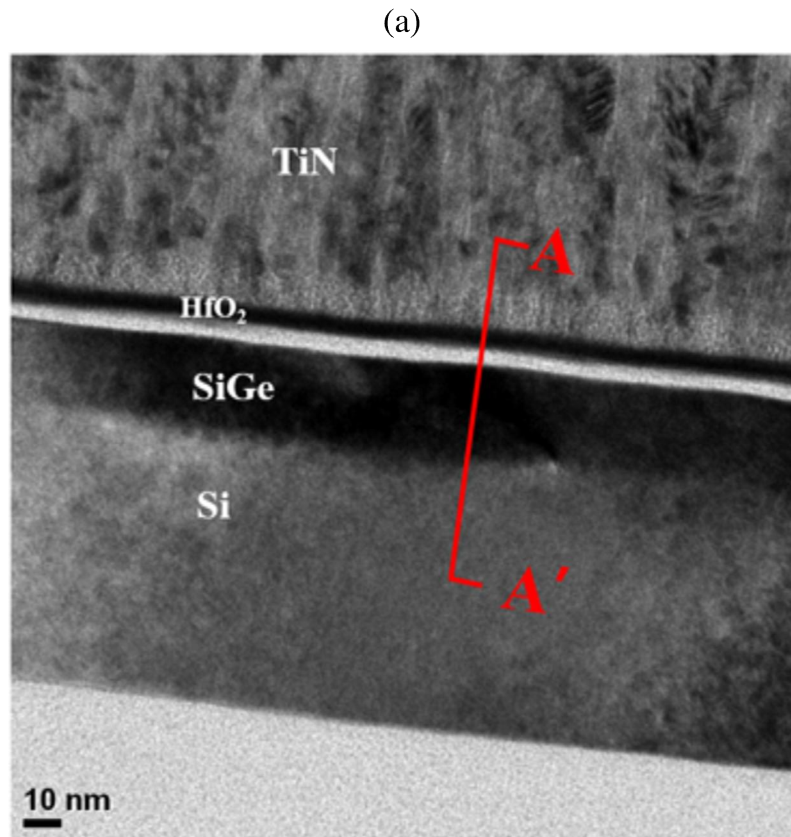


Figure 3.4: (a) Position of the device used to measure EDS. EDS profiles of (b) SiGe with constant Ge content and (c) surface Ge-rich SiGe.

(a)



(b)

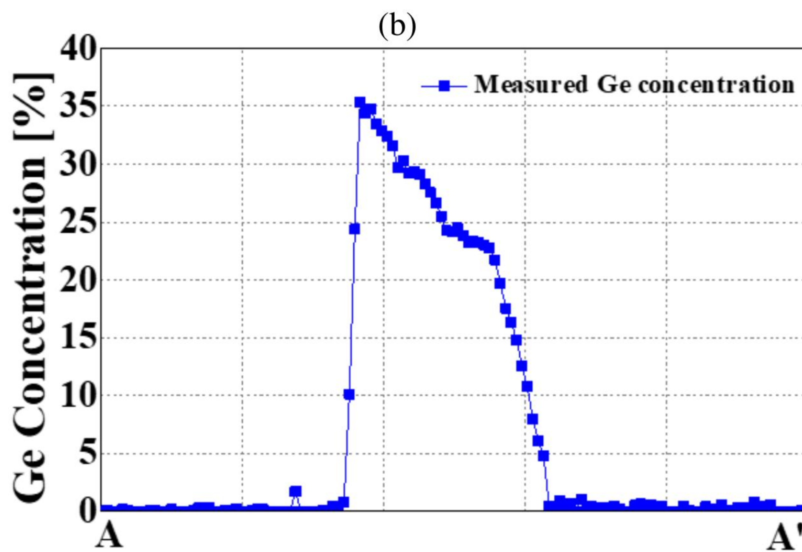


Figure 3.5: (a) TEM of fabricated device, EDS measured along line A-A'. (b)Ge concentration of the SiGe channel measured by EDS.

3.2.2 Channel Formation

Earlier Fig. 3.2 (b) process is simply described as 'photolithography etching', but in fact, this process has been done through some complicated procedures, as can be seen in Fig. 3.6. A two-step oxidation method is used to make a nanowire with graded Ge concentration. After the active region with the narrow fin is formed by electron beam lithography [Fig. 3.6 (a)], a first oxidation is performed to round the channel [Fig. 3.6 (b)]. The edges of a rectangular channel are rounded because the oxidation speed of the edges is faster than a flat surface. Si atoms in the corner are more prone to encounter oxygen molecules, so the oxidation speed is faster at the corner. The temperature and time of the first oxidation process should be appropriately selected. Otherwise, the rounded shape may not be formed or the Si may be exhausted during the oxidation. Before the actual experiment, process simulations are preceded, it is confirmed that round channels are formed with the appropriate temperature and time oxidization as shown in Fig. 3.7. Figure 3.7 (a) is Si with a width and height of 90 and 70 nm on the SOI substrate before the first oxidation. As can be seen in Figures 3.7 (b) and (c), the thickness of SiO_2 film is most affected by temperature and time. By adjusting both conditions well, it is possible to form a rounded-channel. After the first oxidation, the oxide layer which is formed by the first oxidation process is removed [Fig. 3.6 (c)]. Then, the epitaxial growth of 30-nm thick SiGe layer with 20% Ge concentration

is carried out [Fig. 3.6 (d)]. The second oxidation process, called Ge condensation, is conducted [Fig. 3.6 (e)] (Verification of Ge condensation has been completed in the previous section.) Here, the temperature at which the oxidation rate of Si is higher than that of Ge should be selected. When the Si atoms in the SiGe are selectively oxidized, in reduced volume, the amount of Ge atom is preserved, leaving SiGe with increased Ge content. This Ge condensation is experimentally proved by 30 min. oxidation under an oxygen atmosphere at 950 °C.

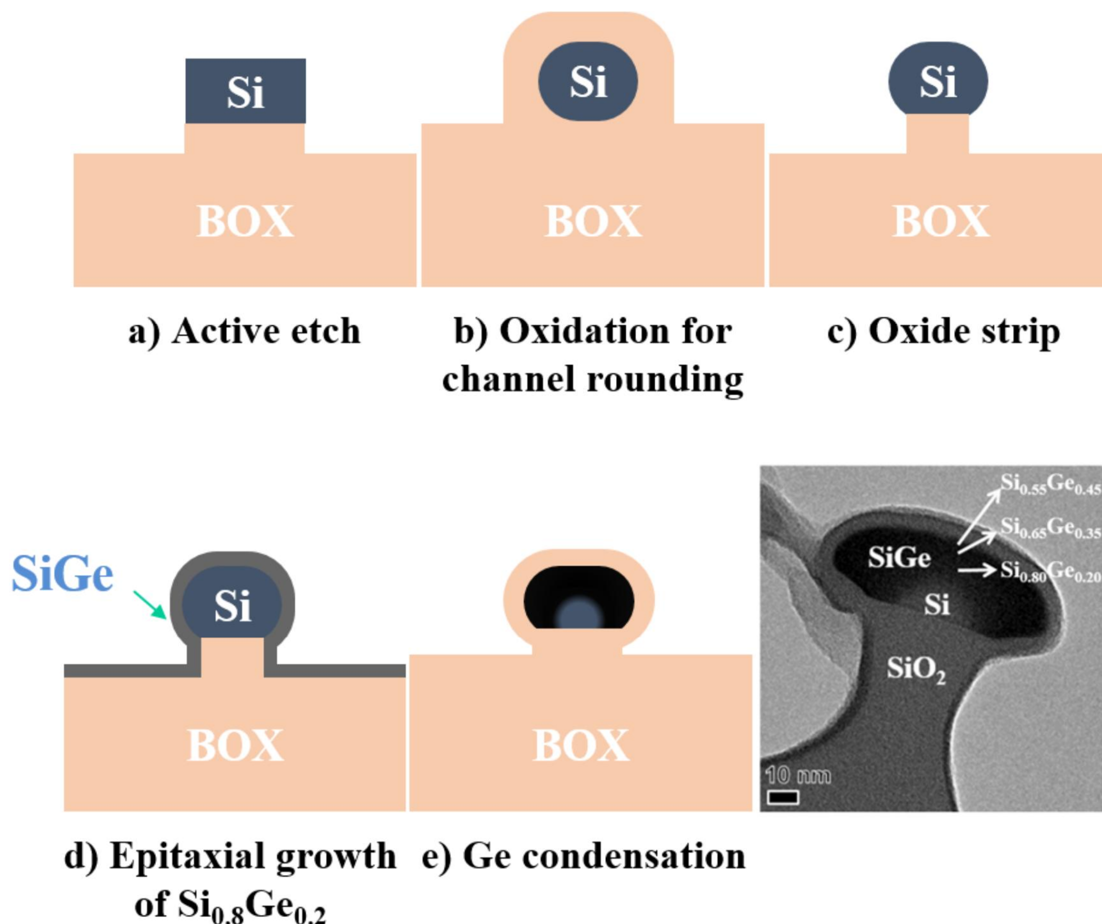
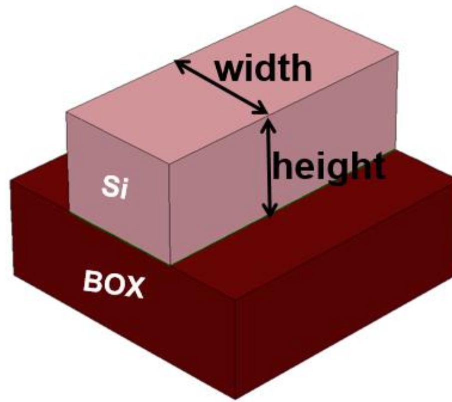
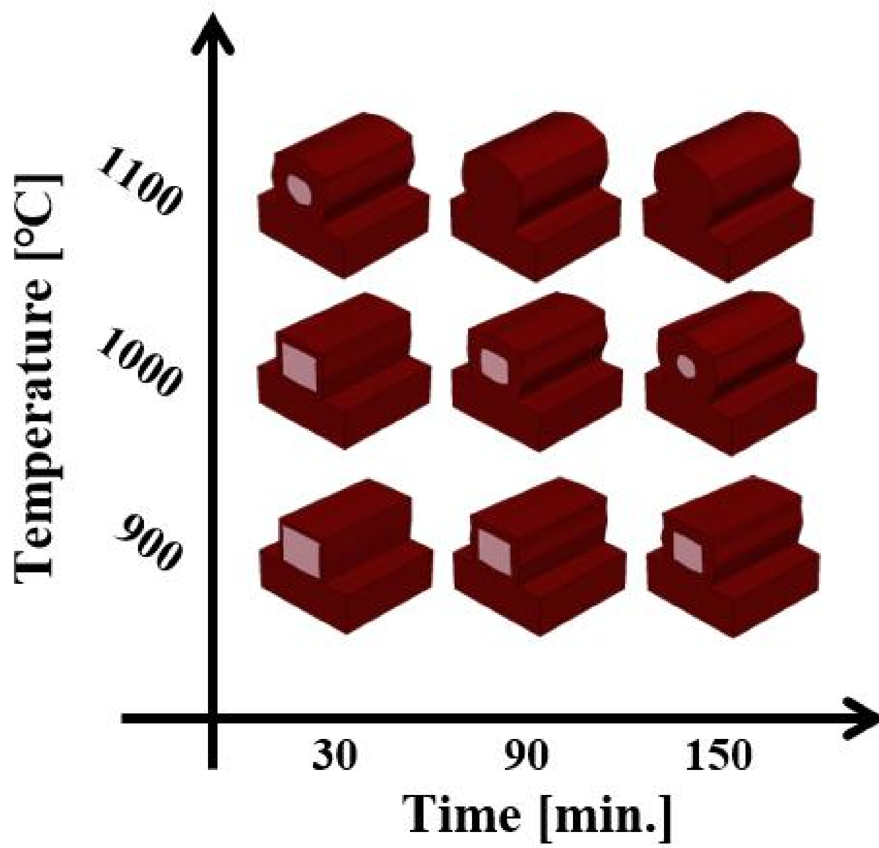


Figure 3.6: Process sequences for active formation.

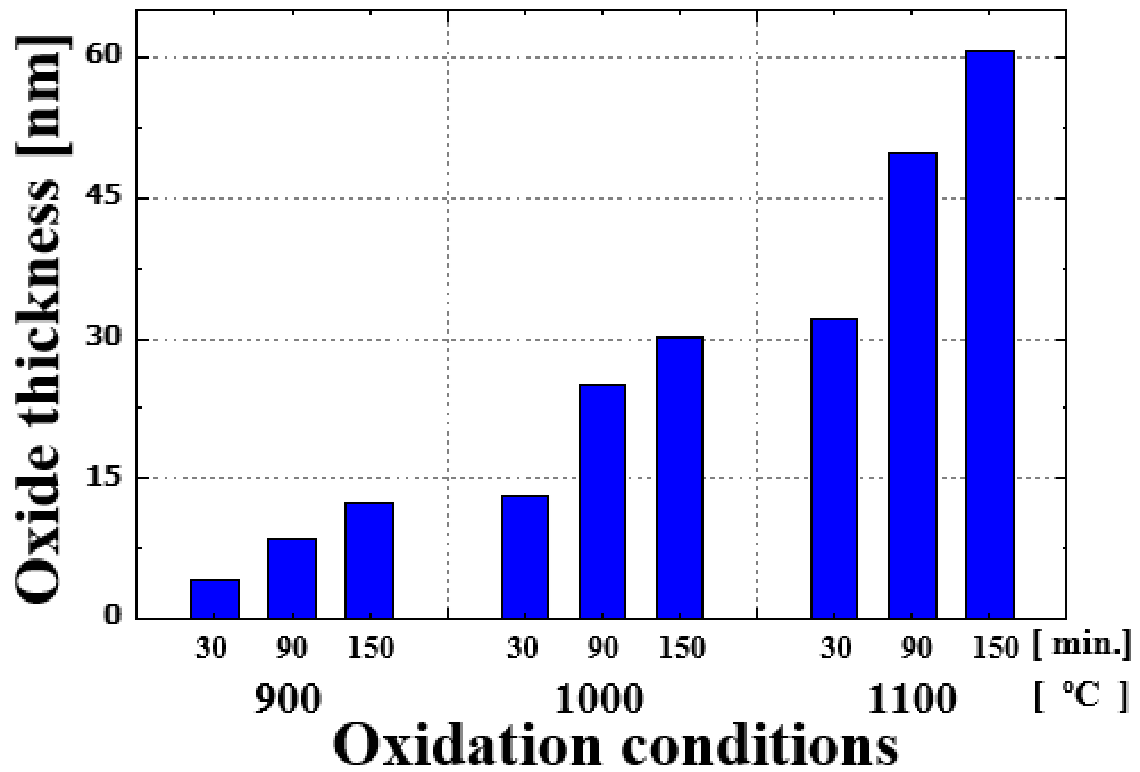
(a)



(b)



(c)



(d)

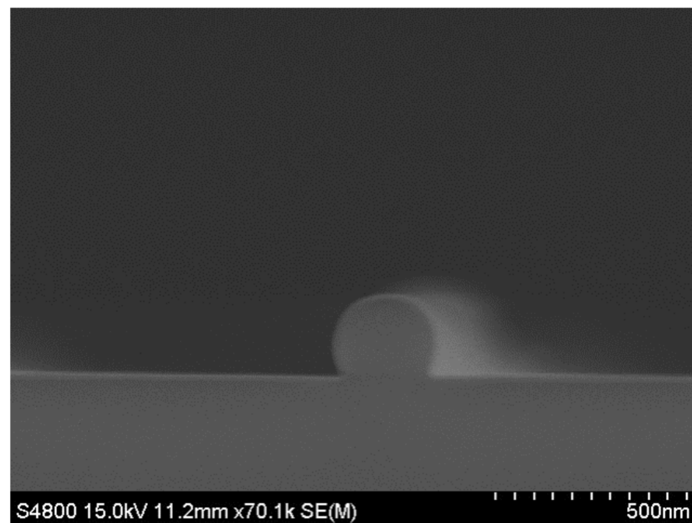


Figure 3.7: (a) Active Si (90 nm width and 70 nm height) before first oxidation process. (b) Shape of active Si after oxidation and (c) Oxide thickness with various temperatures and times.(d) scanning electron microscope (SEM) image from rounding oxidation.

3.2.3 Formation of Asymmetric Source/Drain Junction Depth

According to the band-to-band tunneling theory, the current of TFETs is proportional to (1/W_T)exp(-W_T). The TFET must have a small tunnel barrier width to turn it on quickly and increase the amount of current. Conversely, in order to reduce the ambipolar flow from the drain side to the channel in the off state, the tunnel barrier width viewed from the drain should be large. In other words, it is recommended that the source and drain have an asymmetric junction depth. A typical method used to form asymmetric junctions is to give an asymmetric underlap [15]. There are several ways to give an underlap, offsetting the position of photoresist during photolithography; Utilizing asymmetric spacers [31]; using raised-drain [16]. In this study, rather than giving the physical underlap, the process is designed so that the amount of annealing applied to the drain is greater than that applied annealing to the source, resulting in an asymmetric profile. In the conventional case, the annealing is completed once after the source and drain implantation. However, the proposed method anneals after the drain implantation and then anneals again after the source implantation. This increases the amount of heat applied only to the drain and increases the width of the tunnel barrier (W_T) that exists between the channel and the drain. In this regard, five cases of process simulation are performed to adjust the amount of heat applied to the drain side and apply the same heat to the source. The doping profile is transferred to the TCAD

simulation tool and the tunnel barrier appeared on the energy band in the off state (Fig. 3.9). In addition, the number of carriers generated by band-to-band tunneling between the drain and the channel is also confirmed (Fig. 3.11). Simulations are designed to apply more heat to the drain from case 1 to case 4. The doping sequence follows 3.8 and each annealing condition is listed in the table 3.1. In each case from 1 to 4, barrier widths when the carrier under the channel conduction band looked at the state above the valence band on the drain side are extracted in Fig 3.10. And simulations confirm that the number of carriers produced gradually decreases when the device at the ambipolar state.

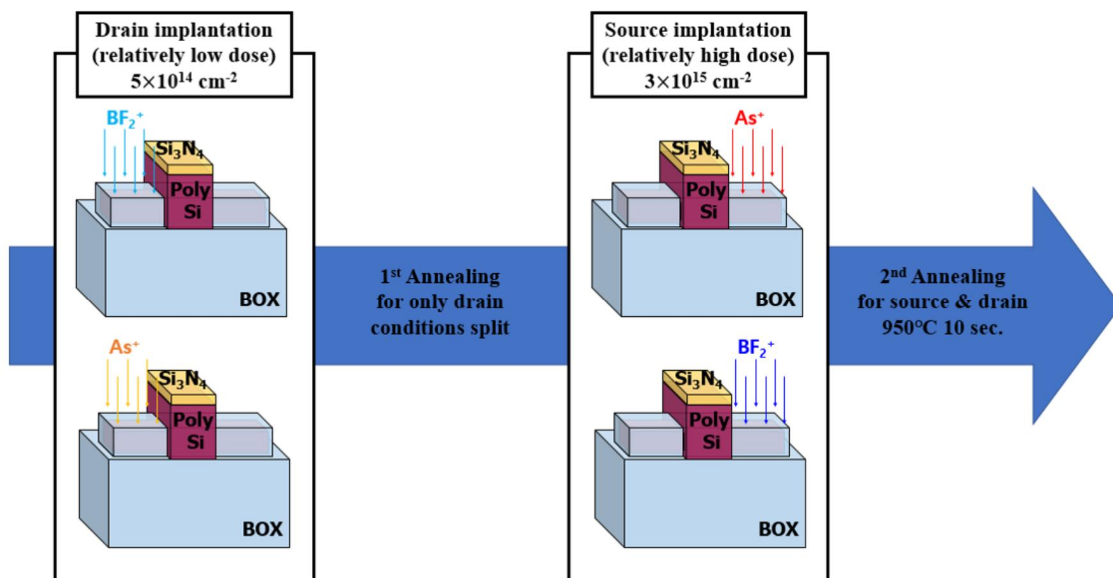


Figure 3.8: Ion implantation sequence to Create asymmetric source and drain dopant Profiles.

Table 3.1: Ion implantation conditions to create asymmetric source and drain profiles

Case	1st ion implantation (dose : $5\times10^{14}cm^{-2}$)	2nd ion implantation (dose : $1\times10^{15}cm^{-2}$)
Case1	-	950 °C 10sec
Case2	950 °C 40sec	950 °C 10sec
Case3	1000 °C 40sec	950 °C 10sec
Case4	1050 °C 40sec	950 °C 10sec

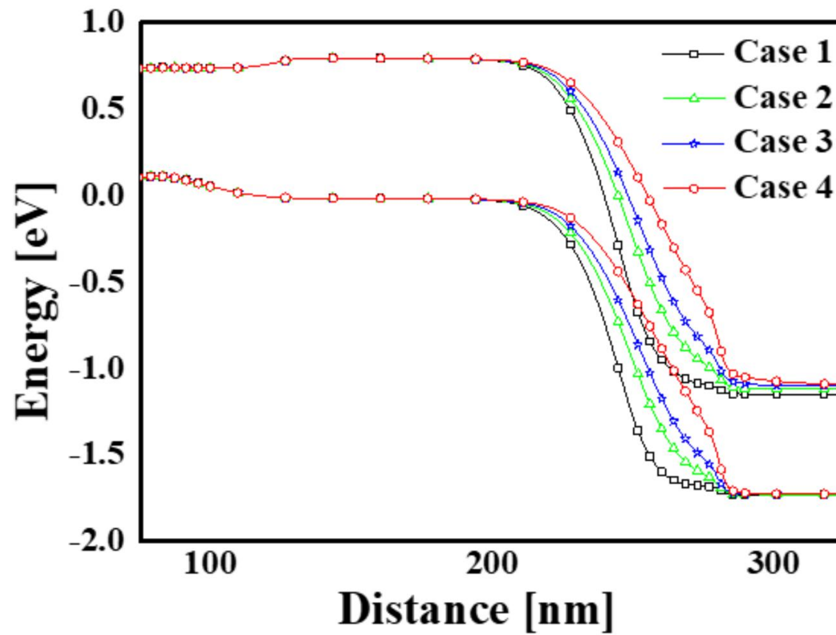


Figure 3.9: Energy band changes due to heat applied to the drain.

Figure 3.10: Barrier width extracted in off state according to various temperatures.

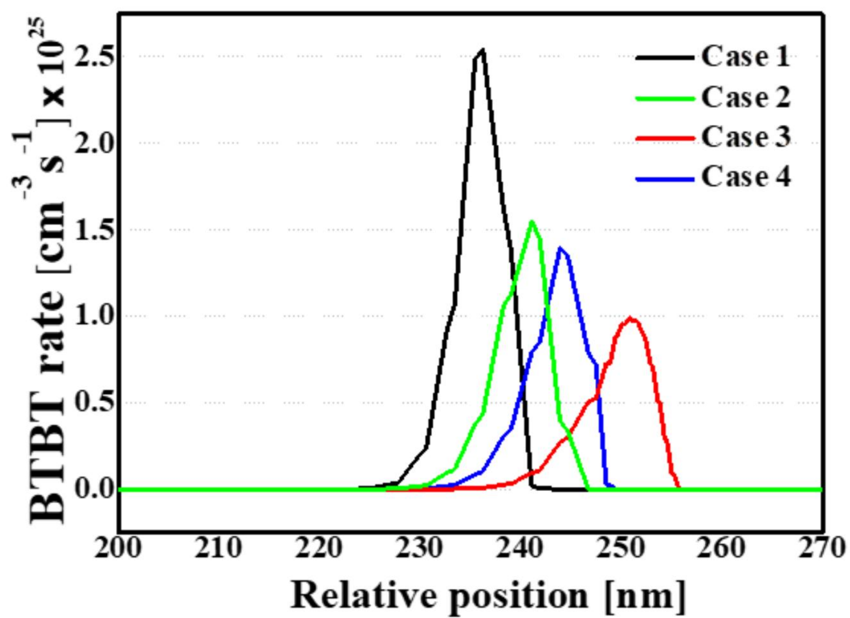


Figure 3.11: Comparison of band to band generation rate at turn off state.

3.2.4 Metal Gate Process

The fabrication of the device required the optimization of the metal gate process. Material options that can be used as dummy gates are poly-Si or silicon-nitride (Si_3N_4). Selecting only one of the two materials simplifies the manufacturing process so that a dummy gate is first formed with each material.

Dummy gate: poly-Si

The advantage of using poly-Si as a dummy gate is that it has a good etch selectivity with the underlying buffer oxide. As shown in the table 3.2, the selectivity of Si and SiO_2 is reported to be about 139.5: 1 in the equipment used in this study [32]. Thus, when patterning and removing dummy gates, the process can be continued without damaging the channel layer, due to its superior selectivity. However, CMP runs without a stop layer such as Si_3N_4, so there is a problem with uniformity [30]. The test showed that when using a single poly-Si as a dummy gate, there is no stopper, so the CMP time could not be taken long and some SiO_2 had to be left over the dummy gate. The problem is confirmed by the nano-spectroscopy that the length of the A portion shown in the figure 3.12 (a) shows a large variation from 1700 to 2100 Å. As can be seen in 3.12, The dummy gate is not exposed even after performing CMP, but is covered with an oxide film, thereby increasing the process of performing photolithography and

etching.

Table 3.2: Etch selectivity of Si to SiO_2

	T	C	B	L	R	Average
Etched Si [Å]	3690	3530	3810	3490	3790	3662
Etched SiO_2 [Å]	25	23	29	25	30	26
Selectivity of Si to SiO_2	146.4	150.9	131.4	140.7	128.0	139.5

Table 3.3: Etch selectivity of Si_3N_4 to SiO_2

	T	C	B	L	R	Average
Etched Si_3N_4 [Å]	3586	3474	3576	3438	3670	3549
Etched SiO_2 [Å]	2430	2380	2340	2340	2420	2382
Selectivity of Si_3N_4 to SiO_2	1.48	1.46	1.53	1.47	1.52	1.49

Dummy gate: Si_3N_4

The second option material that could be selected as the dummy gate material is Si_3N_4. Since the material can be used as a CMP stopper, it is not buried in oxide after CMP and is immediately exposed, so that wet etch can be easily performed without additional photolithography. However, as can be seen from the table 3.3, the etch selectivity be-

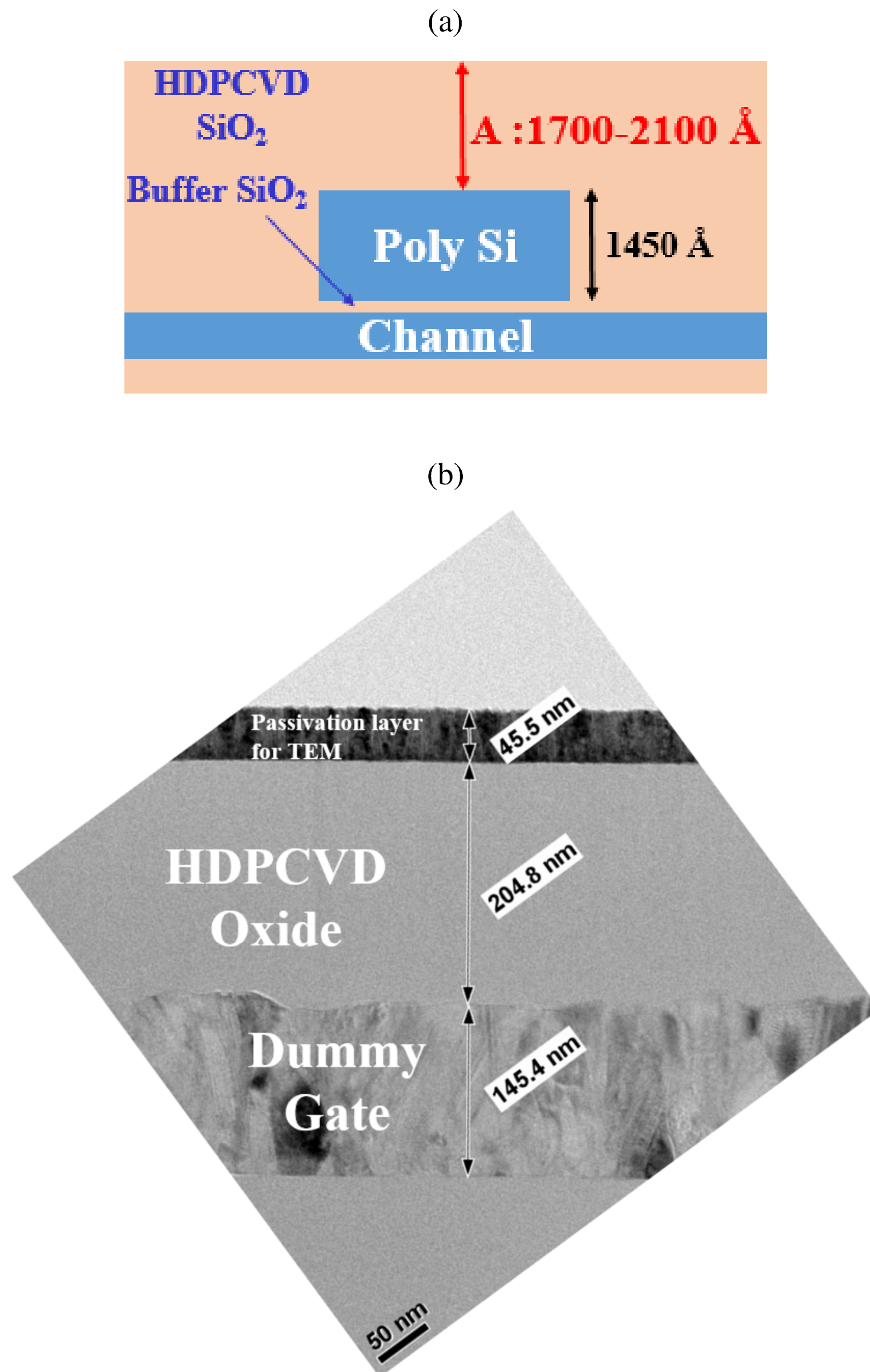
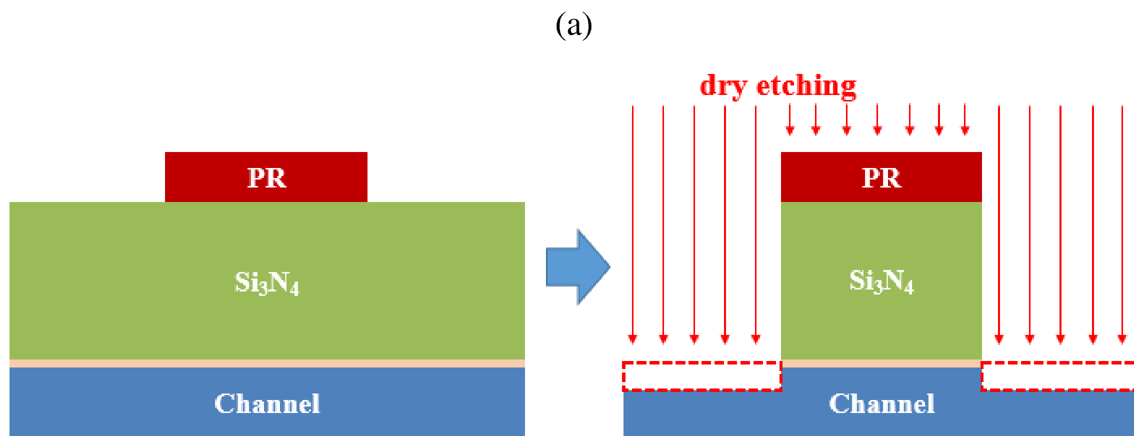


Figure 3.12: (a) Schematic diagram after CMP when using poly-Si as dummy gate (b) TEM image of CMP result.

tween Si_3N_4 and SiO_2 is 1.49:1, Fig. 3.13 (a) Channel material formed under SiO_2 is not protected by buffer oxide and may be etched away. These parts must be protected because they will be made to be source and drain.

(a)



(b)

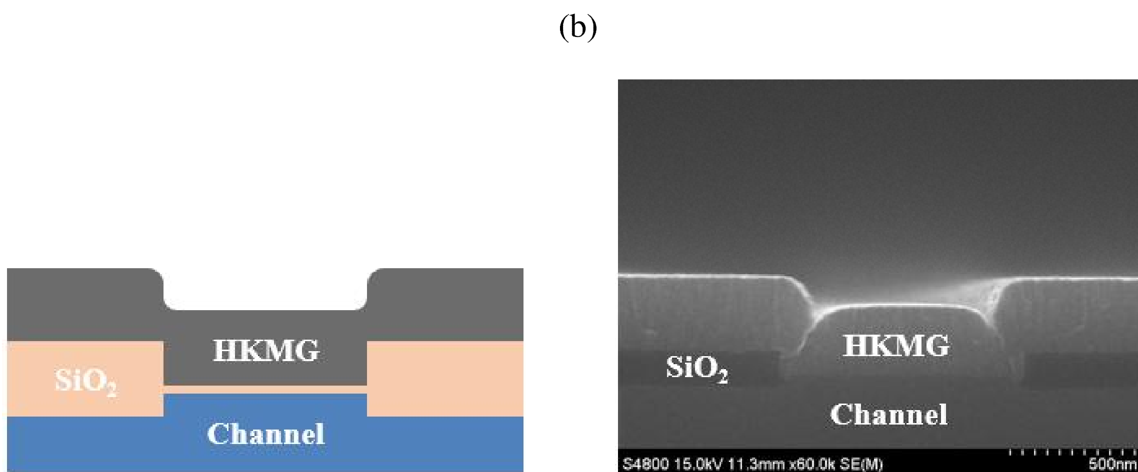


Figure 3.13: (a) Channel material loss during Si_3N_4 etch (b) Results of a HKMG process followed by (a).

Dummy gate: Si_3N_4 on poly-Si

From the experiences of the previous experiments, creating a dummy gate using poly-Si or Si_3N_4 alone is problematic. Therefore, in this experiment, the dummy gate is composed of Si_3N_4 and poly-Si for each purpose; upper Si_3N_4 for CMP stop layer; poly-Si for protection buffer oxide and channel material. The diagrams of constructing a dummy gate with two materials as a dual hardmask is shown in Fig. 3.14 (a). Low-pressure chemical vapor deposition is used to sequentially cover approximately 1500 Åof poly-Si and Si_3N_4. After forming a photoresist pattern by photolithography and dry etching the two materials sequentially, CMP is performed until Si_3N_4 appears on the surface and soaked in a 160 °C phosphoric acid solution (H_3PO_4) for 40 minutes to strip the Si_3N_4. Finally, dry etching the poly-Si on the surface completes the dummy gate removal process. Since the buffer oxide under the dummy gate has etch-selectivity with poly-Si, it can be over-etched by more than 100%. The SEM results of HKMG are shown in Fig. 3.14 (b). It can be seen that up to the subsequent high-κ metal gate is effectively performed without channel partial etching.

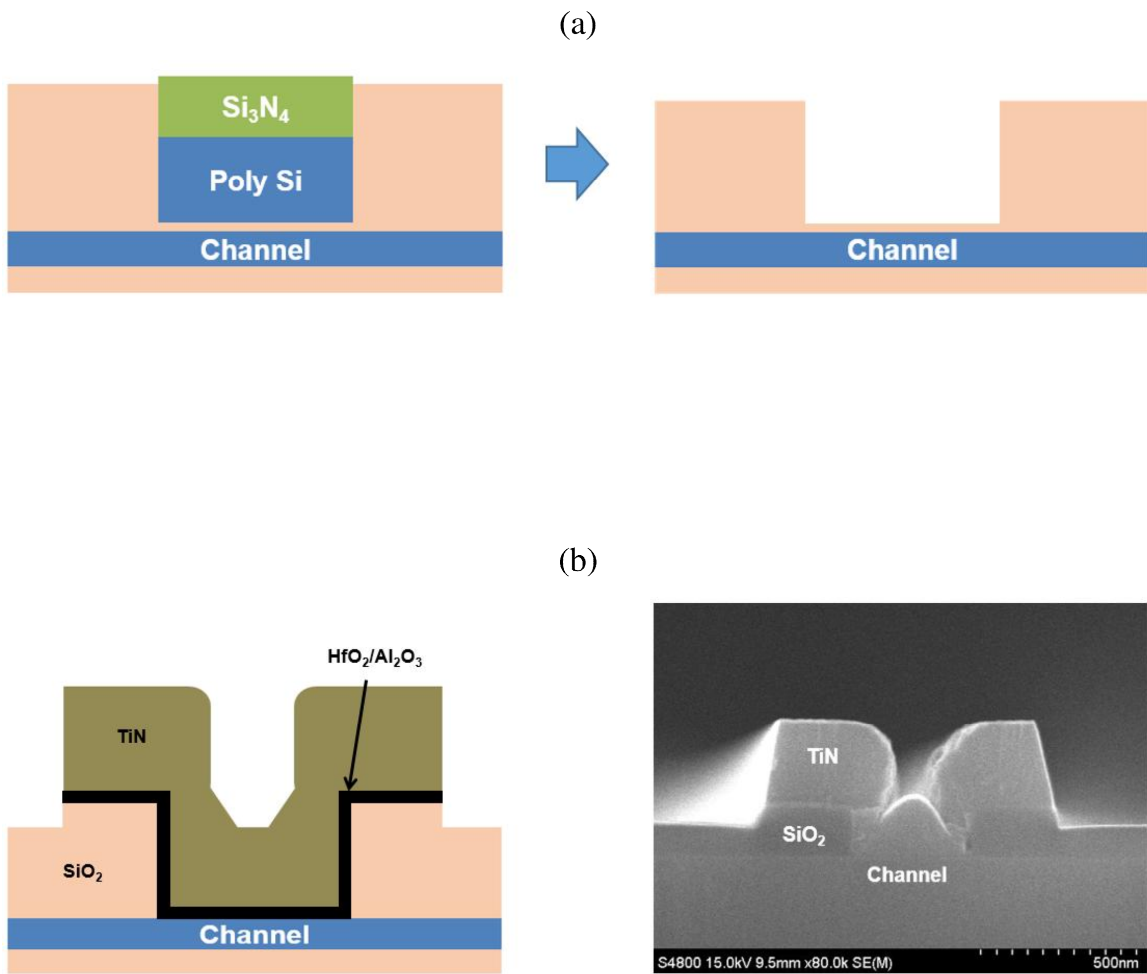


Figure 3.14: (a) Forming and removing dummy gate using poly-Si and Si_3N_4 as dual hard masks. (b) Results of a HKMG process followed by (a).

Chapter 4

Device characteristics

4.1 Optimization of Gate Dielectric

In the process of forming high-κ metal gate stack (HKMG), HfO_2 is used as main dielectric material, and Al_2O_3 is inserted as an interlayer (IL) to improve interfacial state with SiGe (Fig. 4.1. Additionally, in order to improve the quality of dielectric [i.e., in order to lower the interface trap density (D_{IT})], post metallization annealing (PMA) is performed in a gas ambient containing 5% of H_2 and 95% of N_2 with high pressure at 450 °C for 30 min. For PMA condition, the preceding study by M. schmidt [33] is adopted.

The effects of PMA on the quality of the high-κ/metal gate stacks are examined by capacitance measurements as a function of V_{GS} in MOS capacitors by using HP4284A

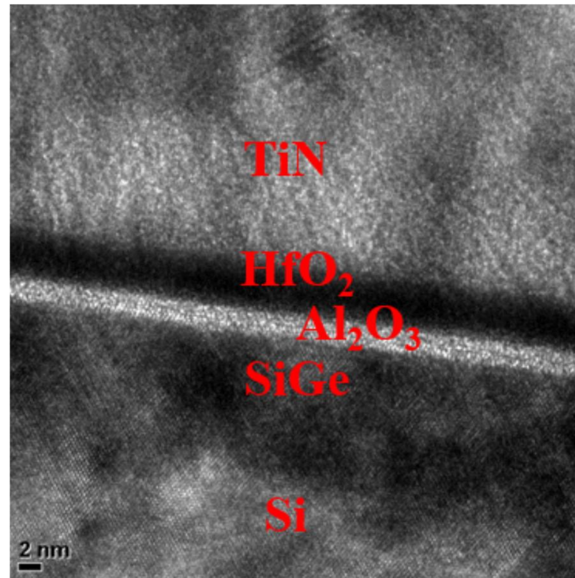
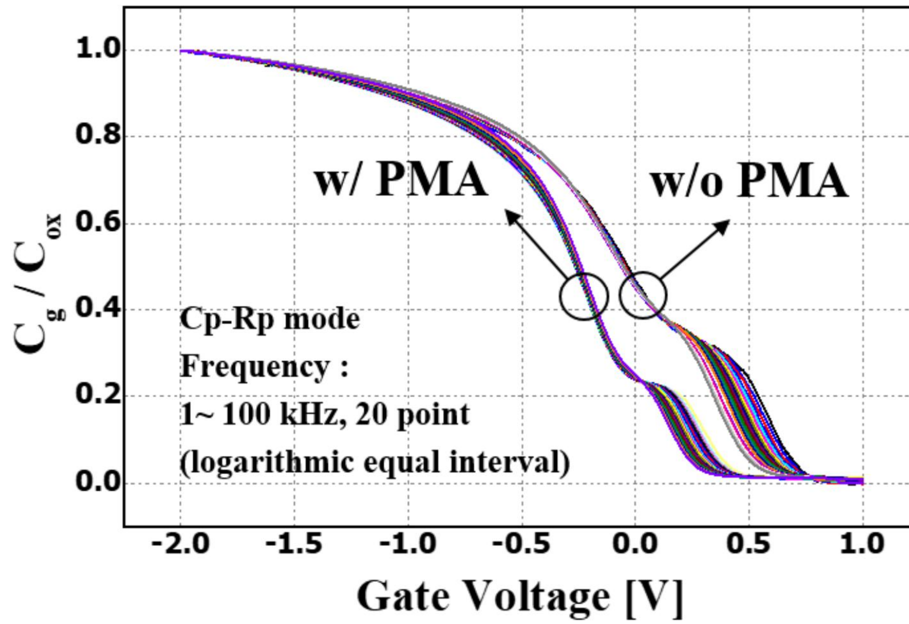


Figure 4.1: Fabricated MOS structure.

precision LCR meter. The capacitance-voltage (C–V) characteristics shown in Fig. 4.2 (a). Capacitance is measured in parallel mode with various frequencies, and real capacitance value (red dot) is extracted by using two-frequency method [34, 35]. The real capacitance graphs extracted by the described method are shown in Figs. 4.2 (b) and (c). The capacitance equivalent thickness (CET) before and after PMA is 1.70 nm and 1.72 nm, respectively. This leads to a slight difference in the potential of the gate applied to the channel, while PMA has a greater benefit in terms of hysteresis and D_{IT}. As shown in Fig. 4.3 (a), the hysteresis decreases by 160 mV. And, D_{IT} extracted by conductance method [36, 37] is reduced by about 20% (Fig. 4.3 (b)).

(a)



(b)

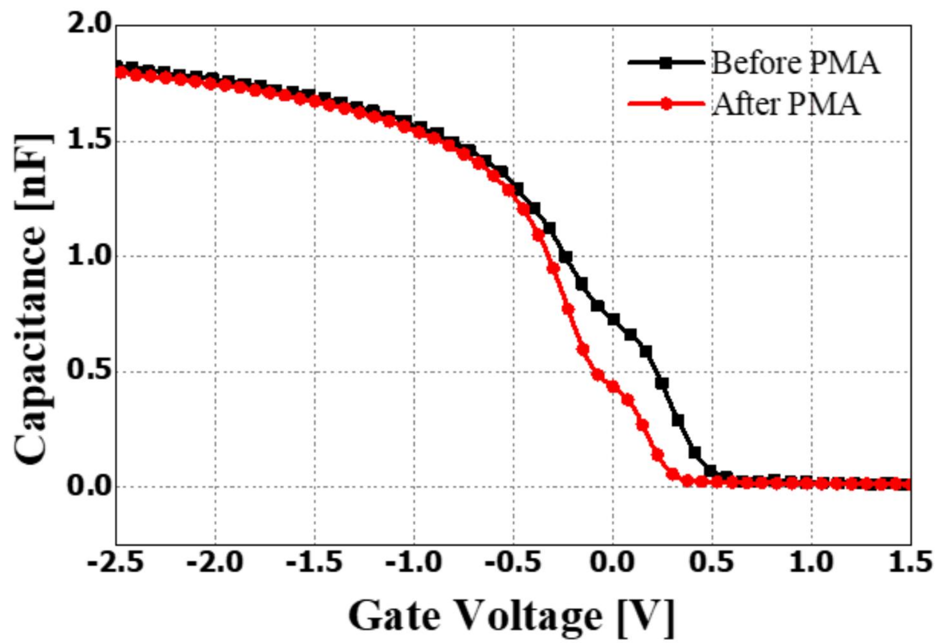
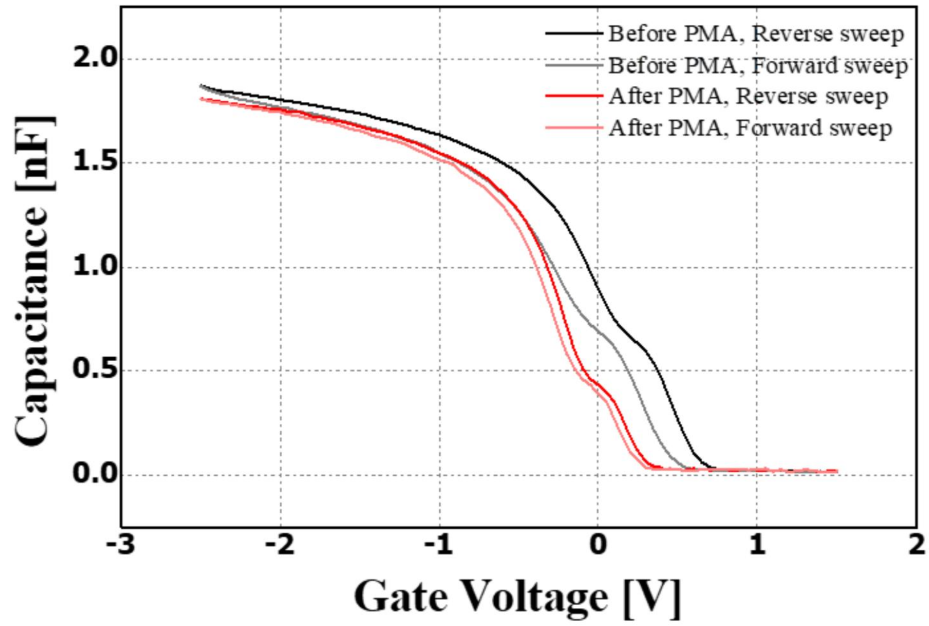


Figure 4.2: (a) Capacitance-Voltage (C-V) curves with various frequencies, and (b) with real capacitance values extracted by two-frequency method before & after PMA.

(a)



(b)

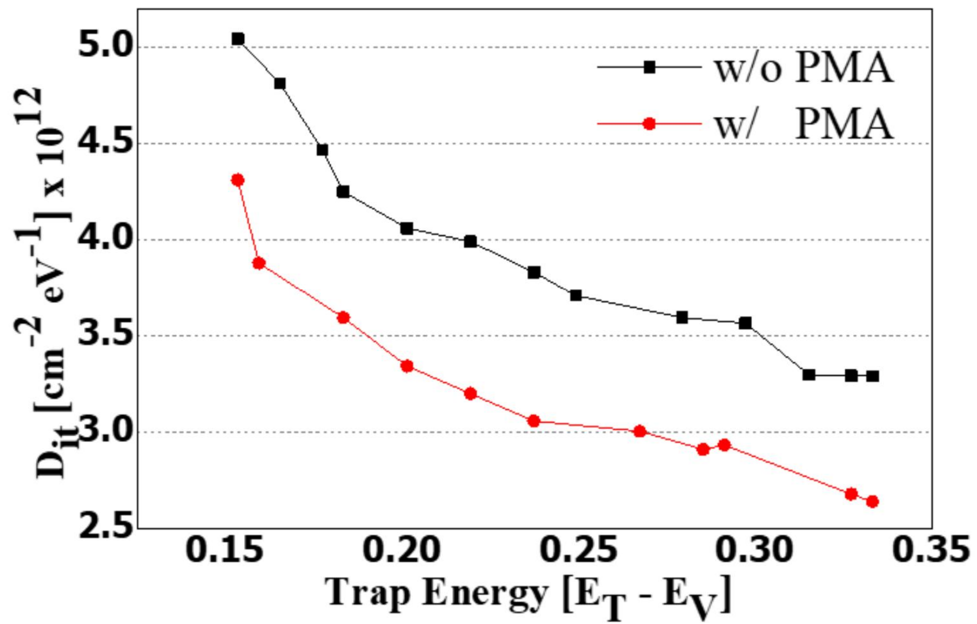


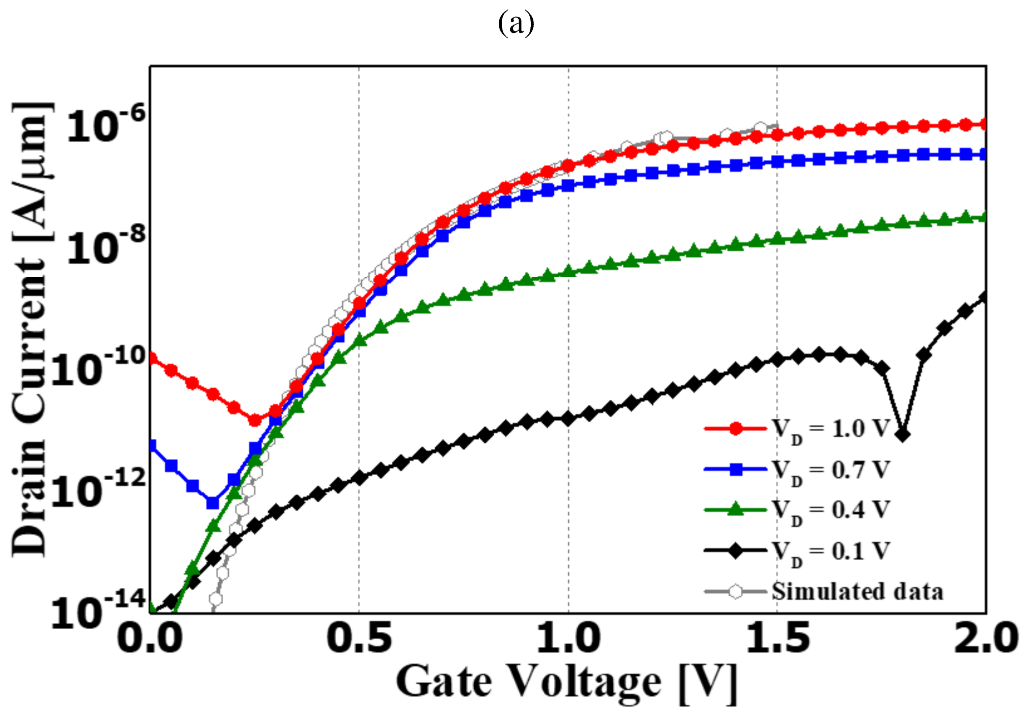
Figure 4.3: (a) Comparison of hysteresis C-V curves. (b) Interfacial trap state density as a function of trap energy.

4.2 DC Characteristics

Using all the previous unit experiments, the devices are fabricated. Figs. 4.4 are the measurement result according to the $|V_{DS}|$ of the nTFET and pTFET having the channel with the increased concentration of Ge content at the channel surface. Simulated data when $|V_{DS}|$ = 1 V are also attached, and it can be seen that they are well-matched. Figs. 4.5 shows the comparison of the transfer characteristics of each nTFET and pTFET between experimental group and control groups when $|V_{DS}|$ are 1 V. As expected in the previous chapter concerning simulation, the higher the Ge content, the better the device's performance. In the case of the experimental group for each nTFET and pTFET, minimum subthreshold swing (SS_{min}) of 26, 52 mV/dec are obtained and the on-off ratio are 1×10^6, 5.44$\times10^5$, whereas those of control SiGe TFET are 87, 66 mV/dec and 4.5×10^4, 5.2×10^4. The differences are attributed to the narrower W_T as indicated in Fig. 2.7. Figure 4.6 shows the SS of the surface Ge-rich TFET as a function of drain current (I_{D}). The SS is maintained less than 60 mV/dec from OFF-state to more than three orders. However, in the case of nTFET, when V_{DS} increases, band to band tunneling near drain is not well suppressed and ambipolar current appears at the off state. In the process of forming soruce and drain based on the process simulation, more heat is applied to the drain to spread the drain junction, but it is not enough. The drain of the nTFET is formed of arsenic, which has a diffusion constant less than that

of boron. Therefore, if the same heat is applied to both the nTFET and pTFET drain, the junction of the nTFET drain is sharper than the junction of the pTFET drain. To improve the process, heat is first applied after the drain implant of the nTFET so that more heat can spread the arsenic and widen the junction of the nTFET drain during a total of three annealing processes. Although the annealing process is added, the use of rapid thermal annealing (RTA) will not cause significant problems in terms of cost or time.

(a)



(b)

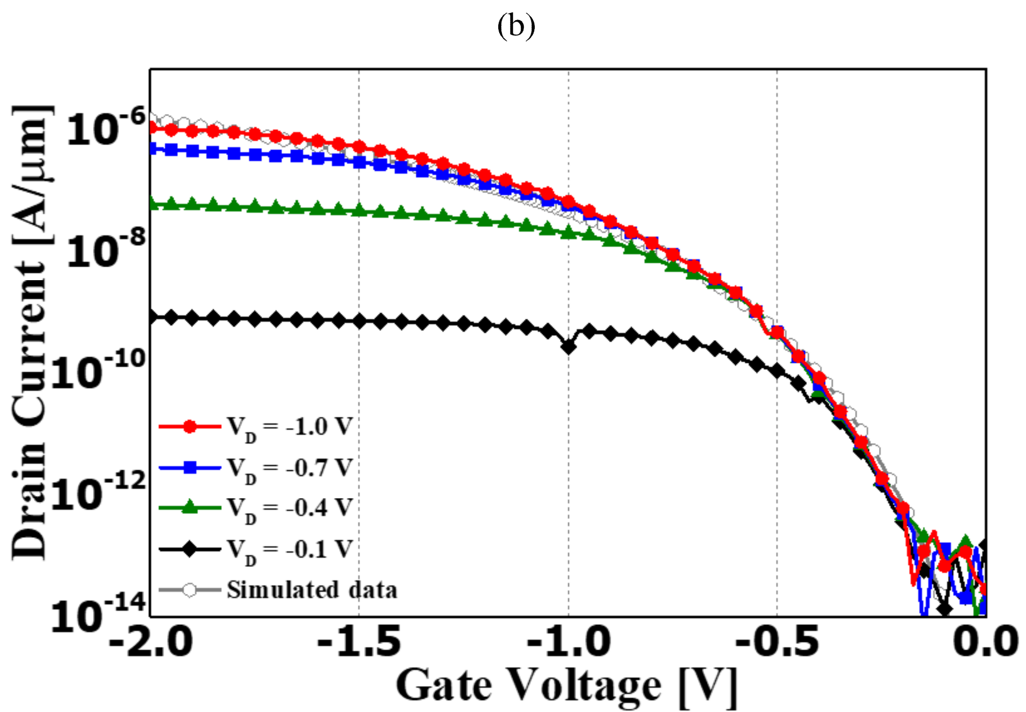
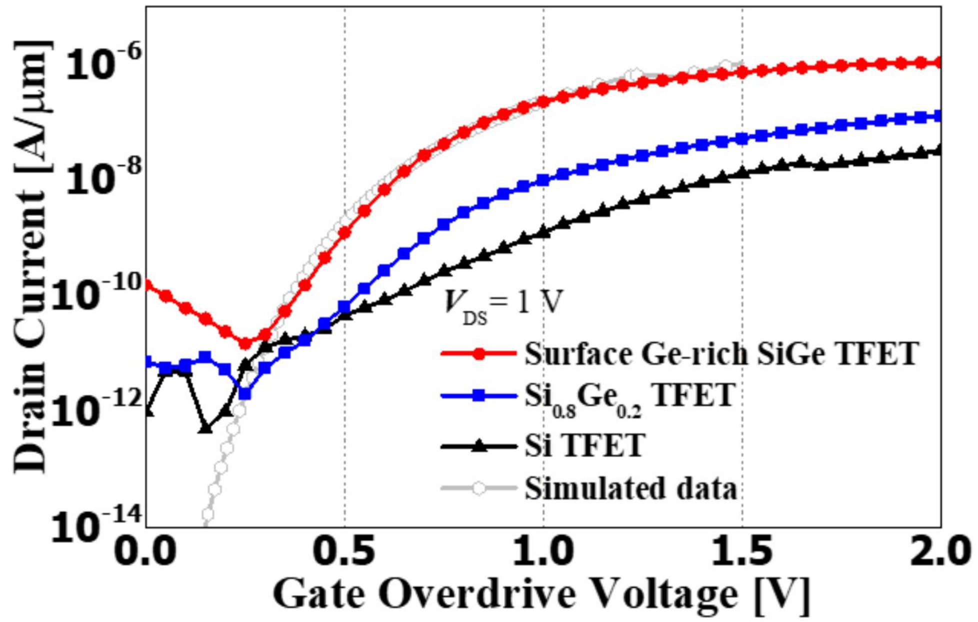


Figure 4.4: Transfer characteristics of (a) n-type and (b) p-type proposed tunnel FET

(a)



(b)

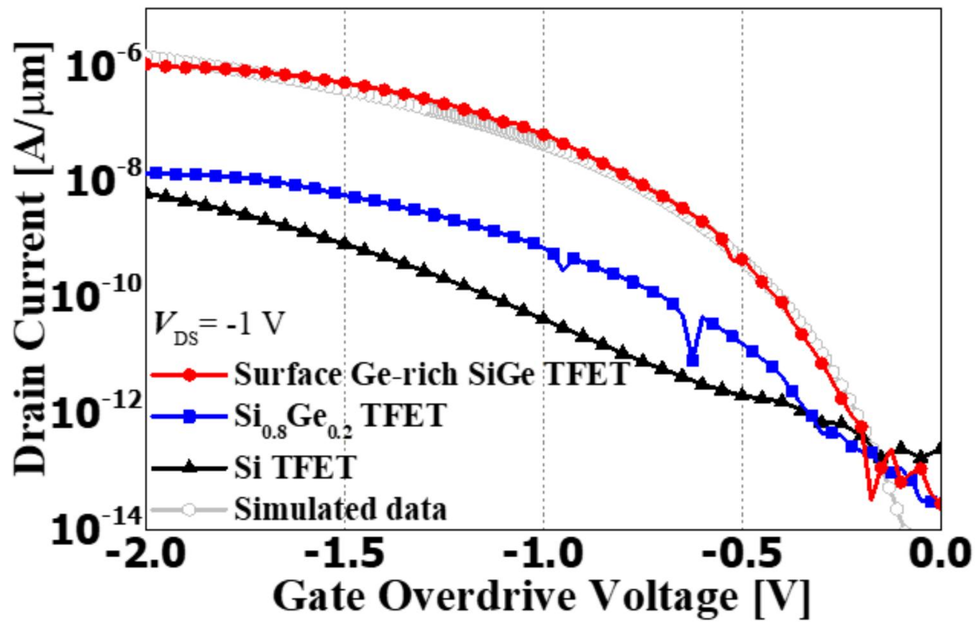


Figure 4.5: Comparison of transfer characteristics between experimental group and control groups when $|V_{DS}|$ = 1V.

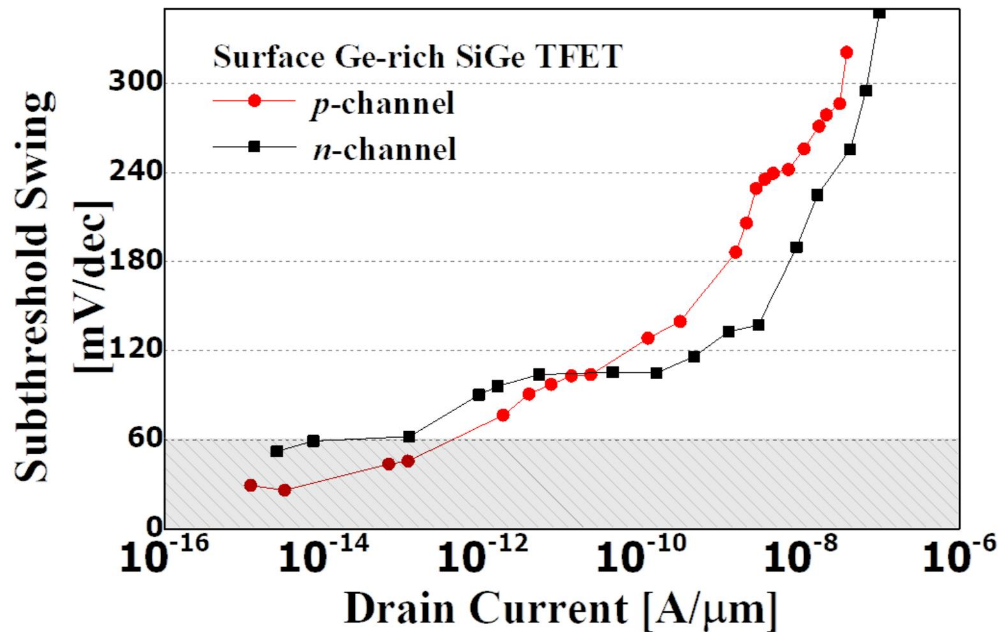


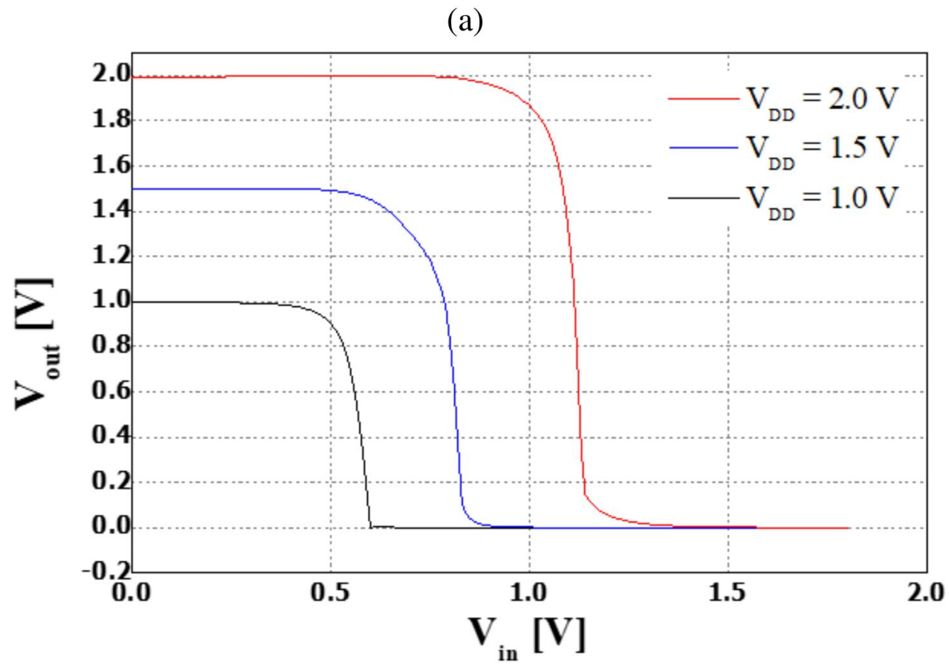
Figure 4.6: SS vs. drain current curve for surface Ge-rich SiGe TFET.

4.3 AC Characteristics

Inverters are manufactured by connecting the fabricated devices, and Figs. 4.7 show voltage transfer curves (VTCs). Figure 4.7 (a) shows an inverter composed of MOSFETs made through the same device fabrication process but with only the doped parts adjusted. Two masks are used for the doping of the MOSFETs, and they are designed to co-integrate together when making the TFET. In the case of the nMOSFET, when As is injected into the drain of the pTFET at high capacity, one mask layout is made so that it is also injected into the source and the drain of the nMOSFET. In contrast, for pMOSFETs, the other mask is made to inject high concentrations of boron into the

source of the nTFET and the source and drain of the pMOSFET. Figure 4.7 (b) shows an inverter configured by replacing a pMOSFET with a pTFET (hybrid inverter). In the meantime, the disadvantage of TFET has been pointed out that on current was smaller than MOSFET, so it has been impossible to make a circuit by mixing TFET and MOSFET. However, the current level of surface Ge-rich SiGe TFET is comparable to that of a MOSFET, making it possible to construct a circuit. The voltage gain of the hybrid inverter circuit is 13 at an operation voltage of 1V. This is not a huge difference when compared to 17 of the MOSFET inverter gain. If there is a fine tunning of TFET performance through future work, it can be overcome. Since the ambipolar characteristic of nTFETs is not effectively suppressed, the fabrication of inverters using only TFETs was not completed. In place of the fabrication results, the effect is verified by simulation, and the results are shown in the Figs. 4.3 (a) and (b). Transient response characteristics of the TFETs are investigated using mixed-mode simulation. Input ramp voltage is applied to peak voltage of 1.0 V and rise time of 1 ns. For considering fan-out, a load capacitor of 1 fF is used. As shown in Fig. 4.10 (b), the delay time of the proposed channel structure is about 14 ns, which is an improvement over 91.7 and 35.8 ns of the control groups.

(a)



(b)

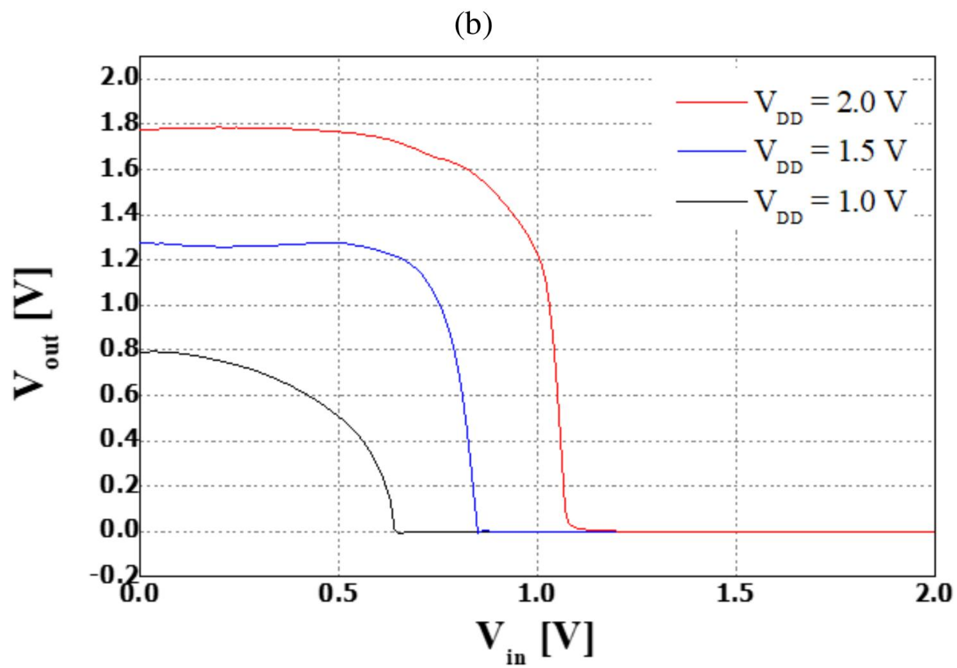
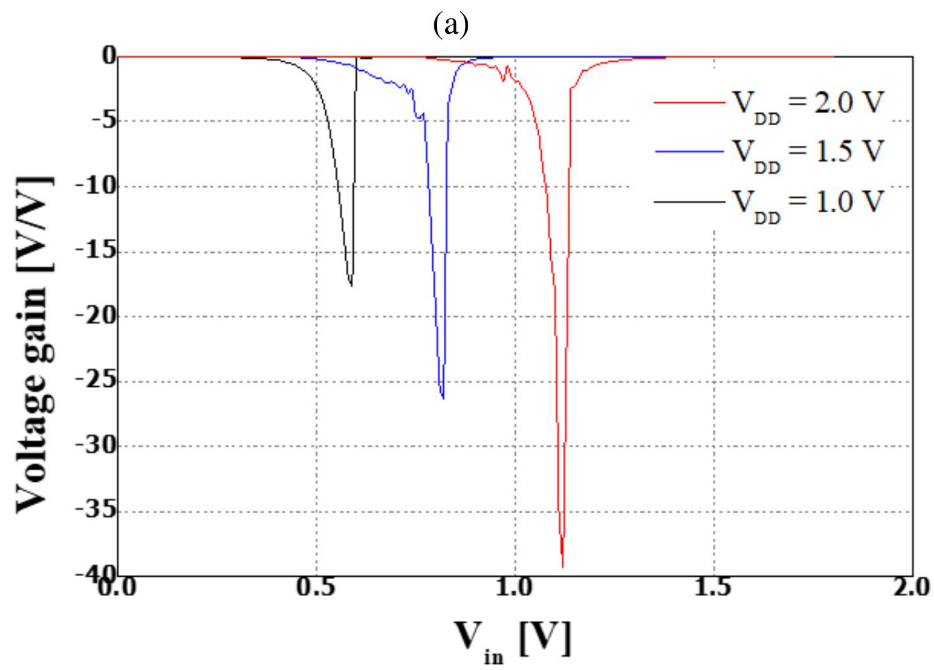


Figure 4.7: Voltage transfer curves of fabricated (a) MOSFET inverter and (b) hybrid inverter.

(a)



(b)

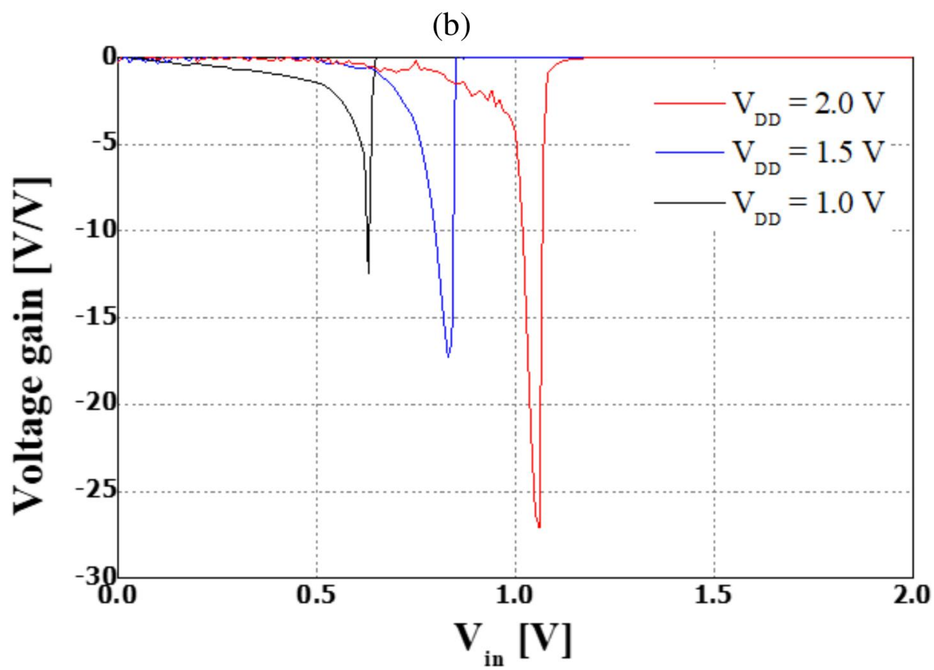


Figure 4.8: Voltage gain of fabricated (a) MOSFET inverter and (b) hybrid inverter.

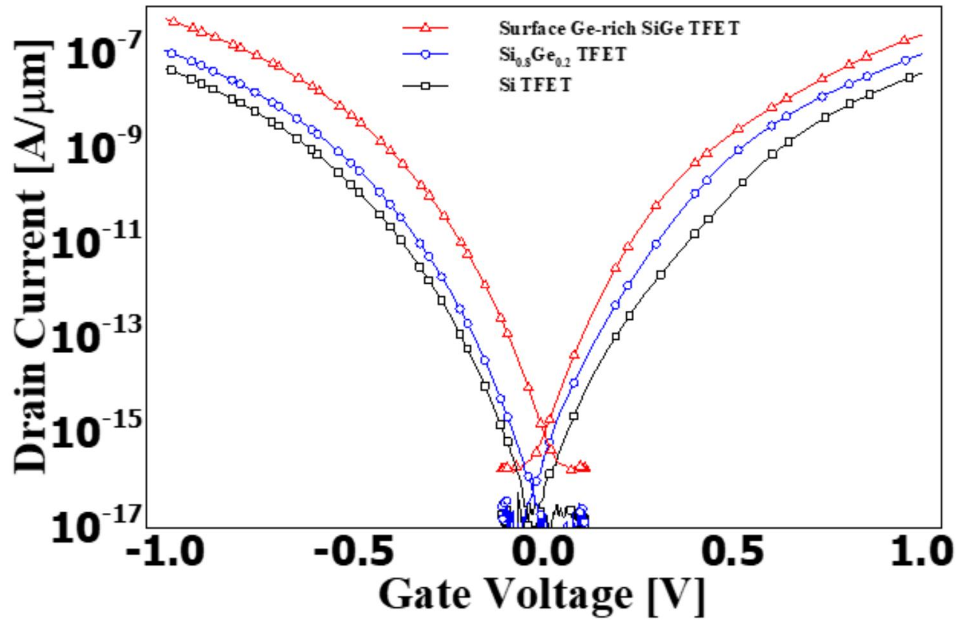
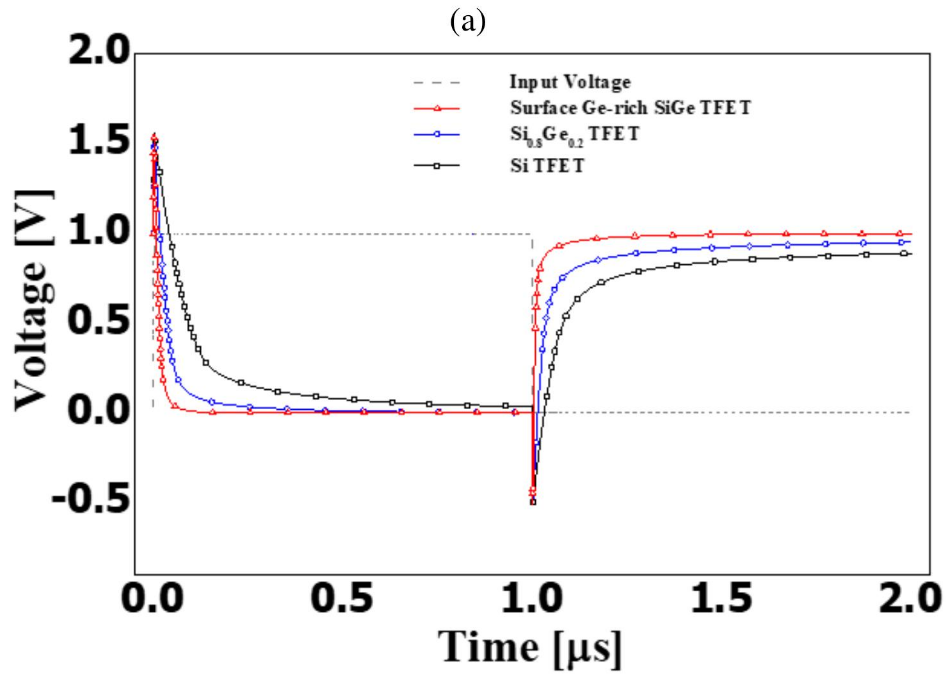


Figure 4.9: Transfer characteristics of nTFETs and pTFETs used in inverter operation.

Comparing with raised-drain structure

In previous work, there was a SiGe TFET with only a raised-drain structure of Si to provide a large bandgap material on the drain side [16]. The result SEM image of the fabricated SiGe channel TFET with raised Si drain is shown in Fig. 4.11. Since the drain-side material is Si having a larger value than that of SiGe, it has an advantage of suppressing ambipolar current. However, there is a disadvantage in that the overlapped area between the gate and the drain becomes large. It is well known that AC characteristics of TFET are closely related with C_{GD} [38]-[42]]. In this study, additional efforts have been made to make the difference between the source and drain concentrations

(a)



(b)

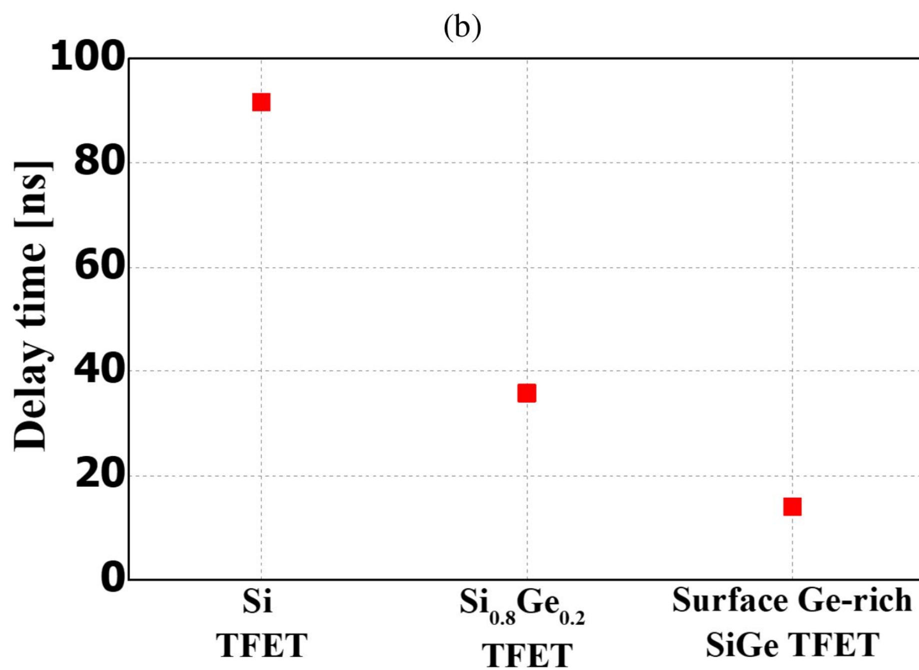


Figure 4.10: (a) Transient characteristics of nTFETs and pTFETs used in inverter operation, and (b) delay time.

in the device fabrication. In this case, the process adds a bit more than physically underlap, but it reduces the complexity of the process. Through simulation, the effect is verified. The figures of the device used in the simulation are shown in Figs. 4.12 (a) and (b). Physical parameters are summarized in table 4.1. Except for the region where Si is additionally deposited in the structure of Fig. 4.12 (b), the rest of the parameters are the same. The source-side structure shows that the operating current of the device is almost similar because the two structures are not different (Fig. 4.13). The results of the transient response are summarized in Fig. 4.14 in the same way as in the previous section. Raised drain inevitably has a structure in which there is a lot of overlap between the gate and the drain, and even high-κ material is inserted between the gate and the drain. To lower C_{GD}, materials with low-κ must be used, but inverter delays are increasing because the opposite material is used. Using the structure Fig. 4.12 (b) increases the delay by 2 to 2.5 times compared to using the structure Fig. 4.12 (a). Therefore, it can be seen that it is more advantageous to fabricate the device in the proposed method.

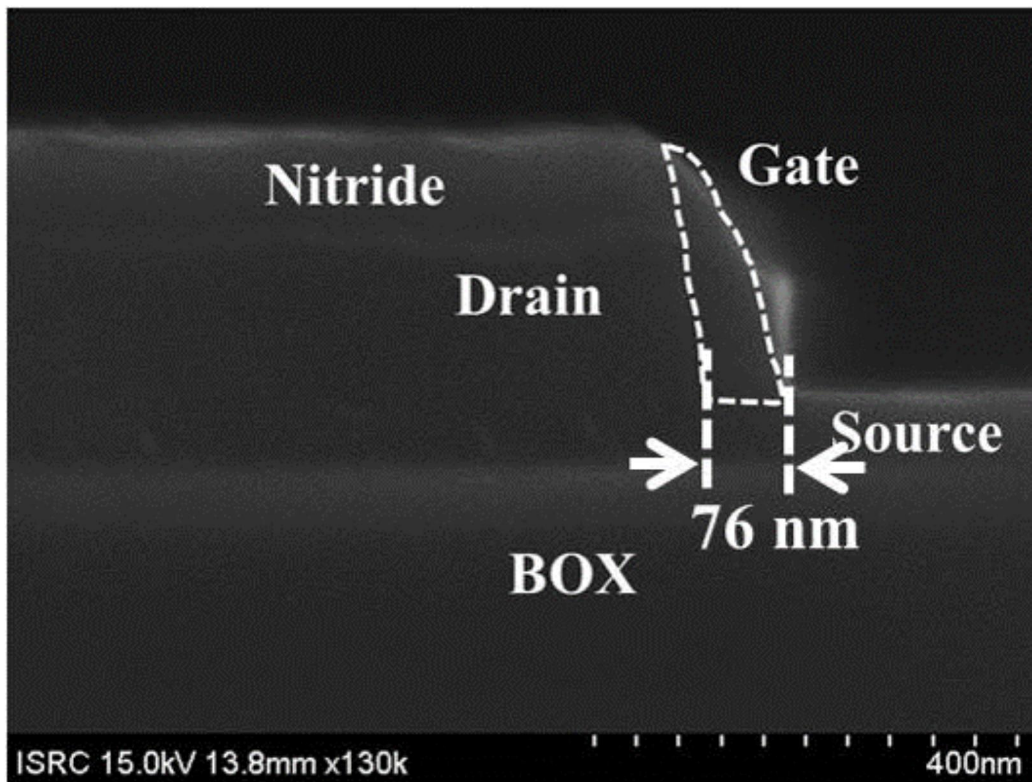


Figure 4.11: The result SEM image of the fabricated SiGe channel TFET with raised Si drain [16].

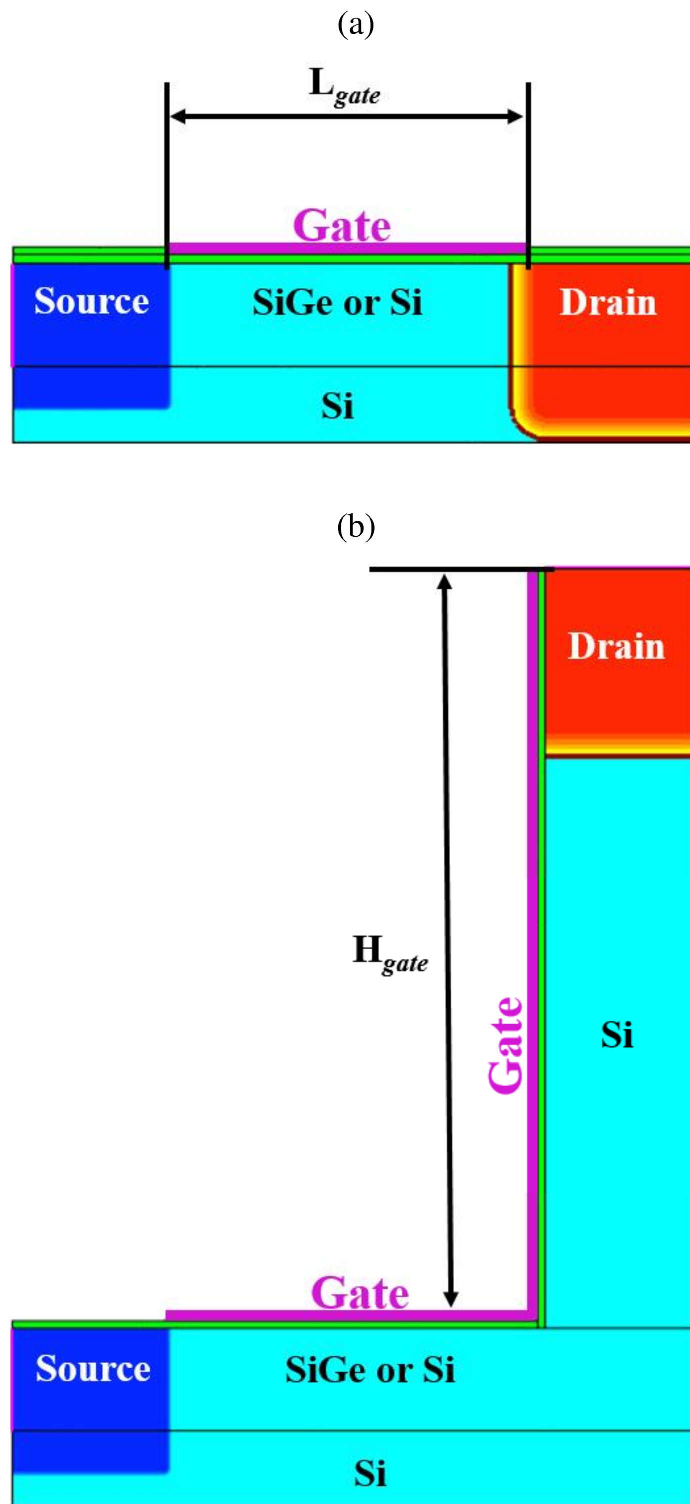


Figure 4.12: Structure used in the simulation for comparison (a) planar with gradual doped drain, (b) raised Si drain.

Table 4.1: The physical parameters of the TFETs used for the inverter simulations

Parameter	Value
L_{gate}	100 nm
H_{gate}	200 nm
EOT	1.7 nm
T_{SiGe}	30 nm
T_{Si}	10 nm
N_{Source}	$1\times10^{20}\ cm^{-3}$
N_{Drain}	$1\times10^{19}\ cm^{-3}$
N_{Body}	$1\times10^{16}\ cm^{-3}$

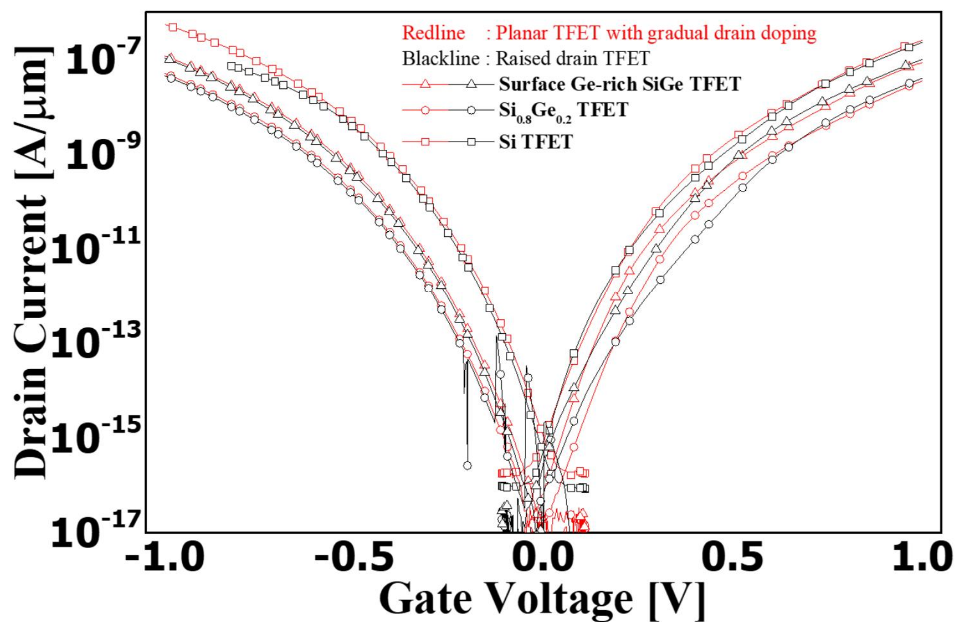
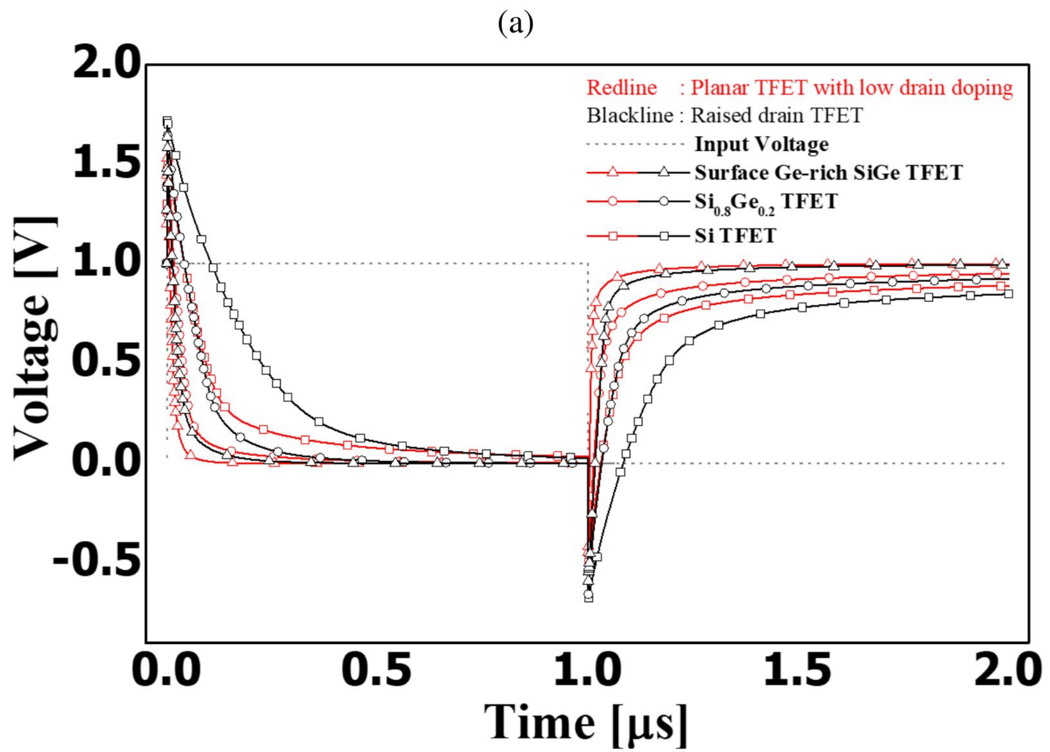


Figure 4.13: Transfer characteristics of nTFETs and pTFETs used in inverter operation.

(a)



(b)

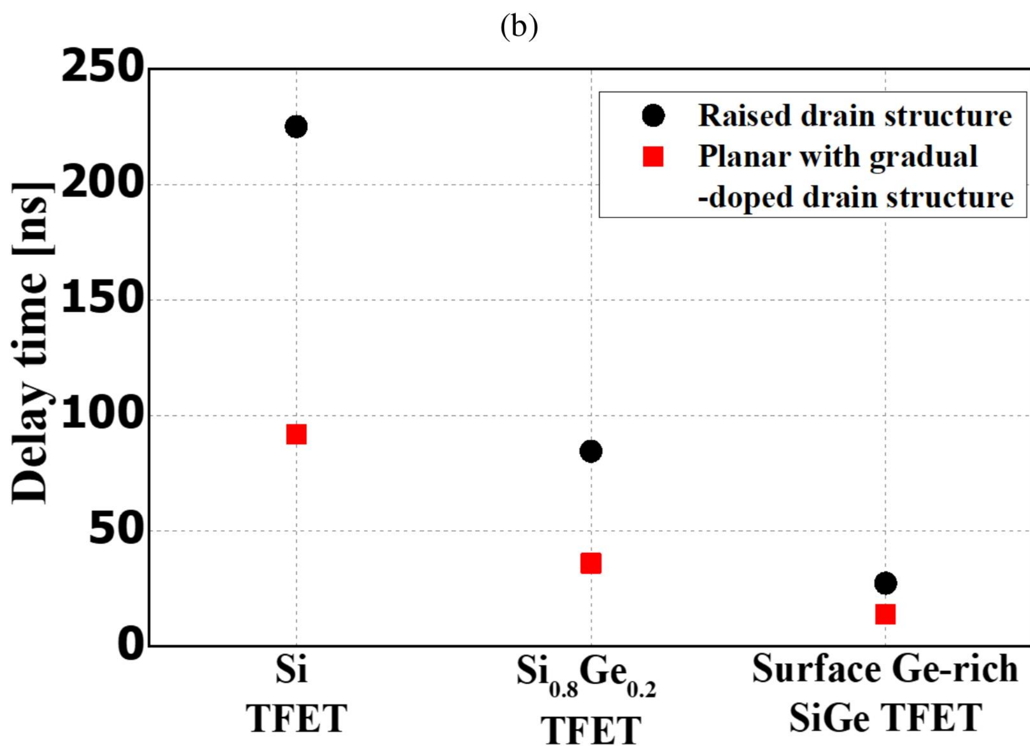


Figure 4.14: (a) Transient characteristics of nTFETs and pTFETs used in inverter operation, and (b) delay time.

Chapter 5

Conclusion

In this dissertation, Proposals and fabrication of TFETs with increased Si content as the channel have been made. When using SiGe, it is common to use the epitaxial growth of SiGe on a Si substrate rather than using a SiGe substrate for cost reduction. Due to the difference in lattice constant, the immediate growth of SiGe with high Ge content is burdened with dislocations. To realize this, a technique called Ge condensation has been used, and the work of increasing the Ge content near the surface has been performed in order to reduce the dislocation density. The reason why the surface content can be increased without increasing the Ge content of the entire channel is that tunneling current generation in the TFET occurs most directly under the gate (i.e., at the top of the channel).

It has been previously determined that the device could be verified by TCAD sim-

ulation in advance and improved over the control groups in terms of SS and I_{ON}. Fabrication process optimization for key processes such as Ge condensation, channel formation, asymmetric source and drain junction formation, and high-κ dielectric with metal gate process are preceded to fabricate the device directly. In summary for each, surface Ge-rich SiGe channel which Ge content have about 45% is successfully formed. And, The channel of omega-shaped is formed by oxidation & condensation method. The process flow is introduced to make the drain junction wider than the source junction, resulting in a device with a wider tunnel barrier width on the drain side than the source side. Finally, a process using a metal gate and a post metallization annealing condition is used to allow the gate to have lower interface trap densities with 1.7 nm EOT to improve controllability for the channel. Consequently, the surface Ge-rich SiGe TFET shows remarkable performances in terms of SS and $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ (minimum 26 mV/dec and 10^6 $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$).

For further performance improvements, In order to suppress the ambipolar current of the nTFET, a more additional annealing process is needed for the implant process. In particular, different annealing conditions will be required for the drains of the nTFET and pTFET. Given that we have optimized the conditions to make each transistor well, there are two major tasks that need to be done. First, establish a process for building a short channel self-aligned structure. This effort is necessarily recommended because

TFETs have a reverse doping type with source and drain. In the case of short channel devices, there is a misalignment factor provided by lithography, which may result in a misalignment of tens or hundreds of nanometers when performing photolithography. Therefore, there is a limit to doping to short channel device using photolithography. Second, in order to further increase the amount of current, it is necessary to make a device having a perfect GAA type structure and a channel stacked structure.

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초 록

상보형 금속-산화물-반도체 (CMOS) 기술은 라이프 인류의 삶을 혁신하고 생산성과 기능의 다양성을 확장하는 데 핵심 기술이다. 현재 이 기술은 소자의 크기 측면에서 나노 스케일 단위로 극도로 축소화 및 집적화가 이루어졌다. 이 개발은 리소그래피 기술의 향상으로 인해 가능해왔다. 그러나 소자의 크기가 줄어드는 것에 맞추어 전계 제어를 수행하지 않으면, 단 채널 효과가 발생하고 장치가 고장 나거나 대기 전력 소비가 증가하는 문제가 발생한다. 장치의 크기를 줄이는 데 비례하여 전기장을 줄이려면 구동 전압 (V_{DD}) 의 감소가 필요하게 된다. 그러나 트랜지스터의 임계 전압 (V_{TH})을 함께 낮추지 못하는 문제 상황이 있기 때문에 임계 전압을 고정한 상태에서 구동 전압만 줄인다면, 구동 전류가 줄어드는 문제가 있고, 소자의 문턱전압 이하 기울기의 역수 (SS) 의 개선 없이 임계 전압을 줄인다면, 대기 전류가 늘어나는 문제가 생긴다.

이러한 딜레마를 해결하기 위해서는 (SS)의 개선이 필수적이다. 그런데, SS의 관점

에서 금속-산화물-반도체 전계 효과 트랜지스터 (MOSFET) 은 게이트 전압 증가에 따른 드레인 전류 증가폭에 물리적인 한계치를 가지고 있다. 터널 전계 효과 트랜지스터 (TFET)는 이 한계를 극복할 수 있는 가능성이 있다. TFET에서의 전류 주입은 소스 접점에서 채널로의 대역 간 터널링에 의존하여 캐리어의 Fermi 분포의 고 에너지 테일이 흐르는 것을 차단하여 대기 전류를 줄일 수 있다. 따라서 낮은 V_{DD}에서 MOSFET보다 성능 이점을 제공합니다.

본 논문에서는 표면 Ge의 함량을 높게 만든 SiGe을 채널물질로 갖는 TFET의 제안 및 제작이 이루어 졌다. 제작 이전에 테크놀로지 컴퓨터 지원 설계 (TCAD) 시뮬레이션을 사용하여 유효성 검증을 먼저 수행하였고, 공정을 위한 제반 기술의 확보가 이어서 진행되었다. 채널 형성 단계를 제외하고 동일한 공정 흐름에 의해 제조 된 대조군들 (상수 Ge 농도 SiGe TFET 및 Si TFET)과 전기적 특성을 비교하여 구동 전류 및 SS 측면에서 개선을 확인할 수 있었다.

주요어: 밴드간 터널링, 터널링 전계효과 트랜지스터, SiGe, Ge 응축 기술, 저전력 소자, 문턱전압 이하 기술기, 전류 구동 능력

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