NANOMATERIALS

A wearable multiplexed silicon nonvolatile memory array using nanocrystal charge confinement

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Strategies for efficient charge confinement in nanocrystal floating gates to realize high-performance memory devices have been investigated intensively. However, few studies have reported nanoscale experimental validations of charge confinement in closely packed uniform nanocrystals and related device performance characterization. Furthermore, the system-level integration of the resulting devices with wearable silicon electronics has not yet been realized. We introduce a wearable, fully multiplexed silicon nonvolatile memory array with nanocrystal floating gates. The nanocrystal monolayer is assembled over a large area using the Langmuir-Blodgett method. Efficient particle-level charge confinement is verified with the modified atomic force microscopy technique. Uniform nanocrystal charge traps evidently improve the memory window margin and retention performance. Furthermore, the multiplexing of memory devices in conjunction with the amplification of sensor signals based on ultrathin silicon nanomembrane circuits in stretchable layouts enables wearable healthcare applications such as long-term data storage of monitored heart rates.

INTRODUCTION

Flash memory devices based on single-crystal silicon (Si) have become the leading nonvolatile data storage device owing to single-crystal silicon's high performance and compatibility with complementary metal-oxide semiconductor (CMOS) processes (*1*–*3*). In a flash memory, information is converted into a charge level and then stored in floating gates (FGs) (*4*). Therefore, the FGs determine the performance of a flash memory. However, FGs based on conventional conducting thin films face challenges such as difficulties in modulation of charge trap density and charge losses via locally distributed defects (*4*–*6*).

Various studies have investigated new materials to replace those used in conventional FGs to achieve increased charge storage efficiency (*7*–*10*). As a viable alternative, gold nanoparticle (AuNP) FGs have been proposed (*11*–*16*). AuNP FGs afford many advantages such as controllability of charge trap density, superb chemical stability, high work function, and, most importantly, efficient charge confinement (*17*). However, nanoscale experimental observation of charge confinement in closely packed AuNP FGs has not been reported yet. Such characterization capability is useful for understanding different aspects of charge confinement in various types of AuNP FGs (for example, different sizes or densities of AuNPs), enabling further optimization to improve memory performance. In addition, most of the previous nanocrystal-based memory devices have focused on a single memory cell instead of a multiplexed memory array in which each cell is individually addressable (*11*, *12*).

At the same time, rapid developments in wearable electronics have led to an urgent demand for deformable electronic devices such as sensors (*18*–*24*), circuits (*25*–*27*), displays (*28*–*30*), and memories (*11*, *12*, *31*–*34*). Most deformable memory devices reported so far, however, are just flexible. These kinds of memory devices are not compatible with wearable applications that require complicated modes of mechanical deformations such as stretching (*35*, *36*). Although previously reported stretchable flash memory devices (*37*) showed some advances, isolated memory cells rather than interconnected ones, relatively unstable data storage owing to intrinsic hysteresis of carbon nanotubes, and metal thin-film FGs that lead to incomplete charge confinement have impeded their use in practical applications. Reliability of the fabricated devices under ambient conditions and process compatibility with conventional CMOS fabrication processes are additional important factors. Considering these, the stretchable memory based on single-crystal silicon nanomembranes (SiNMs) is a good candidate for wearable electronic device applications (*34*, *38*). Although many previous studies have investigated stretchable Si electronics such as diodes (*35*, *36*), transistors (*39*), sensors and actuators (*34*, *38*, *40*), and logic circuits (*41*), the deformable charge trap FG memory (CTFM) based on single-crystal Si has not yet been reported. The integration of Si CTFMs with other sensors and electronics in one wearable platform is another important unmet goal. To realize a large memory window and capacity with high cell-to-cell uniformity, an efficient large-area fabrication process for the uniform and high-density assembly of AuNP FGs on a Si electronics platform is an additional key requirement.

To address these critical issues, in this study, we developed wearable SiNM CTFMs with AuNP FGs assembled using the Langmuir-Blodgett (LB) method. We experimentally confirmed particle-level charge confinement without charge delocalization in closely packed AuNPs. This affords the long retention time of memory devices. FGs assembled using the LB method have a large memory window and high cell-to-cell uniformity. The CTFM array is multiplexed by Si electronics for addressing and data storage in individual cells. The high stability and high reliability of SiNM electronics under ambient conditions enable the realization of an ultrathin, high-density, and

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high-performance wearable CTFM array for practical applications. As a potential application of wearable electronics, this study focuses on monitoring heart rates. By interfacing with wearable Si amplifiers and on-board electrodes, the heart rates after exercise stress tests, as extracted from monitored electrocardiogram (ECG) signals, are processed and stored in CTFMs. The stored data can be retrieved later for the diagnosis of cardiac dysfunctions.

RESULTS

Nanoscale charge confinement in an AuNP FG and its experimental validation

First, an AuNP-based FG cell (insulator-FG-insulator-semiconductor vertical structure) is fabricated (see Materials and Methods) to verify nanoscale charge confinement. A conductive atomic force microscopy (AFM) tip with a 7-V applied potential contacts the top insulation layer of the FG cell [blocking oxide (B_{ox})] and injects charges following predetermined patterns (see Fig. 1A). The potential difference between the AFM tip and the bottom Si substrate facilitates the trapping of electrons in the AuNP FG (see Fig. 1A, inset). Finally, a series of AFM writings finishes the patterned charge injection.

The nanoscale charge confinement in an FG is characterized by the modified AFM measurement. The local electric force produced by confined charges is measured by topographical AFM coupled with electric force microscopy (EFM) data to observe the confined charge pattern (see Fig. 1B, top). The coupled image (EFM and AFM) clearly shows nanoscale charge confinement (minimum linewidth, 70 nm; see Materials and Methods) without lateral charge transport (see Fig. 1B, bottom left), in contrast to a blurred EFM image (see Fig. 1B, bottom middle).

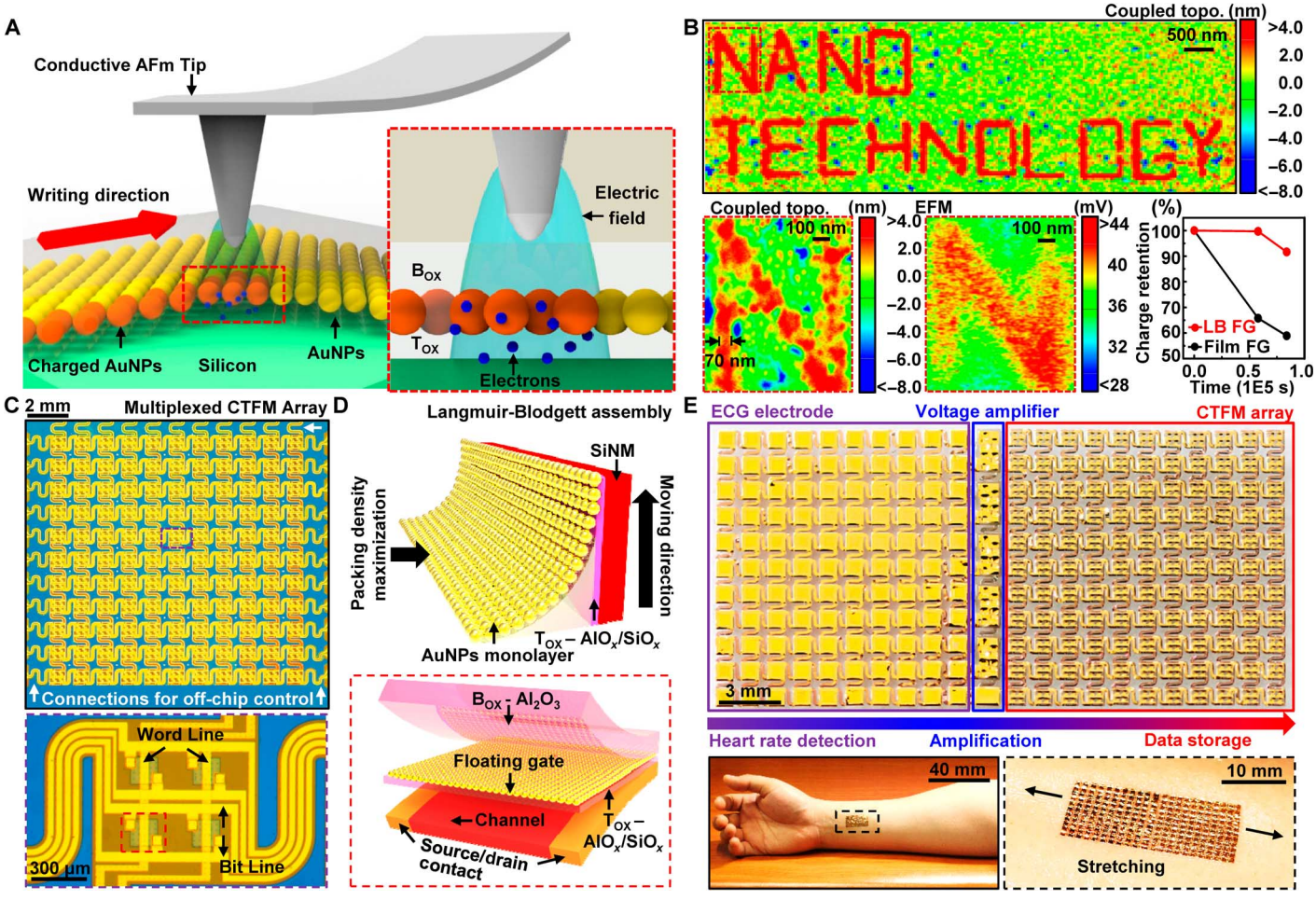

Fig. 1. Characterization of nanoscale charge confinement in AuNP FGs and their large-scale assembly for the wearable CTFM array. (**A**) Schematic showing the process of charge injection to an AuNP FG using a conductive AFM tip. The inset shows the magnified cross-sectional structure of an FG cell (red dashed box) and the charge injection mechanism. (**B**) Representative topographic AFM image coupled with EFM data (top) showing the nanoscale charge confinement capability of AuNPs. Magnified image of the character "N," showing particle-level charge confinement within sub–100-nm width (left bottom, red dashed box) and the corresponding EFM image (middle bottom). Comparison of charge retention characteristics between AuNPs and an Au film (right bottom). (**C**) Photograph of a 22 × 22 wearable multiplexed CTFM array (top). The magnified image shows four memory pixels interconnected with word lines and bit lines (bottom). (**D**) Schematic showing the LB assembly process (top) and a magnified view (bottom) of the channel area of a single CTFM (red dashed box) with AuNP FG assembled using the LB method. (**E**) Representative integrated system composed of a CTFM array, voltage amplifiers, and ECG electrodes (top); its applied form on human skin (bottom left); and its magnified view in stretched mode (bottom right, black dashed box).

The decoupled topographic image of the AuNP FG (see fig. S1A) shows the actual roughness.

We also compare the retention property (see Fig. 1B, bottom right) of the AuNP FG with that of the conventional metal (Au) film FG. The Au film FG only retains ~60% of initially injected charges, whereas the AuNP FG retains more than 90% of the charges, 24 hours after the charge injection. The different retention time originated from the difference in charge-trapping capability between AuNPs and the Au film. The trapped charges can be retained at the surface of AuNPs more efficiently because of the capping ligands that electrically isolate each AuNP (*42*), whereas the trapped charges in the Au film may leak out. The evaluation procedure of contained charges in the FG cell is described briefly in fig. S1B. The efficient particle-level charge confinement of the AuNP FG leads to CTFMs with a long retention time and a large charge storage capacity, which is particularly important for next-generation nanoscale nonvolatile memory devices (*6*).

Integration of CTFM and Si electronics as a wearable system

Figure 1C shows a 22 × 22 CTFM array (top) and its magnified view showing four CTFMs (bottom) (see Materials and Methods). All CTFMs in the array are based on Si transistors and are fully multiplexed, individually accessed, and readily programmed, erased, and read by the off-chip control. The LB method can be used for the large-area fabrication of a closely packed AuNP FG (see Figs. 1D, top, and 2, A and B); this guarantees a highly uniform CTFM performance. The AuNP FG is located between the tunneling oxide (T_{ox}) and B_{ox} (see Fig. 1D, bottom).

Figure 1E shows a wearable CTFM array (top right) with stretchable electrodes (top left) and voltage amplifiers (top middle). The amplifier

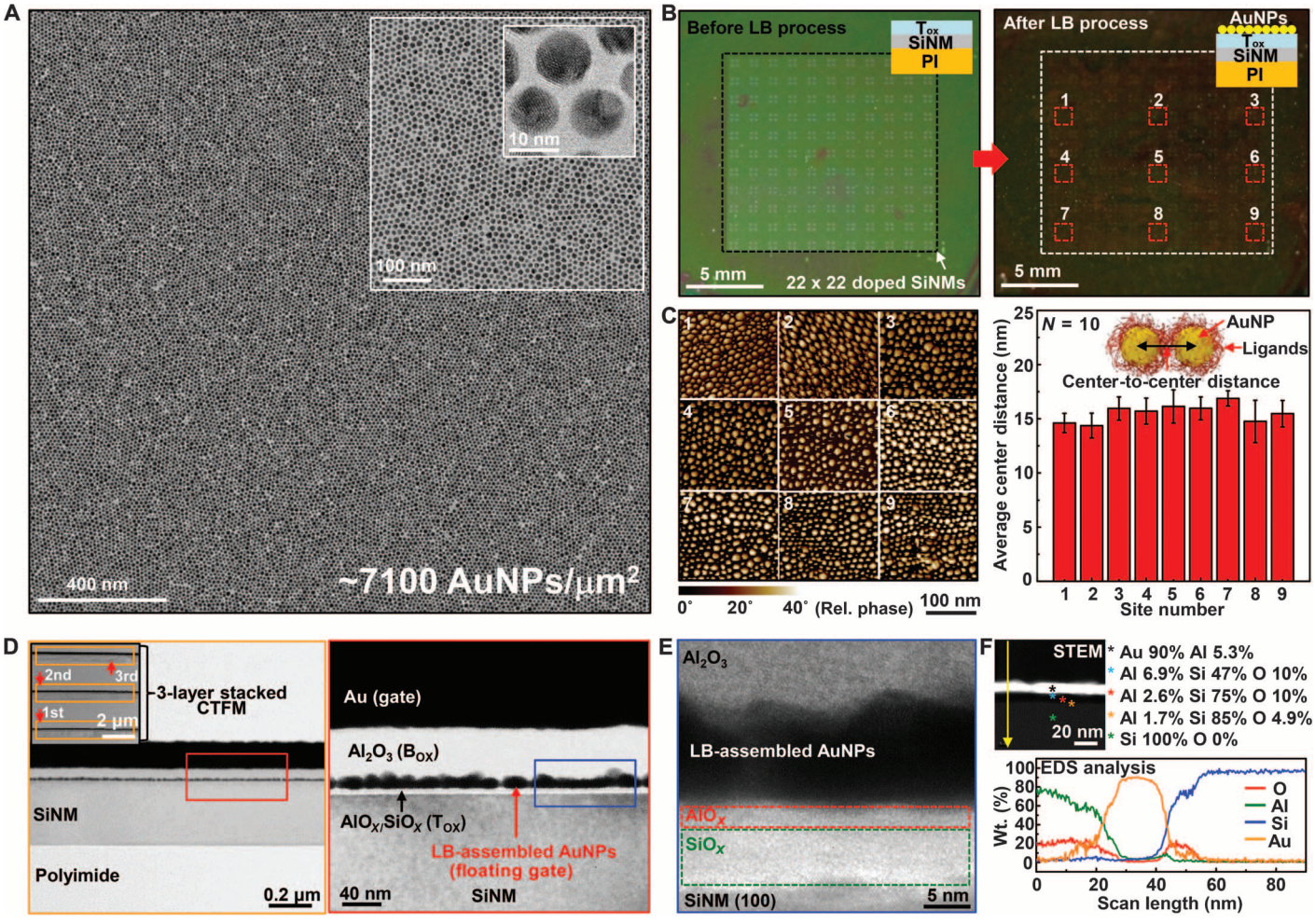

Fig. 2. Large-area and high-density assembly of AuNPs. (**A**) TEM images of AuNPs assembled using the LB method. The insets show magnified TEM images. (**B**) Images before (left) and after (right) LB assembly of AuNPs on T_{ox}. The insets show the corresponding schematics for the cross-sectional structure of the FG cell. (**C**) AFM images and quantitative spatial analysis of AuNPs assembled using the LB method at nine locations [right, red dashed boxes in (B)]. (**D**) TEM images of the CTFM (left). The inset shows a TEM image of the three-layer stacked CTFM. Magnified TEM image showing a detailed cross-sectional structure of the CTFM and uniform AuNP FG embedded in dielectrics (right, red box). (**E**) High-resolution TEM image showing a detailed structure of the dielectric-AuNP interface [blue box in (D)]. (**F**) Scanning TEM (STEM) image showing a cross-sectional structure of the CTFM (top left), quantitative EDS analysis results obtained at the spots marked in the STEM image with colored asterisks (top right), and EDS analysis results obtained along the yellow arrow shown in the STEM image (bottom).

comprises Si pseudo-CMOS inverters (*43*). ECG signals are measured through stretchable electrodes and then amplified by the colocated stretchable amplifiers. Subsequently, the heart rate is extracted from the amplified ECG signals and stored in the CTFMs. The CTFM's ultrathin structure (~5 μm) and serpentine interconnects enable its conformal lamination on the skin under stretched states (see Fig. 1E, bottom). The detailed fabrication procedure is described in Materials and Methods and shown in figs. S2 and S3. The single-crystal nature of Si provides high performance in a multiplexed array.

Uniformity of the large-area AuNP monolayer assembled using the LB method

Figure 2A shows a transmission electron microscopy (TEM) image and magnified views (insets) of the highly uniform and closely packed AuNP monolayer assembled using the LB method. Each AuNP is electrically isolated (minimum spacing, 2 nm) by oleylamine capping ligands, as shown in the highest-magnification TEM image (see the Supplementary Materials). This isolated structure prevents trapped charges from leaking out. The TEM images confirm the high uniformity (in terms of particle size, shape, spacing, and distribution) of AuNPs. To validate macroscale uniformity, 22 × 22 doped SiNMs where T_{ox} is deposited are formed on the polyimide (PI) substrate (see Fig. 2B, left; T_{ox}/SiNM/PI vertical structure, inset), and an AuNP monolayer is assembled on it using the LB method (see Fig. 2B, right; AuNPs/T_{ox}/SiNM/PI vertical structure, inset). The AFM images (see Fig. 2C, left) are collected from nine different locations (red dashed boxes in Fig. 2B). The center-to-center distance of 10 randomly selected AuNP couples (schematic illustration, inset) is measured (see Fig. 2C, right). The results show the uniform macroscale distribution and small standard deviations. This facilitates highly uniform cell-to-cell performance in CTFMs.

Material characterization of the CTFM

To achieve large data storage capacity, multiple CTFM arrays can be stacked (cross-sectional TEM image of three stacked layers; see Fig. 2D, inset) in a manner similar to that in multichip packaging techniques. The magnified TEM image (see Fig. 2D, left) shows the layer information of a single device and uniformly integrated AuNPs. A further magnified view of the red-boxed region in Fig. 2D (see Fig. 2D, right) provides more details of the FG in a CTFM. For example, the spherical morphology of AuNPs is well maintained even after the end of device fabrication. High-temperature processes are avoided to prevent the aggregation of AuNPs (see fig. S4). A further magnified view of the blue-boxed region in Fig. 2D (see Fig. 2E) shows the interfaces around AuNPs that maintain the original topography of the AuNPs.

A STEM image and quantitative material analysis results are obtained by means of energy-dispersive x-ray spectroscopy analysis (EDS; see Fig. 2F, top). The EDS profile shows the material composition and thickness of each layer along the scanned line (yellow arrow). A thin layer of AlO_x/SiO_x (T_{ox}) formed by plasma-enhanced atomic layer deposition (PEALD) and assembled AuNPs are identified (see Fig. 2F, bottom). The EDS results obtained through two-dimensional scanning provide the spatial distribution of specific elements, including Au, Al, and Si, in the cross section of the CTFM (see fig. S5).

Electrical characterization of the AuNP FG

Schematic diagrams illustrating the band structures of the memory capacitor (metal-insulator-FG-insulator-semiconductor vertical structure) under flat band and positive/negative bias conditions are shown in fig. S6. The positive/negative bias corresponds to the program/erase (PGM/ERS) operation. Electrons are trapped in the AuNP FG by tunneling through the T_{ox} during the PGM operation (see fig. S6B, left), whereas trapped electrons can be removed by tunneling back to the Si during the ERS operation (see fig. S6B, right). The tunneling mechanism follows Fowler-Nordheim tunneling (*4*).

Figure 3A shows normalized C-V characteristic curves measured in 30 different memory capacitors. The inset schematically illustrates the device structure and measurement configuration. The AuNP FG (red) assembled using the LB method shows the largest hysteresis among various FGs [chemically adsorbed AuNP (blue) and Au film (10 nm, green) FG]; this confirms that these AuNPs serve as an efficient FG. The cumulative probability plots of FGs as a function of the accumulation capacitance prove that the AuNP FG assembled using the LB method is as uniform as the thermally deposited Au film FG and much more uniform than the chemically adsorbed AuNP FG (see Fig. 3B). We compared accumulation capacitance because it can be easily measured while the device is under the accumulation condition and it largely depends on the uniformity of the FG layer.

To verify the spatially differentiated/patterned charge confinement in the AuNP FG assembled using the LB method, different amounts of charges are injected at different regions in the FG cell through an AFM tip used as a top electrode (see Fig. 3C). EFM images of the FG cell show that the different amounts of charges are well confined in specific areas of the AuNP FG (see Fig. 3D). Their spatial charge distribution is well maintained even after 24 and 72 hours (see fig. S7) from the moment of initial charge injection by virtue of the minimal lateral spreading of the trapped charges in the AuNP-based FG cell.

Electrical and mechanical characterization of wearable CTFMs

The electrical characteristics of the stretchable CTFM array are evaluated by individually addressing multiplexed memory pixels (see the Supplementary Materials). Figure 3E shows the transfer characteristics of a CTFM under multilevel cell (MLC) operations. As the applied bias in PGM/ERS increases, the threshold voltage (V_{th}; indicated by dashed lines in Fig. 3E) shifts right/left (see fig. S8), respectively. The biasing time of the PGM/ERS also affects the V_{th} shift (see Fig. 3F and fig. S9). The ERS requires larger applied voltage and/or longer biasing time than the PGM for the same amount of V_{th} shift. This is because the work function of AuNPs is larger than the electron affinity of Si, which means that larger band bending is required to remove electrons from the FG than to inject them into the FG (see fig. S6, A and B). Figure 3G and fig. S10 show stable charge retention at each voltage level up to 10^3 s. Two states are chosen to observe longer retention (10^5 s; see fig. S11). Further studies on the development of the defect-free T_{ox} that can be formed using low-temperature processes would improve the retention time for long-term data storage. The charge storage of the CTFM is reliable even after up to 10^4 PGM/ERS cycles (see Fig. 3H and fig. S12).

Figure 3I shows a schematic diagram of the NOR-type CTFM array configuration. The electrical disturbances between selected (S; red dashed box) and peripheral (P_a to P_c; blue dashed box) memory pixels are investigated. When the memory pixel S is at the erased/programmed state, coapplied inhibition biases on the bit line/word line minimize the disturbances on the memory pixel S during the PGM/ERS operation of the peripheral memory pixels (see Fig. 3, J and K, and fig. S13). The reliable MLC operation of the CTFM array at each voltage level is confirmed by the cumulative probability data of the sampled

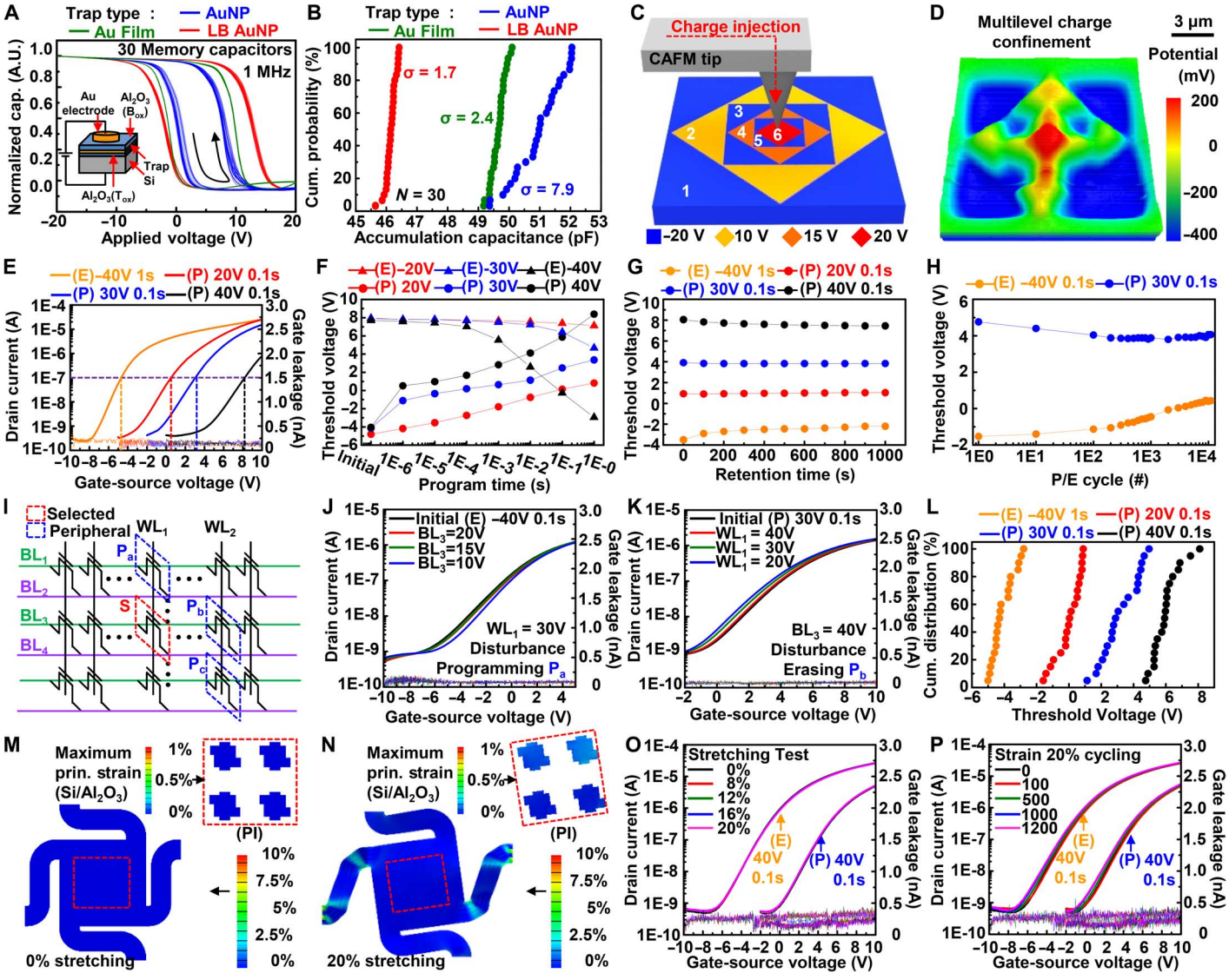

Fig. 3. Electrical and mechanical characterizations of an AuNP CTFM. (**A**) Capacitance-voltage (C-V) hysteresis curves of FG cells containing different FGs, obtained from 30 FG cells of each FG. The amplitude of the applied AC signal is 30 mV, and its frequency is 1 MHz. The inset shows a schematic of the experimental setup. (**B**) Cumulative probability data of accumulation capacitances of the FG cells containing different FGs. (**C**) Schematic of experimental setup for two-dimensional injection of different amounts of charges into the AuNP FG assembled using the LB method. The numbers indicate the sequential order of charge injection performed with different bias conditions. (**D**) EFM image of the FG cell containing different amounts of charges at different locations by two-dimensional injection of charges. (**E**) Transfer characteristics of a CTFM pixel after PGM/ERS operation with different voltages, showing four states. (**F**) PGM/ERS speed characteristics of the CTFM pixel with different operation voltages. (**G**) Retention characteristics of the CTFM pixel for each possible state. (**H**) Endurance characteristics of the CTFM pixel. (**I**) Schematic of the CTFM array in NOR configuration. Dashed boxes indicate the selected memory pixel (red) and manipulated peripheral pixels (blue) for a disturbance test verifying the degree of influence on the electrical state of the selected pixel, induced by manipulation of the peripheral pixels. (**J**) Transfer curves measured from the erased memory pixel of the initial condition and the inhibited condition in which the PGM bias on WL_1 for manipulating the P_a pixel and different inhibition biases on BL_3 are applied simultaneously. (**K**) Transfer curves measured from the programmed memory pixel of the initial condition and the inhibited condition in which the ERS bias on BL_3 for manipulating the P_b pixel and different inhibition biases on WL_1 are applied simultaneously. (**L**) Cumulative probability data of the multilevel states obtained from 20 memory pixels. (**M** and **N**) FEA results showing the distribution of the maximum principal strain on the entire structure and active region (inset) of the CTFM array [strain of (M), 0%; strain of (N), 20%]. (**O** and **P**) Transfer curves of the CTFM pixel after conducting PGM/ERS operation under (O) various applied strains and (P) various stretched cycles of 20% strain.

pixels (see Fig. 3L). A slight V_{th} distribution may exist owing to the difference in interconnection resistance between memory pixels close to and far from the voltage source.

The mechanical reliability of CTFMs is confirmed through cyclic stretching tests (see fig. S14). Finite element analysis (FEA) of the induced strain distribution shows that memory pixels (red dashed boxes in Fig. 3, M and N) under ~20% stretching have negligible strains [~0.2%; cf. fracture strain of Si, ~1% (*44*); fracture strain of Al_2O_3, ~1% (*45*)] (see the Supplementary Materials). Serpentine interconnections accommodate most of the applied strain (see Fig. 3, M and N). The PGM/ERS of CTFMs is conducted under various applied strains (see Fig. 3O) and after repetitive stretching up to 1200 cycles (see Fig. 3P; ~20% strain). In both cases, performance degradation is negligible. Considering that the allowed strain of the human epidermis is ~20% (*35*), the current level of mechanical reliability is suitable for many wearable applications.

Electrical and mechanical characterization of the wearable Si amplifier

To acquire the heart rate, a pseudo-CMOS inverter composed of four n-type MOS transistors (see Fig. 4A) is used to amplify ECG signals (see the Supplementary Materials). The amplifier's output voltage (V_{OUT}) with respect to the input voltage (V_{IN}) under various bias conditions (V_{SS}, V_{DD}) is plotted in Fig. 4B and fig. S15A (solid lines and dashed

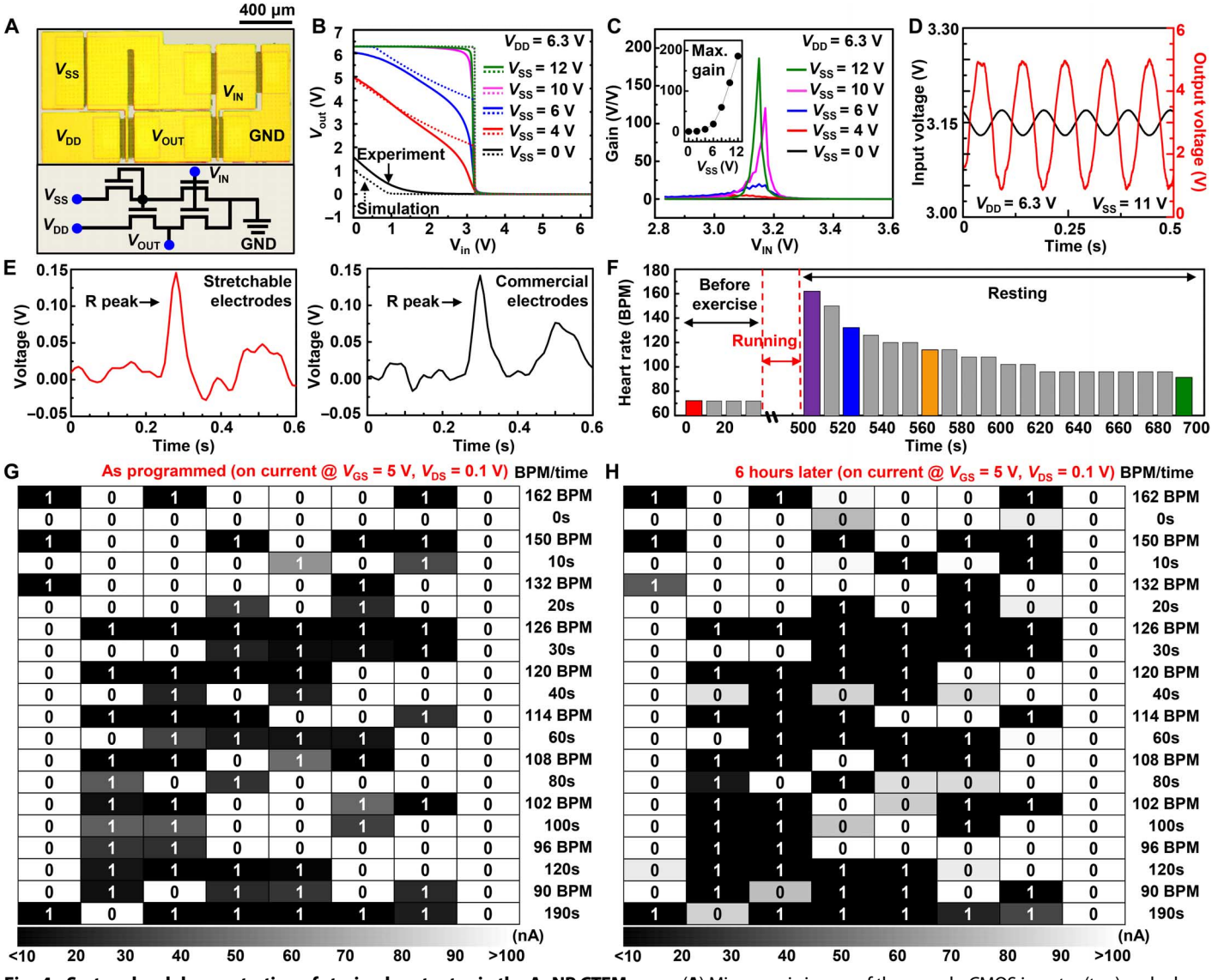

Fig. 4. System-level demonstration of storing heart rates in the AuNP CTFM array. (**A**) Microscopic image of the pseudo-CMOS inverter (top) and schematic circuit diagram (bottom). (**B**) Voltage transfer characteristics of the pseudo-CMOS inverter (dashed line, simulation results; solid line, experimental results) with various biasing voltages (V_{SS} when V_{DD} is fixed to 6.3 V). (**C**) Signal gain of the inverter measured with respect to the input voltage (V_{IN}) under various biasing conditions (V_{SS} when V_{DD} is fixed to 6.3 V). The inset shows the maximum gain with respect to V_{SS}. (**D**) Sinusoidal input signal (black, 40 mV_{p-p}, 10 Hz) and output signal (red) amplified by the pseudo-CMOS inverter. (**E**) ECG signal containing a single R peak acquired using fabricated stretchable electrodes (left) and commercial electrodes (right). (**F**) Measured temporal change of the resting heart rate before exercise and after exercise. (**G** and **H**) Heart rate recovery data and corresponding elapsed time data retrieved from the CTFM array: (G) immediately after data storage and (H) 6 hours after data storage.

lines denote experiment and simulation, respectively). The simulations are based on data of a single transistor (see fig. S15, B and C). The design parameters of the pseudo-CMOS inverter are shown in fig. S16A. The amplifier gain increases with V_{SS} (see Fig. 4C). The maximum amplification gain is ~200 (inset) at a V_{IN} of 3.17 V (V_M) and a V_{SS} of 12 V. The other characteristics of the pseudo-CMOS inverter, such as the noise margins, are also measured/calculated and shown in fig. S16 (B and C) and summarized in table S1.

Figure 4D shows the input sinusoidal signal (40 mV_{p-p}) and filtered output signal (~4 V_{p-p}) amplified by the wearable Si pseudo-CMOS inverter. The low effective gain (~100; that is, lower than the maximum) is caused by the deviation of the input signal from V_M. The decreased deviation of the input voltage from V_M results in a higher effective gain (see fig. S17A). The pseudo-CMOS inverter amplifies the ECG signal (<4.5 mV_{p-p}) with an effective gain of 100 or higher. The frequency response shows that a high effective gain can be maintained during ECG signal amplification because of the relatively low frequency of ECG signals (<5 Hz; see fig. S17B).

To verify mechanical reliability, the amplifier is electrically characterized under stretched conditions (see fig. S18, A and B). FEA shows that an applied strain of ~20% induces a negligible strain of <0.2% in active regions (red dashed box in fig. S18, C and D). The voltage transfer curves of the pseudo-CMOS inverter are obtained under various strains (0 to 20%), in which negligible changes are observed (see fig. S18E). Stretching tests up to 1000 cycles are performed and only minimal shifts in the voltage transfer curve are observed (see fig. S18F).

Monitoring ECGs using amplifiers and storage of heart rates in a memory array

It is important to monitor heart rate recovery to diagnose abnormal cardiovascular parasympathetic functions, as recovery is determined by the reactivated parasympathetic control that usually occurs within 30 s after the end of exercise (*46*). In this regard, we demonstrate the storage of heart rate recovery data that were recorded and amplified using wearable electrodes and amplifiers, respectively, for 200 s after exercise.

A schematic of the sequential procedures comprising ECG signal acquisition, on-site amplification, heart rate measurement, and data storage/retrieval to and from the CTFM array (see the Supplementary Materials) is depicted in fig. S19A. The heart rate and elapsed time data are converted into 8-bit binary data and stored in rows of the CTFM array (see fig. S19B). The amplified ECG signals measured by wearable electrodes and commercial electrodes are shown in Fig. 4E and fig. S20 (A and B). There is no significant difference between these two. Although it is difficult to distinguish P, Q, and S features from the amplified ECG signals, the heart rate can be reliably extracted by detecting the relatively evident R peaks. For better signal quality, additional noise reduction filters and circuits can be integrated in future work. The heart rate recovery of a volunteer is monitored using wearable electrodes and amplifiers (fig. S20C). Immediately after the exercise, the heart rate increased from 72 to 162 beats per minute (BPM) and then continuously decreased to 90 BPM (Fig. 4F and fig. S20C).

PGM/ERS biases are applied to the selected row of the CTFM array to store the heart rate recovery data shown in Fig. 4F. The stored data in the CTFM array can be read easily after data storage; Fig. 4G shows the data storage map. White boxes indicate erased memory pixels storing the binary number "0" and black boxes indicate programmed memory pixels storing the binary number "1." After 6 hours, the stored data are read again, and the retrieved data are found to be exactly the same; this indicates the good retention property of the CTFM array (see Fig. 4H). The stored data contain the heart rate and elapsed time encoded in binary numbers; these data can be converted to decimal numbers to enable medical personnel to check the wearer's heart rate recovery history.

DISCUSSION

Future wearable systems that pursue mobile healthcare monitoring and data analysis based on high-performance bioelectronics should monolithically integrate various stretchable electronic components, such as sensors, amplifiers, and memory modules. However, there have been limited studies for system-level demonstrations using high-performance, stretchable, nonvolatile memory and related electronic devices.

Here, we demonstrated reliable data storage of heart rates, which are obtained from ECG signals amplified by colocated stretchable Si amplifiers to the wearable nanocrystal memory. The stretchable, high-density, and ultrathin memory array with the enhanced charge storage capability has great potential for various wearable electronics applications. Appropriate materials and design strategies using SiNM electronics as well as uniformly assembled AuNPs enable the realization of a wearable, high-performance, nonvolatile memory array. In particular, the large-area uniform assembly of AuNPs forms an efficient FG, which enhances the data storage capacity, retention property, and performance uniformity in the memory array. To validate the superior charge confinement capability of AuNPs, we developed the modified AFM technique, which visualizes confined charges with nanoscale resolution.

The advances in characterization and fabrication technologies reported in this paper will be an important stepping stone that will pave the way to a fully integrated wearable system composed of the stretchable nanocrystal FG memory and other stretchable Si electronics toward mobile and personalized health monitoring.

MATERIALS AND METHODS

Fabrication of the FG cell

The fabrication of the FG cell shown in Fig. 1 (A and B) began with the dry oxidation process of a Si wafer to grow a 5-nm-thick SiO_2 T_{ox} layer. The AuNP FG assembled using the LB method was then coated on T_{ox}. An Al_2O_3 B_{ox} layer (7 nm) was deposited on the AuNP FG using the PEALD process (150°C, 50 cycles). To compare retention characteristics, an Au film (26 nm) FG and a three-layer AuNP (~26 nm) FG were used. Generally, the thermal deposition of an Au film whose thickness is below 10 nm is difficult to achieve. Au deposition of less than 10 nm normally leads to the formation of islands, which makes it difficult to represent Au film characteristics (*11*). Therefore, we used a thicker Au film (~26 nm). For a valid comparison, similar thickness of assembled AuNPs (three-layer AuNPs) was used. At the same time, the fabrication of the FG cell shown in Fig. 3 (C and D) and fig. S7 began with the deposition of Al_2O_3 on a Si wafer using 50 cycles of the PEALD process (250°C) to form T_{ox}. Then, the AuNP FG was assembled on T_{ox} by using the LB method, and 350 cycles of the PEALD process (150°C) were subsequently conducted to form B_{ox}.

Charge confinement characterization in the FG cell

Nanoscale/microscale charge injections and measurements on the FG cell were conducted using AFM (XE7, Park Systems) with EFM.

The AFM lithography program (XEL, Park Systems, for data shown in Fig. 1B) or manual manipulation (for data shown in Fig. 3D) was used to pattern and generate a potential difference between an AFM tip and the bottom electrode for nanoscale/microscale patterned charge injection to the FG cell using the contact mode of the AFM. The AFM topography and EFM images were retrieved simultaneously by applying AC bias to a Pt/Cr-coated tip (tip radius, <25 nm; Budget Sensors Multi75E). Sinusoidal AC bias with a frequency of 14.6 kHz and a peak-to-peak amplitude of 1 V was applied to acquire topological data and EFM images using the noncontact mode of the AFM. The coupled topography with EFM data can be observed by adjusting the frequencies of AC bias and noncontact resonant. It was obtained by coupling the van der Waals force and electric force between the AFM tip and the surface of the FG cell, and it showed superior spatial resolution in illustrating a charge-containing area. The decoupled topography can also be obtained by fine-tuning the frequencies of the tip vibration and AC bias.

Fabrication of the CTFM array

During the fabrication process, first, a p-type silicon-on-insulator (top silicon, 340 nm; Soitec) wafer was doped by ion implantation (R_P, 50 nm; dose, 1×10^{16} ions/cm^2; phosphorus) to define the n-type source and drain regions. After doping, the top SiNM was transferred onto a PI film (thickness, 2 μm) coated on an SiO_2 wafer. By using reactive ion etching (RIE; SF_6 plasma) with photolithography, the active regions of the SiNM were isolated. The AlO_x/SiO_x T_{ox} layer was formed on the SiNM using the PEALD process (250°C, 50 cycles). In contrast to the FG cell, a monolayer of AuNPs was subsequently deposited on the entire T_{ox} area by using the LB method for efficient and reliable fabrication processes. After that, the AuNPs were patterned by photolithography and wet etching and confined to the channel area of the SiNM. The Al_2O_3 B_{ox} layer was subsequently deposited using the PEALD process (150°C, 350 cycles). The Al_2O_3 layers (T_{ox} and B_{ox}) were patterned by photolithography and wet etching using a diluted hydrogen fluoride solution (2%). To form the word lines, deposition of the metal film using thermal evaporation (Au/Cr, 100 nm/7 nm), photolithography, and wet etching processes were conducted in sequence. To electrically isolate the word lines, SU-8 2 (thickness, 1 μm; MicroChem) was coated. The SU-8 layer was then photolithographically patterned to form vertical interconnect accesses (VIAs). Bit lines were deposited by thermal evaporation (Au/Cr, 150 nm/7 nm), patterned by photolithography, and subsequently wet etched to contact the source/drain regions through the VIAs. After the top PI layer (thickness, 1 μm) was coated and annealed, the entire structure (PI/device/SU-8 2/PI) was patterned and etched by RIE (O_2 plasma). As a final step, the entire device was detached from the SiO_2 wafer and transferred onto a polydimethylsiloxane substrate.

SUPPLEMENTARY MATERIALS

Supplementary material for this article is available at http://advances.sciencemag.org/cgi/content/full/2/1/e1501101/DC1

Text

Fig. S1. Original data corresponding to Fig. 1B.

Fig. S2. Fabrication process of the CTFM array.

Fig. S3. Fabrication process of the pseudo-CMOS inverter array.

Fig. S4. TEM images of AuNP FG assembled using the LB method after the B_{ox} deposition using the PEALD process.

Fig. S5. TEM-EDS analysis of AuNPs embedded in an FG cell.

Fig. S6. Energy band diagrams of CTFM under three representative bias conditions.

Fig. S7. EFM images of the FG cell containing different amounts of charges at different locations according to the elapsed time after charge injection.

Fig. S8. PGM/ERS characteristics with operation voltages.

Fig. S9. PGM/ERS speed analysis of the CTFM array.

Fig. S10. Retention characteristics of a CTFM pixel for different memory states.

Fig. S11. Retention characteristics of the programmed state (30 V, 0.1 s) and the erased state (−40 V, 0.1 s).

Fig. S12. Changes in the transfer curves of a CTFM pixel after repetitive PGM and ERS cycles.

Fig. S13. Changes in transfer curves of a CTFM pixel (selected one) after programming or erasing peripheral ones.

Fig. S14. Stretching test of the CTFM pixels.

Fig. S15. Characteristic curves/simulation results of the pseudo-CMOS inverter and a transistor.

Fig. S16. PSpice simulation and experimental results of the pseudo-CMOS inverter.

Fig. S17. Effective gain and frequency response of the pseudo-CMOS inverter.

Fig. S18. Stretching test of the pseudo-CMOS inverter.

Fig. S19. Demonstration procedures and data storage scheme.

Fig. S20. Real-time monitoring of amplified ECG signals.

Table S1. Noise margins of the pseudo-CMOS inverter.

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