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이학박사 학위논문

**Optoelectronic characteristics of MoS₂
phototransistors with organic or van der
Waals heterostructures**

유기물 혹은 반데르발스 접합을 통한
이황화몰리브덴 포토트랜지스터의 광전기적
특성 연구

2019년 8월

서울대학교 대학원

물리·천문학부 물리학전공

박진수

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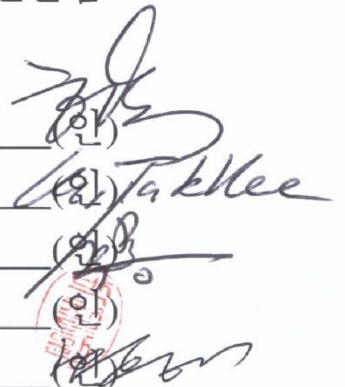
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Abstract

Optoelectronic characteristics of MoS₂ phototransistors with organic or van der Waals heterostructures

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In this thesis, the optoelectronic characteristics of MoS₂ phototransistors are mainly studied. The major reason of exploring the optoelectronic characteristics of 2D materials-based phototransistors, not of photodiodes, during my doctorate course is because 2D materials cannot absorb significant amount of light and they have considerably high exciton binding energy, originating from their atomically thin thickness. These features suppress the optoelectronic performance in the perspective of 2D materials-based photodetectors. However, the phototransistor can amplify the photodetection capability by employing the external electric fields, such as drain-source voltage and gate-source voltage.

After introduction of my thesis work in Chapter 1, in Chapter 2 I will summarize a research result of improving photosensitivity of MoS₂ phototransistors conducted in 2014 as my first research topic. I demonstrated that a surface treatment with organic materials on MoS₂ could improve the photoresponsivity and photoswitching characteristics. In addition to the exploration for improving optoelectronic performance, I became interested in the intrinsic optoelectronic characteristics of 2D materials during my doctorate course. In Chapter 3, I summarize the intrinsic optoelectronic characteristics of fully transparent MoS₂ phototransistors employing

a van der Waals heterostructure. And, in Chapter 4, the effects of p-doping on optoelectronic characteristics of WSe₂ phototransistors are explained.

Because of the nature of phototransistors using external electric fields for amplifying the optoelectronic performance, I studied the electrical and optoelectronic phenomena of 2D-based phototransistors under the high electric fields. I have discovered the interesting electrical phenomena in MoS₂ transistors under the high electric fields in the process of arranging for the experimental setup for studying optoelectronic characteristics. However, I could not finish this research on the optoelectronic characteristics under the high electric fields due to the insufficient time. I summarized the thickness-dependent avalanche breakdown phenomena and charge trapping dynamics under the high electric fields in Chapters 5 and 6.

Keywords: Two dimensional materials, Transition metal dichalcogenides, Molybdenum disulfide, Optoelectronic characteristics, Internal responsivity, Avalanche breakdown, High electric field

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This work is dedicated to my loving fiancé Seuri and our family.

사랑하는 가족과 스리에게 감사를 표합니다.

Chapter 1. Introduction

1.1. Brief introduction of TMDs and MoS₂

Beginning with extensive research on graphene, selected as 2010 Nobel Prize in Physics, the emergence of a new class of atomically thin two-dimensional (2D) materials has opened up a new era for fundamental scientific studies and the next generation of electronics.¹⁻⁴ Figure 1.1.1 shows the diverse 2D materials and corresponding their band gap energy. Among the various transition metal dichalcogenides (TMDs) 2D materials, molybdenum disulfide (MoS₂) has been widely researched as a 2D-based field-effect transistors (FETs) and has exhibited outstanding electrical properties.⁵ In contrast to graphene which lacks an intrinsic band gap, MoS₂ has a thickness-dependent band structure (a direct band gap of 1.9 eV as a monolayer and an indirect band gap of 1.2 eV as a bulk MoS₂). This existence of an intrinsic band gap enables the MoS₂ to be employed as a salient component of various applications such as FETs,⁵ memories,⁶ logic circuit devices,⁷ sensors,⁸ and photodetectors⁹.

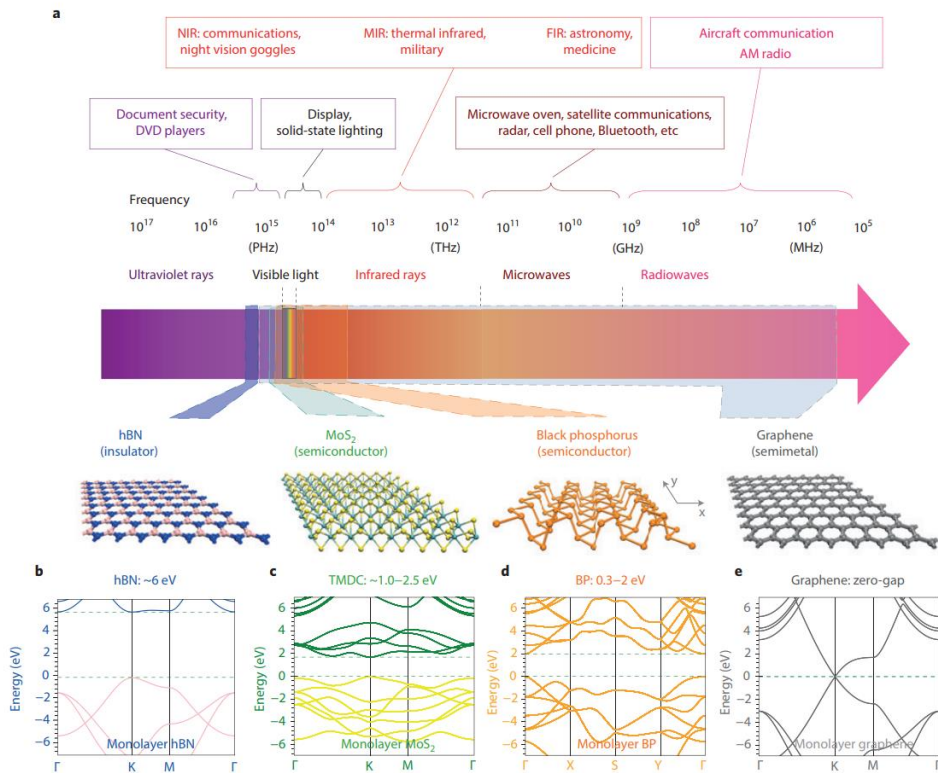


Figure 1.1.1. Introduction of various 2D materials covering a broad spectral range. (a) Applications that utilize the different spectrum ranges are introduced in the top portion of the panel. The schematics of *h*-BN, MoS₂, BP, and graphene. (b-e) Band structures of monolayer *h*-BN, MoS₂, BP, and graphene.

1.2. Optoelectronic characteristics of MoS₂ and a MoS₂-based heterostructure for enhancing photosensitivity

Especially appropriate band gap energy of MoS₂ in the visible spectrum region, high photodetection capability,¹⁰ outstanding electrical stability¹¹ and flexibility¹² suggest that its high potentiality for realizing ideally transparent and flexible photodetectors. Recently beyond the researches on the sole MoS₂-based

photodetectors, its heterostructures with organic materials^{13,14} or other 2D materials¹⁵⁻¹⁷ have been designed to enhance photodetection and photoswitching abilities. The mechanism of enhancing photodetection capabilities by employing a heterostructure is as following: when a MoS₂ forms the heterostructure with other materials, the photogenerated carriers can be separated easily due to the different energy band structures, thus this can lead to improved photocurrent with suppressing the disappearance of photogenerated carriers via recombination processes. In this thesis, a facile and effective method for improving photoresponsive and photoswitching characteristics by stacking an organic material with thermal evaporation system will be discussed in Chapter 2.

1.3. Intrinsic optoelectronics of MoS₂ phototransistors

Although numerous researches of the optoelectronic performance of 2D-based photodetectors heterostructured with organic materials or other 2D materials, from now on, the intrinsic optoelectronic characteristics of MoS₂ has not been investigated. This is because most previous researches have employed opaque substrates, for example most commonly used heavily-doped Si with SiO₂ for the convenience from a manufacturing perspective. The opaque substrates cause the multiple reflections of incident light resulting in the generation of additional photogenerated carriers. In addition, this unintended interference causes a strong photogating effect due to the trapping of photogenerated holes at the low-quality interface, which can overestimate the ability of the photoresponsivity of MoS₂. For a better understanding of MoS₂, the systematic investigation of the intrinsic optoelectronic characteristics

of monolayer MoS₂ was highly required without effects caused by external interference such as reflected or refractive light. These intrinsic optoelectronic results of the MoS₂ phototransistor will be introduced in Chapter 3.

1.4. Electrical characteristics of MoS₂ under high electric fields

In this thesis, the electrical characteristics of MoS₂ FETs under high lateral electric fields were also dealt with as a subtopic. During my doctorate course, this subtopic regarding the electrical characteristics of MoS₂ under the high electric field is also substantially significant, because a terminal goal of my doctorate course was the exploration of the optoelectronic phenomena beyond only electrical studies of TMDs under the high electric fields. Unfortunately, I could not finish the research on optoelectronic characteristics of 2D materials-based phototransistors under the high electric fields due to the insufficient time. However, I have discovered the interesting electrical phenomena in MoS₂ FETs under the high electric fields in the process of arranging for the experimental setup for studying optoelectronic characteristics. Therefore, we systematically explored the avalanche breakdown phenomena in MoS₂ FETs, which is highly dependent on the thickness of MoS₂ layer. Interestingly, this thickness-dependent electrical behavior under the high electric fields had not been explained in 2D system before we did. This research will be discussed in Chapter 5. Furthermore, charge trapping and detrapping phenomena at the interface between MoS₂ and SiO₂/Si substrate were observed, and it was found that those phenomena can be modulated by the range of the applied lateral electric fields. This charge trapping phenomenon is dealt with in Chapter 6.

1.5. Outline of this thesis

This thesis mainly focuses on the optoelectronic characteristics of MoS₂ phototransistors. The major reason of exploring the optoelectronic characteristics of 2D materials-based phototransistors, not of photodiodes, during my doctorate course is because 2D materials could not absorb an amount of light and they have the considerably high exciton binding energy originating from their atomically thin thickness. Both factors can suppress the high optoelectronic performance in the perspective of photodetectors. However, in spite of the low light absorption and high exciton binding energy of 2D materials, the optoelectronic characteristics can be amplified by the applied external electric fields, such as drain-source voltage (V_{DS}) and gate-source voltage (V_{GS}).

In Chapter 2, the researches on enhanced optoelectronic characteristics of MoS₂ phototransistors via the surface treatment with organic material (copper phthalocyanine (CuPc)) are discussed. Through this facile surface treatment by thermal evaporator system, not only photoresponsivity and but also photoswitching characteristics can be improved. In Chapter 3, beyond the perspective of optoelectronic performances, the intrinsic optoelectronic characteristics of MoS₂ phototransistors were investigated, such as internal responsivity, internal quantum efficiency, and internal detectivity. Besides, similar to MoS₂, the effects of *p*-doping on electrical and optoelectronic characteristics of WSe₂ phototransistors are discussed in Chapter 4. Furthermore, the interesting phenomena of MoS₂ FETs under the high lateral electric fields, such as thickness-dependent avalanche breakdown and charge trapping dynamics at the interface of MoS₂/SiO₂ are introduced in

Chapter 5 and 6, respectively. In fact, I wished to investigate the optoelectronic characteristics of 2D materials-based phototransistors under high electric field as an ultimate research topic of my doctorate course, but I could investigate only the electrical properties under the high electric fields due to the insufficient time. However, I believe I partially established the foundation for exploring optoelectronic characteristics under high electric fields, and convinced there is going to be an interesting phenomenon at the end of this study.

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Chapter 2. Optoelectronic characteristics of MoS₂ phototransistors via vertical heterostructure with organic material

In this Chapter, the optoelectronic characteristics of MoS₂ phototransistors when stacking a p-type organic semiconductor (CuPc) layer on the MoS₂ surface are introduced. The CuPc/MoS₂ hybrid devices exhibited better performance as photodetectors compared with the pristine MoS₂ FETs that did not contain CuPc layers, due to the transfer of photo-generated charge carriers from the CuPc to the MoS₂. Furthermore, we observed that the photoresponsive properties of the CuPc/MoS₂ devices depended on the thickness of the CuPc layer. The device with a relatively thinner CuPc layer exhibited a better photodetection performance than that with a relatively thicker CuPc layer, which can be explained by the CuPc layer thickness-dependent interlayer recombination processes across the CuPc/MoS₂ interface. We found that the 2 nm-thick CuPc/MoS₂ device presented the highest photodetection performance. Besides, photoswitching response times (rise and decay times) of CuPc/MoS₂ heterostructure were also improved, which was attributed to the passivation effect preventing the absorption of oxygen on the surface of the MoS₂ channel. This researches may provide a promising route for ultra-thin and highly sensitive MoS₂-based photodetectors.

2.1. Introduction

Recently, transition metal dichalcogenide (TMDs) two-dimensional (2D) materials have gained considerable interest as a candidate for next-generation nanoelectronic devices.¹⁻⁶ TMDs 2D materials have demonstrated several advantageous features, such as a thickness-dependent electronic band structure, high photoconductivity, high transparency, and flexibility in fabricating nanoelectronic devices. Among the various TMDs materials, MoS₂ has been widely researched as a 2D FET and has exhibited outstanding electrical properties, including a low subthreshold swing value, a high on/off ratio, and good carrier mobility.⁷⁻⁹ In contrast to graphene which lacks an energy band gap, MoS₂ has a direct band gap of 1.8 eV as a single layer and an indirect band gap of 1.2 eV as a bulk material.¹⁰⁻¹⁴ Therefore, many studies have used MoS₂ to fabricate transistors,¹⁵⁻¹⁸ memory,^{19,20} logic circuit devices,^{21,22} sensors,^{23,24} and phototransistors.^{25,27-29} Graphene has also been studied for phototransistors for application in photosensitive devices, but graphene-transistor-based photodetectors have a limited photoresponsivity ($\sim 6 \text{ mAW}^{-1}$) due to graphene's low light absorption coefficient and the fast photoinduced carrier recombination rate.²⁶ In contrast, photodetectors made with MoS₂ have exhibited excellent photoresponse properties. For example, devices based on single- and multilayer MoS₂ films have demonstrated photoresponsivities up to 880 AW^{-1} (ref. 27) and $\sim 0.1 \text{ AW}^{-1}$,^{28,29} respectively. Beyond the structures of MoS₂ FET alone, it has been demonstrated that through stacking of other materials, MoS₂-based heterostructures can result in higher photoresponsivity.³⁰⁻³⁵ For example, Kufer *et al.* demonstrated that the photoresponsivity of MoS₂ was enhanced by stacking *p*-type PbS quantum dot materials on an MoS₂ surface due to the photo-generated charge

transfer from the stacked *p*-type PbS quantum dots to MoS₂.³⁵ If *p*-type materials are to be used for heterostructure MoS₂-based photodetectors, organic materials can be a good choice because *p*-type organic semiconductor layers have been extensively studied and can be easily stacked on 2D films by spin-coating or deposition systems, and the thickness of the organic layer on 2D films can be accurately controlled. Among organic materials, CuPc is a *p*-type organic semiconductor that has been widely used in organic and hybrid optoelectronic devices.³⁶ The structural properties of the CuPc layer on the MoS₂ surface have been studied. For example, molecular orientation properties of the CuPc layer on the MoS₂ were studied using angular resolved ultraviolet photoemission spectroscopy or atomic force microscopy,³⁷ and a Raman enhancement effect of the CuPc/MoS₂ was reported.³⁸ However, the effects of the CuPc hybrid structures on the MoS₂-based phototransistors have not yet been examined. Importantly, as the device consisted of a heterostructure with *n*-type MoS₂ and *p*-type CuPc materials, the efficiency of photoresponse can strongly depend on the thickness of the organic layer. In this study, we have characterized the electrical and photoresponsive properties of MoS₂ FET-based photodetectors. We investigated and compared the photodetection characteristics of MoS₂ FETs before and after the devices were stacked with *p*-type organic semiconductor (CuPc) layers on the MoS₂ surface. By varying the thickness of the CuPc layers, we found an optimized condition for achieving higher photoresponsivity in the CuPc/MoS₂ hybrid device structures.

2.2. Experiments

2.2.1. Device fabrication process

Figure 2.1 shows the device fabrication processes. First, MoS₂ flakes were mechanically exfoliated from a bulk MoS₂ crystal purchased from SPI Supplies. Then, the MoS₂ flakes were transferred on 270 nm-thick SiO₂ on a highly doped p⁺⁺ Si Wafer (resistivity $\sim 5 \times 10^{-3} \Omega/\text{cm}$) that can be used as a back gate. Proper MoS₂ flakes were located with an optical microscope and the height of selected MoS₂ flakes were measured with atomic force microscope (NX 10 AFM system, Park Systems). To make electrode patterns, we spin-coated methyl methacrylate (9% concentration in ethyl lactate) and PMMA 950K (5% concentration in anisole) at 4000 rpm. After the spin-coating of each layer, the sample was baked at 180 °C for 90 s on a hot plate. We used an electron beam lithography system (JSM-6510, JEOL) to pattern electrodes. Development of patterns was performed with a MIBK/IPA (1:3) solution for 50s. Electrodes was made by depositing Ti with an e-beam evaporator (KVE-2004L, Korea Vacuum Tech). Finally, the CuPc was deposited on fabricated MoS₂ field effect transistor (FET) devices by a thermal evaporator (GVTE1000, GV-Tech).

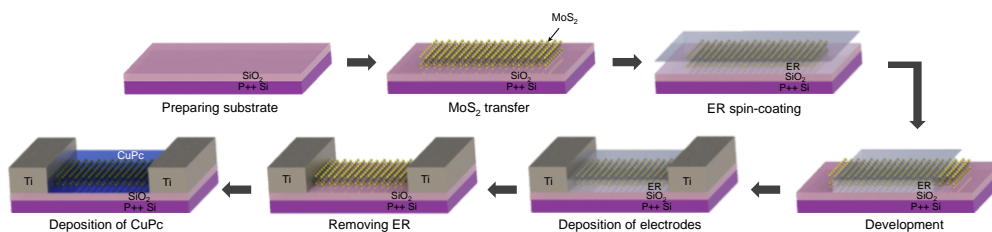


Figure 2.1. Schematic of fabricating processes of MoS₂ FET

2.3. Results and discussions

2.3.1. Electrical characteristics of MoS₂ FETs

Figure 2.2a shows the optical images of a MoS₂ flake and its device fabrication into a MoS₂ FET. Here, MoS₂ flakes were mechanically exfoliated from a bulk MoS₂ crystal and transferred onto a 270 nm-thick SiO₂ layer on a heavily doped p⁺⁺ Si substrate that can be used as a back gate of FETs. Then, Ti metal (30 nm thick) patterns were made into the source and drain electrodes using electron-beam lithography to form ohmic contacts. Since Ti electrode has a relatively lower work function (~ 4.3 eV) than the work function of MoS₂ (4.5 to 5.2 eV), it can form ohmic contact with MoS₂.³⁹ Figure 2.2b displays an atomic force microscopy (AFM) image of a MoS₂ FET. The thickness of the MoS₂ flake channel was found to be ~ 3.2 nm, corresponding to 5 layers of the MoS₂ film (the thickness of a single-layer MoS₂ film is 0.65 nm). We fabricated MoS₂ FETs using 3 to 6 nm-thick MoS₂ flakes, corresponding to 5 to 9 layers. After fabricating the MoS₂ FETs, the CuPc organic material was deposited on the MoS₂ surface using a thermal evaporator. Figure 2.2c illustrates the schematics of a CuPc/MoS₂ photodetector illuminated by a visible light laser. The molecular structures of the MoS₂ and CuPc are also shown in Figure 2.2c.

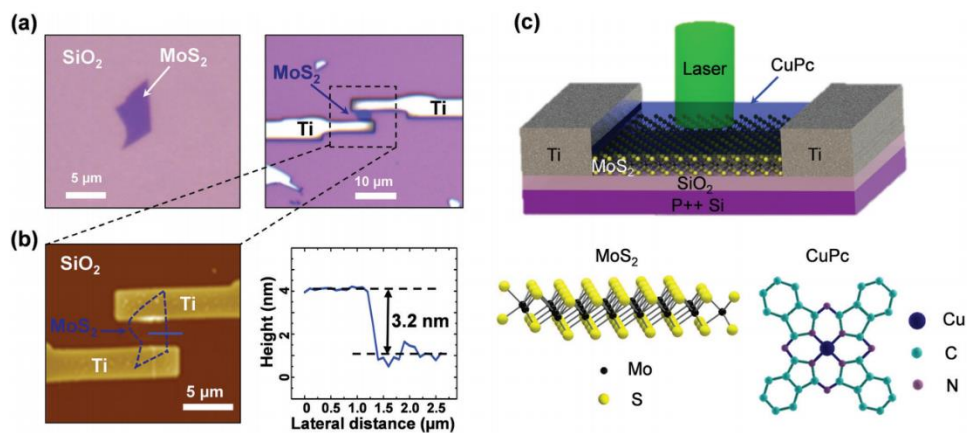


Figure 2.2. (a) Optical images of a MoS₂ flake before (left) and after (right) Ti electrodes were deposited. (b) AFM image (left) of a fabricated MoS₂ FET using the MoS₂ flake shown in (a, b). A cross-sectional topographic profile (right) indicated by the blue line shown in the AFM image. Dashed line indicates the MoS₂ flake. (c) Schematic of CuPc/MoS₂ device illuminated by a laser. The molecular structures of the MoS₂ and CuPc are also shown.

First, we examined the stacking of CuPc layers on MoS₂ flakes by Raman spectroscopy. We observed that the MoS₂ flakes exhibited two Raman characteristic bands at 383 and 405 cm⁻¹, corresponding to out-of-plane (A_{1g} mode) and inplane (E_{2g} mode) vibrations of MoS₂ atoms, respectively (see Figure 2.3). For CuPc, the most intense Raman bands were observed at 1144, 1345, 1454, and 1531 cm⁻¹ for the pyrrole groups, phthalocyanine, the C–N bond, and the C–C bond, respectively (Figure 2.3).

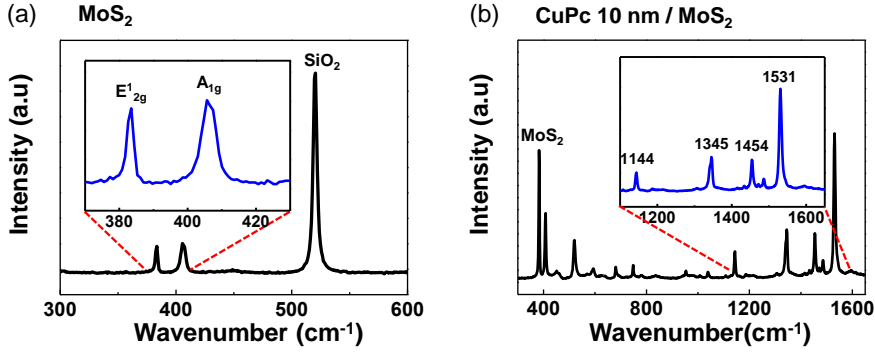


Figure 2.3. Raman spectroscopy data of (a) pristine MoS₂ and (b) CuPc/MoS₂.

2.3.2. Modulation of threshold voltage via a heterostructure

Figure 2.4 shows the transfer characteristics (i.e., drain–source current versus gate voltage, I_{DS} – V_G) of a MoS₂ FET device upon which CuPc layers with different thicknesses, varying from 1 to 10 nm, were deposited. The thickness of the CuPc layer was accurately controlled by a thermal evaporator with few angstroms error. The data were measured at a fixed source–drain voltage (V_{DS}) of 0.1 V in a vacuum ($\sim 10^{-4}$ Torr) at room temperature. The pristine MoS₂ FET (labeled with w/o CuPc, the device before the CuPc layers were coated) exhibited n -type FET behavior. In our work, the room temperature mobility (μ) of the MoS₂ FET was found to be as low as $\sim 1.67 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. Here, the mobility was estimated by using the formula $\mu = (dI_{DS}/dV_G) \times [L/(WC_iV_{DS})]$, where W ($\sim 4.3 \text{ }\mu\text{m}$) is the channel width, L ($\sim 2.4 \text{ }\mu\text{m}$) the channel length, and $C_i = \epsilon_0\epsilon_r/d \sim 1.3 \times 10^{-4} \text{ Fm}^{-2}$ the capacitance between the MoS₂ and p++ Si back gate per unit area. Here, ϵ_0 is the vacuum permittivity, ϵ_r (~ 3.9) is the dielectric constant of the SiO₂ dielectric, and d is the thickness (270 nm) of the SiO₂ layer. The on/off current ratio of this pristine MoS₂ FET was found to be

$\sim 10^6$.

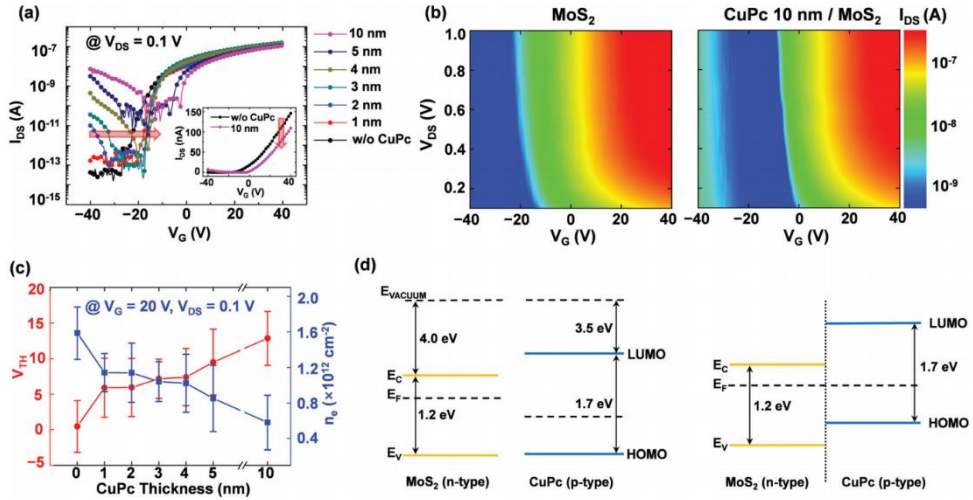


Figure 2.4. (a) I_{DS} - V_G curves on the semilogarithmic scale of the MoS₂ devices without (labeled with “w/o CuPc”) and with CuPc layers of various thicknesses (1, 2, 3, 4, 5, and 10 nm) measured at a fixed $V_{DS} = 0.1$ V. Inset is a linear plot of I_{DS} - V_G curves for a pristine MoS₂ device without a CuPc layer and a 10 nm-thick CuPc/MoS₂ hybrid device. Arrows indicate shifts in threshold voltages and currents. (b) The contour plots of I_{DS} as a function of V_G and V_{DS} for a (left) pristine MoS₂ device and (right) 10 nm-thick CuPc/MoS₂ devices. (c) The threshold voltage and electron carrier concentrations for a pristine MoS₂ device and CuPc/MoS₂ devices as a function of the thickness of the CuPc layers. (d) Schematics of energy band alignment of CuPc/MoS₂ (left) before and (right) after stacking on each other.

The low mobility of MoS₂ FETs is mainly due to the charge traps or adsorbates at the interface between the substrate and the MoS₂ layer.^{1,7} It should be noted that the CuPc layer was coated on the MoS₂ layer after Ti/MoS₂ ohmic contacts were formed, and we measured the electrical properties of the devices in a vacuum ($\sim 10^{-4}$ Torr). These indicate that the lower mobility is not due to the contact properties of Ti/MoS₂, instead we suspect that low mobility of our devices was mainly attributed to the charge traps or adsorbates at the interface between the SiO₂ substrate and the MoS₂

layer. The transfer characteristics of the same MoS₂ FET after the CuPc layers were deposited on the MoS₂ surface are also plotted in Figure 2.4a. When the CuPc layer was deposited, the channel currents at the positive gate voltages decreased, and the threshold voltage shifted towards the positive gate voltage direction compared with the case prior to the CuPc coating and as the thickness of the CuPc layer increased (see inset graph in Figure 2.4a). Throughout the process, we measured the transfer characteristics of the MoS₂ FETs systematically each time we coated the CuPc layers to increase their thickness. For example, the threshold voltage of the pristine MoS₂ FET was ~ 0.45 V, and it shifted from 5.91 to 12.84 V when the thickness of the CuPc layers increased from 1 nm to 10 nm. The channel current of the pristine MoS₂ FET was 1.46×10^{-7} A measured at $V_G = 40$ V and $V_{DS} = 0.1$ V. The channel current decreased from 1.25×10^{-7} to 1.09×10^{-7} A when the thickness of the CuPc layers increased from 1 nm to 10 nm. Note that we also studied the MoS₂ FET by stacking thicker CuPc layers (from 10 to 30 nm), and we observed consistent results, i.e., the current at the positive gate voltage range decreased, and the threshold voltage shifted towards the positive gate voltage direction (see Figure 2.5).

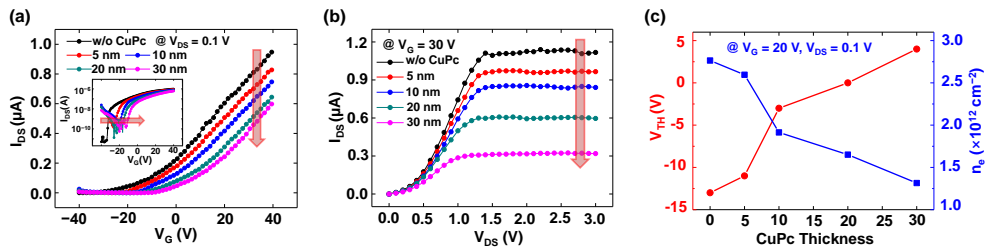


Figure 2.5. (a) I_{DS} - V_G curves and (b) I_{DS} - V_{DS} curves of CuPc/MoS₂ hybrid FETs with different CuPc thickness (5, 10, 20, and 30 nm). (c) Threshold voltage and electron carrier concentration for the CuPc/MoS₂ hybrid FETs.

Additionally, it was observed that the current in the negative gate voltage range

(for example, at $V_G = -40$ V) increased upon increasing the thickness of the CuPc layers. The threshold voltage shift and current change in the MoS₂ FETs after the CuPc treatment can be seen more clearly in the contour plots of the current. Figure 2.4b displays the contour plots of the channel current as a function of V_G and V_{DS} for the MoS₂ FET. These plots were obtained from the transfer characteristic curves measured within the range of 0.1 to 1 V for V_{DS} and -40 to 40 V for V_G before (left) and after (right) the 10 nm-thick CuPc layer stacking. Here, one can clearly see that the channel current decreased at the positive gate voltages and that the threshold voltage shifted in the positive gate voltage direction with increasing thickness of the CuPc layer. The right panel of Figure 2.4b representing the channel current of the CuPc/MoS₂ device also shows the hole conducting region near the high negative gate voltage. These phenomena are due to charge diffusion at the interface between the MoS₂ and CuPc layer. The mechanism of these phenomena will be explained in detail later. Figure 2.4c summarizes the threshold voltage values of all the MoS₂ FET devices that were characterized with and without CuPc layers of different thickness. The error bars in this plot indicate the standard deviations of the threshold voltages from at least four different MoS₂ FET devices at each CuPc layer thickness. One can see that the threshold voltages shifted in the positive gate voltage direction with increasing thickness of the CuPc layers. We estimated the electron carrier concentration of all the MoS₂ FETs, and the results are also plotted in Figure 2.4c. Here, the electron concentration (n_e) was calculated by using the formula $n_e = Q/e = C_g \times |V_G - V_{TH}|/e$, where C_g is the capacitance of the SiO₂ dielectric layer, and e is the elementary charge. In the calculation, we arbitrarily chose the gate voltage $V_G = 20$ V, at which none of the transfer characteristics were in the off condition. The electron concentration at $V_G = 20$ V and $V_{DS} = 0.1$ V decreased with increasing thickness of

the CuPc layers. The observation of the threshold voltage shift and the current decrease in the positive gate voltage range can be explained by the effect of CuPc on MoS₂. CuPc is known to show a *p*-type organic semiconductor characteristic. Therefore, when a *p*-type CuPc layer is stacked on an *n*-type MoS₂, the electrons in MoS₂ can recombine with holes in the CuPc layer at the interface. In case of stacking the CuPc thicker, more electrons can recombine, which is responsible for the threshold voltage shift and the current decrease in the positive gate voltage range (see Figure 2.4d). Such carrier recombination at the interface between MoS₂ and CuPc layers results in a reduction of the electron carrier concentration in the MoS₂ channel layer and threshold voltage shift in the FET. At the same time, the current increased in the negative gate voltage range due to the hole conduction through the *p*-type CuPc layer between the source and drain electrodes. This charge transfer behavior will become more significant when the thickness of the CuPc layer increases on the MoS₂ film.

2.3.3. Enhancement of photoresponsive characteristics

We studied the photoresponsive characteristics of the CuPc/MoS₂ hybrid devices under different light intensity (the power of the laser source) conditions (0.03, 0.05, 10, 25, 35, and 40 mW), and the results are shown in Figure 2.6a. In this figure, the data in black (labeled as Dark) were obtained in the dark without laser illumination. Because the energy of the incident light (~ 2.38 eV, 520 nm wavelength) is greater than the band gap energy of the multilayer MoS₂ (~ 1.2 eV) and the CuPc layer (~ 1.7 eV), it can be absorbed and can generate electron–hole pairs in both the

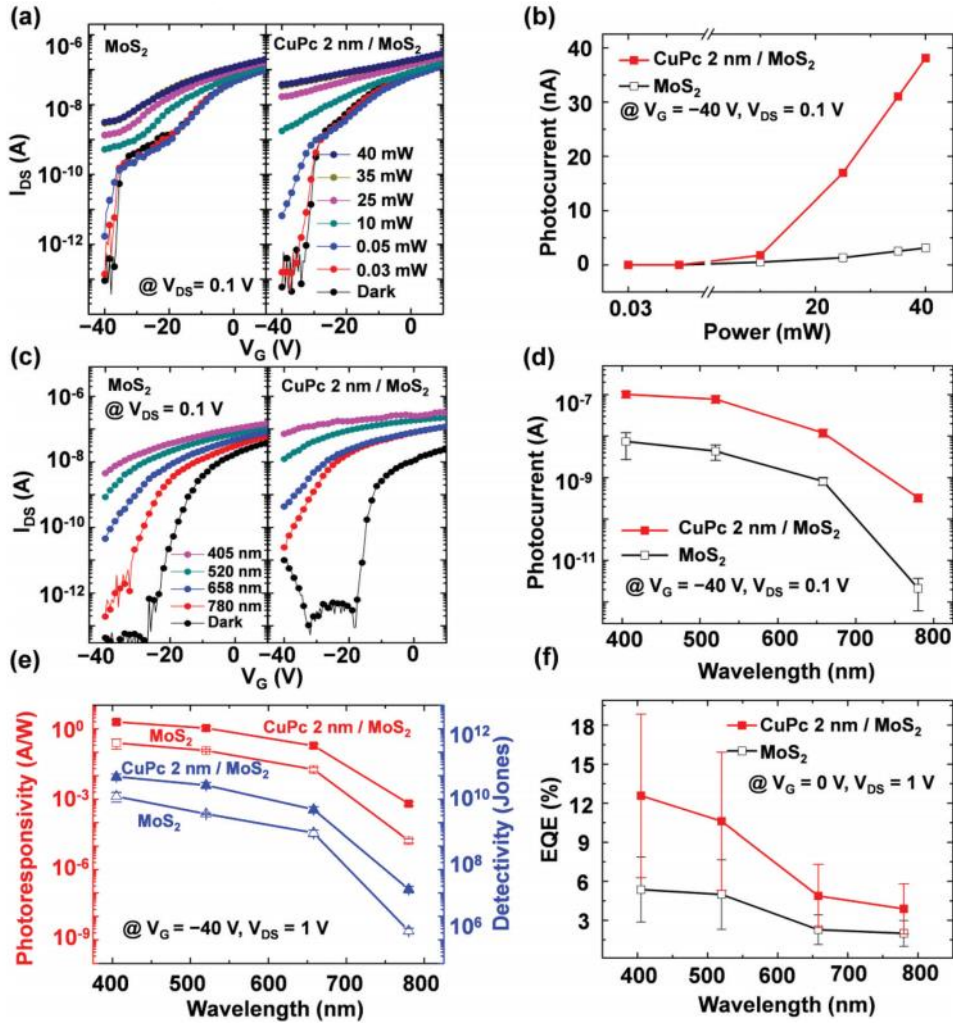


Figure 2.6. (a) I_{DS} - V_G curves of pristine MoS₂ and 2 nm-thick CuPc/MoS₂ photodetectors measured at a fixed $V_{DS} = 0.1$ V under dark and illuminated conditions (wavelength = 520 nm) at different laser intensities. (b) Photocurrent of pristine MoS₂ and CuPc/MoS₂ photodetectors measured at $V_G = -40$ V and $V_{DS} = 0.1$ V as a function of the laser intensity. (c) I_{DS} - V_G curves of pristine MoS₂ and CuPc/MoS₂ photodetectors measured under dark and light illumination conditions at different wavelengths and a fixed laser intensity (40 mW). (d) Photocurrent, (e) photoresponsivity and detectivity, and (f) external quantum efficiency (EQE) of pristine MoS₂ and CuPc/MoS₂ photodetectors as a function of the wavelength of the illumination.

CuPc layer and the MoS₂ channel film. In the case of a pristine MoS₂ FET without

the CuPc layer, the incident light is absorbed by the MoS₂ film, and the photo-generated electron–hole pairs contribute to the increasing current in the MoS₂ FETs. On the other hand, in the case of hybrid CuPc/MoS₂ FETs, the incident light is absorbed by both the CuPc layer and the MoS₂ film. The photo-generated electron–hole pairs in the CuPc layer are separated at the interface between the *p*-type CuPc layer and the *n*-type MoS₂. Then, the electrons migrating from the CuPc layer to the MoS₂ contribute additional current. Note that to check whether the electron–hole pairs can be generated in the CuPc layer by the incident light, we measured the photoconductive properties of the CuPc-only FET without the MoS₂ film in the device structure. From the experimental results (Figure 2.6), we observed two main phenomena. First, the photoinduced current level increased with increasing light intensity for both the pristine MoS₂ and hybrid CuPc/MoS₂ FETs. This result is simply due to a greater generation of electron–hole pairs by the more intense light. Additionally, the photoinduced current in the CuPc/ MoS₂ FET was higher than that in the pristine MoS₂ FET due to the photo-generated electrons in the CuPc layer transferring from the CuPc layer to the MoS₂, producing additional current. These phenomena are summarized in Figure 2.6b, where we plotted the photoinduced current of the pristine MoS₂ and CuPc/MoS₂ FETs measured at $V_G = -40$ V and $V_{DS} = 0.1$ V in the dark and under 520 nm laser illumination at different laser intensities. For example, the photocurrent (38.1 nA) of the CuPc/MoS₂ FET was approximately an order of magnitude higher than that (3.13 nA) of the pristine MoS₂ FET at 40 mW laser illumination at $V_G = -40$ V. Figure 2.6c shows the photoresponsive data of the pristine MoS₂ and CuPc (2 nm-thick layer)/MoS₂ FETs measured at $V_G = -40$ V and $V_{DS} = 0.1$ V in the darkness and under laser illumination with different wavelengths and a fixed intensity of 40 mW. Four different laser wavelengths (405, 520, 658, and

780 nm) were used for this experiment, and all of them exceeded the band gap energy values of the multilayer MoS₂ and CuPc. The photoinduced current increased as the wavelength of the incident light became shorter, indicating that the incident light having energy larger than the energy gap of the CuPc and MoS₂ can create electron–hole pairs more easily. Moreover, similar to the results of Figures 2.6a and 2.6b, we observed that the photocurrent from the CuPc/MoS₂ hybrid device was higher than that of the pristine MoS₂ device by an order of magnitude throughout the wavelength ranges (Figure 2.6d). The performances of photodetectors are often evaluated using photoresponsivity, detectivity, and external quantum efficiency. The photoresponsivity (R) can be estimated from the formula $R = I_{ph}/P_{Light}$, where I_{ph} is the photocurrent and P_{Light} is the intensity of incident light. In the calculation, we only considered the active area of the incident flux of laser illumination (with a laser spot radius of 0.5×10^{-3} m). The calculated photoresponsivity values for the pristine MoS₂ and CuPc (2 nm-thick layer)/MoS₂ phototransistors are plotted in Figure 2.6e. One can see that the photoresponsivity increased with shorter wavelengths of the illuminating light and was higher for the CuPc/MoS₂ than the pristine MoS₂ devices. Moreover, the detectivity (D^*) parameter can be estimated using $D^* = (RA_D^{1/2})/(2eI_D)^{1/2}$, where A_D is the effective detection area, I_D is the unilluminated current, and e is the elementary charge (1.6×10^{-19} C). The determined detectivity values of the CuPc/ MoS₂ and pristine MoS₂ photodetectors are plotted in Figure 2.6e. The results in Figure 2.6e indicate that both the photoresponsivity and detectivity of the MoS₂ devices increased by roughly an order of magnitude with stacking of the CuPc layer on the MoS₂ surface. From the photocurrent values, we estimated the external quantum efficiency (EQE), which is the efficiency of converting electrons according to incident photons (Figure 2.6f). The EQE is defined

as $\text{EQE} = (I_{\text{ph}}/e)/(P_{\text{Light}}/h\nu)$, where $h\nu$ is the photon energy. The pristine MoS_2 photodetectors displayed an R of 0.25 AW^{-1} , a D^* of 1.49×10^{10} Jones (measured at $V_G = -40 \text{ V}$ and $V_{\text{DS}} = 1 \text{ V}$), and an EQE of 5.36 % under 405 nm illumination at 40 mW intensity (measured at $V_G = 0 \text{ V}$ and $V_{\text{DS}} = 1 \text{ V}$). In contrast, the CuPc/MoS_2 hybrid photodetectors exhibited an R of 1.98 AW^{-1} , a D^* of 6.11×10^{10} Jones, and an EQE of 12.57% under the same measurement conditions as the pristine MoS_2 devices. With these photodetection results shown in Figure 2.6, we can confirm that the CuPc/MoS_2 hybrid devices exhibited a better photodetection capability than the pristine MoS_2 devices in the broad wavelength and optical intensity ranges. In addition, we investigated the gate voltage dependence of the photoresponsive characteristics (see Figure 2.7). We found that the photoresponsive properties increased as the increasing gate voltage, which results in the increase of electron carriers in the MoS_2 layer and the reduction of charge recombination.

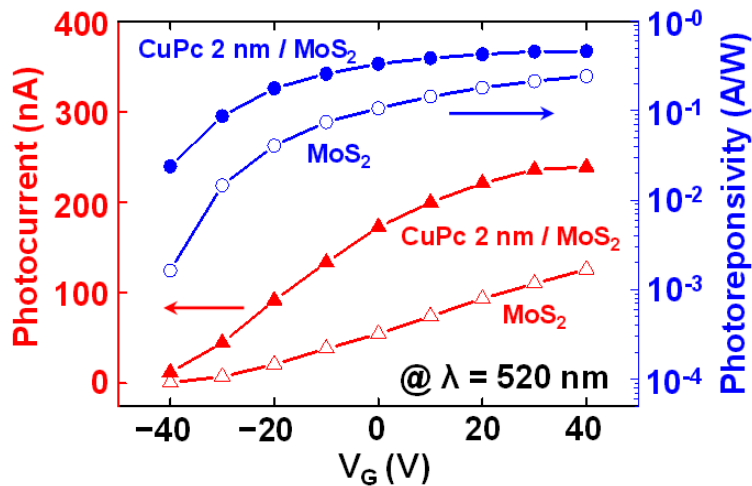


Figure 2.7. Gate voltage dependence of the photocurrent and the photoresponsivity

Figure 2.8a shows the photo-switching data before and after the MoS_2 FET devices were deposited with CuPc layers of different thicknesses (1, 2, 3, 4, 5, and 10 nm).

Note that in order to clearly compare and emphasize differences in the time-dependent photocurrent behavior, the photocurrents were normalized, i.e., the light-off currents in the dark of each curve were shifted by an equal distance (15 nA) in the y-axis. The white areas represent the light-off current of the devices (labeled “light off”), and the cyan areas indicate the light-on current of the devices under 520 nm illumination (labeled “light on”). We observed that there are striking differences in the photocurrent ratio (a photocurrent-to-dark condition ratio) as a function of the thickness of the CuPc layer while the light turns off and on. From Figure 2.8b, it is clearly seen that the photocurrent and photoresponsivity of the CuPc/MoS₂ hybrid devices strongly depended on the thickness of the CuPc layers on the MoS₂, and in particular the device conditions with the 2 nm-thick CuPc layer showed the largest photocurrent and photoresponsivity. This indicates that the high efficient performance between the light absorption and photodetection in the CuPc/MoS₂ heterostructures can be obtained by optimizing the appropriate thickness of a *p*-type organic layer due to the increase of charge recombination at the interface with increasing hole carriers in the CuPc layer. The photo-generated electrons in the CuPc layer can assist the increase of photocurrent in the hybrid device. However, the increase of hole carrier density in the thicker CuPc layer than 2 nm leads to the increase of recombination with electrons in the MoS₂ layer at the interface (see Figure 2.4), which can cause the reduction of photoresponsivity. After the thin MoS₂ and CuPc layers form a junction, the excitons from the CuPc layer are generated upon light illumination. The photo-generated electrons in the lowest unoccupied molecular orbital (LUMO) level of the CuPc move to the

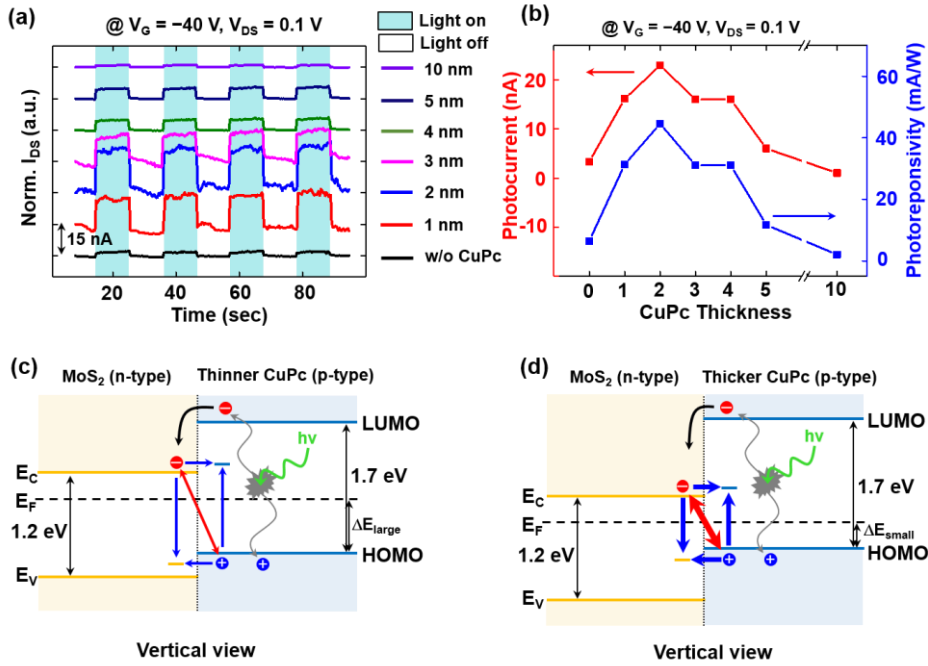


Figure 2.8. (a) Normalized photo-switching data of pristine MoS₂ and CuPc/MoS₂ photodetectors with different CuPc layer thicknesses (1, 2, 3, 4, 5, and 10 nm) measured at $V_G = -40$ V and $V_{DS} = 0.1$ V while a light (wavelength = 520 nm, intensity = 40 mW) was on and off. (b) Photocurrent and photoresponsivity of devices versus the CuPc layer thickness. (c, d) Energy band diagrams of (c) a relatively thinner CuPc/MoS₂ device and (d) a relatively thicker CuPc/MoS₂ device. Blue lines and red lines indicate SHR and Langevin recombination processes, respectively.

interface and then transfer to the MoS₂ layer (black arrows in Figures 2.8c and 2.8d) due to the energy alignment (i.e., LUMO of the CuPc is higher than the conduction band minimum of the MoS₂). In contrast, the photo-generated holes in the highest occupied molecular orbital (HOMO) level of the CuPc could not move to MoS₂ due to the larger barrier. Here, the interlayer recombination processes can occur at the interface between the thin MoS₂ and CuPc layers. These processes are described as trap-assisted recombination (known as Shockley–Read–Hall recombination) by

inelastic tunneling of carriers into trap states in the forbidden gap (marked by the blue arrows in Figures 2.8c and 2.8d) and as Langevin recombination of the electron–hole carriers via the Coulomb interaction (marked by the red arrows in Figures 2.8c and 2.8d) across the interface.^{40–43} Both interlayer recombination processes are proportional to the density of the major charge carriers in the MoS₂ and CuPc layers.^{40,43} Interestingly, in Figure 2.4a the current in the negative gate voltage range for the CuPc/MoS₂ hybrid and CuPc-alone FETs increased with increasing thickness of the CuPc layers, so that the *p*-type behavior became stronger. This indicates that as the thickness of the CuPc layer increases, the density of hole carriers in the CuPc layer increases, which results in the decrease in the energy difference between the Fermi level and HOMO level of the CuPc (Figures 2.8c and 2.8d) with increased CuPc layer thickness. Therefore, the thickness dependence of the density of hole carriers can strongly affect the interlayer recombinations for the CuPc/MoS₂ devices. Compared with the smaller energy difference (ΔE_{small}) of thicker CuPc (Figure 2.8d), the total number of majority carriers that cause interlayer recombinations is relatively smaller due to the larger energy difference (ΔE_{large}) in the case of the junction between the MoS₂ and the relatively thinner CuPc layer, leading to the stronger enhancement of photodetection performance (Figure 2.8c). In addition, when the CuPc layer is much thicker than the exciton diffusion length (~ 1.6 nm),⁴⁴ the photo-generated electron and hole pairs will recombine before they separate and will not contribute to the photocurrent. Therefore, as an overall effect, such as the contribution of photo-generated electrons in the CuPc layer, recombination processes, and exciton diffusion length, the relatively thinner CuPc/MoS₂ devices (near the 2 nm CuPc) exhibited higher photoresponsivity than the relatively thicker CuPc/MoS₂ devices.

2.2.4. Improved photoswitching characteristics

In addition, the photoswitching rise (τ_{rise}) and decay (τ_{decay}) times of the pristine and CuPc treated MoS₂ FETs were investigated. Here, τ_{rise} is defined as the time required for the current change from 10% to 90% of the maximum amplitude, and τ_{decay} is the time at which the amplitude decreases to $1/e$ times from its initial value, where e is the constant based on the natural logarithm. Figure 2.9 shows a plot of the normalized photoswitching data, demonstrating the rise and decay dynamics under 520 nm laser irradiation under ambient conditions for 20 s, measured at $V_{GS} = -40$ V and $V_{DS} = 0.1$ V. After depositing a 2 nm-CuPc layer on the MoS₂ channel, the rise and decay times decreased from 12.87 s to 5.07 s and from 3.57 s to 0.18 s, respectively. In particular, the decay time was drastically shortened to almost 5% of the original value after the CuPc surface treatment. We also investigated the CuPc thickness dependence of the rise and decay times, represented by blue and red symbols, respectively, in Figure 2.10. This result showed that the rise and decay times decreased rapidly up to 2 nm CuPc deposition and then became saturated as the CuPc thickness was further increased. These improved photoswitching response times by the CuPc surface treatment can be explained by the relationship between free carriers and absorbed oxygen at the surface. The photoswitching mechanisms of the pristine and CuPc treated MoS₂ FETs are described in Figure 2.11.

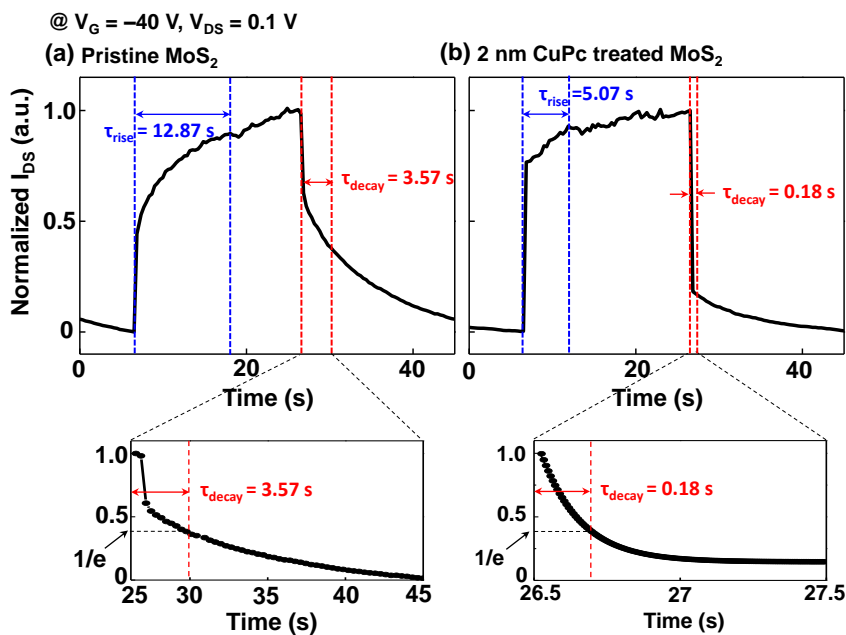


Figure 2.9. Normalized photoswitching results of (a) pristine and (b) 2 nm CuPc treated MoS₂ FETs at $V_{GS} = -40$ V and $V_{DS} = 0.1$ V.

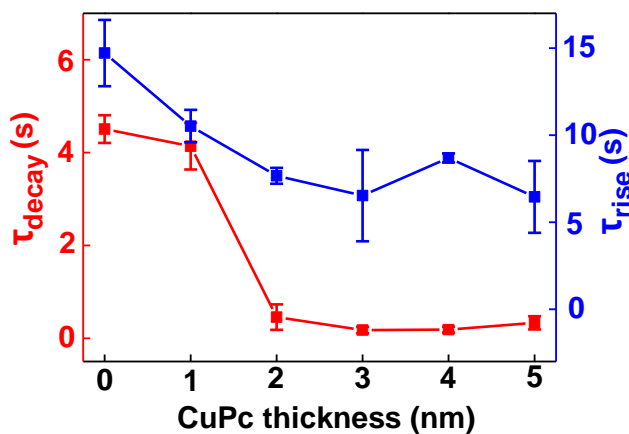


Figure 2.10. Decay (τ_{decay}) and rise times (τ_{rise}) versus CuPc thicknesses from 0 to 5 nm. The symbols and error bars indicate average values and standard deviations from three measurements.

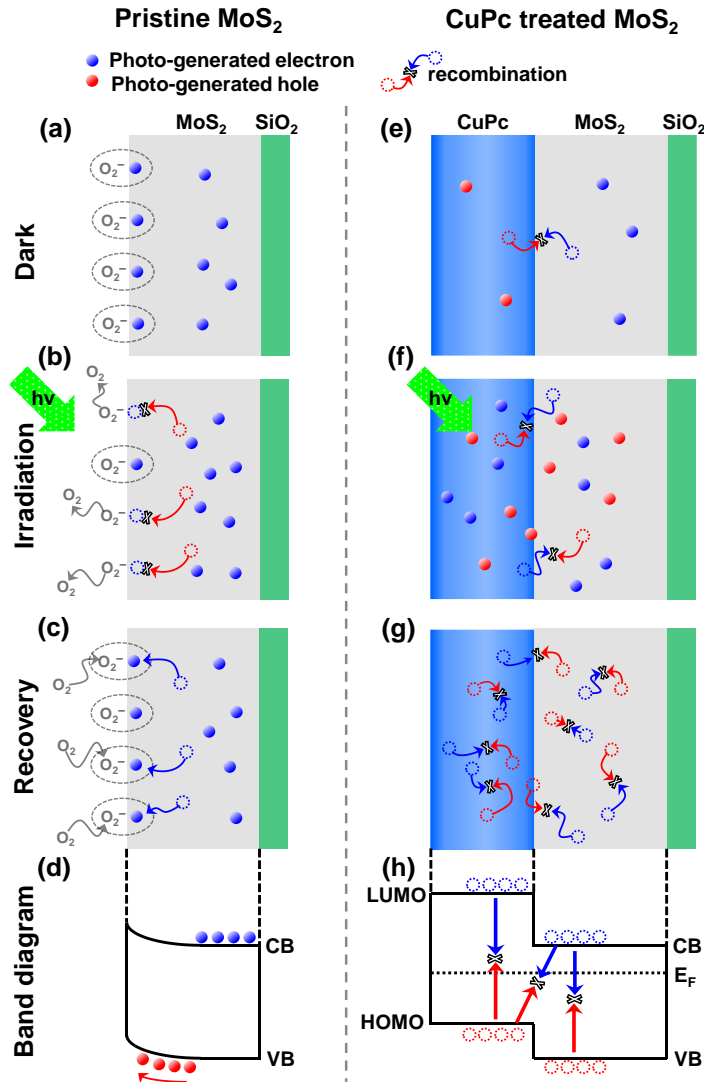


Figure 2. 11. Photoswitching processes and band diagram (a-d) before the CuPc treatment and (e-h) after the CuPc treatment.

For the pristine MoS₂ FETs, oxygen molecules are attached on the MoS₂ surface with trapping electrons [$O_2 + e \rightarrow O_2^-$], which causes a significant reduction of the MoS₂ channel conductance, as shown in Figure 2.11a. Under laser irradiation, adsorbed oxygen can be detached due to the recombination between trapped electrons and photogenerated holes [$O_2^- + h \rightarrow O_2$], which results in an increase in the conductance of the MoS₂ channel (Figure 2.11b). In contrast to photogenerated

holes, which move to the surface to recombine with trapped electrons, photogenerated electrons mainly contribute additional current unless they are trapped again by oxygen adsorbed on the surface (Figure 2.11b). These photogenerated electrons accumulate in the MoS₂ channel gradually until the adsorption and desorption processes of oxygen molecules reach the equilibrium state, which explains why the drain current continuously increased until the saturation region during laser irradiation (see Figure 2.11a). In this manner, the pristine MoS₂ FETs have a long rise time through repeated absorption and desorption processes until reaching the equilibrium state during laser irradiation. If light irradiation is turned off, much more electrons remain than holes because many holes have already recombined with the trapped electrons by oxygen molecules at the MoS₂ surface. Although holes can recombine with electrons right after turning off laser irradiation, electrons which are not recombined still remain in the MoS₂ channel. In other words, unpaired electrons are gradually trapped at the surface and impede the fast photoswitching decay process, as shown in Figure 2.11c. These results are consistent with a previous report, in which the authors showed that absorbed oxygen can destroy the ratio of electrons and holes and lead to a long decay time.⁴⁵ Figure 2.11d shows the energy band diagram with oxygen molecules adsorbed on the MoS₂ surface, which results in band bending near the surface by the reduced electron density. Due to the band bending near the surface, the electron-hole pairs are separated and cannot recombine well, which results in a long decay time. In summary, the absorbed oxygen molecules cause long photoswitching rise and decay times in the untreated MoS₂ FET because oxygen molecules trap electrons, leading to less recombination after the irradiation is turned off.

On the contrary, oxygen molecules cannot be adsorbed on the MoS₂ surface in

the CuPc treated MoS₂ FET. Note that the major carriers of each layer can recombine at the interface in the dark state due to the difference of carrier concentrations, as shown in Figure 2.11e. During laser irradiation, the drain current can reach the saturation region rapidly because of negligible absorbed oxygen molecules on the MoS₂ channel, which results in a short rise time (see Figure 2.9b). Then, additional photogenerated electrons and holes accumulate continuously during laser irradiation, which means that the number of remaining electrons is comparable to that of the remaining holes during laser irradiation. Therefore, the electrons and holes can recombine quickly upon turning off irradiation due to the comparable numbers of electrons and holes, resulting in a fast decay time (Figure 2.11g). Moreover, fast recombination is allowed by the band to band recombination in each layer of the CuPc and MoS₂ as well as Langevin recombination between the CuPc and MoS₂ layers, as shown in Figure 2.11h. From these analyses, the CuPc surface treatment, working as a passivation layer, can be an effective method for shortening photoswitching response times against oxygen.

Conclusion

We examined the photodetection and photoswitching response times of MoS₂ FETs by stacking a CuPc layer. By depositing a CuPc layer on the MoS₂ channel, we observed enhanced photoresponsivity compared to pristine MoS₂ FETs. In particular, the photoswitching rise and decay characteristics of the CuPc-treated MoS₂ FETs were noticeably improved. In particular, the decay time was shortened from 3.57 s to 0.18 s at $V_{DS} = 0.1$ V and $V_G = -40$ V after introducing a 2 nm-thick CuPc layer on the MoS₂ channel. The CuPc surface treatment created a *p-n* vertical interface

with the MoS₂ channel layer, resulting in enhanced photoresponsivity, and this treatment also played a role in creating a passivation layer against oxygen, which induced fast photoswitching response times. Our results may provide a promising route for ultra-thin and highly sensitive MoS₂ photoswitching applications.

Figure captions

Figure 2.1. Schematic of fabricating processes of MoS₂ FET

Figure 2.2. (a) Optical images of a MoS₂ flake before (left) and after (right) Ti electrodes were deposited. (b) AFM image (left) of a fabricated MoS₂ FET using the MoS₂ flake shown in (a, b). A cross-sectional topographic profile (right) indicated by the blue line shown in the AFM image. Dashed line indicates the MoS₂ flake. (c) Schematic of CuPc/MoS₂ device illuminated by a laser. The molecular structures of the MoS₂ and CuPc are also shown.

Figure 2.3. Raman spectroscopy data of (a) pristine MoS₂ and (b) CuPc/MoS₂.

Figure 2.4. (a) $I_{DS}-V_G$ curves on the semilogarithmic scale of the MoS₂ devices without (labeled with “w/o CuPc”) and with CuPc layers of various thicknesses (1, 2, 3, 4, 5, and 10 nm) measured at a fixed $V_{DS} = 0.1$ V. Inset is a linear plot of $I_{DS}-V_G$ curves for a pristine MoS₂ device without a CuPc layer and a 10 nm-thick CuPc/MoS₂ hybrid device. Arrows indicate shifts in threshold voltages and currents. (b) The contour plots of I_{DS} as a function of V_G and V_{DS} for a (left) pristine MoS₂ device and (right) 10 nm-thick CuPc/MoS₂ devices. (c) The threshold voltage and electron carrier concentrations for a pristine MoS₂ device and CuPc/MoS₂ devices as a function of the thickness of the CuPc layers. (d) Schematics of energy band alignment of CuPc/MoS₂ (left) before and (right) after stacking on each other.

Figure 2.5. (a) $I_{DS}-V_G$ curves and (b) $I_{DS}-V_{DS}$ curves of CuPc/MoS₂ hybrid FETs with different CuPc thickness (5, 10, 20, and 30 nm). (c) Threshold voltage and electron carrier concentration for the CuPc/MoS₂ hybrid FETs.

Figure 2.6. (a) $I_{DS}-V_G$ curves of pristine MoS₂ and 2 nm-thick CuPc/MoS₂ photodetectors measured at a fixed $V_{DS} = 0.1$ V under dark and illuminated conditions (wavelength = 520 nm) at different laser intensities. (b) Photocurrent of pristine MoS₂ and CuPc/MoS₂ photodetectors measured at $V_G = -40$ V and $V_{DS} = 0.1$ V as a function of the laser intensity. (c) $I_{DS}-V_G$ curves of pristine MoS₂ and CuPc/MoS₂ photodetectors measured under dark and light illumination conditions at different wavelengths and a fixed laser intensity (40 mW). (d) Photocurrent, (e) photoresponsivity and detectivity, and (f) external quantum efficiency (EQE) of pristine MoS₂ and CuPc/MoS₂ photodetectors as a function of the wavelength of the illumination.

Figure 2.7. Gate voltage dependence of the photocurrent and the photoresponsivity

Figure 2.8. (a) Normalized photo-switching data of pristine MoS₂ and CuPc/MoS₂ photodetectors with different CuPc layer thicknesses (1, 2, 3, 4, 5, and 10 nm) measured at $V_G = -40$ V and $V_{DS} = 0.1$ V while a light (wavelength = 520 nm, intensity = 40 mW) was on and off. (b) Photocurrent and photoresponsivity of devices versus the CuPc layer thickness. (c, d) Energy band diagrams of (c) a relatively thinner CuPc/MoS₂ device and (d) a relatively thicker CuPc/MoS₂ device. Blue lines and red lines indicate SHR and Langevin recombination processes, respectively.

Figure 2.9. Normalized photoswitching results of (a) pristine and (b) 2 nm CuPc treated MoS₂ FETs at $V_{GS} = -40$ V and $V_{DS} = 0.1$ V.

Figure 2.10. Decay (τ_{decay}) and rise times (τ_{rise}) versus CuPc thicknesses from 0 to 5 nm. The symbols and error bars indicate average values and standard deviations from three measurements.

Figure 2.11. Photoswitching processes and band diagram (a-d) before the CuPc treatment and (e-h) after the CuPc treatment.

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Chapter 3. Intrinsic optoelectronic characteristics of MoS₂ phototransistors via a fully transparent van der Waals heterostructure

*In the last decade, intensive studies on monolayer MoS₂-based phototransistors have been carried out to achieve further enhanced optoelectronic characteristics. However, the intrinsic optoelectronic characteristics of monolayer MoS₂ have not still been explored until now because of unintended interferences, such as multiple reflections of incident light originating from commonly used opaque substrates. This leads to overestimated photoresponsive characteristics inevitably due to the enhanced photogating and photoconductive effects. In this Chapter, we reveal the intrinsic photoresponsive characteristics of monolayer MoS₂, including its internal responsivity and quantum efficiency, in fully transparent monolayer MoS₂ phototransistors employing a van der Waals heterostructure. Interestingly, as opposed to the previous reports, the internal photoresponsive characteristics do not significantly depend on the wavelength of the incident light as long as the electron-hole pairs are generated in the same *k*-space. This study provides a deeper understanding of the photoresponsive characteristics of MoS₂ and lays the foundation for two-dimensional materials-based transparent phototransistors.*

3.1. Introduction

Beginning with extensive research on graphene, the emergence of a new class of atomically thin two-dimensional (2D) materials has opened up a new era for fundamental scientific studies and the next generation of electronics.¹⁻⁴ In this group of 2D materials, especially molybdenum disulfide (MoS_2) has been extensively studied as a promising candidate for realizing 2D materials-based flexible photodetectors due to its outstanding optoelectronic properties, such as intrinsic bandgap, high photodetection capability, high carrier mobility, good electrical stability, and mechanical flexibility.⁵⁻¹⁰ Recently, MoS_2 -based 2D heterostructures have been designed to enhance photodetection and photoswitching abilities, which is attributed to the high-quality interfacial properties between 2D materials held together by the weak van der Waals (vdW) interaction without covalent bonds. For instance, vdW heterostructured MoS_2 photodiodes made with tungsten diselenide (WSe_2), molybdenum ditelluride (MoTe_2), and black phosphorus have been realized to improve photoresponsive characteristics.¹¹⁻¹⁵ Also, MoS_2 phototransistors with hexagonal boron nitride (*h*-BN), graphene, and tin diselenide (SnSe_2) in a vertical vdW heterostructure have shown enhanced responsivity or faster photoswitching behaviors.¹⁶⁻¹⁸ Although numerous results of the optoelectronic properties of vdW heterostructured photodetectors have been reported, to date, the intrinsic optoelectronic characteristics of atomically thin MoS_2 have not been explored because most previous studies have employed opaque substrates, typically heavily-doped Si with SiO_2 , due to the convenience from a manufacturing perspective. The opaque platforms allow multiple reflections of incident light, which results in the generation of additional electron-hole pairs at the $\text{MoS}_2/\text{SiO}_2$ and SiO_2/Si

interfaces.¹⁹ Furthermore, this unintended interference causes a strong photogating effect due to the trapping of photogenerated holes at the low-quality interface,^{20,21} which can overestimate the ability of the photoresponsivity of MoS₂. For a better understanding of MoS₂, in this regard, the systematic investigation of the intrinsic optoelectronic characteristics of monolayer MoS₂ is highly desirable without effects caused by external interference such as reflected or refractive light.

Here, we report the intrinsic optoelectronic characteristics of monolayer MoS₂ phototransistors via a fully transparent vdW heterostructure with *h*-BN (as a dielectric layer) and graphene (as a gate electrode). The 2D *h*-BN dielectric provided a near-ideal interface with MoS₂ enabling low-voltage operation. To investigate the intrinsic photoresponsive properties of MoS₂, we compared the characteristics of the MoS₂ phototransistors fabricated on transparent polyethylene naphthalate (PEN) and opaque SiO₂/Si substrates. From the results, it turned out that the MoS₂ phototransistors fabricated on the opaque SiO₂/Si substrate showed higher photoresponsive performances due to the enhanced photogating and photoconductive effects caused by multiple reflections of the incident light. From the MoS₂ phototransistors fabricated on the transparent PEN substrate, the intrinsic photoresponsive properties were revealed; specifically, an internal responsivity of 3.2×10^2 A/W and internal quantum efficiency (IQE) of 7.1×10^5 % were achieved. Interestingly, unlike the external photoresponse determined by the incident photons that shows the wavelength-dependent characteristics, the internal photoresponse determined by absorbed photons in the MoS₂ channel did not significantly depend on the wavelength of the incident light. Furthermore, we found out that the intrinsic photoresponsive characteristics of MoS₂ could be dependent on the locations where photogeneration occurred in *k*-space and the consequent alteration of the effective

mass.

3.2. Experiments

3.2.1. Device fabrication process

Figure 3.1 illustrates the fabrication processes of the transparent molybdenum disulfide (MoS_2) field-effect transistors (FETs). First, monolayer graphene (Gr) layer grown on copper foil by chemical vapor method (CVD) method was transferred onto SiO_2/Si substrate (Figure 3.1b). Next, hexagonal boron nitride ($h\text{-BN}$) was stacked on Gr layer to be used as a dielectric layer (Figure 3.1c). After transferring CVD-grown monolayer MoS_2 onto $h\text{-BN}$ (Figure 3.1d), the source, drain, and gate electrodes of Au (30-nm thick) were formed by using an electron beam lithography (JMS-6510, JEOL) and an electron beam evaporator system (KVE-2004L, Korea Vacuum Tech.). Fabricated van der Waals (vdW) heterostructured MoS_2 FET was coated by PMMA to maintain its device structure during the transfer process to polyethylene naphthalate (PEN) substrate. The vdW heterostructured MoS_2 FETs were coated by PMMA immersed in the 50% potassium hydroxide solution and then annealed at 70 °C for etching the SiO_2/Si substrate. After etching the SiO_2/Si substrate, the vdW heterostructures were transferred onto a 125- μm -thick PEN substrate by scooping method (Figure 3.1f). Lastly, the fabricated fully transparent MoS_2 FETs were annealed at 80 °C in vacuum for 2 h to by eliminating the residues on MoS_2 surface.

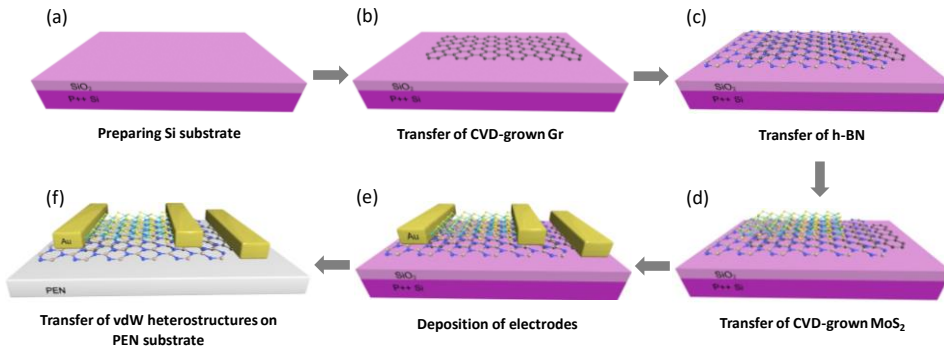


Figure 3.1. Schematics of the fabrication processes for transparent MoS₂ FETs.

3.2.2. Electrical and optical characterizations

The electrical properties of the transparent MoS₂ FETs were measured using a semiconductor parameter analyzer (Keithley 4200-SCS) in vacuum. Transmittance and reflectance data for the vdW heterostructure were obtained by using a UV/Vis/NIR Microspectrometer (CRAIC, QDI-1000). Raman spectra, PL spectra, and PL mapping of vdW materials were characterized using an XperRam 200 (Nanobase, Inc.) instrument using a 532 nm laser as the excitation source with a diffraction-limited laser spot size ($\sim 1 \mu\text{m}$ spot radius). In addition, an electroluminescence measurement system (Nanobase, Inc.) was used to investigate the optoelectronic characteristics of the transparent MoS₂ phototransistors.

3.3. Results and discussions

3.3.1. Structure and electrical characteristics of transparent MoS₂ phototransistors

For the realization of transparent MoS₂ phototransistors, ready-made MoS₂ field-effect transistors (FETs) on a SiO₂/Si substrate were transferred to a PEN substrate

via the transfer method using potassium hydroxide etching solution. To enhance the reproducibility of MoS₂ phototransistors, chemical vapor deposition (CVD)-grown monolayer MoS₂ was used as a channel layer in 2D vdW heterostructured FETs. In addition, by employing CVD-grown monolayer graphene as a gate electrode and mechanically exfoliated multilayer *h*-BN (41-nm thick) as a gate dielectric on a transparent PEN substrate (125- μ m thick), good transparency of over 80 % in the visible range was achieved. Figure 3.2a shows a schematic illustrating the vertically stacked vdW heterostructure on a PEN substrate. After the realization of the 2D heterostructure using a micro-manipulator system (AP-4200GP, UNITEK), no drastically degraded transparency was observed in the optical image (Figure 3.2b). Raman frequency difference (20 cm⁻¹) (upper panel, Figure 3.2c) and a photoluminescence (PL) mapping image displaying uniform bandgap energy (1.86 eV) (Figure 3.2d) support the fact that the CVD-grown MoS₂ used for the channel was a uniform monolayer.²² In addition, the Raman peak observed for the multilayer *h*-BN at 1364 cm⁻¹ is assigned to the in-plane vibration (E_{2g} mode).²³ The large intensity of the 2D-band relative to the G-band, which can only be observed in monolayer graphene due to a triple-resonance process, shows that monolayer graphene film was well grown via the optimized CVD process (lower panel, Figure 3.2c).²⁴ All Raman spectra in Figure 3.2c were measured before transfer to a PEN substrate for observing the distinct spectrum.

Figures 3.2e and 1f show the transfer curve (drain-source current versus gate voltage, $I_{DS}-V_{GS}$) and the output curve (drain-source current versus drain voltage, $I_{DS}-V_{DS}$) for the transparent CVD-grown monolayer MoS₂ FET measured in vacuum ($\sim 10^{-4}$ Torr) at room temperature. Arising from the thin *h*-BN dielectric layer, a low

operation voltage ranging from -4 V to 5 V was achieved. The field-effect mobility (μ) was determined to be $12.2 \text{ cm}^2/\text{V}\cdot\text{s}$, as calculated using the formula

$$\mu = \left(\frac{\partial I_{DS}}{\partial V_{GS}} \right) \frac{L}{W} \frac{1}{C_i V_{DS}}, \quad (1)$$

with a channel width $W = 8.56 \text{ }\mu\text{m}$, channel length $L = 5.05 \text{ }\mu\text{m}$, and unit capacitance for the h -BN dielectric $C_i = 0.756 \text{ mF/cm}^2$ (thickness of 41 nm and dielectric constant of 3.5 for h -BN were considered^{25,26}). Figure 3.2g shows the logarithmic scale plot for I_{DS} - V_{DS} measured at V_{GS} ranging from 0 V to 5 V. The extracted average γ (linearity parameter in the output curve) value of 1.01 in the output characteristics indicates ohmic contacts between the MoS_2 channel layer and Au electrodes.

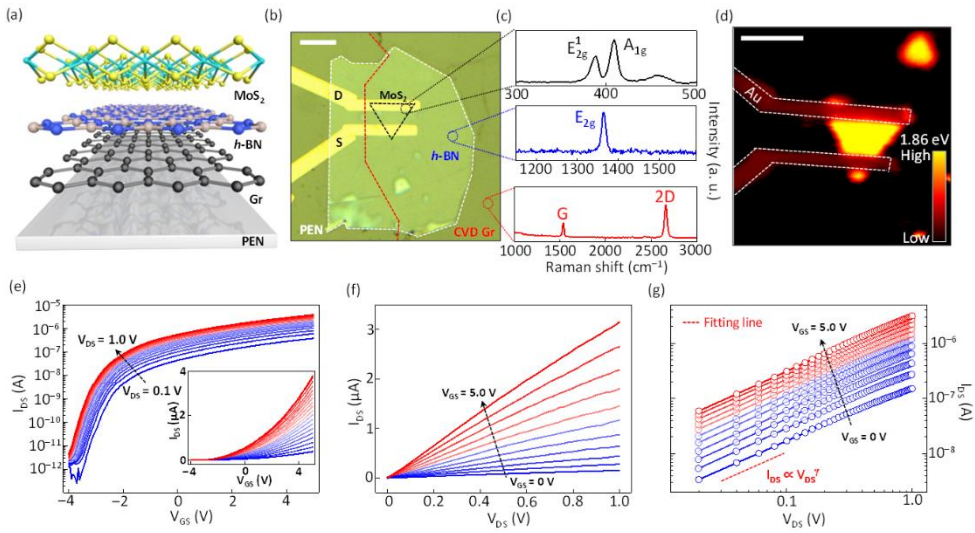


Figure 3.2. (a) The schematic of the vdW heterostructure on a PEN substrate. (b) Optical image of a fabricated fully transparent MoS_2 phototransistor. (c) Raman spectra for the CVD-grown monolayer MoS_2 and graphene (denoted as Gr), and mechanically exfoliated multilayer h -BN. Scale bar = $5 \text{ }\mu\text{m}$. (d) PL mapping image with a 1.86 eV peak intensity. Scale bar = $5 \text{ }\mu\text{m}$. (e) I_{DS} - V_{GS} and (f) I_{DS} - V_{DS} curves for the fully transparent MoS_2 phototransistor. (g) Logarithmic scale plot for I_{DS} - V_{DS} with an average γ value of 1.01.

3.3.2. Spectroscopic characteristics of the transparent MoS₂ phototransistors

Figure 3.3a shows the transmittance and reflectance of the device as stacking the individual layers; transparent substrate (PEN), CVD-grown monolayer graphene (denoted as Gr)/PEN, *h*-BN/Gr/PEN, and CVD-grown monolayer MoS₂/*h*-BN/Gr/PEN. Negligible absorption in the visible range for Gr and multilayer *h*-BN were verified through the observation of unchanged transmittance values after stacking the Gr and *h*-BN layers onto a PEN substrate. The absorbance of CVD-grown monolayer MoS₂ was determined by subtracting the reflectance of the MoS₂ layer from the diminished transmittance after stacking the MoS₂ layer onto an underlying *h*-BN/Gr/PEN layer (Figure 3.3b). The extracted absorbance of the MoS₂ layer was used as a reference to investigate the internal optoelectronic characteristics by absorbed photons, not incident photons in the MoS₂ channel. In Figure 3.3b, the resonance peaks A and B correspond to excitonic transitions split by spin-orbit coupling at the K point in *k*-space.^{22,27} The strong resonance peak C is ascribed to the parallel bands in the density of states even for excitation energy far exceeding the bandgap of MoS₂; this is called the band-nesting effect, which leads to a divergence in the joint density of states.^{28,29} By employing transparent layers of Gr, MoS₂, *h*-BN, and PEN, fully transparent MoS₂ phototransistors were implemented with high transparency, as shown in Figure 3.3c. Also, the incident laser-light fully penetrated through the fully stacked MoS₂ phototransistors without reflection or dispersion (right, Figure 3.3c).

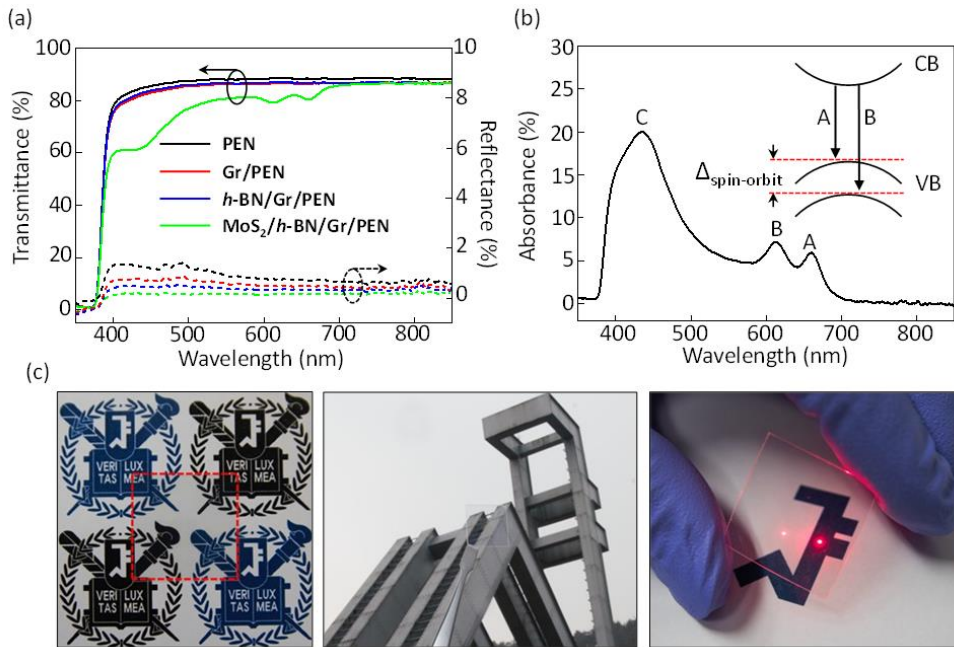


Figure 3.3. (a) Transmittances (solid lines) and reflectances (dashed lines) corresponding to each heterostructure. (b) Absorbance of the CVD-grown monolayer MoS₂ indicating three resonance peaks: A, B, and C. (c) Photographic images displaying high transparency.

3.3.3. Comparison of the optoelectronic characteristics of MoS₂ phototransistors on transparent and opaque substrates

To investigate the effects of the unintended photoresponsive characteristics, which are attributed to the use of an opaque substrate, CVD-grown monolayer MoS₂ phototransistors were fabricated with a *h*-BN dielectric on both a transparent PEN substrate (MoS₂/*h*-BN/Gr, denoted as MhG) and an opaque 100-nm-thick SiO₂/Si substrate (MoS₂/*h*-BN/heavily-doped silicon, denoted as MhS), as depicted in Figures 3.4a and 3.4b, respectively. The photoresponsive characteristics for MhG

and MhS were investigated under various illumination conditions with different light intensities ranging from 15 nW to 1180 nW at a fixed wavelength of 450 nm and

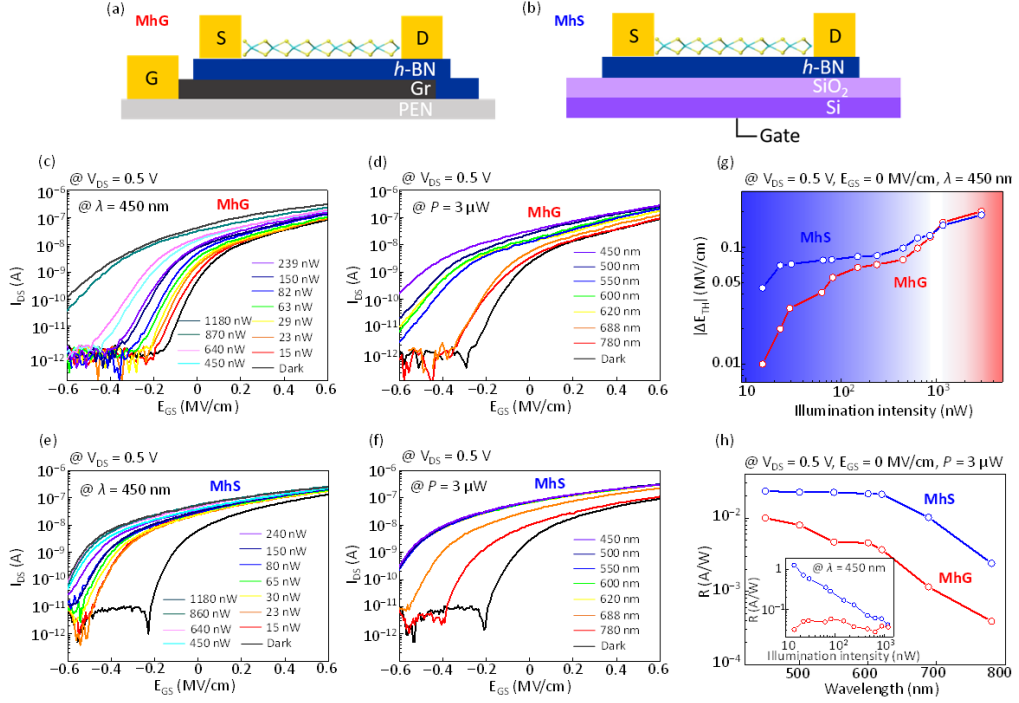


Figure 3.3. The schematics for (a) MhG and (b) MhS. The thickness for the multilayer h -BN was 41 nm and 28 nm for MhG and MhS, respectively. The range of E_{GS} (0.6 MV/cm) corresponds to an applied V_{GS} of 2.46 V and 7.68 V for MhG and MhS, respectively. (c-f) The photoresponsive characteristics of MhG and MhS under various illumination conditions with light intensity ranging from 15 nW to 1180 nW at a fixed wavelength of 450 nm, and wavelength ranging from 780 nm to 450 nm at a fixed intensity of 3 μ W. (g) E_{TH} variation versus illumination intensity and h) the wavelength-dependent responsivity of MhG and MhS at a fixed V_{DS} of 0.5 V and E_{GS} of 0 MV/cm.

with different wavelengths ranging from 780 nm to 450 nm at a fixed light intensity of 3 μ W in ambient air at room temperature (Figures 3.4c-3.4f). Note that the diameter of laser spot was ~ 1 μ m, smaller than the channel area dimension, so that the entire laser-light was focused within the MoS₂ channel area. As shown in Figures

3.4c-3.4f, the photoinduced current steadily increased in both types of devices, MhG and MhS, as the illumination intensity became stronger at a fixed wavelength (Figures 3.4c and 3.4e) and also as the wavelength of the incident light became shorter at a fixed illumination intensity (Figures 3.4d and 3.4f). As shown in Figures 3.4d and 3.4f, the electron-hole pairs could be created by illumination with laser photon energy (1.59 eV and 1.80 eV, corresponding to 780 nm and 688 nm, respectively) smaller than the optical bandgap energy of MoS₂ (1.9 eV)³⁰ via the excitation of carriers localized in band tail states. For a more accurate comparison, the gate electric field (E_{GS}) instead of V_{GS} was used as the x-axis in Figures 3.4c-3.4f because of the different thicknesses of the dielectric layers in MhG and MhS. There were two noticeable distinctions in the photoresponsive characteristics for MhG and MhS: 1) the amount of change in the threshold electric field (ΔE_{TH}) in MhS due to illumination was larger than that in MhG (Figure 3.4g), and 2) the responsivity (R) of MhS was higher than that of MhG (Figure 3.4h). To understand the difference in the photoresponsive properties between MhG and MhS, the components of the photoinduced current should be classified.

To date, various mechanisms for the photoinduced current in MoS₂ have been proposed, such as the photoelectric (PE), photothermoelectric (PTE), photogating (PG), and photoconductive (PC) effects. Typically, the PE and PTE effects dominate in the photoresponse in cases without an electric field; therefore, the PG and PC effects dominantly determine the photoconductivity in phototransistors when an electric field is applied.²⁰ The PG effect is attributed to structural defects in MoS₂ itself or to disorder caused by the imperfect interface with the substrate at which the photogenerated electrons or holes can be trapped, playing the role of a local gate electric field. In *n*-type MoS₂-based FETs, a negative shift in the threshold voltage

(V_{TH}) is typically observed due to the PG effect via the trapped photogenerated holes.²⁰ In contrast, the PC effect corresponds to the contribution of increased channel current due to the photogenerated carriers in the channel, which influence V_{TH} less. So, the total photocurrent (I_{ph}) can be expressed as

$$I_{ph} = I_{ph,PG} + I_{ph,PC} = g_m |\Delta V_{TH}| + \left(\frac{W}{L}\right) V_{DS} \Delta\sigma \quad , (2)$$

where $g_m = \frac{dI_{DS}}{dV_{GS}}$ is the transconductance and $\Delta\sigma = q\mu_n\Delta n$ is the change in conductivity due to the photogenerated carriers. Although the proportion between the PG and PC effects differs depending on the device structure, typically, the PG effect is more dominant in vdW materials.²⁰ If photogenerated minority carriers are trapped with a certain spatial distribution, their lifetime becomes prolonged; therefore, this can produce an additional gate electric field until they disappear through recombination.^{31,32} When the majority carriers pass through the channel for contributing to the photocurrent, additional majority carriers should be injected into the channel to preserve charge neutrality until the trapped photogenerated holes disappear.^{31,32} Therefore, the photoresponsive characteristics in vdW materials-based phototransistors can be amplified by trapping photogenerated minority carriers as well as by applied electric fields for accelerating the movement of the majority carriers.

In this regard, the higher value of $|\Delta E_{TH}|$ for MhS in the low illumination intensity regime than that for MhG (blue area in Figure 3.4g) indicates that the PG effect in MhS was stronger than that in MhG in the low illumination intensity regime. This behavior is due to the influence of the reflected light from the SiO₂/Si substrate along with the PG effect. In our study, the PG effect arises dominantly from the trapped holes at the intrinsic defects such as sulfur vacancies in MoS₂,³³ but not at

the interface trap sites because the underlying inserted *h*-BN layer provided a near-ideal interface with MoS₂. Therefore, the reflected light from the SiO₂/Si substrate in MhS can generate more trapped photogenerated holes, which leads to the enhanced PG effect in MhS in the low illumination intensity regime. However, in the high illumination intensity regime, most trap sites can be occupied by sufficient photogenerated holes in both MhS and MhG. Thus, the values for $|\Delta E_{TH}|$ for MhS and MhG became comparable in the high illumination intensity regime (red area in Figure 3.4g).

Figure 3.4h shows the responsivity for MhS and MhG as a function of wavelength measured at a fixed V_{DS} of 0.5 V, E_{GS} of 0 MV/cm, and illumination intensity (P) of 3 μ W. Note that the maximum power for the illumination intensity was restricted up to 3 μ W to prevent any undesirable physical damage to the atomically thin monolayer MoS₂ channel. The responsivity (R) is an important parameter for evaluating the performance for photodetector applications, which is defined as

$$R = \frac{I_{Ph}}{P_{Light}} \quad , \quad (3)$$

where P_{Light} is the illumination intensity. We observed a higher responsivity for MhS than that for MhG under various wavelengths ranging from 780 nm to 450 nm at a fixed intensity of 3 μ W, as shown in Figure 3.4h. This result is also attributed to the light reflected from the SiO₂/Si substrate along with the PC effect. Because the PG effects in MhS and MhG are comparable under high intensity illumination, the reason for the higher responsivity of MhS is attributed to the stronger PC effect in MhS, which originates from additional carrier creation by the reflected light from the SiO₂/Si substrate (Figure 3.4h). In addition, the responsivity under the various

illumination intensities ranging from 15 nW to 1180 nW at a fixed wavelength of 450 nm is indicated in the inset of Figure 3.4h. Due to the stronger PG effect in MhS in the low illumination intensity regime, a much higher responsivity was observed in MhS than in MhG; then, the responsivity values became comparable between MhS and MhG as the illumination intensity was increased (inset of Figure 3.4h). As the illumination intensity increased, the responsivity of MhS was reduced, whereas a nearly constant responsivity was observed for MhG. The decline of the responsivity for increasing illumination intensity for MhS can be explained in terms of restricted trap sites. In the low illumination intensity regime, a substantial portion of the photogenerated holes can be trapped and act as a positive gate electric field, leading to increased responsivity. On the other hand, in the high illumination intensity regime, the possibility for trapping becomes lower due to a sufficient number of photogenerated holes being more than the number of trap sites, which results in reduced responsivity (inset of Figure 3.4h). Similar phenomena have been reported in MoS₂ phototransistors.^{34,35} Therefore, the photoresponsive characteristics in MoS₂ phototransistors fabricated on opaque substrates are overestimated, which cannot be regarded as the intrinsic optoelectronic characteristics of monolayer MoS₂.

3.3.4. Intrinsic optoelectronic characteristics of transparent MoS₂ phototransistors under visible light

To explore the intrinsic optoelectronic properties of MoS₂, the dependencies of the optoelectronic characteristics of transparent MhG on V_{GS} and wavelength were investigated (Figure 3.5). The contour plots indicating external and internal responsivities as a function of V_{GS} and wavelength measured at a V_{DS} of 0.5 V are

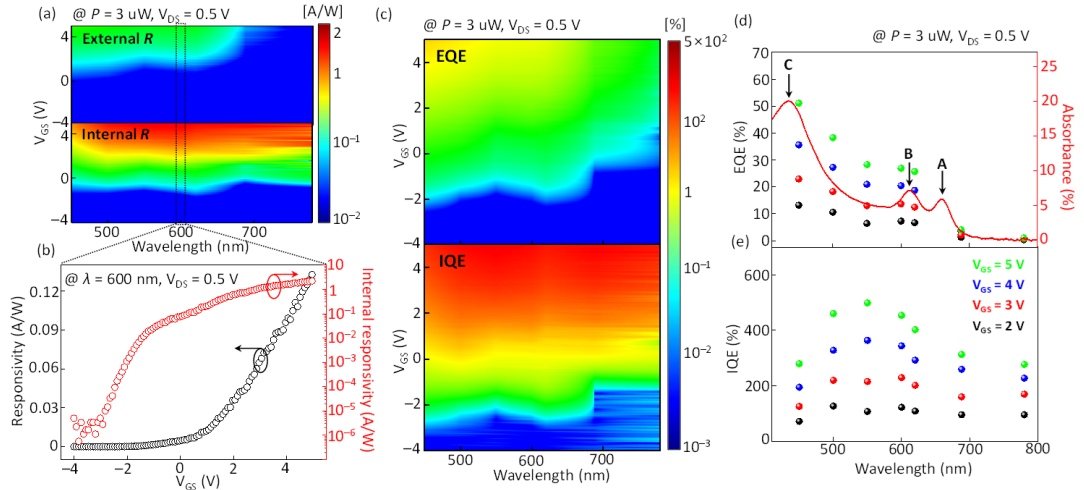


Figure 3.5. (a) Contour plots indicating external (upper panel) and internal (lower panel) responsivities as a function of V_{GS} and wavelength at a fixed V_{DS} of 0.5 V and illumination intensity of $3 \mu\text{W}$. (b) The external and internal responsivities at a fixed wavelength of 600 nm. (c) Contour plots comparing EQE (upper panel) and IQE (lower panel) at a fixed V_{DS} of 0.5 V and illumination intensity of $3 \mu\text{W}$. The wavelength-dependent (d) EQE and (e) IQE values (colored circle symbols) corresponding to each V_{GS} . Absorbance for a CVD-grown MoS_2 monolayer is indicated as a red solid line in (d).

displayed in Figure 3.5a. Because the internal and external responsivity values are defined as the photocurrent per watt of the absorbed and incident illumination intensity, respectively, the internal responsivity is calculated by dividing the external responsivity by the absorbance of the MoS_2 layer (Figure 3.3b). In other words, the values for the internal responsivity are higher than those for the external responsivity under the entire range of wavelengths (Figure 3.5a). To achieve the maximum responsivity in phototransistors, low illumination intensity, high V_{DS} , and high V_{GS} are required. Under optimum measurement conditions, a maximum external responsivity of 16.8 A/W and maximum internal responsivity of $3.2 \times 10^2 \text{ A/W}$ were achieved (Figure 3.6). Figure 3.5c exhibits contour plots comparing the external

quantum efficiency (EQE) and internal quantum efficiency (IQE) versus V_{GS} and

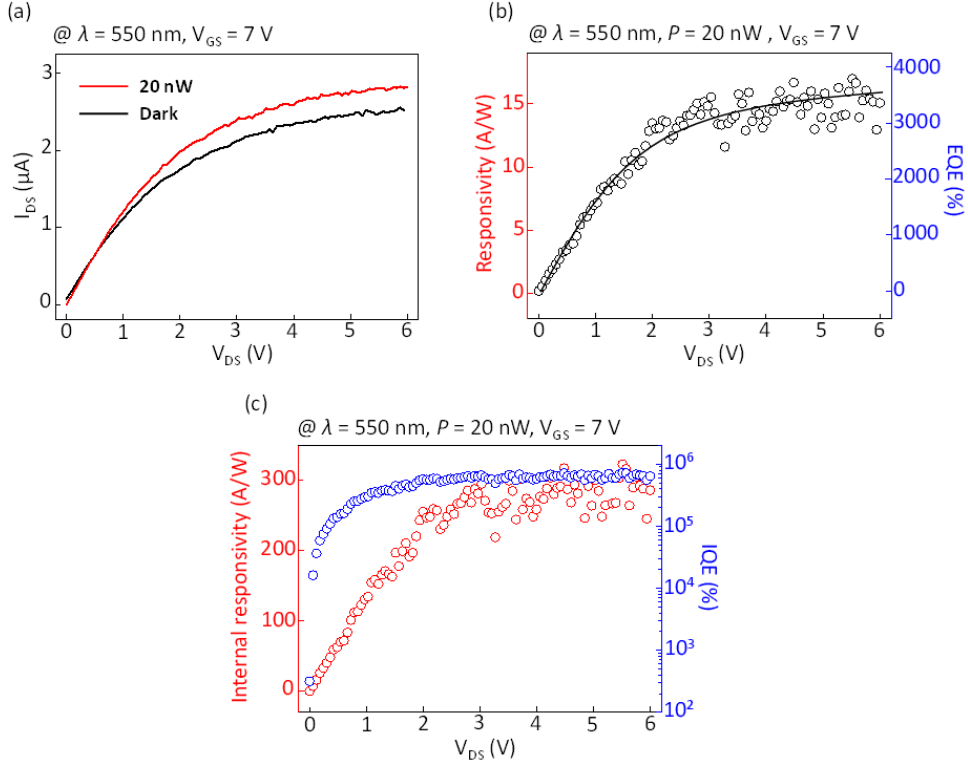


Figure 3.6. V_{DS} -dependent photoresponsive characteristics of transparent MoS₂ phototransistor.

wavelength for a transparent MoS₂ phototransistor measured at V_{DS} of 0.5 V and illumination intensity of 3 μW. EQE and IQE are defined as the number of carriers detected per incident photon and absorbed photon, respectively, as defined by the following formula:

$$\text{EQE (\%)} = \frac{I_{Ph}/e}{P_{Inc}/h\nu} \times 100 \quad \text{and} \quad \text{IQE (\%)} = \frac{I_{Ph}/e}{P_{Abs}/h\nu} \times 100 \quad , \quad (4)$$

where P_{Inc} , P_{Abs} , and $h\nu$ are the incident illumination intensity, absorbed illumination intensity, and photon energy, respectively. Similar to the dependency of the responsivity on V_{GS} (Figure 3.5b), EQE and IQE also increased with increasing V_{GS} at a fixed V_{DS} of 0.5 V (Figure 3.5c). For an in-depth understanding of the

quantum efficiency dependence on the wavelength of the light, the EQE values extracted from the contour plot of Figure 3.5c are exhibited in Figure 3.5d. Note that the condition of $V_{GS} > V_{TH}$ ranging from 2 V to 5 V was taken into account in Figures 3.5d and 3.5e in which photogenerated carriers can contribute to the photocurrent efficiently. An abrupt increase in EQE was observed at a wavelength of around 620 nm due to the A- and B-excitonic transitions represented as the resonance peaks in the absorbance of MoS₂ (red line curve in Figure 3.5d). Higher EQE was also observed near the strong resonance peak at ~440 nm corresponding to the C-excitonic transition induced by the band-nesting effect.^{28,29}

In contrast, the IQE values by the C-excitonic transition were lower than those by the A- or B-excitonic transition, as shown in Figure 3.5e. Previous studies of the C-excitonic transition in MoS₂ reported that the photogenerated electrons and holes in the band-nesting region are well separated in k -space to their immediate band extremum.^{29,36} Because the photogenerated electrons and holes in the band-nesting region move quickly to the Λ valley and Γ hill,^{28,29,36} respectively, on an extremely fast intraband relaxation time scale of C-exciton (< 500 fs),³⁷ a more enhanced photodetection ability could be expected under the C-excitonic transition due to the suppression of direct band-to-band recombination.³⁶ However, contrary to this anticipation, the photogenerated carriers excited by the A- or B-excitonic transition produced a higher IQE than that produced by the C-excitonic transition (Figure 3.5e). Note that a similar consequence was observed in the internal responsivity Figure 3.7. These phenomena can be explained by the different effective masses of the carriers located at different positions in k -space. For the photodetection ability in n -type

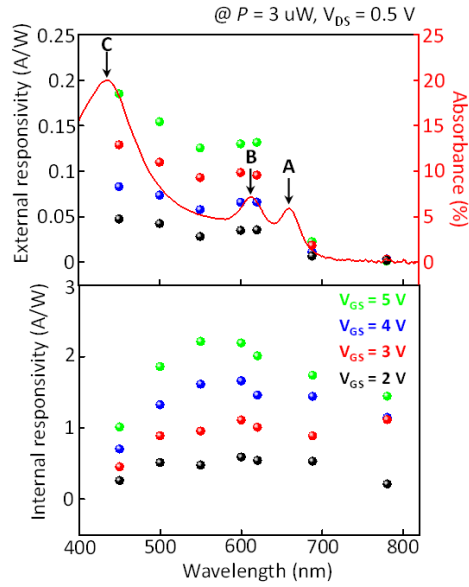


Figure 3.7. The wavelength-dependent external and internal responsivities (colored circle symbols) corresponding to each V_{GS} . Absorbance of monolayer MoS₂ layer is indicated as a red solid line.

MoS₂ phototransistors, the effective mass of the electron is typically a more significant parameter because majority carriers (electrons) are accelerated by applied electric fields, thus contributing to the photocurrent, while minority carriers (holes) are trapped with a long lifetime. However, regardless of the types of carriers, the effective mass of the electron (hole) located at the Λ valley (Γ hill) created by the C-excitonic transition is heavier than that created by the A- or B-excitonic transitions at the K point.^{38,39} In this manner, although the electron-hole pairs photogenerated by the C-excitonic transition can be easily separated without extinction by recombination, the IQE values under illumination at 450 nm (C-excitonic transitions) were 58% of those under illumination at 600 nm (B-excitonic transition), as extracted from the results measured at V_{GS} from 2 V to 5 V (Figure 3.5e). Interestingly, in contrast to the EQE and external responsivity, the IQE and internal responsivity did

not exhibit a significant dependence on the wavelength of visible light. In addition, the IQE can also be amplified up to 7.1×10^5 % by the applied electric fields (V_{GS} and V_{DS}) under low illumination intensity (Figure 3.6).

3.3.5. Time-resolved photoresponse characteristics in transparent MoS₂ phototransistors

We investigated the temporal evolution of the photoresponse of MhG measured at a V_{DS} of 1.0 V and 0.1 V and at a fixed V_{GS} of -2 V (illuminated by a laser with a wavelength of 620 nm and an intensity of 20 nW), as shown in Figure 3.8a. After illuminating the MoS₂ channel for 100 s, the decay process for the photoinduced current was examined after turning the laser off. The decay process followed an exponential decay function with two different decay constants (τ_1 and τ_2) according to the time range.⁴⁰ Even though high-quality MoS₂ phototransistors with a vdW heterostructure were realized, a long-lasting photoconductivity was inevitably observed after turning the laser off (Figure 3.8).^{16,20,34} The origin for the long-lasting photoconductivity in the decay has been described as being due to the influence of random local potential fluctuations (RLPF) in the band structure^{41,42} and influence of the trapped photogenerated minority carriers that hinder recombination in the forbidden gap of MoS₂.^{16,31-33} The confined carriers can escape the potential even after the laser is turned off and then contribute to the photocurrent, resulting in a long decay time. In addition, the trapped photogenerated holes in MoS₂ consistently induce the injection of electrons for charge neutrality until they disappear through the recombination process. In this regard, the increase in V_{DS} from 0.1 V to 1.0 V promoted the release of confined carriers in RLPF and reduced the lifetime of the

trapped photogenerated holes, so the τ_1 (τ_2) value decreased from 66.8 s (86.5 s) to 14.0 s (56.3 s), as shown in Figures 3.8a and 3.8b. Figure 3.8c shows the time-resolved photoresponse under illumination with different intensities of 1150 nW and 40 nW measured at a fixed V_{GS} of -2 V and V_{DS} of 1 V (illuminated by a laser with a wavelength of 620 nm). Because the high illumination intensity created more photogenerated electron-hole pairs, which leads to increased carrier confinement in RLPF or in the trap sites in the forbidden gap, the τ_1 (τ_2) value increased from 20.2 s (53.8 s) to 24.9 s (60.9 s) as the illumination intensity was increased from 40 nW to 1150 nW (Figure 3.8d).

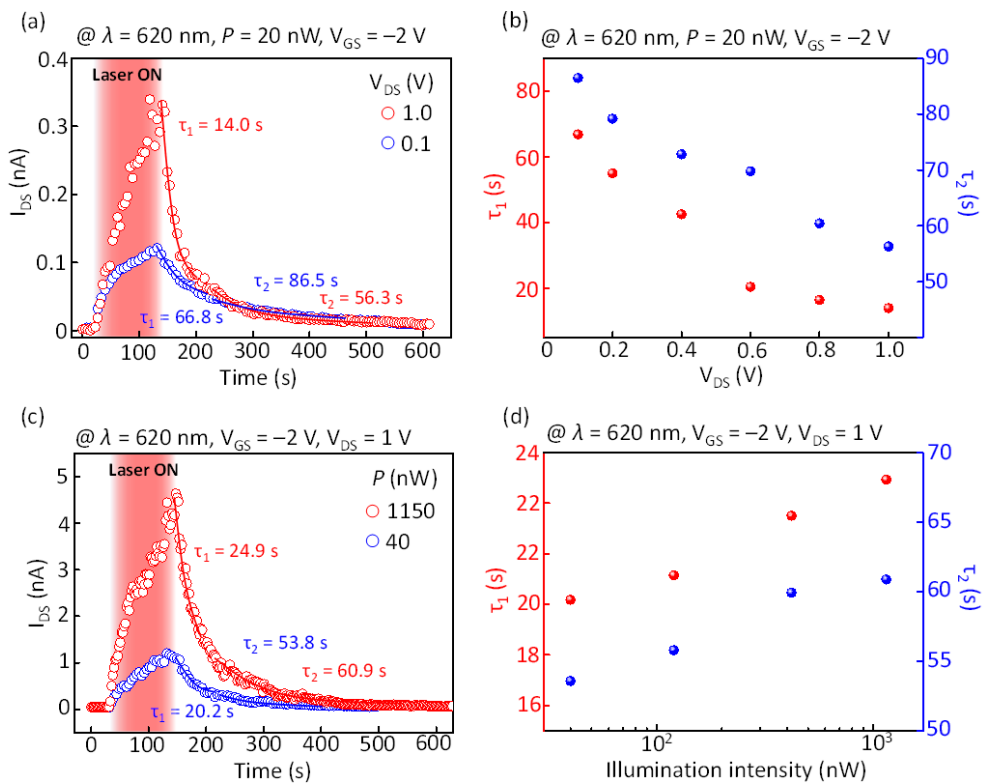


Figure 3.8. (a) Photoswitching characteristics of a fully transparent MoS₂ phototransistor under illumination of the MoS₂ channel for 100 s at different V_{DS} conditions of 1.0 V (red open circle symbols) and 0.1 V (blue open circle symbols)

at a fixed V_{GS} of -2 V. The solid lines are lines fitted by an exponential decay function. (b) τ_1 and τ_2 versus V_{DS} ranging from 0.1 V to 1.0 V. (c) Photoswitching characteristics at different illumination intensities of 1150 nW (red open circle symbols) and 40 nW (blue open circle symbols) at a fixed V_{DS} of 1 V. (d) τ_1 and τ_2 versus the illumination intensity ranging from 40 nW to 1150 nW.

Conclusion

This work explores, for the first time, the internal optoelectronic characteristics of monolayer MoS₂ in fully transparent phototransistors by employing a 2D vdW heterostructure. From the systematic comparison of the optoelectronic characteristics between transparent and opaque MoS₂ phototransistors, it turns out that the photoresponsive characteristics of MoS₂ are overestimated due to enhanced photogating and photoconductive effects originating from the use of opaque substrates. In addition, we found that a maximum internal responsivity of 3.2×10^2 A/W and IQE of 7.1×10^5 % were yielded in a fully transparent MoS₂ phototransistor, which can be regarded as the intrinsic optoelectronic characteristics of CVD-grown monolayer MoS₂. Interestingly, in contrast with the external photoresponse, which was highly wavelength-dependent, the internal photoresponse did not significantly depend on the wavelength of the incident light. Furthermore, relatively lower IQE values at the C-excitonic transitions than those at the A- or B-excitonic transition show different optoelectronic properties depending on the locations of the photogenerated carriers in k -space due to their different effective masses. Our study will shed on light the understanding of the intrinsic optoelectronic characteristics of CVD-grown monolayer MoS₂, and it will provide a deep insight into the realization of 2D materials-based transparent optoelectronics.

Figure captions

Figure 3.1. Schematics of the fabrication processes for transparent MoS₂ FETs.

Figure 3.2. (a) The schematic of the vdW heterostructure on a PEN substrate. (b) Optical image of a fabricated fully transparent MoS₂ phototransistor. (c) Raman spectra for the CVD-grown monolayer MoS₂ and graphene (denoted as Gr), and mechanically exfoliated multilayer *h*-BN. Scale bar = 5 μ m. (d) PL mapping image with a 1.86 eV peak intensity. Scale bar = 5 μ m. (e) $I_{DS}-V_{GS}$ and (f) $I_{DS}-V_{DS}$ curves for the fully transparent MoS₂ phototransistor. (g) Logarithmic scale plot for $I_{DS}-V_{DS}$ with an average γ value of 1.01.

Figure 3.3. (a) Transmittances (solid lines) and reflectances (dashed lines) corresponding to each heterostructure. (b) Absorbance of the CVD-grown monolayer MoS₂ indicating three resonance peaks: A, B, and C. (c) Photographic images displaying high transparency.

Figure 3.4. The schematics for (a) MhG and (b) MhS. The thickness for the multilayer *h*-BN was 41 nm and 28 nm for MhG and MhS, respectively. The range of E_{GS} (0.6 MV/cm) corresponds to an applied V_{GS} of 2.46 V and 7.68 V for MhG and MhS, respectively. (c-f) The photoresponsive characteristics of MhG and MhS under various illumination conditions with light intensity ranging from 15 nW to 1180 nW at a fixed wavelength of 450 nm, and wavelength ranging from 780 nm to 450 nm at a fixed intensity of 3 μ W. (g) E_{TH} variation versus illumination intensity and h) the wavelength-dependent responsivity of MhG and MhS at a fixed V_{DS} of 0.5 V and E_{GS} of 0 MV/cm.

Figure 3.5. (a) Contour plots indicating external (upper panel) and internal (lower panel) responsivities as a function of V_{GS} and wavelength at a fixed V_{DS} of 0.5 V and illumination intensity of 3 μ W. (b) The external and internal responsivities at a fixed wavelength of 600 nm. (c) Contour plots comparing EQE (upper panel) and IQE (lower panel) at a fixed V_{DS} of 0.5 V and illumination intensity of 3 μ W. The wavelength-dependent (d) EQE and (e) IQE values (colored circle symbols)

corresponding to each V_{GS} . Absorbance for a CVD-grown MoS₂ monolayer is indicated as a red solid line in (d).

Figure 3.6. V_{DS} -dependent photoresponsive characteristics of transparent MoS₂ phototransistor.

Figure 3.7. The wavelength-dependent external and internal responsivities (colored circle symbols) corresponding to each V_{GS} . Absorbance of monolayer MoS₂ layer is indicated as a red solid line.

Figure 3.8. (a) Photoswitching characteristics of a fully transparent MoS₂ phototransistor under illumination of the MoS₂ channel for 100 s at different V_{DS} conditions of 1.0 V (red open circle symbols) and 0.1 V (blue open circle symbols) at a fixed V_{GS} of -2 V. The solid lines are lines fitted by an exponential decay function. (b) τ_1 and τ_2 versus V_{DS} ranging from 0.1 V to 1.0 V. (c) Photoswitching characteristics at different illumination intensities of 1150 nW (red open circle symbols) and 40 nW (blue open circle symbols) at a fixed V_{DS} of 1 V. (d) τ_1 and τ_2 versus the illumination intensity ranging from 40 nW to 1150 nW.

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Chapter 4. Effect of facile p-doping on electrical and optoelectronic characteristics of ambipolar WSe₂ field-effect transistors

In this Chapter, beyond MoS₂ material, the effects of p-doping on electrical and optoelectronic characteristics of ambipolar WSe₂ phototransistors were explored. WO₃ layers formed by the annealing introduced p-doping to WSe₂ FETs, resulting in the shift of the transfer curve to the positive gate voltage direction. We achieved considerably improved photoswitching response characteristics of WSe₂ FETs after the annealing. X-ray photoelectron spectroscopy, photoluminescence, and photoswitching experiments were performed to investigate the origins of the changes in the electrical and optoelectronic properties. From these analyses, it was found that long-lasting photoconductivity after turning off light irradiation on WSe₂ FETs could be explained by additional charge injection induced by trapped photogenerated minority carriers. Furthermore, disorder originated from the WO₃/WSe₂ interfaces acted as non-radiative recombination sites, leading to significantly improved photoswitching response time characteristics.

4.1. Introduction

2D materials have attracted considerable interest as promising candidates for next-generation electronics and optoelectronic devices.^{1,2} Although graphene is one of the most well-studied 2D materials, it lacks an intrinsic bandgap, restricting its wide application. Meanwhile, 2D TMDs, such as MoS₂, MoSe₂, WS₂, and WSe₂, are advantageous in that they can be used as a channel material of FETs due to their intrinsic bandgap properties, good carrier mobility, and high on/off ratio.^{2,3} Hence, TMDs have been widely used in various devices, such as transistors,⁴⁻⁶ sensors,⁷ logic circuits,⁸ memory devices,⁹ field-emission devices,¹⁰ and photodetectors.^{11,12}

In particular, FETs based on WSe₂ have demonstrated great performance characteristics such as high effective hole mobility, outstanding photoresponsive properties, excellent mechanical flexibility, and durability.¹³⁻¹⁵ Nevertheless, doping WSe₂ is required to further improve field-effect mobilities or contact properties which are essential in diverse electronic applications.^{13,16} WO₃ has been demonstrated as an efficient p-type dopant since it can be formed by simply oxidizing WSe₂ via oxygen or ozone treatment.¹⁷⁻¹⁹ With this method, enhancement of the electrical properties of WSe₂ FETs has been reported. For example, Liu *et al.* thermally annealed WSe₂ films in ambient without use of additional substances to dope the films in the p-type manner and improved the hole mobility to 83 cm² V⁻¹ s⁻¹ with employing hexagonal boron nitride substrate.¹⁷ However, thorough studies on the optical and optoelectronic characteristics of WSe₂ doped by WO₃ are desired for the optoelectronic applications such as phototransistors, photodiodes, and light-emitting diodes.^{14,15,20,21}

In this work, we studied the electrical, optical, and optoelectronic properties of

ambipolar WSe₂ FETs before and after thermal annealing in ambient. The oxidized layer (WO₃) generated at the WSe₂ surface during the annealing introduced p-doping to the WSe₂ FETs, leading to a shift of the transfer curve to the positive gate voltage direction. Interestingly, long-lasting photoconductivity, which is a phenomenon of the conductance's being retained after the light irradiation is turned on, disappeared after the annealing at a fixed gate voltage. We also performed various experiments, such as X-ray photoelectron spectroscopy (XPS), photoluminescence (PL) spectroscopy, Raman spectroscopy, and photoswitching characterization at various gate voltages to investigate the origin of the changes in the electrical and photoswitching characteristics of the WSe₂ FETs.

4.2. Experiments

Figure 4.1 shows a process of WSe₂ FET fabrication. First, we prepared 270 nm-thick SiO₂ layer on a heavily doped p⁺⁺ Si wafer (resistivity $\sim 5 \times 10^{-3} \Omega \text{ cm}$) which was used as a common back gate. And, WSe₂ flakes were mechanically exfoliated from a bulk WSe₂ crystal (purchased from SPI Supplies). Then, the WSe₂ flakes were transferred from a scotch tape to the SiO₂ surface. After finding locations of the target WSe₂ flakes using an optical microscope, thickness of the WSe₂ flakes was measured by an atomic force microscope (NX 10 AFM, Park Systems). Next, we spin-coated poly(methyl methacrylate) (PMMA) 495K (11% concentration in anisole) at 4000 rpm as an electron resist layer. The samples were baked on a hot plate at 180 °C for 90 s after the spin coating. The patterns of the electrodes were made by an electron beam lithography (JSM-6510, JEOL), and the exposed PMMA regions were developed with a methyl isobutyl ketone/isopropyl alcohol (1:3) solution for 120 s.

Finally, Ti metal (30 nm-thick) used as the electrodes was deposited with an electron-beam evaporator system (KVE-2004L, Korea Vacuum Tech). The deposited Ti was lifted off by an acetone with lift-off time of 300 s.

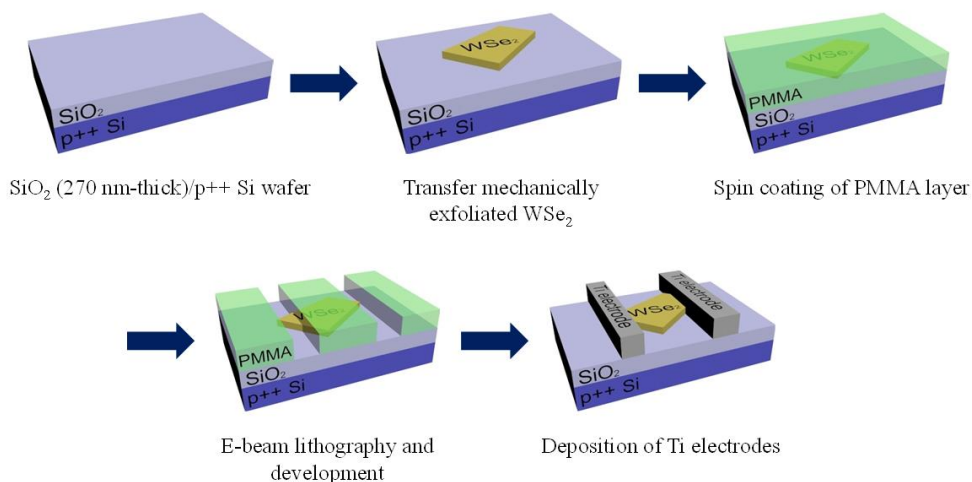


Figure 4.1. Schematics of fabricating WSe₂ FET.

4.3. Results and discussions

4.3.1. Change of electrical and photoswitching characteristics

Figure 4.2(a) shows the optical images of a WSe₂ flake and a FET fabricated from this WSe₂ flake. The WSe₂ flake was mechanically exfoliated from a bulk WSe₂ crystal (purchased from SPI Supplier, USA) and transferred on a 270 nm-thick SiO₂ surface on a heavily doped p++ Si wafer that was used as the back gate of the FET. Next, Ti metal (30 nm-thick) patterns used as source and drain electrodes were deposited on the WSe₂ surface. A schematic of the fabricated WSe₂ FET is shown in Figure 4.2(b). All the electrical and photoswitching properties of WSe₂ FETs were measured in vacuum ($\sim 3.5 \times 10^{-3}$ Torr) since the oxygen and water molecules in the

air can affect the properties of the WSe₂ FETs. For instance, it has been reported that WSe₂ FETs can change from n- to p-type by air exposure.²² An atomic force microscopy (AFM) image of the WSe₂ flake shown in Figure 4.2(a) is displayed in Figure 4.2(c) with the topographic cross-sectional profile. The measured thickness of the WSe₂ flake across the blue line was found to be ~1.2 nm (inset graph in Figure 4.2(c)), corresponding to bilayer WSe₂ (the thickness of a WSe₂ monolayer is ~0.7 nm).¹³ Please note that only a part of the WSe₂ flake where the surface was flat was used as a channel of the FET. Figure 4.2(d) displays the Raman spectrum of a WSe₂ flake showing two clear peaks (the peak at 520 cm⁻¹ is assigned to the Si substrate). The Raman peak at 245 cm⁻¹ corresponds to the in-plane (E_{2g}¹ mode) or out-of-plane (A_{1g} mode) vibrations of WSe₂, and the Raman peak at 308 cm⁻¹ corresponds to the B_{2g}¹ mode that only appears in multilayer WSe₂ due to the additional interlayer interaction.²³ This finding ensures the good quality of the WSe₂ flake used in these experiments. The E_{2g}¹ and A_{1g} peaks of WSe₂ could not be distinguished by the Raman spectroscopy instrument in this study because they are nearly degenerate.²⁴ Figure 4.2(e) shows the transfer curve (source-drain current versus gate voltage; *I*_{DS}-*V*_{GS} curve) of the WSe₂ FET. Typical ambipolar characteristics were observed. Such an ambipolar transport behavior of the WSe₂ FET with a bilayer WSe₂ channel is in agreement with the previous studies which reported that the carrier type of the WSe₂ FETs could be modulated by the changes in the thickness of the WSe₂ flakes.²⁵

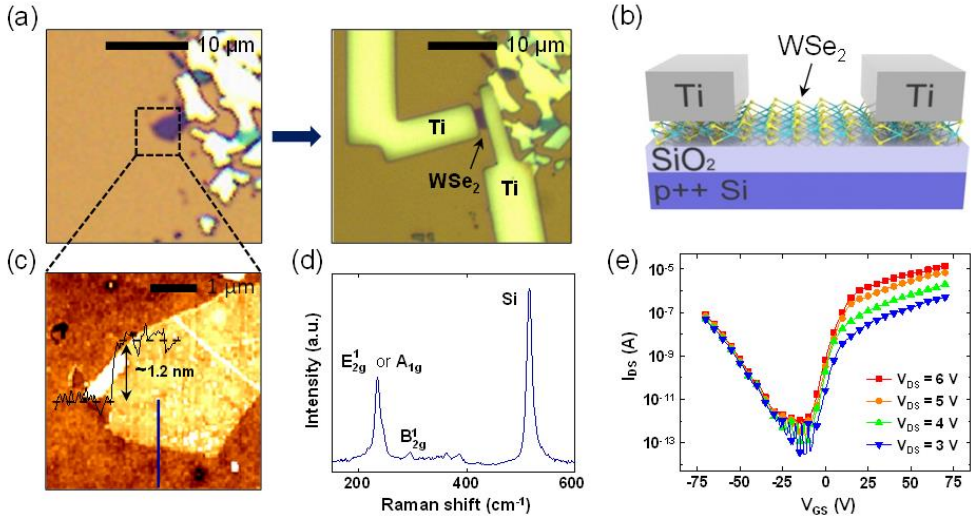


Figure 4.2. (a) Optical images of a WSe₂ flake (left) and fabricated WSe₂ FET (right). (b) An AFM image of the WSe₂ flake. The thickness of the WSe₂ flake (along the blue line) was found to be ~1.2 nm. (c) Raman spectra of a WSe₂ flake. (d) Schematic of the fabricated WSe₂ FET with Ti contacts. (e) I_{DS} - V_{GS} curves of the WSe₂ FET.

Figure 4.3(a) shows the I_{DS} - V_{GS} curves of the WSe₂ FET before and after a thermal annealing in ambient at 200 °C for 1 h. Several points are noted here. First, the voltage at which the type of the majority carriers changes ($V_{n \leftrightarrow p}$) shifted from -15 V to -5 V after the annealing in ambient (represented by the green arrow in Figure 4.3(a)). Second, the I_{DS} increased significantly at the V_{GS} where the majority carriers are holes ($V_{GS} < V_{n \leftrightarrow p}$) and decreased at the V_{GS} where the majority carriers are electrons ($V_{GS} > V_{n \leftrightarrow p}$) after the annealing (represented by the blue arrows in Figure 4.3(a)). This behavior is attributed to the WO₃ layer formed by the annealing that introduces p-doping into the WSe₂ FETs.¹⁷ Third, after the annealing, the hole mobility increased from 0.13 cm² V⁻¹ s⁻¹ to 1.3 cm² V⁻¹ s⁻¹, and the electron mobility decreased from 5.5 cm² V⁻¹ s⁻¹ to 0.69 cm² V⁻¹ s⁻¹. We used the formula $\mu = (dI_{DS}/dV_{GS})$

$\times [L/(WC_iV_{DS})]$ to calculate the carrier mobility, where L ($\sim 1.5 \mu\text{m}$) is the channel length, W ($\sim 2.8 \mu\text{m}$) is the channel width, and $C_i = \epsilon_0\epsilon_r/d = 1.3 \times 10^{-4} \text{ F m}^{-2}$ is the capacitance between the WSe₂ and the p⁺⁺ Si wafer per unit area. Here, ϵ_r (~ 3.9) is the dielectric constant of SiO₂ and d (270 nm) is the thickness of the SiO₂ layer. These changes in the electrical properties after the annealing can be observed more clearly in the contour plots that show the I_{DS} as a function of V_{GS} and V_{DS} before (top) and after (bottom) the annealing in ambient (Figure 4.3(b)). These contour plots were made based on a lot of I_{DS} - V_{GS} curves measured in the V_{GS} range from -70 V to 70 V with a 1.25 V step and V_{DS} range from 3 V to 6 V with a 0.25 V step. The blue regions in the contour plots shifted toward the positive V_{GS} direction after the annealing. This shift is consistent with the transfer curve shift shown by the green arrow in Figure 4.3(a). The change in the color at the positive and negative V_{GS} (Figure 4.3(b)) after the annealing indicates the change in the channel current of the WSe₂ FET (Figure 4.3(a)). Other WSe₂ FETs also showed the same change in the electrical properties after annealing in ambient (see supplementary material, Figs. S3 and S4). Besides, the change of electrical characteristics by the annealing the WSe₂ FET in vacuum ($\sim 4.5 \times 10^{-4}$ Torr) at 200 °C for 1 h were investigated (Figs. 2(c) and 2(d)). In contrast with the results of the FET annealed in ambient, the I_{DS} increased at both V_{GS} conditions of $V_{GS} > V_{n \leftrightarrow p}$ and $V_{GS} < V_{n \leftrightarrow p}$. The increased I_{DS} obtained by annealing in vacuum is attributed to the improved WSe₂-Ti contacts without formation of WO₃.²⁶ From the comparison results, it can be anticipated that p-doping was introduced by interaction with the oxygen molecules during the annealing in ambient. The origins of the change in the electrical characteristics are discussed in more detail via the analysis of XPS data afterward.

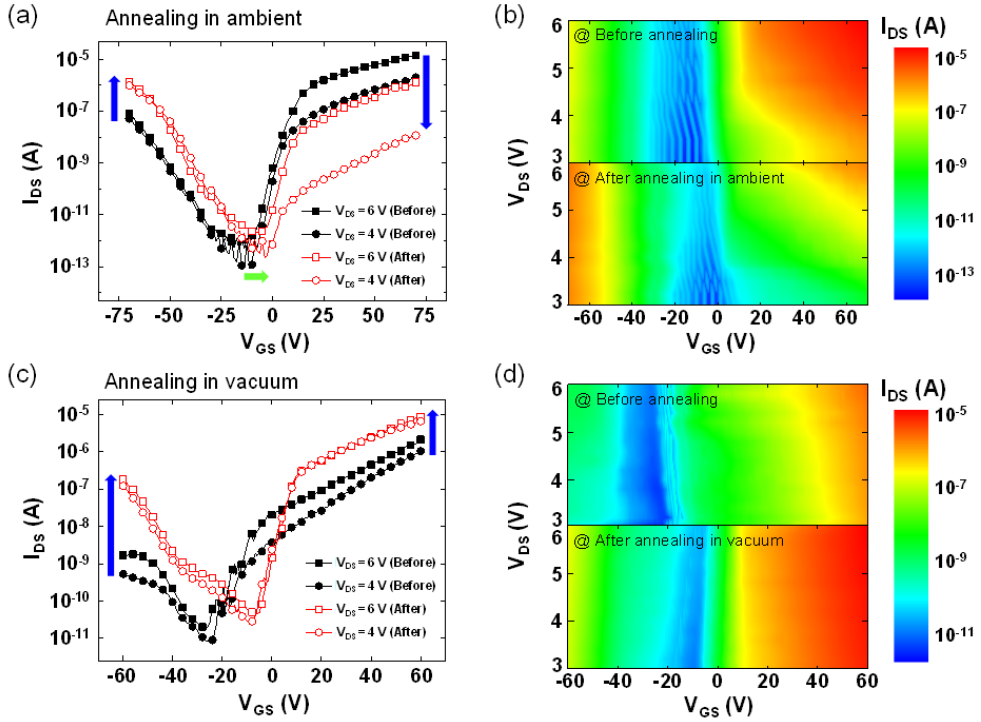


Figure 4.3. (a) I_{DS} – V_{GS} curves on the semilogarithmic scale of a WSe₂ FET before annealing and after annealing in ambient at 200 °C for 1 h. (b) Contour plots of I_{DS} as a function of V_{GS} and V_{DS} before annealing (top) and after annealing in ambient (bottom) at 200 °C for 1 h. (c) I_{DS} – V_{GS} curves on the semilogarithmic scale of a WSe₂ FET before annealing and after annealing in vacuum at 200 °C for 1 h. (d) Contour plots of I_{DS} as a function of V_{GS} and V_{DS} before annealing (top) and after annealing in vacuum (bottom) at 200 °C for 1 h.

Next, we measured the photoswitching characteristics of the WSe₂ FET before and after the thermal annealing in ambient. The laser was irradiated onto the WSe₂ FET and was turned off when the source-drain current appeared to become saturated. Note that the photoswitching experiments were performed at fixed $V_{GS} = 0$ V, $V_{DS} = 10$ V, the laser wavelength of 405 nm, and the laser intensity of 0.73 nW.

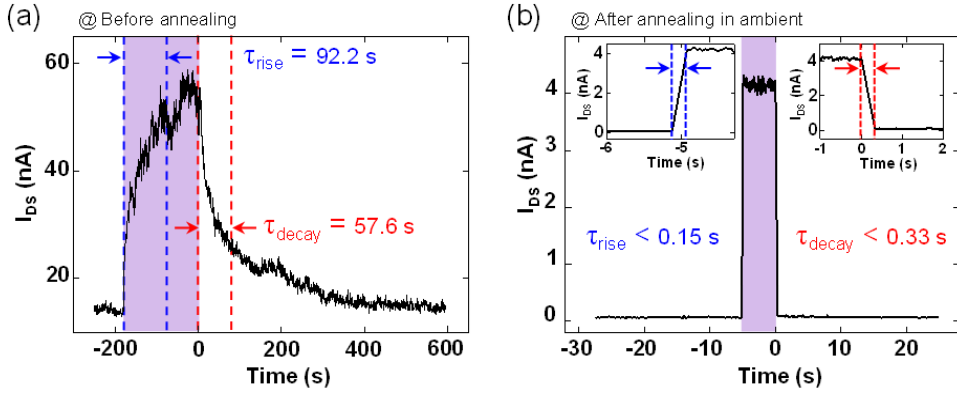


Figure 4.4. Photoswitching responses of the WSe₂ FET (a) before annealing and (b) after annealing in ambient at 200 °C for 1 h measured at $V_{GS} = 0$ V and $V_{DS} = 10$ V.

Figures 4.4(a) and 4.4(b) show the photoswitching characteristics before and after the annealing in ambient, respectively. In this study, the rise time constant (τ_{rise}) is defined as the time required for the photocurrent (difference between the currents measured in the dark and under irradiation, i.e. $I_{ph} = I_{irra} - I_{dark}$) to change from 10% to 90% of the maximum, and the decay time (τ_{decay}) is the time at which the photocurrent decreases to $1/e$ of its initial value. The purple regions in Figs. 3(a) and 3(b) indicate the time under the laser irradiation. We observed a dramatic change in the photoswitching response times of the WSe₂ FET after the thermal annealing. Both τ_{rise} and τ_{decay} decreased from 92.2 s and 57.6 s to less than 0.15 s and 0.33 s, respectively (corresponding to the decrease of more than 610 times and 170 times, respectively). Note that τ_{rise} and τ_{decay} after the annealing could not be measured precisely due to instrument limitations. To verify that the change in the photoswitching response times is due to the effect of the oxidation of the WSe₂ layers, we compared the photoswitching behavior of the WSe₂ FET before and after thermal annealing in vacuum ($\sim 4.5 \times 10^{-4}$ Torr) at 200 °C for 1 h. Contrary to the dramatic

decrease of the photoswitching response times for the FET annealed in ambient, a relatively small change was observed for the sample annealed in vacuum. This result signifies that the oxidation of the WSe_2 surface by annealing in ambient is crucial for the fast photoswitching response. The origins of the dramatically decreased photoswitching response times by annealing in ambient are discussed in detail below.

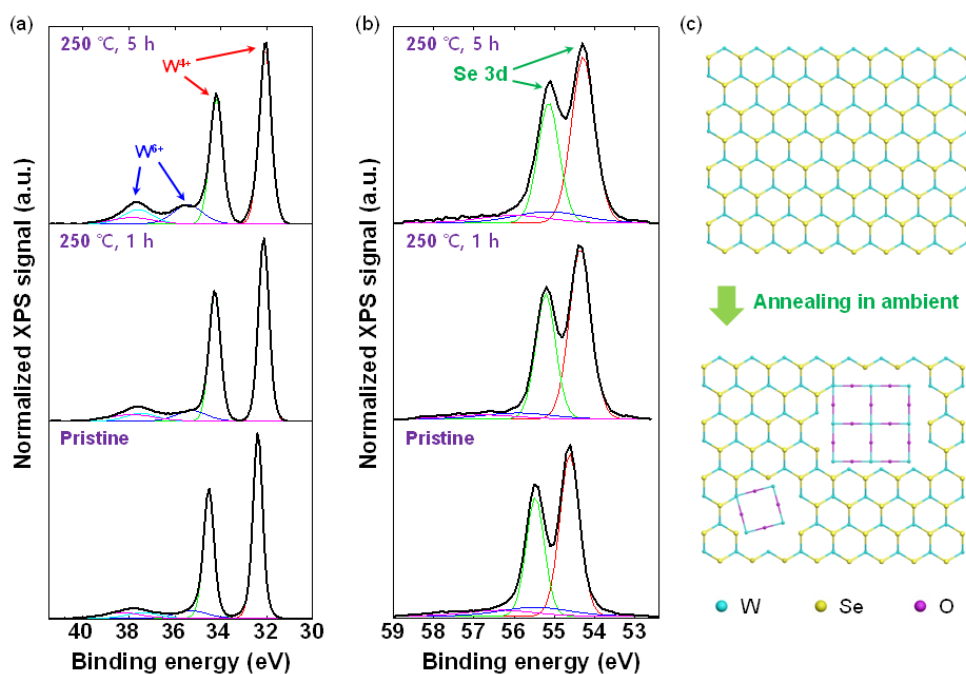


Figure 4.5. (a) W and (b) Se peaks in XPS spectra of WSe_2 flakes before annealing (labeled as pristine) and after annealing in ambient at 250 °C for 1 h and 5 h. (c) Schematics of the structural changes in the WSe_2 flake due to thermal annealing in ambient.

4.3.2. XPS analysis

XPS analyses were performed to investigate the changes in the elemental composition of the WSe₂ flakes by the thermal annealing in ambient, with the results being shown in Figs. 4(a) and 4(b). Although the annealing at 200 °C for 1 h was sufficient to alter both the electrical and photoswitching characteristics as shown in Figs. 2 and 3, these annealing temperature and time were not enough to observe the change in the elemental composition of the WSe₂. Thus, the WSe₂ flakes were annealed at 250 °C for 1 h and 5 h in ambient for XPS analyses as shown in Figs. 4(a) and 4(b). It should be noted that intensities of the two tungsten peaks (labeled as W⁶⁺ in Figure 4.5(a)) at the binding energies of 35.5 eV and 37.8 eV gradually increased with increased annealing time, whereas no changes were observed in the intensities of the selenium peaks. The tungsten peaks of W⁶⁺ generated by the thermal annealing indicate the formation of WO₃ due to the reaction of WSe₂ with oxygen in air during the annealing.^{17,27} On the other hand, the formation of selenium oxides, such as Se₂O₃, was not noticeable (Figure 4.5(b)). Schematics of the microscopic structure during the WSe₂ oxidation are shown in Figure 4.5(c) and were drawn based on the actual geometric structures of WSe₂ and cubic WO₃ (W-Se bond length of 2.53 Å, Se-Se bond length of 3.34 Å, and W-O bond length of 1.93 Å).^{17,28,29} Since WSe₂ has a hexagonal structure, while WO₃ has a cubic structure, the WSe₂-WO₃ structure is a quilted in-plane heterojunction, as shown in Figure 4.5(c).¹⁷ Therefore, the origin of the changed electrical properties after the annealing in ambient (Figs. 2(a) and 2(b)) can be explained by the formation of WO₃. The formed WO₃ can serve as an acceptor due to the difference between the work functions of WSe₂ (~4.4 eV) and WO₃ (~6.7 eV) that gives rise to the increased I_{DS} in the negative V_{GS} region ($V_{GS} < V_{n \leftrightarrow p}$) and the decreased I_{DS} in the positive V_{GS} region ($V_{GS} >$

$V_{n \leftrightarrow p}$).^{17,30,31} Similar to our results, there have been several reports that a WO_3 layer which is either deposited on or embedded in a WSe_2 sheet introduced p-doping into a WSe_2 FET.¹⁷⁻¹⁹ Furthermore, the transfer curves shifted toward the positive gate voltage direction due to the p-doping effect introduced by WO_3 , which is consistent with our obtained results shown in Figs. 2(a) and 2(b).

4.3.3. Photoluminescence analysis

To determine the changes in the band alignment after the formation of WO_3 , we performed PL spectroscopy experiments. Figures 4.6(a) and 4.6(b) show the optical microscopy image and PL mapping images, respectively, of a monolayer WSe_2 flake (labeled as Sample 1). Figures 4.6 and 4.6 display the change of the maximum PL intensity and optical bandgap of the WSe_2 flakes as the annealing time increased. In this instance, the WSe_2 flakes were annealed for 30 min and 60 min at 250 °C in ambient. Interestingly, the PL intensity of the WSe_2 flake decreased as the annealing time increased, as shown in Figs. 5(b) and 5(c). A similar phenomenon was observed in the MoS_2 treated by oxygen plasma.³² These results can be explained as follows. Since WO_3 has an indirect bandgap,³³ the band structure of the WSe_2 flakes may be partially changed to that with an indirect bandgap, decreasing the PL intensity.³² Additionally, the lattice mismatch between the WSe_2 and WO_3 structures provides traps and recombination sites in the bandgap of WSe_2 that can affect the electrical and optical characteristics of the WSe_2 . For instance, disorder, defects, and sulfur vacancies can produce shallow or deep trap sites in the MoS_2 layers, giving rise to the recombination process.^{34,35} Therefore, as the annealing time increased, the degree of disorder and the defects originating due to the lattice mismatch of the WSe_2 - WO_3

structure leads to non-radiative (Shockley-Read-Hall) recombination,³⁵ decreasing the PL intensity.

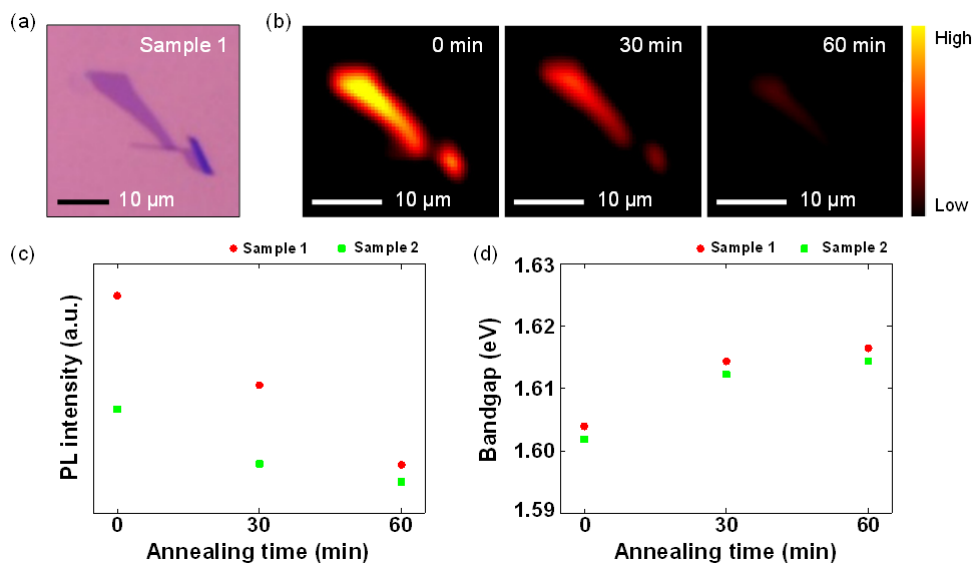


Figure 4.6. (a) Optical image of a monolayer WSe₂ flake (labeled as Sample 1). (b) PL mapping images of the Sample 1 before annealing (left) and after annealing in ambient at 250 °C for 30 min (middle) and 60 min (right). Change of (c) maximum PL intensity and (d) optical bandgap of the WSe₂ flakes due to the annealing.

The optical bandgaps of the WSe₂ flakes changed slightly as the annealing time increased, as shown in Figure 4.6(d). The optical bandgaps of the WSe₂ flakes were estimated from the peak point of the PL spectra. While the optical bandgap of the Sample 1 was measured as ~1.60 eV before the annealing corresponding to the bandgap of monolayer WSe₂,²⁴ the bandgap value changed to ~1.61 eV after the annealing for 60 min. Although the increase (~10 meV) of the optical bandgap is slight, this phenomenon can be explained by the formation of the WSe₂-WO₃ in-plane heterojunctions and the dielectric screening effect. Since WO₃ has a larger

bandgap of 2.75 eV compared to WSe₂ (1.60 eV for a monolayer),³³ the optical bandgap of the monolayer WSe₂ flakes increased through the annealing in ambient.³² Furthermore, the formation of WO₃ on WSe₂ can generate a stronger dielectric screening effect due to the larger dielectric constant of WO₃ (~90) compared to that of WSe₂ (~22).^{36,37} Consequently, the stronger dielectric screening effect leads to the diminished exciton binding energy and slightly increased the optical bandgap during the thermal annealing.³⁸ The distinct change of the Raman peaks was not observed after the annealing, which suggests that only a little of WSe₂ were transformed into WO₃ during the annealing. This observation is in accordance with very slight change (increase by ~10 meV) of the bandgap of WSe₂ films after annealing in ambient (Figure 4.6(d)).

The long-lasing photoconductivity in the WSe₂ FET observed in Figure 4.4(a) originates from the trapped photogenerated minority carriers with long life time (the type of minority carrier in ambipolar WSe₂ FETs can be decided by the applied V_{GS} which determines the location of Fermi level). The trapped photogenerated minority carriers can produce the additional gate electric field, and also demand the additional charge injection for charge neutrality even after turning off the light irradiation, which is so-called photogating effect.^{34,39-41} This charge injection model was verified by the additional photoswitching experiments at various V_{GS} in which the amount of trapped minority carriers was controlled by the applied V_{GS} . The charge injection model can help to explain the improved photoswitching characteristics of WSe₂ FETs after thermal annealing in ambient, for detailed explanation of the charge injection model). Regarding τ_{decay} , there are two factors which can reduce long-lasting photoconductivity by WO₃ formation. First, the p-doping by annealing in ambient locates Fermi level towards the valence band, which

induces weak photogating effect. Thus, less carriers are injected to satisfy charge neutrality after turning off the irradiation, thereby leading to the fast photoswitching. Second, WO_3 layers on a WSe_2 channel can act as non-radiative recombination sites, which was verified by the reduced PL intensity (Figure 4.6). The recombination processes can be promoted, resulting in fast τ_{decay} . In terms of τ_{rise} , since less carriers are injected after the annealing, time to reach the steady state during the irradiation through the scattering processes of photogenerated carriers with free carriers can be shortened. On the other hands, non-radiative recombination sites induced by WO_3 layers decrease the life time of photogenerated carriers. This could prolong the time necessary to reach the steady state after turning on the irradiation, thereby leading to longer τ_{rise} . According to the result of shortened τ_{rise} (Figure 4.4), we think that the first factor (p-doping) was more dominant than the second one (induced non-radiative recombination sites).

Conclusion

In conclusion, we fabricated WSe_2 FETs and studied the electrical properties and photoswitching responses before and after thermal annealing in ambient. We observed that the WSe_2 FETs were doped in the p-type manner and that the photoswitching responses became considerably faster after the ambient thermal annealing. The XPS and PL studies demonstrated that the WO_3 layer formed on the WSe_2 surface can play the roles of a p-doping layer and non-radiative recombination sites. Besides, through the analysis of V_{GS} -dependent photoswitching characteristics, we proposed that the photoswitching characteristics of the WSe_2 FETs can be improved by the annealing in ambient and those phenomena were explained by the

continuous charge injection model. This study may provide an insight into the mechanism of the photoswitching behaviors in the WSe₂ FETs for the realization of improved WSe₂-based optoelectronic applications.

Figure captions

Figure 4.1. Schematics of fabricating WSe₂ FET.

Figure 4.2. (a) Optical images of a WSe₂ flake (left) and fabricated WSe₂ FET (right). (b) An AFM image of the WSe₂ flake. The thickness of the WSe₂ flake (along the blue line) was found to be ~1.2 nm. (c) Raman spectra of a WSe₂ flake. (d) Schematic of the fabricated WSe₂ FET with Ti contacts. (e) I_{DS} - V_{GS} curves of the WSe₂ FET.

Figure 4.3. (a) I_{DS} - V_{GS} curves on the semilogarithmic scale of a WSe₂ FET before annealing and after annealing in ambient at 200 °C for 1 h. (b) Contour plots of I_{DS} as a function of V_{GS} and V_{DS} before annealing (top) and after annealing in ambient (bottom) at 200 °C for 1 h. (c) I_{DS} - V_{GS} curves on the semilogarithmic scale of a WSe₂ FET before annealing and after annealing in vacuum at 200 °C for 1 h. (d) Contour plots of I_{DS} as a function of V_{GS} and V_{DS} before annealing (top) and after annealing in vacuum (bottom) at 200 °C for 1 h.

Figure 4.4. Photoswitching responses of the WSe₂ FET (a) before annealing and (b) after annealing in ambient at 200 °C for 1 h measured at $V_{GS} = 0$ V and $V_{DS} = 10$ V.

Figure 4.5. (a) W and (b) Se peaks in XPS spectra of WSe₂ flakes before annealing (labeled as pristine) and after annealing in ambient at 250 °C for 1 h and 5 h. (c) Schematics of the structural changes in the WSe₂ flake due to thermal annealing in ambient.

Figure 4.6. (a) Optical image of a monolayer WSe₂ flake (labeled as Sample 1). (b) PL mapping images of the Sample 1 before annealing (left) and after annealing in

ambient at 250 °C for 30 min (middle) and 60 min (right). Change of (c) maximum PL intensity and (d) optical bandgap of the WSe₂ flakes due to the annealing.

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Chapter 5. Thickness-dependent avalanche breakdown phenomena in MoS₂ field effect transistors under high electric fields

In this Chapter, the electrical characteristics of MoS₂ FETs under the high electric fields. As 2D transition metal dichalcogenides electronic devices are scaled down to the sub- μm regime, the active layers of these materials are exposed to high lateral electric fields, resulting in electrical breakdown. In this regard, understanding the intrinsic nature in layer-stacked 2D semiconducting materials under high lateral electric fields is necessary for the reliable applications of their field-effect transistors. Here, we explore the electrical breakdown phenomena originating from avalanche multiplication in MoS₂ field-effect transistors with different layer thicknesses and channel lengths. Modulating the band structure and bandgap energy in MoS₂ allows the avalanche multiplication to be controlled by adjusting the number of stacking layers. This phenomenon could be observed in transition metal dichalcogenides semiconducting systems due to its quantum confinement effect on the band structure. The relationship between the critical electric field for avalanche breakdown and bandgap energy is well fitted to a power law curve in both monolayer and multilayer MoS₂.

5.1. Introduction

Ultrathin 2D nanosheets of TMDs have attracted much attention as post-silicon semiconducting materials because of their outstanding mechanical flexibility, transparency, high surface to volume ratio, and the absence of dangling bonds.¹⁻³ Among the TMDs, layered MoS₂ has been intensively researched due to its excellent electrical characteristics and thickness-dependent band structure (changing from indirect energy bandgap of 1.2 eV to direct bandgap of 1.8 eV as the number of layer decreases).⁴⁻⁷ MoS₂ offers promising opportunities to realize emerging electronics, such as ultra-thin transparent FETs,^{8,9} logic circuits,^{10,11} and sensor applications.¹²⁻¹⁵ For a use of MoS₂ in spatial integrated electronic design and applications, the channel length of FETs should be scaled down to sub- μm regimes. Consequently, it could be exposed to high lateral electric fields (E -fields), which can result in electrical breakdown. In addition, an electrical breakdown is affected by the electronic band structure and bandgap energy of semiconductors. Accordingly, the electrical breakdown in MoS₂ FETs will be determined by the thickness of MoS₂ channel layer due to its quantum confinement, which allows the tunable band structure and bandgap energy. Therefore, a more thorough understanding of the origin of electrical breakdown in MoS₂ semiconducting systems under high E -fields is highly desirable. To date, however, very little has been reported on the electrical characterization of MoS₂ under high E -fields because the atomically thin MoS₂ channel layer shows a limited thermal energy dissipation capability, which leads to thermal breakdown.^{16,17} Also, high thermal resistance of its insulating interface materials such as SiO₂ and polymer dielectrics accelerates this phenomenon.¹⁸ From these reasons, most

electrical measurements in MoS₂ FETs have been performed in the linear regime with low source-drain bias to prevent thermal breakdown by Joule heating.

Here, we studied the electrical breakdown in MoS₂ FETs with different bandgap energies using MoS₂ channels of different thicknesses. The observed electrical breakdown of MoS₂ FETs in high E -fields is attributed mainly to impact ionization in MoS₂ channel, which is called avalanche multiplication. The critical electric field (E_{CR}) and impact ionization rate (α), which are defined as the minimum E -field needed for avalanche multiplication and the number of electron-hole pairs generated per unit distance traveled by a hot carrier, respectively, were carefully investigated in MoS₂ with different thicknesses. In particular, a strong dependence of E_{CR} and α on the thickness of MoS₂ layer was closely related to its quantum confinement effect observed in 2D systems. Also, we performed thermal simulation with COMSOL Multiphysics to investigate the thermal effect by Joule heating and heat dissipation on the electrical breakdown. Although it is well known that the transport mechanism of MoS₂ is charge-hopping transport,¹⁹ both monolayer and multilayer MoS₂ FETs in this work have E_{CR} -bandgap relationships similar to those of three-dimensional semiconductor FETs.

5.2. Experiments

5.2.1. Device fabrication process

Figure 5.1 illustrates the MoS₂ FETs fabrication processes. To prepare MoS₂ channel layers, MoS₂ flakes were transferred from a bulk MoS₂ crystal on a 270 nm-thick SiO₂/Si substrate using a micromechanical exfoliation method. Onto the transferred MoS₂ channels, we spin-coated the double electron resistor layers with

methyl methacrylate (MMA) (9% concentration in ethyl lactate) and polymethyl methacrylate (PMMA) 950K (5% concentration in anisole) at 4000 rpm, sequentially. Each layer was baked at 180 °C for 90 s on a hot plate. After the source and drain electrodes patterns were defined using electron beam lithography (JSM-6510, JEOL), Ti (5 nm) and Au (30 nm) were deposited using an electron beam evaporator (KVE-2004L, Korea Vacuum Tech.) sequentially for the source and drain electrodes formation. The fabricated MoS₂ FETs were annealed at 200 °C in Ar atmosphere for 2 h to achieve better electrical performances by eliminating residues on the surface of the MoS₂ channels.

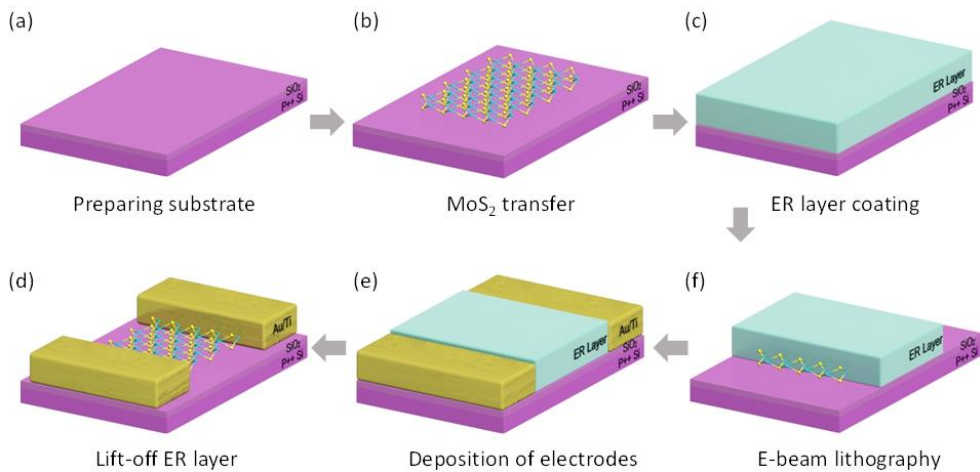


Figure 5.1. Schematics of the process flow for the MoS₂ FET fabrication.

5.2.2. Electrical and optical characterizations

The electrical properties of the MoS₂ FETs were measured using a semiconductor parameter analyzer (Keithley 4200-SCS) under various temperatures. Raman spectra, PL spectra, and PL mapping of MoS₂ were characterized using an XperRam 200 (Nanobase, Inc.) instrument with a 532 nm laser as the excitation source. The laser

poser was 11.3 μW , with a diffraction-limited laser spot size ($\sim 1 \mu\text{m}$ spot radius).

5.3. Results and discussions

5.3.1. Structure and electrical characteristics of MoS₂ FETs

Figure 5.2a shows the optical images (upper panels) and atomic force microscopy (AFM) images (lower panels) of a mechanically exfoliated monolayer MoS₂ flake and a fabricated MoS₂ FET. A schematic of the MoS₂ FET is shown in Figure 5.2b. Here, the back-gated MoS₂ FETs were fabricated on 270-nm-thick SiO₂ grown on a heavily doped Si substrate. The MoS₂ layer thickness ($\sim 0.8 \text{ nm}$) measured by AFM, together with photoluminescence (PL) spectra (Figure 5.2c), PL mapping exhibiting uniform bandgap energy at 1.82 eV (Figure 5.2d), and Raman frequency difference (20 cm^{-1}) data (Figure 5.2e), indicate that the prepared MoS₂ channel layer was a uniform monolayer.^{20,21} In Figure 5.2c, the positions of peaks A ($\sim 1.82 \text{ eV}$) and B ($\sim 2.0 \text{ eV}$) correspond to the direct band-to-band transitions with the energy split from the valence band by spin-orbital coupling.²¹ In addition, with an increasing number of MoS₂ layers, the PL intensity of the peaks decreased, and the peak positions redshifted, which was caused by the transition of the band structure from direct bandgap to indirect bandgap.²²

Figures 5.2f and 5.2g show the transfer curve (*i.e.*, drain-source current *versus* gate voltage, $I_{DS}-V_{GS}$) and the output curve (*i.e.*, drain-source current *versus* drain voltage, $I_{DS}-V_{DS}$) of the monolayer MoS₂ FET measured in vacuum ($\sim 10^{-4}$ Torr) at

room temperature. Typical *n*-type semiconductor behaviors with the on/off current

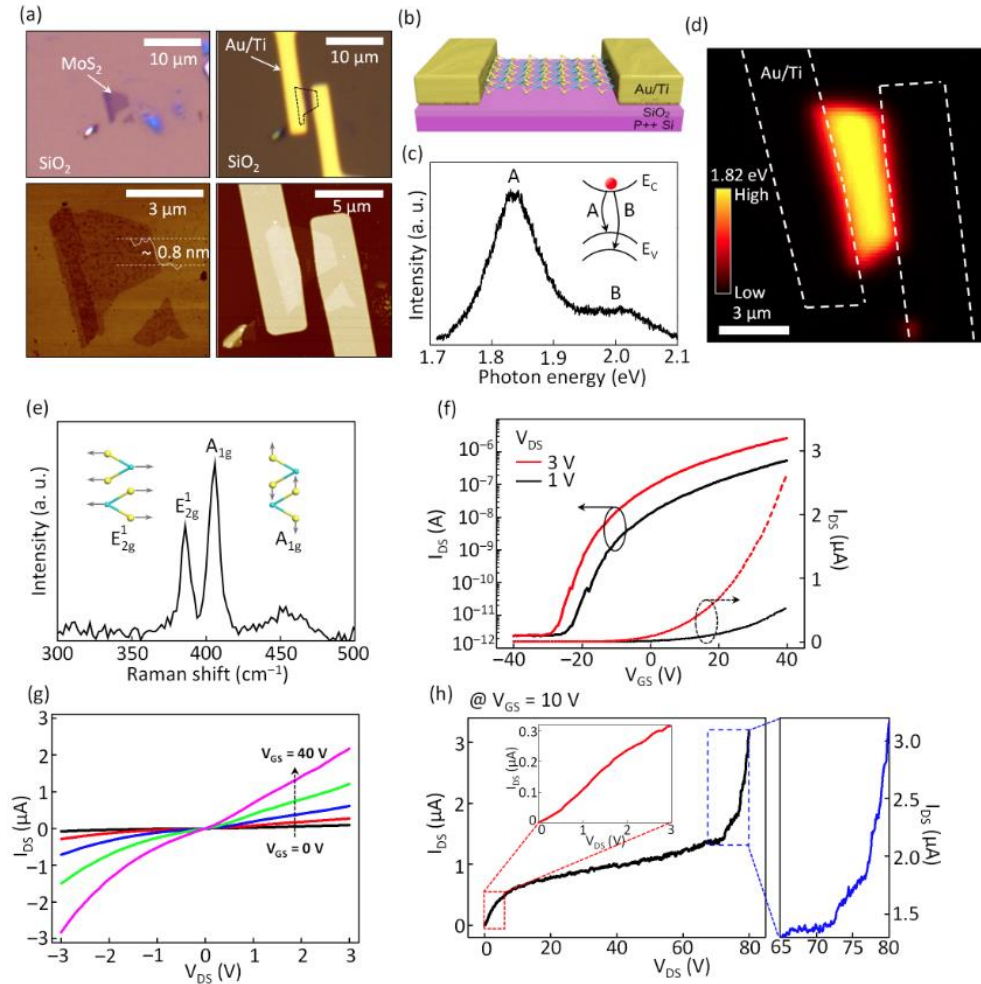


Figure 5.2. (a) Optical images (upper panels) and an AFM image (lower panel) of a monolayer MoS₂ flake and fabricated MoS₂ FET. (b) The schematic of the fabricated MoS₂ FET with Au/Ti contacts. (c) PL spectra, (d) PL mapping image, and (e) Raman spectra of a mechanically exfoliated MoS₂ channel layer. (f) Representative transfer and (g) output curve of a monolayer MoS₂ FET. (h) The output curve exhibiting electrical breakdown in high V_{DS} regime over 70 V. The I_{DS} increased linearly in low E -field regime (plotted with red line), whereas it increased abruptly in the high E -field regime (plotted with blue line).

ratio over 10^7 were observed. The mobility (μ) of this representative device was

determined to be $1.54 \text{ cm}^2/\text{V}\cdot\text{s}$, as calculated using the formula, $\mu = \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right) \frac{L}{W C_i V_{DS}}$,

with a channel length $L = 1.6 \mu\text{m}$, channel width $W = 4.7 \mu\text{m}$, and unit capacitance $C_i = 13 \text{ nF/cm}^2$. From the I_{DS} - V_{GS} characteristics shown in Figure 5.2f, the transconductance ($G_m = dI_{DS}/dV_{GS}$) can be derived with different V_{DS} . As shown in Figure 5.2h, we clearly observed an abrupt increase of the channel current (measured at $V_{GS} = 10 \text{ V}$) in the high V_{DS} regime ($V_{DS} > 70 \text{ V}$), resulting in electrical breakdown. Note that this electrical breakdown was also observed in MoS₂ FETs with ohmic-contacts, and most of V_{DS} drop occurred across the MoS₂ channel layer, not at the contact region due to the much higher channel resistance than the contact resistance. These results indicate that electrical breakdown was dominantly from the MoS₂ channel layer under high E -fields, not from the contact properties such as Schottky barriers. Also note that the electrical measurements were stopped before permanent device failures occurred by Joule heating, so reversible breakdown. In general, there are three possible mechanisms for electrical breakdown in FETs: breakdown by drain induced barrier lowering (*DIBL*), thermal runaway, and avalanche multiplication.²³ For these, it has been reported that a negligibly small *DIBL* ($\sim 10 \text{ mV/V}$) was observed in 2D semiconducting systems due to their excellent electrostatics, even for MoS₂ FETs with an extremely short channel length of 75 nm .²⁴ To explore the origin of the electrical breakdown in MoS₂ FETs, thorough investigations on MoS₂ FETs with different channel lengths, carrier concentrations, bandgap energies, and in particular on the thermal effect by Joule heating are necessary.

5.3.2. Effects of lateral electric field, thermal stress caused by Joule heating, and carrier concentration on electrical breakdown in MoS₂ FETs

To investigate the effect of lateral E -fields on the electrical breakdown, we fabricated MoS₂ FETs with various channel lengths ($\sim 1.49, 1.95, 3.42,$ and $4.97 \mu\text{m}$) using a common trilayer MoS₂ flake (thickness of $\sim 2.4 \text{ nm}$) (see Figure 5.3a). Note that the MoS₂ FETs had the uniform channel width of $2.2 \mu\text{m}$. The electrical

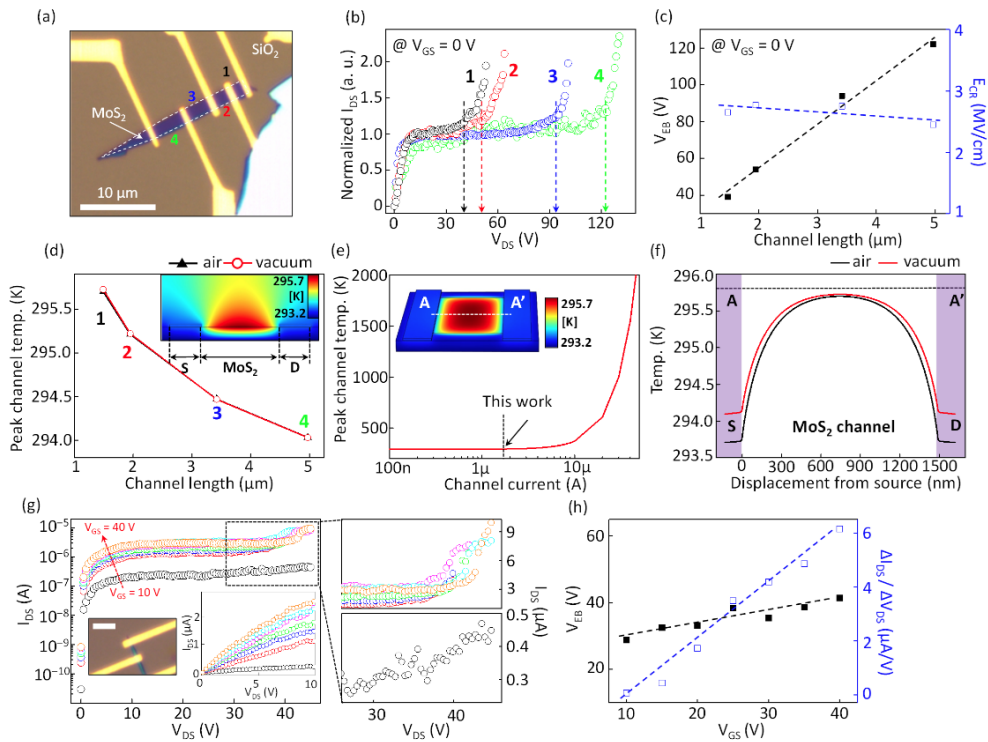


Figure 5.3. (a) An optical image of multilayer MoS₂ FETs (MoS₂ thickness of $\sim 2.4 \text{ nm}$) with different channel lengths of $1.49, 1.95, 3.42,$ and $4.97 \mu\text{m}$ (labeled from 1 to 4, respectively) made on a common trilayer MoS₂ flake (thickness of $\sim 2.4 \text{ nm}$). (b) The normalized I_{DS} – V_{DS} characteristics for the MoS₂ FETs measured at fixed $V_{GS} = 0 \text{ V}$. Color dashed lines indicate the breakdown voltages depending on the lateral E -fields. (c) The V_{EB} and E_{CR} values *versus* the channel length of MoS₂ FETs,

represented as black and blue symbols, respectively. (d) Peak channel temperatures corresponding to the MoS₂ FETs indicated in (a). An inset image shows a 2D thermal simulation result of the MoS₂ FET with a channel length of 1.49 μm. (e) Calculated peak MoS₂ channel temperature *versus* channel current in our device structure. An inset image indicates 3D thermal simulation result of the MoS₂ FET with a channel length of 1.49 μm. (f) Heat distribution of the MoS₂ channel along the dashed line in (e). (g) The I_{DS} - V_{DS} characteristics at various gate voltages ranging from 10 V to 40 V with a step of 5 V. An optical image of the multilayer MoS₂ FET is included in inset (scale bar = 3 μm). (h) The V_{EB} and $\Delta I_{DS}/\Delta V_{DS}$ values *versus* the gate voltage, represented as black and blue symbols, respectively.

characteristics were measured in air. It should be noted that the adsorbed air molecules on MoS₂ damp down the vibration of the out of plane phonons, which leads to reduced energy loss by electron-phonon scattering. Examination of the normalized I_{DS} - V_{DS} characteristics shows that the initial voltages of electrical breakdown (V_{EB}), with an abrupt increase of the channel current, shifted to the positive V_{DS} direction as the channel length increased (see Figure 5.3b). Importantly, the values of V_{EB} , which are indicated with dashed lines, showed a linear relationship to the channel length (black symbols and dashed fitting line in Figure 5.3c). Then, the critical electric field (E_{CR}), which allows free electrons to have sufficient kinetic energy for creating electron-hole pairs (blue symbols and dashed fitting line in Figure 5.3c) of the MoS₂ FETs, was determined to be 2.66 MV/cm, on average, with a standard deviation of 0.15 MV/cm.

To investigate the thermal effect by Joule heating on the electrical breakdown, the temperature increase and heat dissipation were analyzed with COMSOL Multiphysics. Interestingly, the calculated peak temperatures caused by Joule heating of all the MoS₂ FETs in Figure 5.3a were too low to affect the device operation (peak

temperatures *versus* the channel length are shown in Figure 5.3d). Note that due to the lower channel current in the long-channel device, the peak temperature on MoS₂ decreased as the channel length increased. This negligible temperature increase by Joule heating in the MoS₂ channel is attributed to the low channel current as shown in Figure 5.3e (a current range of $\sim\mu\text{A}$ when the electrical breakdown occurred). The previous research paper including the thermal simulation results by finite element modeling (FEM) reported that the temperature of the MoS₂ channel increased up to approximately its melting temperature at the channel current of a few milliamperes.¹⁵ In our simulation model, it is consistent that the channel temperature also significantly increases over 1000 K if the channel current increases over 1 mA (see Figure 5.4), but as aforementioned, μA -range currents cannot generate lots of heat that affects the electrical breakdown. Therefore, these results support that the electrical breakdown phenomena of MoS₂ FETs in high E -fields are primarily attributed to avalanche multiplication, not thermal effects by Joule heating. Furthermore, the reversible I_{DS} - V_{DS} behaviors including the electrical breakdown under the multiple V_{DS} sweeps at fixed V_{GS} also support that the MoS₂ channel was not damaged after the reversible electrical breakdown by thermal stress originated by Joule heating. Figure 2f shows the heat distribution in the MoS₂ FET (device 1 in Figure 5.3a) with the channel current of 1.8 μA at fixed gate bias ($V_{GS} = 0\text{ V}$). Due to the much higher thermal conductivity of the Ti/Au electrodes, the generated heat dissipated drastically near the contact regions, which indicates short-channel MoS₂ FETs have an advantage to relieve thermal stress *via* highly conductive contacts although there is a trade-off with heat-generation by the channel current. This result also indicates that the heat generated by Joule heating also increased the peak temperature of contact region, but it could not be efficiently dissipated in vacuum,

resulting the higher peak temperature at the contact regions in vacuum compared to that calculated in air. Therefore, the temperature difference between the contact region and the channel region was relatively smaller in vacuum compared to the case in air. Also, the dominant place of heat generation was located at the MoS₂ channel, not on the contact region, because the channel resistance was much higher than the contact resistance at fixed $V_{GS} = 0$ V.

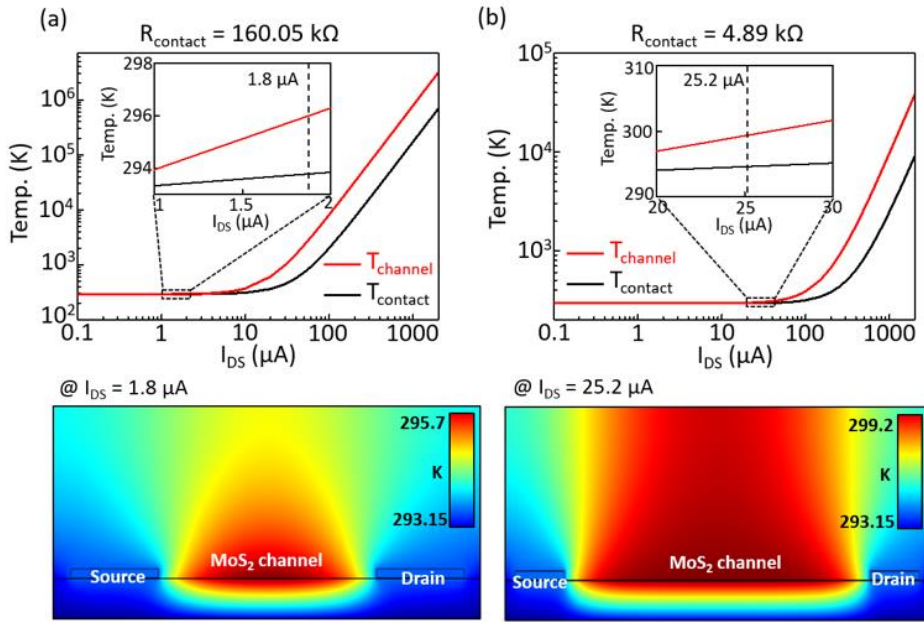


Figure 5.4. Calculated peak temperature at the MoS₂ channel and contact region *versus* the channel current at fixed $R_{contact}$, and 2D simulation result in the two different devices.

For further investigation, the effect of carrier concentration (which is modulated by gate electric field) on the abrupt increase of the channel current was investigated by adjusting the gate voltage. Figure 5.3g shows the I_{DS} - V_{DS} characteristics of a multilayer MoS₂ FET with a channel thickness of ~ 12 nm measured at various gate voltages ranging from 10 V to 40 V, plotted on a semi-logarithmic scale. We

observed that V_{EB} , the starting point of the electrical breakdown, shifted in the positive drain-source voltage direction from 28.8 V to 41.5 V as the gate voltage was increased (black symbols and dashed fitting line in Figure 5.3h). The origin of the higher V_{EB} is attributed to the increased electron-electron scattering with increasing accumulated carrier concentration in the MoS₂ channel. Therefore, a higher E -field is needed to observe electrical breakdown for compensating the energy loss by the electron-electron scattering. The increase of the gate bias also affects the number of generated electron-hole pairs such that the increase of the channel current per unit drain-source voltage change ($\Delta I_{DS}/\Delta V_{DS}$) increases drastically, from 0.07 $\mu\text{A}/\text{V}$ to 6.14 $\mu\text{A}/\text{V}$, when increasing the gate bias from 10 V to 40 V (blue symbols and dashed fitting line in Figure 5.3h). In other words, the electrical breakdown in the bias range over V_{EB} is accelerated proportionately with the number of free carriers. These results indicate that avalanche multiplication is the primary origin of the observed electrical breakdown of MoS₂ FETs in high E -fields. Note that if thermal runaway is the main mechanism for breakdown, then a larger current would produce an earlier breakdown phenomenon due to the Joule heating effect associated with a higher current, which is inconsistent with our observations (see Figure 5.3g).

5.3.3. Unique thickness dependency of MoS₂ on avalanche multiplication

The mechanism of avalanche multiplication is explained with the energy band diagram presented in Figure 5.5a. To generate an electron-hole pair, free carriers should be accelerated with sufficient kinetic energy that can take out an electron from its bound state (in the valence band) to a state in the conduction band. Additionally, the generated electron-hole pair can be accelerated in high E -fields, and the pair can generate other electron-hole pairs. This process is called the

avalanche multiplication or impact ionization process.²⁵ In this manner, a higher E_{CR} is needed to observe the avalanche multiplication for semiconductors with wider bandgaps. Therefore, we can expect that E_{CR} can be dependent on the number of MoS₂ layers (*i.e.*, MoS₂ film thickness) because MoS₂ has a layer-thickness-dependent bandgap energy. Note that in the avalanche multiplication in *n*-type semiconductors such as MoS₂, electron-hole pairs are generated mostly by

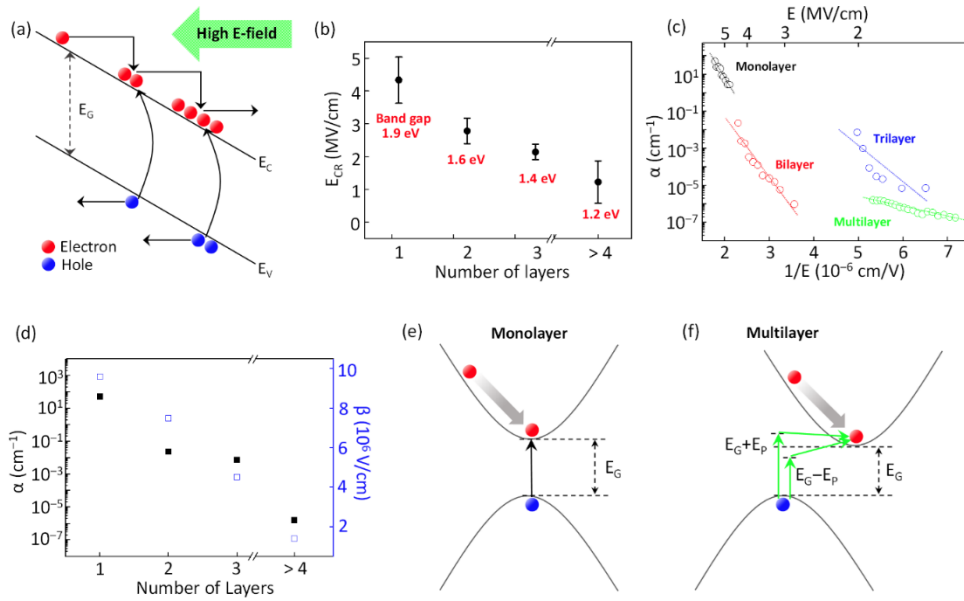


Figure 5.5. (a) The mechanism of avalanche multiplication phenomena. (b) The E_{CR} values *versus* the number of MoS₂ layers. The error bars indicate the standard deviations of E_{CR} extracted from 3-7 different MoS₂ FET devices for each condition. (c) The α values as a function of inverse E-field for the MoS₂ FETs with different numbers of MoS₂ layers. (d) The maximum α and calculated β values *versus* the number of layers of the MoS₂ channel, represented by black and blue symbols, respectively. The energy band structures for avalanche multiplication process in (e) monolayer and (f) multilayer MoS₂ FETs.

accelerated electrons because of the larger impact ionization rate by an electron (α_e) than by a hole (α_h).²⁶

Figure 5.5b summarizes the E_{CR} values for MoS₂ FETs with different MoS₂ layer thicknesses. For monolayer, bilayer, trilayer, and multilayer MoS₂ FETs, the E_{CR} was statistically determined as 4.33 MV/cm, 2.78 MV/cm, 2.14 MV/cm, and 1.22 MV/cm, respectively. These E -field ranges are comparable with those in the previously reported studies on electrical characteristics of short-channel MoS₂ FETs. Note that the thickness of multilayer MoS₂ flakes ranged from 2.4 nm to 50.4 nm, corresponding to the variation from 4 layers to 72 layers. The E_{CR} decreased as the thickness of MoS₂ increased because the bandgap energy of MoS₂ increased with decreasing MoS₂ thickness, as shown in Figure 5.5b.

We investigated the impact ionization rate (α) expressed by the following equation:

$$\alpha = \frac{1}{n} \left(\frac{dn}{dx} \right) = \frac{1}{v_d} \left(\frac{1}{K} \right) \left(\frac{dK}{dt} \right) \quad , \quad (1)$$

where n , v_d , and K are the electron concentration, electron drift velocity, and surface current density, respectively. The α values for MoS₂ FETs with monolayer, bilayer, trilayer, and multilayer MoS₂ channels were extracted by observing the relationship between the channel current and time. Figure 5.5c shows the plot of α versus $1/E$ (E is electric field) for different layer thickness MoS₂ FETs. The results were fitted with a Shockley form, $\alpha = \alpha_0 \exp(-\beta/E)$, where α_0 and β denote the constant extracted by an extrapolation method and the ionization parameter depending on the local E -field, respectively.^{27,28} Specifically, as the thickness of MoS₂ increased from monolayer to multilayers, the maximum α values decreased drastically from 52.5 cm⁻¹ to 1.6 × 10⁻⁶ cm⁻¹, and the calculated β values decreased from 9.6 × 10⁶ V/cm to 1.4 × 10⁶ V/cm, as summarized in Figure 5.5d. The strong thickness-dependence of the α and β values in MoS₂ FETs can be explained through

the energy band diagrams showing its the energy band structure transition (indicated in Figures 5.5e and 5.5f). As shown in Figures 5.5e and 5.5f, the electron-hole pair can be created by a collision with a hot electron. The energy conservation equation for the avalanche multiplication in monolayer MoS₂ with a direct bandgap energy can be written as²⁹

$$\frac{1}{2}m_i^*v_i^2 = E_G + \frac{1}{2}m_{e1}^*v_{e1}^2 + \frac{1}{2}m_{e2}^*v_{e2}^2 + \frac{1}{2}m_h^*v_h^2 \quad . \quad (2)$$

Here, E_G is the bandgap energy and $m_{i,e1,e2,h}^*$ are the effective masses of the incident electron before the collision (i), incident electron after the collision ($e1$), the created electron ($e2$), and the created hole (h), respectively. Similarly, $v_{i,e1,e2,h}$ are the velocities of the incident electron before the collision (i), incident electron after the collision ($e1$), the created electron ($e2$), and the created hole (h), respectively. Equation (2) means that only kinetic energy above the bandgap energy is sufficient for creating an electron-hole pair *via* impact ionization.

In contrast, as the number of MoS₂ layers increases, the conduction band minimum and valence band maximum become more separated in k-space (see Figure 5.5f). The energy conservation equation for avalanche multiplication in multilayer MoS₂ with an indirect bandgap energy is expressed as

$$\frac{1}{2}m_i^*v_i^2 = E_G \pm E_P + \frac{1}{2}m_{e1}^*v_{e1}^2 + \frac{1}{2}m_{e2}^*v_{e2}^2 + \frac{1}{2}m_h^*v_h^2 \quad . \quad (3)$$

Here, $\pm E_P$ denotes absorption and emission energies, respectively, of phonons with the wave vector equal to the wave vector difference between the created electron and hole (momentum conservation). Therefore, for multilayer MoS₂ FETs, the additional help of phonons is needed to create an electron-hole pair to fulfill both energy and momentum conservation, reducing the possibility of electron-hole pair creation. For this reason, the monolayer MoS₂ FETs showed higher α and β values

than did multilayer MoS₂ FETs. These results indicate that avalanche multiplication in MoS₂ FETs is extremely sensitive to the number of MoS₂ layers corresponding to the thickness of the channel. Therefore, it is possible to easily optimize α and β values by adjusting the number of MoS₂ layers in MoS₂ applications exploiting avalanche multiplication.

5.3.4. Temperature dependence of avalanche multiplication in MoS₂ FETs

We also measured $I_{DS}-V_{DS}$ of a multilayer MoS₂ FET (~17-nm-thick) at a fixed V_{GS} of 0 V under temperatures ranging from 80 K to 300 K to investigate the effect of temperature on avalanche multiplication. As shown in Figure 5.6a, the normalized I_{DS} increased rapidly to its saturation current as the temperature increased in the low E -field regime because the thermal energy provided to the electron overcomes the Schottky barrier at the interface between the electrode and MoS₂ channel (see Low E -field region in Figure 5.6a). In the high E -field regime, the electrons had sufficient energy to flow over the Schottky barrier and start to interact with optical phonons. Therefore, the normalized I_{DS} decreased due to the energy loss caused by the scattering with optical phonons as temperature increases (see high E -field region in Figure 5.6a). The E_{CR} values at the start of avalanche multiplication were also sensitive to the temperature because a higher E -field was required to compensate for the energy loss by electron-phonon scattering as the temperature increased (Figures 5.6a and 5.6b). For the same reason, the α values were decreased significantly over one order of magnitude as the temperature increased from 80 K to 400 K in the entire E -field range (Figures 5.6c and 5.6d). These results strongly support the effect of temperature-dependent electron-phonon scattering on the electron-hole pairs

generation. Interestingly, the β values of multilayer MoS₂ were insensitive to temperature (opened blue symbols in Figure 5.6d). This behavior is attributed to two compensating effects: a higher temperature increases electron-phonon scattering (negative effect for impact ionization) and reduces the bandgap energy of MoS₂,³⁰ leading to increased electron concentration (positive effect for impact ionization).

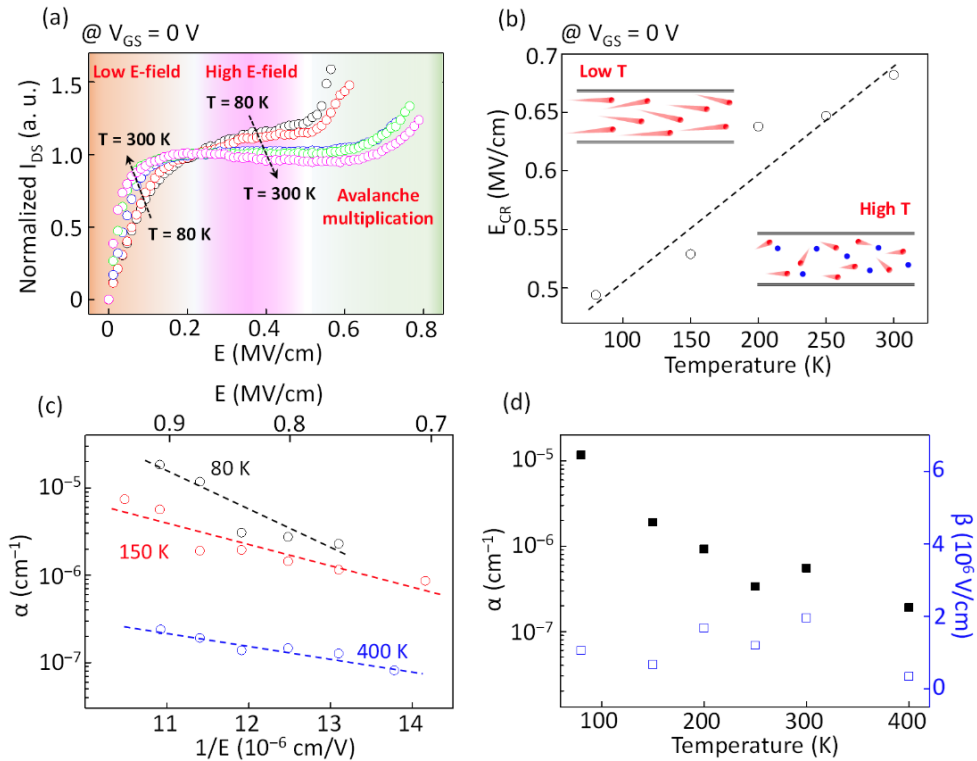


Figure 5.6. (a) The normalized I_{DS} as a function of E -field for various temperatures ranging from 80 K to 300 K measured at $V_{GS} = 0$ V. (b) The E_{CR} values depending on temperature extracted from the result of (a). (c) The α values under different E -fields at various temperatures. (d) The α and β values at different temperatures under a fixed E -field (0.88 MV/cm), represented by black and blue symbols, respectively.

5.3.5. Comparison of critical electric field with conventional semiconductor materials

Because the bandgap structure and bandgap energy of MoS₂ is sensitively thickness-dependent, the key parameters of avalanche multiplication including E_{CR} , α , and β could be adjusted by its number of layers. It is well-known that the E_{CR} is proportional to bandgap energy to the power of 2.5 ($E_{CR} \propto E_G^{2.5}$) for direct bandgap semiconductors, whereas the E_{CR} of indirect semiconductors is proportional to the square of bandgap energy ($E_{CR} \propto E_G^2$).^{31,32} Here, we compared the E_{CR} of MoS₂ FETs with the different number of layers to various conventional three-dimensional (3D) semiconductors. Figures 5.7a and 5.7b show that the E_{CR} values of monolayer MoS₂ with a direct bandgap energy and multilayer MoS₂ (from 2 layers to 72 layers) with an indirect bandgap energy were well fitted to the given power law dependences of $E_{CR} \propto E_G^{2.5}$ and $E_{CR} \propto E_G^2$, respectively. These results support that the avalanche multiplication phenomena observed in MoS₂ flakes are in good agreement with those of conventional 3D semiconductors and that their properties could be easily controlled by stacking the MoS₂ layers.

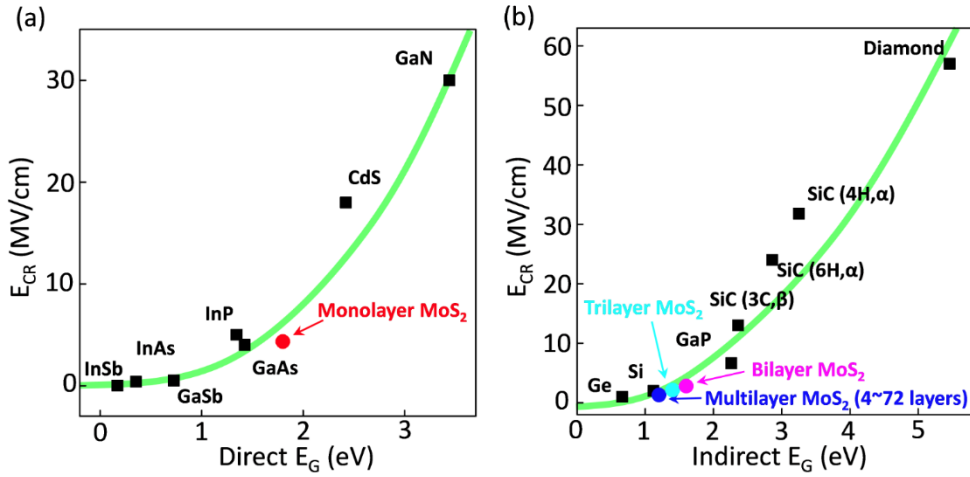


Figure 5.7. The E_{CR} values for monolayer, bilayer, trilayer, and multilayer MoS₂ as well as those of conventional semiconductors. The solid green lines indicate that the E_{CR} of monolayer, bilayer, trilayer, and multilayer MoS₂ FETs were well-fitted to the given power law dependence of (a) $E_{CR} \propto E_G^{2.5}$ (direct bandgap) and (b) $E_{CR} \propto E_G^2$ (indirect bandgap). The E_{CR} values of the semiconductors were obtained from references; InSb,³¹ InAs,³¹ GaSb,³¹ GaAs,³¹ GaN,³¹ Si,³¹ SiC,³¹ diamond,³¹ InP,³³ CdS,³⁴ Ge,³⁵ and GaP.³⁶

Conclusion

We investigated electrical breakdown phenomena in MoS₂ FETs under high E -fields. The effects of lateral E -fields and carrier concentration on the electrical breakdown indicated that avalanche multiplication is the origin of the electrical breakdown in MoS₂ FETs. The avalanche multiplication phenomena depended on the thickness of MoS₂ channel layer. In particular, the E_{CR} and α of avalanche multiplication in MoS₂ FETs decreased with an increasing number of MoS₂ layers due to the thickness-dependent tunable band structure and bandgap energy of the 2D MoS₂ layers. The effect of electron-phonon scattering and the power law fitting of the relationship between E_{CR} and bandgap energy showed that the avalanche

multiplication behaviors in MoS₂ were consistent with those in 3D semiconductors. Our study helps understand the electrical breakdown phenomena in MoS₂ under high E -fields. Furthermore, it will provide insight for the future achievement of controllable avalanche multiplication characteristics that are currently only feasible in thickness-dependent 2D layered MoS₂ and other transition metal dichalcogenides.

Figure captions

Figure 5.1. Schematics of the process flow for the MoS₂ FET fabrication.

Figure 5.2. (a) Optical images (upper panels) and an AFM image (lower panel) of a monolayer MoS₂ flake and fabricated MoS₂ FET. (b) The schematic of the fabricated MoS₂ FET with Au/Ti contacts. (c) PL spectra, (d) PL mapping image, and (e) Raman spectra of a mechanically exfoliated MoS₂ channel layer. (f) Representative transfer and (g) output curve of a monolayer MoS₂ FET. (h) The output curve exhibiting electrical breakdown in high V_{DS} regime over 70 V. The I_{DS} increased linearly in low E -field regime (plotted with red line), whereas it increased abruptly in the high E -field regime (plotted with blue line).

Figure 5.3. (a) An optical image of multilayer MoS₂ FETs (MoS₂ thickness of ~ 2.4 nm) with different channel lengths of 1.49, 1.95, 3.42, and 4.97 μm (labeled from 1 to 4, respectively) made on a common trilayer MoS₂ flake (thickness of ~ 2.4 nm). (b) The normalized I_{DS} - V_{DS} characteristics for the MoS₂ FETs measured at fixed $V_{GS} = 0$ V. Color dashed lines indicate the breakdown voltages depending on the lateral E -fields. (c) The V_{EB} and E_{CR} values *versus* the channel length of MoS₂ FETs, represented as black and blue symbols, respectively. (d) Peak channel temperatures corresponding to the MoS₂ FETs indicated in (a). An inset image shows a 2D thermal simulation result of the MoS₂ FET with a channel length of 1.49 μm . (e) Calculated peak MoS₂ channel temperature *versus* channel current in our device structure. An inset image indicates 3D thermal simulation result of the MoS₂ FET with a channel

length of 1.49 μm . (f) Heat distribution of the MoS₂ channel along the dashed line in (e). (g) The $I_{DS}-V_{DS}$ characteristics at various gate voltages ranging from 10 V to 40 V with a step of 5 V. An optical image of the multilayer MoS₂ FET is included in inset (scale bar = 3 μm). (h) The V_{EB} and $\Delta I_{DS}/\Delta V_{DS}$ values *versus* the gate voltage, represented as black and blue symbols, respectively.

Figure 5.4. Calculated peak temperature at the MoS₂ channel and contact region *versus* the channel current at fixed $R_{contact}$, and 2D simulation result in the two different devices.

Figure 5.5. (a) The mechanism of avalanche multiplication phenomena. (b) The E_{CR} values *versus* the number of MoS₂ layers. The error bars indicate the standard deviations of E_{CR} extracted from 3-7 different MoS₂ FET devices for each condition. (c) The α values as a function of inverse E-field for the MoS₂ FETs with different numbers of MoS₂ layers. (d) The maximum α and calculated β values *versus* the number of layers of the MoS₂ channel, represented by black and blue symbols, respectively. The energy band structures for avalanche multiplication process in (e) monolayer and (f) multilayer MoS₂ FETs.

Figure 5.6. (a) The normalized I_{DS} as a function of E -field for various temperatures ranging from 80 K to 300 K measured at $V_{GS} = 0$ V. (b) The E_{CR} values depending on temperature extracted from the result of (a). (c) The α values under different E -fields at various temperatures. (d) The α and β values at different temperatures under a fixed E -field (0.88 MV/cm), represented by black and blue symbols, respectively.

Figure 5.7. The E_{CR} values for monolayer, bilayer, trilayer, and multilayer MoS₂ as well as those of conventional semiconductors. The solid green lines indicate that the E_{CR} of monolayer, bilayer, trilayer, and multilayer MoS₂ FETs were well-fitted to the given power law dependence of (a) $E_{CR} \propto E_G^{2.5}$ (direct bandgap) and (b) $E_{CR} \propto E_G^2$ (indirect bandgap). The E_{CR} values of the semiconductors were obtained from references; InSb,³¹ InAs,³¹ GaSb,³¹ GaAs,³¹ GaN,³¹ Si,³¹ SiC,³¹ diamond,³¹ InP,³³ CdS,³⁴ Ge,³⁵ and GaP.³⁶

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Chapter 6. Trapped charge modulation at the MoS₂/SiO₂ interface by lateral electric field in MoS₂ field-effect transistors

Controlling trapped charges at the interface between a 2D material and SiO₂ is crucial for the stable electrical characteristics in FETs. Typically, gate-source bias has been used to modulate the charge trapping process with a narrow dielectric layer with a high gate electric field. Here, we observed that charge trapping can also be affected by the lateral drain-source voltage (V_{DS}) in the FET structure, as well as by the gate-source bias. Through multiple V_{DS} sweeps with increasing measurement V_{DS} range, we demonstrated that the charge trapping process could be modulated by the range of the applied lateral electric field. Moreover, we inserted hexagonal boron nitride (h-BN) layer between the MoS₂ and SiO₂ layer to explore the charge trapping behavior when a better interface is formed. This study provides a deeper understanding of controlling the electrical characteristics with interface-trapped carriers and lateral electrical fields in 2D materials-based transistors.

6.1. Introduction

Atomically thin 2D materials such as MoS₂, MoSe₂, WS₂, and WSe₂ have attracted tremendous attention as innovative nanoelectronic materials [1-4]. Among the 2D materials, MoS₂ is an excellent channel material for realizing 2D-based FETs due to its outstanding electrical characteristics [5, 6] and intrinsic band gap feature (~1.9 eV for monolayer and 1.2 eV for bulk MoS₂) [7, 8]. In addition to having these advantages, the MoS₂ FET shows good electrical stabilities from thermal [9, 10] and mechanical [11, 12] alterations, which are essential requirements for FETs. In spite of the innate stabilities of MoS₂, unstable electrical characteristics could be observed, caused by extrinsic sources. For example, trapped charges existing at the interface between MoS₂ and a gate dielectric layer (such as SiO₂) have been considered one of the dominant sources incurring electrically unsteady states [13, 14]. Occasionally, deliberate charge trapping at the interface between MoS₂ and SiO₂ or charge injection into SiO₂ has been used for materializing 2D materials-based memory devices [15, 16]. Typically, to control trapping or detrapping electrons, gate-source bias has been used with a thin gate dielectric layer where a high gate electric field can be built [15, 16]. In our study, we observed that the charge trapping process in MoS₂ FETs could also be controlled by the measurement range of lateral drain-source voltage (V_{DS}). Understanding of altering electrical characteristics by the V_{DS} sweep range is considerably important for the realization of the stable electrical performance as FETs.

In addition to having advantage, trapped charges can function as Coulomb scattering sites and provide an effective gate-source bias, which can lead to fluctuating conductance [13, 14]. Therefore, large hysteresis in MoS₂ FETs induced

by trapped charges can be an obstacle to practical applications in electronic devices. To avoid such obstacles, inserting a hexagonal boron nitride (h-BN) layer between MoS₂ and SiO₂ has been proposed to improve the interface condition due to its atomically flat surface without dangling bonds [17, 18]. Then, high carrier mobility was successfully achieved in 2D materials-based FETs with such an h-BN buffer layer [17, 18].

Here, charge trapping and detrapping processes at the interface between MoS₂ and SiO₂ layers in MoS₂ FETs were investigated through multiple V_{DS} sweeps with increasing measurement range of V_{DS} . We observed that electrons became trapped at the MoS₂/SiO₂ interface in the V_{DS} measurement range of up to 105 V, and then trapped electrons started to be withdrawn by a lateral electric field of ~ 67.3 kV/cm. Moreover, we fabricated a MoS₂ FET by inserting an h-BN buffer layer between the MoS₂ and SiO₂ layers and compared the electrical characteristics of this MoS₂ FETs with those of MoS₂ FETs without an h-BN layer. The carrier mobility of the MoS₂ FET with the h-BN layer showed a higher value (~ 52.7 cm²/V·s) than those of all MoS₂ FETs without the h-BN layer characterized in this work (ranging from 0.5 cm²/V·s to 46.0 cm²/V·s), and the hysteresis disappeared when a better interface was formed between the semiconductor and gate dielectric layer.

6.2. Experiments

6.2.1. Device fabrication process

Figure 6.1 illustrates the fabrication processes for MoS₂ field-effect transistors (FETs). MoS₂ films were transferred from a bulk MoS₂ crystal on a 270 nm-thick SiO₂/Si substrate by mechanical exfoliation method. To pattern the drain and source

electrodes by using electron beam lithography, the electron resistor layer (poly(methyl-methacrylate) (PMMA) 950 K 11% concentration in anisole) was spin-coated at 4000 rpm, and then it was annealed at 180 °C for 90 s on a hot plate. After drain and source patterns were made by an electron beam lithography system (JSM-6510, JEOL), Ti (5 nm) and Au (30 nm) were deposited using an electron beam evaporator (KVE-2004L, Korea Vacuum Tech.) sequentially.

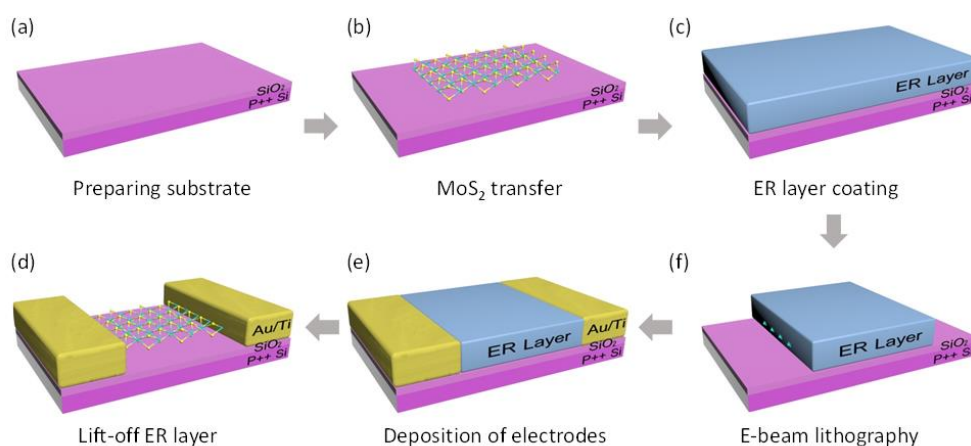


Figure 6.1. The schematics indicating the fabrication processes for MoS₂ FET.

6.2.2. Electrical characterizations

The electrical properties of the MoS₂ FETs were measured using a semiconductor parameter analyzer (Keithley 4200-SCS) under various temperatures. Raman spectra of MoS₂ were characterized using an XperRam 200 (Nanobase, Inc.) instrument with a 532 nm laser as the excitation source.

6.3. Results and discussions

6.3.1. Structure and electrical characteristics of MoS₂ FETs

Figure 6.2(a) shows a schematic of the multilayer MoS₂ FET device and the molecular structure of MoS₂. An optical image of a fabricated MoS₂ FET is shown in figure 6.2(b). The thickness of the mechanically exfoliated MoS₂ film (~3.8 nm) was measured by atomic force microscopy (AFM). The Raman peak positions of E_{2g}¹ and A_g¹ correspond to the in-plane and out-of-plane lattice vibrations, respectively, and the value of the frequency difference (~24 cm⁻¹) indicates an uncontaminated multilayer MoS₂ sheet (figure 6.2(c)) [19]. Figures 6.2(d) and 6.2(e) exhibit the transfer curve (drain-source current versus gate-source voltage, $I_{DS}-V_{GS}$) and the output curve (drain-source current versus drain-source voltage, $I_{DS}-V_{DS}$) of a multilayer MoS₂ FET measured in vacuum (~10⁻⁴ Torr) at room temperature. These data showed good *n*-type semiconductor behavior with a high on/off ratio of over 10⁹ and a carrier mobility of 29.3 cm²/V·s. Note that all the mobility values in this work signify the maximum values measured at V_{DS} in the linear region. The carrier mobility (μ) was calculated by the formula $\mu = (dI_{DS}/dV_{GS}) \times [L / (WC_iV_{DS})]$, where W (~25 μ m) is the channel width, L (~15.6 μ m) is the channel length, and $C_i = \epsilon_o\epsilon_r/d = 1.3 \times 10^{-4}$ F·m⁻² is the capacitance between the MoS₂ and heavily doped Si back gate per unit area. Here, ϵ_o is the vacuum permittivity, ϵ_r (~3.9) is the dielectric constant of the SiO₂ dielectric, and d is the thickness (270 nm) of the SiO₂ layer.

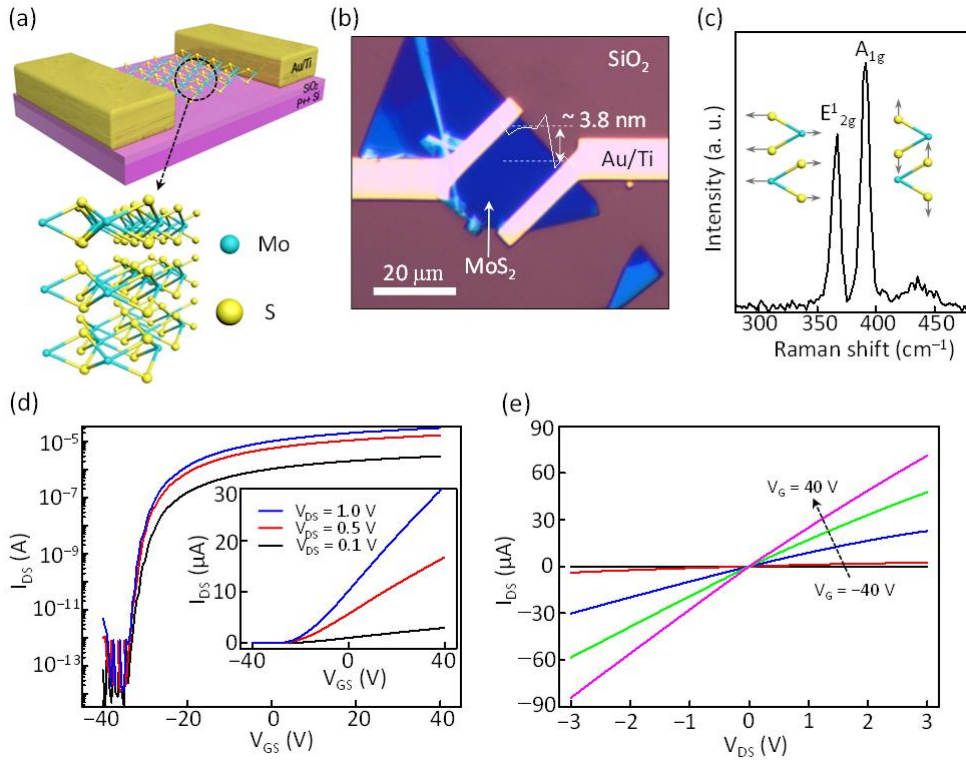


Figure 6.2. (a) Schematic of MoS₂ FET and the molecular structure of MoS₂. (b) An optical image of a MoS₂ FET and an AFM profile indicating the thickness of the MoS₂ film (~3.8 nm). (c) Raman spectrum of a multilayer MoS₂. (d) I_{DS} - V_{GS} and (e) I_{DS} - V_{DS} curves of the multilayer MoS₂ FET.

6.3.2. Charge trapping and detrapping phenomena depending on the V_{DS} measurement range

To investigate the trapped charge effect on electrical characteristics, we applied a finite gate-source voltage pulse (denoted as $V_{GS,before}$) of -40 V or 40 V for one second before the actual measurement and then examined the output curve at a zero gate-source voltage ($V_{GS} = 0$). Figure 6.3(a) indicates that two different electrical configurations were observed: one with a higher saturation current (represented by filled circular symbols) and another with a lower saturation current (represented by

open circular symbols), which are controlled by $V_{GS, before}$ (figure 6.3(a)). The origin of the two separate configurations can be explained by the effect of trapped electrons induced by $V_{GS, before}$. Because the MoS₂ channel and SiO₂ dielectric form an incomplete interface, trapped electrons could exist at the interface of MoS₂/SiO₂, which influences the channel current flow. This result is consistent with previous studies in which V_{GS} was used to control charge trapping by taking advantage of a narrow dielectric layer (a few hundred nanometers) with a high gate electric field [13, 14]. In order to classify two different configurations markedly, we applied the strong voltage of $V_{GS, before}$ (−40 V or 40 V). As shown in figure 6.3(b), when $V_{GS, before} = -40$ V was applied, the trapped electrons escaped from the trap sites at the interface to the MoS₂ channel. On the other hand, when $V_{GS, before} = 40$ V was applied, some free electrons were trapped at the trap sites at the interface. These two electrical configurations are denoted as unoccupied-traps state and occupied-traps state, respectively (figures 6.3(a) and 6.3(b)). The trapped electrons induced by $V_{GS, before}$ caused Coulomb scattering with the free carriers (conduction electrons) in the MoS₂ channel and acted as a negative gate-source bias during the measurement even at a fixed value of $V_{GS} = 0$ V, leading to reduced conductivity in the MoS₂ channel (figure 6.3(a)).

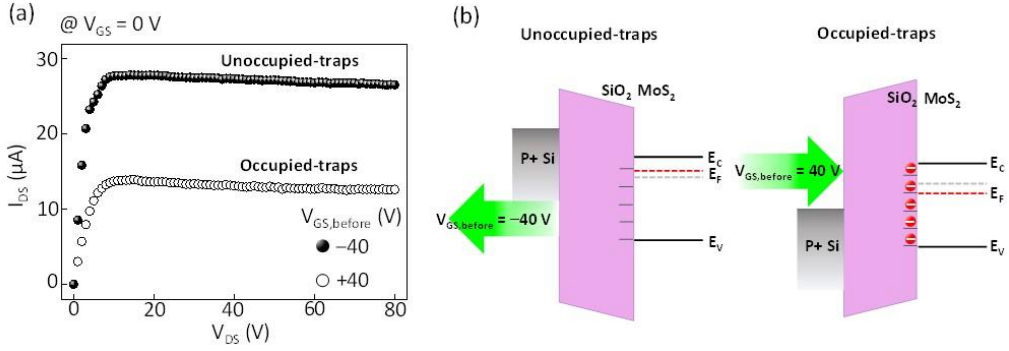


Figure 6.3. (a) I_{DS} - V_{DS} curves of the multilayer MoS₂ FET illustrating two different electrical configurations (occupied-traps state and unoccupied-traps state) measured at $V_{GS} = 0$ V controlled by initial gate-source voltage pulse ($V_{GS, before}$). (b) Schematic band diagrams illustrating the two different electrical configurations when $V_{GS, before} = -40$ V or 40 V is applied.

Similar to the above method using a gate-source voltage, trapped charges can also be controlled by a lateral electric field. Figure 3(a) shows the output curves of a multilayer MoS₂ (12 nm-thick) FET under a series of V_{DS} sweeps with an increasing measurement range from 40 V to 130 V at a fixed $V_{GS} = 0$ V. Each V_{DS} sweep with increasing measurement ranges was performed in sequence without interval time. We fixed $V_{GS} = 0$ V, so that the channel current does not flow too much in the MoS₂ channel, even at high V_{DS} range, which avoids a permanent breakdown phenomenon by the Joule heating effect. When the measurement range increased from 40V (from 0 V to 40 V, black filled circular symbols) to 105V (from 0 V to 105 V, violet filled circular symbols), the saturation current gradually decreased from ~ 130 nA to ~ 30 nA, as shown in figures 3(a) and (b). In contrast, the saturation current continuously increased in V_{DS} sweeps from the measurement range of above 110 V (from 0 V to 110 V, gray open circular symbols). The decreased saturation current during the V_{DS} sweeps up to the measurement range of 105 V is ascribed to the charge trapping process because the free electrons can be trapped in the trap sites at the MoS₂/SiO₂

interface, and so the trapped electrons negatively affect the saturation current on the next V_{DS} sweep measurement (represented by the trapping process shown in figure 3(b)). After the V_{DS} sweep of 105 V (violet filled circular symbols), the trapped electrons started to be detrapped out of the trap sites owing to the strong lateral drain source electric fields, which resulted in an increased saturation current in the next V_{DS} sweep measurement ranges from 110 V to 130V (represented by the detrapping process shown in figure 3(b)). To calculate the energy levels of trap sites, we utilized the simplified Poole–Frenkel model in which the trapped charge can begin to escape the potential barrier via thermionic-field emission at $V_{DS} = 105$ V. From the calculation, it was determined that the trapped electrons in trap sites would be located more than 72 meV away from the conduction band, which is in accordance with a previous study [20] (see figure S3 for details in the supplementary information). Note that the abrupt increase in the channel current above 110 V is due to the avalanche breakdown process under strong lateral electric fields [21].

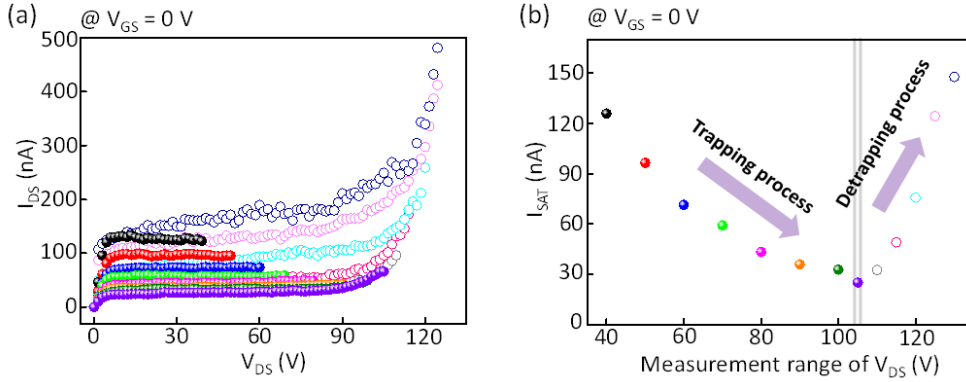


Figure 6.4. (a) I_{DS} – V_{DS} curves under multiple V_{DS} sweeps with increasing measurement V_{DS} range from 40 V (from 0 V to 40 V) to 130 V (from 0 V to 130 V) at $V_{GS} = 0$ V. (b) Saturation current as a function of the measurement V_{DS} range at $V_{GS} = 0$ V. Black, red, blue, green, magenta, orange, dark green, and violet filled circular symbols correspond the V_{DS} sweep range of 40, 50, 60, 70, 80, 90, 100, and 105 V, respectively, for trapping process. Gray, pink, cyan, light pink, and navy open circular symbols correspond the V_{DS} sweep range of 110, 115, 120, 125, and 130 V, respectively, for detrapping process.

6.3.3. Charge detrapping processes by the multiple V_{DS} sweeps

To clearly identify whether the origin of the change in saturation current in response to the different V_{DS} sweep ranges is due to trapped charges, we further investigated and compared the saturation currents obtained from the repeated measurements under the occupied-traps state or unoccupied-traps state. Before the actual measurement, the occupied-traps or unoccupied-traps states were formed by applying $V_{GS, before} = 40$ V or -40 V, respectively (figures 6.5(a) and 6.5(b)). In the occupied-traps state (after applying $V_{GS, before} = 40$ V), the saturation current gradually increased and became saturated during the multiple V_{DS} sweeps from 0 V to 105 V at a fixed value of $V_{GS} = 0$ V, as shown in figure 6.5(a). This phenomenon is attributed

to the detrapping process by the high lateral drain-source electric field (~ 67.3 kV/cm). Note that quite a high V_{DS} over 105 V was required for detrapping process due to the long channel length (~ 15.6 μm) of our FET, and the range of V_{DS} depends on the channel length of each device. The electrons escaped from the trap sites by the multiple V_{DS} sweeps, which gradually changed from the occupied-traps state to the unoccupied-traps state. On the other hand, in the unoccupied-traps state (after applying $V_{GS, before} = -40$ V), the saturation currents did not change during the multiple V_{DS} sweeps because of a lack of electrons in the trap sites at the interface, as shown in figure 6.5(b). Figure 6.5(c) summarizes the values of the saturation currents during multiple V_{DS} sweeps in the occupied-traps and unoccupied-traps states. The difference in saturation current after the six repeated measurements between the occupied-traps state (~ 38 nA) and unoccupied-traps state (~ 67 nA) signifies the influence of the trapped electrons remaining after repeated measurements.

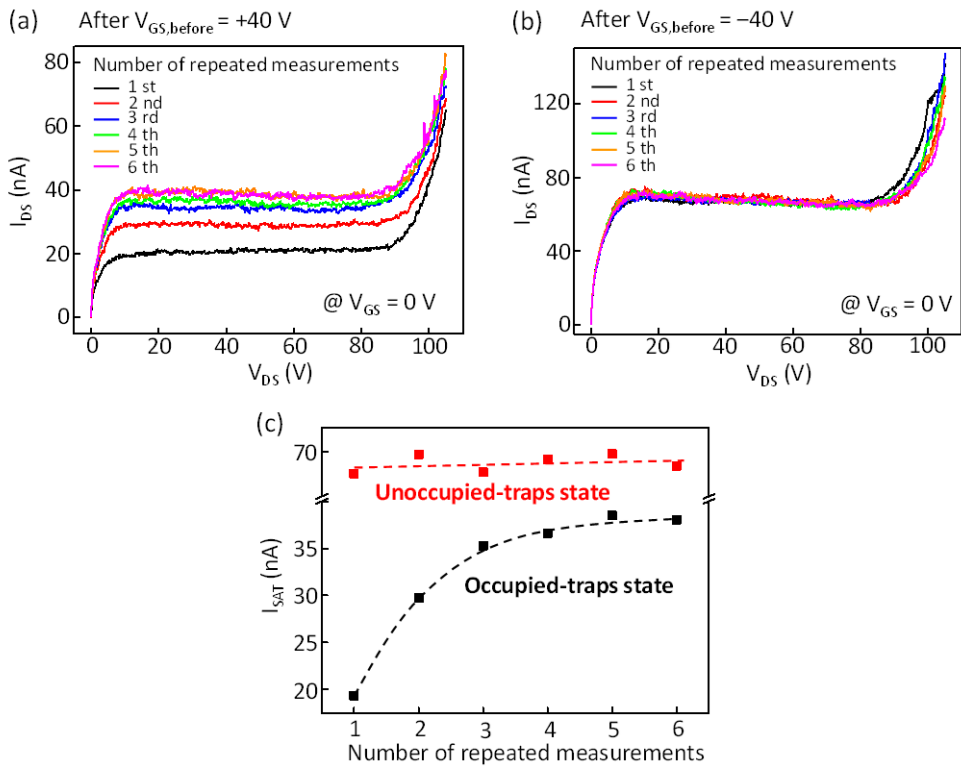


Figure 6.7. I_{DS} – V_{DS} curves of the MoS₂ FET under repeated V_{DS} sweeps at $V_{GS} = 0$ V after (a) $V_{GS, \text{before}} = 40$ V or (b) $V_{GS, \text{before}} = -40$. (c) Saturation current versus number of repeated measurements for the two different electrical configurations (occupied-traps state and unoccupied-traps state).

6.3.4. The influence of h-BN buffer layer inserted between MoS₂ channel and SiO₂ interfaces

As mentioned in the introduction, understanding of controlling trapped electrons is required for the stable electrical characteristics of MoS₂-based transistors or memory devices. In particular, a better interface between MoS₂ and the dielectric layer should be formed to avoid fluctuating conductance by trapped charges. In this manner, we inserted the h-BN layer between MoS₂ and SiO₂ to form an ideal interface without dangling bonds. Figures 6.6(a) and 6.6(b) show the schematics of the multilayer MoS₂ FETs without and with h-BN between the MoS₂ and SiO₂ layers. The thicknesses of the multilayer MoS₂ for the data of figures 6.6(a) and 6.6(b) were found to be ~12 nm and ~18 nm, respectively. We could not use the same MoS₂ thickness to compare the charge trapping behavior in figure 6.6. Note that the electrical characteristics can be dependent on the MoS₂ thickness [22, 23], but the influence of charge trapping by the difference of the MoS₂ thickness has been reported to be unclear and disputable [24-27]. So, a further study exploring charge trapping behavior with diverse MoS₂ thicknesses is needed to investigate the accurate thickness-dependency of charge trapping. The thickness of the h-BN layer for the data shown in figure 6.6(b) was ~19 nm. Figures 6.6(c) and 6.6(d) indicate the transfer curves of the MoS₂ FET without and with the h-BN layer measured in vacuum (~10⁻⁴ Torr) at room temperature. The mobility for the MoS₂ FET without the h-BN layer (figure 6.6(a)) and with the h-BN layer (figure 6.6(b)) was determined to be ~46.0 cm²/V·s and 52.7 cm²/V·s, respectively. Here, a dielectric constant of 3.5 was used for the h-BN layer for the estimation of mobility values [4]. Note that the mobility of the MoS₂ FET with the h-BN layer showed a higher value than those of all the MoS₂ FETs without the h-BN layer (ranging from 0.5 cm²/V·s to 46.0 cm²/V·s)

characterized in this work. More importantly, hysteresis was not observed in the MoS₂ FET with the h-BN layer in contrast with the MoS₂ FETs without the h-BN layer because the h-BN layer forms a nearly ideal interface without dangling bonds and trap sites, as shown in figure 6.6(d). Note that in the hysteresis comparison between the two devices, we did not apply the same V_{DS} (figures 6.6(c) and 6.6(d)), but the charge trapping process is dominantly affected by V_{GS} rather than V_{DS} in our device because the electric field by V_{GS} is much stronger than that by V_{DS} . Therefore, the electrical characteristics did not change in the MoS₂ FETs with the h-BN layer regardless of whether $V_{GS,before} = 40$ V or -40 V (figure 6.6(f)), whereas the electrical characteristics changed for $V_{GS,before} = 40$ V compared to that for $V_{GS,before} = -40$ V for the MoS₂ FETs without the h-BN layer (figure 6.6(e)). For these reasons, inserting the h-BN layer between SiO₂ and MoS₂ is desirable for realizing the stable electrical characteristics in MoS₂ FETs.

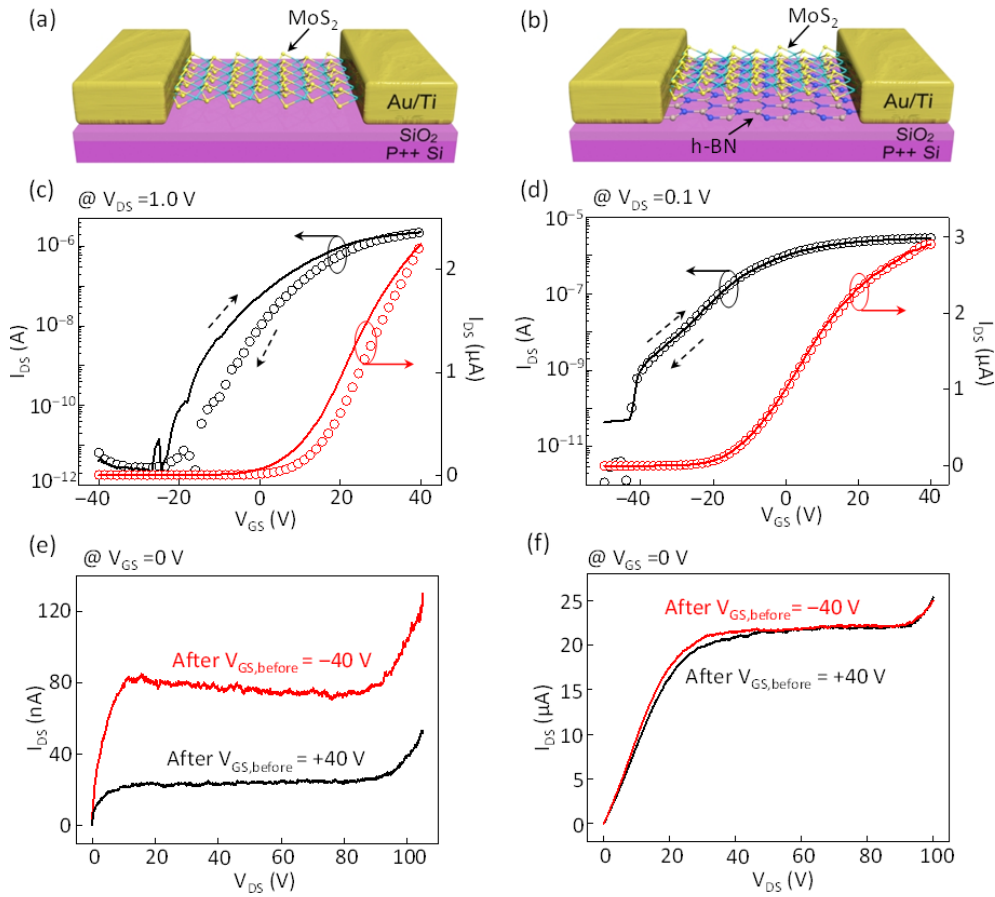


Figure 8.6. (a,b) Schematics and (c,d) I_{DS} - V_{GS} curves exhibiting the degree of hysteresis in MoS₂ FET (a,c) without and (b,d) with an h-BN layer. I_{DS} - V_{DS} curves at $V_{GS} = 0$ V after $V_{GS, before} = 40$ V (black lines) and $V_{GS, before} = -40$ (red lines) in MoS₂ FET (f) without and (e) with the h-BN layer.

Conclusion

In summary, we studied the influence of a lateral electric field on the charge trapping and detrapping dynamics at the interface between the MoS₂ and SiO₂ layers. From the results of multiple V_{DS} sweeps with increasing measurement ranges of V_{DS} , it was found that saturation current initially decreased in the low V_{DS} sweep range and then started to increase with a larger V_{DS} sweep range over 110 V. We

demonstrated that this phenomenon was due to the charge trapping and detrapping processes originating from the imperfect interface between the MoS₂ and SiO₂ dielectric. In addition, we inserted an h-BN buffer layer between MoS₂ and SiO₂ to investigate the charge trapping effect after forming a near-ideal interface. Consequently, the hysteresis caused by trapped charges at the interface disappeared, and the trapped charge effect on electrical characteristics by $V_{GS, before}$ was also eliminated. This study provides a better understanding of the effect of interface trapped carriers and controlling electrical characteristics by the lateral electrical field in 2D materials-based transistors.

Figure captions

Figure 6.1. The schematics indicating the fabrication processes for MoS₂ FET.

Figure 6.2. (a) Schematic of MoS₂ FET and the molecular structure of MoS₂. (b) An optical image of a MoS₂ FET and an AFM profile indicating the thickness of the MoS₂ film (~3.8 nm). (c) Raman spectrum of a multilayer MoS₂. (d) $I_{DS}-V_{GS}$ and (e) $I_{DS}-V_{DS}$ curves of the multilayer MoS₂ FET.

Figure 6.3. (a) $I_{DS}-V_{DS}$ curves of the multilayer MoS₂ FET illustrating two different electrical configurations (occupied-traps state and unoccupied-traps state) measured at $V_{GS} = 0$ V controlled by initial gate-source voltage pulse ($V_{GS, before}$). (b) Schematic band diagrams illustrating the two different electrical configurations when $V_{GS, before} = -40$ or 40 V is applied.

Figure 6.4. (a) $I_{DS}-V_{DS}$ curves under multiple V_{DS} sweeps with increasing measurement V_{DS} range from 40 V (from 0 V to 40 V) to 130 V (from 0 V to 130 V) at $V_{GS} = 0$ V. (b) Saturation current as a function of the measurement V_{DS} range at $V_{GS} = 0$ V. Black, red, blue, green, magenta, orange, dark green, and violet filled circular symbols correspond the V_{DS} sweep range of 40, 50, 60, 70, 80, 90, 100, and 105 V,

respectively, for trapping process. Gray, pink, cyan, light pink, and navy open circular symbols correspond the V_{DS} sweep range of 110, 115, 120, 125, and 130 V, respectively, for detrapping process.

Figure 6.5. I_{DS} - V_{DS} curves of the MoS₂ FET under repeated V_{DS} sweeps at $V_{GS} = 0$ V after (a) $V_{GS,before} = 40$ V or (b) $V_{GS,before} = -40$. (c) Saturation current versus number of repeated measurements for the two different electrical configurations (occupied-traps state and unoccupied-traps state).

Figure 6.6. (a,b) Schematics and (c,d) I_{DS} - V_{GS} curves exhibiting the degree of hysteresis in MoS₂ FET (a,c) without and (b,d) with an h-BN layer. I_{DS} - V_{DS} curves at $V_{GS} = 0$ V after $V_{GS,before} = 40$ V (black lines) and $V_{GS,before} = -40$ (red lines) in MoS₂ FET (f) without and (e) with the h-BN layer.

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Chapter 7. Summary

This thesis mainly focuses on the optoelectronic characteristics of MoS₂ phototransistors. As a first research topic, the researches on enhanced optoelectronic characteristics of MoS₂ phototransistors via the surface treatment with organic material (copper phthalocyanine (CuPc)) were conducted. Through this facile surface treatment by electron beam evaporator system, not only photoresponsivity and but also photoswitching characteristics can be improved. Furthermore, beyond the perspective of optoelectronic performances, the intrinsic optoelectronic characteristics of MoS₂ phototransistors were investigated, such as internal responsivity, internal quantum efficiency, and internal detectivity. Similar to MoS₂, the effects of *p*-doping on electrical and optoelectronic characteristics of WSe₂ phototransistors were discussed. Furthermore, the interesting phenomena of MoS₂ FETs under the high lateral electric fields, such as thickness-dependent avalanche breakdown and charge trapping dynamics at the interface of MoS₂/SiO₂ are introduced in Chapter 5 and 6, respectively. Indeed, I wished to investigate the optoelectronic characteristics of 2D materials-based phototransistors under high electric field as an ultimate research topic of my doctorate course, but I just could investigate the electrical properties under the high electric fields due to the insufficient time. However, I believe I partially established the foundation for exploring optoelectronic characteristics under high electric fields, and convinced there is going to be an interesting phenomenon at the end of this study.

국문초록

유기물 혹은 반데르발스 접합을 통한 이황화몰리브덴 포토트랜지스터의 광전기적 특성 연구

박진수

서울대학교 물리천문학부

본 학위 논문에서는 이황화 몰리브덴 포토트랜지스터의 광 전자적 특성에 대해 연구를 수행하였다. 박사 학위 과정에서 2차원 물질 기반의 포토 트랜지스터의 광 전자적 특성을 주로 탐구하였다. 2차원 물질은 원자스케일의 얇은 두께로 인해 많은 빛의 양을 흡수할 수 없고 상당히 큰 엑시톤 결합 에너지를 가지고 있다. 이 두 요인은 2차원 물질 기반의 광 검출기의 광 반응성을 억제시킨다. 그러나 포토 트랜지스터는 드레인 전압 및 게이트 전압을 이용해서 광 특성을 증폭시킬 수 있는 구조이기 때문에, 2차원 물질 기반의 포토 트랜지스터의 광 전자적 특성을 향상시킬 수 있다.

본 학위 논문의 2장에서는 이황화 몰리브덴 포토트랜지스터의 광 특성 향상시키는 연구를 소개한다. 이황화 몰리브덴 표면에 유기물질을 이용한 표면처리로 광 반응성과 광 스위칭 특성을 개선시킬 수 있었다. 광 전자적 특성 성능향상을 위한 연구뿐만 아니라, 이차원 물질의 본질적인 광 전자적 특성에 대해서 연구를 수행하였다. 본 학위 논문의 3장에서는 반데르발스 헤테로 구조를 이용하여 제작한 완전히 투명한 이황화 몰리브덴 포토트랜지스터의 본연의 광 전자적 특성을 설명하였다. 4장에서는 이황화 몰리브덴 뿐만 아니라, 홀 도핑이 텅스텐 디셀레나이드 기반의 포토트랜지스터의 광전자 특성에 미치는 영향에 대해서도 요약하였다.

광 전자적 성능을 증폭하기 위해서 외부 전기장을 이용하는 포토트랜지스터의 구조적 특성 때문에, 강한 전기장 내에서의 전기적 그리고 광 전자적 특성에 대해서 연구를 수행하였다. 이황화 몰리브덴 트랜지스터가 강한 전기장 내에서 어떤 전기적 특성이 나타나는지에 대해 연구를 수행했고 흥미로운 현상들을 발견했다. 5장과 6장에서는 강한 전기장 내에서 발생하는 애벌런치 항복 현상과 이차원 물질과 기판사이에서의 전자 트랩현상에 대해서 설명하였다.