Ph.D. Dissertation

Design of High-Speed Power-Efficient Optical Transmitter With Push-Pull Driving Technique

푸쉬-풀 구동 기술을 이용한 고속 저전력 광 송신기 설계

by

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August, 2019

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Design of High-Speed Power-Efficient Optical Transmitter With Push-Pull Driving Technique

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이 논문을 공학박사 학위논문으로 제출함

2019 년 5 월

서울대학교 대학원

전기·정보공학부

황 정 호

황정호의 공학박사 학위논문을 인준함

2019 년 5 월

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부위원장 _____ **(인)**

위 원 _____ **(인)**

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A Dissertation Submitted to the Department of
Electrical and Computer Engineering
in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy
at
SEOUL NATIONAL UNIVERSITY
May, 2019

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Abstract

Data usage dramatically increases by year due to Internet of Things (IoT) and 5G networks. Even though required data keeps going up, backbone network of wireline such as data center has to transmit and receive data without or less errors. However, electrical wireline interface is difficult to process data for the data surge due to skin effects and dielectric loss in the copper channel at high frequency. Therefore, the significance of high-speed and power-efficient optical links utilizing optical fibers keeps increasing owing to its low loss even delivering data for the long distance.

Following this trends, this thesis is focused on transmitter side of optical links. Push-pull driving technique, which is suitable for high-speed and power-efficient network, is proposed and utilized. Based on this technique, 32Gb/s NRZ driver with large output swing, which drives Mach-Zehnder modulator (MZM) or electro-absorption modulator (EAM), has been implemented with the power efficiency of 6.28pJ/b in 65nm CMOS process. It achieves an active area of 0.086mm^2. Also, 4-channel HDMI active optical cable (AOC) transmitter chips achieving 12Gb/s per channel is fabricated in 180nm CMOS process using push-pull driving scheme with the total area of 1.62mm^2.

In the subsequent section, optical transmitters with clocking architecture have been proposed. Vertical-cavity surface-emitting laser (VCSEL), which has low cost for fabrication and high ability for integration, are utilized for clocked optical transmitters. Both forwarded and embedded clocking architectures have been employed for the future optical interface between application-specific integrated

circuit (ASIC) and optical links. As a result, 56Gb/s VCSEL PAM-4 transmitter with forwarded clocking and 64Gb/s VCSEL PAM-4 transmitter with embedded clocking have been implemented in 65nm CMOS process. Figure of merits for power efficiency are 2.12pJ/b and 2.69pJ/b, respectively. Both chips occupy the area of 0.133mm^2 and 0.278mm^2, respectively.

Keywords: Push-pull driver, Mach-Zehnder modulator (MZM), Electro-absorption modulator (EAM), current-mode logic (CML) driver, vertical-cavity surface-emitting laser (VCSEL), NRZ, PAM-4, CMOS

Student Number: 2014-21636

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Chapter 1

Introduction

1.1. Motivation

Nowadays, large amounts of data will be required to handle with internet of things (IoT) and 5G network. Per-pin data rate is keep increasing since number of pins are limited in the recent data interface. High-speed standards such as 400G Ethernet (400GbE) reflects this trend. However, increasing per-pin data rate is difficult to achieve because the copper medium has severe skin effects at high frequency and channel with long length. To compensate the copper loss at high frequency, required power consumption dramatically increases at both transmitter and receiver side. For this reason, many systems have been designed with optical links owing to advantages in signal integrity and power consumption. Therefore, optical links have large potential for both short and long reach high-speed networks.

However, in spite of advantages of optical system, high-speed optical network

has been facing with some difficulties. First, optical transceivers should drive bandwidth-limited devices unlike conventional electrical transceivers with terminated load. It may cause even more power consumption than electrical transceivers. Second, optical components such as modulators and VCSELs have some nonlinear characteristics. Due to those points, transmitters should be designed to compensate mentioned drawbacks mentioned above.

In this thesis, designs of high-speed and power-efficient optical transmitter are described. To achieve good power efficiency at high data rate, push-pull current-mode driving technique is compared with other types of drivers and applied to different kinds of optical transmitters such as modulators and VCSELs. With various implementations of optical transmitter, it will give the design directions for future ultra-high-speed optical transmitters. Moreover, clocking architectures for ultra-high-speed optical transmitter are analyzed. Detailed circuits with the chosen clocking architecture are discussed in the subsequent Chapter.

1.2. Thesis Organization

This thesis is organized as follows. In Chapter 2, background of optical link is described. Overall system and basis of optical links in data center are discussed. Design issues regarding bandwidth and power consumption are brought up in the followings. Also, basic optical components in the transmit side of data center such as modulators and VCSEL are dealt in the chapter.

In Chapter 3, high-speed optical drivers are explained. For power-efficient driving, push-pull technique in current-mode logic (CML) is proposed. With this scheme, 32Gb/s NRZ MZM/EAM driver and 4-channel HDMI AOC NRZ drivers are designed in power-efficient way.

In Chapter 4, high-speed clocked optical transmitter is implemented. Unlike Chapter 3, it utilizes VCSEL, which can be used in low cost and highly integrated. It analyzes clocked optical transmitter for quarter-rate system. Also, power-efficient and high-speed core blocks, such as quadrature error correctors, 4:1 MUXs, and VCSEL driver are proposed. Furthermore, it drives VCSELs in both NRZ and PAM-4 data format.

Chapter 5 summarizes the proposed implementations and concludes this thesis.

Chapter 2

Background of Optical Link

2.1. Overview

Photonic technologies have been widely used in various applications such as advanced manufacturing, cloud, networking, and 3D sensing as shown in Fig. 2.1 [2.1]. Especially among those applications, cloud and networking requires large amounts of data transmission for long distances. Therefore, optical links have been employed owing to its advantages as discussed in Chapter 1. Many applications among Internet of Things (IoT), edge computing, and 5G wireless applications will require large amounts of data in the near future. Data centers are key buildings for various applications using optical communications. That is the reason why many data centers have been built with optical links as shown in Fig. 2.2 [2.2] .

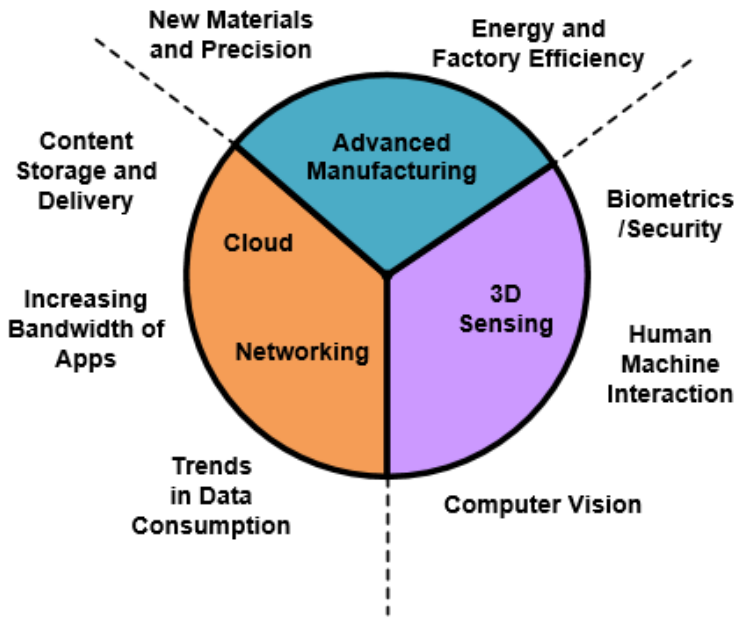


Fig. 2.1. Applications of optical communications.

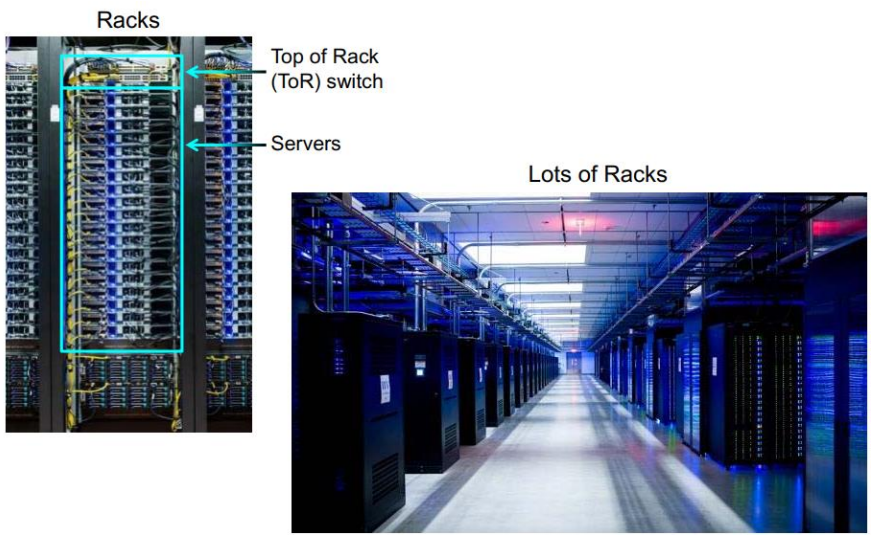


Fig. 2.2. Hardware of optical links in data centers in [2.2].

Furthermore, high-performance computing (HPC) systems which has high power density compared to conventional data centers also have been built with optical

Fig. 2.3. Examples of optical links in high-performance computing in [2.2].

links as shown in Fig. 2.3 [2.2].

However, data centers and HPC consume lots of power due to large amount of data transmission and increased per-pin data rate. To reduce power consumption in data centers, basis of data center and design challenges are discussed in further sections. Furthermore, optical components used in transmitter side of data center, for example, modulators and VCSELs are also discussed at the end of the Chapter.

2.2. Basic Principles of Optical Transmission

To transmit/receive data with optical format mentioned at the earlier section, fibers take the same role as copper wires in electrical communications. There are two types of fiber, single-mode fiber and multi-mode fiber, which can be used for different purposes. Single-mode fibers commonly have 9-μm core diameters in 125-μm claddings as shown in Fig. 2.4 [2.3]. Small dimension enables only one mode propagation through the fiber without modal dispersion. Due to this advantage, single-mode propagation enables to transmit data for the long-reach (long-haul) network such as outside of data centers. However, single-mode fibers have difficulties in packaging due to small dimensions for aligning fibers. On the other hand, multi-mode fibers have larger dimensions than single-mode fibers. Multi-mode fibers have 50-μm/62.5-μm core diameters with 125-μm claddings as shown in Fig. 2.4 [2.3]. Since multi-mode fibers have larger core dimensions, it has strong advantages for fiber alignment and requires less packaging costs. However, since multi-mode fibers propagate several modes of wave, they have modal

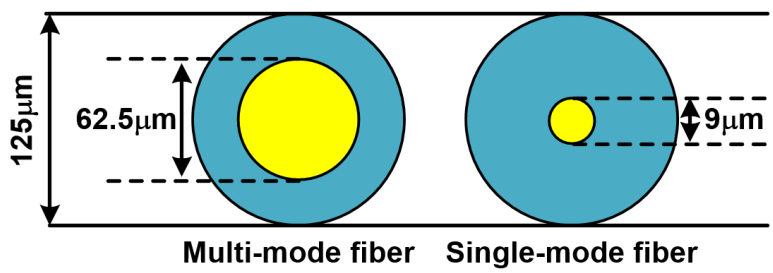


Fig. 2.4. Cross section view of multi-mode fiber and single-mode fiber.

dispersions and it limits the distance of data communication. Therefore, multi-mode fibers are commonly used in short-reach (short-haul) network such as inside of data centers.

When fiber types are decided by applications and distances, wavelengths of light are one of the other major issues. To decide which spectrum to use, absorption and scattering attenuations of band should be considered. As can be seen in Fig. 2.5,

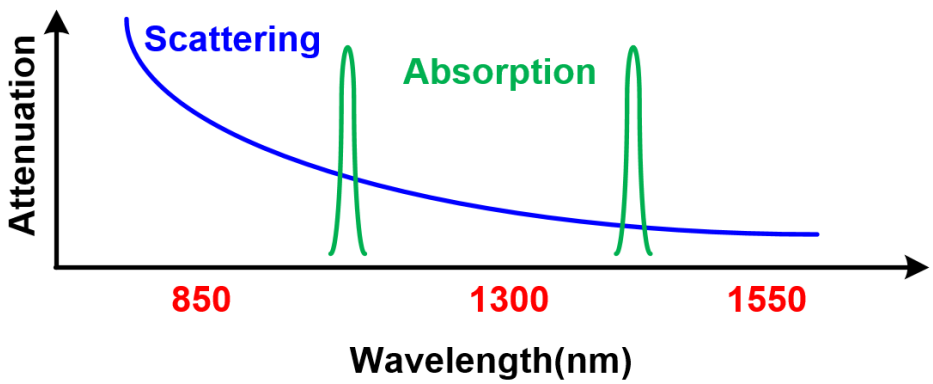


Fig. 2.5. Scattering and absorption loss by wavelength.

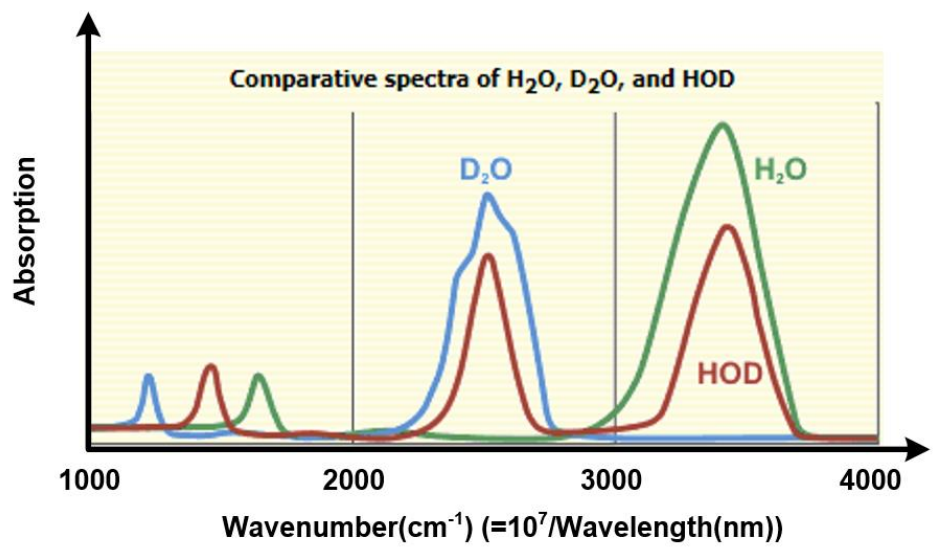


Fig. 2.6. Absorption loss of infrared light as shown in [2.5].

light having longer wavelengths have less scattering loss [2.4]. Moreover, it has absorption bands including infrared lights due to water and glass in fiber which light becomes absorbed as described in Fig. 2.6 [2.5]. Also, it is known that infrared light has large background noise even though it has small attenuation loss. As a result, wavelengths of 850nm, 1310nm, and 1550nm are commonly used in optical communications. Luckily, optical components used in optical communication can be fabricated in this range of wavelength. More specific details will be discussed in Section 2.5.

However, the method of chip fabrication and packaging limit the selection of wavelength. Electronic integrated circuit (EIC) and photonic integrated circuit (PIC) can be fabricated in a single integrated chip or several chips. The former one is called as monolithic integration and the latter one is called as hybrid integration.

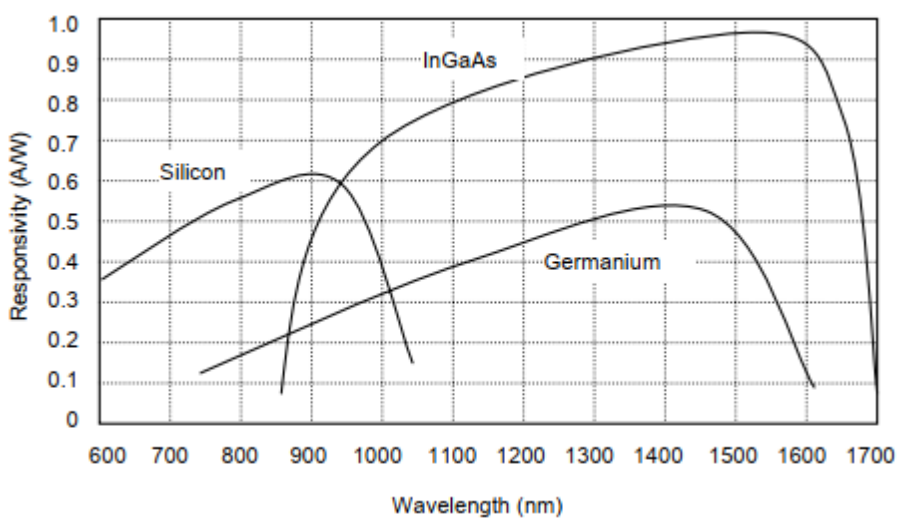


Fig. 2.7. Typical responsivity curves for silicon and others in [2.6].

When the chip is designed in monolithic integration, it is fabricated in a single fabrication process. Silicon photonics is the case when the single CMOS technology is applied. However, the light is only absorbed below the wavelength of 1180nm as shown in Fig. 2.6 [2.6]. As a result, transmitting light in silicon waveguide is possible for 1310nm and 1550nm. Since the range of absorbing light and transmitting light are incompatible, there needs extra material such as germanium (Ge) which lowers bandgap energy for photodetector as illustrated in Fig. 2.7 [2.7]. As it deals with longer wavelength, which has lower attenuation loss for transmission, silicon photonics platform or systems using 1310nm & 1550nm light naturally fit with the long-reach network.

On the other hand, hybrid integration utilizes EICs and PICs in multiple chips. The fabrication process can be chosen independently. PICs can be selected by various types such as modulators and light-emitting diodes. Therefore, each

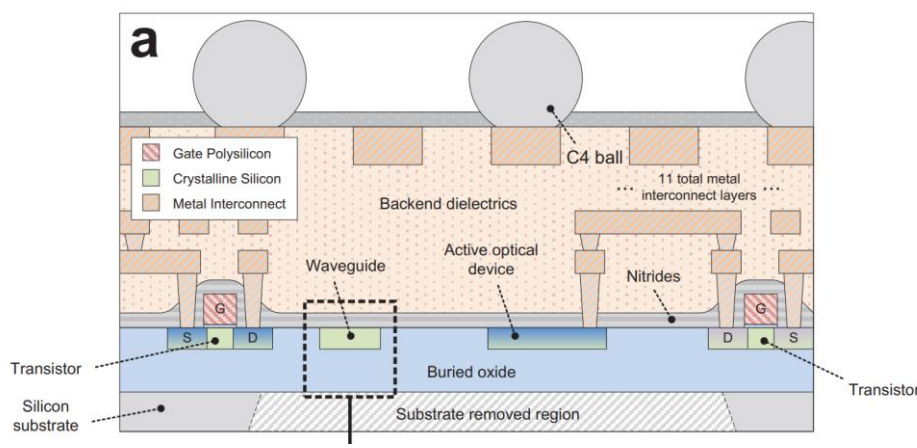


Fig. 2.8. Representative example of monolithic integration in [2.7].

advantages can be utilized simultaneously as shown in Fig. 2.9 [2.8]. The chip used in monolithic integration can be used for only PIC and EIC can be fabricated independently. For example, Fig. 2.9 uses 28nm CMOS process for the driver and SOI chip for modulators and photodiode. Furthermore, PICs fabricated with cheap process and small area occupation such as VCSEL can be utilized as shown in Fig. 2.10. However, hybrid integration has power and packaging issues since it requires wire-bonding between chips. To remedy these issues, flip-chip bonding is utilized or circuit techniques compensating the package with wire-bonding.

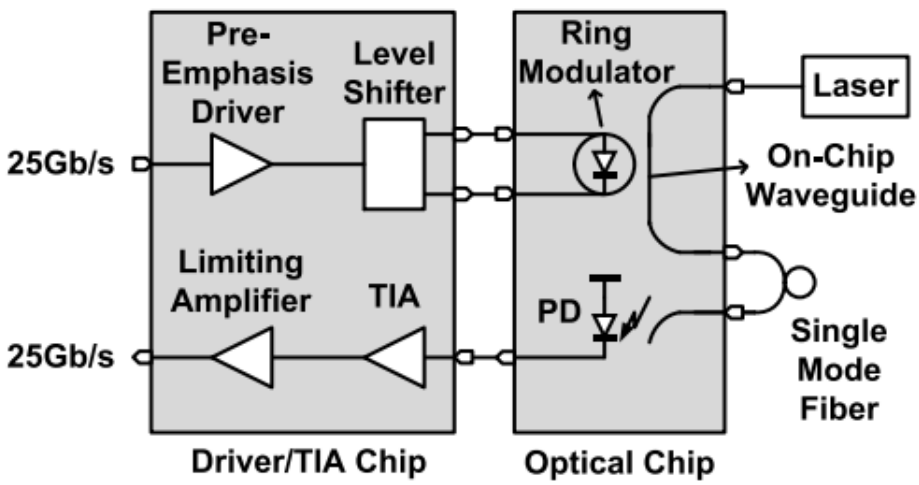


Fig. 2.9. Example of hybrid integration with silicon photonics platform in [2.8].

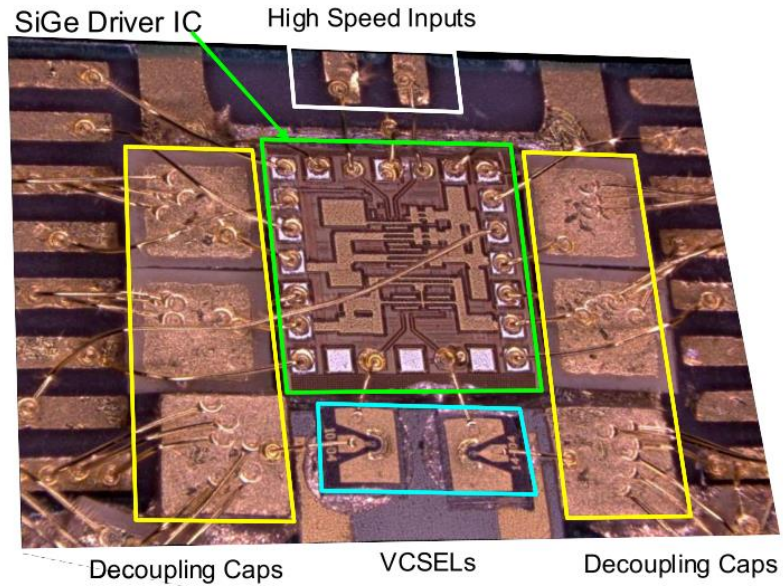


Fig. 2.10. Example of hybrid integration with VCSEL [2.9].

2.3. Basis of Data Center

As mentioned in the earlier section, optical links are mainly applied in data centers and HPCs. There are two communication systems, telecommunications and data communications, which are controlled by data centers or HPCs. Telecommunication and data communication networks are deployed via data center as shown in Fig. 2.11 and Fig. 2.12 [2.10]. Telecommunication supports data transmission from access network (~several tens of kilometers), which includes fiber to the home (FTTH), up to long-haul networks (~several thousands of kilometers). Data with optical fiber is transmitted and received through pluggable optics module such as small form-factor pluggable (SFP) and C form-factor

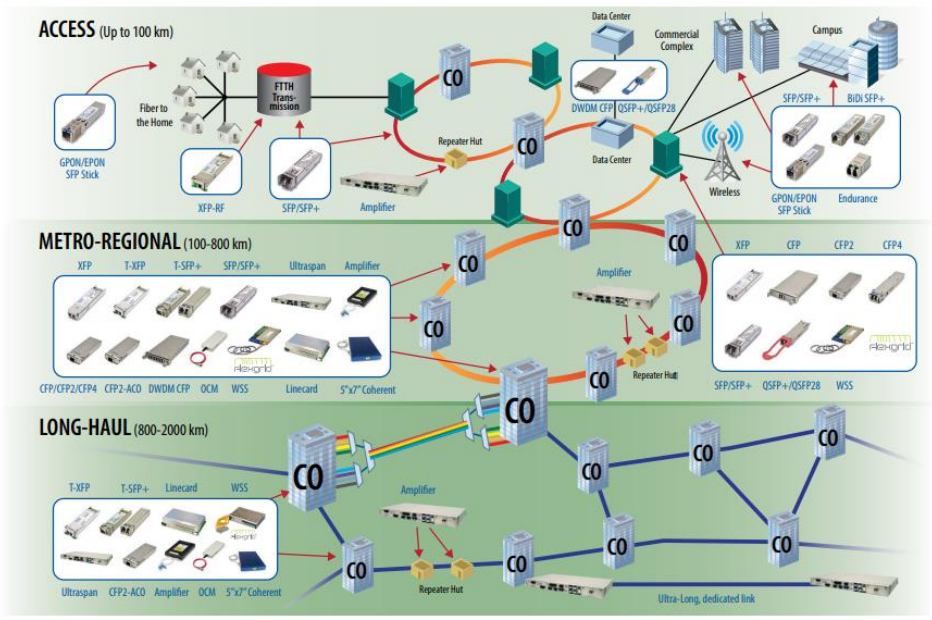


Fig. 2.11. Network diagram of telecommunication in [2.10].

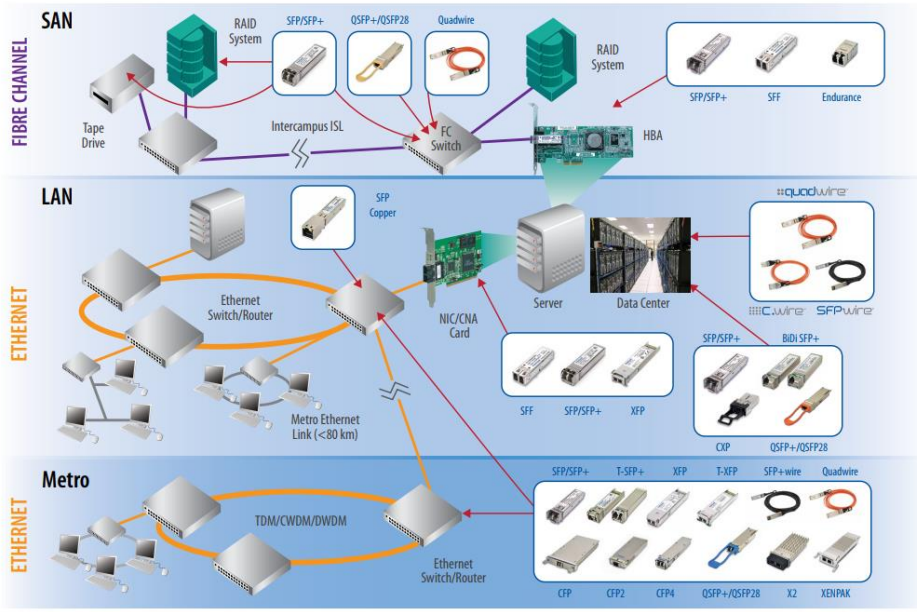


Fig. 2.12. Network diagram of data communication in [2.10].

pluggable (CFP). While transmitting/receiving data, data center takes its significant role as a control tower. On the other hand, data communication mainly deals with data storage such as local area network (LAN) and storage area network (SAN). Unlike the telecommunication, data centers in data communication takes more important role since they control the way of switching and routing data in servers. The various pluggable optics are also utilized such as telecommunication.

The system architecture of traditional data center is well described in Fig. 2.13 [2.11]. A number of racks are tied into top of rack (ToR). Copper wires are used inside ToRs, owing to its short length. Then, several ToRs are connected to Tier 1 switch through active optical cables (AOC) which are deployed up to several tens of meters and called as row. When lots of rows are tied as a group and controlled by Tier 2 switches, the group is called data center. Data is transmitted/received with

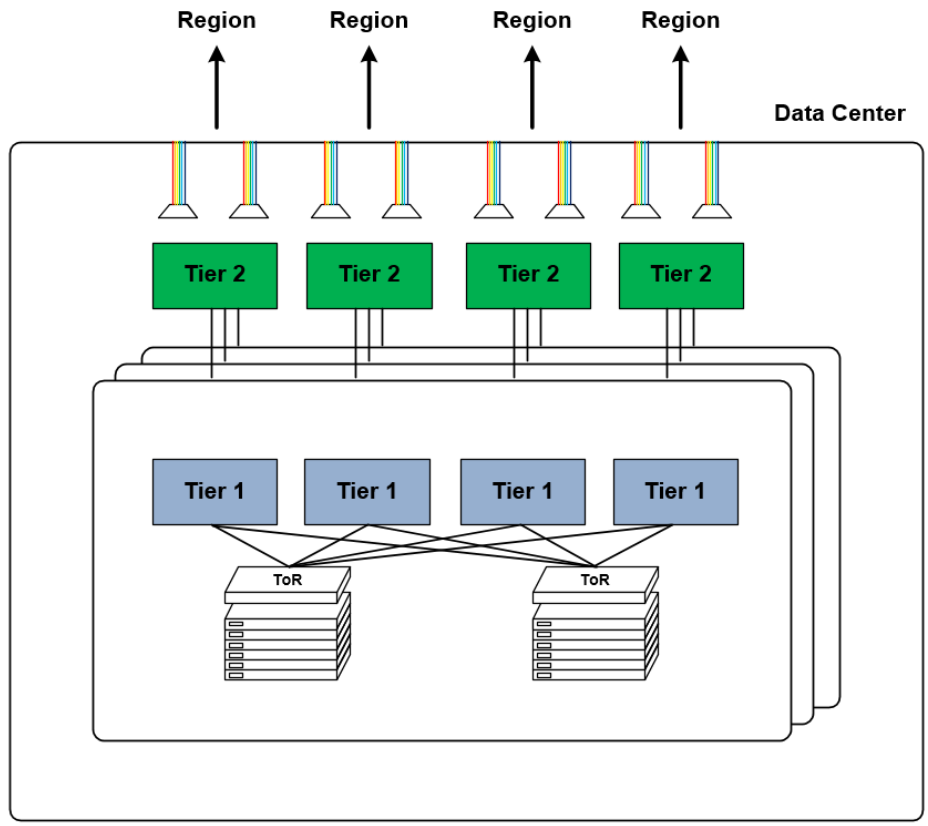


Fig. 2.13. Traditional data center.

parallel single-mode fibers (PSM) due to its long distance. Data centers are then connected to other data centers for the long distance.

2.4. Design Challenges of Optical Link in Data Center

2.4.1. Required Bandwidth of the Data Center Interconnects

Despite of having data centers, large demand of the data in both telecommunication and data communication are increasing. The data increasing trend is predicted in Fig. 2.14 [2.12]. According to the annual report, 20.6 zettabytes of data will be required in 2021, which is third times bigger than 2016.

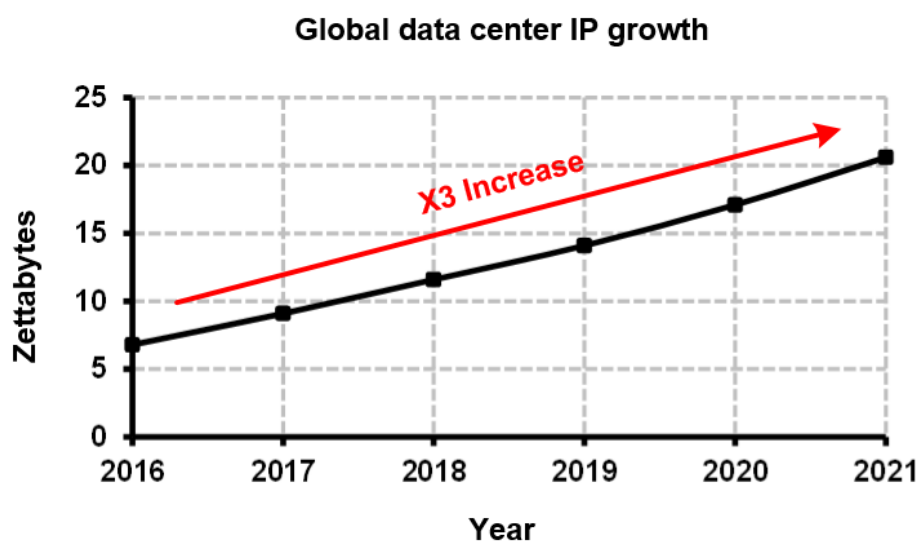


Fig. 2.14. Predicted global data center IP growth.

This trend will make data center bigger to support required data. Since there are limited number of I/O pins due to hardware constraint, per-pin bandwidth should be increased for advanced data center interconnects. Following this trends, many standards and protocols such as Ethernet, Infiniband, and Fibre Channel are proposed for 400 Gb/s data transmission.

2.4.2. Power Budget of the Data Center

Power consumption and data center area occupation as well as bandwidth are dramatically increasing as shown in Fig. 2.15 [2.12]. This is because number of I/O pins or per-pin bandwidth should be increased to meet required data demand.

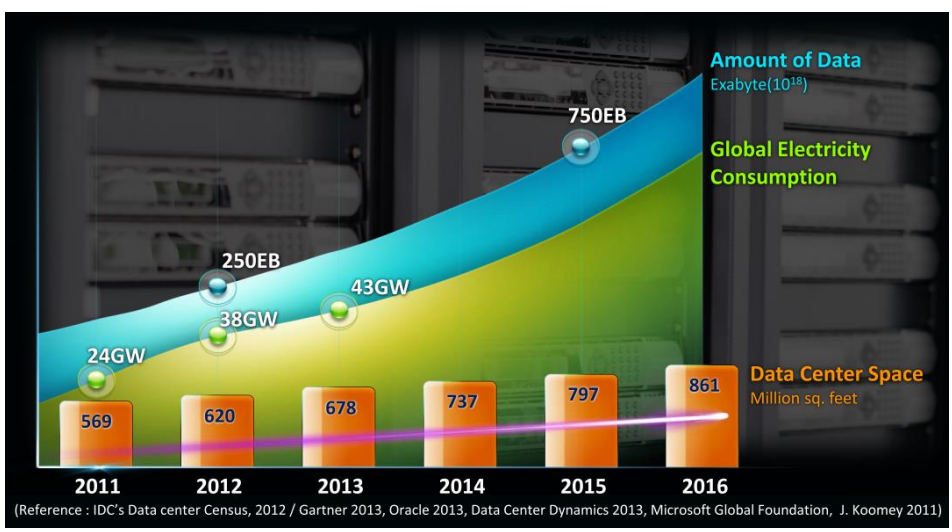


Fig. 2.15. Predicted power consumption and area occupations of data center in [2.12].

2.4.3. Future Data Center

As can be seen in earlier sections, bandwidth, power consumption, and area occupation are main design challenges when data centers are designed. Therefore, advanced hardware which supports data transmission with sufficient bandwidth is required for future data centers. Furthermore, future data centers will replace ToR switch with optical switches inside servers as shown in Fig. 2.16 [2.11]. This is

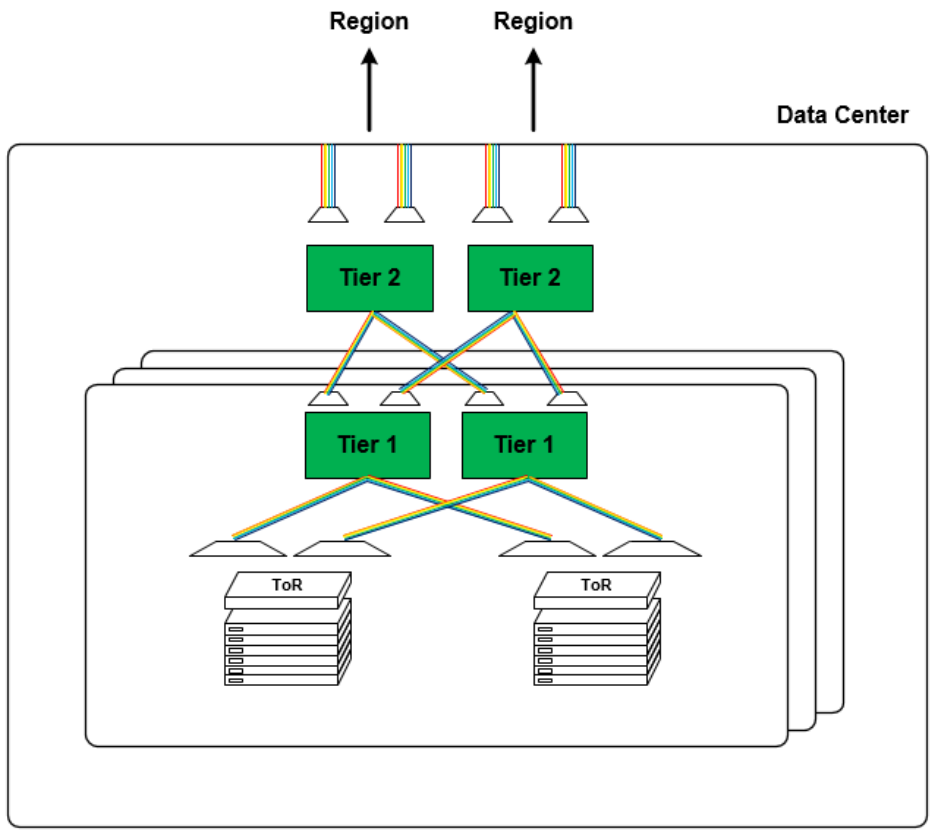


Fig. 2.16. Future data centers with advanced architectures in server.

because increased bandwidth gives burden to the traditional data center with conventional architecture. The replacement will give less power burden to Tier 1 and ToR switches and optical interconnects more important.

2.5. Basis of Optical Components for Transmitter

2.5.1. Modulator

As mentioned in the earlier section, single-mode fiber is mostly used in long-reach communications. Since single-mode fibers are compatible with silicon waveguide, on-chip modulators are suitable in long-reach communications.

There are two types of modulator which are mainly used. The first type of modulator is Mach-Zehnder modulator (MZM) and an electro-absorption modulator (EAM). The modulator is operated by the light interference using electro-optic effects such as Pockel's effect [2.14]. It has strong advantages of spectral efficiency, however modulator requires large swing and area for the light interference. The second type of modulator is ring resonator as illustrated in Fig. 2. 18. It mainly uses PN depletion or injection-type ring modulator. For high-speed operation, depletion-type ring modulators are mainly used because minority carriers have limited lifetimes for injection-type ring resonators [2.15]. When the reverse bias voltage is applied to PN junction, the refraction index becomes decreased then the wavelength is red-shifted due to Pockel's effect [2.14].

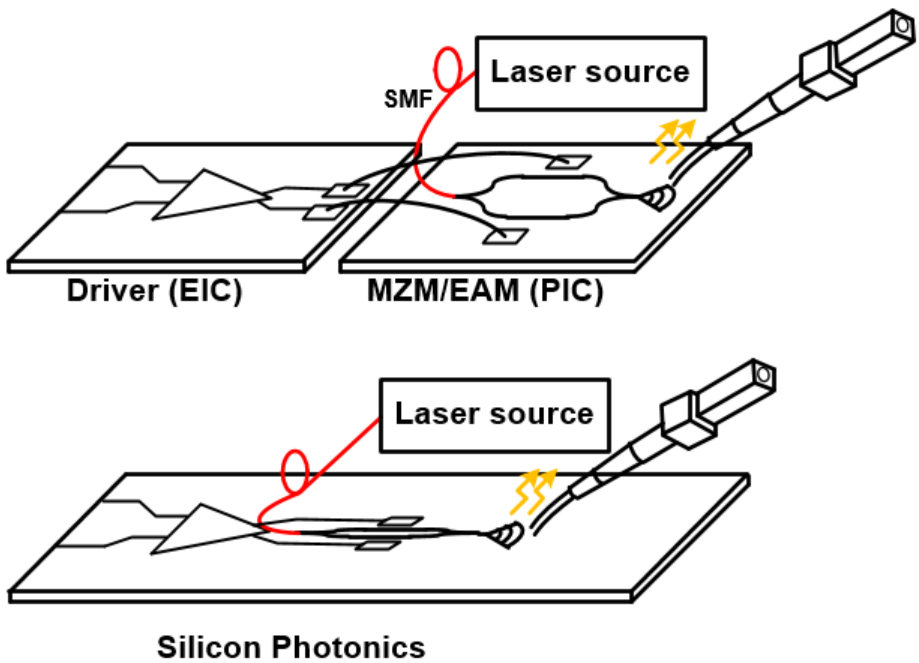


Fig. 2.17. MZM/EAM drivers with hybrid and monolithic packaging.

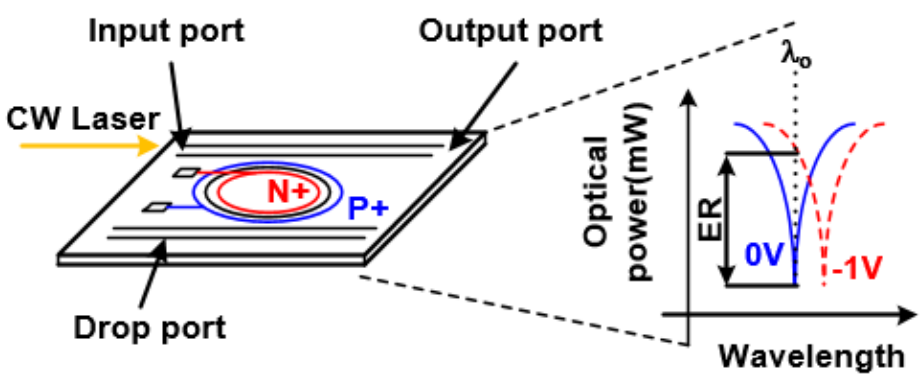


Fig. 2.18. Cross section view and operating principle of ring modulator.

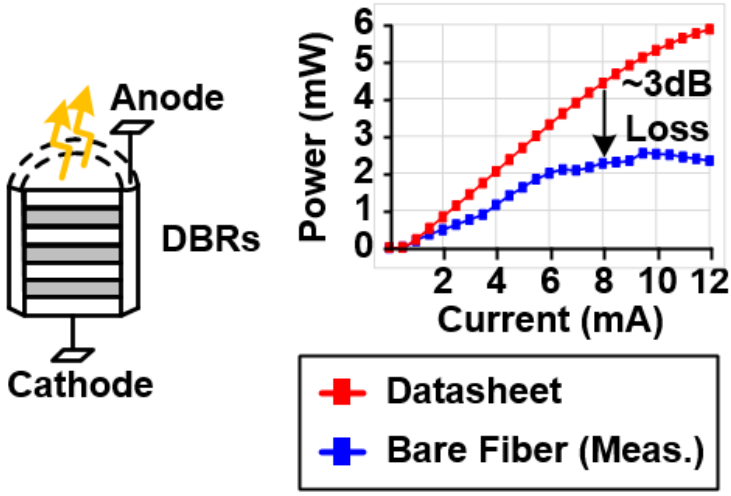


Fig. 2.19. Cross section view and L-I curve of the VCSEL.

2.5.2. VCSEL

Vertical cavity surface-emitting laser (VCSEL) emits light upside the cavity using stimulated emission as shown in Fig. 2.19. It has many numbers of distributed bragg reflector (DBR)s to achieve large optical power [2.14]. Owing to its small size and low cost, it is used widely nowadays. In addition, it can operate up to 71Gb/s NRZ data as shown in [2.9].

However, unlike modulators, VCSEL has some issues about operations and fabrications. It has only been fabricated for 850nm wavelength due to the condition of emitting light. Moreover, it has nonlinearities when the bias current is changed.

It makes the frequency response keep varying unlike other linear lumped elements such as resistor, capacitor, and inductor.

Despite of those drawbacks of VCSEL, it is very promising solutions since it has low fabrication cost. Also, it can be highly integrated in two-dimensional array. Furthermore, advanced VCSELs are fabricated which can operate up to single-mode fibers [2.16] and 1550nm [2.17] .

Chapter 3

High-Speed Optical Driver Implementations With Power-Efficient Push-Pull Driving Scheme

3.1. Overview

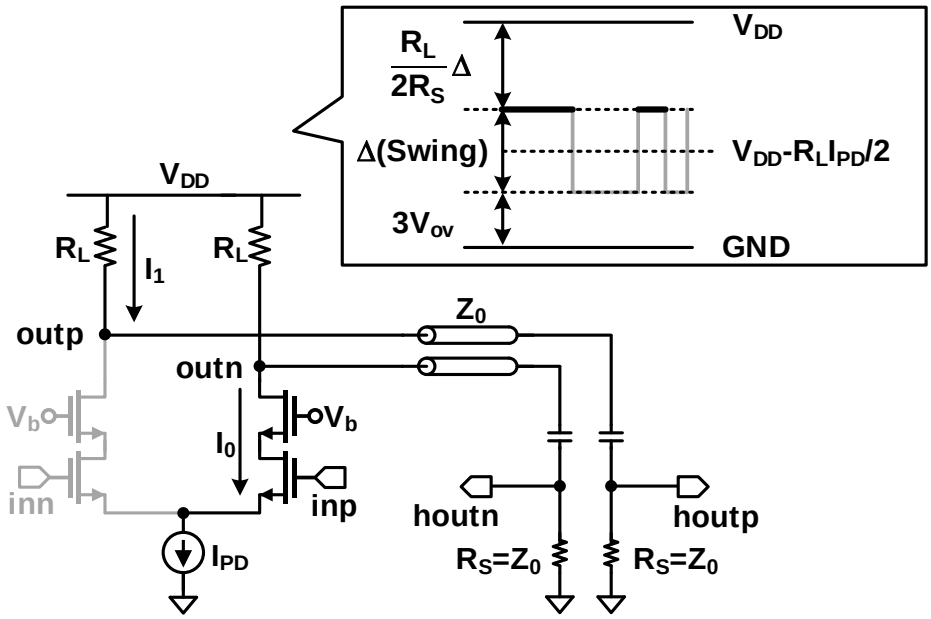
There have been various types of drivers implemented in many optical transmitters. As similar with conventional electrical transmitter, voltage-mode and current-mode drivers are mainly utilized. The main parameters for efficient driver is operation speed, power consumption, and swing. Unlike electrical drivers, drivers used in optical interface have more importance for swing than termination. Therefore, to achieve the performance of the driver, push-pull driving technique,

which is power-efficient, high-speed, and large swing technique is discussed in this Chapter. After analyzing push-pull driving scheme, specific implementations of the driving scheme will be shown. The first will be MZM/EAM driver which requires large swing for the given length to utilize interference like conventional MZM interferometers [3.1]. Next, multi-channel HDMI AOC driver will be discussed with the same driving technique [3.2].

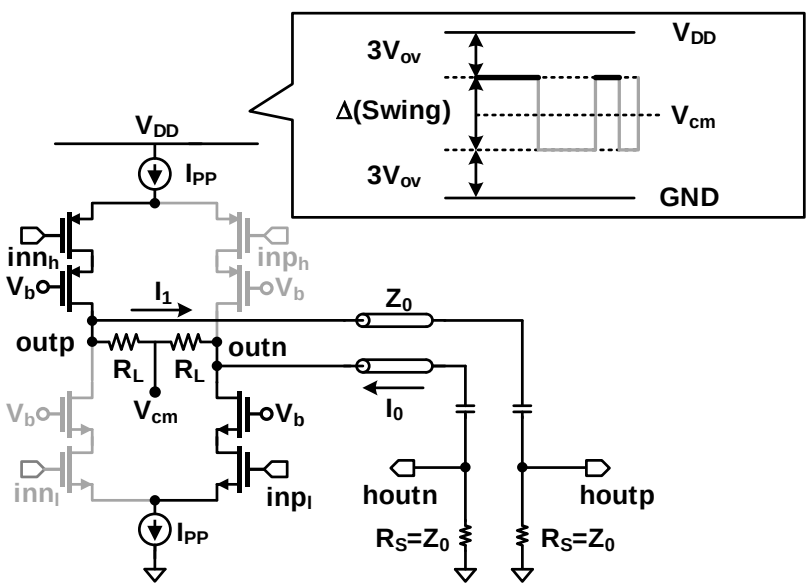
3.2. Push-Pull Technique in Current-Mode Driver

Two types of current-mode signaling schemes, pull-down only driver and push-pull driver, are shown in Fig. 3.1. Both schemes drive the modulator, terminated with R_S matched to the transmission line impedance Z_0. Drivers include load resistors R_L and cascode transistors biased with the bias voltage V_b to reduce the voltage stress. Further, DC block capacitors are used to decouple the bias condition of the modulator from that of the driver. The following analyses assume that the DC block capacitors are settled to their final DC values. The focus of the analyses is the difference between the source currents and the required supply voltages to achieve the same single-ended peak-to-peak output swing (Δ). As shown in Fig. 3.1(a), the common-mode DC voltage at the output of the pull-down only driver is V_{DD}-$R_L I_{PD}/2$ and the single-ended peak-to-peak output swing Δ is expressed as $I_{PD}(R_L R_S)/(R_L+R_S)$. Assuming that the input and current source transistors have the same overdrive voltage V_{ov} and operate at the edge of the saturation region, the minimum required supply voltage is $(R_L/(2R_S)+1)\Delta+3V_{ov}$.

The load resistors R_L in the pull-down only driver carry current only in one direction; however, bipolar current flow is possible for the push-pull driver as shown in Fig. 3.1(b). When the data '1' is driven at the node *outp*, the current I_1 flows from the load resistor R_L on the left to the load resistor on the right. On the



(a)



(b)

Fig. 3.1. Driver comparison of pull-down only driver and push-pull driver. (a) Pull-down only driver: data ‘1’ and (b) push-pull driver: data ‘1’.

contrary, the current I_0 representing data '0' flows in the opposite direction. Using the same assumption used in the pull-down only driver, the minimum supply voltage is $\Delta+6V_{ov}$.

Fig. 3.2 compares the power consumption of the pull-down only driver and the push-pull driver analytically. Compared with the pull-down only driver, the push-pull driver requires only half the current to achieve the same output swing. When all overdrive voltages of the transistors are assumed as V_{ov} for comparison, the power consumption for the pull-down only driver ($Power_{PD}$) and the push-pull driver ($Power_{PP}$) with the minimum power supply can be calculated as

$$Power_{PD} = \frac{R_L+R_S}{R_L R_S}\left(3V_{ov} + (\frac{1}{2}\frac{R_L}{R_S}+1)\Delta\right)\Delta \tag{3.1}$$

$$Power_{PP} = \frac{R_L+R_S}{R_L R_S}\left(3V_{ov} + \frac{\Delta}{2}\right)\Delta \tag{3.2}$$

From equations (3.1) and (3.2), it can be determined that the push-pull driver is more power-efficient than the pull-down only driver. Power consumption versus the load resistance is also shown in Fig. 3.2(b) with a 2-V single-ended peak-to-peak swing. The graph shows that the large load resistance makes the driver more power-efficient. However, the larger resistance than the impedance of the transmission line degrades the signal integrity and sacrifices speed performance due to under termination at the source.

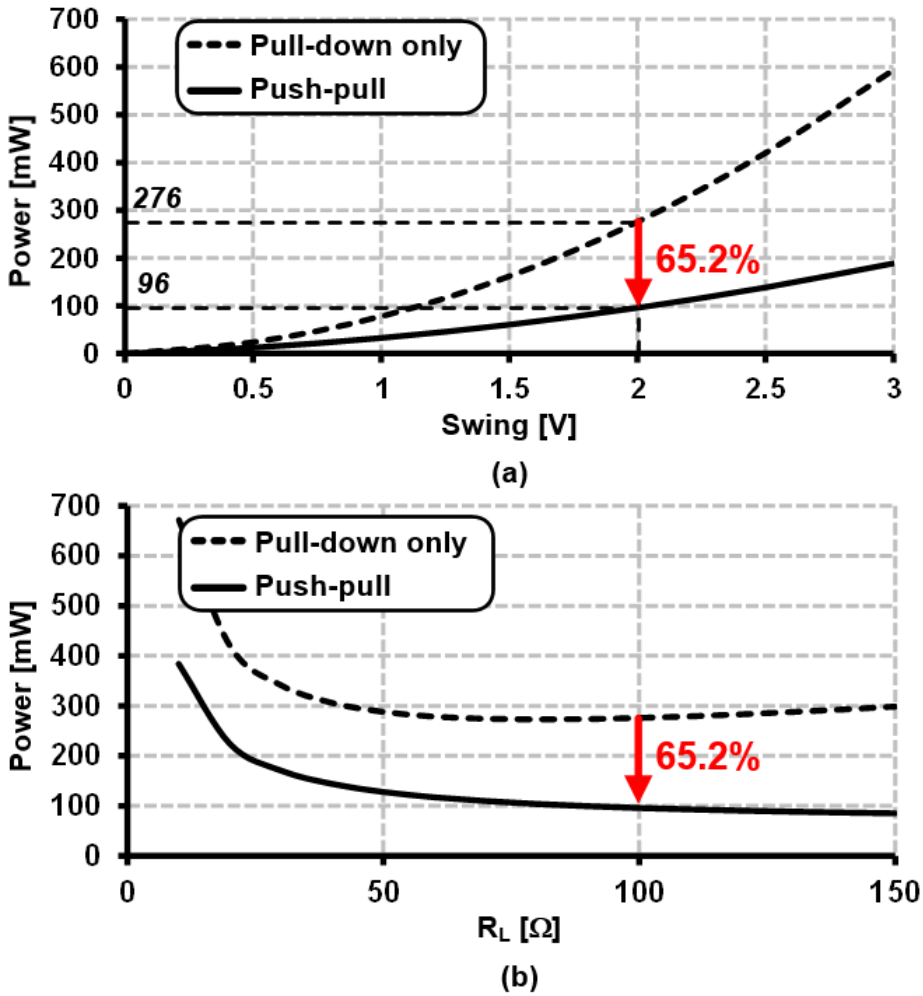


Fig. 3.2. Comparison of the estimated power consumption between the pull-down only logic and push-pull logic: (a) R_L=100 Ω and (b) varying R_L.

3.3. Mach-Zehnder/Electro-Absorption Modulator Driver

3.3.1. Previous Works

As data rates required for digital communication continue to rise, silicon photonics has become one of the most promising candidates for the next generation

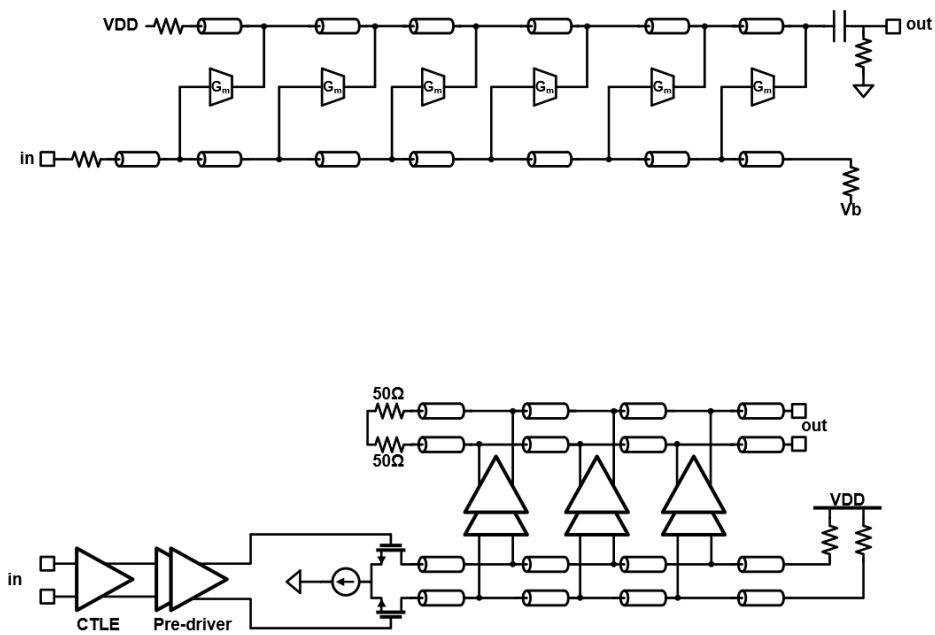


Fig. 3.3. Previous works of modulator driver.

of high-speed link technology. Recently, various types of modulators for silicon photonics have been developed, i.e., a Mach-Zehnder modulator (MZM) and an electro-absorption modulator (EAM). The MZM introduces interference between two optical paths using electro-optic effects [3.3]. The EAM absorbs different amounts of the light depending on the reverse bias voltage [3.4]. Both modulators require a large input swing in order to achieve a sufficient extinction ratio (ER) [3.3], [3.4]. To generate the large swing, a digitally controlled distributed amplifier [3.5], [3.6], multi-stage driver [3.7], and pull-down only drivers [3.8]-[3.10] have been proposed as shown in Fig. 3.3. However, the abovementioned drivers consume high power, typically larger than 10 mW/Gb/s. Among the various types of drivers, we analyze and compare the power and swing of pull-down only current-mode logic (CML) driver and the push-pull CML driver in this Chapter. The push-pull CML driver is proposed as the most efficient candidate and optimized for MZM/EAM applications to improve the power efficiency and 32 Gb/s operation, which is shown in Fig. 3.2. The cascode structure is added in the proposed driver in order to alleviate the over-voltage stress while achieving a sufficiently large voltage swing of 4 Vppd [3.1], [3.10]-[3.12]. In addition, shunt-peaking inductors are placed in series with the load resistors for the pre-driver and the main driver to extend the bandwidth and to achieve a flat group delay response simultaneously [3.13].

3.3.2. Proposed MZM/EAM Driver

The value of the load resistor R_L is chosen as 100 Ω as a trade-off achieving a good power efficiency while satisfying the bandwidth requirement as [3.14], whereas 50 Ω resistors are used in previous works, [3.1], [3.6], [3.9], [3.10]. In addition, difference between pull-up current and pull-down current makes the rise and fall times asymmetric. The common mode voltage is supplied to solve these issues.

For a large output voltage swing, a cascode structure with thin-oxide

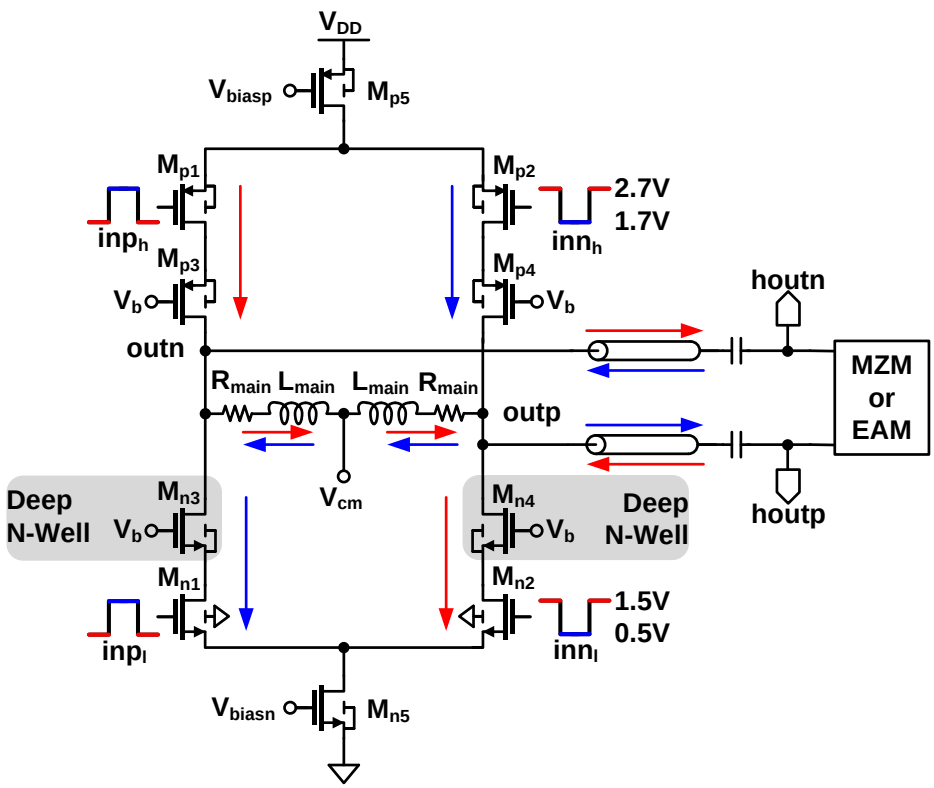


Fig. 3.4. Driver comparison of pull-down only driver and push-pull driver. (a) Pull-down only driver: data ‘1’ and (b) push-pull driver: data ‘1’.

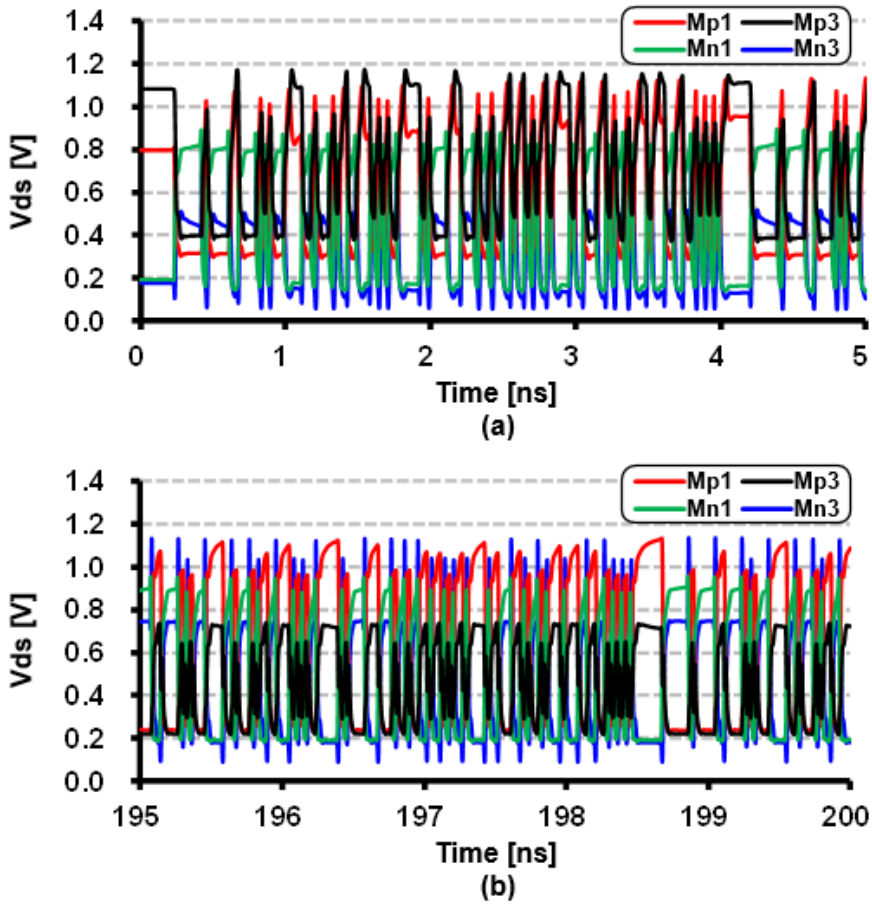


Fig. 3.5. Voltage stress of the main driver. (a) Before settling and (b) after settling.

transistors is used to protect the transistors from the over-voltage stress while achieving both high bandwidth and large swing. In addition, deep n-well NMOS transistors (M_{n3}, M_{n4}) have their body nodes connected to their source, mitigating the voltage stress further and eliminating the body effect [3.3], [3.10]. The body nodes of the PMOS transistors (M_{p1}-M_{p4}) are also connected to their sources for the same reason. As a result, the drain-source voltage stress of the cascode transistors are less than 1.2 V during the transient and steady state as shown in Fig. 3.5.

Since the required voltage range is different between the pair of NMOS (M_{n1}-M_{n2}) and PMOS (M_{p1}-M_{p2}) transistors for the main driver, high-speed sub-blocks such as the pre-driver and the level converter are designed for the optimum pre-driver swing. Fig. 3.6 shows the overall architecture of the transmitter. Pre-drivers and a level converter are implemented with a pull-down only driver configuration, since they do not require a large output swing. A differential input of 1-V swing is applied to the first buffer. The output of the second buffer is applied to the level converter to generate a high common-level input for the proposed push-pull CML driver. The level converter uses an on-chip AC-coupling capacitor C_b of 1.8 pF and an on-chip DC-bias resistor R_b of 10.2 kΩ. It achieves a cut-off frequency of 8.7 MHz, which is sufficiently low to transmit a 32 Gb/s PRBS7 data pattern. The pre-drivers and the level converter utilize shunt-peaking inductors for the bandwidth extension. Shunt-peaking inductors, using only a metal-8 (M8) layer, are optimized using an EM simulation tool for the compact area and the proper frequency response for transmitting high-speed signals.

As shown in Fig. 3.6, it is essential to consider the interface parasitics of the

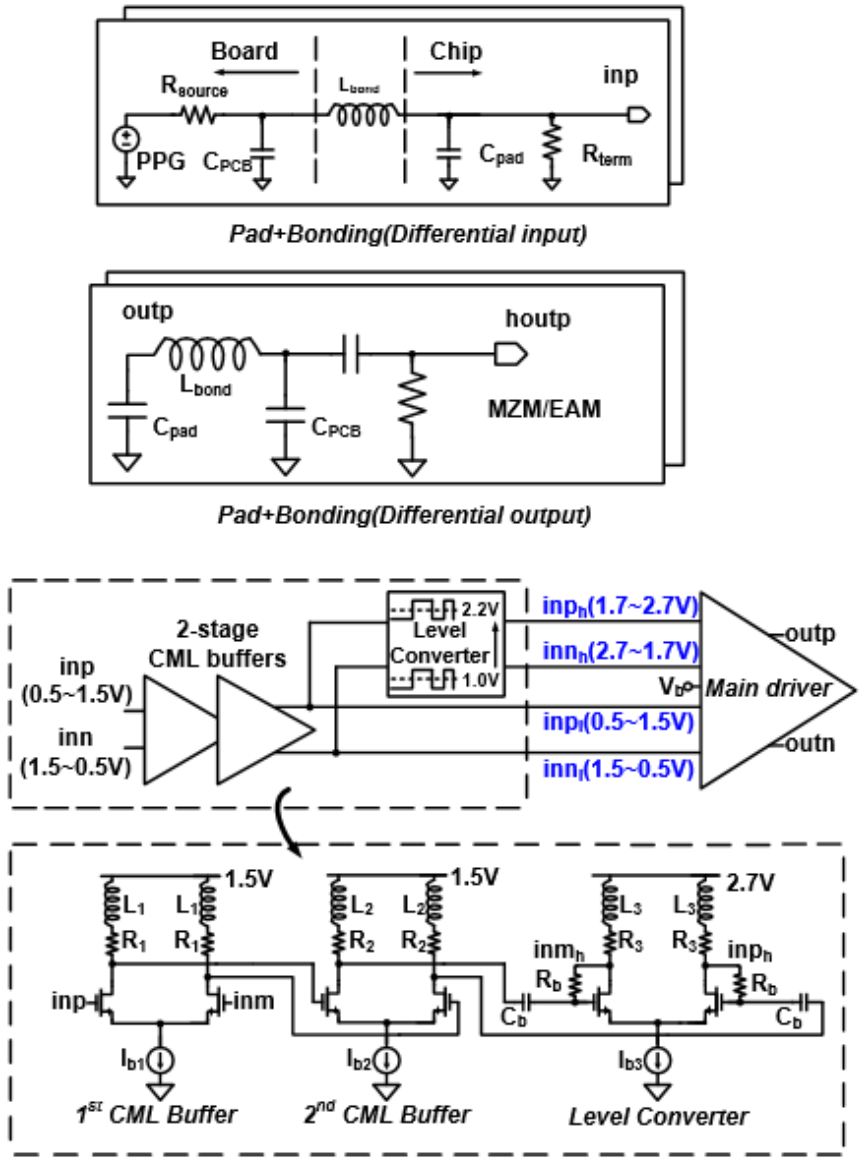
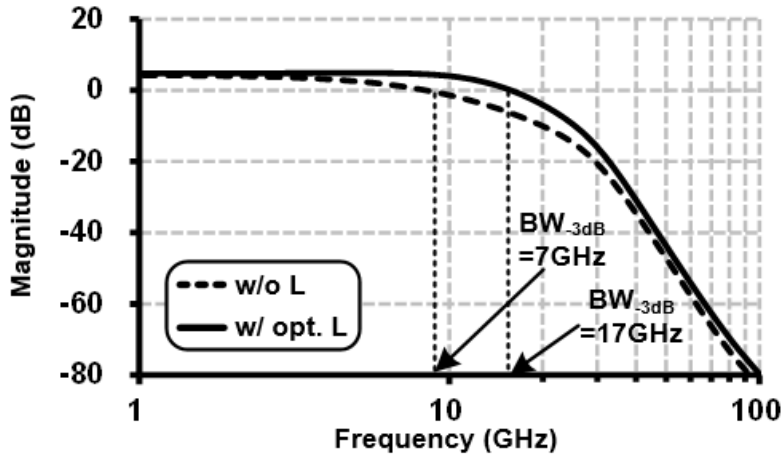
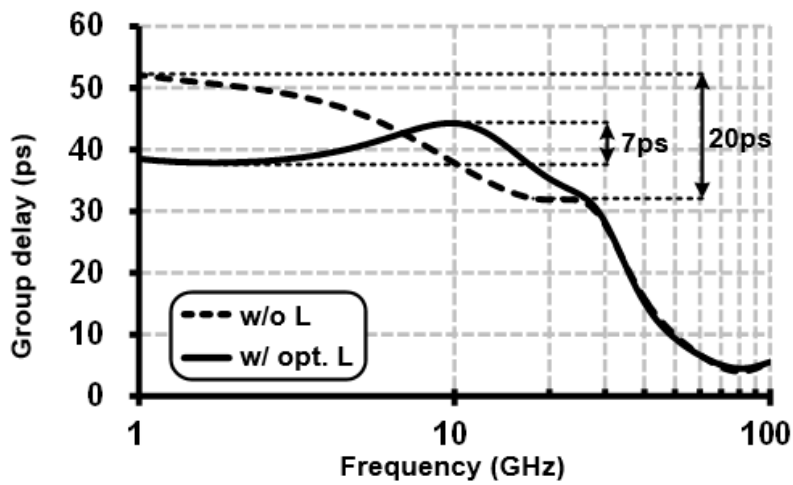


Fig. 3.6. Overall architecture of the transmitter.



(a)



(b)

Fig. 3.7. Simulated frequency response of the overall transmitter: magnitude and group delay in the case of without inductors and with optimized inductors.

Table. 3.1. Descriptions of passive components in MZM/EAM driver

	L [pH]	R [Ω]
1st CML buffer (L_1, R_1)	510	65
2nd CML buffer (L_2, R_2)	330	30
Level converter (L_3, R_3)	330	30
Main driver (L_{main}, R_{main})	510	100

chip such as the pad capacitance and bond wire inductance since they become critical when a high-speed signal is transmitted. The pad capacitance is 80 fF and bond wire inductance is 500 pH. In order to verify the optimal operation of shunt-peaking inductors for transmitting high-speed signals, the magnitude response and group delay response of the overall transmitter are simulated. As shown in Fig. 3.7, the transmitter offers the bandwidth of 17 GHz and exhibits a peak-to-peak group delay variation of 7 ps over the range of 1-17 GHz, which is sufficiently low for the target bandwidth. Shared shunt-peaking inductors for both pull-up and pull-down paths are used instead of using separate inductors, which make the driver area-efficient. The optimized values of the inductors and resistors used for the entire transmitter are described in Table 3.1.

3.3.3. Measurement Results

Fig. 3.8 shows the die photomicrograph of the prototype chip fabricated using the 65 nm CMOS process. The active area of the driver is only 0.086 mm2. Since the proposed driver uses a partially terminated load, a reflection characteristic of the electrical channel is important. Therefore, the test board with its traces designed in microstrip is verified by the EM simulation tool to keep the reflection loss S_{11} and the transmission gain S_{21} within an acceptable level. Measured results show S_{11} below -15 dB and S_{21} above -3 dB at 20 GHz for a differential input/output trace as shown in Fig. 3.9. The electrical eye diagram of the proposed driver is measured by an Agilent 86100D DCA-X wide-bandwidth oscilloscope. Rise/fall times and peak-to-peak jitter are compared in Fig. 3.10. Rise/fall time mismatch and peak-to-peak jitter becomes larger with the common mode node floating. The

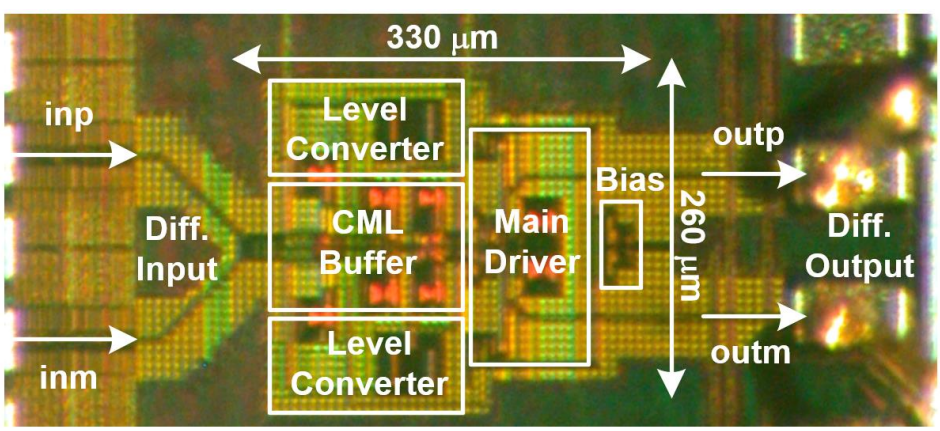


Fig. 3.8. Die photomicrograph.

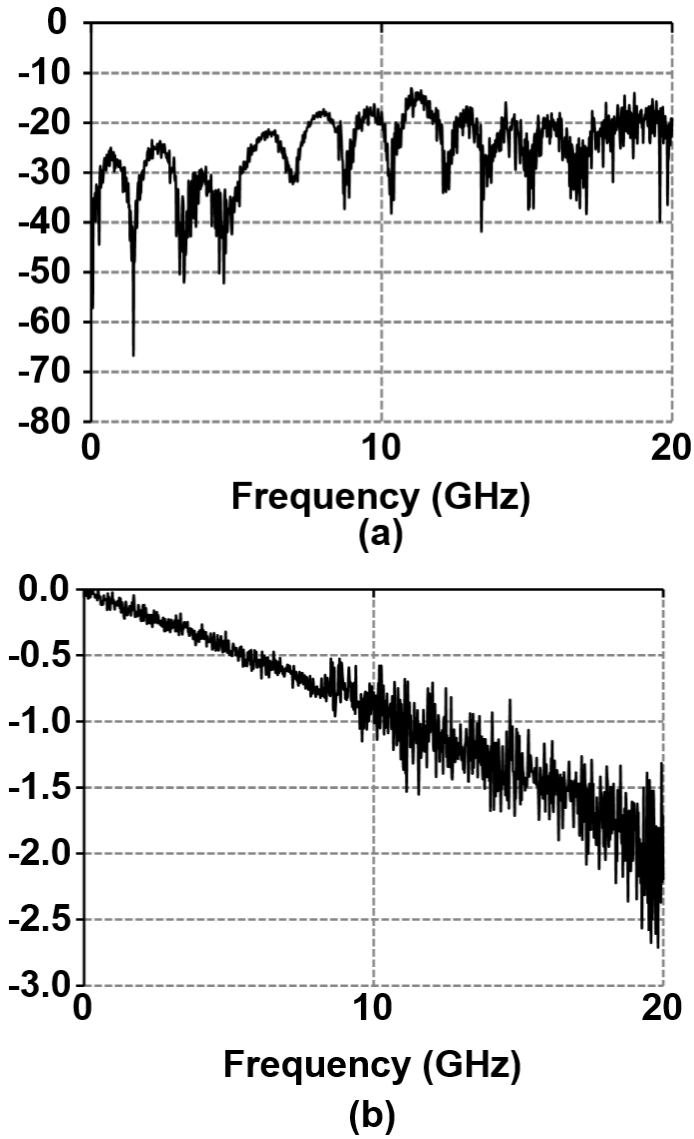


Fig. 3.9. Measured S-parameters: (a) S_{11} and (b) S_{21}.

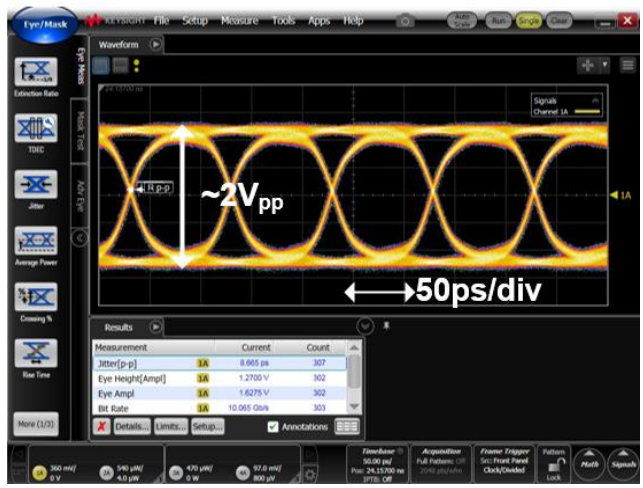
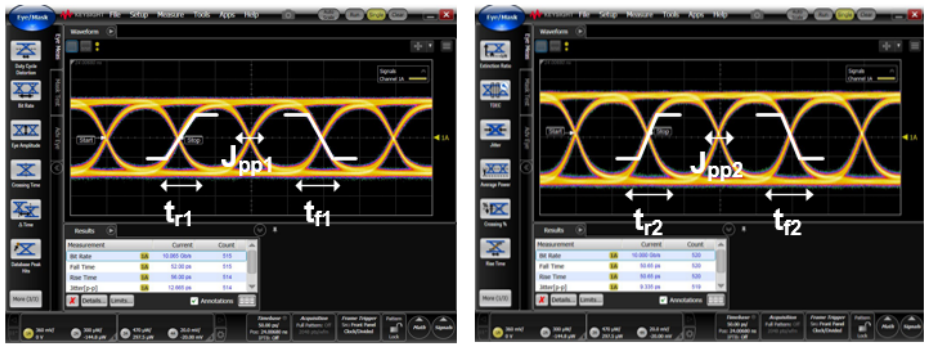


Fig. 3.10. Measured electrical single-ended eye diagram at 10 Gb/s.

measured single-ended output swing is 2 V_{pp} at 10 Gb/s, as shown in Fig. 3.11. Fig. 3.12 shows that the proposed driver has timing margins of 0.52 UI and 0.24 UI at the bit error rate (BER) of 10-12 for 28 Gb/s and 32 Gb/s, respectively. The bathtub curve is measured by an Anritsu MP1800A signal quality analyzer. The prototype driver is connected to a 40 Gb/s LiNbO3 MZM with a polarization controller and a 1:1 splitter via the DC block module as shown in Fig. 3.13. It is later connected to a 43 Gb/s Oki EAM laser module, which includes both EAM and the distributed feedback laser (DFB) in the same module as shown in Fig. 3.14. The optical eye diagrams for the MZM and EAM are



(a) (b)

	Rise time (10% to 90%)	Fall time (90% to 10%)	Jitter (Peak-to-peak)
(a) CM OFF	t_{r1} = 56 ps	t_{f1} = 52 ps	J_{pp1} = 12.67 ps
(b) CM ON	t_{r2} = 50.65 ps	t_{f2} = 50.65 ps	J_{pp2} = 9.34 ps

Fig. 3.11. Measured rise/fall time and peak-to-peak jitter comparison at 10 Gb/s.

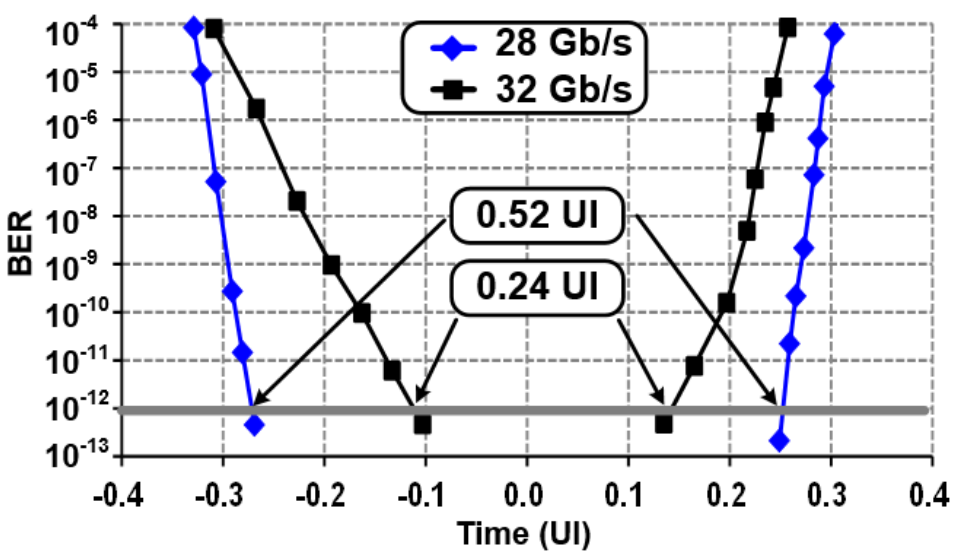


Fig. 3.12 Measured electrical bathtub curve using 28 Gb/s and 32 Gb/s PRBS7.

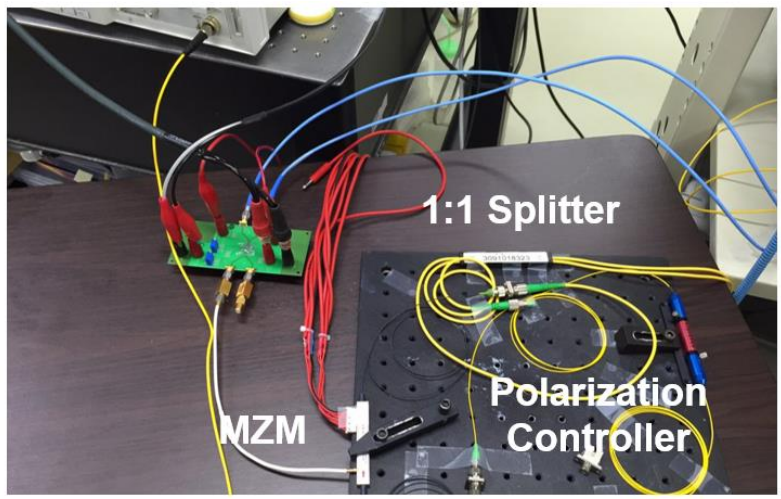


Fig. 3.13 Measurement setup of driver with MZM.

measured by the same oscilloscope used for the electrical eye diagram. The optical eye diagrams are shown in Fig. 3.15. PRBS7 data pattern is passed directly to the driver for both MZM and EAM without any bias-T. ERs of 5.08 dB at 28 Gb/s and 4.53 dB at 32.4 Gb/s are measured in MZM while ERs of 4.59 dB at 27.8 Gb/s and 4.17 dB at 32.4 Gb/s in EAM. With the differential configuration of the MZM and EAM, ER can be improved by 3 dB as in [3.6]. The pre-driver composed of first and second CML buffers consumes 49 mW utilizing a 1.5 V supply. The level converter carries the drive voltage to the upper voltage range while dissipating 49 mW with a 2.7 V supply. The core block, the main driver, consumes 103 mW with a 3.3 V

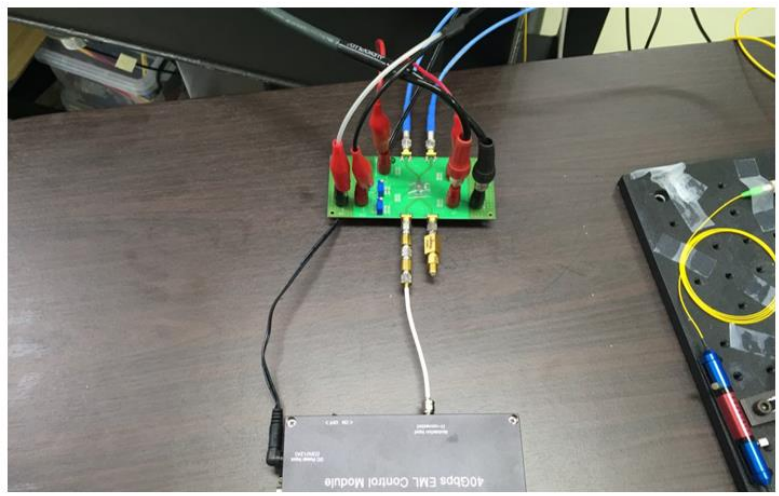


Fig. 3.14 Measurement setup of driver with EAM.

supply as estimated in Section 3.2. The entire transmitter consumes 201 mW. Compared with the state-of-the-art works shown in Table II, the proposed transmitter achieves the highest power efficiency of 7.18 mW/Gb/s at 28 Gb/s and 6.28 mW/Gb/s at 32 Gb/s for both modulators.

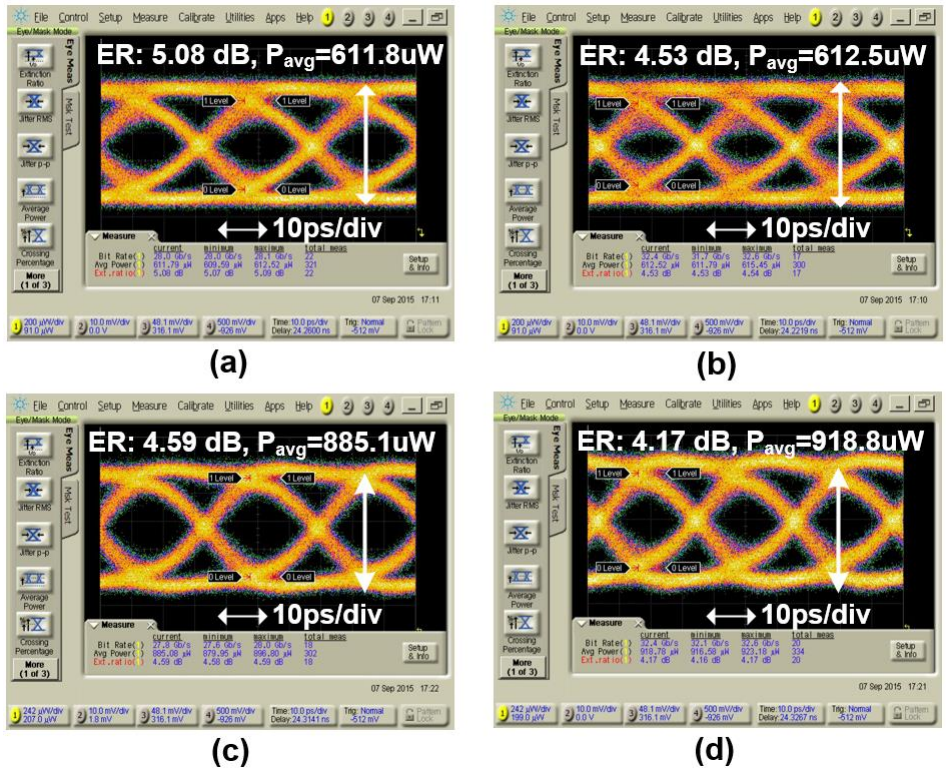


Fig. 3.15 Measured optical eye diagrams. (a) 28 Gb/s MZM, (b) 32 Gb/s MZM, (c) 28 Gb/s EAM, and (d) 32 Gb/s EAM.

Table 3.2 Comparison table with state-of-the-art works

	TVLSI'16 [3.3]	ISSCC'13 [3.5]	OFC'15 [3.6]	ISSCC'15 [3.7]	TVLSI'14 [3.8]	ASSCC'15 [3.9]	TCAS'16 [3.10]**		Letter'15 [3.15]	This Work
Technology	65 nm CMOS	180 nm BiCMOS	65 nm CMOS	65 nm CMOS	130 nm CMOS	65 nm CMOS	65 nm CMOS		130 nm CMOS	65 nm CMOS
Main topology	Pull-down only VML	Distributed amplifier	Distributed amplifier	Multi-stage	Pull-down only CML	Pull-down only CML	Pull-down only CML		Push-Pull VML	Push-Pull CML
Supply voltage [V]	1.0/2.0/3.0	-5.2/5	4.5	1.25/2.5	1.2/4.0	1.2/3.3	Type 1 1.5/2.3/2.6	Type 2 1.5/3.9	1.6/3.3	1.5/2.7/3.3
Data rate [Gb/s]	10	10	25	25	20	25	20	25	20	32
Power [mW]	98	2130	520	275	900	480	534	348	312	201
Output swing [$V_{pp,diff}$]	4.4	6	6.4	5	7	3.3	5	3.8	3.4	4(@10Gb/s)
Single-ended ER[dB]	N/A	N/A	1.07*	3.1*	9.78 (@10Gb/s)	N/A	N/A	N/A	5.01	4.53(MZM) 4.17(EAM)
Active area [mm^2]	0.04	0.95	N/A	0.6	0.72	0.029	0.068	0.038	N/A	0.086
Bias-T	X	X	X	X	O	O	O	X	X	X
F.O.M [mW/Gb/s]	9.8	213	20.8	11	45	19.2	26.7	13.9	15.6	6.28

*Calculated from differential ER

**Driver type1 & type2

3.4. HDMI 4-Channel Driver for AOCs

3.4.1 Previous Works

The required data rate keeps increasing due to the large demand of applications such as display interface. The increasing tendency for the data demand will continue due to the augmented/virtual reality [3.16], [3.17]. High-definition multimedia interface (HDMI) is one of the most promising solutions for the enormous data. To meet this demand, different kinds of high-speed supporting HDMI cables are in production. For example, HDMI 2.0 cables support 3 high-

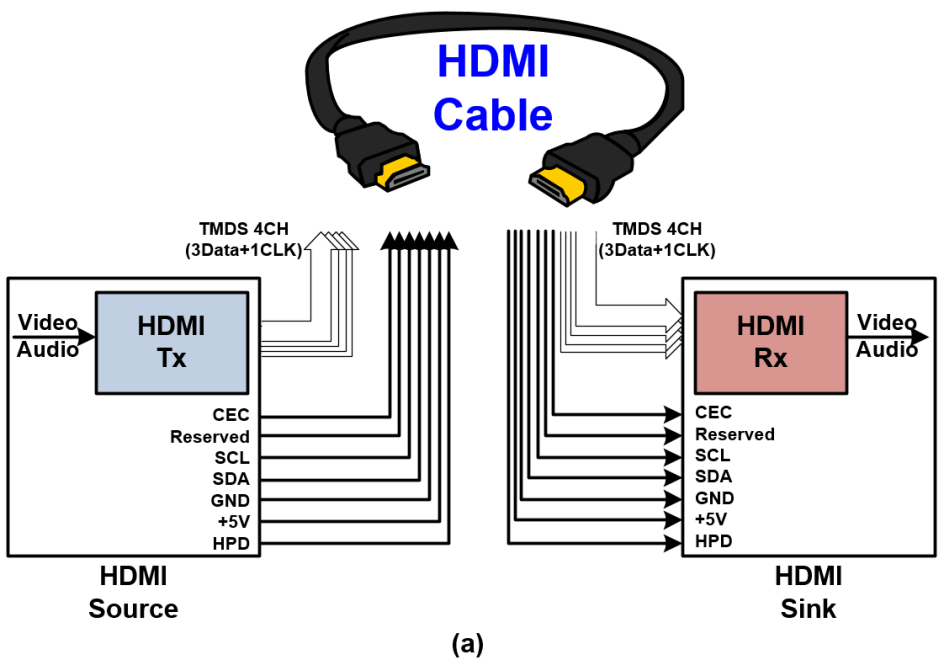


Fig. 3.16 Pin configurations of HDMI electrical cable.

speed data channels, transmitting at 6 Gb/s in 8b/10b data format, and an additional clock channel as shown in Fig. 3.16. The auxiliary signals, consumer electronic control (CEC), I2C control pins (SCL and SDA), and hot plug detect (HPD) also help HDMI operate normally [3.18]. In spite of various additional pins, the price and power consumption of the cable rise exponentially as the length of the cable gets longer and data rate increases higher to compensate the cable loss.

Data transmission with light can solve these issues, since it doesn't require any complex equalizations. The alternate HDMI solution with light, HDMI active optical cable (AOC), is described in Fig. 3.17. Instead of equalizers or repeaters, power-efficient drivers and transimpedance amplifier (TIA) should be designed for

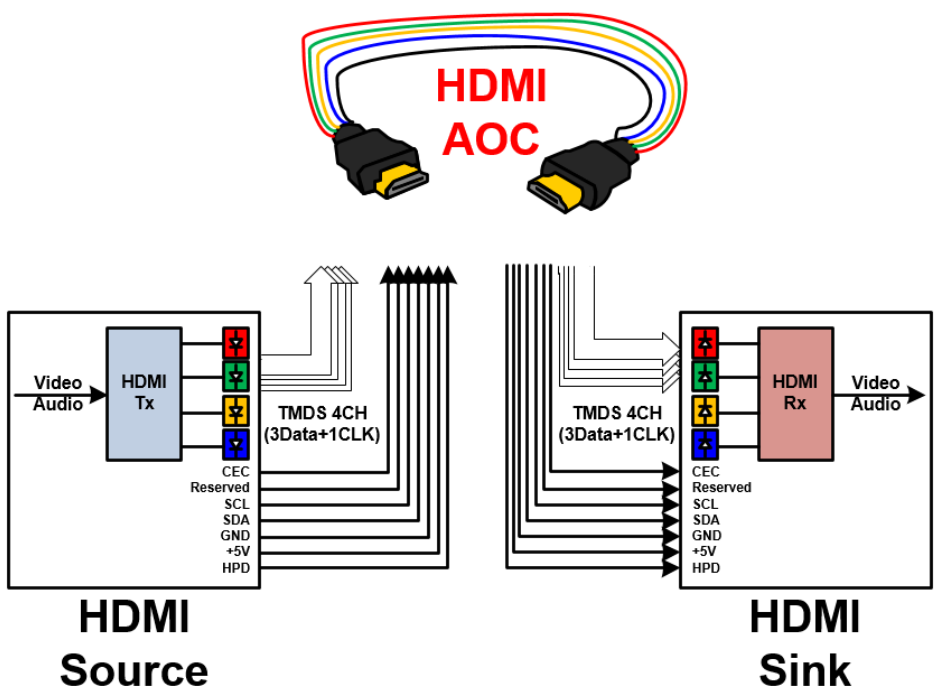


Fig. 3.17 Pin configurations and conceptual model of HDMI AOC.

additional optical components such as vertical-cavity surface-emitting laser (VCSEL) and photodiode (PD).

In this section, HDMI applicable 4-channel push-pull VCSEL drivers are fabricated in 0.18- μm CMOS for HDMI AOC [3.2]. Schematics and properties for two types of driver are described in the next Section. Measurements including S-parameters and eye diagrams with 4-channel VCSEL arrays are also shown in the next Section..

3.4.2 Proposed HDMI AOC

There are some main features HDMI transmitters should follow for the normal operation: 1) transition-minimized differential signaling (TMDS), similar to 8b/10b encoding, should be transmitted for 3 data channels; 2) clock can be transmitted in variable frequency such as blanking period [3.18]; 3) total current supplied by 5-V power line should be less than 55 mA (<275 mW) [3.18]. For these requirements, many conventional pull-down only current-mode logic (CML) drivers have been used for the operation. However, since AOC has additional components, it should be power-efficient by different driver designs. Power-efficient push-pull driving scheme is applied to proposed drivers for this reason [3.11], [3.19]-[3.22]. Fig. 3.18 shows the comparison between conventional pull-down only [3.23]-[3.28] and push-pull driving schemes. To compare power efficiency between them, power consumption is fixed to IBVDD. As a result, current ratio (Iv(a)/Iv(b)) between Fig. 3.18(a) and Fig. 3.18(b) is smaller than 1. It shows that push-pull driving scheme achieves larger swing than pull-down only driving scheme when consuming the same power for the same supply [3.1]. Also, a 3.3-V supply voltage is used for the standard 0.18-μm CMOS process and total power budget of the HDMI AOC. Drivers are optimally designed with Verilog-A VCSEL model which reflects light information in addition to I-V (Current-Voltage) characteristics [3.28]. AC simulations are also performed for the signal integrity simultaneously. Furthermore, both drivers drive not only VCSEL chips, but also ESD protection cells for the pad (~1kV HBM). Two types of the VCSEL driver architecture are described below.

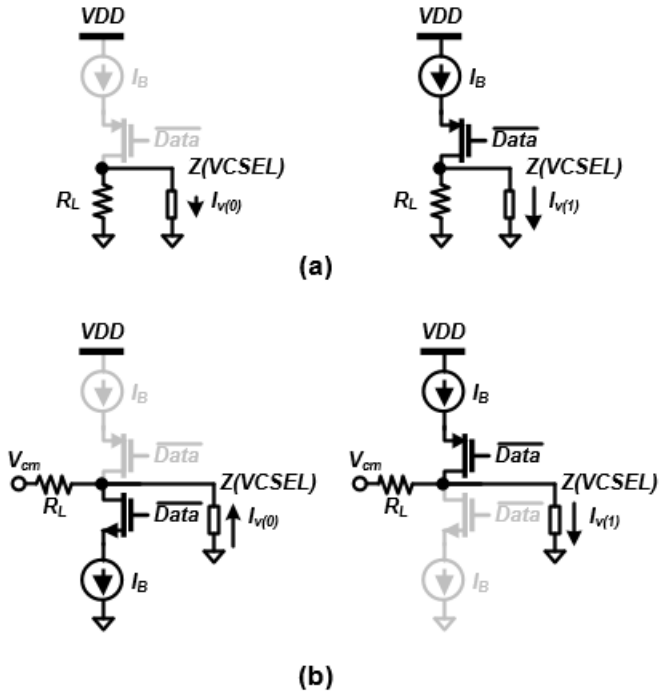


Fig. 3.18 Comparison between (a) pull-down only and (b) push-pull driving schemes.

The overall architecture for the first candidate of the VCSEL driver, AC-coupled push-pull CML driver, is described in Fig. 3.19. The proposed driver transmits data and bias path separately. TMDS data is terminated with 50 Ω to 3.3-V supply voltage, since HDMI sources assume 3.3-V termination. For the proper operating condition of the driver, it employs common-mode feedback for the node cm. All blocks use 3.3-V supply voltage and 1.8-V regulated power by the voltage regulator. Especially, bias currents are 4-bit binary weighted. The AC-coupled driver is wire-bonded to off-chip 1-μF capacitors (0402 size) for the separation

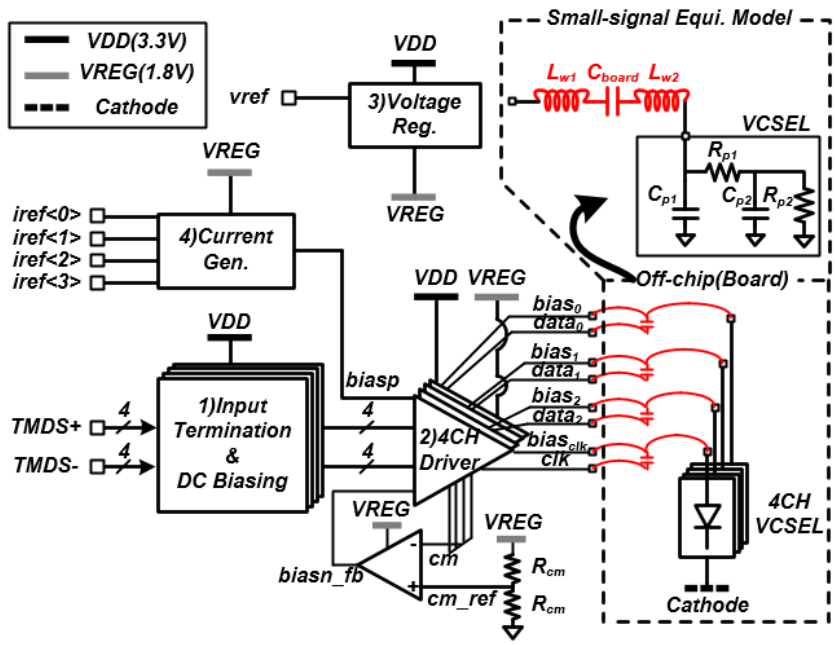


Fig. 3.19 Overall block diagram of AC-coupled push-pull CML driver.

between *biasCH* and *dataCH*.

Fig. 3.20 shows the bias and data path, respectively. DC value of input differential data is set to 1.65V after passing through AC coupling capacitors, CAC. Since it passes both on-chip and off-chip AC coupling capacitors, value of DC biasing resistors, R_B is set to 234 kΩ to pass PRBS7 pattern without loss [3.29]. RM and CM take roles as Miller compensation due to the common-mode feedback loop. The load resistance, R_L, is set to 250 Ω for the good power efficiency while satisfying bandwidth requirement [3.1]. To reduce the channel length modulation effect, 3.3-V nominal V_T transistor is used for Mb6. More details of passive components are described in Table 3.3.

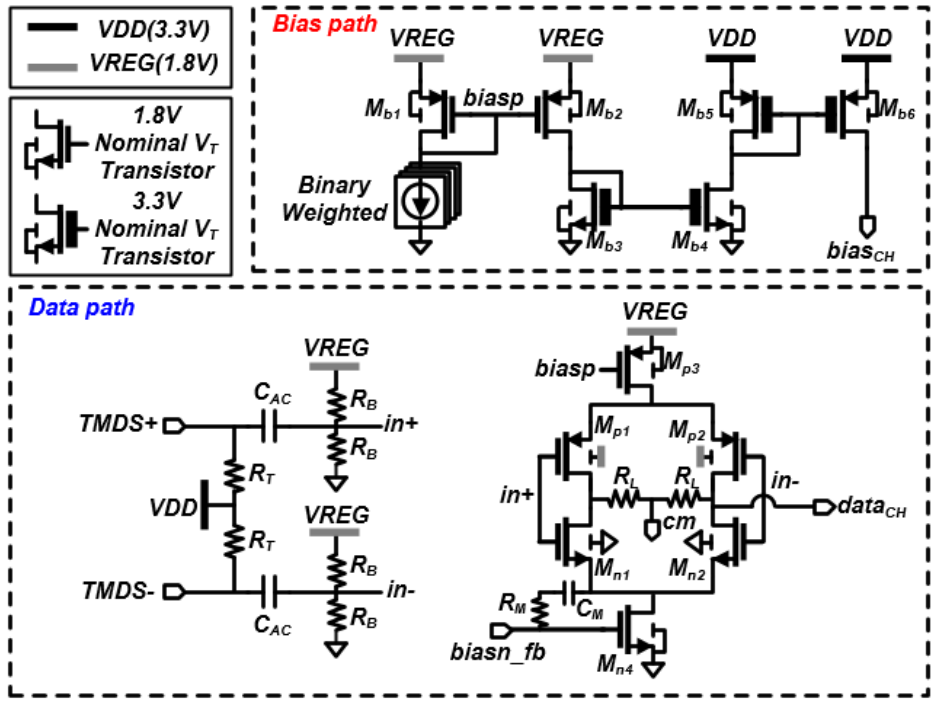


Fig. 3.20 Bias and data path of AC-coupled push-pull CML driver.

Table 3.3 Descriptions of passive components in AC-coupled push-pull driver

	Description	Purpose
R_T	P+ poly w/o silicide 50-Ω resistor	50-Ω termination
R_B	High-resistance poly 234-kΩ resistor	DC biasing
C_{AC}	MIM 1.8-pF capacitor	AC coupling
R_L	P+ poly w/o silicide 250-Ω resistor	Load resistor
C_M	MIM 1.8-pF capacitor	Miller compensation
R_M	P+ poly w/o silicide 10-kΩ resistor	

The other type of the driver, DC-coupled push-pull CML driver, is illustrated in Fig. 3.21. Except the main driver and the board environment, other structures (voltage regulator, current generation block, and input network) are the same as the former type.

Fig. 3.22 shows the bias and data path, respectively. The driver output should be higher than turn-on voltage of the VCSEL, because it is directly wire-bonded to the VCSEL chip. A 3.3-V power is used for the main driver for this reason. However, for the high-speed operation, 1.8-V nominal V_T transistors (M_{n1}~M_{n4} and M_{p1}~M_{p3}) are utilized with the same purpose as the former type of the driver.

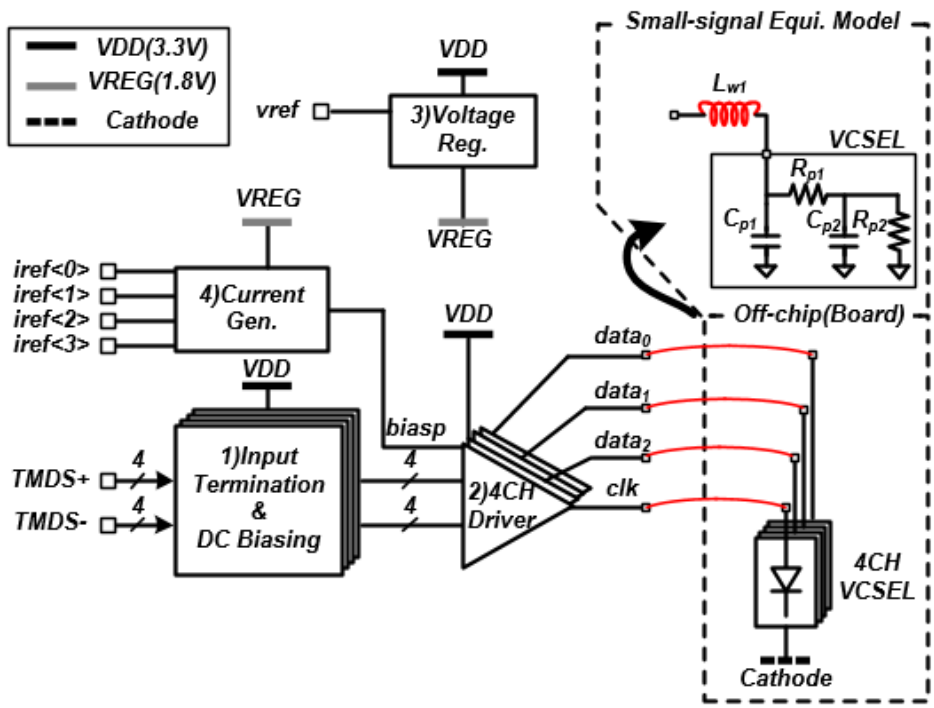


Fig. 3.21 Overall block diagram of DC-coupled push-pull CML driver.

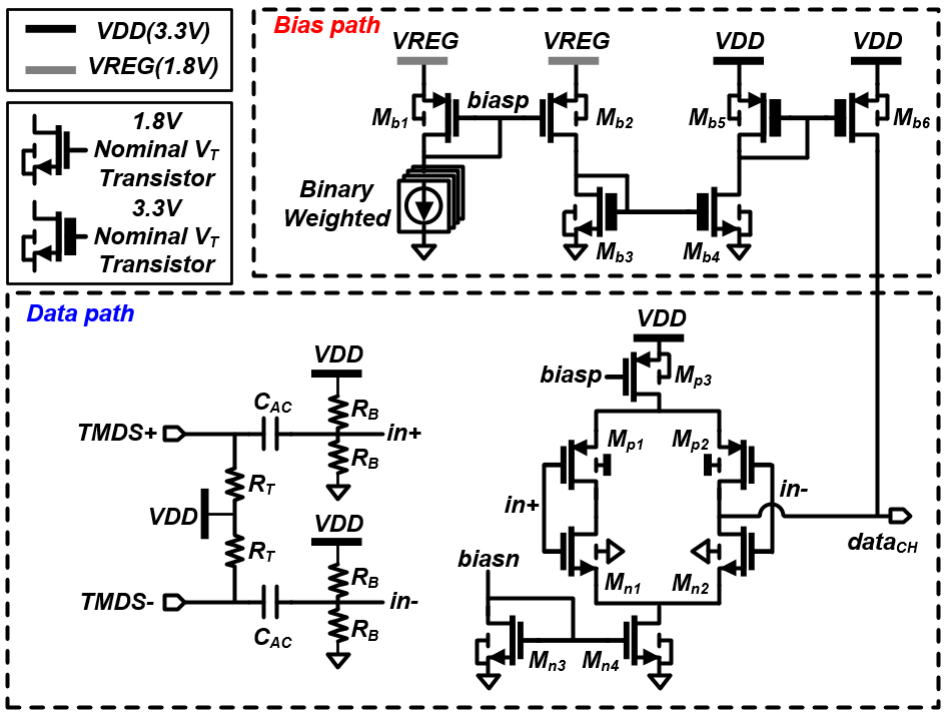


Fig. 3.22 Bias and data path of DC-coupled push-pull CML driver.

Table 3.4 Descriptions of passive components in DC-coupled push-pull driver

	Description	Purpose
R_T	P+ poly w/o silicide 50-Ω resistor	50-Ω termination
R_B	High-resistance poly 4.6-MΩ resistor	DC biasing
C_{AC}	MIM 1.8-pF capacitor	AC coupling

Descriptions and purposes for the other components such as R_T, R_B, and C_{AC} are described in the Table 3.4. Especially, the value of R_B is set to 20 times bigger than

Table 3.5 Comparison between AC-coupled and DC-coupled driver

	AC-Coupled	*DC-Coupled*
AC-Coupling (Input, On-chip)	O	O
DC Separation	O	X
Load Resistor	O	X
CMFB	O	X
AC-Coupling (Output, Off-chip)	O	X
	More parasitics	Less parasitics

that of the former driver even using the same value of C_{AC}. It is because there are no cascaded high-pass filters attached to the VCSEL unlike the former driver. Since the load resistance becomes infinity for this driver, the bandwidth gets reduced. Nevertheless, the swing of becomes higher and reduction of board components improve signal integrity than the AC-coupled driver. Comparison between two types of driver are shown in Table 3.5.

3.4.3 Measurement Results

Two types of driver prototype are both fabricated in 0.18-μm CMOS. They both occupy 1.62 mm^2 (970μm by 1670μm) area. As described in the previous

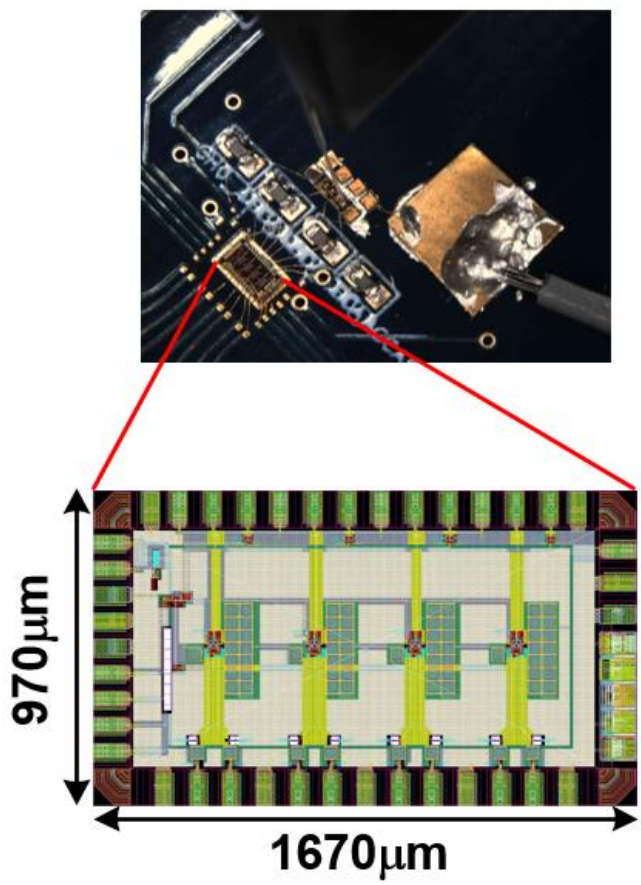


Fig. 3.23. Die photomicrograph: AC-coupled push-pull driver.

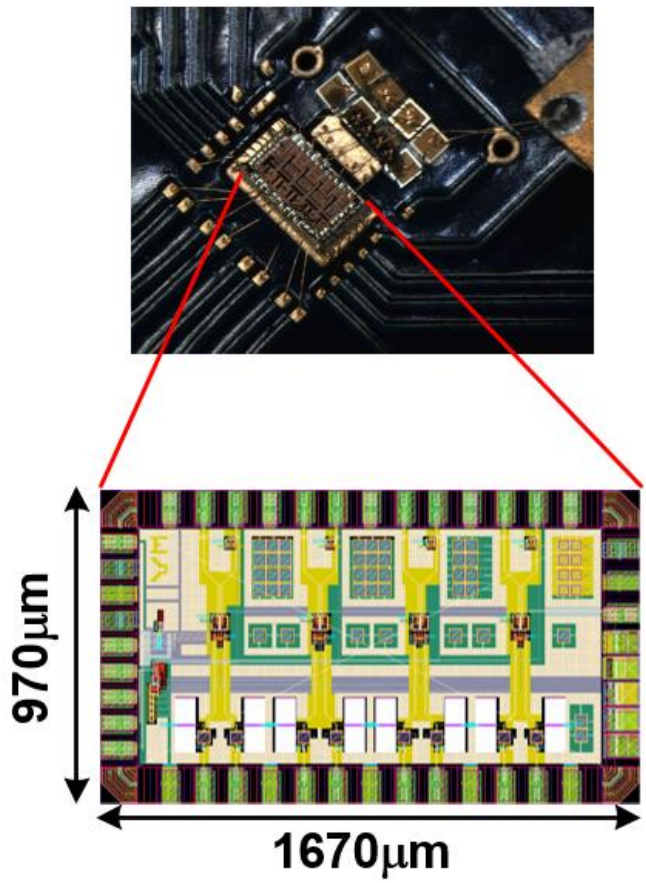


Fig. 3.24. Die photomicrograph: DC-coupled push-pull driver.

Section, they are packaged in different ways. TMDS data, bias pads of the AC-coupled push-pull CML chip, and anode pads of the VCSEL chip are wire-bonded to AC coupling capacitors which are placed on the board as shown in Fig. 3.23. On the other hand, the DC-coupled push-pull CML chip is directly wire-bonded to the VCSEL chip as shown in Fig. 3.24. Especially, cathodes of VCSEL arrays are decoupled to the ground of the driver chip through board capacitors. Both packages have the same

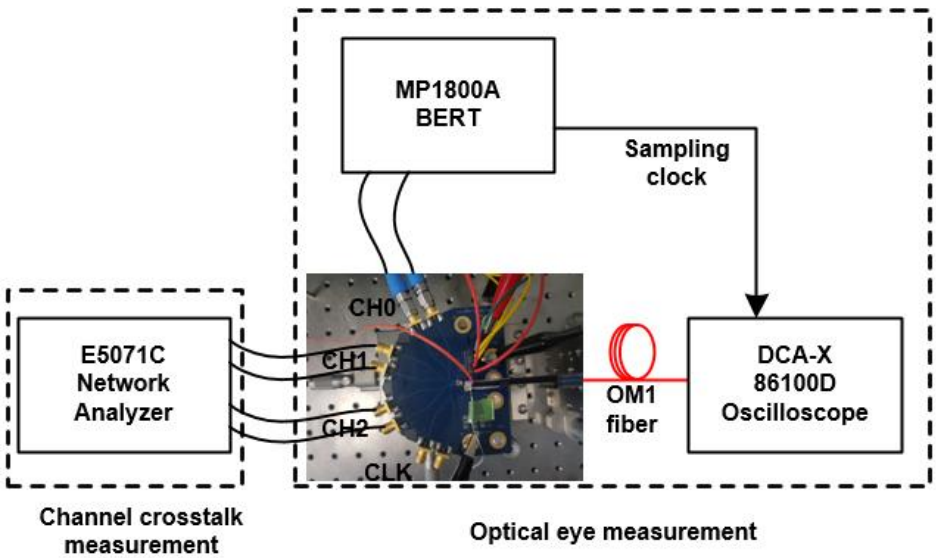


Fig. 3.25. Measurement setup.

optical measurement setup as described in Fig. 3.25. For the multi-channel measurement configuration, return loss and channel crosstalk are measured using E5071C network analyzer. Return loss of each channels and crosstalk between adjacent channels of the both package are shown in Fig. 3.26 and Fig. 3.27. They are all in the acceptable range for the signal integrity.

Based on the packaging, various optical eye diagrams for both types of the driver are shown in Fig. 3.28 and Fig. 3.29, respectively. All eye diagrams are measured with an MP1800A signal quality analyzer and DCA-X 86100D sampling oscilloscope with OM1 multi-mode fibers. PRBS7 data patterns are tested with TMDS data channels (TMDS Channel 0~2) and the clock channel. Especially, the clock channel is additionally verified with 27 MHz clock pattern in case of

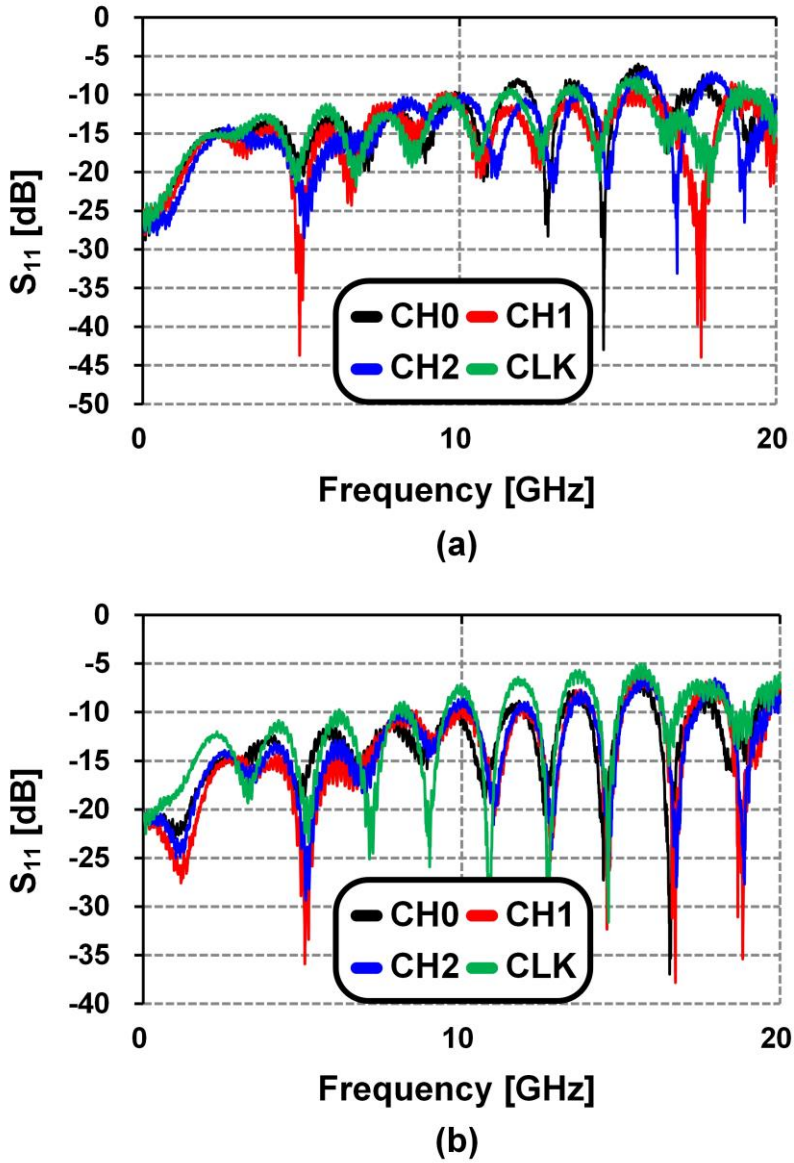


Fig. 3.26. Measured S-parameters of drivers; (a) return loss of AC-coupled driver and (b) return loss of DC-coupled driver.

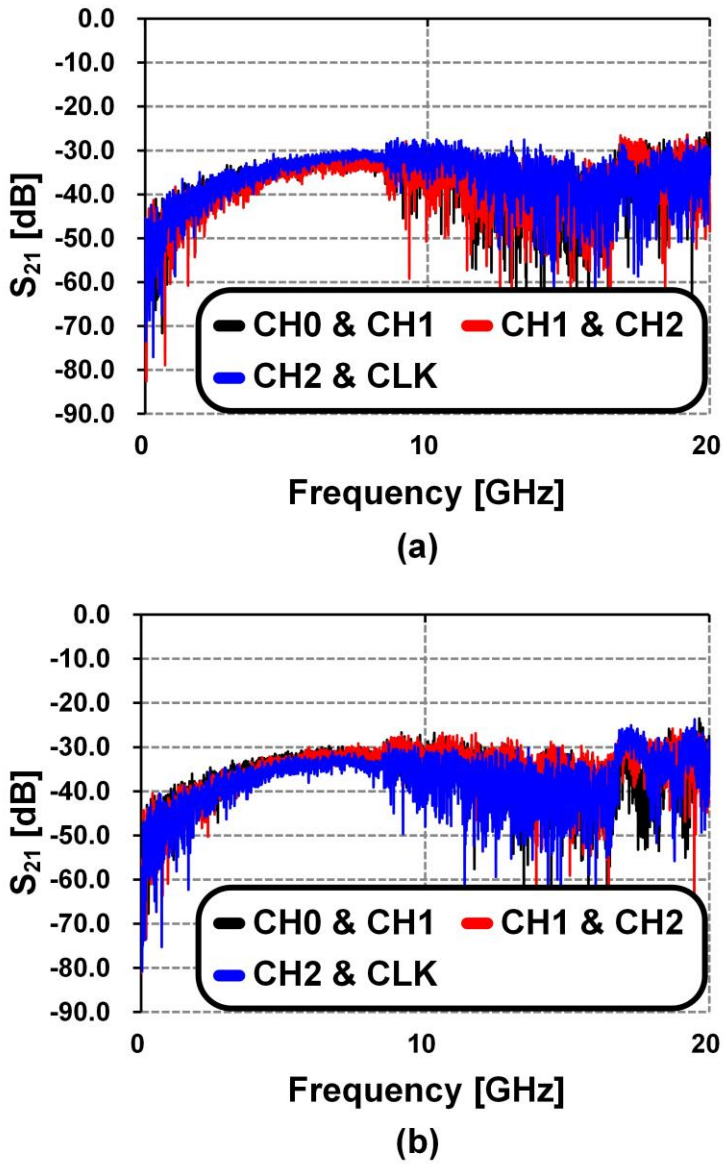


Fig. 3.27 Measured S-parameters of drivers; (a) crosstalk of AC-coupled driver and (b) crosstalk of DC-coupled driver.

operating during the blanking period. The clock pattern is applied by the user-defined data which is then triggered by 6.75-MHz divided clock. Results vary with channels due to the different fiber alignment conditions. Proposed drivers are compared with the recent multi-channel VCSEL drivers in Table 3. It shows that proposed drivers achieve comparable power efficiency with the other recent multi-channel VCSEL-based transmitters.

Table 3.6 Comparison table with multi-channel VCSEL drivers

	ECSI'16 [3.16]	ISCAS'14 [3.30]	OIC'15 [3.31]	This Work	
	0.18-μm BiCMOS	65-nm CMOS	65-nm CMOS	0.18-μm CMOS	
Main topology	Pull-down only	Pull-down only	N/A	Push-pull AC-Coupled CML	Push-pull DC-Coupled CML
Supply voltage [V]	3.3	1.0/3.3	1.2/3.0	3.3	
Data rate [Gb/s]	25.78	25	30	6	12
Power [mW]	*272	*300	*620	146	99
# of channels	4	4	4	4	
OMA [μW]	620	N/A	****N/A	**443	**437
Single-ended ER[dB]	N/A	N/A		**3.31	**5.78
Total area [mm^2]	1.1	***5.82	2.52	1.69	
FoM [mW/Gb/s/CH]	2.64	3.00	5.17	3.65	2.06

*Multiply by 4-channels
**Averaged by 4-channels
***Receivers are included
****Electrically measured

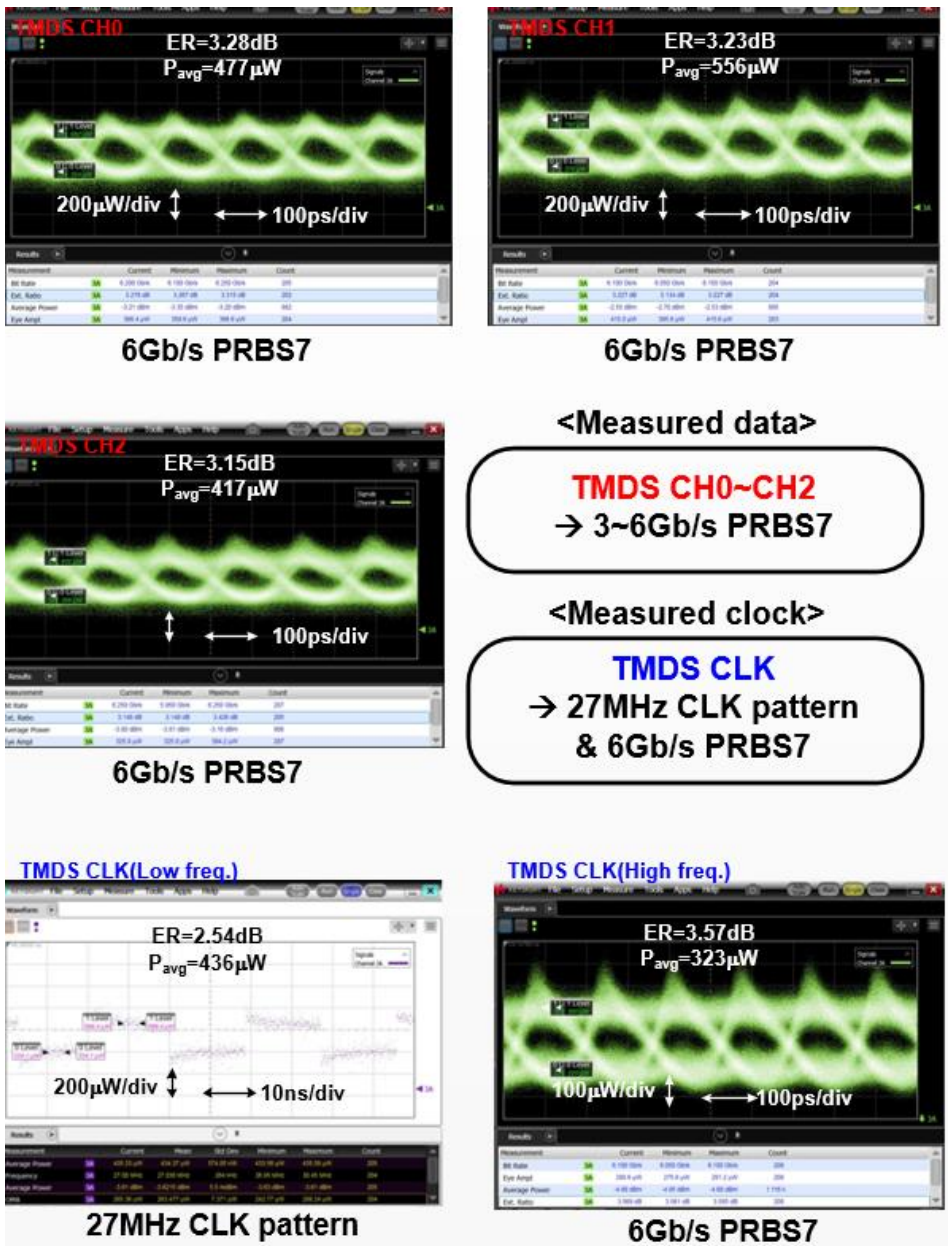


Fig. 3.28. Measured optical eye diagrams of AC-coupled driver.

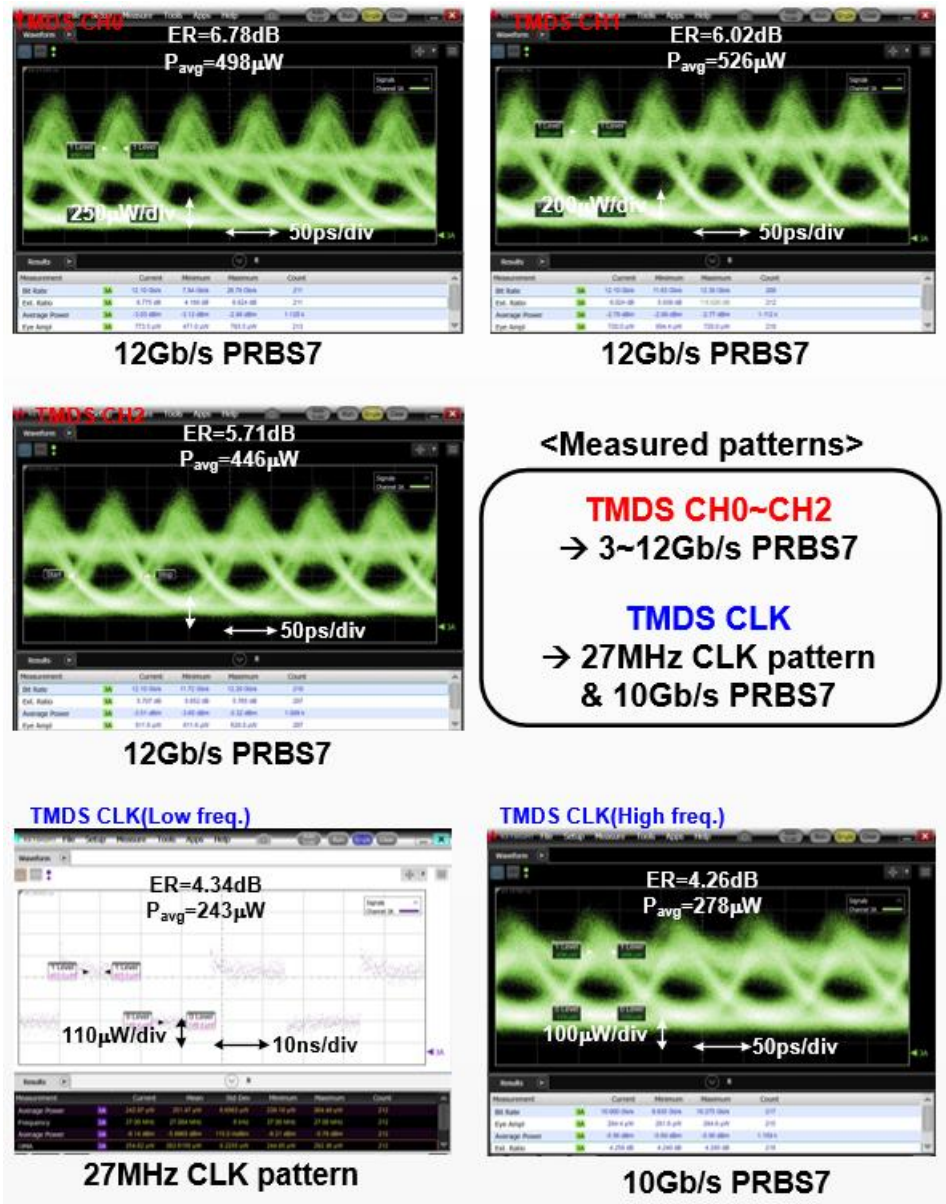


Fig. 3.29 Measured optical eye diagrams of DC-coupled driver.

Chapter 4

High-Speed Clocked Optical Transmitter Implementations With Power-Efficient Techniques

4.1 Overview

Many optical transmitters have been implemented with delay lines to implement FFE. However, it can function only for the limited situation due to the range of delay line and PVT variations [4.1]. Furthermore, required amounts of data go up as mentioned in earlier chapters and recent standard [4.2], not only driver but also whole architecture of the transmitter has to be reconsidered. Especially, the interfaces between electrical application-specific integrated circuit

(ASIC) and optical link have to be taken carefully. Therefore, clocking architecture will be analyzed in this Chapter. Based on the analysis, optical transmitter with forwarded clocking [4.3] and embedded clocking [4.4] are also implemented. Since multi-mode solutions using VCSEL are cheap and area-efficient, VCSEL discussed in Chapter 2 is chosen as the main optical component.

4.2 System Comparison of High-Speed Transmitter

Various clocking architectures (full-rate/half-rate/quarter-rate) can be chosen for the high-speed clocked optical transmitter. A full-rate architecture has difficulties in generating and distributing clocks when it becomes ultra-high-speed transceiver. Also, it is costly with large power consumption and chip area to distribute the full-rate clock [4.5]. On the other hand, a half-rate architecture has less stringent requirement for clock path [4.6]-[4.7]. However, design issues for the final 2:1 mux remain because of the reduced timing margin. The power consumption of the dotted box, which only includes high frequency of the clock domain in Fig. 4.1 can be calculated as

$$Power = \Sigma(2 \times N / 4 \times 2^n \times C_l \times I \times V^2 + 2 \times N / 2 \times 2^n \times C_l \times I \times V^2) + f_{DCC} + f_{DIV2} \quad (4.1).$$

It includes basic clock buffers of half-rate and divided clock. Also, duty-cycle correction (DCC) and divided-by-2 block are included in the calculation.

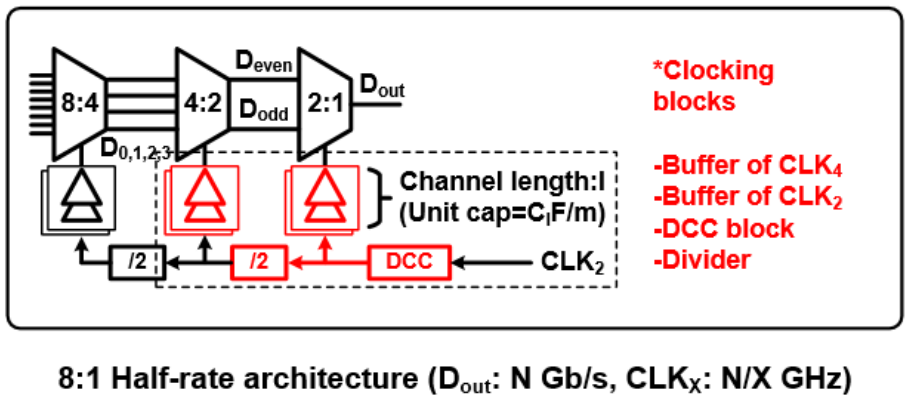


Fig. 4.1. The half-rate architecture of the transmitter.

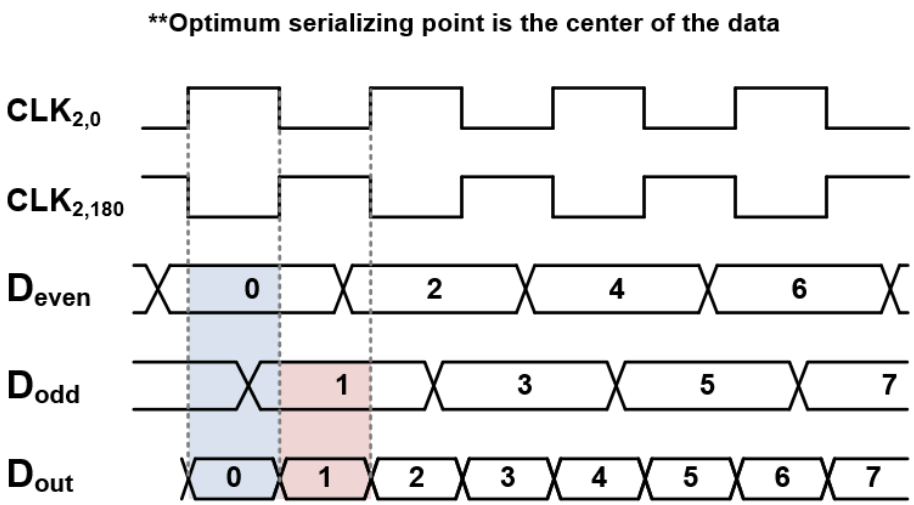


Fig. 4.2. The timing diagram of the half-rate architecture.

The last candidate, a quarter-rate architecture, can be designed with smaller power consumption for clock distribution [4.8]-[4.9]. Nevertheless, it requires additional blocks such as a 4:1 mux and a quadrature clock generator/corrector (QCG/QEC)

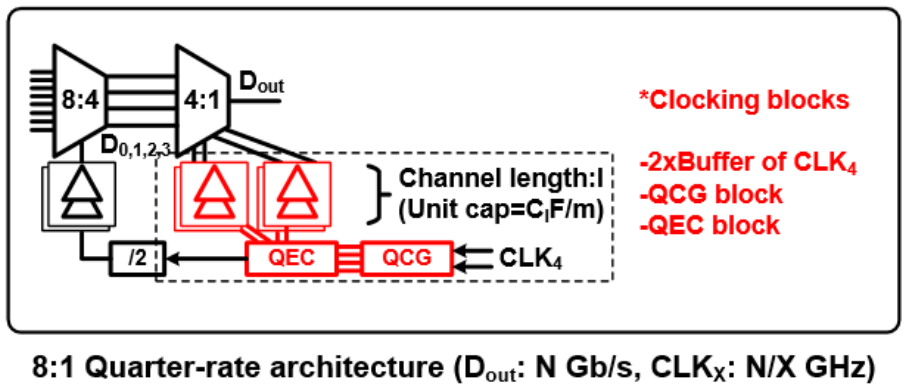


Fig. 4.3. The quarter-rate architecture of the transmitter.

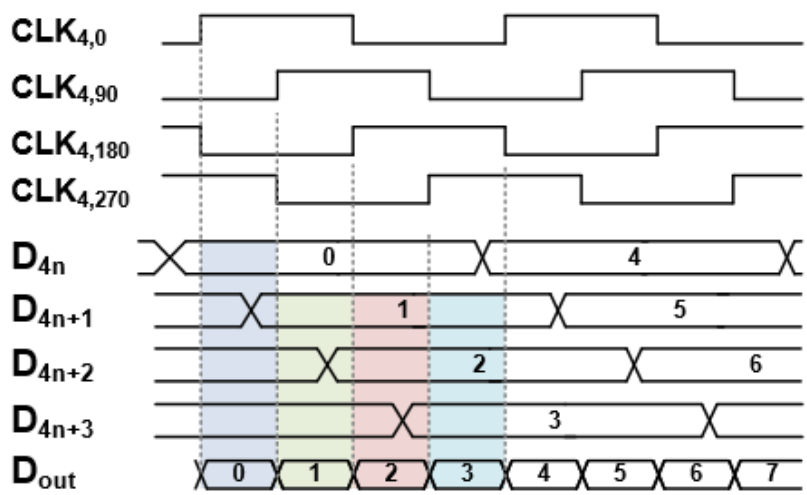


Fig. 4.4. The timing diagram of the quarter-rate architecture.

as illustrated in Fig. 4.3. Despite additional blocks, a quarter-rate architecture consumes less power. It can be calculated as

$$Power = \Sigma(4 \times N / 4 \times 2^n \times C_l \times I \times V^2) + f_{QCG} + f_{QEC} \qquad (4.2).$$

Unlike half-rate clocking architecture, the timing margin is relaxed as shown in equation (4.2). As a result, power issue can be more severe for the half-rate architecture when the data rate goes up or other retiming blocks such as flip-flops are added and the internal wires become longer.

4.3 Proposed Clocked Optical Transmitter

4.3.1 Previous Works

Recently, the requirement of the data throughput in data center interconnections is increasing explosively. The 100Gb/s throughput has been popular for most standards, however, the industry is preparing for the transition to 400Gb/s and higher throughputs [4.2]. One important aspect that enables this transition is the adoption of a PAM signaling format because it provides a much relaxed bandwidth requirement. Specifically, PAM-4 signaling effectively doubles the throughput with the same bandwidth condition. The degraded SNR might affect the BER performance, which can be addressed by introducing a dedicated FEC. On the other hand, MMF-based VCSEL links [4.5], [4.6], [4.10], [4.11] have played an important role in short-reach interconnections because of its cost effectiveness. However, the VCSEL basically suffers from nonlinearity issues, which makes it not suitable for the generation of a PAM-4 signal. Therefore, asymmetric equalization techniques are required to mitigate the nonlinear effects. This Chapter presents a 56Gb/s PAM-4 VCSEL TX with forwarded clocking and a 64Gb/s PAM-4 VCSEL TX with embedded clocking architecture. The quarter-rate architecture is employed for high-speed data transmission owing to its power reduction as discussed in the earlier section. A quadrature clock generator, and a high-bandwidth 4:1 MUX are also integrated in the proposed TX which is implemented in 65nm CMOS

technology.

4.3.2 Proposed Forwarded Clocked Optical Transmitter

Unlike conventional optical modules such as QSFP without any clock channels, a clocked optical module can be introduced as described in Fig. 4.5. With a single-ended or differential pair of forwarded clocks, data from ASIC chip can be serialized easily without additional power consumption for clock generation. As mentioned in the previous section, the quarter-rate forwarded clocking system with a differential pair of clocks is chosen for power efficiency. By receiving a pair of quarter-rate differential clocks (CK4p/n), a pair of divided clocks (CK8p/n) are generated for the 8:4 serializer and quadrature clocks (CK40/90/180/270) for the 4:1 mux. The quadrature clocks are generated and corrected in a similar way as

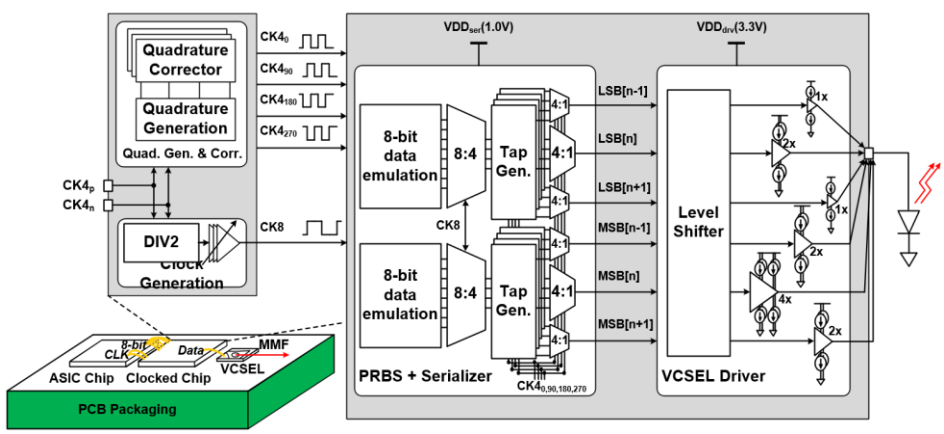


Fig. 4.5. Clocked transmitter with forwarded clocking.

[4.9]. Using the set of quadrature clock, the PRBS7 MSB and LSB pre/main/post taps are multiplexed in a power-efficient way. Since all the retimed taps are combined at the mux, CML is used with shunt-peaking inductors for the bandwidth extension. Each serialized data passes through AC-coupling capacitors and DC-biasing resistors which converts the voltage domain from 1V to 3.3V. The level-shifted driver then drives the anode-driving VCSEL achieving a high swing optical modulation amplitude (OMA) with the use of a push-pull driving scheme. The cathode of the VCSEL is connected to the chip ground. Hence, the VCSEL shares the same ground with the transmitter, simplifying the design of the entire package.

4.3.3 Measurement Results

The NRZ/PAM-4 VCSEL transmitter with forwarded clocking is designed and fabricated in 65nm CMOS occupying an active area of 0.133mm^2. It is wire-bonded to the 850nm multi-mode VCSEL having a -3dB bandwidth of 20GHz. The VCSEL chip is wire-bonded over a very short distance of 300μm length for high-speed operation. In addition, bias and power are supplied via chip capacitors for better power delivery. The value and size of chip capacitors are 15pF and 230μm by 300μm. The chip photomicrograph and chip capacitors are shown in Fig. 4.6. For the measurement, forwarded clock is generated from MP1800A. The optical NRZ/PAM-4 eye diagrams are obtained by a DCA-X 86100D oscilloscope with a

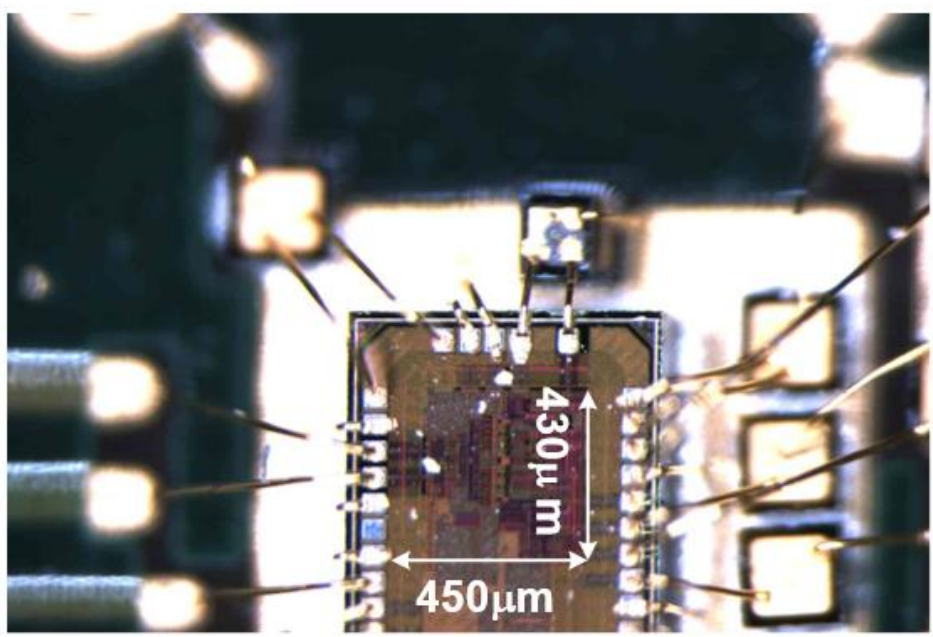


Fig. 4.6. Chip micrograph of forwarded optical transmitter.

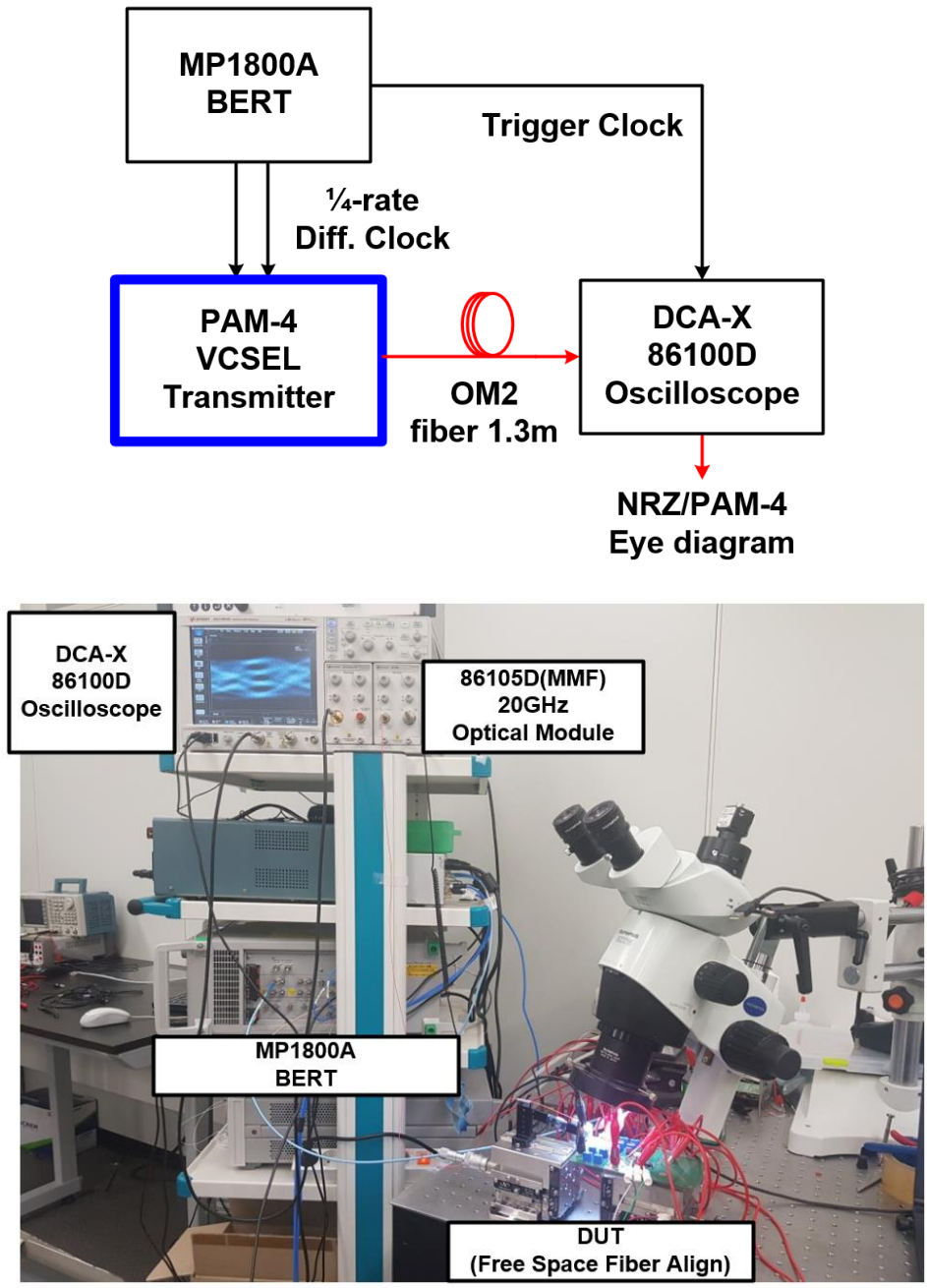


Fig. 4.7. Measurement setup.

PRBS7 pattern which is triggered by an MP1800A BERT. The detailed measurement setup is described in Fig. 4.7.

A fiber is aligned in free space using an OM2 1.3m multi-mode bare fiber without any special alignment such as lens. For the scalability, the bandwidth of the chip is tested from 12.5Gb/s to 40Gb/s for NRZ and 25Gb/s(=12.5GS/s) to 56Gb/s(=28GS/s) for PAM-4 data. Optical eye diagrams are shown in Fig. 4.8 and Fig. 4.9. A large OMA and ER are measured owing to the push-pull driver architecture. Power efficiency for both data formats is also given.

Fig. 4.8. Optical eye diagrams of NRZ data from 12.5Gb/s to 40Gb/s.

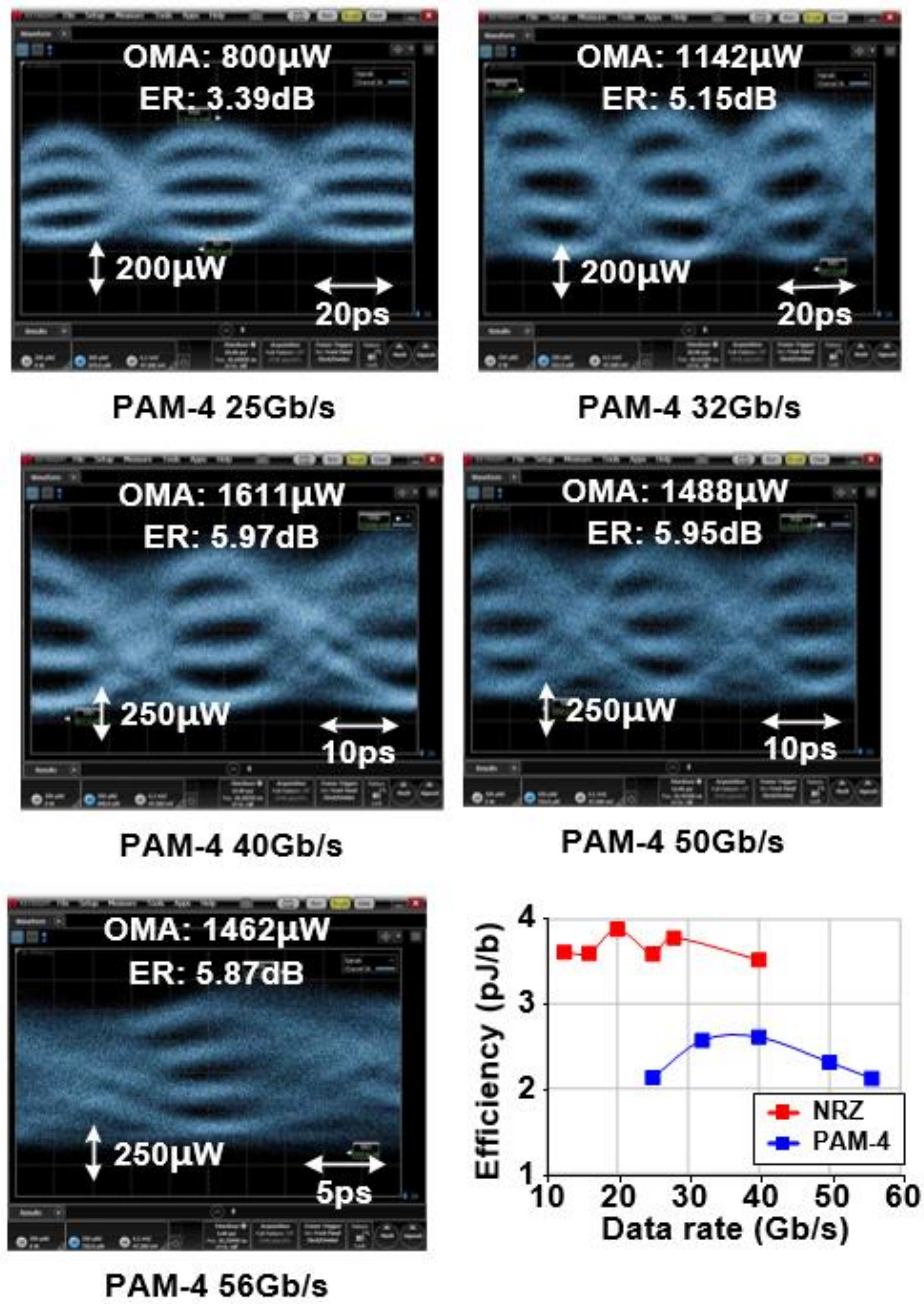


Fig. 4.9. Optical eye diagrams of PAM-4 data from 25Gb/s to 56Gb/s and power efficiency graph.

4.3.4 Proposed Embedded Clocked Transmitter

The overall block diagram is described in Fig. 4.10. A differential pair of the clock, $CK4_P$ and $CK4_N$, is generated by the third-order charge-pump PLL which is based on the LC oscillator. Phase errors of the generated quadrature clocks are then corrected by three consecutive stages of quadrature correctors. The quarter-rate clock ($CK4_0$, $CK4_{90}$, $CK4_{180}$, $CK4_{270}$) and the divided clock, CK8 are then utilized in the data path. A pair of 4Gb/s PRBS7 generators for MSB and LSB forwards the random data sequences to 8:1 serializers to deliver a total of 64Gb/s through both MSB and LSB paths to the VCSEL driver. Asymmetric FFE at the driver compensates for the nonlinear dynamics of the VCSEL.

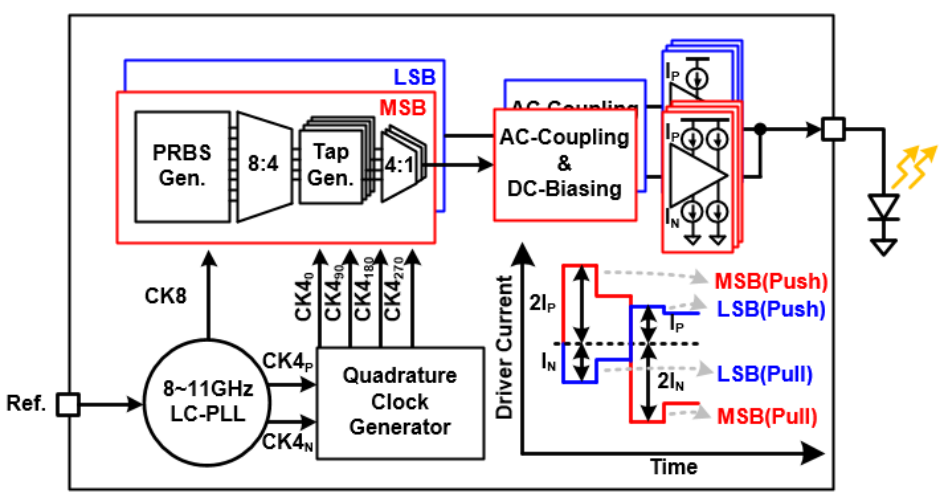


Fig. 4.10. Overall block diagram of embedded clocked transmitter.

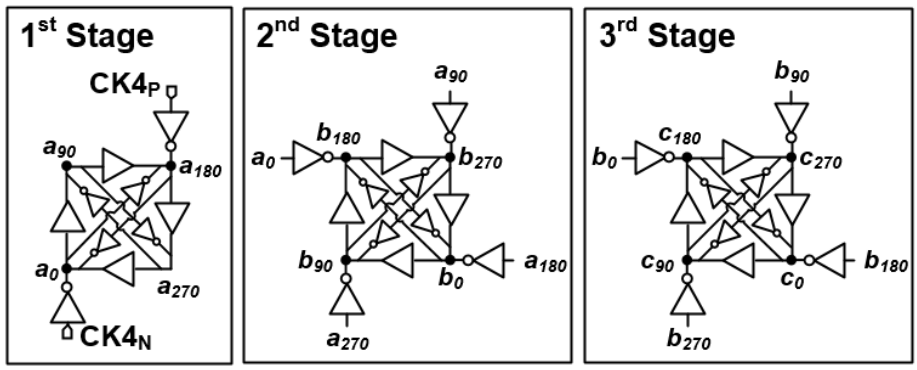


Fig. 4.11. Schematics of quadrature clock generator (1st stage) and quadrature corrector (2nd and 3rd stage).

The main blocks and functions of the clock path for the quarter-rate architecture are detailed in Fig. 4.11 and Fig. 4.12. A pair of differential clocks ($CK4_P$, $CK4_N$) is injected to the ring-based quadrature clock generator. Generated quadrature clocks are then corrected by three consecutive stages of inverter-based quadrature correctors. As a result, the quadrature clocks ($CK4_0$, $CK49_0$, $CK4_{180}$, $CK4_{270}$) are sufficiently corrected at the last stage in the frequency range from 5GHz to 10GHz. $\pm 3\sigma$ variation of the last stage is 1.86ps with 8GHz clock injection which is verified by Monte-Carlo simulation as shown in Fig. 4.13. Furthermore, for the process mismatch compensation, the inverters in the last stage are designed with current starved structure which can be finely adjusted by PMOS and NMOS current sources. The quadrature skew between $CK4_0$ and $CK4_{90}$ can be controlled up to 2.5ps at the last stage as shown in Fig. 4.14.

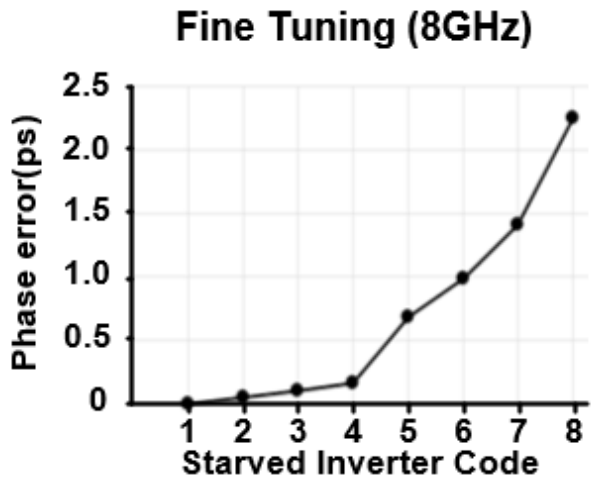


Fig. 4.14. Simulation results of tunability of the last stage at 8GHz clock.

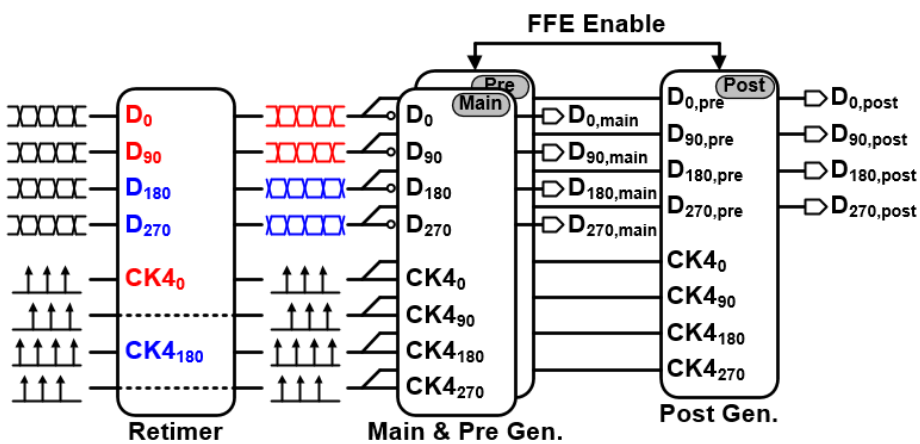


Fig. 4.15. Retimer blocks for the quarter-rate system.

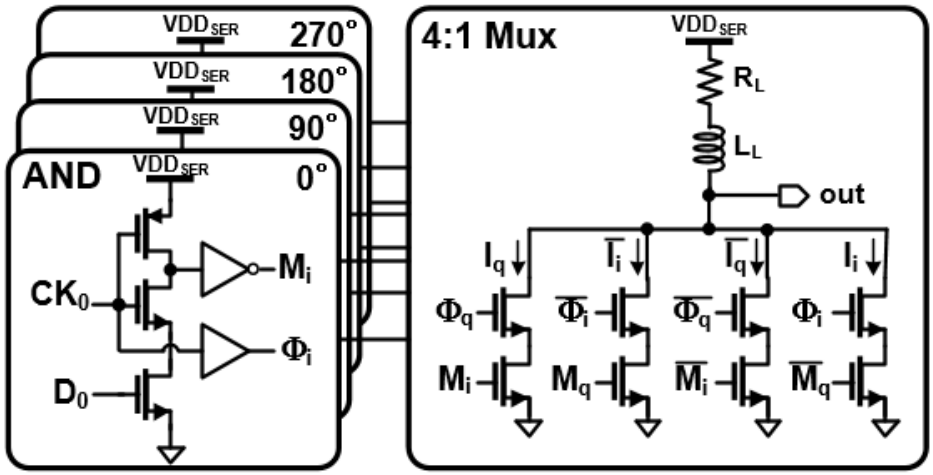


Fig. 4.16. Schematics of 4:1 MUX.

Using the generated quadrature clocks, the 4:1 MUX is optimized with overlap between clock and retimed data from Fig. 4.16. Detailed schematics are shown in Fig. 4.16. Instead of generating 1UI data pulse at the previous stage of 4:1 MUX, overlapping scheme generates data with 2UI pulse width (M_i). Since the high-frequency signals (I_0, I_{90}, I_{180}, I_{270}) are combined, single-ended CML is used with shunt-peaking inductors and load resistors are used instead of using PMOS for increased bandwidth unlike other 4:1 MUXs as illustrated in Fig. 4.17.

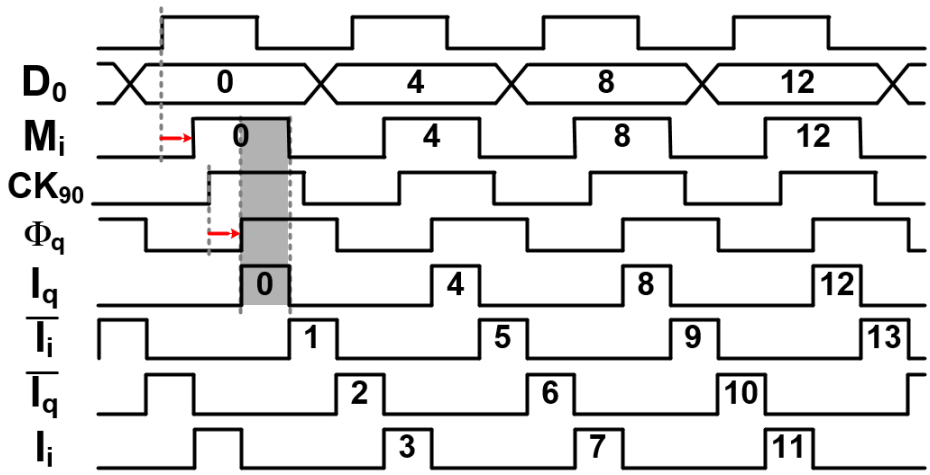


Fig. 4.17. Operating principle of 4:1 MUX.

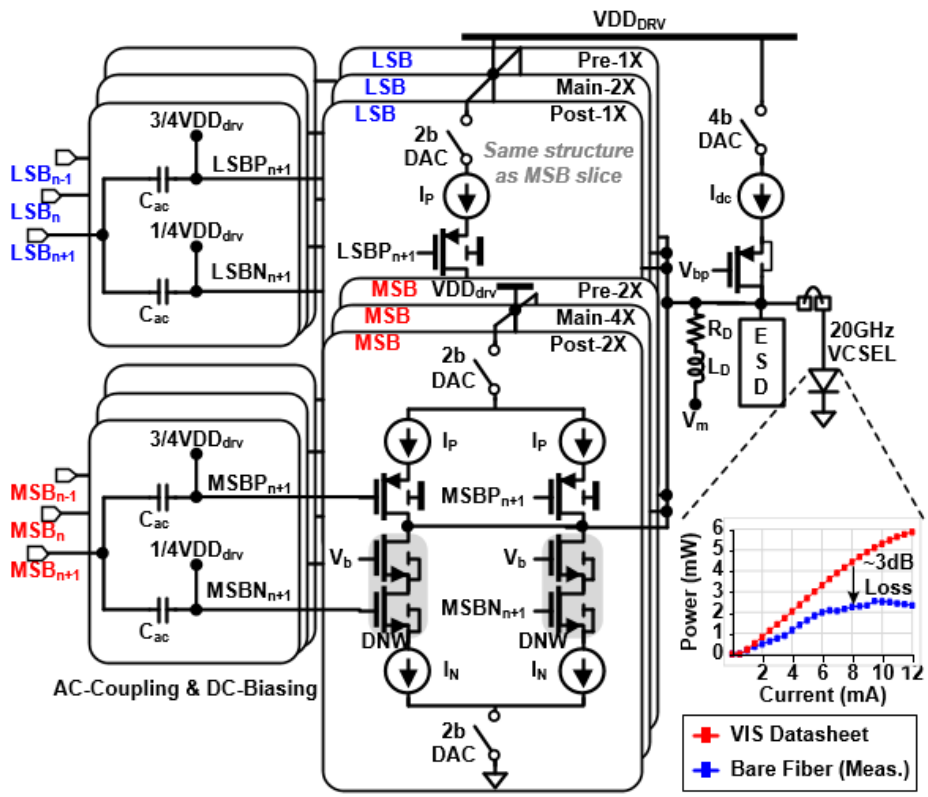


Fig. 4.18. Schematics of VCSEL driver.

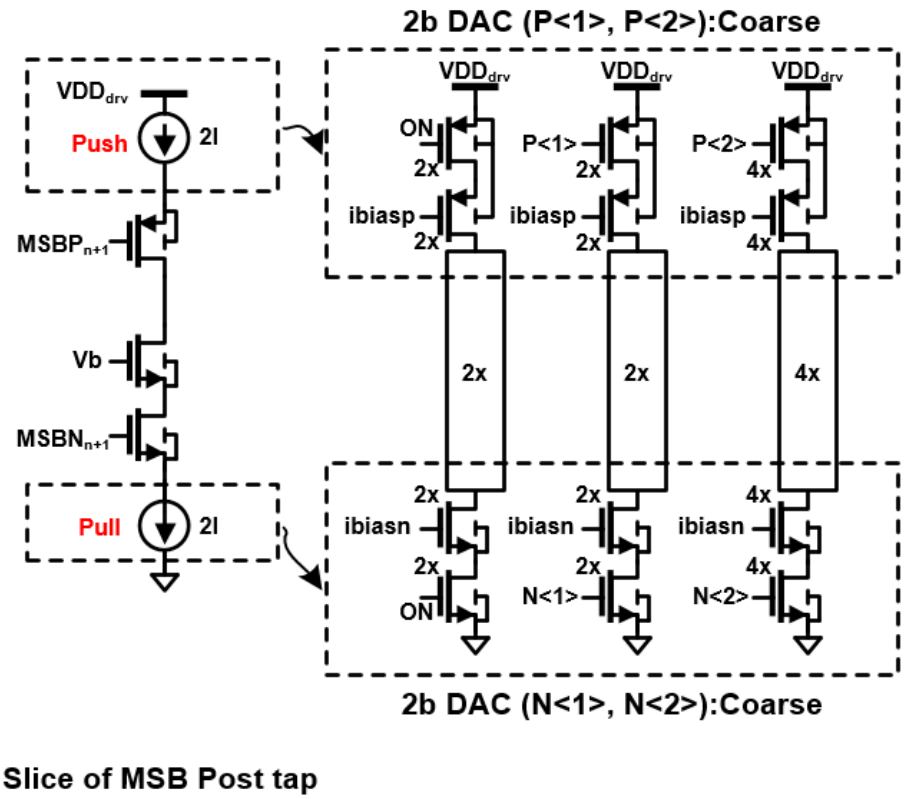


Fig. 4.19. Bias switches of the VCSEL driver: post tap for the MSB slice.

The voltage headroom for the driver is chosen from 0V (GND) to 3.3V (VDD_{DRV}) because typical common-cathode VCSELs barely turn on above 1.8V. Serializer outputs from pre/main/post taps for the MSB and LSB are passed through AC-coupling capacitors and DC-biasing network, and converted from the VDD_{SER} domain to the VDD_{DRV} domain as shown in Fig. 4.18. To minimize the voltage stress, DC bias points of the PMOS and NMOS of the driver are fixed to $3/4VDD_{DRV}$ and $1/4VDD_{DRV}$, respectively. Pre/main/post taps of push(PMOS)/pull(NMOS) can be independently controlled by 2b DAC for

asymmetric pre-emphasis as shown in Fig. 4.19. As a result of push/pull driving scheme, the driver voltage swing is increased and SNR degradation of PAM-4 modulation is reduced. In order to support various VCSEL bias conditions, this work employs 4b current DAC to adjust I_{dc} properly. Possible voltage stress due to large voltage headroom is relaxed by stacked deep n-well NMOS transistors with the gate voltage of V_b and PMOS transistor biased with V_{bp}. A shunt-peaking inductor (L_D) and a load resistor (R_D) parallel to the VCSEL are utilized to improve limited bandwidth due to having various parasitics at the output node such as FFE slices of drivers, taps of I_{dc}, an ESD protection diode, and the VCSEL. In addition, V_m is set to 2.5V for the proper operating condition of the VCSEL.

4.3.5 Measurement Results

The chip microphotograph including VCSEL chip is illustrated in Fig. 4.20.

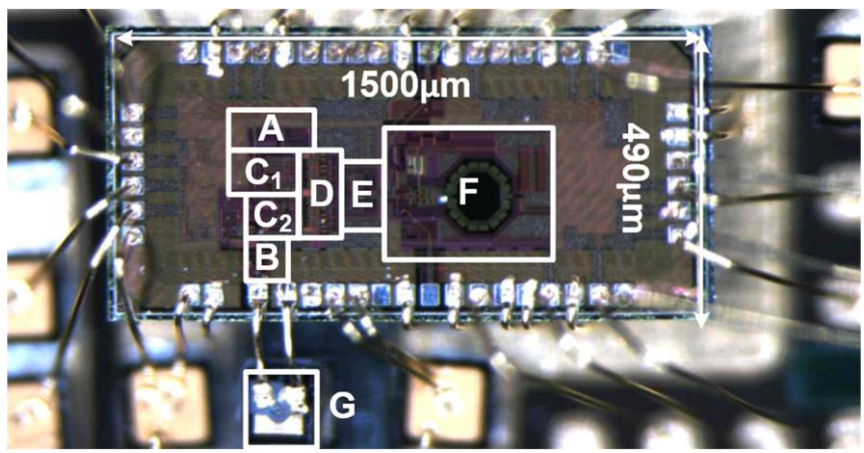
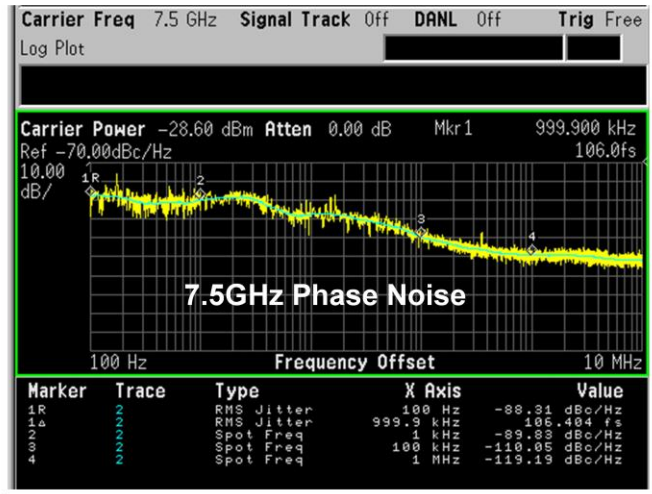


Fig. 4.20. Chip micrograph of embedded clocked optical transmitter.

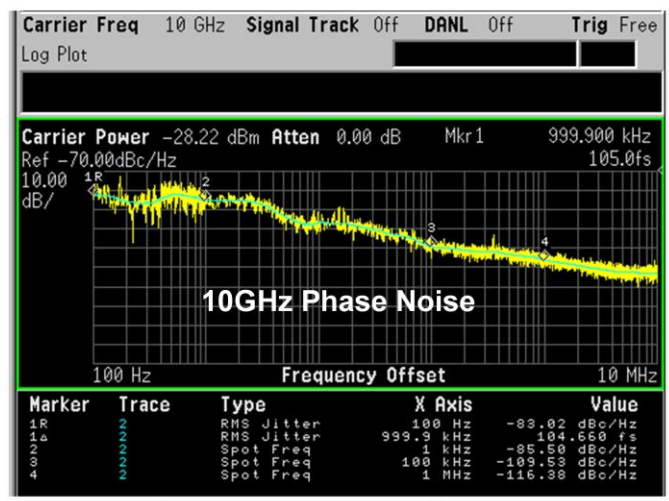
Table 4.1 Area and power breakdown of core blocks

	Block Description	Area (mm^2)	Supply (V)	Power Breakdown (mW)
A	Bias of Main Driver	0.013	3.3	40.7(NRZ 40Gb/s) 56.1(PAM-4 64Gb/s)
B	VCSEL Bias and Inductor	0.009		
C(C_1+C_2)	MSB slice LSB slice	0.02		
D	4:1 Mux	0.035	1.0	71.7(NRZ 40Gb/s) 64.9(PAM-4 64Gb/s)
E	8:4 Serializer Quad gen.	0.016		
F	PLL	0.165	1.0	26.2(NRZ 40Gb/s) 26.0(PAM-4 64Gb/s)
G	850nm VCSEL	0.04	-	Included in Driver

The proposed VCSEL TX is fabricated in 65nm CMOS. It is assembled with 850nm VCSEL module using wire-bonding method. The fabricated chip occupies 0.184mm^2 for PLL and 0.094mm^2 for driver and serializer, respectively. Detailed area and power breakdown of core blocks are shown in Table 4.1. The integrated RMS jitter from 100Hz to 1MHz of PLL is measured as 104.6fs for the 10GHz clock output as measured in Fig. 4.21.



	RMS Jitter (fs) (100Hz~1MHz)	Phase Noise (dBc/Hz)
PLL Metrics	106.4@7.5GHz	-119.2@1MHz



	RMS Jitter (fs) (100Hz~1MHz)	Phase Noise (dBc/Hz)
PLL Metrics	104.6@10GHz	-116.4@1MHz

Fig. 4.21. Measurement of phase noise with 7.5GHz and 10GHz PLL output.

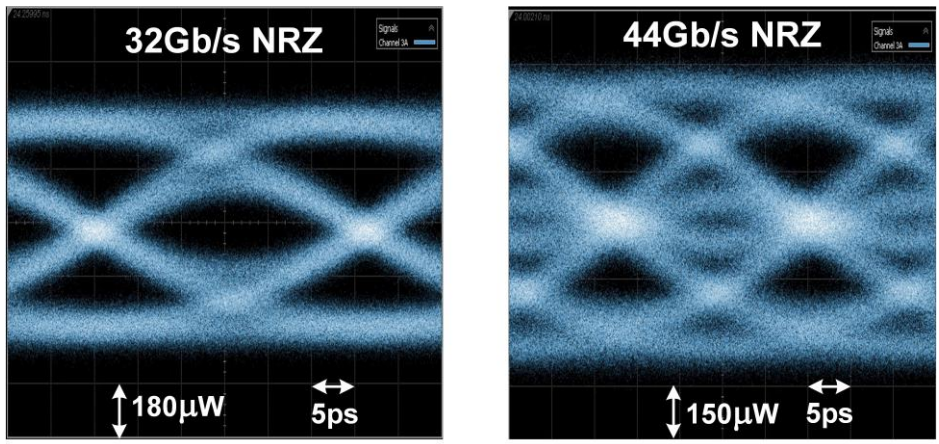
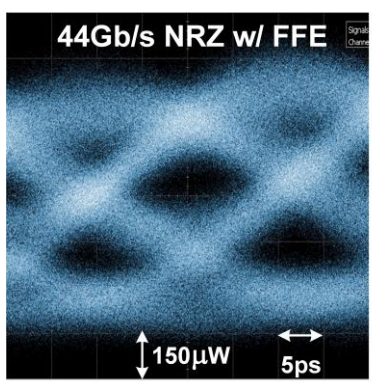


Fig. 4.22. Measurement results of bare VCSEL.



	Tap Coefficients [Pre/Main/Post]	Amplitude Power
44Gb/s NRZ	Push (PMOS) [2,16,4] Pull (NMOS) [0,16,0]	OMA:0.33dBm (=1.08mW) Power (w/PLL): 160.9mW

Fig. 4.23. Measurement results of NRZ optical eye diagrams using FFE at 44Gb/s.

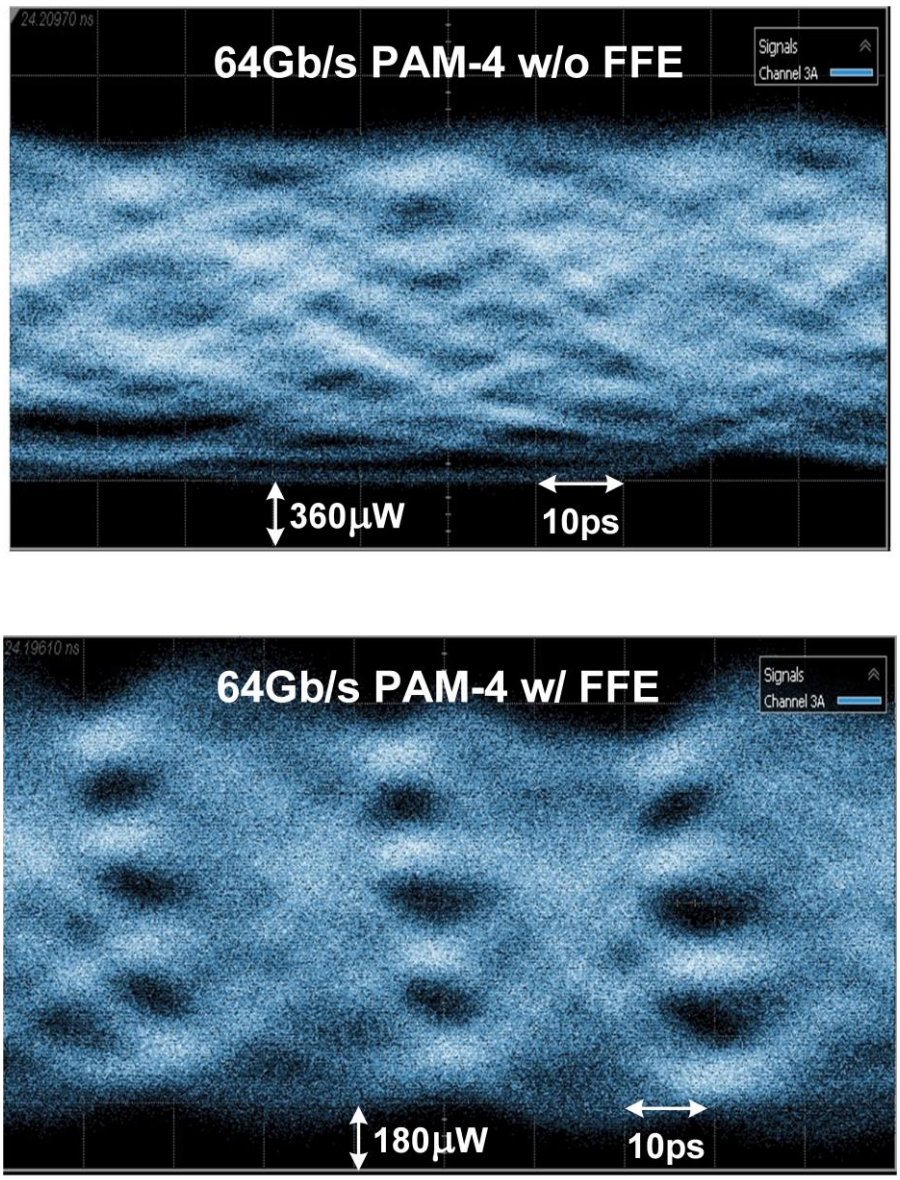


Fig. 4.24. Measurement results of PAM-4 optical eye diagrams without FFE and with FFE at 64Gb/s.

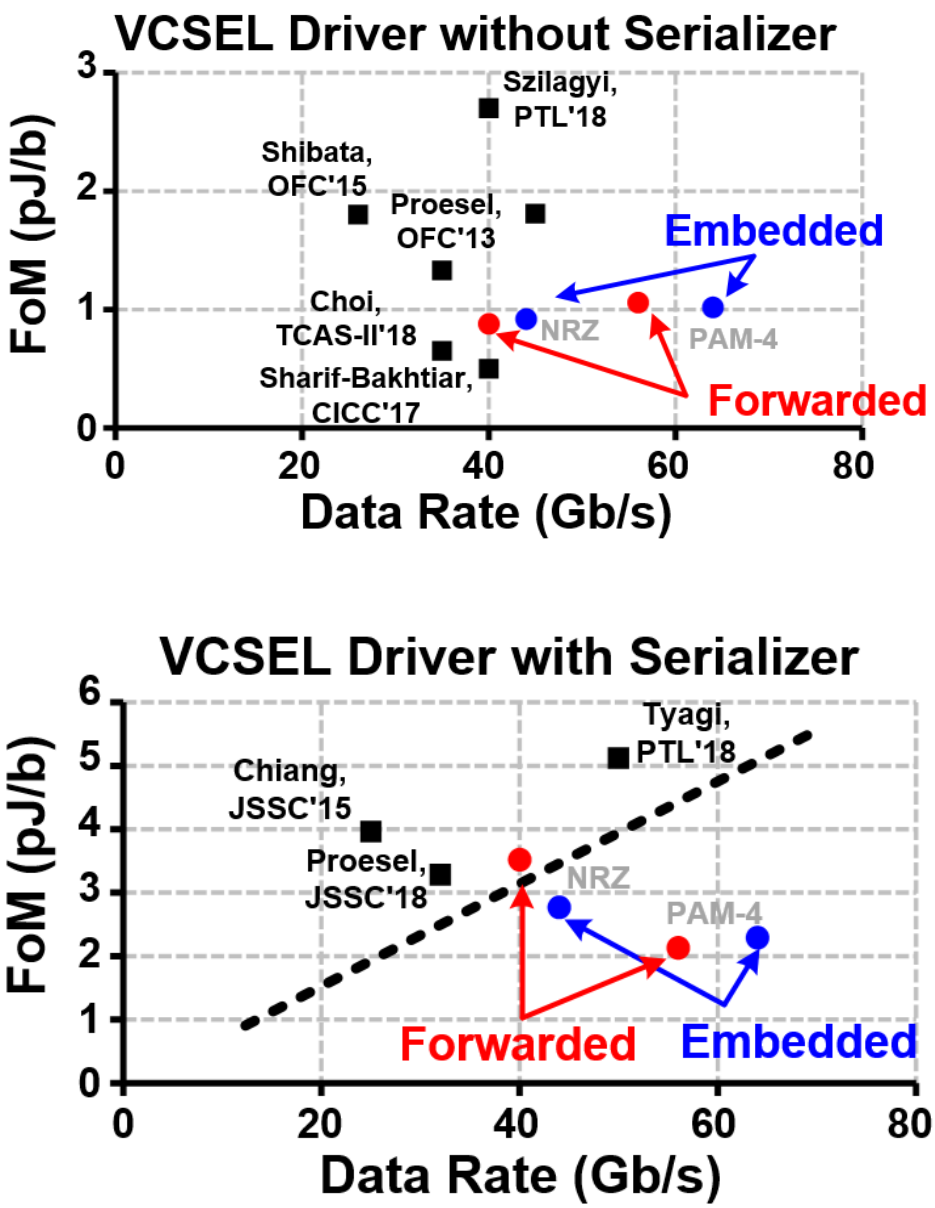


Fig. 4.25. Comparison graphs.

Since VCSEL with wire-bonding has limited bandwidth of 20GHz, optical eye diagram is closed with 44Gb/s BERT PRBS7 signal as shown in Fig. 4.22. On the other hand, equalized optical eye diagrams of the VCSEL TX are shown in Fig. 4.23 with NRZ and Fig. 4.24 with PAM-4, respectively. Optical modulation amplitude (OMA) is estimated by de-embedding 3dB coupling loss due to bare fiber alignment as shown in Fig. 4.18 and the previous works [4.1], [4.11]. For the 44Gb/s NRZ optical eye diagram, the [pre, main, post] tap coefficients of push/pull are [2/0, 16/16, 4/0]. It achieves the de-embedded OMA of 3.33dBm and extinction ratio (ER) of 3.27dB. The FFE tap coefficients for 64Gb/s PAM-4 optical eye diagram are [2/0, 16/16, 6/0], [1/0, 8/8, 3/1] for MSB and LSB, respectively. The de-embedded OMA is 3.98dBm and ER is 3.21dB, respectively.

Comparison with recently published CMOS VCSEL TXs is presented in Fig. 4.25 and Table 4.2. The TX achieves 64Gb/s PAM-4 and exhibits with 2.29pJ/b and 1.02pJ/b power efficiency with and without serializer, respectively. The 64Gb/s CMOS PAM-4 VCSEL TX, integrated with PLL and serializer, offers the highest data rate, the best FoM1 (pJ/b) and FoM2 (FoM1/OMA).

Table 4.2 Performance comparison with state-of-the-art works

	CICC'17 [4.10]	PTL'18 [4.6]	JSSC'18 [4.1]	JSSC'18[5]	Forwarded Clocking[4.3]		Embedded Clocking[4.4]	
CMOS Tech.	28nm	65nm	14nm	14nm	65nm		65nm	
Serializer	X	Half-rate	Half-rate	X	Quarter-rate		Quarter-rate	
PLL Type	X	X	X	X	X		LC-PLL	
Data Rate (Gb/s)	40	50	32	45	40	56	44	64
Data Format	NRZ	PAM-4	NRZ	NRZ	NRZ	PAM-4	NRZ	PAM-4
Supply (V)	1.0/-1.1	1.2/3.0	1.0/1.2/3.22	1.0/1.7/-2.0	1.0/3.3		1.0/3.3	
Fiber Alignment	With lense	With lense	With lense	With lense	Bare Fiber		Bare Fiber	
OMA (dBm)	1.3	3	1.23	1.4	2.63*	4.65*	3.33*	3.98*
VCSEL BW (GHz)	19	11	15	20	20		20	
FoM$_1$ (pJ/b) w/PLL	X	X	X	X	X	X	3.65	2.69
FoM$_1$ (pJ/b) Ser.+Drv.	X	5.12	3.28	X	3.52	2.12	2.77	2.29
FoM$_1$ (pJ/b) Driver	0.5	N/A	0.94	1.81	1.08	0.94	0.92	1.02
FoM$_2$* (pJ/b/mW)**	0.37	N/A	0.71	1.31	0.59*	0.32*	0.37*	0.41*
Area (Overall) (mm^2)	0.033	0.2	0.049	0.088	0.133 (0.094**)		0.278 (0.094**)	

* De-embeded with 3dB fiber coupling loss
** Area (Serializer+Driver) (mm^2)
*** Only for driver

Chapter 5

Conclusions

In this thesis, high-speed and power-efficient techniques of optical transmitter are discussed. To design high performance optical transmitter, the background of the general optical link is first discussed at Chapter 2. Basics of optical link and data center, which is the main applications in optical link, are discussed. The major optical components of optical transmitter are also explained.

With the background of the optical link, high-speed and power-efficient technique, push-pull CML driving scheme is discussed in the Chapter 3. With this driving scheme, high-speed optical drivers are implemented. First, 32Gb/s MZM/EAM modulator driver fabricated in 65nm CMOS process, achieving large swing, is implemented. Even though it has large output swing, it achieves 6.28pJ/b at 32Gb/s thanks to power-efficient push-pull CML driving scheme. Second, two types of HDMI AOC transmitter using VCSEL are designed in 180nm CMOS process. As a result, 6Gb/s AC-coupled driver and 12Gb/s DC-coupled driver could be implemented, respectively. Due to parasitics of off-chip AC coupling capacitor on the board, DC-coupled driver has better performance than the former.

For more advanced system and standard, drivers with clocked system are implemented in the Chapter 4. Since the architecture decides power consumption

of the whole system, architectures are analyzed in the earlier part of Chapter 4. After selection of quarter-rate architecture, forwarded and embedded clocked optical transmitter with VCSEL are implemented in 65nm CMOS process. With power-efficient and high-speed techniques of core blocks, 56Gb/s PAM-4 and 64Gb/s PAM-4 optical eye diagrams can be achieved, respectively.

In the near future, single-mode fibers will be more applied to the systems owing to its higher spectral efficiency than multi-mode fibers. However, many VCSELs with single-mode and other wavelengths have been developed which makes VCSEL one of the promising solutions for optical transmitter.

Appendix A

Verilog-A Model of VCSEL

A few approaches have been made to model equivalent components of the VCSEL [A.1], [A.2]. Among these approaches, a 50-Ω resistor (or a 100-Ω resistor in differential way) is the popular model for the VCSEL [A.1], [A.2]. However, VCSEL has nonlinear impedance, hence, it cannot be modeled the same as a 50-Ω resistor. Other famous approach is using rate-equations of the VCSEL [A.3]. However, rate-equations require large sets of parameters related to physical dimensions and quantities which are difficult to obtain for customers.

To deal with these points, this thesis utilizes the raw datasheet of the commercial VCSEL that includes its own features. Raw datasheets should include voltage-current (V-I, “vis_v2i.tbl”) and current-light (I-L,”vis_i2l.tbl”) information. It proposes using Verilog-A with HSPICE to fit the raw data. It can be shown that when fitting the raw datasheet, Verilog-A model is not the same as a 50-Ω resistor (or a 100-Ω resistor in differential way) due to its nonlinearity. The specific code is written in Fig. A.1

```
`include "disciplines.vams"
`include "constants.vams"

module vcsel_850 (a, c, l);

electrical a, c, l;
inout a, c;
output l;

analog begin
        I(a, c) <+ $table_model (V(a,c), "./vis_v2i.tbl","L");
        V(l)    <+ $table_model (I(a,c), "./vis_i2l.tbl","L");
        //to quantify output optical power
        end
endmodule
```

Fig. A.1. Simple Verilog-A model of VCSEL based on table

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초록

다가오는 IoT와 5G 무선망으로 인해 해마다 데이터의 사용량은 급격히 증가하고 있다. 요구되는 데이터의 양이 계속 증가되는 가운데, 유선 망에서는 한정된 자원으로 에러 없이 혹은 적은 에러로 전송을 해야 한다. 하지만, 기존의 유선 네트워크로는 고속 주파수에서의 표피효과와 유전체의 손실로 인해 구리 선에서 데이터를 처리하는 것은 쉽지 않다. 따라서, 장거리를 손실 없이 고속의 데이터를 보낼 수 있는 광섬유를 활용의 중요함은 커지고 있다.

이러한 흐름을 따르며, 본 논문에서는 광통신의 송신부에 초점을 맞추었다. 고속 저전력에 적합한 푸쉬-풀 구동 기술이 제안되고 사용되었다. 해당 기술을 기반으로 큰 스윙을 가지며 6.28pJ/b의 효율성을 가진 32Gb/s 마크-젠더 광 변조기/전계-흡수 광 변조기가 65나노 CMOS 공정으로 설계되었다. 해당 칩은 0.086mm^{2}의 작용면적을 지니고 있다. 또한, 채널당 12Gb/s의 속도를 지닌 4-채널 HDMI AOC 드라이버 역시 180나노 공정을 이용하여 설계하였다. 마찬가지로 푸쉬-풀 구동 기술을 사용했으며 총 면적은 1.62mm^{2}였다.

후속 섹션에서는 클락을 가진 광 송신기가 제안되었다. 값싸고 집적도가 높은 면발광 레이져가 본 섹션에서 이용되었다. 클락 전송형,

클락 내장형 송신기가 차세대 광통신을 위해 적용되었다. 그 결과 56Gb/s 4-레벨 진폭변조가 가능한 면발광 레이저를 구동하는 클락 전송형 광 송신기와 64Gb/s 4-레벨 진폭변조가 가능한 면발광 레이저를 구동하는 클락 내장형 광 송신기가 설계되었다. 전력효율성은 각각 2.12pJ/b와 2.69pJ/b 이며 0.133mm^{2}와 0.278mm^{2}의 작용면적을 갖고 있다.

주요어 : 푸쉬-풀 구동기, 마크-젠더 광 변조기 (MZM), 전계-흡수 광 변조기, 전류 구동 로직 드라이버, 면발광 레이저, 비제로 복귀, 4-레벨 진폭변조, 상보성 금속산화막 반도체

학번 : 2014-21636