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Synthesis of Thin Film Barriers by Plasma Enhanced Chemical Vapor Deposition for Display Applications

플라즈마 화학 기상 증착법을 이용한 베리어 필름 합성과 디스플레이 응용

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서울대학교 대학원

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A Ph.D Dissertation

Synthesis of Thin Film Barriers by Plasma Enhanced Chemical Vapor Deposition for Display Applications

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Abstract

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OLED is a self-emissive display can be driven at low voltage and manufactured in a thin layer. In addition, this display operates at a very high speed and emit a color that can be rapidly implemented. Recently, OLED's main interest is mobile screen, large screen TV, flexible and transparent display. The driving device for display is classified to the passive matrix and active matrix. Active matrix is preferred because of higher resolution, lower energy consumption, and large size screen. To apply active matrix on display device, a switching device such as thin-film transistor (TFT) is attached to each pixel. For active driving devices, amorphous silicon (a-Si) and low-temperature polycrystalline silicon

(LTPS) technologies are applied in current TFT –LCD or AMOLED back frame.

Recently, there is an ongoing research on using amorphous oxide semiconductors with large bandgaps to research transparent and fast responsive display driving devices. Moreover, RC delay has a technical problem that must be minimized and reduce power consumption.

Implementation of Source Drain (SD) is a metal wiring essential element for high-speed TFT execution in high-resolution UHD (Ultra High Definition) display's backplane. In this study, the graphite growth plays the role of diffusion barrier of copper wiring that has low resistance wiring with SD metal wiring. The chemical and mechanical stripping methods of conventional graphene synthesis application on large area panels is limited. Up to now, the large size graphene has been used as an electrode, but this implementation is limited to making the large-scale process by synthesizing graphene at thermal CVD (900~1000℃) and transferring it to the glass. Despite the fact, a lot of ongoing studies, graphite's thin film synthesis using Plasma Enhanced Chemical Vapor Deposition (PECVD) enables large size and mass production. Furthermore, this area still requires more research on mass production. If low-temperature process for graphite synthesis is possible, this will

become a more advanced technology for device implementation. In this study, the role of copper diffusion barrier was verified, and the possibility of graphite barrier and mass production was verified by TEM and EDAX analysis by synthesizing the deposition temperature at low temperature. In addition, this study suggests the large size display can be obtained through direct PECVD synthesis that will solve the existing problems of large size synthesis.

The display' s TFT characteristics also require a high mobility device that is much higher than the conventional active material a-Si TFT. In particular, a new TFT capable of applying a transparent display and uniformly having high mobility characteristics is required. Materials such as ZnO (Zinc Oxide), IZO (Indium Zinc Oxide) and IGZO (Indium Gallium Zinc Oxide) have been studied as oxide TFTs. IGZO materials with higher mobility than conventional a-Si mobility (<1 cm^2 / V · s) are transparent devices and can be used in transparent displays, thus extending applicability. In this study, we propose a graphite synthesis based on IGZO to be applicable to transparent display and expect the application on large size displays.

The low-temperature Graphite synthesis has many advantages in terms of cost and process simplification because it implements the

process only by using Graphene gas without replacing existing CVD equipment. In addition, it can be used as a graphite synthesis catalyst not only for metal but also for the oxide semiconductor, to raise activation. Moreover, the graphite synthesis to make a thin film can be applied to other fields.

In the next study, it is essential to use backlight in LCD display. The backlight not only includes the visible light but also the UV region, and has instability of TFT characteristics in the active material IGZO device. Due to IGZO' s reaction to light in UV region, it is essential to use a barrier film in order to solve the reliability characteristics of the TFT device deterioration. To maintain the reliability and stability of the TFT, this study on reliability of the TFT was not changed by SiGe (Silicon Germanium) synthesis thin film as a photo blocking barrier. Based on previous research on SiGe has been used as the light absorbing layer in the intrinsic layer in which a P-I (intrinsic layer)-N type structure in a solar cell that is not doped with an impurity in an intermediate insertion layer.

In this study, in order to prevent oxygen vacancy during a-IGZO photoreaction on TFT device, the formation of a light-shielding film of Si-Ge prevents oxygen deficiency. Capacitance formation between SiGe

and IGZO thin film in the thin film formation and lamination structure accumulates electrons charge on the IGZO thin film interface. The characteristics of the transistor were short, and to prevent this shortness, it is important to control the thickness of the buffer layer. Therefore, this shows that the reliability of the TFT device is improved by making the barrier laminate structure that can block the light from the bottom through the optimization of the thickness of the buffer layer.

There are various ongoing technological studies on transparent and flexible displays that to observe the contents without opening the door through the smart window and refrigerator. For this application, the thin film barrier is an essential element and expect to be implemented.

Keyword : Thin Films , Graphite , PECVD , Silicon Germanium , Display Applications

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Chapter 1. Introduction

1.1. Graphene characteristics

Graphene is a perfect 2D crystal of covalently bonded carbon atoms and forms the basis of all graphitic structures.[1,2] Its isolation and characterization by Geim and Novoselov in 2005 [3] has significantly increased the research and potential application for this material. Graphene is the best conductor of heat we know, the thinnest material, it conducts electricity much better than silicon, is 100-300 times stronger than steel, has unique optical properties, and impermeable as a monolayer. These extreme properties combined or separated exhibited in various areas of study; new possibilities are being recognized all the time as the science of graphene and other two-dimensional materials progresses. Graphene's science and technology relies on carbon, which is one of the most abundant materials on Earth. Furthermore, graphene is inherently sustainable and an economical technology. This planar material is compatible with the established production technologies in the field of information and communication technologies. Graphene has attracted increased interest due to fundamental reasons and its

potential for a wide variety of applications. [3,4,5] Among the wide variety of graphene property, graphene's role as a diffusion barrier is examined. A physical separation between protected metal and reactants occur when sp^2 carbon allotropes surfaces form a natural diffusion barrier. This can be seen from the encapsulation of various atomic species inside of fullerenes and carbon nanotubes at high temperatures and in a vacuum. [6] More recently, graphene has been used to form a microscopic airtight "balloon" [7], which clearly demonstrates its property as an impermeable barrier. Graphene is stable under thermal and chemical conditions. Under inert environment, graphene at high temperature is stable and other substrates conducts rapid reactions. When impermeability and thermal (or chemical) stability is combined makes graphene a great alternative for novel protection layer.

In Figure 1 we show photograph images of various metal surfaces, both graphene-coated and uncoated after air anneals and exposure to a liquid etchant. In all cases, the graphene-coated metal surfaces show very little visible change, as opposed to the uncoated metals whose surfaces change appearance dramatically. As a Figure 1(a),

the graphene film can be seen as a molecular diffusion barrier, preventing the reactive agent from ever reaching the metal underneath. More specifically, graphene-coated Cu and Cu/ Ni foils show no changes after lengthy air anneals (200℃,4h, see Figure 1(c)), whereas uncoated films exhibited a substantial darkening.[9] Despite being only one atom thick, graphene is believed to be impermeable to all solid and gases and liquids.[10] This makes it possible to exploit this material as a barrier film.

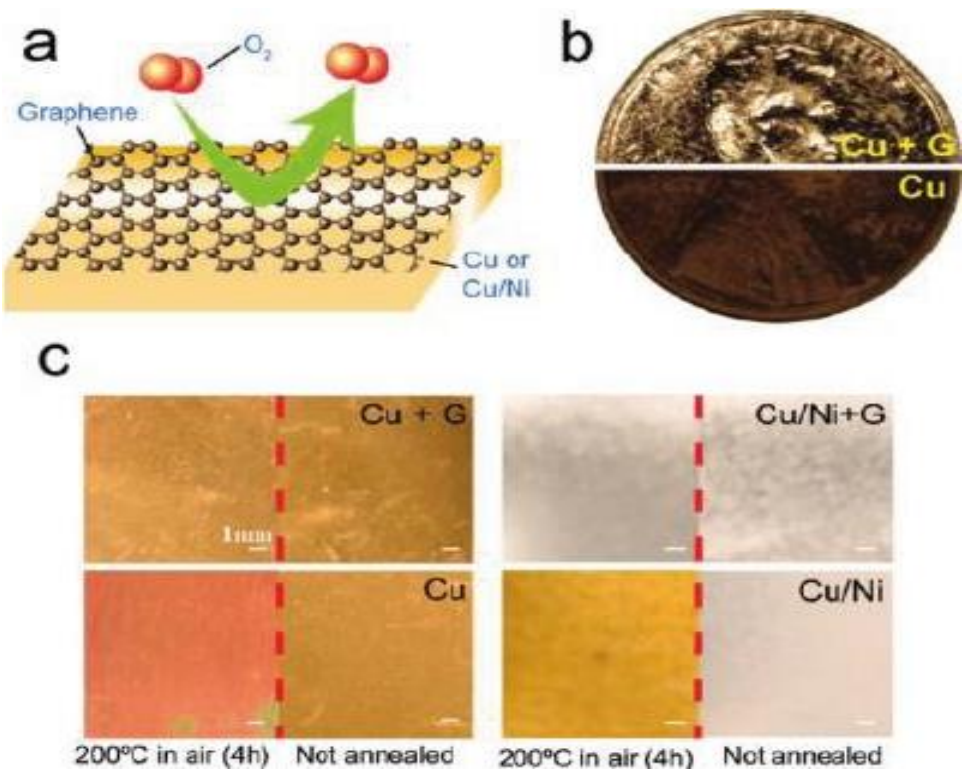

Figure 1. Oxidation Resistance of Graphene-Coated Cu and Cu/Ni Alloy.[8] (a) Illustration depicting a graphene sheet as a chemically inert diffusion barrier. (b) Photograph showing graphene coated (upper) and uncoated (lower) penny after H_2O_2 treatment (30%, 2 min). (c) Photographs of Cu and Cu/Ni foil with and without graphene coating taken before and after annealing in the air (200℃, 4 h).

1.2. Amorphous Si:H and LTPS TFT backplane technology in display

TFT (Thin Film Transistor) controls driving (on/off) of a pixel and known as a switching element, which is a minimum image forming unit of a display. A TFT-Liquid Crystal Display (LCD) is a circuit where a semiconductor film is prepared on an ultra-thin glass substrate to control the liquid crystal and to control each pixel, which is a basic unit of an image. The image information is transferred to liquid crystal when image information with electric signal is applied on TFT, According to the signal intensity arranges the liquid crystals. Then, as the backlight passes through the arranged liquid crystal, and the color filters (R, G, B) implements the image on the screen.

TFTs are formed of thin films and consist of three metal terminals consisting of a gate, source, and drain, an insulating layer, and a semiconductor layer (active layer), which is an electrically conducting channel. TFTs are classified into amorphous-silicon (a-Si), poly-Si (Low-Temperature Polycrystalline Silicon, LTPS) and oxide depending on the materials used. The materials that will be

used depends on the display resolution (ppi) and the driving speed (Hz).

The high-resolution of the display means an increase in the number of pixels per unit area, a reduction in the pixel size, which means a reduction in the size of the TFT by increasing the number of TFTs per unit area. Thin film transistors are generally defined as "Field Effect Transistors (FETs) made using a semiconductor thin film on an insulating substrate". Similarly, a TFT is a device that has three terminals: a gate, a drain, and a source. The main function is the switching operation. The operation principle of the TFT is very similar to that of FET. The switching operation is performed by turning on the conduction state (ON) or turning off the conduction state (OFF) by adjusting the voltage that applies the current flowing between the source and the drain to the gate which is the third electrode. Therefore, the gate induces the voltage towards the source, drain electrode.

The operation region of the thin film transistor is divided into two regions: a linear region and a saturation region, as in a Metal Oxide Semiconductor Field Effect Transistor (MOSFET). When the drain voltage is low, the characteristics between the drain and the source

basically exhibit the ohmic characteristic. As a result, the drain current becomes proportional to the drain voltage. On the other hand, at a high drain voltage, the drain current exhibits a constant value regardless of the increase of the drain voltage.

The analysis of the electrical characteristics of TFTs uses a gradual channel approximation, in which the electric field in the x-direction (vertical axis) forms a channel and the electric field in the y-direction (horizontal axis). (E_y is the constant in the channel) Thus, it is assumed that the thickness of the channel is only affected by the gate voltage on the x-axis and not on the y-axis.

The relationship between the induced charge Q_I and the gate voltage V_g when the gate voltage is greater than the threshold voltage (V_{th} or V_t), the charge is induced in the channel expressed below.

$$Q_I = -C_{sinx}(V_g - V_t)$$

Where C_{sinx} is the capacitance of the gate insulating film in the channel. This is the case when the channel voltage is 0V. In fact, since the voltage V is formed by the voltage between the drain and source, the charge induced in the channel is corrected below.

$$Q_I = -C_{sinx}(V_g - V_t - V)$$

The channel current can be used by using the expression below.

$$I_D = W * \mu_n * Q_I * E_y$$

Where W is the width of the channel, μ_n is the electron mobility, Q_I is the induced charge, and E_y is the y direction electric field. Now, using $= -\frac{-dV}{dy}$ to assign to I_d expression,

$$I_d dy = W * \mu_n * Q_I * C_{sinx}(V_g - V_t - V)dV$$

Integrating this from y= 0 to, and V= 0 to V_d (drain voltage) gives,

$$I_d = C_{sinx} * \mu_n * \frac{W}{L}\left[(V_g - V_t)V_d - \frac{1}{2}V_d^2\right] \cdots\cdots (1)$$

When V_d is under the very small linear region (V_d <1V), we can simply express as follows.

$$I_d = C_{sinx} * \mu_n * \frac{W}{L}[(V_g - V_t)V_d] \cdots\cdots (2)$$

If the drain voltage is increased and the gate voltage is neutralized, $Q_I = -C_{sinx} * (V_g - V_t - V)$ channel will disappear from the drain side (pinch off) and the drain current will no longer increase. Therefore, the drain current in the linear region obtained previously is no longer matched.

This situation can be satisfied by setting Q_I to 0. Thus, substituting $V = V_g - V_t = V_d$ into equation (1) gives the following expression.

$$I_d = \frac{C_{sinx} * \mu_n * W}{2L}(V_g - V_t)^2 \cdots\cdots (3)$$

This equation assumes that the saturation condition is satisfied ($V_g < V_d + V_{th}$)

$$I_d = K(V_g - V_{th})^2$$

$$\sqrt{I_d} = \sqrt{K}(V_g - V_{th})$$

$$K = \frac{1}{2} * \mu_n * C_{sinx} * \frac{W}{L}$$

When the capacitance of the insulating thin film is known, the length and the width of the transistor channel, μ_n (mobility: electron mobility) can be known since the slope $\sqrt{K}$ is known from the measurement curve of V_g and $\sqrt{I_d}$.

The hydrogenated amorphous silicon (a-Si:H) TFT has long been the key technology in the Active-Matrix Liquid Crystal Display (AM-LCD) industry. As the most critical element of the entire AM-LCD, the active-matrix backplane commonly consists of an array of a-Si:H TFT pixel electrode circuits, which directly drive each individual liquid crystal cell pixel.[11,12] This approach crucially reduces the pixel crosstalk and validates LCD to have higher resolution. Alike other microelectronics industry pursues the transistors miniaturization that is dictated by Moore's Law for lower production cost, heightened functionality. Therefore, scientists and engineers continuously explore new material and processing technologies to fabricate TFT backplane over larger substrate areas. Because of this

unique technological roadmap, the TFT backplane has also frequently been called "macro electronic" device. [13,14]

The crystalline silicon is in diamond formation, and has similar bonding angle and bond length of a-Si. However, there is no regularity in the tens of atomic groups. The hydrogenated amorphous silicon has larger defect density than the hydrogenated amorphous silicon (a-Si:H). To justify the larger defect is because they have more dangling bonds in the non-hydrogenated amorphous silicon and reduced by hydrogenation.

During the past decades, the plasma enhanced chemical vapor deposition (PECVD) has been proven to be the ideal technique to deposit highly uniform a-Si:H thin film while keeping up the trend of substrate size scaling.[15] Today, the state-of-art Gen-8 facility is able to process glass substrate approximately 2160 ×2460 mm in size,[16] which can be produced up to six 52-inch flat panel TV screens from one single substrate. The typical PECVD a-Si:H TFT has field effect mobility (μ_{eff}) of 0.6 ~ 0.8cm^2/V·s, sub-threshold swing of 0.3 ~ 0.4V/dec, off-state drain current (ID_off) below 10-13A and on-to-off ratio about 10^7.[17] These properties are suitable for liquid crystal cell switching but the μ_{eff} could become insufficient for the

new requirements of next-generation displays. For example, the future trend for AM-LCD is toward large area (e.g. 82-inch) with QFHD (3840×2160 pixels) resolutions.[18,19] To suppress the display motion blur effect in QFHD, high frequency (120~240Hz or even higher) display driving circuits will be inevitable.[20] The driving scheme of the 120Hz (or higher) QFHD display only allows the pixel charging time to be less than 4 μsec.[19] Conventional a-Si:H TFT backplane configuration does not work well in such short time and the pulse/clock signal can be distorted. To address this issue, proposed solutions are focused on reducing the gate bus-line RC propagation delay, such as adding gate planarization layer[21], adopting buried bus-line structure[22] or using low resistance Cu interconnection[23]. Nonetheless, the low μ_{eff} (< 1cm^2/Vs) of a-Si:H TFT itself can still fundamentally restrict the high-frequency response of backplane. A TFT LCD pixel charging time (t-charge) is about five RC time constants (t-charge ~ 5RonC_{pixel}), where C_{pixel} is the pixel capacitance and Ron is the TFT channel resistance. Ron can be estimated as follows:

$$Ron \cong \frac{L}{W * \mu_{eff}(V_{gs} - V_{th}) * C_{sinx}} \cdots\cdots (4)$$

Where W and L are channel width and length, respectively; V_{gs} and Vth are gate voltage and TFT threshold voltage, respectively; and C_{sinx} is the gate insulator capacitance. For a typical a-Si:H TFT pixel, C_{pix} is ~0.5pF, and Ron is ~1.67MΩ (W/L=3, μ_{eff} ~ 0.6cm^2/Vs, ($V_{gs}-V_{th}$)~10V and C_{sinx} ~3.32×10-8 F/cm^2). This combination results in a t-charge of 4.2μsec. Thus, the t-charge required for a-Si:H TFT is too long, and driving large size, high rate/ resolution display with a-Si:H TFT backplane will be either impractical or complicated.[19] A high-mobility material is desired, since it can reduce Ron and t-charge. The other emerging area in AM-FPD is the emissive display such as the active-matrix organic light-emitting display (AM-OLED), where the organic light emitting diode (OLED) is directly integrated with the TFT pixel electrode circuit. AM-OLED avoids the need of backlight and the dynamic range of the AM-OLED brightness can be controlled at the pixel level, which is ideal for TV applications.[24] In addition, it can have an extremely high contrast ratio and delivers much better picture quality than the AM-

LCD.[25] Regardless of these aesthetic properties, AM-OLED poses a more strict condition on the TFT backplane. Unlike liquid crystal that only changes it phase with external electrical field, OLED takes a significant portion of current to produce light. The μeff of a-Si:H TFT, unfortunately, is not high enough to drive a large area AM-OLED.[26] Because the TFT may constantly operate under high bias, a long-term electrical instability is another concern[27] and can also make the pixel electrode circuit design more complicated (e.g. additional compensation circuits are needed).[28]

Active-Matrix Organic Light Emitting Diode (AMOLED) displays are manufactured using Low-Temperature Polycrystalline Silicon (LTPS) Thin Film Transistor (TFT) substrates (backplanes). Amorphous-Silicon (a-Si) TFTs widely used in conventional Liquid Crystal Displays (LCDs) have advantages such as low process cost, high yield, and excellent uniformity. Nevertheless, incessantly turned causes severe deformation of threshold voltage that is unsuitable for AMOLED pixel driving. Since the positive and negative gate voltage are periodically and repetitively applied to a TFT that is used for a pixel switch of an LCD, an a-Si TFT will alleviate the threshold voltage fluctuation. Therefore, even if the threshold voltage slightly

changes, the voltage applied to the liquid crystal is not affected because the TFT acts as a simple switch. On the other hand, in AMOLED, TFT is not a simple switch but a current source that determines the current flowing in the OLED according to the signal voltage. Thus, a small change in the TFT threshold voltage has a decisive influence on the luminance of each pixel. Therefore, when the threshold voltage changes according to the elapsed time of the driving time of the TFT, the afterimage and the luminance change is severe.

AMOLEDs using LTPS TFTs are fabricated from top-gate structures in which the source or the drain is doped with Boron (B) to form PMOS and the gate is formed on top of the LTPS thin film. The LTPS thin film is mostly fabricated using an excimer laser annealing (ELA) process in which a-Si thin film is irradiated with an excimer laser to crystallize. The metal layer constituting the electrode and the data line of the gate of the TFT and the source or the drain is sequentially formed with the inter-layer dielectric (ILD) interposed in between. The organic layer is thick (about 3 μm) to cover the organic layer. The voltage information for determining the luminance of each pixel is stored in a storage capacitor (C_{st}), which is

formed using a gate metal layer, a doped LTPS thin film, and a source or a drain electrode.

The most of the a-Si thin film is crystallized through the 308 nm XeCl excimer laser. The LTPS thin film crystallized by the ELA process is composed of irregularly arranged grains. Since there are a large number of dangling bonds at the boundaries of the crystal grains. The crystal grain boundaries and crystal grain boundaries are clearly expressed, the characteristic deviations are enormous according to the arrangement of the crystal grains in the channel region of the TFT.[11,16,18] The characteristic deviation of the LTPS TFT causes a deviation of the current flowing in the pixel OLED, causing the irregular brightness of the red, green and blue pixels.

LTPS TFT using the ELA process is currently applied to AMOLED production but requires improvement because it requires expensive laser equipment and demanding process control. Considering the production of large-area AMOLED TVs in the future, it is more necessary to develop low-cost solid-state crystallization technology that can replace ELA or new TFT materials such as oxide semiconductors.

Table 1 summarizes the challenges of TFT backplanes for next-generation optoelectronics and it is clear that a new high mobility semiconductor material yet with a uniform amorphous phase over a large area is highly desired.

	a-Si:H TFT	LTPS TFT	Oxide TFT
Mobility ($cm^2/V \cdot s$)	~1	~100	~30
Uniformity	Good	Poor	Good
Process Temperature(℃)	150~350	350~450	150~400
Cost	Low	High	Low
Yield	High	Low	High
Comment	Low mobility Limited current driving capability	Additional crystallization process required	Balance between mobility and process

Table 1. Comparison of different TFT technologies.

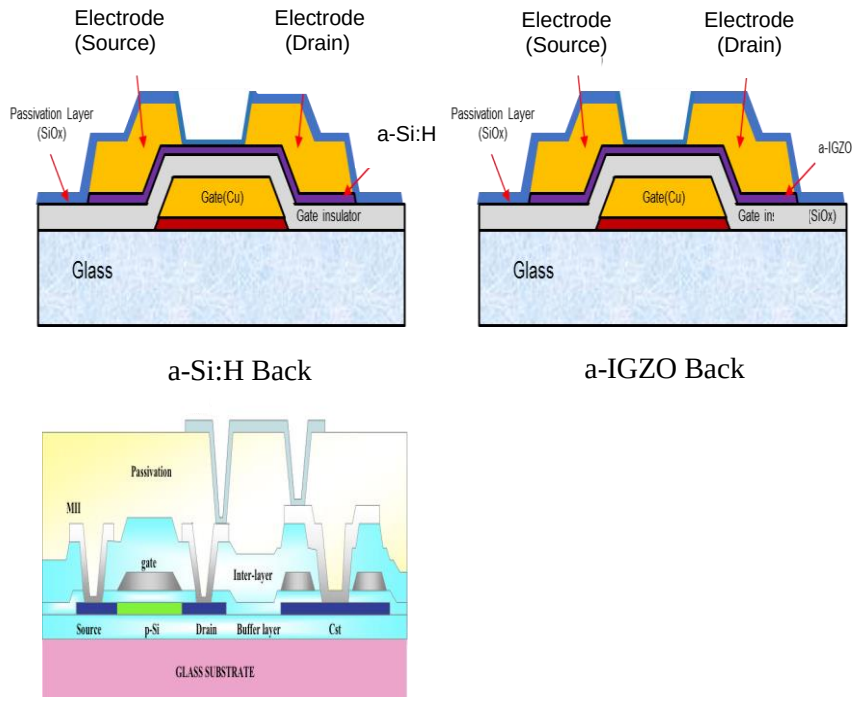

Figure 2. Comparison of different TFT backplane structure.

1.3. High performance amorphous In-Ga-Zn-O TFTs

Despite the fact, the a-Si TFT is a typical driving device of an LCD, the electron mobility is as low as 0.5 (cm^2 / V·s) or less in the case of a mass-production device. In particular, characteristics of uniformity, simplicity, excellent reproducibility of the process in the large area is the result of technology advancement. Despite this fact, TFT characteristics in TFT-LCD is still required for evolution of higher resolution, 3D TVs and larger TVs. Moreover, it entails higher mobility devices that exceeds a-Si TFTs. Consequently, a new TFT is called for that can uniformly perform high mobility characteristics in a large area. Hence, the solution to this problem is the study of an oxide TFT.

The greatest feature of oxide TFTs is their high electron mobility compared to conventional a-Si TFTs. Due to the low leakage current, these features make it possible to implement high-resolution panels. The panel structure is almost the same as a-Si TFT, and easily switched to the production line.

Oxide TFT and a-Si TFT are similar except for the production of these TFTs. Therefore, it is possible to utilize existing LCD line equipment and immensely reduce facility investment.

There has been great interest in adapting TFT made of ionic amorphous oxide semiconductors. Specifically, the ternary oxide system which consists of In_2O_3, Ga_2O_3 and ZnO has shown promising electrical performance for TFT active layer with a high μ_{eff} (3~12 $cm^2/V \cdot s$), low ID_off (<10-12A) and expected good uniformity compatible with the state-of-the-art Gen-8 substrate size.[29,30] It can be easily seen that a-IGZO TFT is currently the only technology which can achieve the desired balance between high mobility and large area uniformity. Although poly-crystalline silicon (poly-Si) TFT has μ_{eff} close to 100 $cm^2/V \cdot s$, it required additional re-crystallization steps such as excimer-laser annealing[31] , metal seeding[32] or solid phase crystallization[33]. These add more complexity and costs to the process. Also, the substrate area used by poly-Si TFT technology (Gen-4, 730 × 920 mm) [25] is about 4 generations behind what a-Si:H TFT can achieve (Gen-8) today. Mono-oxide semiconductor, ZnO, has been used as the active-layer in TFT channel. ZnO layer can be deposited by pulse laser deposition

(PLD)[34], RF magnetron sputtering[35] or atomic layer deposition (ALD)[36] and the TFT μ_{eff} is around 20~50 cm^2/Vs. Despite its high mobility, due to its strong poly-crystalline nature even when deposited at room temperature[37], the grain boundary of such oxide semiconductor could affect device electrical properties, uniformity and stability over a large area. Single-crystalline $InGaZnO_4$ (sc-IGZO) has a complex layered structure with alternating laminated layers of InO_2 and GaO(ZnO).[38,39] Figure 3 (a) illustrates the crystal structure of $InGaZnO_4$. This structure was then inputted into the modeling software[40] to simulate the x-ray diffraction pattern of the $InGaZnO_4$.[38] The result is highly consistent with the actual XRD rocking curves. This also indicates that the structural model is closely representing the actual material. Orita et al. reported the first-principles molecular orbital (MO) calculations of $InGaZnO_4$ crystal structure by discrete variational (DV)-Xα method.[39] Figure 4 shows the density-of-states (DOS) distribution calculation for $InGaZnO_4$. The O 2p and Zn 3d-orbitals primarily forms valence band while the s and p orbitals of the three metals form conduction band with certain influence by the O 2p-orbitals. The In 5s partial DOS shows a shoulder peak at low energy. Therefore, In 5s band is the

only one that forms the conduction band minimum (CBM) of $InGaZnO_4$. Nomura et al. subsequently reported the calculation of a-IGZO electronic structure by the pseudopotential and plane wave method at the local-density approximation (LDA) level.[38] Also, it suggested that the CBM of a-IGZO is formed mainly by In ions (Figure 5).

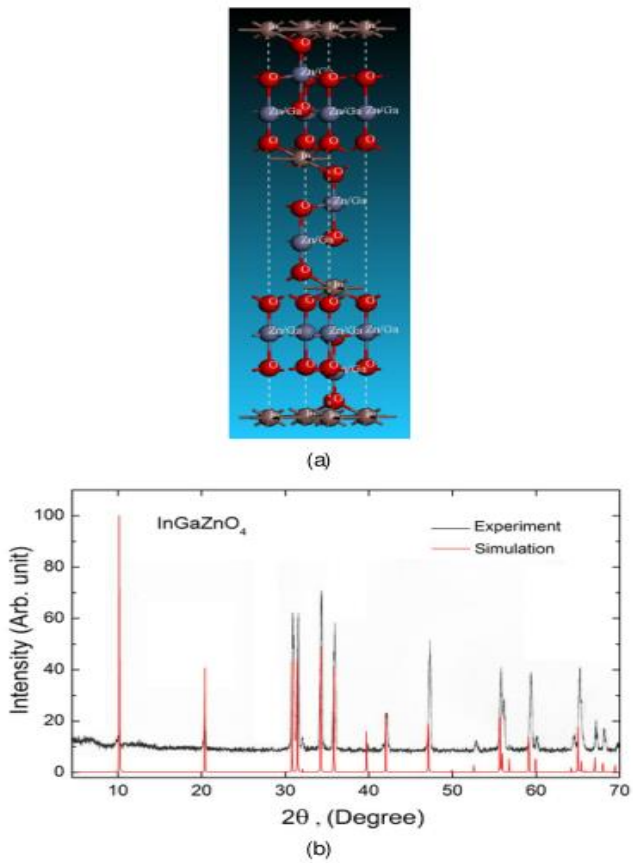

Figure 3. Illustrates the crystal structure of $InGaZnO_4$[38,39]

(a) Structure of the $InGaZnO_4$ crystal. The brown, blue and red balls represent In, Zn/Ga and O atoms, respectively. (b) XRD rocking curves of the $InGaZnO_4$. Black line: experimental result, red line : simulation result.

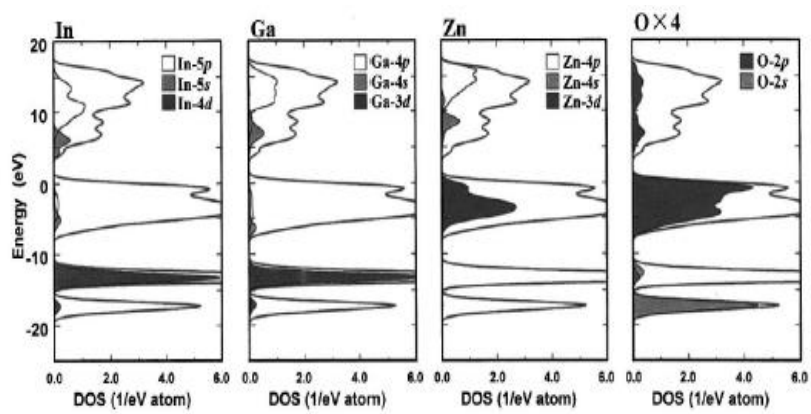

Figure 4. Partial density-of-states (DOS) curves for $InGaZnO_4$crystal structures.[39] The top of the valence band is located at zero energy and the total DOS is also shown in each figure as reference.

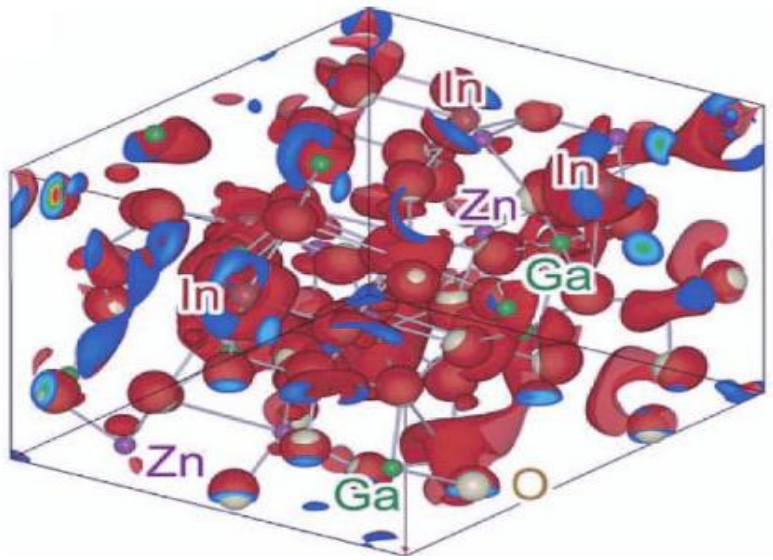

Figure 5. The red surfaces represent the conduction band minimum (CBM) wave function in a-IGZO structure.[38] The CBM is composed of In 5s orbitals hybridized with O 2p. The blue to red planes show a cross section of the CBM on the edge planes of the simulation cell.

Unlike ZnO, a-IGZO can have a uniform amorphous phase because multiple oxides(In_2O_3& Ga_2O_3) are introduced to promote the glass phase formation[41] and the amorphous phase is thermally stable up to ~500 ° C. [42] Several methods are been reported for a-IGZO deposition, including PLD.[42,43] RF[44] and DC[45] magnetron sputtering while the latter is the most attractive due to high rate deposition in comparison to other methods. Because of the unique electronic structure, a-IGZO is insensitive to bond angle variance of metal-oxide-metal chemical bonds induced by structural randomness. As illustrated in Figure 6(a), in previous covalent bond semiconductors (such as Si), electrons conduct at highly directional sp^3 bonding. At amorphous state, these semiconductors distortions can occur in sp^3 bonding and the result is decrease in carrier mobility. On the other hand, in Oxide base material (such as In-Ga-Zn-O), electrons conduct at metal ion' s ns orbital. Since ns orbital is symmetrical, the conducting path and carrier mobility can still be preserved even in the amorphous phase. (Figure 6(b)) In order to ensure high mobility on the amorphous phase it is necessary for a sufficient ns orbital overlap between the metal ions. To fulfill this requirement, Hosono et al. proposed a working hypothesis that states the metal ion should

be heavy post transition metal cations with electronic configuration of $(n-1)d^{10}ns^0$, where $n \geqq 5$.[45-47] For example, the fraction of In_2O_3 content[45] primarily determines the Hall mobility of the In-Ga-Zn-O system. Hence this verifies the Hosono working theory since In^{3+} ionic radius(n=5) is the largest among the metal cations.

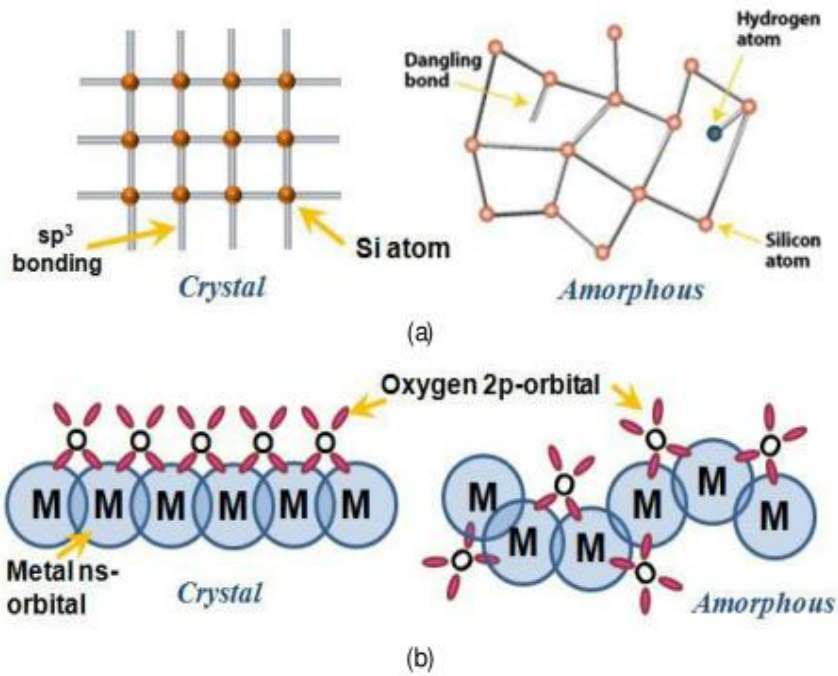

Figure 6. Schematic orbital drawing of electron conducting pathway. [42]

(a) Conventional covalent bond semiconductors (e.g. Si) and (b) ionic oxide semiconductors.

For TFT to have a low ID_off and high on-to-off ratio, it is important to control the semiconductor carrier concentration to a very low level. In IAOS, carrier generation can occur via oxygen vacancy formation. For examples, ZnO has been reported to have a very high carrier concentration in the as-deposited states.[48] It is usually because of the un-optimized deposition condition and the generation of excess oxygen vacancies in the thin-film. The incorporation of Ga^{3+} actually helps in suppressing the oxygen vacancies in a-IGZO thin-film since it has a stronger bonding to oxygen than Zn or In ions.[42] A comparative study between a-IZO and a-IGZO has also shown that a-IGZO is able to have five orders of magnitude larger reduction in carrier concentration than a-IZO when two thin-films are deposited under the same condition [35] A-IGZO TFTs possesses unique physical properties and better electrical performance over traditional a-Si:H TFTs.

The disadvantage of a-IGZO semiconductor materials is that LCD display is non-self emitting white light and always irradiates from a separate backlight unit like CCFL or LED. The gate metal electrode reflects most of the light, but around 5% of the total light transmitted to the channel by refraction or reflection in lateral

direction. However, when light having a high energy such as UV wavelength or blue light enters the oxide semiconductor, a photocurrent is generated and the threshold voltage (V_{th}) of the TFT shifts to negative.[49]

This threshold voltage shift is a significant issue because it causes malfunction of the TFT element responsible for the switching function to cause panel lighting failure. In order to overcome the optical effects of a-IGZO, we will address a stable device through barrier thin film synthesis that acts as light shielding.

The scope of this dissertation work is to study various aspects of the a-IGZO TFTs and to shed light on the potential application of such technology to future electronics.

1.4. Overview of PECVD system

The Plasma Enhanced Chemical Vapor Deposition (PECVD) is a modification of the CVD process, in which a plasma is used as a source of energy in order to obtain the dissociation of the reactive gases at temperatures at which they would not dissociate thermally. The ionization of atoms (or molecules) in the gas is alternatively known as the plasma. The following components are neutral atoms or molecules (depending on the type of gas), ions and elections. To measure the ratio between ionized and neutral particles is known as the degree of ionization. The plasma's degree of ionization used for PECVD can range between $10^{-6} \sim 10^{-4}$. The energy transfer between the atoms and the electrons is inefficient due to the mass difference between them: this condition makes it possible to increase the mean kinetic energy of the electrons without increasing the global temperature of the gas. This kind of plasma is at non-equilibrium conditions and, since the degree of ionization is very low, the temperature of the whole gas is practically equal to that of the neutral molecules, while the electron energy can be more than 1eV(which, in thermal equilibrium conditions, would correspond to a temperature of About 10^4K). A detailed description of the plasma is possible in terms

of kinetic equations, which have to account for the different processes that take place inside the plasma: First, acceleration of the electrons due to the energy transfer from the external source. Second, excitation of neutral atoms by electron impact (possibly followed by relaxation with radiative emission). Third, ionization of neutral atoms by electron impact. Forth, ionization of neutral atoms due to collisions with other atoms or ions. Fifth, recombination of ions and electrons (with radiative emission). In order to light the plasma, it is necessary that a few ionized atoms are present before the external energy source is turned on. Otherwise, there would not be any electrons to accelerate and it would not be possible to initiate ionization of the neutral atoms. However, under the gas atmosphere, there is always a slight degree of ionization, due to the thermal energy or the effect of cosmic rays. If the plasma consists several gas species, which in the case two or more reactive gases dilute into the carrier gas. Moreover, there are additional processes that are present involving different chemical species. Under this circumstance, the presence of high kinetic energy electrons allows the formation of chemical reactions which would normally require a higher gas temperature. To be more specific, there is a high possibility of

obtaining molecule dissociation of a gas and radical formation, which are formed at significantly lower temperature than the required temperature for thermal dissociation.

To generate the plasma, a D.C supply is applied in the gas phase, or tens of GHz radio frequency (R.F). The most common frequency is at 13.56 MHz. In the plasma state, the electron's speed is faster than the cation's speed. Therefore, the electrons shift toward the anode and these electrons bounce back. Thus, the potential near the electrode is lower than the center portion of the plasma. In addition, a sheath region which does not generate plasma occurs, and the plasma region has a constant potential between two electrodes.[50]

There are various process parameters for forming a thin film in a plasma. The following control parameters must be well controlled to obtain good films. The pressure in the chamber determines the mean free path until gas molecules collide with each other, thus affecting whether the reaction occurs on the substrate surface or in the gas. When radials react in the gas before they reach the substrate, contamination occurs in powder form. The gas flow rate determines the residence time of the gas in the chamber. RF power determines the amount of dissociation of the feed gas, thus affects the growth

rate. The temperature of the substrate affects the chemical reaction at the growth surface of the film.

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Chapter 2. Growth of thin graphite films for solid diffusion barriers

2.1. Large-scale transfer-free growth of thin graphite films at low temperature for solid diffusion barriers

2.1.1. Introduction

The structure of graphite is shown in Figure 7. The carbon atoms form continuous hexagons in stacked basal planes (ab direction). Within each basal plane, the carbon atom is strongly bonded to its three neighbors with a covalent bond, having a bond strength of 524 kJ/mol. This atomic bonding is threefold coordinated and is known as sp^2. The hybridized fourth valence electron is bonded to an electron of the adjacent plane by a much weaker metallic-like bond of only 7 kJ/mol. The spacing between basal planes (0.335 nm) is larger than the spacing between atoms in the plane (0.142 nm). [1]

A single sheet of sp2 hybridized carbon atoms defines the two-dimensional graphene crystal, the elementary building block of graphite. Due to its unique electronic, mechanical and optical properties, [2,3] researches on fundamental and industrial aspects of

graphene have been actively performed[4,5]. Especially, a number of synthetic methods have been proposed to the industrial application mainly using chemical vapor deposition (CVD) method with various feeding gasses and substrates.[6,7] There has been continuous effort on devoting graphene growth on Cu and various experimental variables affect the sample quality. The active species for graphene growth is CH_x species instead of carbon. As shown in Figure 8, on Cu (111) surface, various CH_x species are used in Cu substrates. All four dehydrogenation steps are endothermic with activation energy barrier about 1.0−2.0eV for each step. The final product C+4H is already 3.60eV higher in energy.[8] The most common precursor is methane (CH_4), which is generally pyrolyzed at 1100°C or above, over a wide range of pressure from about 100 Pa (0.001 atm) to 10^5 Pa (1 atm). The reaction in a simplified form is as follows:[9,10]

Reaction: $CH_4 \rightarrow C + 2H_2$

Other common precursors are ethylene (C_2H_6) and acetylene (C_2H_2). Acetylene can also be decomposed at lower temperatures (300–750°C) and at pressures up to 1 atm, in the presence of a

nickel catalyst.[11] Another common precursor is propylene (C_3H_6), which decomposes in the 1000–1400°C temperature range at low pressure (= 1.3 x 10^4 Pa or 100 Torr).[12]

The decomposition activation energy of precursor gases are still undetermined and shows a large scatter. There are some reported values shown below:

Methane, 78–106 kcal/g·mol.

Ethane, 60–86 kcal/g·mol.

Acetylene, 30–50 kcal/g·mol.

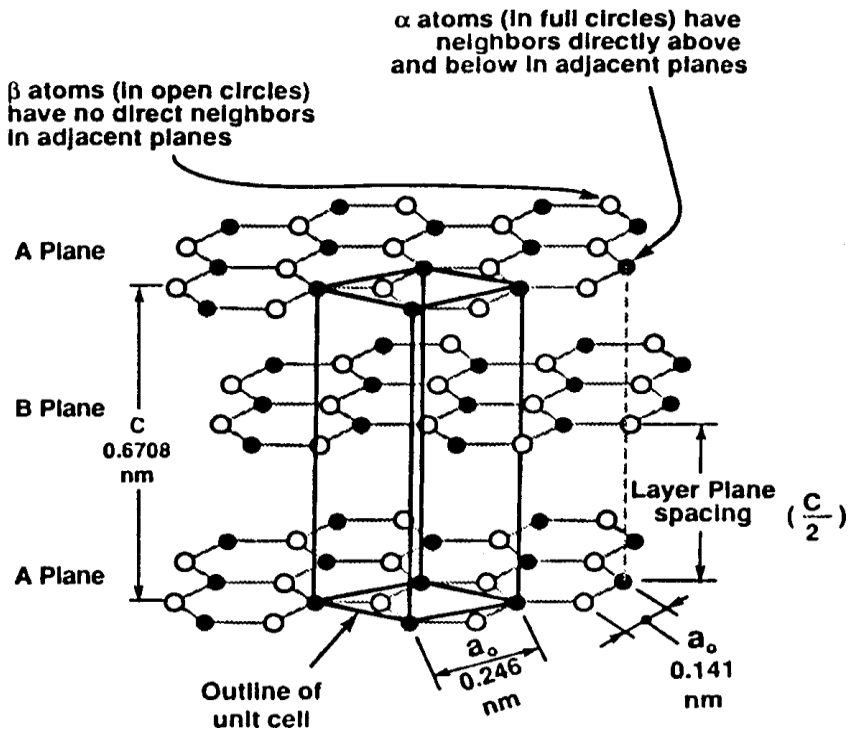

Figure 7. Structure of graphite.[1]

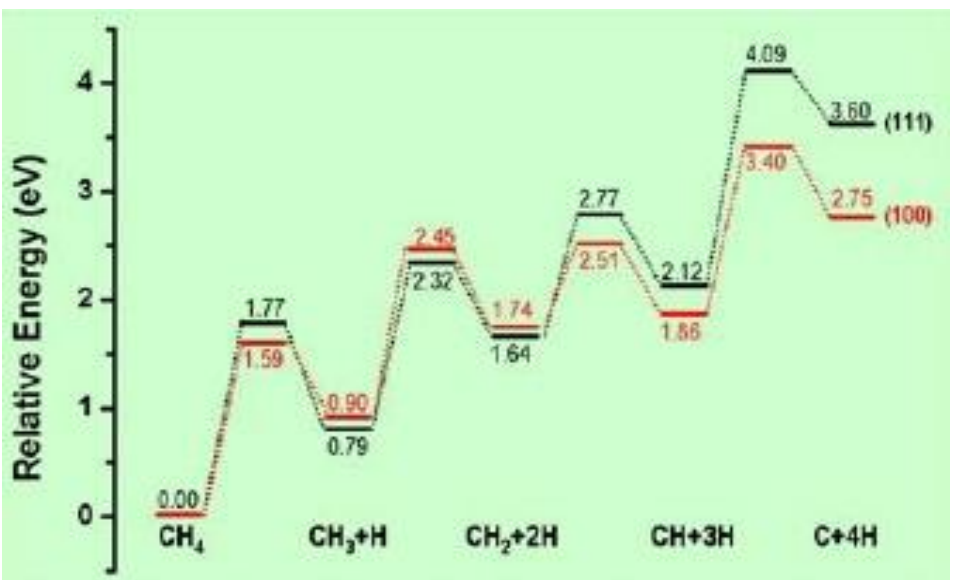

Figure 8. Energy profile of the dehydrogenation processes of CH_4 on Cu (111) and (100) surfaces.[8]

We can use the C_2H_2 (acetylene gas) species in Graphene growth. The CVD becomes a general route for graphene synthesis but high-temperature process around ~1000° C is inevitable. However, to enhance their accessibility from the various industrial fields as an economical way, a low-temperature synthesis of graphene would be an important subject. For the industrial mass production of graphene-based films, a low temperature, rapid, and large-scale synthesis is a key technology. A low-temperature process is an important factor for semiconductor contact materials for device production. More specifically, the direct growth of high-quality graphene on predesigned electronic devices might become a feasible solution as many researchers hope to realize using carbon -based materials. From the point, the trials to realize the low temperature graphene synthesis have been reported recently.[7,13] In this paper, we present the low-temperature synthesis of thin graphite sheets at less than 350° C using acetylene gas (main gas) in a plasma enhanced CVD system; the system consists of a plasma-assisted feeding gas dissociation region. Plasma enhanced CVD is also expected to be a useful method for graphene-based film synthesis. Although there is a room for further development to reach high

structural integrity of graphene structure and further decrease of synthesis temperature, the obtained results show the availability of the present system and high potential of the produced materials for various applications such as transparent, flexible and conductive films in LCD, OLED and flexible displays. Generally, Carbon atoms with sp^2 and sp^3 hybrid orbital' s are able to form three and four bonds with neighboring carbon atoms, respectively, which form the bases of graphene and diamond. An ideal graphene consists a monatomic layer of carbon in the form of perfect two-dimensional (2D) honeycomb lattice. Looking at the graphene properties that monolayer graphene membrane is impermeable to standard gases including helium [14] when considered a C-C bond distance of 1.42Å.[15] Since graphite is a formation of multiple layers via Van der Waals force, the impermeable graphene properties between C-C bond spacing can be used in the role of a solid diffusion barrier.

Conventional active-matrix flat panel displays are based on amorphous silicon or low-temperature polycrystalline silicon (LTPS) thin-film due to their superior applicability and uniformity.[16~18] However, in terms of electrical properties, a-Si based materials show poor mobility (~1.5 $cm^2 V^{-1} s^{-1}$) and LTPS has difficulties and

complications in obtaining a high mobility due to its crystallization originating from laser annealing.[19,20] Consequently, researchers have been focusing on amorphous indium gallium zinc oxide (a-IGZO) thin films, which have superior charge mobility with convenient synthesis methods without any complex post-process.[21~23] Nevertheless, the solid diffusion of the components into other layers such as electrodes, passive layers, gate materials and dielectric layers during the fabrication of TFTs highly degrades the electrical and optical properties of the a-IGZO TFTs.[24~27] Therefore, it is essential that the barrier films are able to prevent this diffusion phenomenon.

Graphene, which has a hexagonal carbon lattice in two dimensions,[28] shows outstanding electrical, optical and mechanical properties with high thermal and chemical stabilities.[29-31] Many research studies have focused on graphitic films as the barrier layers for silicon-based industrial devices.[32,33] It is also expected that the diffusion-impenetrable properties of carbon-nanofilms can be utilized for conventional a-IGZO TFT based display application.[34,35] However, the conventional transfer method and direct growth on the TFTs with high temperature are limited due to wet transfer conditions and low T_g (540 °C) of the glass substrates,

respectively.[36–38] A new transfer–free synthesis platform should be introduced for future industrial displays with low temperature and reasonable cost. In this work, we report the large–scale transfer–free growth of thin graphite films on an a–IGZO substrate (370 × 470 mm^2) at low temperature (350 ° C) for solid diffusion barriers using plasma enhanced vapor deposition (PECVD). In addition, hydrogen plasma treatment on the a–IGZO substrate brings about homogeneous sheet resistance and resistivity (~1.89 $\times 10^2$ Ohm/sq and ~37.8 $\mu\Omega$ cm, respectively). Through these graphite solid diffusion barriers, we were able to fabricate a–IGZO TFTs without any structural changes and solid diffusion to other layers. Therefore, we believe that our method can be widely used to protect solid–diffusion in industrial TFTs that need to be preserved for stable operation in future display electronics.

2.1.2. Experimental

Synthesis. A large-scale a-IGZO film (thickness ~150 nm) was grown on a glass substrate (370 × 470 mm^2) using a DC sputtering system under Ar and O_2 gas atmosphere at room temperature. In_2O_3, Ga_2O_3, and ZnO (the ratio is 1 : 1 : 1 mol%) was used as the precursors to synthesize a-IGZO films. After the synthesis of a-IGZO films, very homogeneous graphite layers were directly synthesized on the a-IGZO substrate using PECVD. Before graphite synthesis on the a-IGZO substrate, hydrogen plasma pre-treatment was processed on the a-IGZO substrate. The plasma power was 700 W and the base pressure was 700 mTorr. The graphite film was grown with C_2H_2 : Ar (30 : 1) at 350 ° C under 700 mTorr for 600 s.

Characterization. Structure bonding was analyzed using X-ray photoelectron spectroscopy (XPS), which was carried out with a KRATOS AXIS-His model at the Research Institute of Advanced Materials. Raman spectra were obtained with a Renishaw micro-Raman spectroscopy with an excitation wavelength of 514.5 nm, and an Ar laser. The spot diameter was approximately 2 μm. To confirm the uniform sheet resistance (R_s), at least 49 points of sheer

resistance and R_s were mapped over the glass substrate. To determine the surface morphology and component elements, field-emission scanning electron microscopy (FE-SEM) was performed (AURIGA Carl Zeiss). Optical microscopy was performed with a Nikon ECLIPSE LV 100ND, and the transmittance was characterized using UV-vis spectroscopy (Agilent 8453).

2.1.3. Results and Discussion

Figure 9 shows a schematic illustration of a columnar graphite growth process on the a-IGZO substrate and field-emission scanning electron microscopy (FE-SEM) images, which show a gradual increase of the column density with growth time. At the initial step, hydrogen gas treatment was processed and low density of carbon nucleation was formed (Figure 9a) and then, the density of seeds was increased (Figure 9b). Finally, the seeds were grown to a columnar structure and the density of the columnar structure also increased (Figure 9c and 9d). The SEM images show the gradual increase of the surface roughness with a number of carbon nucleations on the a-IGZO substrate after 2 and 4 min acetylene gas flow (Figure 9e and 9f). And then, these seeds were agglomerated together to form larger clusters, as shown in Figure 9g and 9h. Next, the grown clusters were connected to each other (Figure 9i) and finally the surface was fully covered by graphite sheets, which were 191.4 nm thick after 10 min (Figure 9j). In addition, no protrusion was observed in the graphite layers, indicating that the graphite films were uniformly synthesized with columnar structure over the large area.

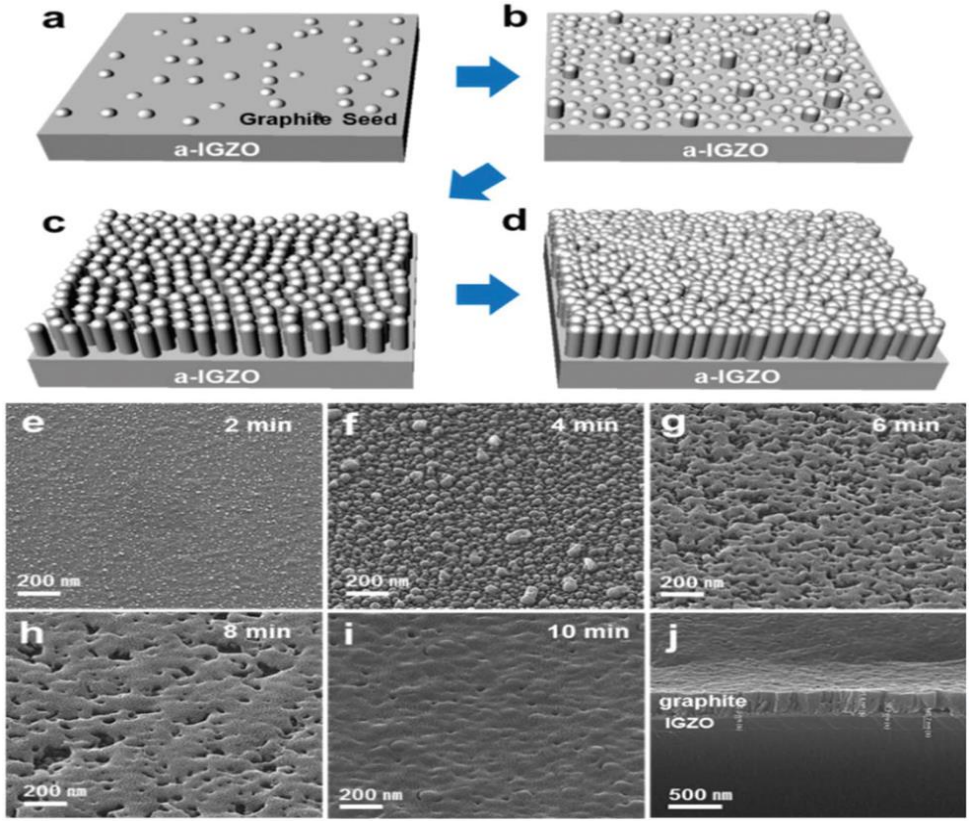

Figure 9 Schematic illustrations and SEM image of the graphite growth.

(a)-(d) Schematic illustration of the graphite synthesis process on the a-IGZO substrate using PECVD. (e)-(i) Surface morphologies measured using FE-SEM after a growth time of 2, 4, 6, 8, and 10 min, respectively. (j) Cross section SEM image of the graphite films on the a-IGZO substrate synthesized using PECVD after a growth time of 10 min.

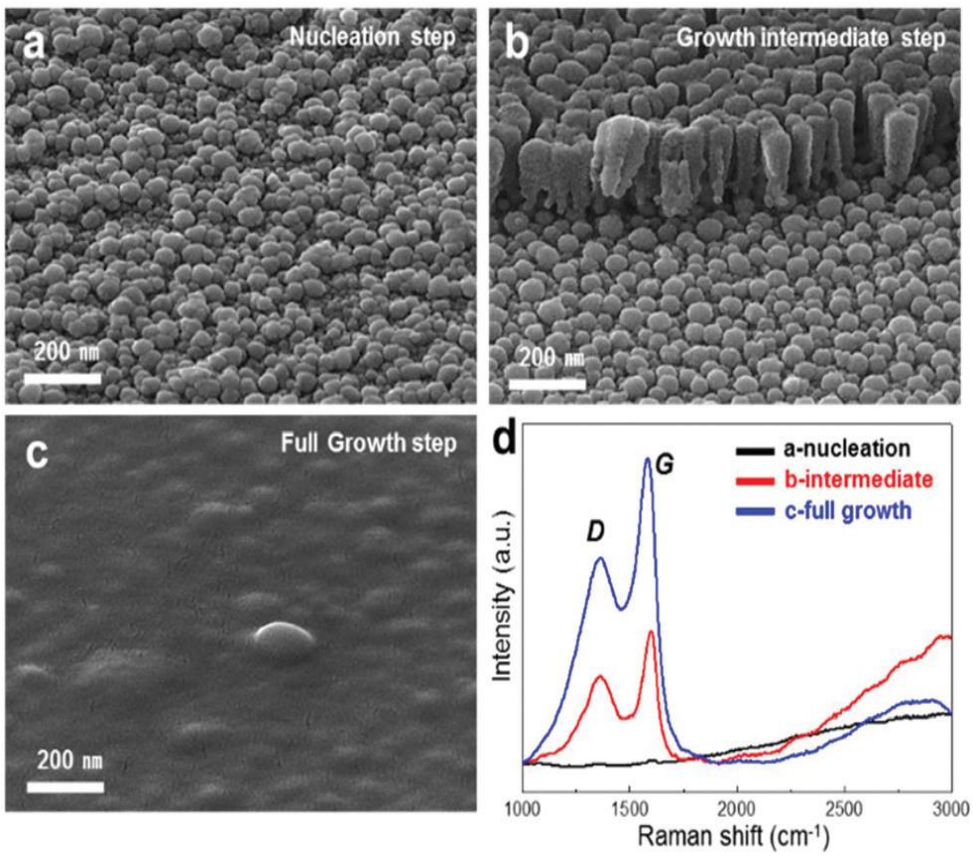

Figure 10. SEM image and Raman spectra of graphite growth process.

(a)-(c) SEM images of the graphite layers on an a-IGZO substrate according to growth step. (d) Raman spectra of each growth step: (a) nucleation step (black), (b) growth intermediate step (red), and (c) full growth step (blue), respectively.

To verify the quality of the graphite layers, Raman spectroscopy was investigated at each growth step of the graphite layers on the a-IGZO substrate, as shown in Figure 10. The Raman spectra consist of two intensive peaks: G and D peaks. The G peak at 1580 cm^{-1} comes from the doubly degenerate zone, the so called E_{2g} mode, and the D peak at 1350 cm^{-1} is due to the defects in the graphite layers. [39] At the nucleation step, no strong peaks appear, which indicates that amorphous carbon layers are formed on the substrate. This is matched well with the randomly grown seeds on the a-IGZO substrate in the above SEM image at the initial growth stage. However, a significant change in the shape and intensity appeared after 6 min, representing that graphite layers have begun to form on the a-IGZO substrate. After 10 min, the ID/IG ratio of the fully grown graphite film (blue line) is decreased compared to that of intermediate step (ESI Fig. 2†). These results demonstrate that high-quality graphite layers with low defects are synthesized on the a-IGZO substrate.

To develop uniform graphite films with superior conductivity, a hydrogen (H_2) plasma process on the a-IGZO substrate was introduced to engineer the surface properties. The a-IGZO substrate

was treated with H2 plasma at 700 mTorr for 300s. Previous reports[40–42] show that hydrogen plasma treatment effectively reduces the oxygen vacancies in the a–IGZO substrate and could induce passivation effects. Hydrogen acts as a donor in the a–IGZO substrate and increases the carrier concentrations.[43,44] Therefore, the interaction between hydrogen and oxygen could affect the reduction of the interfacial trap density and numbers in the a–IGZO substrates. The chemical bonding states of bare a–IGZO and hydrogen plasma treated a–IGZO (H_2–IGZO) were characterized using X–ray photoelectron spectroscopy (XPS), as shown in Fig. 11a and b. The O 1s spectrum of the a–IGZO substrate without H_2 plasma treatment is de–convoluted into two peaks. The peaks at 529.8 eV and 531.6 eV are assigned to O_2 ions surrounded by In, Zn, and Ga atoms in the a–IGZO compound and to O_2 ions in oxygen– deficient regions, respectively. However, the O 1s spectrum of H_2–IGZO in Fig. 3b is de–convoluted into three characteristic peaks with different intensity ratios at 529.8 eV, 531.6 eV, and 532.8 eV. The peak located at around 532.8 eV was attributed to surface oxygen species. The O 1s spectrum of H_2–IGZO shows that the intensity of O_2 ions weakly decreases, while the hydroxyl group (OH) at 532.8

eV noticeably appears because of the interaction between reactive hydrogen and oxygen binding to metal ions. [45~47]

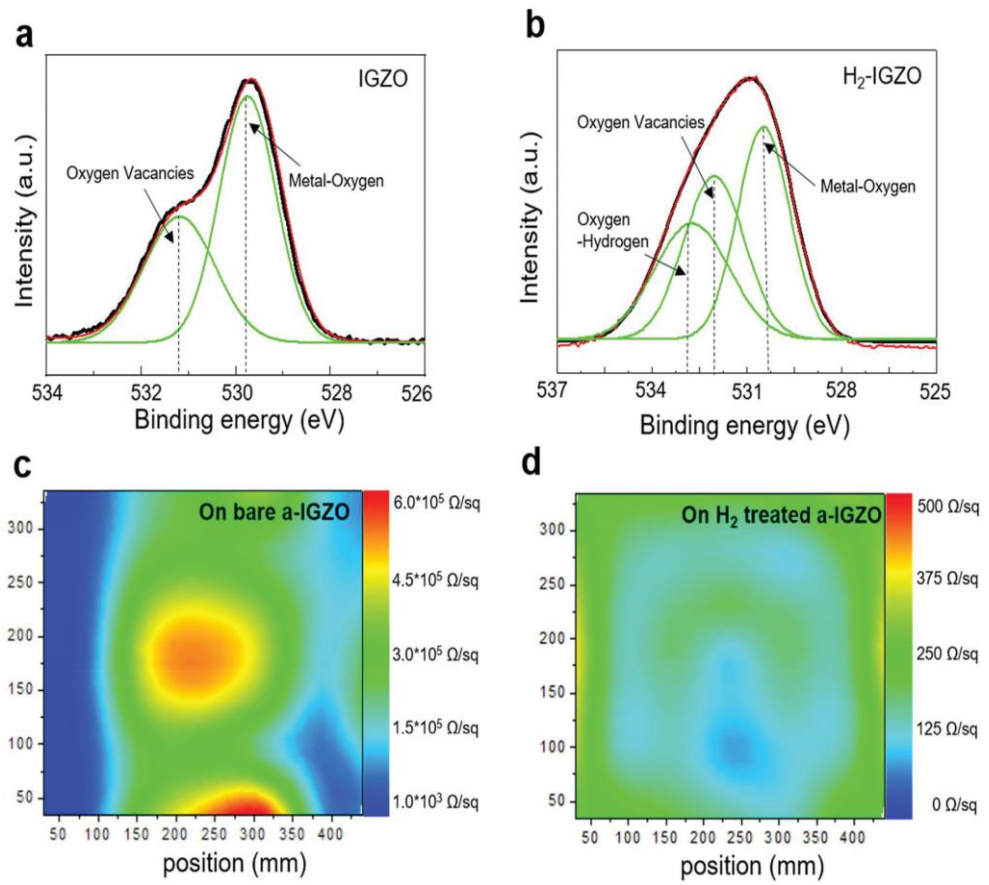

Figure 11. Comparison of treatment with and without hydrogen on a-IGZO.

XPS of the O 1s core level of (a) bare a-IGZO substrate and (b) hydrogen treated a-IGZO substrate. Sheet resistance mapping of the graphite films on (c) the bare a-IGZO substrate and (d) the hydrogen plasma pre-treated a-IGZO substrate.

To verify the effect of hydrogen plasma on electrical properties, we measured surface sheet resistance. Figure 11c and d show the mapping of the sheet resistance distribution measured using a 4 point probe over a large-sized graphite/a-IGZO/glass substrate with/without hydrogen treatment, respectively. The graphite/H_2-IGZO film exhibits very low resistance in the middle (blue) and moderate low resistance (green) at the edges, as shown in Figure 11d. This indicates the significantly uniform and low sheet resistance (1.89×10^2 Ohm/sq) over the large area, while the graphite films without plasma treatment exhibit 3 orders of magnitude higher sheet resistance and various colors indicating inhomogeneous resistance. Refer to Table 2 to compare H_2 plasma treatment and without H_2 plasma treatment. These results support the fact that H_2 plasma on the a-IGZO substrate before graphite layer synthesis plays a key role in developing superior conductive graphite/a-IGZO films. To confirm a possibility for solid-diffusion barrier application, we fabricated a-IGZO TFTs. Figure 12a shows a schematic illustration of the a-IGZO TFT structure, which has graphite barrier films directly synthesized on the a-IGZO substrate. Conventional polymer assisted wet transfer processes to cause other impurities or liquid

trapping between the graphene films and a-IGZO. As a result, the metal oxide inevitably has surface oxidation and eventually brings about efficiency degradation.

	Pretreatment H_2	
R_s	H_2 (With)	H_2 (Without)
Average (ohm/sq)	1.89E+02	2.07E+05
Maximum	4.23E+02	6.43E+05
Minimum	9.02E+01	7.91E+01
Range	3.32E+02	6.43E+05
Deviation	7.01E+01	1.71E+05
Uniformity (%)	64.82	99.98

Table 2. Sheet resistance mapping of the graphite films to compare H_2 plasma treatment and without H_2 plasma treatment.

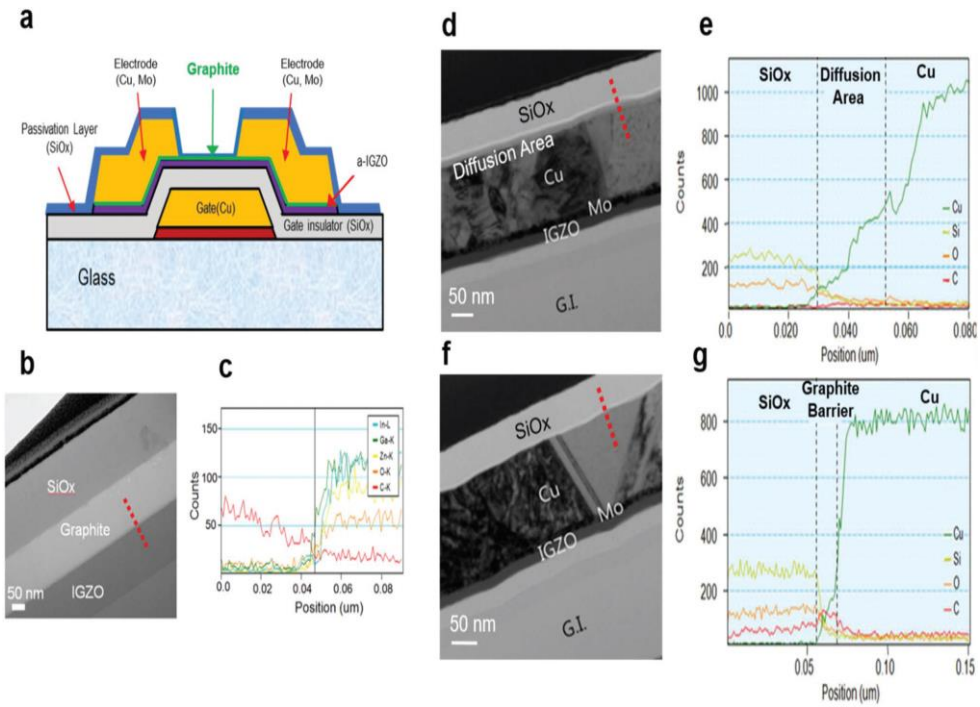

Figure 12. Illustration of TFT backplane application and analysis.

(a) Illustration of the a-IGZO TFT structure. (b) A cross-section SEM image and (c) EDS spectrum measured at the red line profile in (b) at the channel area. (d) A cross-section SEM image and (e) the EDS spectrum measured at the red line profile in (d) at the electrode area without the graphite barrier. (f) A cross-section SEM image. (g) EDS spectrum measured at the red line profile in (f) at the electrode area with the graphite barrier.

Therefore, direct graphite growth on a-IGZO could also passivate the a-IGZO from conventional oxidation. To demonstrate the passivation effect, we analyzed energy dispersive X-ray spectroscopy (EDS) results through FE-SEM. Figure 12b shows a cross-section SEM image of the a-IGZO thin film TFTs. The graphite films were placed between a-IGZO and conventional silicon oxide buffer layers. Silicon oxide films were deposited subsequently on the graphite layers using the PECVD system. Figure 12c exhibits the EDS spectrum measured at the red line in Figure 12b. As shown in the SEM image and EDS spectrum, there is no considerable change in a-IGZO films compared with data in ref. 48. This result proves that the direct graphite synthesis on a-IGZO could prevent unnecessary oxidation of metal oxide. To further analyze barrier characteristics, we also performed graphite synthesis on the Mo/Cu electrodes using the same synthesis method. Since SiO_x passivation layers are deposited using PECVD at 370 ° C, the copper electrode migrates and forms diffusion layers without any barrier films, as shown in Figure 12d and e. On the other hand, a considerable amount of copper diffusion is prevented by graphite films, which could play a

key role as a solid-diffusion layer at not only channel layers but also at electrode layers.

Currently, there are several methods for fabrication of graphene that vary in scale, structural consistency, the simplicity of fabrication, and cost including. Chemical Vapor Deposition (CVD) is an attractive approach to fabricate graphene in mass production due to its capability of producing large area deposition. In the other way of fabrication, transferred graphene sheet, we obtain weaker adhesion in the contact of metal layer throughout adhesion tests compared to CVD method. In the aspect of large-scale graphene growth, it is considered that the adoption of CVD is the right way for growth methods. We conducted low-temperature graphene growth with CVD to utilize glass substrate, which used in LCD display. We conducted CVD using plasma enhanced methods at ambient pressure with argon, hydrogen, and acetylene gas flows.

We evaluate Cu metal which plays the role of catalyst in Graphene CVD method and also S/D metal electrode. This catalytic effect of Cu is explained by the self-limiting mechanism due to very low carbon solubility in Cu (~0.03 atom % at 1000° C). [49] The substrate is placed in a gas delivery chamber and flows carbon based

source downstream to the metal electrode patterned glass-substrate. It is normally known that carbon is firstly adsorbed into the metal surface at high temperature, and then precipitated out during the cooling down to room temperature due to the lowest free energy state of graphene. To find out the condition of low temperature processing for graphene growth, main process temperature of graphene splits into 200℃ and 350℃ after deposition of 0.5 ㎛ Cu electrode. On the condition of low temperature, various conditions were tested to prevent the Cu diffusion to active layers. In the Figure 13, TEM (Transmission electron microscope) analysis was carried out to define the cross-sectional structure of the layers. Figure 13(a) shows the graphite layer on Cu surface and main multi-layer graphene growth process was conducted at 200℃. As indicated in the images Cu diffusion into SiO_x was happened. Meanwhile, Multi-layer graphene growth of main process temperature performed at 350℃ does not show Cu diffusion territory. We can assure that graphene layers can be a Cu diffusion barrier. Various growth parameters were verified to determine the optimal fabrication condition for graphene growth. We can estimate the help of plasma enhanced is possible to graphene growth at low temperature of 350℃. Also we can guess

250℃ process is not sp^2 hybridization. Carbon bonding remains amorphous states.

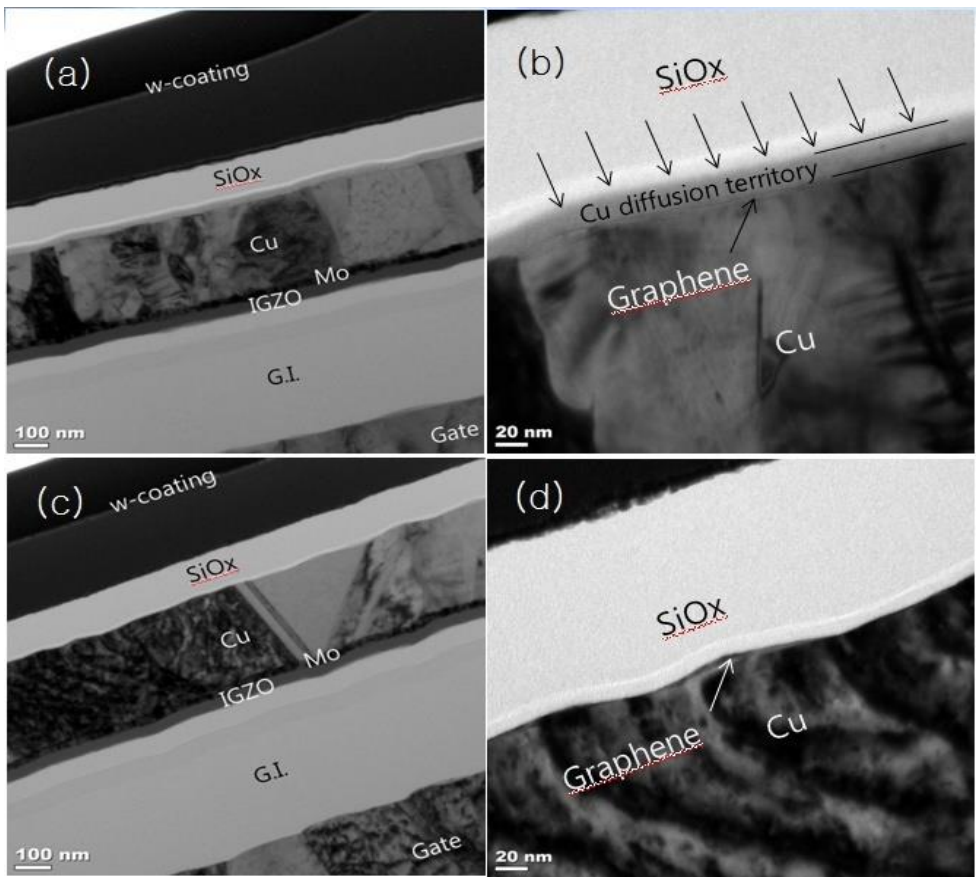

Figure 13. Comparison with different temperature synthesis of graphitic layers. (a) PECVD process temperature at 200℃, (b) is a magnification of figure (a), (c) PECVD Process temperature at 350℃, (d) is a magnification of figure (c).

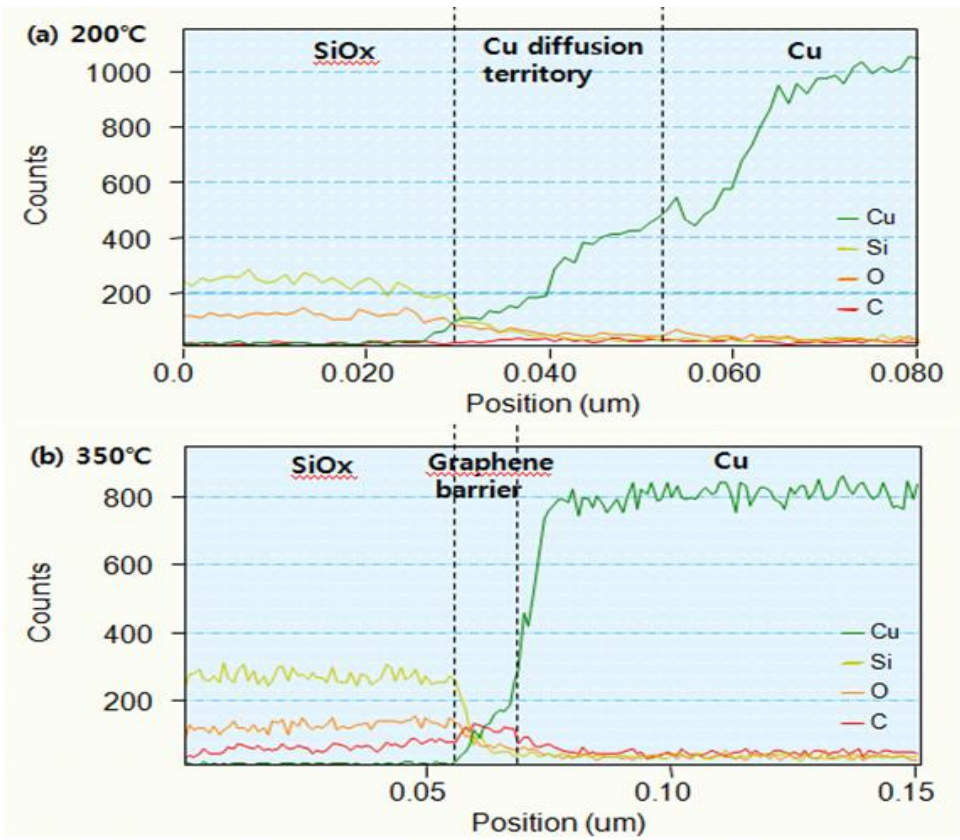

Figure 14. EDX Analysis with different temperature synthesis of graphitic layers. EDX analysis of PECVD synthesis condition (a) Process temperature 200℃, (b) Process temperature 350℃

EDX (Energy Dispersive X-ray spectrometer) Data shows Cu diffusion in Figure 14 (a) graphene grown at 200℃, but Figure 14(b) performed temperature at 350℃ is well blocking Cu diffusion. Also, throughout Comparison of two graphs, we can certain Graphene of (b) graph plays well Cu diffusion barrier role.

Figure 15 shows the results of adhesion test between a-IGZO and graphite layer. The adhesion property is one of the important factors in the device fabrication process. The adhesion test was performed using the scotch tape, and it was graded by observing the conditions of peeling-off states. Figure 15 (a) shows the Cu (Copper) metal deposited on top of a-IGZO as reference data, on the other hand, (b) shows that the Cu metal was deposited on the surface of graphite growth on a-IGZO material. And then draw a line with a knife on the top with 6 * 6 lines. Then stick it to the top surface with scotch tape and remove it. The scotch tape was used to check the adhesion between the metal and graphite layer. In this experiment, no peeling-off of metal from the graphite was observed, meaning that it showed the superior adhesion behavior and can be beneficial in the application for the fabrication of device.

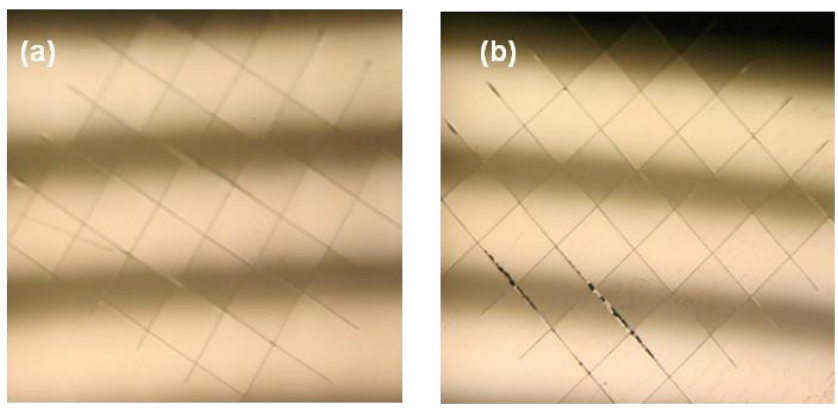

Figure 15. Results of peel off test using scotch tape. (a) The copper metal deposited on top of a-IGZO as reference data (b) The Cu metal was deposited on the surface of graphite growth on a-IGZO material.

2.1.4. Conclusion

Amorphous indium-gallium-zinc oxide (a-IGZO) thin-film transistors (TFTs) have been under in-depth research as one of the promising solution for active matrix flat-panel displays. However, the solid diffusion of a-IGZO to other layers during TFT device fabrication cause high degradation of electrical and optical properties. Thus, it is expected that graphitic materials diffusion-impenetrable properties can be utilized as diffusion barriers. A conventional transfer method and direct growth on TFTs with high temperature are limited due to wet transfer conditions and low T_g (~540 ° C) of the glass substrates, respectively. Here we report the large-scale transfer-free growth of thin graphite films at low temperature (~350 ° C) for solid diffusion barriers in the a-IGZO TFTs using plasma enhanced chemical vapor deposition (PECVD), which can be widely used to protect solid-diffusion for sustainable and scalable future industrial technology.

To monitor the entire uniformity on the glass, at least 49 points of sheer resistance were measured and R_s was mapped over the glass substrate. The R_s of graphite film is 1.89E+02(ohm/sq) at the average of 49 points in 370x470 mm glass size. Also, regarding the

plasma treatment, the graphite films with H_2 plasma pre-treatment shows the improved uniformity from 99.98% to 65.38%. This can be attributed to the interaction between a-IGZO layer and H_2 atoms. The taping test is performed to check the adhesion of graphite layer grown on a-IGZO. The superior adhesion indicate that it has been applied on the device fabrication. From then on, it creates a path for graphite layer growth on a-IGZO and copper materials can be well applied in the next generation of electronic devices.

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Chapter 3. Growth of silicon germanium films for photo-blocking layers in industrial display

3.1. Silicon germanium photo-blocking layers for a-IGZO based industrial display

3.1.1. Introduction

The amorphous-indium-gallium-zinc-oxide (a-IGZO) thin-film transistors (TFTs) electrical instability behaviors under ultraviolet (UV) illumination are studied. As UV radiation dosage increases, the when the voltage is turned on the TFT shows continuous negative shift, which is accompanied by enhanced degradation of sub-threshold swing and field-effect mobility. The electrical instability is due to an increase in the concentration of the carrier and defects within the device channel that can be further attributed to additional oxygen vacancy generation and ionization related defects upon UV illumination, respectively.[1]

In order to suppress the reactivity of a-IGZO light as described above, a SiGe (Silicon Germanium) thin film is deposited on the lower layer of a-IGZO to investigate whether the light is blocked. SiGe has

been studied and used as a light absorbing layer in the field of solar cells.

Unlike a crystalline silicon solar cell having a P-type-N junction structure doped with impurities, a solar cell using an amorphous and nanocrystalline silicon thin film has a P-I (intrinsic layer) -N-type structure. The carrier generated from the crystalline silicon does not require additional energy for carrier collection because the diffusion length of the minority carriers is larger than the thickness of the substrate. On the other hand, in the case of amorphous or nanocrystalline silicon thin film, the diffusion distance of the carrier is much lower than that of the crystalline silicon substrate, so that the efficiency of collecting electron-hole pairs produced by the light is very low when manufactured with the p-n structure. Therefore, it has an intrinsic layer structure in which impurities are not added, thereby improving the collection efficiency. In this study, SiGe is used as an intrinsic layer, and studies have been made on the difference of optical absorption by the PECVD method according to the change of the gas flow of Germanium. According to a report that as the gas flow rate of Germanium increases, the energy band gap

(E_g) reduces, so that more energy photons of the sunlight enters the light absorbing layer to form a relatively larger number of carriers.

In this study, the stability of the driving device is by controlling SiGe as a thin film in a display device, not controlling the gas amount of Germanium, so that the IGZO thin film is not optically oriented.

As a panel size has been changed to large-scale screen size in the active-matrix flat panel displays, many researchers have investigated in transparent metal oxide semiconductors instead of amorphous silicon because of their high mobility and low synthesis temperature (~250 ℃).[2-4] In particular, amorphous indium-gallium-zinc oxide (a-IGZO) have been suggested for a future active material, which shows superior charge mobility and threshold gate swing (~0.083 V/decade).[5] In addition, a-IGZO based thin film transistors (TFTs) have attracted more attention due to its transparent optical properties and convenient synthesis methods at low temperature with reasonable cost.[6]

In the display industry, the top gate TFT method has been widely used for the process architecture to create liquid crystal display (LCD) and organic light emitting diode (OLED).[7,8] Top gate method has an advantage to increase an aspect ratio compared to the bottom

gate method.[9,10] However, in case of top gate method, it could not avoid that a-IGZO reacts with the light leakage originated from backlight in LCD display.[11,12] IGZO has been known that the optical bandgap is E_g = 3.2 eV, which indicates that it could be activated on the condition of UV wavelength less than 400 nm.[13,14] Through the inevitable reaction with UV range in light leakage, the electrical properties and reliability tests for long term panel displays show considerable degradation of the performance.[15] The attributions to degradation of the electrical properties are trapping of holes created by photo-generation and instability in the interface between a-IGZO and dielectric materials.[16]

Recently, a few research groups have focused on metal based photo blocking layers for a-IGZO films.[17-19] Although the metal based photo blocking layers prevent the reaction of a-IGZO films from the backlight, the performance of the a-IGZO TFTs is decreased due to the increased cap size between metal and IGZO. In addition, the high power consumption is also needed to increase the brightness of a backlight for the purpose of keeping the brightness of screen.[20,21] Therefore, the demand for the photo blocking layers

composed of new materials different from conventional metal layers is continuously raised in display industry.

In this study, we suggest the silicon-germanium (Si-Ge) films as the photo-blocking layers in a-IGZO based TFTs. According to preceding research, ultraviolet (UV) absorbance is increased in the Si-Ge alloy which have more Ge ratio than Si ratio.[22] However, the difference of UV absorbance depending on components ratio is not enough to satisfy the absorbance condition for a photo blocking layer. In order to find better results, we controlled the thickness of the Si-Ge films which have fixed component ratio (Si:Ge = 1:1). It was found that TFTs with Si-Ge photo blocking layers preserved the initial value including mobility and threshold voltage (V_{th}) without any oxidation or chemical damages under the light illumination.

3.1.2. Experimental

Synthesis. Using plasma enhanced chemical vapour deposition (PECVD), the 100 nm SiO_2 layers were deposited on a glass substrate for the efficient synthesis of the Si–Ge films. The SiO_2/glass substrate was placed on a quartz flat inside of 4–inch quartz tube. The Si–Ge films were synthesized on SiO_2/glass substrates through the PECVD method, using silane (10 sccm) and germane (10 sccm) with vacuum pumping at 370 ℃ at initial low vacuum (~25 mTorr). After 5~10 min of direct exposure to the plasma (100 W) at that temperature, a large–area Si–Ge films formed on the SiO2/glass substrate. Then, silicon nitride buffer layers also deposited on the substrate using PECVD with same method above.

Characterization The entire structure was investigated by field–emission scanning electron microscopy (FESEM, AURIGA Carl Zeiss). The crystal phases were collected using an X–ray diffractometer (D8–Advance, Bruker Miller Co.) with Cu Ka1 irradiation. The Raman spectra were obtained by a Raman spectrometer (RM 1000–Invia, Renishaw, 514 nm). Structure

bonding in the structure is analysed by XPS carried out with a KRATOS AXIS-His model in Research Institute of Advanced materials. The electrical properties were measured by Agilent 2602.

3.1.3. Results and Discussion

The Si-Ge films were synthesized on glass substrates coated by silicon oxide by plasma-enhanced chemical vapor deposition (PECVD). Without the silicon oxide, it is difficult to directly grow the Si-Ge films on the glass substrate. Figure 16a shows a schematic illustration of the structure of a-IGZO TFTs passivated by the Si-Ge photo-blocking layers with the top gate and electrode contact. Silicon Nitride buffer layers were deposited on the Si-Ge layers for dielectric materials. The synthesis method is more explained in following experimental synthesis parts. Figure 16b is the side image of the structure of a-IGZO TFTs measured by scanning electron microscopy (SEM). We confirmed that uniform Si-Ge films were placed among the two oxide-based dielectric layers without any external damage to the overall structure.

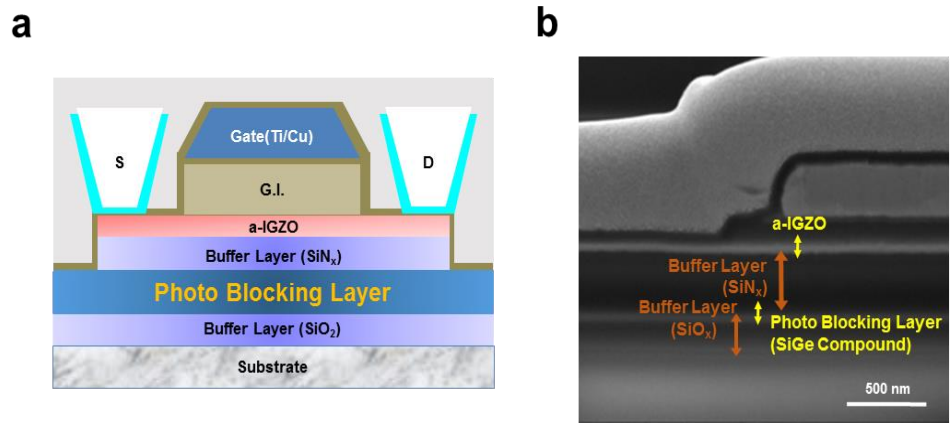

Figure 16. The entire structure of a-IGZO based display passivated by photo blocking layer. (a) Schematic illustration of the Si-Ge photo blocking layer for industrial a-IGZO TFT degradation. (b) Side view SEM image of a-IGZO TFT passivated by the Si-Ge films.

The crystallinity of the Si-Ge films synthesized by PECVD was investigated by X-ray Diffraction (XRD). As shown in Figure 17a, the XRD patterns of the Si-Ge films exhibit conventional cubic phase similar to that of bulk silicon (JCPDS No. 27-1402). Reflections of the Ge phase are imperceptible in the XRD patterns, suggesting that Ge exists as a solid solution. [23]The formation of the Si-Ge bonding is more clearly explained by Raman spectrum as shown in Figure 17b. The Raman peaks at 510, 405 and 295 cm^{-1} from Si-Si, Si-Ge and Ge-Ge bonding, respectively, are observed. In particular, the additional Raman peaks between 420 and 470 cm^{-1}, which are the vibrational modes of Si superlattice, are measured. These vibrational modes which are composed of localized Si-Si optical modes whose frequencies are lowered because of the larger mass of adjacent Ge atoms.[24] X-ray Photoelectron Spectroscopy (XPS) also demonstrates chemical composition and surface oxidation of the Si-Ge films. The Si 2p and the Ge 3d peaks obtained from XPS could be ascribed to elemental Si and Ge, as shown in Figure 2c and 2d. Owing to slight surface oxidation, weak peaks related oxygen are also detected around 101.5 eV at Figure 17c and 33 eV at Figure 18d,

respectively. These characterizations summarize that the elemental phases are originated from Si and Ge elements and their bonding.

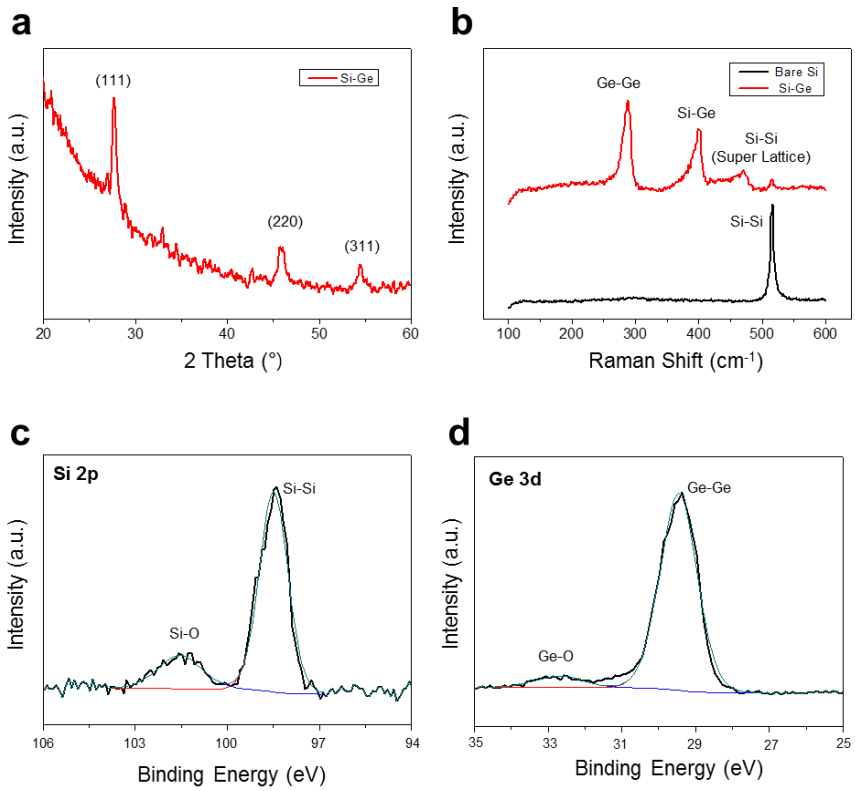

Figure 17. Material characterization of the Si-Ge photo blocking layers.

(a) XRD patterns of the Si-Ge films. (b) Raman spectra of the Si-Ge photo blocking layers compared with a bulk Si. XPS spectra of the Si-Ge films showing signals of (c) Si 2p and (d) Ge 3d.

Figure 18a shows the Ultraviolet-Visible (UV-Vis) spectrum according to the thickness of the Si-Ge compounds. The UV absorbance peak was gradually shifted in which direction increasing the thickness of Si-Ge layers according to the equation above. In particular, we confirmed the UV absorbance at 450 nm more detail, which the a-IGZO react with actively (Figure 18b).[25] Photo blocking effect is also proportional to the thickness like as another wavelength. Therefore, it is clear that the higher thickness of Si-Ge compounds has good blocking effects, thereby offering a possibility for superior photo blocking layers in a-IGZO based displays.

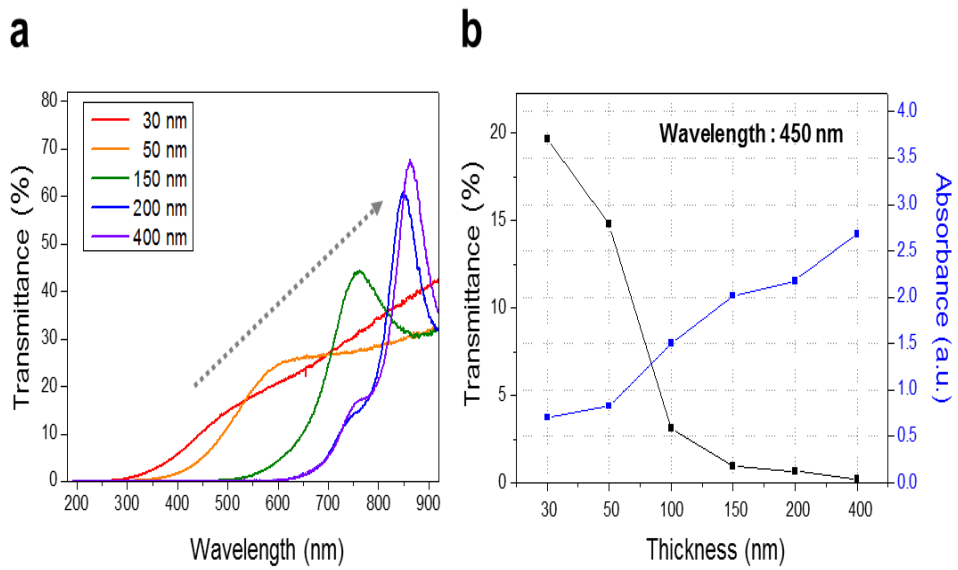

Figure 18. UV-Vis spectrum analysis of the Si-Ge films. (a) UV-Vis spectrum according to the thickness of the Si-Ge films. (b) UV absorbance of the Si-Ge films at 450 nm.

Although the higher thickness of the Si-Ge films has outstanding UV absorbance, the electrical superiority is inversely proportional to the thickness. Figure 19a shows the threshold voltage (V_{th}) is negatively shifted depending on the thickness of the Si-Ge films at dielectric buffer layers 300 nm. Furthermore, Si-Ge film thickness can be observed at 50nm, 100nm and 200nm under SEM images in Figure 20. The more charge carrier density, so called free electrons, are accumulated in the Si-Ge films as the thickness of the Si-Ge films is increased. The accumulated electrons make the Si-Ge films more conductive, thus making it a kind of capacitance with a-IGZO. Eventually this accumulated charge carriers cause the a-IGZO channel to shut off while generating tunnelling effects to the Si-Ge layers. Therefore, we optimize the thickness of Si-Ge compounds without any tunnelling effects. In addition, the thickness of the silicon nitride buffer layers could also give rise to the performance of the a-IGZO TFTs. as shown in Figure 19. Moreover, the dielectric buffer layers at 100nm and 300nm are depicted in Figure 21. The more deposition of dielectric materials results in the improved efficiency of TFTs due to the decrease in capacitance.[26,27] However, too high thickness of buffer layers lead to surface instability, which makes

post processes to fabricate the TFTs very difficult. Hence, we selected the heights of the Si-Ge films and the silicon nitride buffer layers to 300 nm and 200 nm, respectively for achieving maximum TFT efficiency. Figure 19c shows the evolution of the transfer curves (drain current versus gate voltage) as a function of light illumination time. The a-IGZO TFTs show very good electrical properties with mobility above 10 $cm^2V^{-1}s^{-1}$ and on/off ratio of ~ 10^8 under darkness condition. Upon the exposure of the a-IGZO TFTs to light illumination, the V_{th} is negatively shifted (>10 V). In contrast, the a-IGZO TFTs passivated by the Si-Ge photo blocking layers show no change in electrical properties during the light illumination, as shown in Figure 19d. This result suggests a superior possibility of the Si-Ge films as a photo blocking layers for the a-IGZO based industrial display field under light illumination.

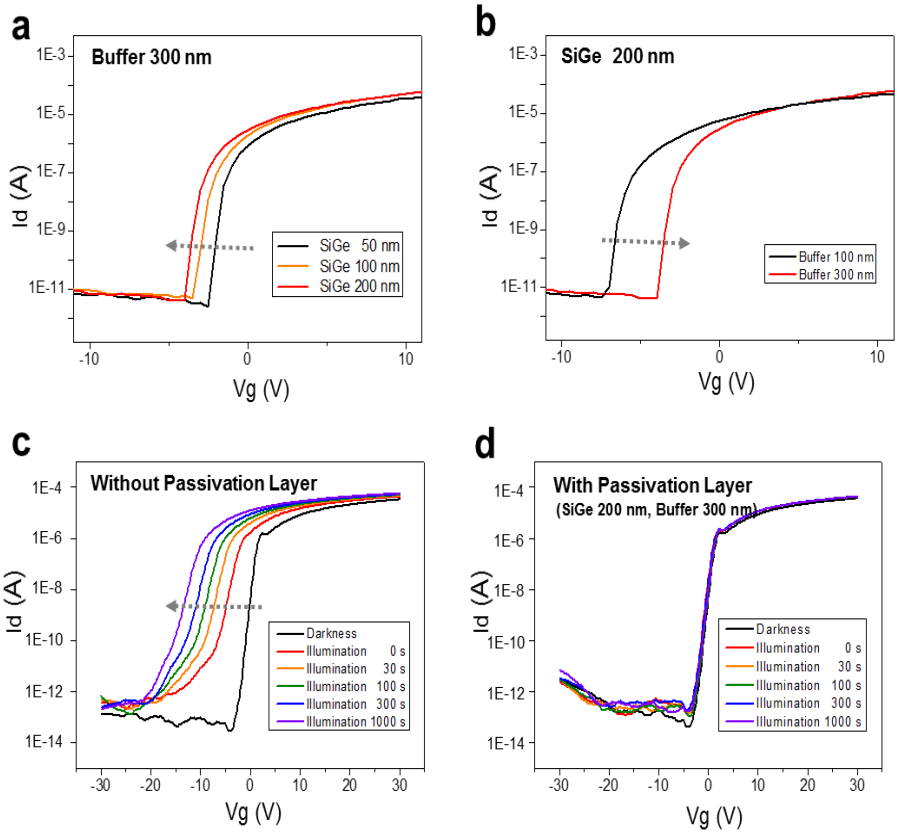

Figure 19. Electrical characteristics of the a-IGZO TFTs.

(a) Transfer Characteristics depending on the thickness of the Si-Ge films at dielectric buffer layers 300 nm. (b) Transfer Characteristics depending on the thickness of the dielectric buffer layers at the Si-Ge films 200 nm. Representative electrical properties of a-IGZO TFTs (c) without and (d) with the Si-Ge based photo blocking layers.

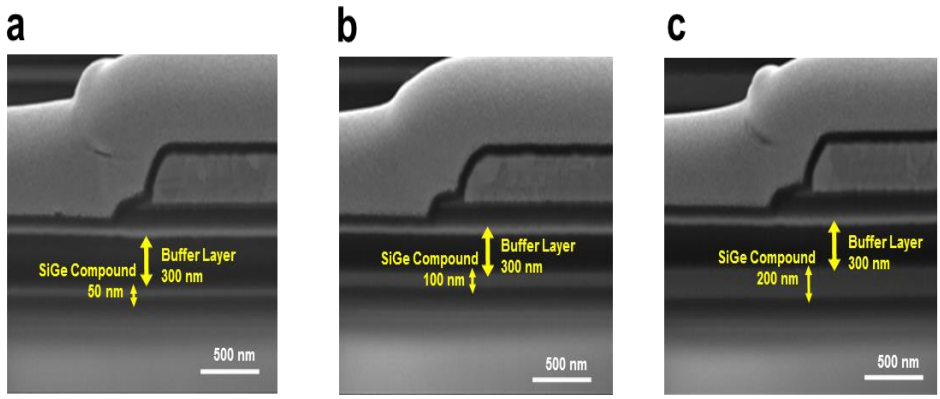

Figure 20. Side view SEM images of a-IGZO TFT at dielectric buffer layers 300 nm. (a) The Si-Ge films 50 nm TFTs. (b) The Si-Ge films 100 nm TFTs. (c) The Si-Ge films 200 nm TFTs.

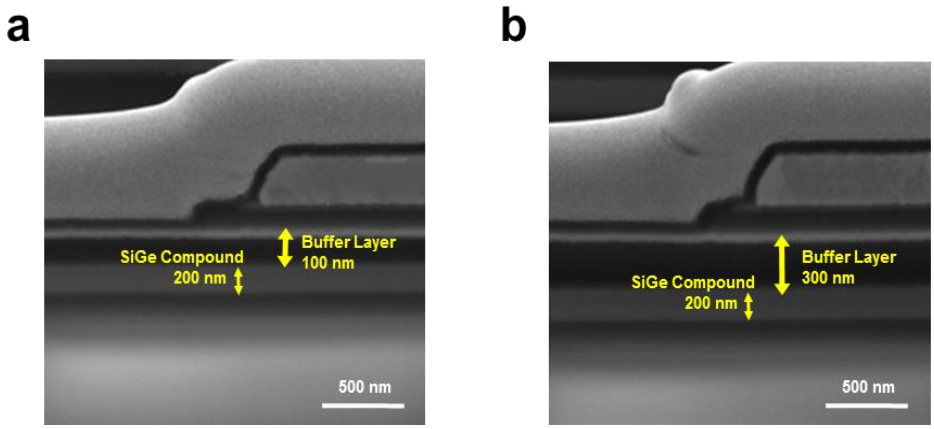

Figure 21. Side view SEM images of a-IGZO TFT at the Si-Ge films 200 nm. (a) The dielectric buffer layers 100 nm. (b) The dielectric buffer layers 300 nm.

When photo-induced transition from neutral oxygen vacancies (V_o) to singly ionized oxygen vacancies (V_o^+) by light illumination, photo-excited electrons from the high-density occupied V_o states near valence band maximum would increase average carrier density the percolation conduction through distributed potential barriers around the conduction band edge.[28] This phenomena could explain the increase of the electron mobility with light illumination. Below indicates an illustration of summarized mechanism in Figure 22.

In order to obtain more information about electrical properties on the a-IGZO TFTs passivated by the Si-Ge photo-blocking layers, the effect of light stress time on the change of V_{th} and electron mobility was investigated in detail. The V_{th} changes without and with the Si-Ge passivation layer to the light illumination condition are compared, as shown in Figure 23a. By applying 10 V gate voltage, V_{th} of pristine a-IGZO is largely negatively shifted (~15 V at 1000 sec) in the direction with increasing the light stress time, while that of the Si-Ge passivated a-IGZO persists similar value compared with initial value. Furthermore, the electron mobility of the a-IGZO TFTs passivated by the Si-Ge layers shows no change under the light stress time, as shown in Figure 23b. Therefore, the V_{th} shift and

electron mobility are greatly dependent on the existence of the Si-Ge photo-blocking layers.

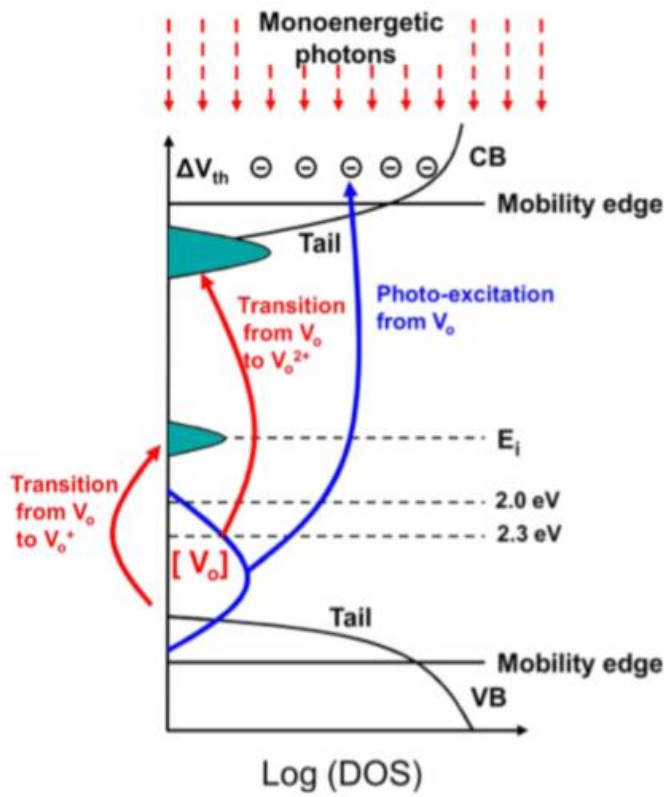

Figure 22. Schematic illustration of the electron transfer process in a-IGZO by light illumination.[28]

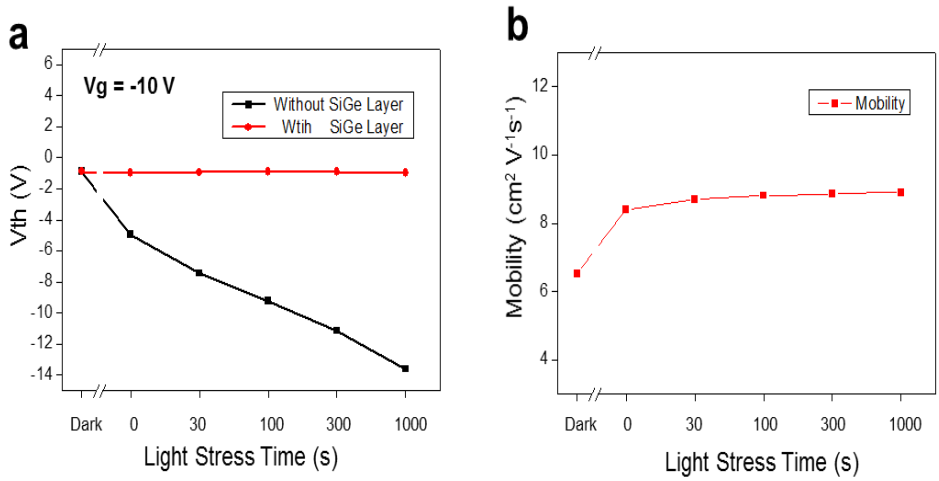

Figure 23. V_{th} and mobility of a-IGZO TFTs passivated by the Si-Ge films depending on the light stress time. (a) V_{th} change of a-IGZO TFTs passivated by the Si-Ge photo-blocking layers as a function of the light illumination compared with pristine a-IGZO. (b) Electron mobility change of a-IGZO TFTs passivated by the Si-Ge photo-blocking layers depending on light stress time.

We synthesized the Si-Ge films by PECVD and investigated the effects of the photo blocking Si-Ge layers on the electrical properties of a-IGZO semiconductors. Although the thicker Si-Ge films show stronger the light absorbance, the electrical performance of a-IGZO TFTs is inversely proportional to the thickness of the Si-Ge films because of accumulated free electrons. The thickness of the dielectric buffer layers changes the charge capacitance and surface instability of the TFTs, which also considerably affects the device performance. Therefore, we optimize the thicknesses of the Si-Ge films (~200 nm) and the buffer layers (~300 nm). After up to 1,000 s exposure to light, the V_{th} and electron mobility of the a-IGZO TFTs passivated by the Si-Ge photo-blocking layers were unchanged. Considering the simple fabrication process by PECVD with outstanding scalability, we expect that this method can be widely applied to various metal-oxide TFT devices that are sensitive to light illumination.

3.1.4. Conclusion

Amorphous indium- gallium-zinc oxide (a-IGZO) has been assiduously studied for the application to active matrix flat-panel display that has superior electrical and optical properties. Nevertheless, a-IGZO characteristics were found to be very sensitive to external circumstance. For instance in light illumination it dramatically degrades the device performance and stability required for display applications. Here, we suggest the use for silicon-germanium (Si-Ge) films grown plasma-enhanced chemical vapour deposition (PECVD) as photo-blocking layers in the a-IGZO thin film transistors (TFTs). The charge mobility and threshold voltage (V_{th}) of the TFTs depend on the thickness of the Si-Ge films and dielectric buffer layers (SiN_X), which were carefully optimized to be ~200nm and ~300nm, respectively. As a result, even after 1,000 s illumination time, the V_{th} and electron mobility of the TFTs remain unchanged, which was enabled by the photo-blocking effect of the Si-Ge layers for a-IGZO films. We demonstrated that the thicker Si-Ge films shows stronger the light absorbance. However, the electrical performance of a-IGZO TFTs is inversely proportional to the thickness of the Si-Ge films. This is because when the Si-Ge

films thicken, the charge density from accumulated electron increase and become more conductive, thus making it a kind of increased cap size with a-IGZO, which degrades the performance of a-IGZO. Eventually, the a-IGZO is shut off because of thick Si-Ge films. Therefore, we optimized the Si-Ge films and buffer layers thickness. Considering the simple fabrication process by PECVD with outstanding scalability, we expect that this method can be widely applied to TFT devices that are sensitive to light illumination.

3.1.5. References

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초 록

플라즈마 화학 기상 증착법을 이용한 베리어 필름 합성과 디스플레이 응용

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자발광형 디스플레이이며, 저전압 구동이 가능하고 얇은 두께로 제작이 가능하며 동작속도가 매우 빠를 뿐만 아니라 높은 해상도 구현이 가능한 OLED 는 디스플레이에서 빠른 성장세를 보이고 있다. 최근 OLED 의 가장 큰 관심 분야는 모바일용 디스플레이와 대면적 TV, 그리고 플렉시블 및 투명 디스플레이 구현이다. 디스플레이를 구동하기 위한 구동소자는 수동형(passive matrix)과 능동형(active matrix, AM)로 나뉘며, 수동형에 비하여 고화질, 낮은 소비 전력, 대형화에 유리한 능동형 디스플레이가 선호된다. 표시소자를 능동 구동하기 위해서는 각 화소마다 박막 트랜지스터(thin-film transistor, TFT)와 같은 스위칭 소자를 부착시켜야 한다. 능동형 구동소자의 경우 현재의

TFT-LCD 나 AMOLED 용 백플레인에 주로 사용되는 비정질 실리콘(a-Si), 저온 다결정 실리콘 (LTPS) 기술이 우선 개발되어 응용되고 있다.

최근에는 큰 밴드 갭을 가지는 비정질 산화물 반도체를 이용해 투명하면서 빠른 응답속도의 디스플레이 구동소자에 대한 연구가 활발히 진행되고 있다. 또한 배선의 RC Delay 를 최소화 시켜야 하고, 파워소비량을 줄여야 하는 기술적인 문제가 있다.

디스플레이의 고해상도인 UHD (Ultra High Definition)의 backplane 에서 고속 TFT 구현을 위하여 SD(Source-Drain) 메탈 배선 구현은 필수적인 요소이다. 본 연구에서는 SD 메탈 배선으로써 저저항 배선인 Copper 배선의 diffusion barrier 역할을 하는 Graphite 성장을 다루고 있다. 기존의 Graphene 합성은 기계적 및 화학적 박리 방법에는 대면적 패널 구현으로써 한계가 있다. 현재까지 대형 Size scale Graphene 시도는 전극으로써 Graphene 활용은 있지만, 이 구현은 Thermal CVD (900~1000℃)에서 Graphene 을 합성하고, Glass 에 transfer 한 논문으로써 실제 대면적으로 만드는 공정 적용에는 한계가 있다. 이에 현재 많이 연구는 진행 중이고 있지만, PECVD (Plasma Enhanced Chemical Vapor Deposition)를 이용한 graphite 박막 합성은 대형 size, mass production 을 가능하게 하며, 아직 mass production 적용을 위해 연구해야 할 점은 많지만, 저온

공정 Graphite 합성이 가능하다면, large scale device 구현에 한층 더 진보된 기술이 될 것임을 확신한다. 본 연구에서 Copper diffusion barrier 으로써의 역할을 검증하고, 증착 온도를 저온으로 합성함으로써 TEM 및 EDAX 분석으로 Graphite barrier 및 mass production 의 가능성을 검증하였다. 본 연구의 직접적인 PECVD 합성 방법을 통해 대면적이 가능함을 제시함으로써 기존의 대면적 합성 문제점을 해결해 줄 수 있는 방안이 될 것이다.

또한 디스플레이의 TFT 특성도 기존의 Active material 인 a-Si TFT 보다 훨씬 더 높은 고이동도 소자를 요구하며, 특히 투명 디스플레이의 적용 가능하며, 고이동도 특성을 균일하게 가질 수 있는 신규 TFT 를 요구하게 되었다. 이에 대한 방안으로 산화물 TFT 로써 ZnO (Zinc Oxide), IZO (Indium Zinc Oxide), a-IGZO (Amorphous Indium Gallium Zinc Oxide) 등의 재료가 연구되고 있다. 기존의 a-Si 의 이동도 ($<1cm^2/V \cdot S$) 보다 높은 이동도를 가진 IGZO 재료는 투명한 소자로써 투명디스플레이에서도 활용이 가능하여, 응용성을 확대하고 있다. 본 연구에서는 투명디스플레이 에서도 활용이 가능하도록 a-IGZO를 substrate로 하는 Graphite 박막을 합성 방법을 제시하고, 대면적 구현으로써 그 응용성을 기대하고 있다.

Graphite 의 저온 합성 기술 개발은 기존 라인의 CVD 장비 교체 없이 단지 Graphene Gas 사용만으로 공정을 구현한다는 점이 cost 및

공정 단순화의 관점에서 많은 장점이 있다. 또한 고속 구동을 위하여 SD 배선으로 metal 뿐 아니라 산화물 반도체로도 Graphite 합성의 catalyst 로써 사용되어, 패널 구현을 가능하게 해준다는 관점에서 의미가 있다. 또한 Graphite 합성 기술을 thin film 박막을 만들어 다른 application 에서도 활용 가능함을 보여줌으로써 파급 효과가 크다고 판단된다.

다음 연구에서는 LCD 디스플레이에서 Backlight 사용이 필수적이다. Back light 는 가시광선 영역 뿐 아니라 UV 파장영역도 포함하고 있으며, Active 재료인 a-IGZO 소자에서 TFT 특성의 불안정성의 문제를 가지고 있다. IGZO 의 특성상 UV 파장대에서의 빛과의 반응으로 TFT 소자의 신뢰성 특성이 악화되는 문제점을 해결하고자 Barrier 박막을 사용이 필수적인 요소이다.

본 연구에서는 TFT 의 신뢰성 및 안정성을 유지하기 위해서 Photo blocking barrier 로써 SiGe (Silicon Germanium) 박막 재료 합성을 통하여 TFT 신뢰성의 특성 변화 없는 것을 연구하였다. 이전 SiGe 연구되어진 바로는 태양전지에서 P-I(intrinsic layer)-N 형 구조에서 중간 삽입층에서 불순물이 첨가되지 않은 무첨가층 (Intrinsic layer)에서 SiGe 이 광흡수층으로 사용되어진 연구가 있었다.

본 연구에서는 TFT 소자에서 a-IGZO 가 광반응으로 인해 산소 결핍 (Oxygen Vacancy)을 막아 TFT 특성의 저하 효과를 막고자

SiGe 의 광 차단 박막 형성을 통해 광반응으로 인한 a-IGZO 특성 변화가 되지 않도록 하였다.

또한 박막 형성 및 적층 구조에서 SiGe 와 IGZO 의 박막 사이에 Capacitance 형성으로 전자의 charge 가 IGZO 박막 계면에 누적되어, 트랜지스터 특성이 단락(short) 현상이 발생 하였으며, 이를 방지하기 위해 Buffer layer 의 두께 조절이 중요하였다. 이에 Buffer layer 의 두께 최적화를 통해 하부에서 들어오는 빛에도 차단을 할 수 있는 Barrier 적층 구조를 만들어 TFT 소자의 신뢰성 개선됨을 보여주고자 하였다.

스마트 Window 및 냉장고에서 문을 열지 않고 내용물을 확인할 수 있는 투명 디스플레이 및 플렉시블 디스플레이 구현을 위해 여러 요소의 기술 연구가 진행되고 있으며, 이 구현을 위해 본 연구의 Barrier 박막 구현은 필수적인 요소로 응용성이 확대되어 활용됨을 기대해 본다.

Keyword : Thin Films , Graphite , PECVD , Silicon Germanium , Display Applications

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Appendix

List of Publications

1. Su Hyoung Kang, Sangmin Kang, Seong Chae Park, Jong Bo Park, Youngjin Junga, Byung Hee Hong, "Large-scale transfer-free growth of thin graphite films at low temperature for solid diffusion barriers", Nanoscale, 10, 14819-14823 (2018).
2. Su Hyoung Kang, Sangmin Kang, Seong Chae Park, Jong Bo Park, Youngjin Jung, Byung Hee Hong, "Silicon germanium photo-blocking layers for a-IGZO based industrial display", Scientific Reports, 8, 17533 (2018).