THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Thin-film ultraviolet light-emitting diodes realized by electrochemical etching of AlGaN

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Front cover illustration: Optical microscope image of thin-film flip-chip (TFFC) ultraviolet-B (UVB) light-emitting diodes (LEDs) on Si carrier. The inset shows a single TFFC UVB LED.

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Abstract

Ultraviolet (UV) light sources have a direct impact on everyone's life. They are used to sterilize surfaces as well as for water purification. In addition, they are used in green houses to enhance health-promoting substances in plants, for phototherapy to treat skin diseases, for sensing and material curing. Today, most of these applications use mercury lamps that are fragile, bulky and toxic. AlGaN-based UV light-emitting diodes (LEDs) have the potential to solve all these issues, but their implementation has been limited due to their low electrical to optical power conversion efficiency (PCE) being below 10%. Blue-emitting GaN-based LEDs have already found their way into everyone's home through general lighting. This was made possible by the tremendous performance improvements, reaching PCEs close to 90%. Unfortunately, the device concepts for achieving highly efficient GaN-based LEDs, such as the thin-film flip-chip (TFFC) design that can greatly improve light-extraction efficiency, are not easily transferred to AlGaN-based UV LEDs.

In this work, we demonstrate a new device platform to realize UV LEDs with a TFFC design based on electrochemical etching to remove the substrate. In the first part of this work, electrochemical (EC) etching of AlGaN layers with a high Al content up to 50% was demonstrated, which enabled the separation of epitaxial LED layers from their substrate while maintaining the high quality of the active region. The second key technological step was the integration of EC etching in a standard UV LED fabrication process, which required protection schemes to prevent parasitic electrochemical etching of the LED structure and the development of a device design compatible with flip-chip bonding. Finally, this work was completed by the first demonstration of a TFFC UVB LED using electrochemical etching.

Keywords: AlGaN, electrochemical etching, heterogeneous integration, light-emitting diodes, LEDs, substrate removal, thermocompression bonding, thin-film flip-chip, ultraviolet light, UVB

List of papers

This thesis is based on the following appended papers:

[Paper A] **Michael A. Bergmann**, Johannes Enslin, Rinat Yapparov, Filip Hjort, Björn Wickman, Saulius Marcinkevičius, Tim Wernicke, Michael Kneissl, and Åsa Haglund, "Electrochemical etching of AlGaN for the realization of thin-film devices," *Applied Physics Letters*, vol. 115, issue 18, p. 182103, 2019.

[Paper B] **Michael A. Bergmann**, Johannes Enslin, Filip Hjort, Tim Wernicke, Michael Kneissl, and Åsa Haglund, "Thin-film flip-chip UVB LEDs realized by electrochemical etching," *Applied Physics Letters*, vol. 116, issue 12, p. 121101, 2020.

[Paper C] **Michael A. Bergmann**, Johannes Enslin, Martin Guttmann, Luca Sulmoni, Neysha Lobo-Ploch, Filip Hjort, Tim Kolbe, Tim Wernicke, Michael Kneissl, and Åsa Haglund, "High-efficiency UVB LEDs using a thin-film flip-chip design and surface roughening," manuscript.

Related papers not included in the thesis:

[Paper D] Filip Hjort, Johannes Enslin, Munise Cobet, **Michael A. Bergmann**, Johan Gustavsson, Tim Kolbe, Arne Knauer, Felix Nippert, Ines Häusler, Markus R. Wagner, Tim Wernicke, Michael Kneissl, and Åsa Haglund "A 310 nm optically pumped AlGaN vertical-cavity surface-emitting laser," submitted.

[Paper E] Joachim Ciers, **Michael A. Bergmann**, Filip Hjort, Jean-François Carlin, Nicolas Grandjean, and Åsa Haglund "Smooth GaN membranes by polarization-assisted electrochemical etching," manuscript.

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Abbreviations

CE	Counter electrode
DBR	Distributed Bragg reflector
EC	Electrochemical
EQE	External quantum efficiency
DLW	Direct laser writing
FC	Flip-chip
LED	Light-emitting diode
LEE	Light extraction efficiency
LLO	Laser-induced lift-off
MOVPE	Metalorganic vapor-phase epitaxy
PCE	Power conversion efficiency
PEC	Photoelectrochemical
QCSE	Quantum-confined stark effect
RE	Reference electrode
RIE	Reactive-ion etching
SEM	Scanning electron microscope
TD	Threading dislocations
TFFC	Thin-film flip-chip
TLM	Transmission line measurement
UV	Ultraviolet
UVB	Ultraviolet-B
WE	Working electrode

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Chapter 1

Introduction

The most important technologies today are invisible and taken for granted. The replacement of incandescent light bulbs with white light-emitting diodes (LED)s and the use of white LEDs as camera lights in smartphones, has brought GaN technology into everyone's home and pockets. The energy efficiency, lifetime and ease of use of these devices shows their significance [1].

This year, in 2020, the COVID-19 pandemic has reached almost every country of the planet earth as reported by the World Health Organization (WHO) [2]. Therefore, methods to disinfect surfaces, air and liquids are of great importance. Ultraviolet light with a wavelength between 280 nm and 210 nm can be used stop the reproduction of microorganisms such as bacteria, spores and viruses [3]. AlGaN-based ultraviolet (UV) LEDs can meet the requirements for these applications both in wavelength and in exposure dose. Compared to the predominant and conventional Hg-lamps used for disinfection, LEDs provide a small form-factor, have a long lifetime and are environmentally friendly by not using mercury.

Besides sterilization in the UVC (280 nm to 100 nm) wavelength range to combat the pandemic and for water purification, UV light has many more applications such as optical lithography, 3D printing and resin curing in the UVA (400 nm to 320 nm) and plant lighting and skin treatment of psoriasis in the UVB (320 nm to 280 nm) [4].

However, in order to benefit from using UV LEDs for such applications, the devices have to be energy efficient resulting in low cost. Whereas blue-emitting GaN-based

LEDs show an electrical to optical conversion efficiency of close to 90% [5], AlGaN-based UV-emitting LEDs are still below 10%. The largest obstacle to realize efficient LEDs is to extract the photons that are generated in the active region from the device. Even for highly-efficient state-of-the-art UVC LEDs, still only 16% of the photons are extracted and thereby useful for any application [3]. This is in contrast to blue-emitting LEDs, for which around 90% of the photons are extracted. Unfortunately, device concepts that are used for highly efficient GaN-based devices such as thin-film flip-chip (TFFC) LEDs are not easily realized for AlGaN-based devices.

This work

In this work we demonstrate electrochemical etching as a way to fabricate TFFC UVB LEDs. In [Paper A], we found suitable etching conditions to achieve a device lift-off which is necessary for a TFFC design. We also showed that transferred epitaxial LED layers maintained the quality of the active region. This formed the basis for [Paper B] with the first demonstration of a TFFC UVB LED using electrochemical etching to remove the substrate. In [Paper C], we show TFFC UVB LEDs with an improved performance using a coplanar contact scheme and surface roughening to enhance the light extraction.

In Chapter 2, the most important properties of III-nitrides are discussed and their consequences for the realization of LEDs. Chapter 3, identifies the factors that limit the power conversion efficiency of UV LEDs and describes the structure of efficient LEDs employing a TFFC design. Chapter 4 describes different potential methods for the fabrication of TFFC UVB LEDs and in detail focuses on implications from using electrochemical etching. The working principle of electrochemical etching is explained in Chapter 5 and includes how it is implemented both in the device design and process hardware. Finally in Chapter 6, the key building blocks of the realized TFFC UVB LEDs are presented, which is concluded by Chapter 7 with a summary of the work and future directions.

Chapter 2

Properties of III-nitrides

Crystal structure and built-in polarization fields

AlN, GaN, InN and their ternary and quarternary compounds belong to the III-nitride material group, i.e. group III in the periodic system combined with nitrogen. The thermodynamically stable phase of these materials is the wurtzite crystal structure. Wurtzite consists of two interpenetrating hexagonal close-packed sublattices, one with group III material and one with group V. The unit cell of a wurtzite crystal is shown in Fig. 2.1(a) and the lattice constants, a and c, define the hexagonal Bravais lattice. The c-plane, which is the most common growth plane, is indicated in red. Due to the different electronegativity of group III (Al, Ga, In) and group V elements (N), the metal-N bonds form dipoles leading to spontaneous polarization fields, P_0, along the bonds as illustrated in Fig. 2.1(b). In unstrained layers, the in-plane components of the spontaneous polarization fields of each tetrahedron cancel out as do the vertical components, and as a result the overall spontaneous polarization is zero. However, III-nitrides deviate slightly from an ideal tetrahedron, i.e. have a non-ideal c/a ratio, and due to the lack of an inversion symmetry plane in the wurtzite crystal structure in the c-direction the material have built-in spontaneous polarization fields along the c-direction. If strain is applied to the crystal, the vertical components of the local polarization fields changes and they do not compensate each other in the same way. This results in what is referred to piezoelectric polarization fields and together with the spontaneous polarization gives the overall polarization fields in the crystal. Since the III-nitrides experience strong piezoelectric and spontaneous

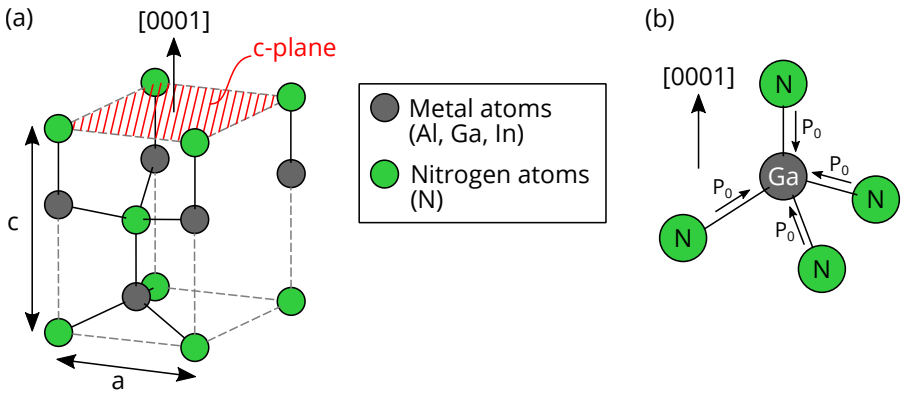

Figure 2.1: (a) A unit cell of the wurzite crystal structure and (b) schematic representation of an ideal GaN tetrahedron.

polarization fields, a heterostructure will experience different built-in fields depending upon strain and its compositions. The built-in fields can greatly affect the band structure and accumulation and depletion of charges, thus affecting both optical and electrical properties.

Optical properties

III-nitride alloys based on AlN, GaN and In have a direct band gap that reaches from $0.6-0.8\,\mathrm{eV}$ for InN to $6.1-6.2\,\mathrm{eV}$ for AlN at room temperature [6]. If double heterostructures, such as a quantum wells, are grown on the c-plane, the built-in polarization fields will lead to band bending across the quantum well that red-shifts the emission wavelength, an effect called the Quantum Confined Stark Effect (QCSE). The bandbending also results in a spatial separation of the electron and hole wave functions, which reduces their overlap and thereby the radiative recombination rate. At higher carrier densities, the built-in polarization fields are screened, which mitigates the QCSE.

The electronic band structure further determines the polarization of the emitted light, determining if it is dominated by transverse electric or transverse magnetic polarized light. For a band structure that yields an emission wavelength of about 240 nm there is a valance band switching which results in an emission pattern where photons mainly propagate parallel to the c-plane for shorter emission wavelengths [7].

This drastically reduces the light extraction through the c-plane and both strain and Al-compositions are therefore being explored to improve the fraction of transverse electric polarized light for short wavelength UV LEDs [8].

Electrical properties

To realize electro-optical devices such as LEDs, p- and n-doped layers are needed to efficiently inject holes and electrons in the active region for recombination. The realization of p-doping has been challenging so far, because magnesium which is the most common p-dopant gets passivated during growth by hydrogen when grown by metalorganic vapor-phase epitaxy (MOVPE) and therefore requires post-growth activation. In addition, the ionization energy of 0.2 eV for the Mg acceptor in GaN and 0.4 eV for the Mg acceptor in AlN [9], makes it a deep acceptor and therefore high dopant concentrations are necessary to achieve a sufficiently high hole density. Holes have a much lower carrier mobility than electrons and therefore current spreading in p-GaN is greatly reduced, and the resistivity of p-doped material is thus much higher, which has to be considered in the device design. The large difference between holes and electrons when it comes to mobilities and concentrations makes it hard to achieve a vertically uniform carrier distribution among the QWs. The large band offsets and built-in polarization fields add additional challenges to this task. The carrier distribution can be improved by preventing an electron overflow to the p-side through introducing a potential barrier in the conduction band in the form of a higher bandgap material on top of the QWs on the p-side, a so called electron blocking layer.

Thermal properties

In semiconductors, heat is mainly conducted by acoustic phonons and therefore depends on dislocations and impurities [10]. The binary materials GaN and AlN have very high thermal conductivities, while AlGaN has significantly lower thermal conductivity due to the induced disordering by an alloy. Minimum thermal conductivity is obtained for Al contents of around 60% [10]. UVB LEDs mostly consist of AlGaN layers with an Al content close to 50% indicating the importance of a good thermal design for these devices.

Chapter 3

UV light-emitting diodes

Within a given set of requirements like emission peak wavelength or process complexity, LEDs are mainly judged by their energy efficiency. Therefore, important figure of merits for LEDs are the power conversion efficiency (PCE) and the external quantum efficiency (EQE). The PCE is the ratio between emitted optical power and electrical input power, whereas the EQE gives the ratio between the number of emitted photons and the number of electrons passing through the device. The PCE includes voltage losses due to electrical resistance at the metal-semiconductor contacts as well as in the semiconductor layers. The following equation relates the PCE η_{PCE} with the EQE η_{EQE} based on the operation voltage of the LED V, the elementary charge e and the photon energy $\hbar\omega$ [11].

$$\eta_{\mathrm{PCE}} = \eta_{\mathrm{EQE}} \times \frac{\hbar\omega}{e \times V} \tag{3.1}$$

Despite the tremendous improvement of blue-emitting GaN-based LEDs over the last decades with power conversion efficiencies reaching up to 84% and external quantum efficiencies over 90% [5], the EQE for UV LEDs still does barely exceed 10% [3]. The highest reported EQE for UVB LEDs, that are within the scope of this thesis, is 6% [7, 12].

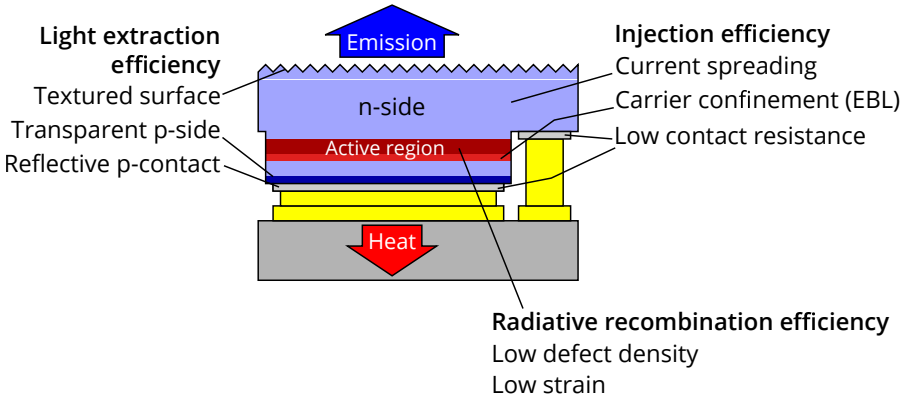

Figure 3.1: Schematic of a TFFC LED with the parts highlighted that influence the EQE.

3.1 LED efficiency

To understand the low EQE, it is important to separate the parts that constitute the EQE. The EQE can be broken down into the injection efficiency $\eta_{\text{injection}}$, the radiative recombination efficiency $\eta_{\text{radiative}}$ and the light-extraction efficiency (LEE) $\eta_{\text{extraction}}$.

$$\eta_{\text{EQE}} = \eta_{\text{injection}} \times \eta_{\text{radiative}} \times \eta_{\text{extraction}} \tag{3.2}$$

To increase the EQE, each efficiency has to be optimized. In high-performing AlGaN LEDs with emission in the UVC, the injection efficiency is about 80%, the radiative efficiency 50% and the light extraction efficiency 16% [3]. The most important parts that influence the EQE are highlighted in Fig. 3.1 that shows an LED in a TFFC design. The TFFC design gives the highest flexibility in the device design because it allows access to both the n-side and p-side. Therefore, both light and heat extraction schemes can be implemented [13].

The injection efficiency $\eta_{\text{injection}}$ is a measure of how many of the electrons that pass through the device actually reach the quantum wells. In order to confine the electrons to the active region, the epitaxial structure contains an electron blocking layer (a high Al-containing AlGaN-layer) above the quantum wells on the p-side. This prevents an overflow of electrons from the n-side to p-side. To achieve a uniform carrier injection into the active region, current spreading on the n- and p-side is important. Due to the low mobility of holes, it is necessary to employ a continuous metal p-contact layer.

Electrons and holes that reach the quantum wells can either recombine radiatively or non-radiatively and the ratio between these recombination mechanisms is expressed by the radiative recombination efficiency, $\eta_{\text{radiative}}$. $\eta_{\text{radiative}}$ is mainly influenced by threading dislocations (TD) and points defects that are incorporated during epitaxial growth [3]. UVA-LEDs with low Al content can be grown on GaN/sapphire templates or freestanding GaN-substrates [14]. UVC LEDs with a high Al can be grown either on AlN/sapphire templates [15] or freestanding AlN-substrates [16]. The use of native substrates yields a low TD density which leads to a high IQE. However, the growth of UVB LEDs on AlN/templates requires buffer layers to mitigate the strain due to the lattice-mismatch and to reduce defects close to the active region [17].

Light extraction

Photons that are generated in the active region have to be extracted from the device to be usable. However, the LEE is limited by total internal reflection and absorption in the semiconductor and metal layers. The absorption is strongly affected by the epitaxial p-(Al)GaN layers and the metallization on the p-side. For UVB LEDs, a thin p-GaN contact layer is often used as a trade-off between achieving a low contact resistance and a low optical absorption [18]. A continuous p-metal contact has to be formed to inject current over the whole active region area due to the poor current spreading on the p-side. To increase the light-extraction, the reflectivity of this metal p-contact should be maximized. It has however been challenging so far to find a suitable metal stack that has both a high reflectivity and yields a low contact resistance. To mitigate the impact from absorption in the p-contact layer on the LEE, reflective photonic crystal structures have been integrated at the interface to the contact layer [19]. In this thesis, 50-nm Pd p-contacts with a reflectivity of around 42% at 305 nm have been used [18, 20]. The impact of absorbing layers on the light extraction is enhanced by reflections at material boundaries and device surfaces. Fig. 3.2(a) illustrates that for a planar LED and only a fraction of the emitted light can escape the device due to total internal reflection, which is defined by the extraction cone. The critical angle θ_{crit} that defines the extraction cone depends on the refractive index of the AlGaN, n_{AlGaN}, and air, n_{air}, and is given by the following equation [11].

$$\theta_{\text{crit}} = \arcsin\left(\frac{n_{\text{air}}}{n_{\text{AlGaN}}}\right) \tag{3.3}$$

Fig. 3.2 only shows the surface emission from the LED, thus only one of the potential six extraction cones. However, light is usually also extracted from other surfaces

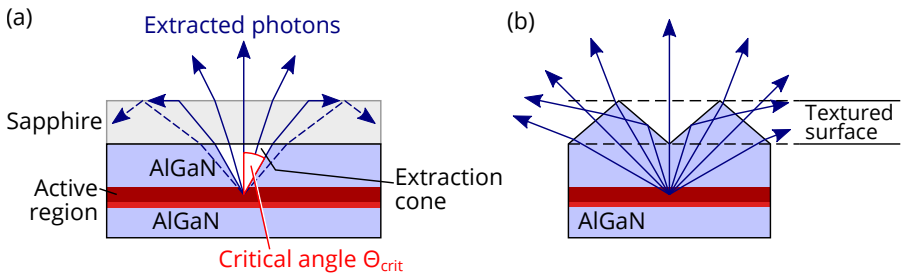

Figure 3.2: Light-extraction from an LED with (a) a flat surface and (b) a textured surface.

such as the edge of the LED chip [21]. The edge-emission becomes more important for small-area LEDs as well as short-wavelength LEDs where a large fraction of the generated light is transverse magnetically polarized and thereby propagates in-plane with the QWs. The distribution between transverse magnetic and transverse electric polarized light is determined by the Al composition and strain of the active region which need to be taken into account when optimizing the light extraction efficiency [21]. Shaping the LED die has been demonstrated to improve the light extraction [5, 22], but requires more complex dicing procedures. Refractive index matched substrates such as GaN-substrates for GaN-based blue LEDs, eliminates reflections at the LED/substrate interface and allows for full use of the extraction cones at the four edges of the LED. Unfortunately, AlGaN bulk substrates that would be required for implementing the same concept for UVB LEDs are not available. To reduce the influence of the planar AlN/sapphire interface, patterned sapphire substrates have been used [23].

TFFC LEDs offer an increased light extraction efficiency by removing the substrate, thereby avoiding reflections at the AlGaN/sapphire interface, and texturing the AlGaN surface. Due to the angular dependence of the reflections, surface texturing helps to achieve an incidence angle close to the surface normal for an increased extraction, see Fig. 3.2(b). The improvement due to surface texturing has been shown for a number of UV LEDs [24–29].

3.2 TFFC designs

In a TFFC design, the LED is bonded on the p-side and the n-side is roughened, which is enabled by the substrate removal. Such devices can be realized using dif-

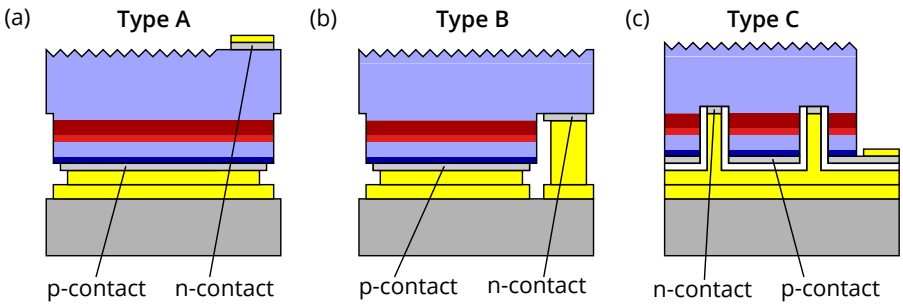

Figure 3.3: Comparison of different contacting schemes for TFFC LEDs.

ferent contact schemes as shown in Fig. 3.3.

For all three types A-C, a similar active region area can be achieved. To take full advantage of the TFFC design and the potentially high light-extraction, a transparent p-side and a reflective p-contact have to be used. Type A has the drawback that the p-contact together with buried metal bonding layers can be heavily affected by the n-contact annealing, with is done in a later step. Therefore type A doesn't allow a proper annealing scheme. In addition, due to the top n-contact, probing has to be done directly on the device or by wire-bonding, which can deteriorate the thin-film device due to the mechanical force. However, the advantage of type A is the simple mesa design and the simple bonding process. Therefore, the first demonstration of a TFFC UVB LED within this work, shown in [Paper B], is based on a type A design.

It is important to note that the n-contact for type A is on the N-polar surface for metal polar growth, whereas for type B and C, the n-contact is formed on the metal-polar surface. If the substrate removal process includes an etch stop layer, the n-contact is either deposited on that layer or the etch stop layer needs to be removed before the contact deposition.

Both type B and type C allow a proper order of the metallization steps with decreasing process temperatures. For the devices demonstrated in this work, the n-contact requires the highest process temperature during the annealing with up to 900 °C followed by the Pd p-contact with temperatures up to 600 °C. The Au-Au thermocompression bonding is done after these steps at a temperature of 300 °C. The advantage of type B is that after the flip-chip bonding only the surface roughening as the last process steps remains, whereas type C additionally requires a dry etching step to

expose the p-contact and potential wire bonding. Regarding the flip-bonding complexity, type B requires a structured carrier wafer and an aligned bonding process.

From a thermal perspective, type A and type B have no dielectric layers between the active region as the main heat source and the substrate. Type C requires a dielectric layer to separate the n- and p-contact layers.

Challenge

The realization of a TFFC design requires substrate removal to texture the AlGaN surface. Despite the demonstration of several TFFC UV LEDs [24–33], substrate removal is not yet done in a straight forward way. The different methods that have been explored for substrate removal together with their associated challenges will be outlined in more detail in the next chapter.

Chapter 4

Heterogeneous integration of AlGaN/GaN

One of the driving factors of the continuous development of semiconductor devices, not only LEDs, is to improve the performance. In order to maximize the device performance, the most suitable materials for each part of the device have to be chosen. However, in many cases these materials cannot be combined using a monolithic design. Whereas metal or dielectric layers can be fabricated using additive processes, epitaxial layers require a proper substrate to be grown on. Therefore, the integration of thin epitaxial layers, requires substrate removal and a transfer process, as illustrated in Fig. 4.1.

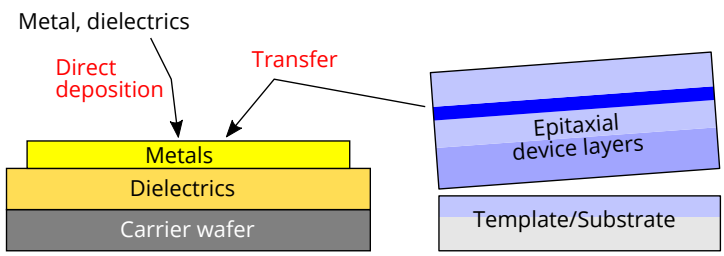

Figure 4.1: Heterogeneous integration of the epitaxial layers using a layer transfer process.

There are basically two different ways to separate epitaxially grown device layers from their substrate, either by the use of an epitaxially grown sacrificial layer from the same material system as the device layer or by the use of a different material in the sacrificial layer (or the full substrate) that is more easily removed. A third possibility is to grind away the substrate and thereby expose the epitaxially grown layers. Ideally the separation method should not affect the separated device layers and should yield a surface roughness close to that of the as-grown epitaxial surface in order to be used for device structures like optical resonators, photonic crystals and waveguides. In addition, the substrate removal process should be compatible with the overall device process and should be preferably done in a cleanroom environment. The use of an AlGaN sacrificial layer is preferred for AlGaN devices since it will not affect the quality of the device layers grown on top of the sacrificial layer.

4.1 Methods for substrate removal

Substrate removal to transfer epitaxial layers is used for a variety of material systems such as InP [34] and GaAs [35], where wet etching is usually employed to selectively dissolve sacrificial layers and enable the transfer. Unfortunately wet etching is not easily applied to the AlGaN material system due to its chemical inertness [36]. Therefore, alternative ways to achieve substrate removal are being explored.

Laser-induced lift-off (LLO) is as a common method to separate GaN-based LEDs from their sapphire substrate. It is based upon thermal decomposition of the GaN at the sapphire substrate interface induced by optical absorption of a high power laser beam illuminating from the backside of the sapphire substrate (see Figure 4.2) [37]. LLO has been demonstrated for both wafer-scale epitaxial layer transfers and for single device transfer [38, 39]. The resulting surface roughness of a few nanometers does not degrade the LED performance in general, but it limits the applicability of this method to devices which require optically smooth surfaces [40]. In addition, achieving an accurate thickness control of the separated layers is difficult because the decomposition can take place in an extended region of the interfacial GaN layer. Post-processing using chemical mechanical polishing presents a possibility to reduce the roughness, but setting the exact thickness remains a challenging task and can only be applied on a wafer-level [41] or larger areas but not for individual devices. Whereas LLO works for GaN-based LEDs within the aforementioned limitations, thermal decomposition has been proven to be challenging when applied to AlGaN [30]. The decomposition of AlGaN yields additional Al residues which are more

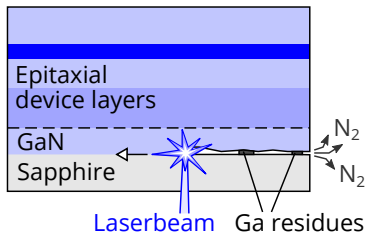

Figure 4.2: Thermal decomposition by laser induced lift-off.

difficult to remove than just Ga residues in the case of GaN and the higher laser power required to decompose AlGaN results in even a higher thermal chock to the devices which are more likely to crack due to built-in strain. Therefore, only few thin-film UV devices using LLO have been demonstrated [24–26, 28–31].

Similar to the thermal composition through optical absorption, work has been done to selectively decompose GaN layers using high temperature conditions. The etching selectivity is achieved by using different Al contents, since layers with higher Al-compositions showed a reduced etch rate. By using this method, AlGaN-based photonic crystal structures have been demonstrated by decomposing GaN layers [42, 43]. Compared to the LLO process, selective decomposition can yield a better thickness control, but the high temperatures of up to 1000 °C potentially affect many other parts of the device such as active regions and metal layers and therefore limits its use. The high process temperatures, which are similar or even higher than the epitaxial growth temperatures, could also lead to compositional changes in the semiconductor layers and diffusion of dopants.

The chemical inertness of AlGaN has been overcome by using electrochemical (EC) etching [44] and photoelectrochemical (PEC) etching [45]. These methods are based upon the generation of electrons and holes at the interface between the semiconductor and a wet etchant, and these carrier then enable an electrochemical reaction the etches the material. In EC etching, the holes are created by electron tunneling across the bandgap or avalanche breakdown induced by an applied bias voltage. The etching contrast can hereby be achieved by using both the doping level and the composition of the AlGaN, which determine the bandstructure in the interfacial region. EC etching has low requirements on the experimental setup and is compatible with existing cleanroom equipment used for processes such as electroplating. In PEC etching, the holes are generated by photoexcitation and selectivity is mainly achieved by bandgap

engineering to achieve a contrast in optical absorption [45]. The sacrificial layer is a lower bandgap material, like InGaN, surrounded by higher bandgap material such as GaN layers to limit the hole generation to the sacrificial layer. This contrast in optical absorption and confinement of carriers can be enhanced by the integration of AlGaN etch block layers to increase the bandgap step. Because the etching process requires holes, any recombination of the photogenerated carriers should be minimized. The band bending at the semiconductor electrolyte interface helps to separate electrons and holes. Since the band bending is influenced by the doping level, PEC etching is also doping selective [46]. To further increase the band bending, external bias voltages have been applied [47–51]. However, depending on the crystallographic growth direction of the epitaxial layers and the incorporated strain, carrier separation can be enhanced by the built-in spontaneous polarization and piezoelectric polarization fields. PEC etching, has been demonstrated for devices based on nonpolar and semipolar GaN but smooth etched surfaces have also been obtained for devices on c-plane GaN [47, 52, 53]. The combination of a high etching selectivity and a low surface roughness this technique offers have led to the realization of several photonic devices such as electrically injected VCSELs in the blue [52] and optically pumped cavities [47]. For both EC etching and PEC etching, the crystallographic growth direction also plays a role if the wet etchant used in the these processes leads to pure wet etching and thus an increased surface roughness. Especially in the case of PEC etching, for which KOH is the most common electrolyte, increased surface roughness with increasing concentration of the electrolyte has been demonstrated [47]. In addition to leading to a rough N-polar surface, KOH is also not compatible with several cleanroom processes [54].

As an alternative to the removal of AlGaN layers with the aforemetioned methods, sacrificial layers that could be more easily removed or allow for an exfoliation of the epitaxial layers have been investigated, see Fig. 4.3(b). The challenge for this approach is to find materials that allow the growth of high-quality epitaxial layers on top of the sacrificial layer. Nb_2N sacrificial layers, which can be removed using XeF_2 vapor etching, have been successfully integrated in a GaN epitaxial structure [55, 56]. GaN-based devices have also been separated by a mechanical transfer using BN sacrificial layers [57, 58].

Instead of integrating sacrificial layers between the device layers and the substrate, alternative substrates that can be etched more easily than III-nitride substrates have been used to enable a substrate removal. GaN-on-Si has for example been used

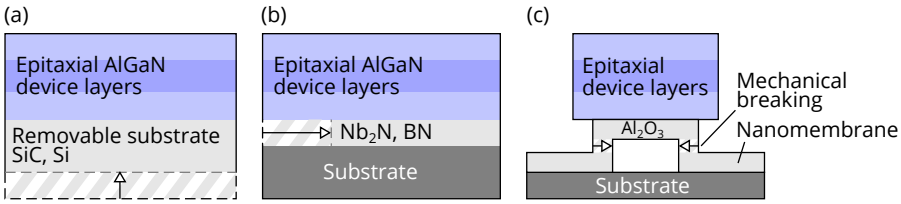

Figure 4.3: (a) Substrate removal using alternative substrate materials, (b) sacrificial layers from other material systems and (c) alternatively shaped substrates.

to demonstrate suspended membranes for a variety of devices [59–64]. However, the growth of GaN on silicon requires buffer layers inbetween, which could impede the device design and quality as well as the process flow. GaN-on-SiC allows for dry etching of the SiC and has led to the demonstration of thin-film UV LEDs [27, 32, 33]. Rather than growing on bulk substrates, the growth of GaN layers and GaN-based devices on sapphire nanomembranes acting as a compliant substrate have been demonstrated [65, 66]. In these works, Al layers have been transformed into a crystalline Al_2O_3 layer by high temperature annealing, which allowed for the growth of epitaxial GaN on top. Due to the possibility of shaping these nanomembranes, single devices or continuous membranes are grown and can be separated by a mechanically transfer, as shown in Fig. 4.3(c).

In this work, EC etching has been chosen because it can yield smooth etched surfaces, it provides an epitaxially defined etch stop and the AlGaN sacrificial layer allows for the growth of high-quality epitaxial device layers on top. EC etching is also a fast etch method with lateral etch rates of tens of micrometers per minute, which allows the underetching of LEDs with a size of $300\,\mu m \times 250\,\mu m$ in a few minutes.

4.2 General considerations for transferring epitaxial layers

In general, there are two different ways to transfer device layers between substrates. The first way is to bond these device layers to a carrier substrate, which is followed by a removal of the original substrate. The second way is to release the device layers but still keeping them in place and then transfer these device layers to a carrier substrate. Bonding the device layers first can result in a better bond because the devices are not yet released, thus planar and the applied force is more uniform. In addition, non-released devices are less prone to cracking induced by the bonding force. Especially

for transferring large-sized epitaxial layers, this is the method of choice. However, this method is associated with a number of challenges. First, the formed bond has to be compatible with the substrate removal process. For example, metal bonding layers could be etched by a chemical substrate removal or reformed if heat is generated in the removal process. Secondly, if the bonding results in a negligible gap between device substrate and the carrier substrate, this may hinder a substrate removal that requires lateral access to each of the devices. This effect becomes more severe with a scaled-up sample size [67]. If the substrate removal process yields gas evolution, tightly bonded samples can capture the generated gas, which can significantly slow down the etching process. The gas formation also leads to a pressure on the bonded samples, stressing the bonding connection.

Both problems can be solved by using the second approach where devices are released before bonding. In order to bond released device layers, the bonding method should be able to accommodate any non-planarity. Bonding on a device level also relaxes the constraints imposed by built-in strain and differences in thermal expansion coefficients between devices and substrate. It should be noted that for devices that are going to be electrically connected to the carrier substrate, such as TFFC LEDs, the substrate removal must be done before the transfer if the removal method affects exposed electrical contacts. One example of such a removal technique is electrochemical etching.

4.3 Tether design

Devices that are released from the growth substrate before bonding, must be held in place by tethers after the sacrificial layer removal, see Fig. 4.4(a), a concept that has been used for example for GaN LEDs on Si [68] and InP-based devices [34]. Common materials for tethers are photoresist layers, due the easy removal, and patterned device layers because no additional layers are required. For large area devices ($> 500\,\mu m \times 500\,\mu m$), additional tethers inside the device area can be integrated (see Fig. 4.4(b)). Such anchors have been used to keep suspended membranes fixed to the substrate before transfer-printing [69].

In this work, the protective SiO_2 layers for the electrochemical etching are also used as tethers. This is a suitable material because it withstands both the acid used for the electrochemical etching and the solvent cleaning afterwards. The strength of the tether depends both on the layer thickness and the perimeter of the device. Dur-

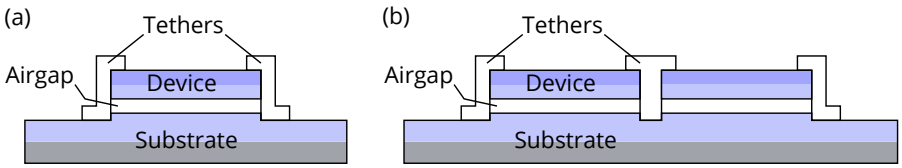

Figure 4.4: (a) Tethers at the device perimeter for small devices, (b) additional anchors for larger devices.

ing the device release, the tether is further supported by an additional resist layer. As the sacrificial layer is etched, gas generation leads to an additional force on the formed membrane. Under some circumstances the tethers were not strong enough and devices detached after removing the resist layer.

4.4 Strain considerations

When fabricating large continuous membranes by removing a sacrificial layer below, buckling can occur as shown in Fig. 4.5(a)-(c). The buckling of the released top layer indicates compressive strain in the as-grown epitaxial layers. As shown in the top view image in Fig. 4.5(c) the membrane is connected to the surrounding non-underetched part and the strain cannot be fully released. To more effectively release the strain, the membrane can be patterned and attached to the surrounding layers on single points using tethers as shown in Fig. 4.5(d) and (e). The extent of the buckling depends of course on the strain state of the epitaxial layer after the growth. In this work some tethers have been broken due to strain-induced bowing of devices which resulted in too early detachment of devices. Bowing of devices can also affect the bonding quality and it is thus of importance to consider and engineer the strain. Additional layers like dielectrics that are added during the device process, can, depending on the deposition method, introduce additional strain, but could also be used for strain compensation.

4.5 Methods for bonding

In order to complete the transfer of epitaxial layers, these layers must be integrated on a carrier substrate. Depending on the function of the transferred layer, different requirements are set on the chosen method. If an electrical connection has to be

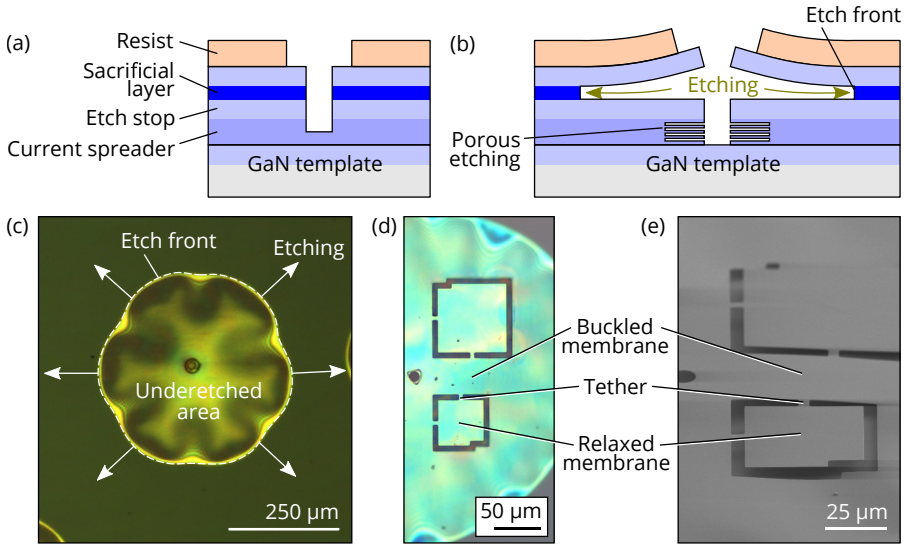

Figure 4.5: (a), Schematic cross-sectional view of the sample structure before electrochemical etching, (b) schematic of sample during electrochemical etching, (c) optical microscope image of a membrane after electrochemical etching, (d) optical microscope image of a patterned membrane, and (e) SEM image of a patterned membrane.

established between the transferred layer and the carrier substrate, direct bonding without an interlayer or metallic bonding would allow for such a connection. Depending on the placement of the bonding interface, also its optical properties have to be considered. If there is no need for an electrical connection, adhesion bonding using polymers like BCB is a possible choice but needs to be compatible with the optical design. Further the formed bond must be also compatible with any post processing in terms of chemical and thermal robustness. The surface quality also sets restrictions on which bonding method that can be applied. For samples with a high surface planarity and a low surface roughness, direct bonding can be used, while for lower-quality surfaces (induced by epitaxial growth and/or device fabrication) eutectic or adhesive bonding are the only options.

To realize TFFC LEDs, the devices need to be bonded to a carrier chip with electrical connections. This bonding contact further works as a heat sink for the bonded device. Therefore, a metal-metal thermocompression bonding is used for this work, which

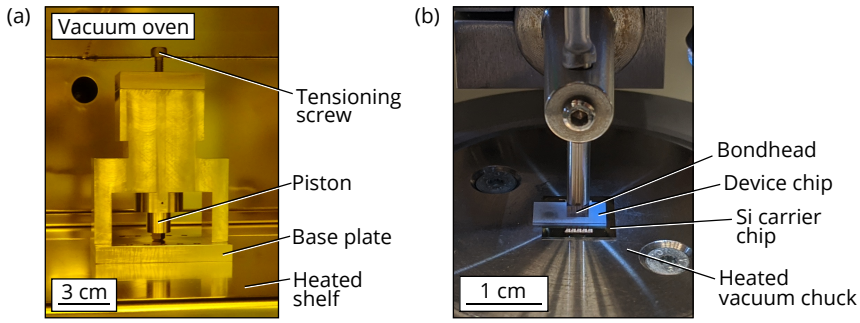

Figure 4.6: Picture of (a) the used bonding fixture in a vacuum oven and (b) the flip-chip die bonder.

fulfills both criteria. Au-Au was chosen for the bonding layers due to its chemical stability and thermal conductivity. Typical bonding temperatures are in the range of 250 °C to 350 °C and bonding pressures are in the range of 1 MPa to 100 MPa [70–72]. However, unsuitable bonding conditions could potentially affect the p-contact reflectivity.

To apply the pressure for the bonding either a stainless steel fixture as shown in Fig. 4.6(a) or a commercial flip-chip die-bonder from JFP Microtechnic, shown in Fig. 4.6(b), was used. The flip-chip die bonder allows an alignment of the chip before the bonding, which is important for devices with coplanar n- and p-contacts. Whereas the bonding fixture is used for LED samples and bonding tests that have no requirement on the alignment. Furthermore, the bonding fixture can be placed in an vacuum oven to prevent air inclusions and potential oxidation of any metal layers on the sample.

4.6 Choice of carrier material

The carrier that hosts the TFFC LEDs after the bonding can be of different materials, but there are some restrictions. First, the substrate has to be suitable for the bonding process. Problems can arise from a large difference in the thermal expansion coefficient, which can lead to a cracking of the transferred devices [25]. For all devices of this work, Si substrates were used and no major cracking of LEDs, that could be ascribed to too much strain, was observed. This is facilitated by the bonding on a device level compared to transferring large-sized thin films. Second, if further processing is to be done on the LEDs on the carrier chip, the substrate material has to be

compatible. For example, wet etching for surface roughening of the LED can affect e.g. Si substrates. Third, the substrate material also influences the device performance. In the case of LEDs, the substrate functions as a heat sink and materials with a high thermal conductivity are therefore preferred. In addition, to the factors that influence the device process and performance, also the convenience factor should be considered. Si substrates allow standard processing and are relatively cheap.

Chapter 5

Device release using electrochemical etching

5.1 Electrochemical etching of AlGaN

In an AlGaN-electrolyte junction at equilibrium, the Fermi level in the AlGaN and the electrolyte adjust by exchanging electrons [73]. As a result, a space charge region forms near the interface and the semiconductor bands are bent in the AlGaN due to the built-in field (see Fig. 5.1(a)). The built-in field depends on the position of the Fermi level relative to the position of the redox level in the electrolyte before forming the junction.

By applying a bias voltage to the AlGaN sample relative to a counter electrode (CE), which are connected by an electrolyte, the Fermi level in the semiconductor is shifted and the field across the space charge region changes (see Fig. 5.1(b)). The bias voltage U_b which is applied between the AlGaN sample (called the working electrode WE) and the CE, distributes across the semiconductor, electrolyte, counter electrode, electrical contact on AlGaN and the interfaces. Therefore, the potential drop across the space charge region will be smaller than the applied voltage. In addition, processes ongoing at the counter electrode influence the electrode potential and are current dependent. To solve these two problems, a reference electrode (RE) is commonly used in addition to the counter electrode. Such a setup is called a three-

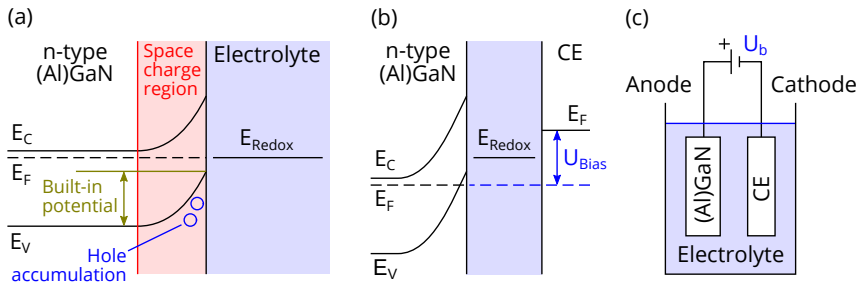

Figure 5.1: (a), Semiconductor-electrolyte junction under equilibrium and (b) under positive bias relative to a metallic counter electrode (CE). (c), Schematic of a two-electrode setup.

electrode setup and is shown in Figure 5.2. Using a potentiostat, the potential at the working electrode (i.e. AlGaN sample) is set relative to the electrode potential of the RE and the required current for this potential is established with the CE. Therefore, the current over the reference electrode is minimized and a stable potential is achieved. The reference electrode which is used in this work is based on the Ag/AgCl reaction: $\mathrm{AgCl(s)} \rightleftharpoons \mathrm{Ag^+ + Cl^-}$ and has a well known electrode potential [74]. To reduce the resistance in the electrolyte between RE and WE, RE is placed as close as possible to WE. In addition, the counter electrode should have a sufficiently large surface that the current between WE and CE is not limited by the charge transfer on the cathode side. Depending on the application and the requirements on potential stability and accuracy, a two-electrode setup can be sufficient. When using a two-electrode setup it is important to keep the arrangement of the electrodes the same for each experiment to prevent major changes in the potential drop over the electrolyte.

Depending on the potential drop across the space charge region, Zener tunneling and avalanche breakdown can occur (see Fig. 5.3). In the case of Zener tunneling, valence electrons tunnel to the conduction band and thereby leaving holes behind. Avalanche breakdown creates electron-hole pairs by impact ionization in the space charge region. Due to the electric field in the space charge region, the generated holes, no matter the hole generation process, accumulate at the AlGaN/electrolyte interface. In order to achieve Zener tunneling, the applied bias voltage including the built-in potential has to be larger than the bandgap. The required bias voltage to obtain etching for AlGaN increases with the Al content as we have demonstrated in [Paper A]. Increasing the n-doping of the AlGaN reduces the required bias voltage,

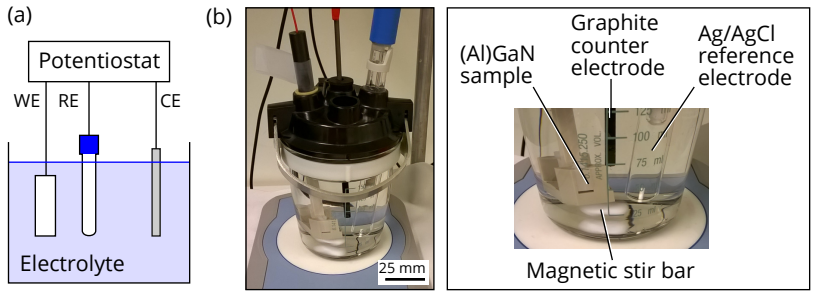

Figure 5.2: (a), Schematic of a three-electrode setup and (b) photograph of the three-electrode setup used for the electrochemical etching of AlGaN.

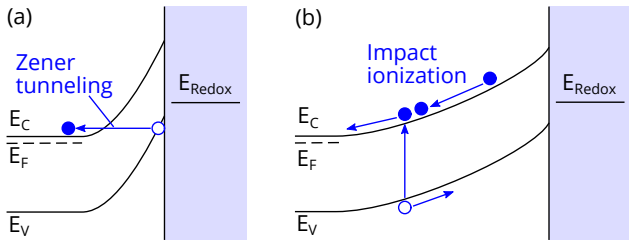

Figure 5.3: Illustration of (a) Zener tunneling and (b) avalanche breakdown.

since that increases the built-in field (increased Fermi level) and reduces the barrier width at the semiconductor/electrolyte junction.

The presence of holes in the semiconductor at the semiconductor/electrolyte interface effectively means that a bond has been broken between a group III element and N. Thus the oxidation of the semiconductor has been facilitated by the carrier generation caused by the applied electric field [75]. Due to the difference in the oxidation potential of GaN and water, the oxidation of GaN is more likely than the oxidation of water (see Fig. 5.4) [76]. As a result of the electrochemical decomposition of AlGaN, oxidation products can form an oxide or hydroxide depending on the electrolyte. With the goal to etch the AlGaN, the electrolyte is chosen such that formed oxides or other chemical compounds with Ga and Al are not stable [77]. Common acids are nitric acid, oxalic acid [78–80] and hydrofluoric acid [81, 82], but also neutral electrolytes like $NaNO_3$ were successful in electrochemical etching of GaN [83–85]. Based on the stability of the decomposition products, the overall electrochemical reaction for

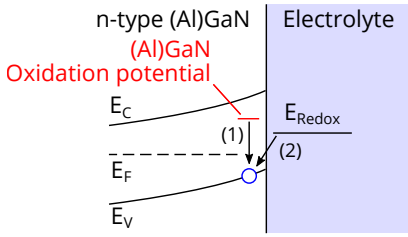

Figure 5.4: Competing oxidation processes of GaN and water.

AlGaN using nitric acid, as proposed in [Paper A], is the following:

$$2\,\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{N} + 6\,\mathrm{h}^+ \longrightarrow 2\,x\,\mathrm{Al}^{3+} + 2\,(1\text{-}x)\mathrm{Ga}^{3+} + \mathrm{N}_2\,. \tag{5.1}$$

Depending on the alignment of the valence band in the semiconductor to redox potentials in the electrolyte, additional oxidation processes can occur at the AlGaN anode (see process (1) and (2) in Fig. 5.4). For example, generated holes in the valence band can also lead to water oxidation, process (2) in Fig. 5.4 [76].

$$2\,\mathrm{H_2O} \longrightarrow \mathrm{O_2} + 4\,\mathrm{H}^+ + 4\,\mathrm{e}^-\,. \tag{5.2}$$

Besides, changing the reaction and its products, the pH level of the electrolyte affects the position of the redox level and its position relative to the band edges. Therefore, the necessary potential for the dissolution of AlGaN can change [83]. Changing the concentration of the electrolyte influences the resistance in the electrolyte and the dynamics of the dissolution process can change.

5.2 Etching conditions for device lift-off

The dependency of the etching process on the material properties like doping and composition is used to create an etch selectivity and to define a sacrifical layer (see Fig. 5.5). Doping is the most commonly used property and preferential electrochemical etching of n-doped GaN over unintentionally doped GaN layers has been widely used to suspend layers and to lift-off devices [78, 86–88].

Lifting-off devices requires uniform etching of the sacrificial layer as shown in Fig. 5.5(c). That means the oxidation reaction has to happen across the entire sacrificial layer, which requires a sufficiently high hole concentration. Because the surface

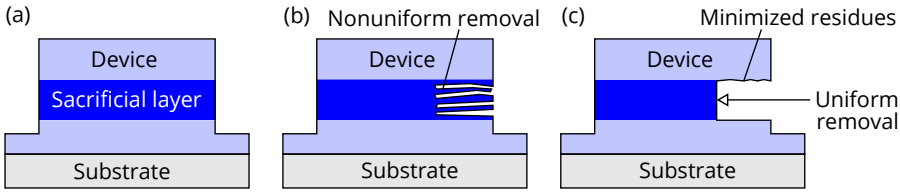

Figure 5.5: (a) Schematic of device on top of sacrificial layer and illustration of (b) nonuniform, and (c) uniform sacrificial layer removal.

layer of the semiconductor is not completely uniform in morphology, homogeneity and quality, etching conditions can vary locally. The morphology of the surface influences the local electrical field and the space charge region. As a result, localized spots exhibit a different behaviour and a non uniform etching is observed (see Fig. 5.5(b)). This behaviour is exploited for porous etching [78, 81, 89]. To make sure that the oxidation process proceeds in the whole sacrificial layer, the electrical field has to exceed a certain value at the whole AlGaN/electrolyte interface. This is done by choosing the right conditions with a sufficiently high doping concentration and bias voltage. The onset of the etching process can be determined by a cyclic voltammetry experiment. By sweeping the applied potential at the AlGaN anode, disolution is recognizable by the onset of a current flow. However it does not give conclusive information about uniform etching of the layer and how the etching proceeds because at the onset of the current flow, porous etching is observed. Because etching in the porous regime greatly alters the interface between the sacrificial layer and the electrolyte, a continuation at a higher voltage might be influenced. One reason is that the porous sacrificial layer increases the resistivity and thereby affect the etching conditions [90]. Therefore, the conditions for uniform etching are mostly found by an etching series with an applied constant potential.

To obtain an etch selectivity, not only doping concentration, but also material composition, such as the Al-composition of an AlGaN sacrificial layer in relation to surrounding layers can be used. It should however be noted that the voltage to achieve uniform etching of AlGaN increases with the Al content as we have shown in [Paper A]. Having both the doping and the composition as parameters to design the sacrificial layer and etch block layers gives the possibility to achieve a higher selectivity. In addition, it allows to work around limitations like such as maximum doping levels imposed by a required surface morphology.

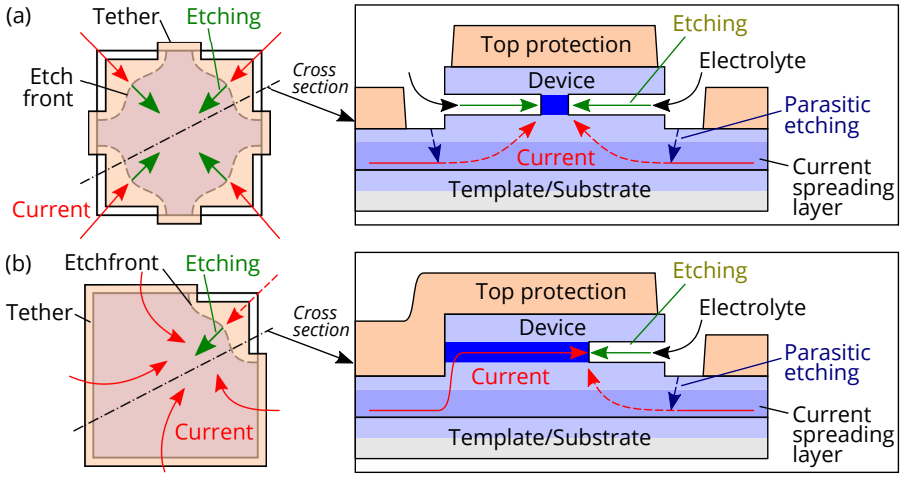

Figure 5.6: Schematic of current supply, tether and electrolyte supply in the case for (a) nearly full sacrificial layer exposure and (b) strongly limited sacrificial layer exposure.

For devices that require smooth surfaces, the etching contrast between the sacrificial layer and the etch block layer has to be maximized. That means that in the sacrificial layer at the interface to the electrolyte, the hole density should be as high as possible but should decrease abruptly at the interface to the etch block layer. To increase that contrast, sacrificial layers with an increased doping level at the interfaces have been demonstrated [91]. Using a higher Al content in the etch block layer can further reduce the hole density.

In order to achieve an uniform etching for all devices across the sample, usually a current spreading layer below the sacrificial layer is used. The doping level of the current spreading layer is chosen sufficiently high that the potential drop across the sample is not significant but still low enough to reduce parasitic etching in that layer.

In addition, to the epitaxial design, also the lateral dimensions and how the etching progresses in the sacrificial layer influences the obtained smoothness. For pure wet etching, usually the sacrificial layer is fully exposed at its perimeter to accelerate its removal. If devices are transferred after the sacrificial layers removal, single tethers on the device edges are used to keep it in place (see Fig.5.6.a). However, for electrochemical etching it is important to control not only the etchant access to the sacrificial layer but also the current supply. If not considered, this might lead

to merging etch fronts which obstruct the current supply and thus inhibits the complete removal of the sacrificial layer, leaving residues behind [88, 91]. This could be detrimental for devices which require a smooth surface. This issue can be solved, as illustrated in Fig. 5.6(b), by exposing the mesa to be underetched only at one part of the perimeter, and the etch front progresses unidirectionally across the mesa without interruption. Thus minimizing residues by keeping constant etching conditions for the whole sacrificial layer removal.

5.3 Sample design to avoid parasitic etching

In the ideal case, only the sacrificial layer is removed and all surrounding layer are not affected. However, most devices contain multiple doped layer and other materials like metals that can potentially etch due to the applied positive bias potential. Therefore, there are several pathways for the parasitic electrochemical etching, which are illustrated in Fig. 5.7.

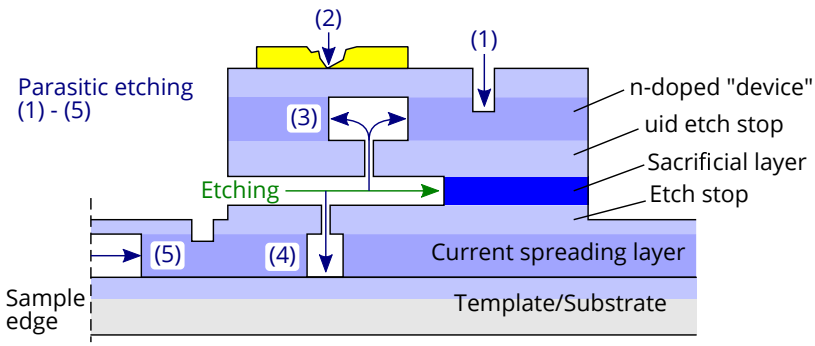

Figure 5.7: Pathways for parasitic etching.

To prevent parasitic etching of epitaxial layers and metal contacts from the top, as shown in Fig. 5.7(1) and (2), samples are usually coated by an insulation layer which also has to be stable in the electrolyte. Depending on the sample design SiO_2 or resist layers are used. Resist protection layers have the advantage of being flexible and thereby adapting to potential buckling of released membranes. In addition, thick layers are easily applied, which can cover large topographies of various materials. Afterwards, the resist can be removed by using solvents or plasma ashing.

Resist layers to protect planar structures are working well but resist layers are com-

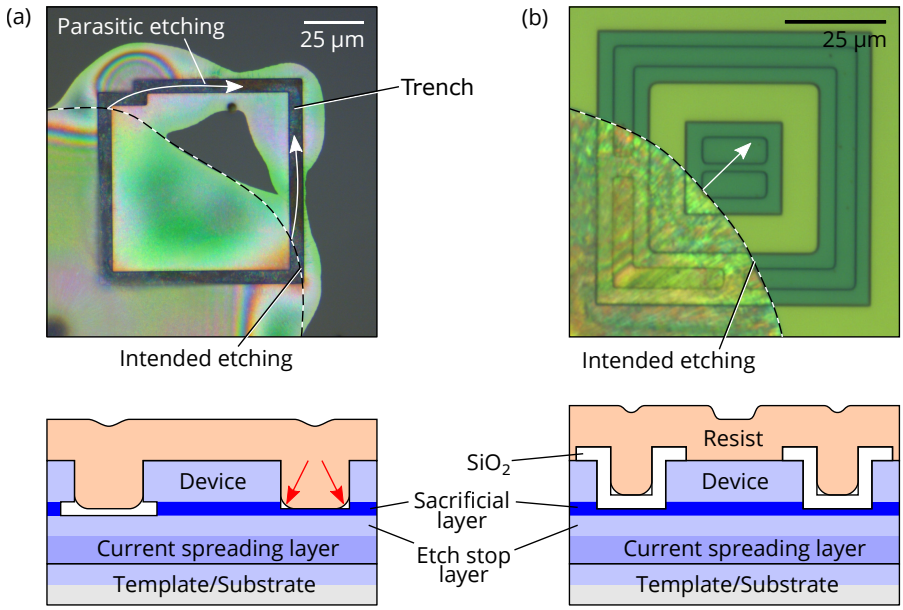

Figure 5.8: Comparison of protection layers for electrochemical etching. (a), single resist layer on top of patterned sample leading to parasitic etching and (b) SiO_2 filling the trenches leading to more controlled etching front.

monly applied using spin-coating which doesn't cover very well high mesa sidewalls. As a result, inner corners are not completely filled and provide channels for the electrolyte, indicated by the red arrows in Fig. 5.8(a), leading to parasitic etching. Figure 5.8(a) shows how the etching proceeds faster in the trenches which is attributed to a inferior filling and adhesion. In contrast, SiO_2 or SiN layers can be deposited conformally and lead to a more controlled etching front as shown in Fig 5.8(b). The resist layer on top of the SiO_2 still provides channels but these are not connected to the electrolyte. A combination of SiO_2 protective layers and resist layers have been found to be the best working solution. SiO_2 is used for the parts where coverage is essential like mesa sidewalls, and resist layers are used for parts where the insulation needs to be removed after the electrochemical etching. The device design is chosen in such a way that non-optimal sidewall coverage of the resist is not an issue.

When using doping to achieve an etching contrast, unintentionally doped layers are usually used as etch block layers. However, the etching can proceed even through

such unintentionally doped layers at distinct spots if it separates n-doped layers, as illustrated in Fig. 5.7(3). This can be attributed to dislocations and is used in others work to consecutively etch stacked layers [92]. Figure 5.9(a) shows a schematic with parasitic etching occuring through the etch stop layer on top of the sacrificial layer and in the n-doped device layer on top. Figure 5.9(b) shows two SEM images with cavities etching in between the uid-GaN layers. The SEM images further show that the parasitic etching occurs at distinct spots, which is an indication for dislocations.

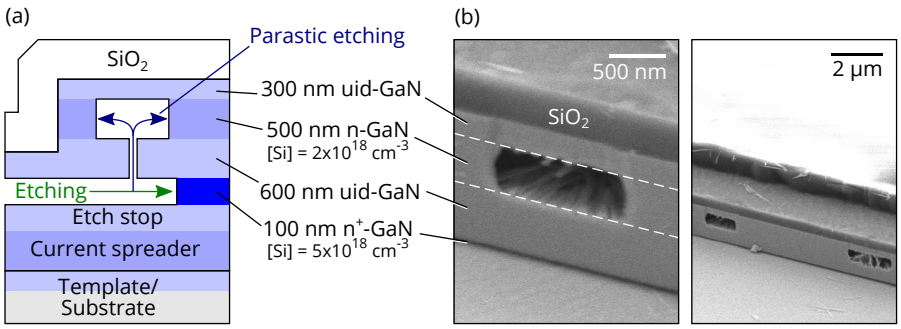

Figure 5.9: (a) Schematic of pentration through the etch stop layer on top of sacrificial layer and (b) SEM images showing etching of the n-doped GaN embedded inbetween uid-GaN layers.

Depending on the epitaxial structure, parasitic etching occurs in the current spreading layer by penetrating the bottom etch block layer as illustrated in Fig. 5.7(4). The etching of the current spreading layer can increase the resistance and the caused voltage drop affects the etching conditions for the sacrificial layer. This problem could be avoided by adapting the doping level and thickness of the current spreading layer.

Lastly parasitic etching can occur at the sample edges as indicated in Fig. 5.7(5), which can potentially affect the etching conditions.

5.4 Electrical connection to the sample

Because electrochemical etching depends on the band bending in the sacrificial layer that is set by the potential drop over the semiconductor-electrolyte interface, accurate setting of that potential is essential. Establishing a proper current flow between the

voltage source and the sacrificial layer interface is therefore a crucial part of the device and setup design. In an ideal case, all the current is transported across the semiconductor/electrolyte interface that is intended to be etched. Thus, any parasitic exposure of current conducting parts on the AlGaN sample with the electrolyte is avoided. Especially metals, which in general require a lower potential for corrosion [77], have to be protected from the electrolyte. Therefore either the whole sample is not immersed in the electrolyte or the contact is sealed. Small-sized chips ($<$ 10 mm $\times$ 10 mm) are difficult to partially immerse and therefore the second option is chosen in this work. In addition to the insulation, the resistance between the voltage source and the semiconductor/electrolyte interface has to be minimized to accurately set the bias potential. Especially for samples containing higher Al contents, proper n-contact formation is important.

There are several ways to establish an electrical connection to a semiconductor sample. Common methods include conductive tape [79, 81, 83, 93], conductive paste [94], In-dots [89, 95–103], wirebonding [95, 96] and clamping [104]. Because the samples undergo further processing after the electrochemical process, the electrical contacting should not leave residues which are incompatible with the subsequent steps. Especially in the case of full immersion, shielding electrical contacts by using wax or glue can be unreliable and difficult to reproduce. In order to use small sample sizes, the footprint of the connection should be minimized. In this work, spring loaded pins, which are commonly found in electrical interconnects, are used to connect to a metal contact formed on the AlGaN sample. This combination offers a reliable connection and the sample is not affected by the contacting. Figure 5.10 shows a schematic cross-sectional drawing of the sample holder including the connection to the sample. The sealing ring clamps the sample to the holder and prevents exposure of the metal connection to the electrolyte. Figure 5.11 shows an exemplary sample with the left part dedicated to the electrical connection and process control structures like transmission line measurement (TLM) patterns. The sample is designed to only expose those parts to the electrolyte that are intended to be etched. However, it is difficult to protect the sample edges and parastic etching can therefore occur. A modified sample holder, that only exposes the device area would solve such parastic etching. In addition, for such a holder, the exposed area is defined and the monitored current can lead to a better current density estimation.

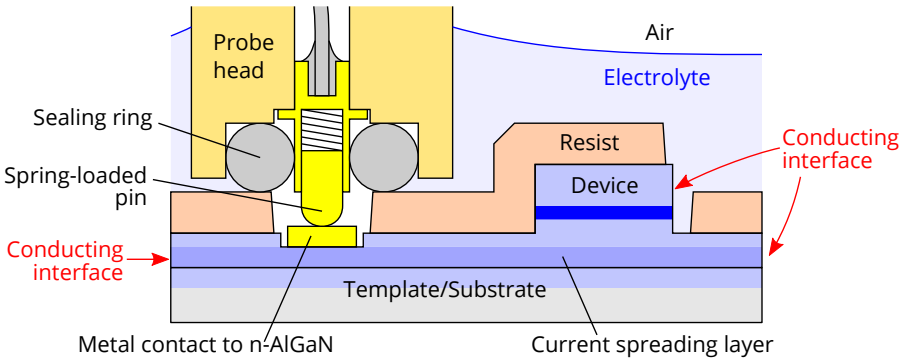

Figure 5.10: Schematic of the holder with a contacted sample.

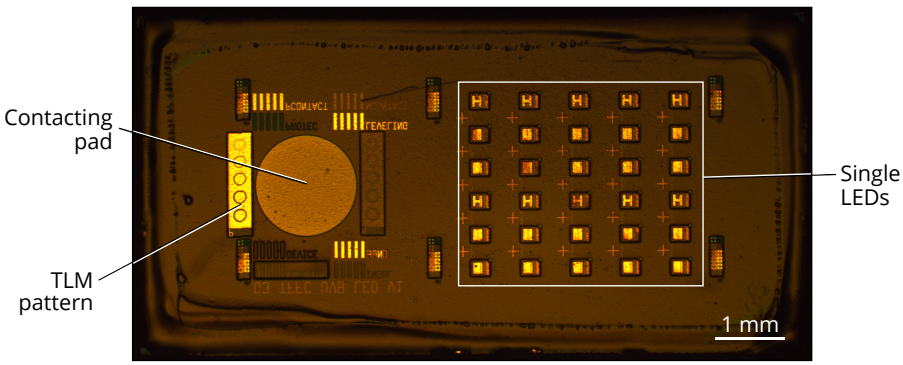

Figure 5.11: Microscope image of an UV LED sample before electrochemical etching.

5.5 Process control of electrochemical etching

Process control is a very crucial part of designing cleanroom processes to obtain a reliable result.

Monitoring the current during the electrochemical process to the remove the sacrificial layer gives a direct indication if etching occurs (see equation 5.1). However, additional processes happening at the anode side such as water oxidation can affect the charge transfer across the semiconductor/electrolyte interface. Assuming that only anodic oxidation of AlGaN/GaN occurs, the amount of the dissolved layer can be calculated using Faraday's law [90]. It has been shown that for a simple sample

design, the observed current correlates well with the evolution of the surface area of the sacrificial layer [90]. However, such a calculation is challenging for samples that include different device designs and an exposure of n-doped epitaxial layers at the sample perimeter. Furthermore, parasitic etching of other materials on the sample like metals, make it even harder to predict the amount of the removed sacrificial layer. Therefore, this method is only useful when the exposed surface and the material is known.

A common way to control the extent of the electrochemical etching is to time the process. This requires a known etch rate, which can be determined in a sample series. Unfortunately, the etch rate depends not only on the epitaxial structure but also on the etch conditions and the device geometry which could limit the electrolyte supply. It has been observed that if underetched layers buckle, as shown in Fig. 4.5, the etch rate increases due to an increased gap for the electrolyte supply. Because the buckling of the released layers depends on the device design, it is difficult to predict the etching time for more complex devices. Consecutive etching with inspection of the sample in between requires a drying step after each etching step, which through capillary forces exerts a force on the membrane each time. To reduce this force, the samples can be immersed in solvent such as isopropanol and subsequently dried in air. However, if the sample design includes protective resist layers during the electrochemical etching, as described in Section 5.3, the isopropanol partially removes the resist protection and re-etching is thus not possible. Restarting the etching after each step could also impede the etching conditions and result in a different morphology of the sacrificial layer compared to if the etching is done in one continuous step.

Instead of predicting the etching time or monitoring the current, optical in-situ monitoring can be used to control the process. In addition to process control it also offers more insight into the etching behaviour. It is regularly observed that even devices of the same design require different etching times which is attributed to a non-homogeneous current spreading across the sample. Adapting to such irregularities is impossible without in-situ monitoring. Monitoring samples in solution is challenging if the air/electrolyte interface is non-planar and the view is distorted. This is the case especially for monitoring small samples with devices close to the sample holder where the surface tension causes the electrolyte surface to rise as illustrated in Fig.5.10. To overcome this problem with a non-flat liquid surface over the sample, a special sample holder was developed with a minimal height profile allowing for it to be fully submerged near the sample, as illustrated in Fig. 5.12. The reduced

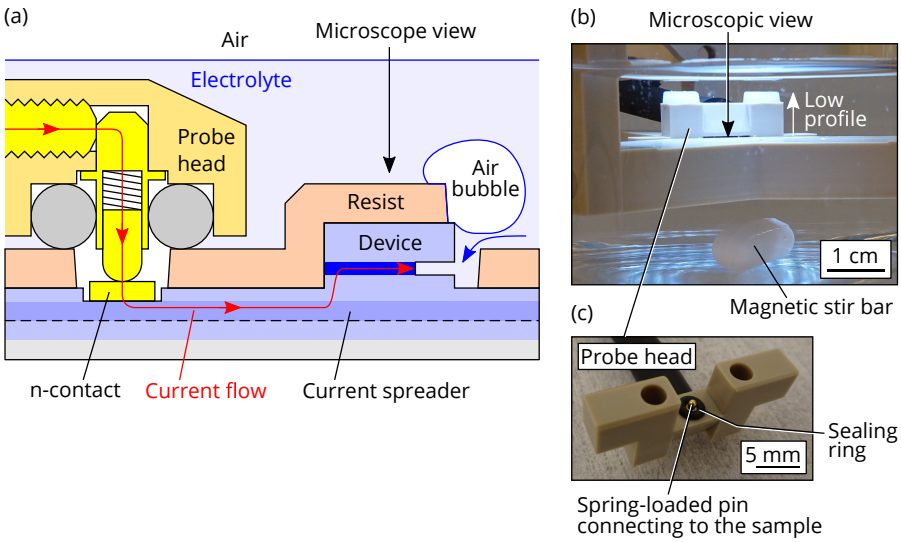

Figure 5.12: (a) Schematic of current supply and electrolyte supply with modified holder to improve distortion caused by the electrolyte surface during in in-situ monitoring, (b) picture of fully immersed sample holder yielding a flat electrolyte/air interface, and (c) picture of probe head.

distance between the sample and the electrolyte surface reduces distortions. As the solution is stirred during the etching, the resulting vortex can further lead to a turbulence in the solution impairing the view. However, the sample holder is additionally designed to break the vortex. During the etching process, gas is produced as part of the dissolution process. However, parasitic etching of metal layers usually leads to a much higher gas evolution and bubble size. The gas bubbles can stick to the sample surface and disturb the view or even prevent etching as illustrated in Fig. 5.12(a). This can be solved by gentle agitation of the solution. The bubble formation can also be supressed by adding substances to the electrolyte [50, 51, 105].

Even with the in-situ monitoring, it can be challenging to see the progress of the lateral etching because metal contact areas are blocking the view. Figure 5.13(a) shows the microscopic view on an LED array during electrochemical etching. The progress is usually still visible because underetched devices partially detach from the sample and slightly bend. Therefore, the changed reflection from these devices and cracks in the protective layer around the mesa compared to before the etching, as

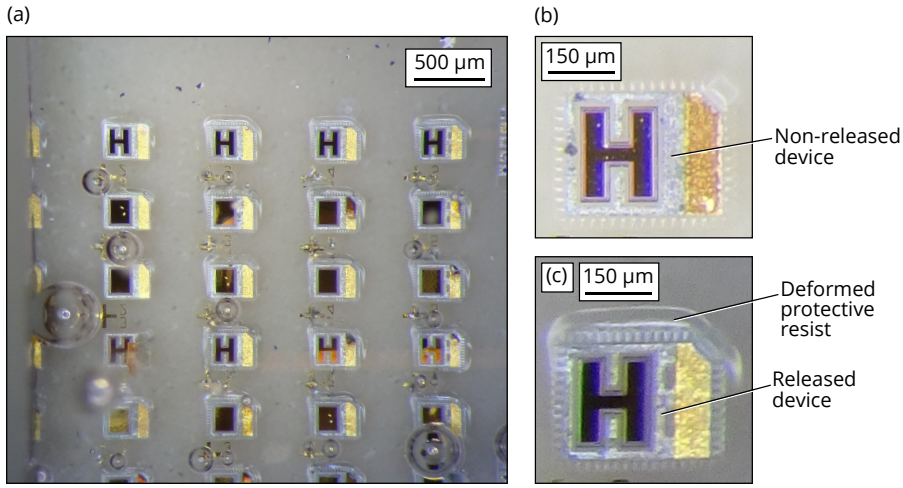

Figure 5.13: Microscopic view on (a) LED array during electrochemical etching, (b) non-released LED, and (c) released LED.

shown in Fig.5.13(b), can be observed (see Fig. 5.13(c)).

Chapter 6

TFFC UVB LEDs realized by electrochemical etching

The device design for TFFC LEDs using a lift-off based on electrochemical etching, consists of two principle parts: The first part is the LED including passivation and metallization, and the second part includes the layers that are required to achieve the lift-off. The goal is hereby to make these two parts as independent as possible to achieve the maximum performance of the LED and at the same time achieve a reliable release of the LED.

Therefore, the ideal sacrificial layer does not influence the crystal quality of the layers grown on top. The epitaxial structures used for the UVB LEDs in this work, mainly have layers with an Al content of around 50% and it is preferred to have the same Al content in the sacrificial layer. We have shown in [Paper A] that by choosing the right etching conditions, AlGaN layers with up to 50% Al can be completely removed. However, that result has to be treated with caution because not only the selectivity to the etch block layer has to be considered but also to other exposed devices layers, which can depending on the device design not completely be protected.

6.1 Epitaxial design

Based on the AlGaN etching series from [Paper A], first generation devices as demonstrated in [Paper B] used a sacrificial layer with 37% Al content. The 37% Al is sufficiently high to allow on-wafer testing for which the light is outcoupled through the substrate but it is low enough to allow a reliable electrochemical etching. For second generation devices, a sacrificial multi-layer with alternating $Al_{0.11}Ga_{0.89}N/Al_{0.37}Ga_{0.63}N$ layers was chosen to further facilitate the etching while maintaining an excellent growth quality.

To confine the electrochemical etching, the sacrificial layer was enclosed between etch block layers. Ideally, the top etch block layer is unintentionally doped to reduce parasitic etching into n-doped LED layers. However, depending on the TFFC design, the n-contact is formed on the top etch stop layer after flip-chip bonding as shown in [Paper B]. In such case, both the top and the bottom etch block layer were doped with $[\mathrm{Si}] = 0.5 \times 10^{18}\,\mathrm{cm}^{-3}$. In the later device generation with coplanar contacts as demonstrated in [Paper C], the top etch stop layer had no intentional doping. In all device generations, the bottom etch block layer was doped to $[\mathrm{Si}] = 0.5 \times 10^{18}\,\mathrm{cm}^{-3}$ to reduce any voltage drop during the electrochemical etching.

All samples shown in this work used a doping level of $[\mathrm{Si}] = 2 \times 10^{18}\,\mathrm{cm}^{-3}$ in the current spreading layer for EC etching.

6.2 Device process

Electrochemical release

The sacrificial layer was removed using electrochemical etching. Due to the lack of visual in-situ monitoring for early device generations, the etching time was chosen based on previous experiments and by monitoring the etching current. Etching for a longer time than required should not affect the etched surface because once the sacrificial layer is removed, the thin-film device is electrically disconnected. The lateral progression of the electrochemical etching of second generation devices that are presented in [Paper C] was monitored in-situ, as described in Section 5.5.

To keep the complexity of the LED fabrication process low, only a double mesa design was employed, which cannot protect all doped layers on top of the sacrificial layer, as shown in Fig. 6.1(a). Therefore the current spreading layer of the LEDs

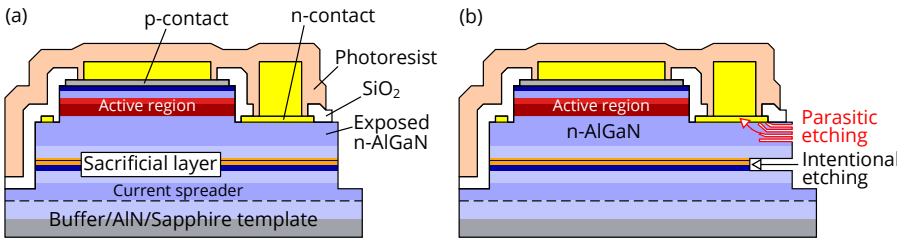

Figure 6.1: Incomplete protection of conductive layers using double-mesa design: (a) Before and (b) after the electrochemical etching.

can porosify laterally, which eventually leads to etching of the metal n-contact, as illustrated in Fig. 6.1(b). In this case, the enhanced etch rate of these metal layers results usually in a fully removed n-contact, which made the device unusable.

After electrochemical etching, the sample were immersed in de-ionized water to dissolve acids residues and the resist layer was stripped using acetone and isopropanol. In between the cleaning steps, the sample should stay immersed to prevent stiction and moving of the thin-film LED devices. After the sacrificial layer removal, the thin-film devices were only held by tethers and absolutely no process was done that applied any force on the membrane. The solvent cleaning frequently left resist residues because no agitation was used. O_2 plasma to further reduce the resist residues has lead to the detachment of single LEDs on first generation sample runs, which might have been caused by air streams during the venting of the process chamber. To prepare the sample for the flip-chip bonding, UV-ozone cleaning was used to remove remaining organic residues. No further detachment of devices at that stage was observed.

Tether design

In order to increase the tether strength, the mesa perimenter was increased by using a fin-like structure as highlighted by the white line in Fig. 6.2(b) and (c). To further increase the tether area, additional anchors were formed within the device area (see Fig. 6.2(c)). Despite the improved tether design, devices still moved after the removal of the protective resist. Future devices should use an improved tether design and material to achieve a higher device yield after electrochemical etching and sample cleaning. Thicker SiO_2 layers exceeding 1 µm could increase the strength but become impractical for deposition and patterning. Using more anchors within

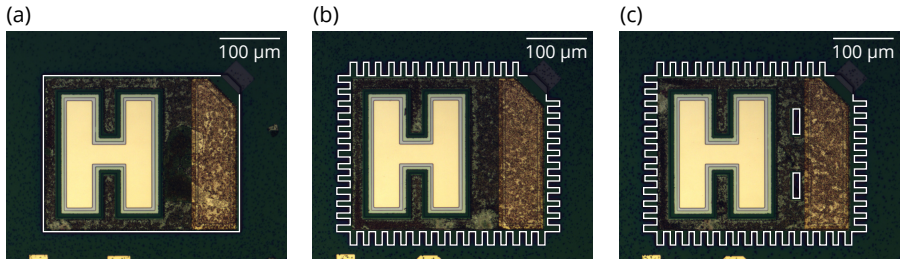

Figure 6.2: Comparison of different mesa designs with (a) a rectangular shape, (b) a rectangular shape and fins on the perimeters and (c) additional tethers within the device area. The white line highlights the outline of the mesa.

the devices reduces the device area and potentially affects the lateral removal of the sacrificial layer.

Carrier design and bonding

First generation TFFC LEDs based on type A, used a continuous Ti/Au bonding layer on the Si carrier. However, later TFFC LED generations required structured carriers to achieve a type B TFFC design. The carrier wafers were based on 3-inch Si wafers with a thermal oxide to insulate the individual bondpads. Whereas carrier chips that are used only for TFFC LEDs allow contacting at the individual LEDs, a carrier wafer for measuring FC-LEDs further requires metal lines to contact single LEDs which are buried below the sapphire substrate. To prevent short-circuits of the final devices, a SiO_2 layer is deposited on the metal lines. Due to the poor adhesion of the SiO_2 layer on the metal lines, a Ti interlayer between the Au of the metal lines and the SiO_2 is used. The first carrier chips to test flip-chip bonding used Ti/Au (10/600 nm) bondpads, which did not properly work if there were any particle preventing a sufficient contact. Therefore later generations employed electroplated Au bonding pads. To compensate for small deviations in height of the bondpads as well as not perfect leveling during bonding, the bondpads on the carrier chip are electroplated to a thickness of 3 µm to 4 µm. Electroplated bondpads on the device side are avoided because the required seed layer needs to be sputtered across all devices and the subsequent ion-milling to remove the seedlayer could be challenging.

Bonding tests have shown that the bonding force of the used flip-chip bonder is too little deform the continuous bondpads that covered full devices. As a result, the

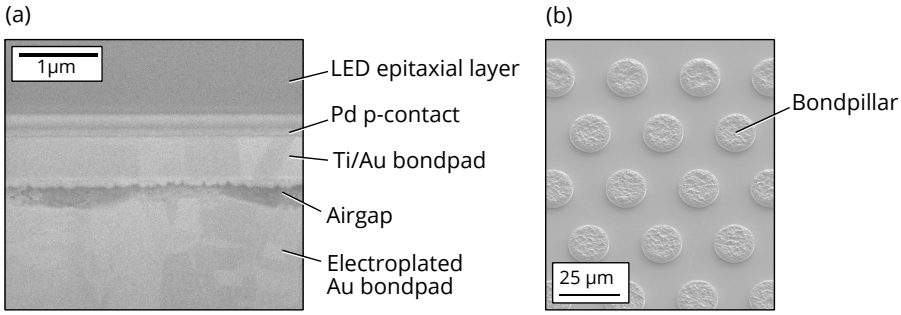

Figure 6.3: (a) Cross-sectional SEM image of incomplete thermocompression bond and (b) SEM image of bonding pillar array.

bonding is incomplete and leaves an airgap between TFFC LED and the carrier, which is shown in Fig. 6.3(a). It also shows the significant surface roughness of the electroplated bondpad. To increase the pressure during bonding, the bondpad area on the carrier side was reduced by using bonding pillars with a diameter of 15 µm as shown in Fig. 6.3(b). Bonding pillars also showed an improved deformation during the bonding and therefore adapt better to the bonded device. However, ideally the bondpad spreads across the whole active region area of the TFFC LED to maximize the heat conduction to the substrate. As a last step, the carrier wafer was diced into $10\,\text{mm} \times 10\,\text{mm}$ samples for the chip-level bond and a convenient sample handling for subsequent processing.

Roughening

The TFFC design provides access to the N-polar top surface of the LED for surface texturing, which is usually achieved using KOH, to increase the light extraction. Because only a number of LEDs per chip were roughened, a lithography step is done to protect the LEDs which should not be roughened. For the exposure, direct laser writing (DLW) was used to prevent damage of the bonded devices due to contact lithography. DLW also gives the flexibility in the exposure pattern, which needs to be adjusted if the position of LEDs after transferring deviates from the mask design. It was observed that already the development to expose single LEDs caused a major roughening of the N-polar surface. Therefore, it was decided only use the TMAH-based developer for further roughening, which yielded a surface texture as shown in Fig. 6.4(a) and (b). Because the resist development did not proceed completely

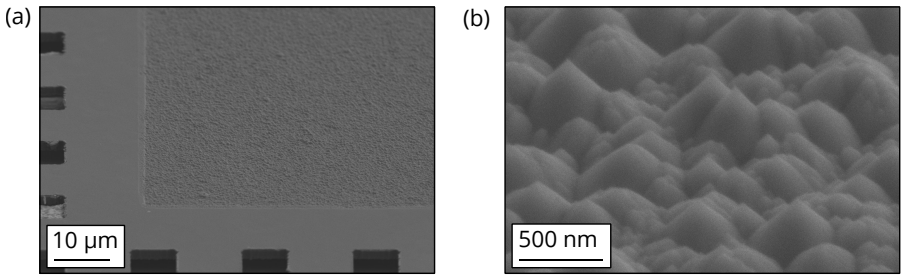

Figure 6.4: (a) SEM image of partially roughened N-polar AlGaN surface and (b) single cones achieved by the wet etching.

homogeneous, also the surface roughening proceeded inhomogeneously. Therefore, single devices showed a different degree of surface roughening. To avoid inhomogeneous roughening by separating development and roughening, a developer should be chosen that does not attack the surface.

The easy roughening of the N-polar AlGaN surface has to be kept in mind when doing lithography steps using a TMAH-based developer on the N-polar surface.

Chapter 7

Summary and future directions

7.1 Summary

This work has demonstrated the realization of TFFC UVB LEDs based on substrate removal using electrochemical etching of AlGaN. Key steps that enabled such a substrate removal were the development of electrochemical etching of AlGaN with up to 50% Al-content and measures in epitaxial and device design to prevent parasitic etching of the LED. In addition, device structures such a tethers and bonding layer to enable flip-chip bonding were developed.

In the study to find suitable conditions to etch AlGaN with different Al-composition, shown in [Paper A], it was found that AlGaN with up to 50% Al content can be completely etched using 0.3 M nitric acid at a bias voltage of 30 V.

This formed the basis to develop a substrate removal technique for UVB LEDs with a proper encapsulation of the doped device layers and metal contacts to prevent parasitic etching, as demonstrated in [Paper B] and [Paper C]. Using a sacrificial layer with alternating low and high Al contents resulted in a reliable and complete removal of the sacrificial layer while still offering the growth of a high crystal quality device structure on top of the sacrificial layer. An in-situ monitoring setup allowed for improved process control to time the etching and gave further insights into the etching process to study etching delays, homogeneity, parasitic etching and bubble formation. Parasitic etching was prevented by a combination of an epitaxially grown

etch block layer between the device layers and the sacrificial layers. A protective SiO_2/resist layer on top of the devices was used to prevent the contacts from being exposed to the electrolyte and to encapsulate conducting n- and p-doped device layers. By choosing a proper mesa design, a controlled unidirectional etching across the device was accomplished, which minimized etch residues.

Based on the aforementioned process development, UVB LEDs with a coplanar contacting scheme were fabricated. Flip-chip thermocompression bonding based on Au-Au bonding layers was used to achieve a multi device transfer to a metallized Si carrier chip. The device process of the thin-film flip-chip LED was completed by surface roughening using TMAH-based wet etching, which lead to an enhancement in the emission power in the order of 45%. These result are included in [Paper C].

7.2 Future directions

UVB LEDs

We have developed a new technology platform to realize thin-film flip-chip UVBs with the potential to greatly improve the light extraction efficiency in these devices. To push the power conversion efficiency of these devices to that of the power efficient blue LEDs, efforts and progress are required in all areas highlighted in Fig. 3.1 as well as in improving the voltage efficiency. Our demonstration of TFFC UVB LEDs through electrochemical etching are the first of their kind, thus leaving some room for improvement in for example process yield, optimized surface roughness, highly reflective p-contacts, and an optically transparent p-side of the LED to use the full potential of the method to increase the light extraction efficency.

To increase the process yield, both the prevention of parasitic etching of the LED and the bonding uniformity must be improved. To fully prevent parasitic etching, all doped LED layers should be encapsulated and that would require a three-step mesa instead of the two-step mesa used in this work. However, to make this TFFC approach appealing, one should not increase the process complexity by introducing another lithography and dry etch step. A way to achieve a three-step mesa with only two dry-etch steps that overlap to achieve a third depth, is illustrated in Fig. 7.1(a) to (c). Note that for this concept to work, the step height between the epitaxial top surface and n-contact LED layer must be larger than the step height between top etch block and bottom etch block layer.

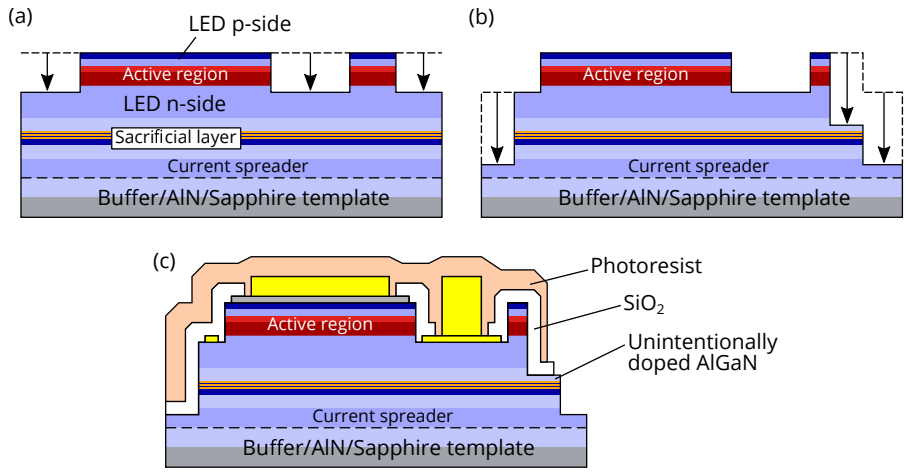

Figure 7.1: A two etch steps process to achieve a three-step mesa required to fully protect the doped LED layers during electrochemical etching. (a) First dry etch step. (b) Second dry etch step. (c) All doped LED and metal layers are fully encapsulated between SiO_2, photoresist and unintentionally doped AlGaN layers.

Aligned bonding is crucial for advanced device designs and post-processing of transferred devices. However, incomplete bonding reduces the device yield and degrades device performance. In TFFC LEDs, the bond keeps the devices in place but is also crucial for current injection and heat sinking. In lasers, that operate at much higher current densities than LEDs (kA/cm^2 instead of 10's of A/cm^2), heat sinking is even more important. Thus improving the bonding by optimizing the uniformity of the bonding pressure and choice of the bonding layers will be required for high performing devices.

Surface roughening has clearly shown to be important to increase the light extraction efficiency. In our devices there is room for improvement in optimizing the surface structures as well as in achieving the same degree of roughness across all exposed devices during the wet etching. We used photolithography to selectively roughen a few devices at a time, but the TMAH-based developer also roughened the devices leaving less flexibility in optimizing the surface roughness.

To fully benefit from a TFFC design and boost the LEE, both a fully transparent p-side of the LED as well as a highly reflective p-side are desired. Tunnel junctions

could offer a solution to both. They allow for the use of an n-doped transparent current spreading AlGaN-layer on top of the LED structure instead of a poorly conductive and optically absorbing p-GaN/AlGaN and thereby gives more flexibility in the contact shape and placement. Low resistive contacts are also easier to form on n-AlGaN than p-AlGaN. By decoupling the electrical contact from the desired high reflectivity of the p-side leaves many more options for the reflector material being either metal or multi-layered dielectrics such as a distributed Bragg reflector (DBR).

Electrochemical etching of high Al-containing AlGaN and the realization of TFFC UVC LEDs

Many important applications such as water purification require ultraviolet light in the UVC wavelength range. Therefore, extending the developed device platform towards shorter wavelength is crucial. In such UVC LEDs, usually Al contents above 50% are needed and suitable conditions for the electrochemical etching need to be explored to achieve a substrate removal. To facilitate the electrochemical etching for these high Al contents, demonstrated concepts such as the multilayered sacrificial layer is a promising solution but needs further refinement.

New and improved devices enabled by electrochemical etching of AlGaN

The demonstration of selective lateral etching of AlGaN opens up many new possibilities for devices besides LEDs. The TFFC technology platform that has been developed for UVB LEDs can for example enable electrically-injected UV VCSELs with a double dielectric DBR scheme. This is a device concept that circumvents the increasing difficulty of achieving high reflectivity broadband epitaxial DBRs in AlGaN with increasing Al-content. The ability of the technology to lift-off very smooth doped AlGaN-membranes with precise thickness control could also be explored for embedded AlGaN waveguides for UV photonic integrated circuits where also the non-linear properties of AlGaN could be utilized. It would also be of interest to create free-hanging mechanical, opto-mechanical or micro-electro-mechanical or electro-opto-mechanical systems benefiting from the piezoelectric properties of AlGaN, its wide transparency window and chemical inertness with the ability to withstand harsh environments. The technology could also be used to create high-quality high-power high-electron mobility transistors that could be placed on any material of choice with a high thermal conductivity. This is just the beginning of the realization and utilization of AlGaN membranes for a wide variety of devices based

on this technology platform.

Chapter 8

Summary of papers

Paper A

Electrochemical etching of AlGaN for the realization of thin-film devices

Michael A. Bergmann, Johannes Enslin, Rinat Yapparov, Filip Hjort, Björn Wickman, Saulius Marcinkevičius, Tim Wernicke, Michael Kneissl, and Åsa Haglund

Applied Physics Letters, vol. 115, issue 18, p. 182103, 2019.

First time demonstration of complete electrochemical etching of a sacrificial AlGaN layer with up to 50% Al-composition. The sacrificial AlGaN-layer morphology after electrochemical etching depends on the applied etch voltage in a similar way as electrochemically etched GaN, and the Al-composition has a strong influence on the required voltage needed to achieve complete etching. The etched N-polar surface shows the same macroscopic topography as that of the as-grown epitaxial structure, and the root-mean square roughness is 3.5 nm for $1\,\mu m \times 1\,\mu m$ scan areas. Separated device layers have a well-defined thickness and smooth etched surfaces. Transferred multi-quantum-well structures were fabricated and investigated by time-resolved photoluminescence measurements. The quantum wells showed no sign of degradation caused by the thin-film process.

My contribution: I identified electrochemical (EC) etching as a promising technology for creating GaN membranes and further developed this etch technique to also be able to etch AlGaN with high Al-compositions and create AlGaN membranes. I designed and built the EC etching cell and sample holder and choose suitable etch conditions (etch voltage, choice of electrolyte and concentration). I also contributed to the epitaxial design (sacrificial layer and etch block layer designs) together with the group at TUB and did the sample layout design and processing including the EC etching of all the samples. I did the characterization of the membranes by SEM and AFM and wrote the manuscript with feedback from the co-authors.

Paper B

Thin-film flip-chip UVB LEDs realized by electrochemical etching

Michael A. Bergmann, Johannes Enslin, Filip Hjort, Tim Wernicke, Michael Kneissl, and Åsa Haglund

Applied Physics Letters, vol. 116, issue 12, p. 121101, 2020.

First time demonstration of a thin-film flip-chip (TFFC) UVB LED where the substrate has been removed by electrochemical etching. This is an important step toward improving the light extraction efficiency that limits the power conversion efficiency in AlGaN-based LEDs. The electroluminescence spectrum of the TFFC LED corresponds well to that of the as-grown LED structure, showing no sign of degradation of structural and optical properties by electrochemical etching. This is achieved by a proper epitaxial design of the sacrificial layer and the etch stop layers in relation to the LED structure and the electrochemical etch conditions.

My contribution: Based on the results from [Paper A], I contributed to the epitaxial design of sacrificial layer and etch block layers together with the group at TUB. I, together with Filip Hjort, did the device layout design, developed the process flow and the thermocompression bonding technique, processed the LEDs including the EC etching where I selected the suitable etch conditions and did the tranfer of the devices. I did the electrical and optical characterization of the LEDs as well as the investigation by SEM and optical microscopy and wrote the manuscript with feedback from the co-authors.

Paper C

High-efficiency UVB LEDs using a thin-film flip-chip design and surface roughening

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Manuscript.

TFFC LEDs are demonstrated where the LEDs are fabricated by a standard LED device process flow, which is followed by a substrate removal and flip-chip bonding of the devices. The thin-film device realization is enabled by a proper sample layout in combination with the right epitaxial design of the sacrificial layer and etch block layers in relation to the device structure. The device performance is compared for TFFC LEDs with and without surface roughening, demonstrating the impact of the surface roughening on the light extraction efficiency and thereby the overall power conversion efficiency.

My contribution: I contributed to the epitaxial design of different sacrificial layers and etch block layers that were explored together with the group at TUB. I did the device layout and carrier design, most of the process steps for the LEDs (p-contacts, metal leveling layer, bondpads, insulation, and etch protection) including the EC etching where I selected suitable etch conditions. In addition, I developed the selective surface roughening step for the LEDs as well as the design and full processing of the carrier chips. I developed the thermocompressive bonding with pillars instead of planar layers and did the bonding of LEDs to carrier wafer. I did the initial electrical and optical characterization of the LEDs as well as the investigation by SEM and optical microscopy and wrote the manuscript with feedback from the co-authors.

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Papers A–C