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A power cycling degradation inspector of power semiconductor devices

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Abstract

We have proposed a failure analysis based on a real-time monitoring of power devices under acceleration test. The real-time monitoring enables to visualize the mechanism that leads to a failure by obtaining the change of structure inside the device in time domain with high spatial resolution. In this paper, we presented a new analytical instrument based on the proposed failure analysis concept. The essential functions of this instrument are (1) power stress control, (2) non-destructive inspection and (3) water circulation. An original design power-stress control system and a customized scanning acoustic microscopy system enable us a non-destructive inspection inside the device under power cycling test. This instrument exhibits a great advantage especially to monitor failure mechanisms without having to open the module.

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1. Failure analysis based on a real-time monitoring

Power semiconductors have improved the mass productivity by reducing the chip area and have met to the enormous demand accompanying the spread of energy-saving products. On the other hand, the current density and electric field inside the device are increased and the risk of failure is increasing. Due to the conflicting demands of improvement in mass productivity and low failure rate, ensuring the reliability of power semiconductors is becoming difficult.

Failure of power semiconductor involves three factors: applied stress called mission profile, structure of chip and package, and material used in the device. In order to ensure reliability, we have made full use of utilization of knowledge obtained from past failure, reproduction of failure by accelerated test and estimation of failure rate, and failure analysis (FA) by observation [1-10]. However, as mentioned above, the current density and internal electric field in the device have increased in recent years. In addition, the insulation and the wiring structure have become complicated. Therefore, it becomes difficult to ensure sufficient reliability with the conventional methods.

We have proposed a failure analysis based on a real-time monitoring [11,12]. The real-time monitoring is a tool to observe the primary failure at micro level in time and space. In other words, it enables to visualize the mechanism that leads to a failure by obtaining the change of structure inside the device, current distribution, electromagnetic field distribution and temperature distribution in time domain with high spatial resolution [11-16]. For example, in the conventional analysis represented FA, the cause of failure is determined by static observation with opening the failed device. On the other hand, in the real-time monitoring, microscopic phenomena which can be cause of failure is dynamically observed in time series before a failure occurs. The real-time monitoring has a great advantage for extraction of the relationship between

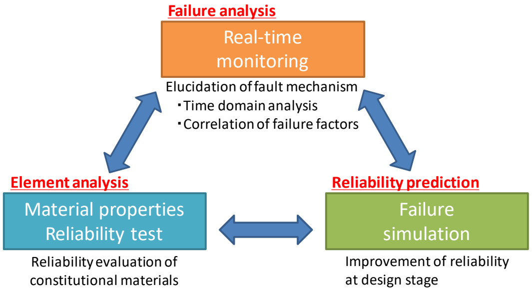

Fig. 1. Method for enhancing reliability of a power semiconductor based on a real-time monitoring.

physical properties of constitutional materials and degradation phenomena inside the device or extraction of phenomena that cannot be modelled in simulation. Therefore, the real-time monitoring proposes a clear spec for materials and a new evaluation method for material development, and also it opens the way to the development of a highly accurate simulation model (see Fig. 1).

2. New analytical instrument

In this paper, we introduce a power cycling test inspector for power devices. This instrument was developed based on knowledge obtained by a test model. The essential functions of this instrument are (1) power stress control, (2) non-destructive inspection and (3) water circulation. Fig. 2 shows the components. This instrument exhibits an advantage especially to monitor failure mechanisms without having to open the module.

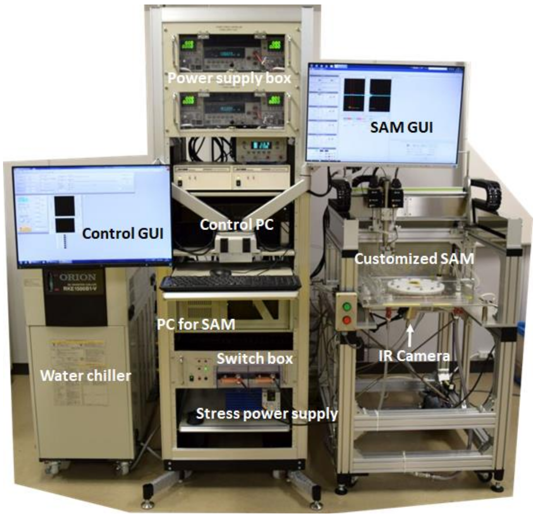

Fig. 2. Components of the power cycling test inspector.

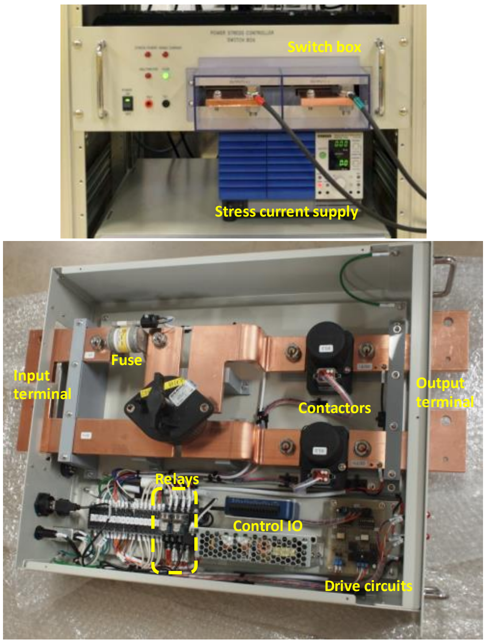

Fig. 3. Switch box.

Fig. 4. Power supply box.

2.1. Power stress control

We designed a power stress controller for the system. The power stress controller was consisted of a switch box and a power supply box. The switch box includes two switching lines, one is for applying stress current and the other is for measuring a temperature sensitive parameter (TSP) (see Fig. 3). The stress current line is composed of copper bus bars and DC contactors to apply a stress current of 500A. The input of stress line is arranged on the back of the controller so that a power supply can be changed according to the required power stress. The load current range and minimum load pulse duration is depend on a power supply and switching speed of the DC contactors. The stress power supply output terminal is arranged on the front side. A signal from PC controls the contactors and this system enables mechanically isolation of the DUT from the stress current line.

An on-state voltage drop at low current is used as TSP. A small-current supply and a digital voltmeter for the TSP measurement is mounted in the power supply box (see Fig. 4). These are connected to the output terminal of stress current line through relays so that we can safely isolate them from the stress current line when applying stress to the DUT. The drivers for contactors and relays forms using MOSFETs to prevent malfunction due to noise and they are optically insulated from the control interface. The timing to switch the contactors in the stress current line and the relays for TSP measurement are controlled by a PC. The power stress and the switching sequence is programed through an original GUI written by LabVIEW (National Instruments).

A power supply to drive the gate of DUT also mounted in the power supply box. The output of it is also provided on the front of the switch box. Because the output of power supplies and the input for measurement of the power stress control are integrated to the switch box, a wiring to the DUT is basically possible with three cables. By adding a set of a power supply for stress current, a switch box and a power supply box, the system can apply to multiple DUTs.

2.2. Non-destructive inspection

For non-destructive inspection of inside DUTs, we employed a scanning acoustic microscopy (SAM). The SAM enables non-destructive observation inside power devices with fine resolution using ultrasonic [1-6]. We designed a new SAM system based on a commercial model (Insight K.K.). A mechanical part of the system employs an open style shape to ensure a wide space under the DUT for wiring and observation.

The DUT is fixed at the bottom of a water tank for observation by epoxy resin. An observation surface of the DUT is exposed to water (see Fig. 5). When this surface and an electrode of the DUT is common, the stress current is applied with this electrode grounded. Therefore, the SAM inspection is possible even under power stress applied. As the start and stop of scanning is controlled with external signals, an acquisition of images can be completely synchronized with the power cycle. The acquisition time of SAM image depends on scan area and scan speed. To ensure the sufficient acquisition time, e.g. it is 90 sec. for 55 × 12 mm^2 with 0.05mm pitch, the image was usually taken in the cooling interval of each cycle. The obtained images are automatically stored in a specified folder of the PC. The system is equipped with two transducers. This dual scanner system enables to observe different place at same time and to improve the image acquisition speed. Moreover, it also enables to analyse two interfaces with optimal focus.

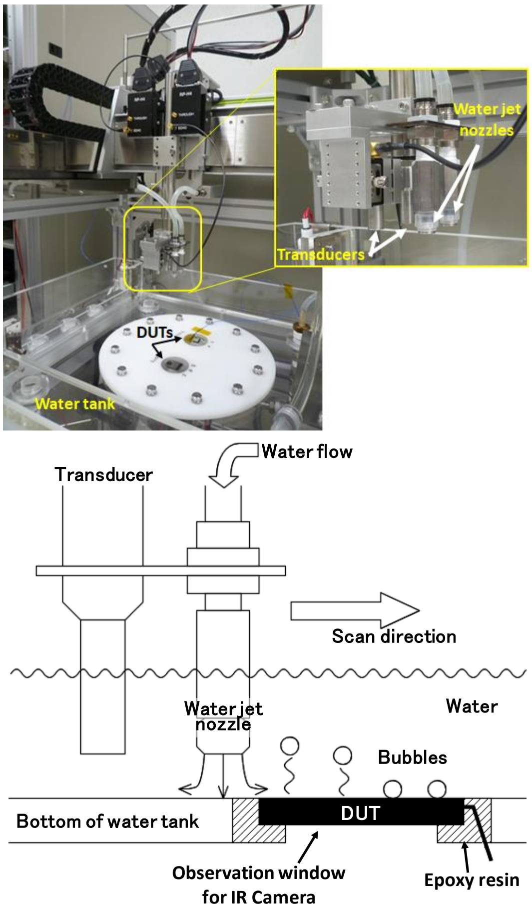

Fig. 5. Observation stage of SAM with dual scanner and schematic of DUT setup.

2.3. Water circulation

A couplant water is necessary for the SAM observation and the water plays two important roles of our system. One is a DUT cooling and the other is a bubble removing. An additional structure for device cooling perturbs ultrasonic wave transmission. Therefore, water cooling using the couplant water was employed for DUT cooling. To obtain high efficiency of the cooling, a cooled water is directly circulated into a water tank for the SAM observation and the water tank was designed to maintain the water depth. The system can be applied up to 5.8kW device because the cooling capability of the water chiller.

Small bubbles on the DUT surface generated by self-heating of the DUT also perturbed ultrasonic wave transmission. To solve this problem, the water jet was also effective to sweep away the bubbles [11, 12]. The couplant water is introduced to a nozzle attached at the ultrasonic transducer by using a small pump and a water jet is generated forward the direction of the scan. The switching of the water jet also can be controlled by the PC to generate the water jet when the scan starts.

2.4. Another features

The temperature of base plate of DUT, circulated water and the package is also monitored. A fiber optic temperature sensor is attached to a surface of the base plate and the inside wall of the water tank. Temperature of the package is monitored by an Infrared camera through an open window at the back side of the DUT. This side was painted black to control of the surface emissivity.

3. Discussion

Fig. 6 shows an example of obtained data. We confirmed that the system stably operated over 3000 continuous cycles (over 108 hours). In this case, the image change was gradually occurred at the chip top area. For automatic detection of such slight image change, an analysis using image processing is effective [12]. Moreover, such image change have to be related to a degradation phenomenon inside the device for the failure analysis.

There is a need to improve the chip temperature monitoring and the device cooling system. As for chip temperature monitoring by TSP, there is an error of monitored maximum temperature originate from data acquisition timing. Moreover, as the measurement needs to wait for the end of the relays switching (< 100 ms), it is need to a compensation for this delay, e.g. an extrapolation from decay of TSP curve, to estimate the maximum temperature of the chip [17]. As for the device cooling system by the water circulation, the thermal diffusion in the DUT is different from a conventional heat sink. Especially, the image acquisition with water jet sometime results in excessive cooling shown in Fig. 6. Therefore, the cooling condition should be adjusted to represent a specific failure mode.

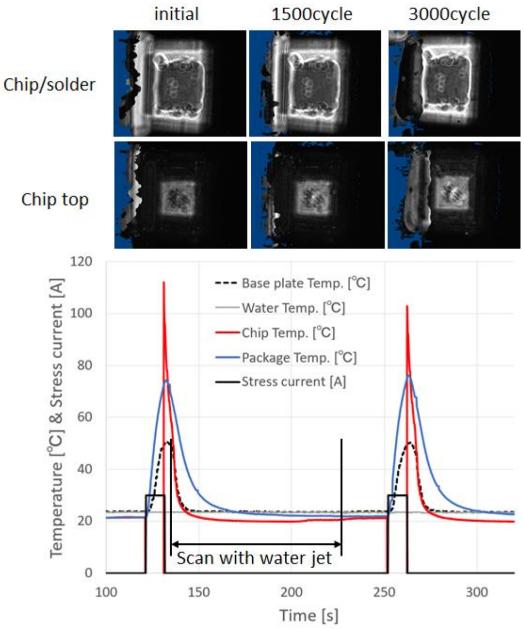

Fig. 6. Example of recorded Data.

4. Conclusions

We developed a new analytical instrument of power device based on a concept of real-time monitoring based failure analysis. An original design power-stress control system and a customized scanning acoustic microscopy system enable us a non-destructive inspection inside the device under power cycling test. By using this system, the microscopic phenomena which can be cause of failure is dynamically observed in time series before a failure occurs. The system can apply not only failure analysis of power devices but also degradation test of constitutional materials of devices. We believe the system make a significant contribution for extraction of the relationship between physical properties of materials and degradation phenomena inside the device or extraction of phenomena that cannot be modelled in simulation.

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References

[1] L. Feller, S. Hartmann, D. Schneider, Lifetime analysis

of solder joints in high power IGBT modules for increasing the reliability for operation at 150 °C, Microelectron. Reliab. 48 (2008) 1161-1166.

[2] T. Chung, J. Jhang, J. Chen, Y. Lo, G. Ho, M. Wu and C. Sun, A study of large area die bonding materials and their corresponding mechanical and thermal properties, Microelectron. Reliab. 52 (2012) 872-877.

[3] P. Mario, M. Josef and I. Michael, Inverted high frequency Scanning Acoustic Microscopy inspection of power semiconductor devices, Microelectron. Reliab. 52 (2012) 2115-2119.

[4] U.M. Choi, F. Blaabjerg, S. Jørgensen, F. Iannuzzo, H.Wang, C. Uhrenfeldt, S. Munk-Nielsen, Power cycling test and failure analysis of molded Intelligent Power IGBT Module under different temperature swing durations, Microelectron. Reliab. 64 (2016) 403-408.

[5] C. Durand, M. Klingler, M. Bigerelle, D. Coutellier, Solder fatigue failures in a new designed power module under Power Cycling, Microelectron. Reliab. 66 (2016) 122-133.

[6] M. Junghaenel, U. Scheuermann, Impact of load pulse duration on power cycling lifetime of chip interconnection solder joints, Microelectron. Reliab. 76-77 (2017) 480-484.

[7] P. Cova, N. Delmonte and D. Chiozzi, Numerical analysis and experimental tests for solder joints power cycling optimization, Microelectron. Reliab. 55 (2015) 2036-2040.

[8] A. Ibrahim, J.P. Ousten, R. Lallemand, Z. Khatir, Power cycling issues and challenges of SiC-MOSFET power modules in high temperature conditions, Microelectron. Reliab. 58 (2016) 204-210.

[9] C. Herold, J. Franke, R. Bhojani, A. Schleicher, J. Lutz, Requirements in power cycling for precise lifetime estimation, Microelectron. Reliab. 58 (2016) 82-89.

[10] U.M. Choi, F. Blaabjerg and F. Iannuzzo, Advanced power cycler with intelligent monitoring strategy of IGBT module under test, Microelectron. Reliab. 76-77 (2017) 522-526.

[11] A. Watanabe, M. Tsukuda, I. Omura, Failure analysis of power devices based on real-time monitoring, Microelectron. Reliab. 55 (2015) 2032–2035.

[12] A. Watanabe, R. Nagao, I. Omura, Real-time imaging of temperature distribution inside a power device under a power cycling test, Microelectron. Reliab. 76-77 (2017) 490-494.

[13] H. Shiratuchi, K. Matsushita, I. Omura, IGBT chip current imaging system by scanning local magnetic field, Microelectron. Reliab. 53 (2013) 1409-1412.

[14] H. Shiratuchi, K. Matsushita, I. Omura, IGBT chip current imaging system by scanning local magnetic field, Microelectron. Reliab. 53 (2013) 1409-1412.

[15] N. Hirata, A. Watanabe, I. Omura, High Speed Real-time Temperature Monitoring System inside Power Devices Package Using Infrared Radiation, Proc. of 2014 International Conference on Solid State Devices and Materials (2014) 1016-1017.

[16] M. Tsukuda, K. Matsuo, H. Tomonaga, S. Okoda, N. Ryuzo, K. Tashiro, I. Omura, Magnetic Flux Signal Simulation with 16-channel Sensor Array to Specify Accurate IGBT Current Distribution, Proc. of International Conference on Integrated Power Electronics Systems (2016) 264-268.

[17] W. Chen, J. Franke, C. Herold, R. Bhojani, J. Lutz, Internal processes in power semiconductors at virtual junction temperature measurement, Microelectron. Reliab. 64 (2016) 464-468.